RESEARCH AND DESIGN OF HIGH-SPEED ADVANCED ANALOGUE FRONT-ENDS FOR FIBRE-OPTIC TRANSMISSION SYSTEMS

BY

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Nasir Abdul Quadir

Cork, Ireland

ABSTRACT

In the last decade, we have witnessed the emergence of large, warehouse-scale data centres which have enabled new internet-based software applications such as cloud computing, search engines, social media, e-government etc. Such data centres consist of large collections of servers interconnected using short-reach (reach up to a few hundred meters) optical interconnect. Today, transceivers for these applications achieve up to 100Gb/s by multiplexing 10x 10Gb/s or 4x 25Gb/s channels. In the near future however, data centre operators have expressed a need for optical links which can support 400Gb/s up to 1 Tb/s. The crucial challenge is to achieve this in the same footprint (same transceiver module) and with similar power consumption as today's technology. Straightforward scaling of the currently used space or wavelength division multiplexing may be difficult to achieve: indeed a 1Tb/s transceiver would require integration of 40 VCSELs (vertical cavity surface emitting laser diode, widely used for short-reach optical interconnect), 40 photodiodes and the electronics operating at 25Gb/s in the same module as today's 100Gb/s transceiver. Pushing the bit rate on such links beyond today's commercially available 100Gb/s/fibre will require new generations of VCSELs and their driver and receiver electronics. This work looks into a number of state-of-the-art technologies and investigates their performance restraints and recommends different set of designs, specifically targeting multilevel modulation formats.

Several methods to extend the bandwidth using deep submicron (65nm and 28nm) CMOS technology are explored in this work, while also maintaining a focus upon reducing power consumption and chip area. The techniques used were pre-emphasis in rising and falling edges of the signal and bandwidth extensions by inductive peaking and different local feedback techniques. These techniques have been applied to a transmitter and receiver developed for advanced modulation formats such as PAM-4 (4 level pulse amplitude modulation). Such modulation format can increase the throughput per individual channel, which helps to overcome the challenges mentioned above to realize 400Gb/s to 1Tb/s transceivers.

STATEMENT OF ORIGINALITY

I hereby certify that I am the sole author of this thesis. Except where indicated, all the work presented in this thesis is solely attributed to the author. Precise details of collaborators may be ascertained from the list of co-authors in the *List of Publications*.

I declare that this is a true copy of my thesis and has not been submitted for another degree to any other University or Institution.

LIST OF PUBLICATIONS

JOURNALS

J1. P. Ossieur, **N.A. Quadir**, S. Porto, C. Antony, W. Han, M. Rensing, P. O'Brien and P.D. Townsend, "A 10Gb/s linear burst-mode receiver in 0.25µm SiGe BiCMOS", *IEEE Journal of Solid State Circuits*, 2013. 48(2): p. 381-390.

J2. P. Ossieur**, N. A. Quadir**, S. Porto, M. Rensing, C. Antony, P. O'Brien, Y (Frank) Chang, and P. D. Townsend, "A 10G Linear Burst-Mode Receiver Supporting Electronic Dispersion Compensation for Extended-Reach Optical Links, " *Optics Express*, vol. 19, iss. 26, pp. 604–B10, Dec 2011.

J3. M.V. Krishna, A. Jain, **N.A. Quadir**, P.D. Townsend and P. Ossieur, "Progammable multi-modulus frequency dividers using Low Power True Single-Phase Clocked CMOS 2/3 and 4/5 Dividers, " in preparation for submission to *Transactions on Circuits and Systems-I*.

CONFERENCES

C1. **N. A. Quadir**, P. D. Townsend and P. Ossieur, "An inductorless linear optical receiver for 20Gbaud (40Gb/s) PAM-4 modulation using 28nm CMOS", submitted to *ISCAS 2014* Melbourne.

C2. **N.A. Quadir**, P.D. Townsend and P. Ossieur, "Design of a 40Gb/s, 20Gbaud PAM-4 VCSEL Driver with Digitally Programmable Bias and Modulation Currents using 65nm CMOS", submitted to *ISCAS 2014* Melbourne.

C3. P. Ossieur, S. Porto, C. Antony, A. Jain, D. Kelly, **N.A. Quadir**, G. Talli and P.D. Townsend "Burst-mode electronic dispersion compensation", (invited) in *Proceedings Optical Fiber Conference* (OFC'2014), San Francisco, USA, March 2014.

C4. **N. Quadir**, P.D. Townsend and P. Ossieur, "Feasibility of a small footprint linear optical receiver for 50Gb/s PAM-4 using 28nm CMOS". *Photonics Ireland Conference,* Belfast 2013.

C5. P. Ossieur, C. Antony, A. Naughton, S. Porto, **N.A. Quadir**, A.M. Clarke and P.D. Townsend, "Hybrid DWDM-TDMA PONs for Next Generation Access, " (invited) in *Proceedings Optical Fiber Conference* (OFC'2012), Paper OW1B.7, Los Angeles, USA, March 2012.

C6. **N. Quadir**, P. Ossieur and P. D. Townsend, "A 56Gb/s PAM-4 VCSEL driver circuit" , *ISSC 2012*, NUI Maynooth, June 28-29.

C7. P. Ossieur, **N.A. Quadir**, S. Porto, M. Rensing, C. Antony, W. Han, P. O'Brien and P.D. Townsend, "A 10Gb/s linear burst-mode receiver", *Irish Systems and Signals Conference 2012*, Maynooth, Ireland, June.

C8. P. Ossieur, **N.A Quadir**, S. Porto, M. Rensing, C. Antony, W. Han, P.O. Brien, Y. (Frank) Chang and P.D. Townsend, "A 10G linear burst-mode receiver supporting electronic dispersion compensation for extended-reach optical links, " *European Conference on Optical Communication* (ECOC'2011), Postdeadline Paper Th.13.B.4, Geneva, Switzerland, Sept. 2011.

C9. P. Ossieur, M. Rensing, M. Mulcahy, W. Han, P. O'Brien, **N. A Quadir**, A. Jain and P. D. Townsend, "Packaging technology for a 10Gb/s burst-mode receiver", *Photonics Ireland 2011 Conference*, Dublin, Ireland.

C10. **N. A. Quadir**, A. Jain, P. Ossieur and P.D. Townsend, "Low-power, high speed CMOS driver circuits for high-capacity, short-reach optical data-links", *Photonics Ireland 2011 Conference*, Dublin, Ireland.

LIST OF ACRONYMS

AC	Alternating Current
ADC	analogue-to-digital converter
ADSL	Asymmetric digital subscriber line
AGC	Automatic Gain Control
APD	Avalanche Photo Diode
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BIMMF	Bend Insensitive Multi-Mode Fibre
CAPEX	Capital Expenditure
CATV	Cable Television
CM	Common Mode
CMFB	Common Mode Feed Back
CML	Current Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CATV	Cable Television
CM	Common Mode
CMFB	Common Mode Feed Back
D/A	Digital/Analogue
DAC	Digital to Analogue Converter
DC	Direct Current
DFB	Distributed Feedback
DSLAM	Digital Subscriber Line Access Multiplexer
EDC	Electronic Dispersion Compensation
EDFA	Erbium Doped Fiber Amplifier

EMI	Electromagnetic Interference
E/O	Electrical/Optical
ER	Extinction Ratio
ESD	Electrostatic Discharge
FDSOI	Fully Depleted Silicon On Insulator
FEC	Forward Error Correction
FF	Fast Fast
FP	Fabry Perot
FR4	Flame Retardant 4
FS	Fast Slow
FTTH	Fibre to the home
GBPS	Giga Bit Per Second
Gbyte	Giga Byte
GHz	Giga Hertz
GPPO	Gilbert Push On Connector for high speed application
HDTV	High Definition Television
I/O	Input/Ouput
IO	Input Ouput
LAN	Local Area Network
LBMRx	Linear Burst Mode Receiver
LNA	Low Noise Amplifier
Mb/s	Mega Bits per Second
MCML	Metal oxide semiconductor Current Mode Logic
MoM	Metal on Metal
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NA	Numerical Aperture
NMOS	Negative Metal Oxide Semiconductor

NRZ	Non Return to Zero
O/E	Optical/Electrical
OLT	Optical Line Termination
ONU	Optical Network Unit
OPEX	Operative Expenditures
PAM	Pulse Amplitude Modulation
PC	Personal Computer
PCB	Printed Circuit Board
PKD	Peak Detector
PMOS	Positive Metal-Oxide Semiconductor
PON	Passive Optical Network
PRBS	Pseudo Random Bit Sequence
PVT	Process Voltage Temperature
PWD	Pulse Width Distortion
RGC	Regulated Gate Cascode
SAN	Storage Area Network
SCM	Sub-Carrier Multiplexing
SiGe	Silicon Germanium
SF	Slow Fast
SS	Slow Slow
TDMA	Time Division Multiple Access
TIA	Transimpedance Amplifier
TIR	Total Internal Reflection
THD	Total Harmonic Distortion
VCSEL	Vertical Cavity Surface Emitting Laser
VDSL	Very High Speed Digital Subscriber Line
VGA	Variable Gain Amplifier

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1
INTRODUCTION

The world that we live in today has an endless demand for huge amounts of information travelling to and fro at a rapid rate. For this transmission, optical fibre networks have been and are being deployed world-wide ranging from long-haul networks (connecting continents and countries) over metro networks (linking cities), and now even down to access networks (connecting individual users using optical fibre technology)[1]. Until recently, fibre-optic communication was reserved for long-reach, high-capacity links between cities (metro networks), countries and continents (long-haul and submarine). Such high-end systems require transmitters and receivers where the ultimate performance in terms of capacity is of overriding importance. As this infrastructure is shared amongst millions of users, the cost of the required transponders is of secondary importance. Furthermore, volumes are relatively low, especially when compared to consumer products.

However, for some years now we are witnessing fibre-optic communication is moving into high-volume, consumer-oriented applications as shown in Fig. 1.1 [2] (short-reach interconnect such as the Thunderbolt link developed by Intel and Apple [3], or interconnect for local-area networks (LANs) and Fibre-to-the-Home applications), as well as high-end applications but requiring very high volumes of fibre-optic transceivers (short-reach interconnect for data centres and supercomputers, requiring millions of units). Traditionally, all these applications used copper-based interconnection technology. However, physical limitations (bandwidth and crosstalk in twisted pair cabling, bandwidth and physical space in coaxial based cabling) [4, 5] are increasingly pushing system integrators and operators towards fibre-optics as an alternative.

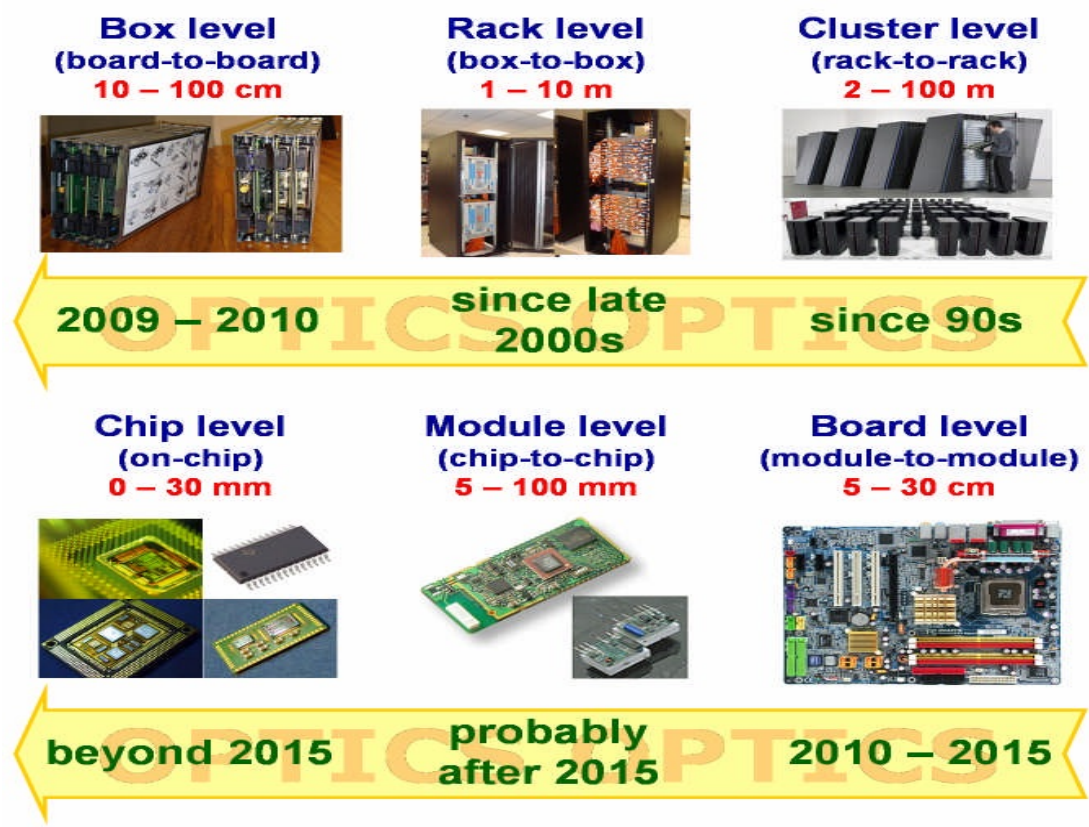


Fig.1.1 Photonics is getting closer to the processor and memory.

1.1 MOTIVATION

Today, data centres which support e.g. cloud computing, search engines, etc. make massive use of short-reach optical links to connect their servers together. State-of-the-art transceivers for these applications achieve up to 100Gb/s by multiplexing 10x 10Gb/s or 4x 25Gb/s channels [6]. Over the next few years, data centre operators have expressed a need for optical links which can support 400Gb/s up to 1Tb/s. Such transceivers should occupy the same physical footprint and have similar power consumption as today's 100Gb/s transceivers. Short-reach optical links for these applications are typically based on a directly modulated, short-wavelength (e.g. 850nm) vertical cavity surface emitting laser (VCSEL) and multimode fibres. Straightforward scaling of the currently used space or wavelength division multiplexing may be difficult to achieve: indeed a 1 Tb/s transceiver would require

integration of 40 VCSELs (vertical cavity surface emitting laser diode, widely used for short-reach optical interconnect), 40 photodiodes and the electronics operating at 25 Gb/s in the same module as today's 100 Gb/s transceiver.

This research is based upon developing high speed electronics with lower power consumption, small footprint and better performance. This research is also focussed in developing receiver and transmitter electronics for more advanced modulation formats such PAM-4 (4-level pulse amplitude modulation) as one runs into several physical limitations that will make further increase of the serial link speed using simple non-return to zero modulation difficult:

- The need for higher bandwidth VCSELs: higher modulation bandwidths can be achieved by making the active region of the VCSEL smaller (smaller diameter). However to maintain the same output power, this implies the current density increases, which has a detrimental effect on the reliability of the device. While 40GHz VCSEL devices have been demonstrated, their reliability is still a matter of research. Further scaling beyond 40GHz will prove even more challenging.
- Dispersion (modal in multi-mode or chromatic in single-mode) in the fibres: the bandwidth x distance product scales inversely proportional to the square of the bit rate.
- Packaging: scaling to very high bandwidths (>40GHz) requires exotic and expensive packaging technology (e.g. ceramic substrates) with high mechanical precision which is expensive and not compatible with high volume production.

1.2 SHORT REACH OPTICAL INTERCONNECT APPLICATIONS

1.2.1 LAN (LOCAL AREA NETWORKS) AND SAN (STORAGE AREA NETWORKS)

In local area networks (LAN) and storage area networks (SAN) (which connect computers, servers and storage devices together inside e.g. company sites) copper had the competitive edge from a lower cost perspective, however the increase of data rates, largely driven by consumer internet video, digital television and

enterprise backup applications, are pushing the industry to deploy optical interconnect within their own LAN and SAN infrastructure [6] as can be seen in fig. 1.2 [7].

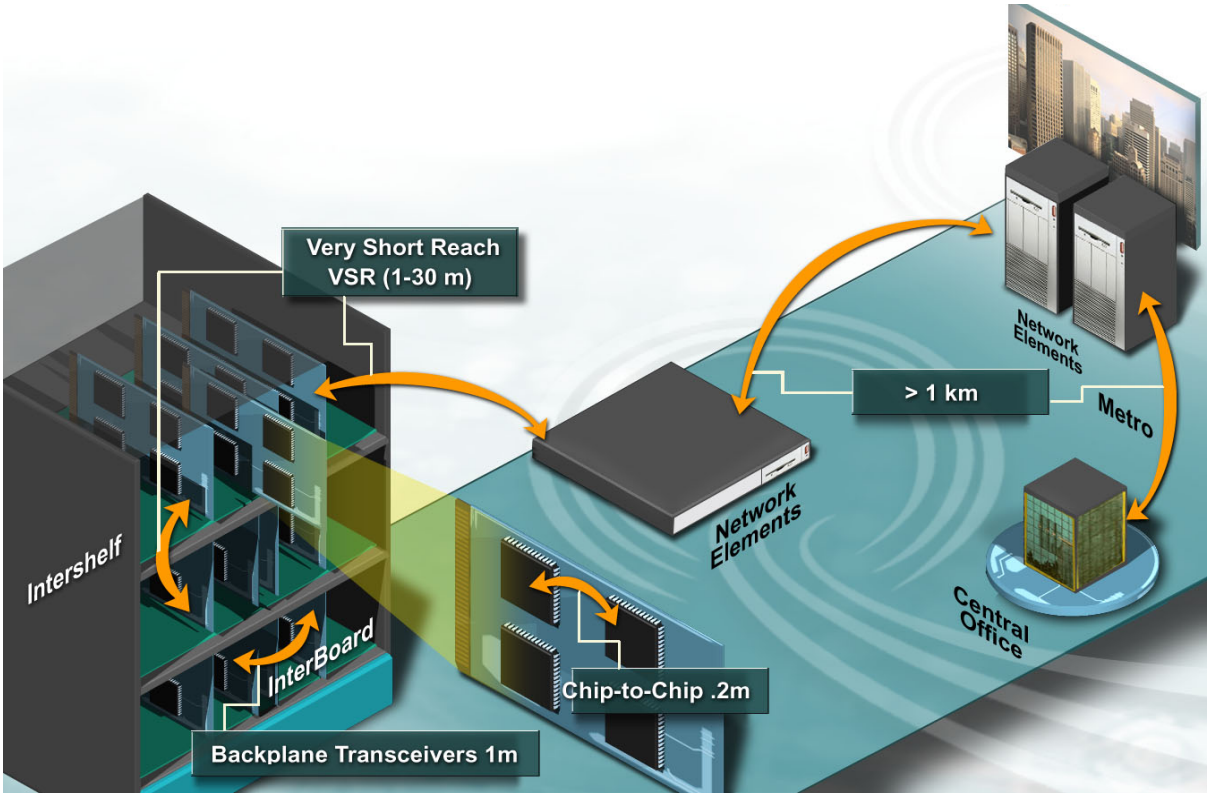


Fig.1.2 Optical interconnects in the LAN and SAN networking arena.

1.2.2 Data Centres

In the last few years, we've witnessed the rapid emergence of huge data centres, also sometimes called 'warehouse scale computers'. These data centres underpin applications such as cloud computing, internet search engines, video-on-demand, social media etc. A diagram of a typical data centre shown in Fig. 1.3: such a data centre consists of thousands (some rumoured to contain hundreds of thousands of servers) of servers, arranged in racks, connected together with high-speed switches. Today, data centres face continuous pressure to expand their capacity to handle

more data from a growing user group, new data-intensive applications and bandwidth hungry applications. Already, today's data centres make massive use optical links.

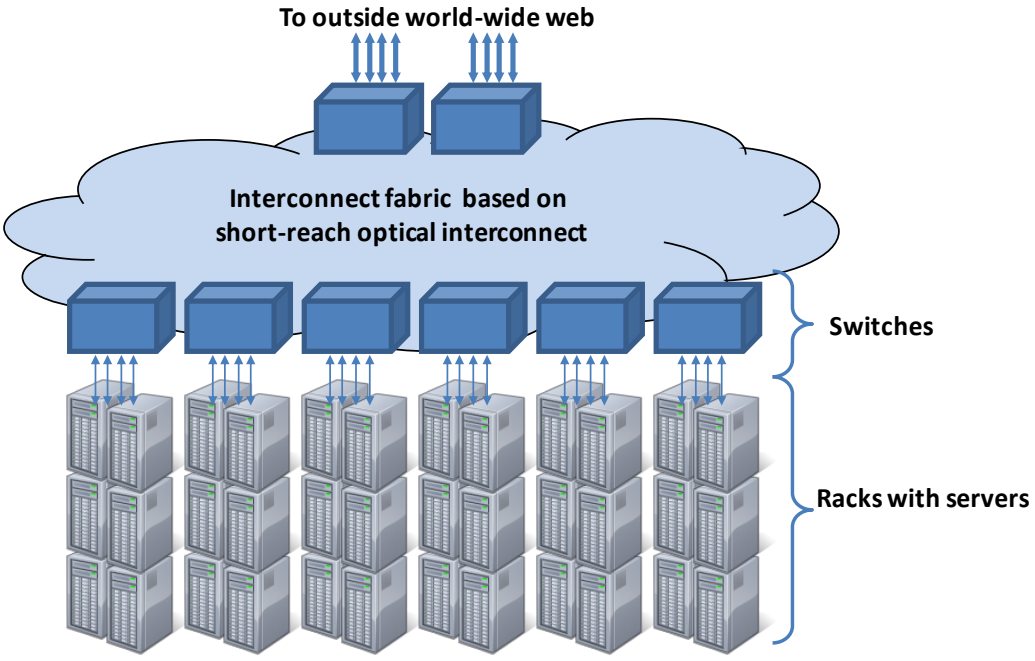


Fig.1.3 A typical data centre network.

The most challenging issue in the design and deployment of a data centre is its power consumption. However as data rates and number of lanes per I/O (Input/Output) port increase, the size of electrical connectors and the power dissipation in copper traces is difficult to keep in control[8]. To meet the demands of high throughput, reduced latency and low power consumption optical networks are now being used in such systems [9, 10].

1.2.3 High Performance Computing

In a simplified view, a high performance computer consists of racks of servers, all tightly interconnected together. As shown conceptually on Fig. 1.4, each

such server consists of processor and memory cards; connected together using parallel busses running across the backplane.

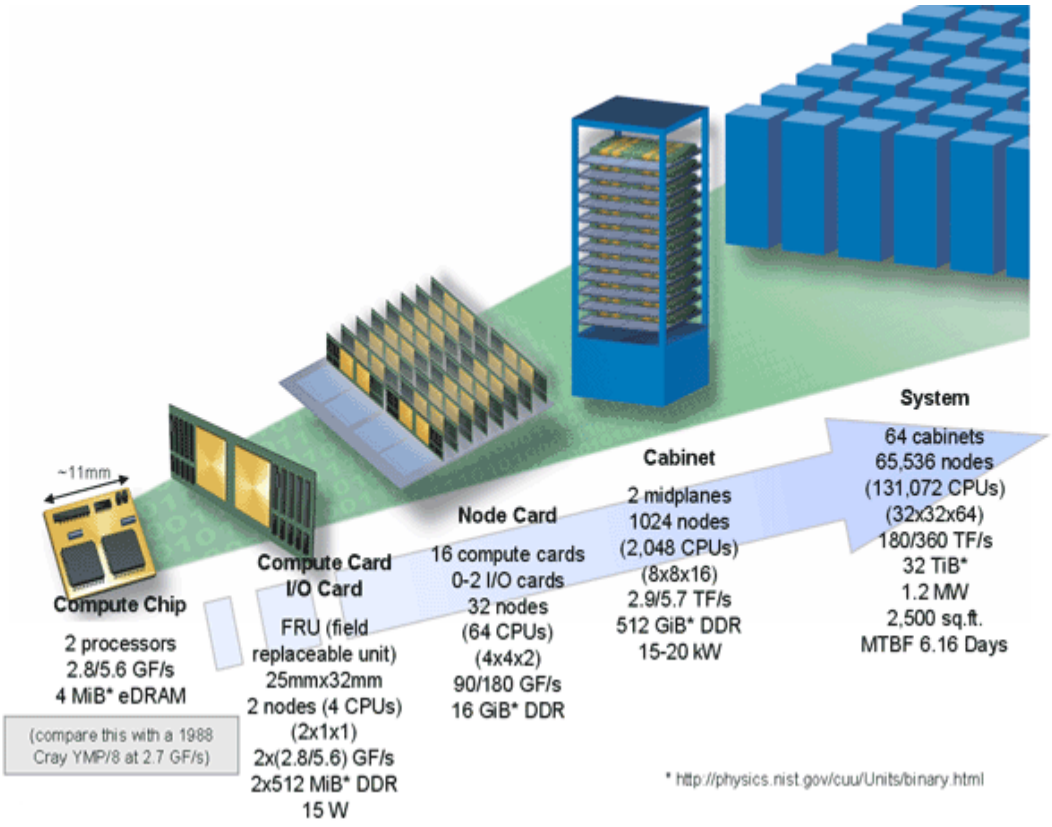


Fig.1.4 Conceptual view of a high-performance supercomputer (Blue Gene): the compute cards (containing the processors with memory) and IO cards are assembled into “node cards” which are basically backplanes.

To overcome limitations in the number of IO (Input Output) pins per chip, the interconnect between processor and memory cards is implemented using serial links and SerDes (Serializer/Deserializer) chips, which serialize the data prior to sending it across the backplane. In high-end servers which contain several processor and memory cards per backplane, such a backplane can easily have an area of ~1m^2. With ever increasing IO bandwidths between the processing units and the memory banks, this server technology faces two significant bottlenecks for

further upscaling (which requires more IO pins per processor and memory chip, increasing bus widths and higher throughput per individual bus link):

1) Conventionally, backplanes are manufactured using FR4 (flame retardant – 4) material (a glass reinforced epoxy composite material widely used for fabricating printed circuit boards), onto which copper traces are etched. While this manufacturing process is very well established, unfortunately it is not very well suited for high-speed data transfer. Indeed for example, Fig. 1.5 shows the insertion loss of a 1 meter long (impedance matched) trace on an FR4 board: an insertion loss of 25 dB at 5 GHz can be observed.

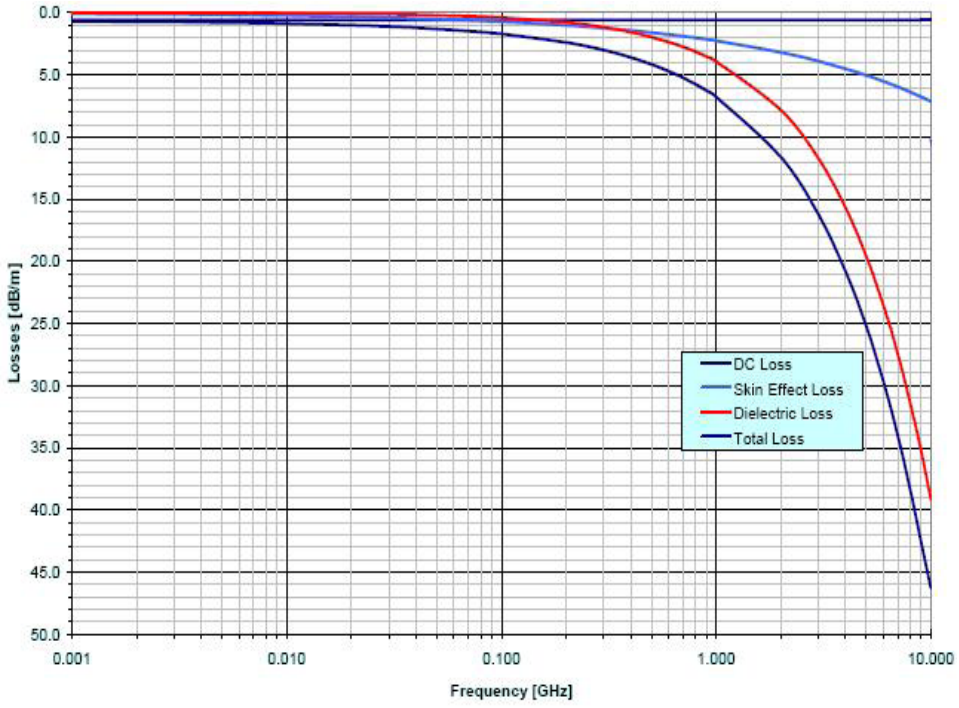


Fig.1.5 Insertion loss (dB/m) of a 100 Ωmatched differential transmission line versus frequency (Avago application note AN5362).

Using sophisticated equalization techniques, these losses can be overcome and transmission speeds up to 25 Gb/s have been demonstrated across such links. However, how to scale up beyond 25 Gb/s is currently an open question. Signal integrity across backplanes is further compromised by

crosstalk and electromagnetic interference, all of which become worse with increasing bandwidths.

2) The amount of IO pins that can be placed around the core circuitry of eg. multicore processors and memory chips. The ever increasing integration density (set to continue for at least another decade despite numerous claims that Moore's law has ended) allows to place more and more transistors on a given chip area, thus increasing its functionality. This requires higher IO bandwidths to and from the processor and memory chips. However, the size of IO pins does not scale accordingly. 3D integration is set to become the answer to this, however even then connections with ever increasing bandwidth will be required.

One option to overcome these problems is an optical bus: this can solve the problem of cross-talk and signal loss[11]. Such an optical bus consists of serializers/deserizalizers, O/E (Optical/Electrical) and E/O (Electrical/Optical) converters connected together using e.g. optical waveguides in a PCB (Printed Circuit Board). Fig. 1.6 shows a combination of electrical and optical cabling in IBM (International Business Machines) supercomputers and in Fig. 1.7 optical to optical connection is shown[12].

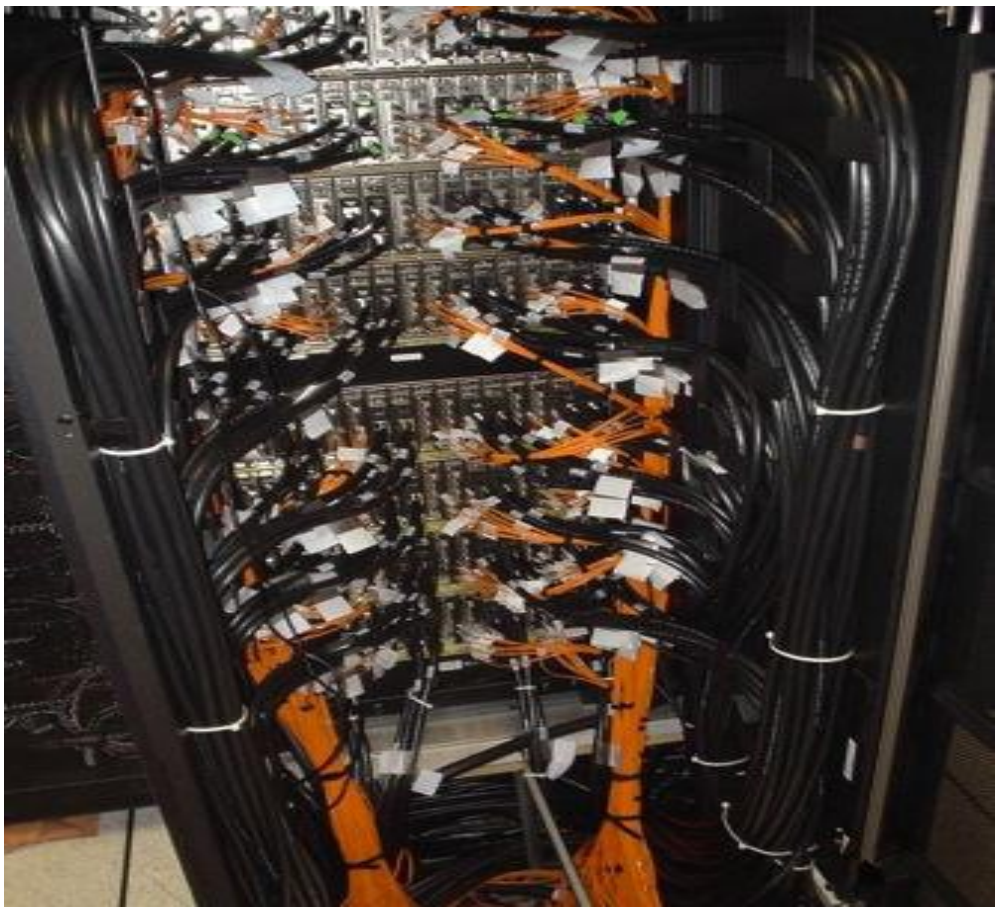


Fig.1.6 Electrical and optical cabling in supercomputers

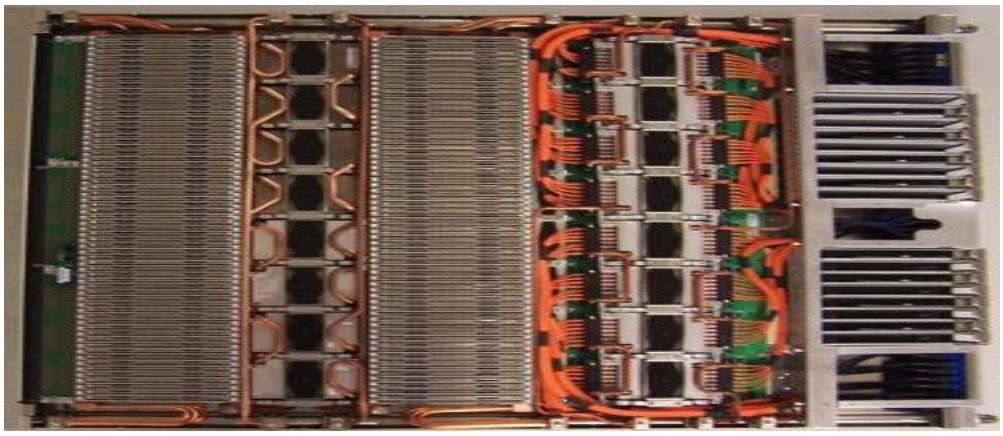


Fig.1.7 Optical to Optical communication between chips externally

1.2.4 Consumer Applications

In modern homes increasing number of consumer electronic devices for communication and entertainment needs need to be interconnected and connected to the outside content providers, thus requiring the home networking solutions to have higher bandwidths as shown in Fig. 1.8[13].

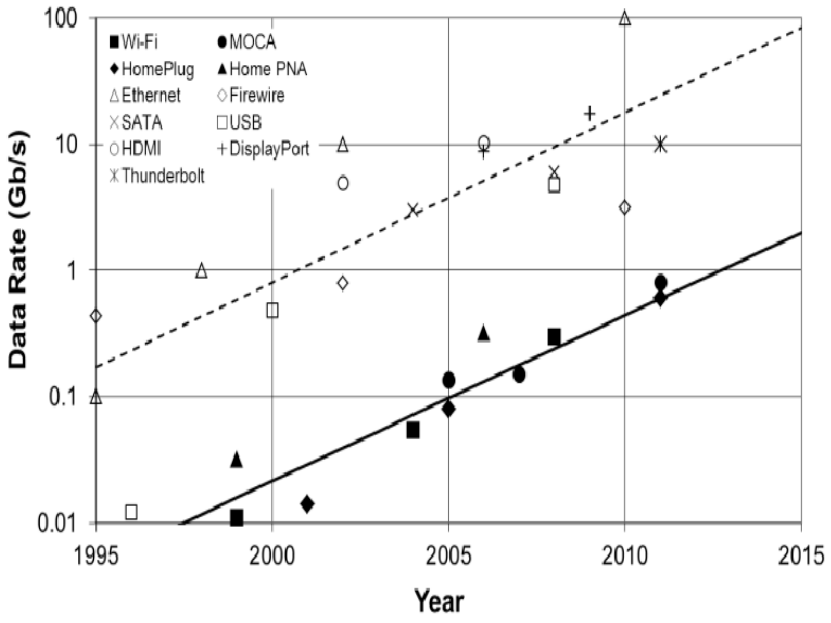


Fig.1.8 Data rate evolutions of various protocols commonly used in "backbone" homenetworks (closed symbols) and for device-to-device direct communication (open symbols).

For example, if a conventional USB link is used to transfer high definition files, a complete transfer requires 6-8minutes assuming a Blu Ray file of 30 GByte and an USB 2.0 link having a throughput of 480 Mb/s. Transferring such a file in a matter of seconds will require short-reach links with multi-Gb/s capacity. As with other applications mentioned above the classical copper based interconnect is again losing out here due to its high-power consumption (due to the use of extensive signal processing to counter the cable attenuation at high frequencies), and greater EMI (electro-magnetic interference) issues. Low-cost fibres (such as Plastic Optical

Fibre) and VCSEL's (Vertical Cavity self Emitting Lasers) can give optical links an edge in terms of cost and performance benefits [14]. The importance of POF is not just that it is easy to handle (e.g. a sharp knife is sufficient to cut it to length) and is cheap, but also that its large core significantly relaxes the tolerance on mechanical alignment of the transceiver optics. This is usually a significant fraction of the overall transceiver production cost. An example of such technology is shown in Fig. 1.9: this link is known as Thunderbolt link which offers the customers to connect their devices to PC's and transfer the data at speeds up to 10 Gbps[3].

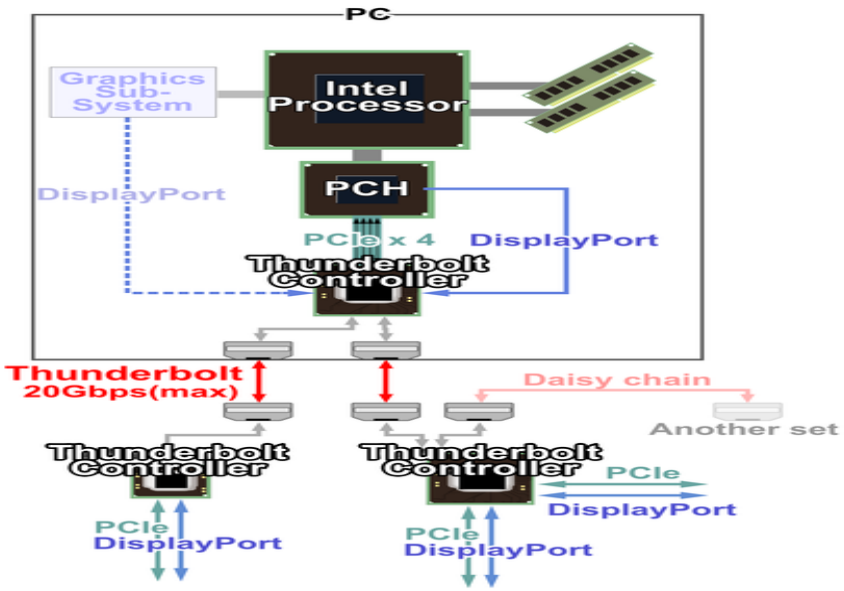


Fig.1.9 Thunderbolt technology by Intel

As discussed above optical links are replacing electrical links in local-area networks, and may now also become the prime choice for even shorter links in consumer applications. As usual, the optical transceiver design needs to consider three major criteria: low power consumption, low cost and small size, in order to allow the integration of parallel optical interconnects. With the advent of VCSEL's [15](Vertical cavity surface emitting lasers) having lower threshold current and higher bandwidth, it provides an attractive solution in such design dominated by power, cost and size. The challenge in these links is to maximize the data rate per pin as the number of pins will remain constant across future technologies [16].

CMOS (Complementary Metal Oxide Semiconductor) front end-circuitry becomes then an interesting choice as it provides the highest possible level of integration [17]. Low-cost can be achieved once high sales volumes are realized.

1.3 OVERVIEW STATE-OF-THE-ART ELECTRONICS FOR SHORT-REACH OPTICAL INTERCONNECT

VCSEL driver circuitry operating up to 10 Gb/s (non-return to zero) have been demonstrated in [18-21]. In [18-20], these drivers were part of 1-dimensional arrays for parallel interconnects. In [21], a 2D driver was demonstrated with a total throughput of 250 Gb/s (48 x 5.21 Gb/s) More recently, VCSEL drivers operating up to 25 Gb/s and 40 Gb/s have been described [22] by VI Systems, without disclosing performance details however. In [23] and [24], 18 Gb/s and 20 Gb/s VCSEL drivers were reported respectively. High single channel bandwidth is achieved by implementing various emphasis techniques which overcomes bandwidth limitations due the parasitic capacitance (of both IO cell and VCSEL itself) and non-linear response of VCSEL by introducing some pre-distortion in the output driver waveform. Scaling beyond 20 Gb/s using CMOS technology is difficult without peaking inductors. Additionally, VCSELs face severe reliability issues when scaling beyond 10 Gb/s due to high current density (which becomes higher for increased speed, as increased VCSEL bandwidth is achieved by pushing the same VCSEL current through a smaller cross-section).The use of inductors increases the chip size, thus making it undesirable for optical interconnects as a small size is a critical requirement for optical interconnects. Clearly, pushing bit-rates beyond 25 Gb/s as standard bodies are now doing [25, 26] is challenging. An alternative solution is then Pulse Amplitude Modulation (PAM) in which the information is encoded in the amplitude of a series of signal pulses decreasing the constraints on the bandwidth of the single channel and increasing the spectral efficiency. A PAM-4 VCSEL driver is reported in [27] operating at 10 Gb/s; at 32 Gb/s in [28] and a 25 Gb/s PAM4 transmitter in [29].

Chapter 3 of this work describe in detail the design of a single channel 40 Gbps VCSEL driver using rising and falling edge emphasis and chapter 4 describes a PAM4 VCSEL driver operating at 56 Gbps achieved by using MCML gates and low power

techniques for the driver stage. Both the drivers are designed using 65 nm pure CMOS technology.

Very high speed receivers are also reported in [30-33] using various SiGe (Silicon Germanium) and sub micron CMOS technologies operating at 40 gbps and a four channel 25 gbps receiver is reported in [34] for NRZ modulation. All the receivers reported above are limiting in nature which works fine for NRZ modulation but they do not provide equal gain to all the levels of signals if the modulation is multilevel PAM. A receiver for multilevel PAM needs a linear response over its entire dynamic range which uses a VGA (variable gain amplifier) instead of a limiting amplifier [35]. Chapter 5 presents a 20 GHz linear receiver designed using 28 nm CMOS technology having a linear response for its entire dynamic range of 20 µA to 500 µA.

1.4 OPTICAL ACCESS AND FIBRE TO THE HOME

A simplified view of the present day communication network is shown in Fig. 1.10: it consists of long-haul or core networks (between countries and continents), metro networks (from exchanges to local aggregation points, linking together cities) and access networks (from home to local aggregation points).

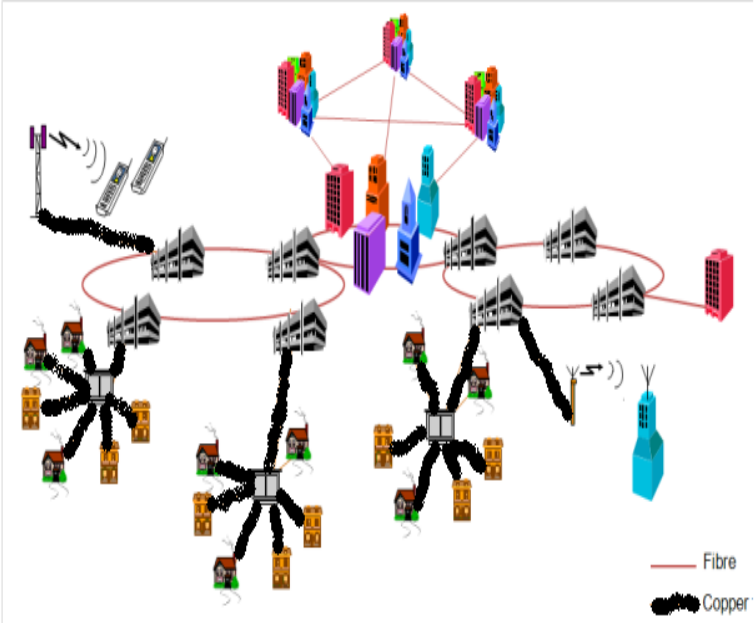


Fig.1.10 Present day communication network

Today, copper (under the form of the twisted pair carrying both telephony and broadband internet using digital subscriber line technology (VDSL, ADSL, etc) and coaxial cable for CATV) is still the dominant technology in the access networks. However, ever increasing bandwidth demands are pushing the fibre closer “to the home”: for example many operators nowadays would use technologies such as “fibre-to-the-cabinet” or “fibre-to-the-curb”, in which the data to and from the DSLAMs (digital subscriber line access multiplexers) and local access points are carried using optical fibres. In the future it is anticipated that optical fibre will eventually run right into the homes of the individual subscribers. For example, in Japan the number of fibre-to-the-home users has exceeded the number of VDSL lines since [36]. This was achieved through government subsidized schemes.

Technology in access networks needs to be low cost, especially the modems in the subscriber’s house, as the cost of this infrastructure is not shared by many customers [37, 38]. Over the last five years, we have witnessed an overwhelming development of new access networks based on Fibre-to-the-home (FTTH) technology especially in the Far East (Japan, China and S. Korea) and the US. One of the means of implementing FTTH is a passive optical network (PON) which is very cost effective as it shares the cost of the fibre plant and fibre-optic transceivers over many customers and it doesn’t have any active component between the central office or exchange and the customer[39, 40]. PONs have a tree like fibre plant structure which is used to connect a number of subscribers (which have optical networks units or ONU) to a central office (or optical line termination – OLT) as shown in Fig. 1.11. Note that by using this tree like fibre plant, N customers can be connected full duplex to a central office using N+1 transmitters (N transmitters in the ONUs and a single transmitter in the OLT) and N+1 receivers (N receivers in the ONUs and a single receiver in the OLT). This almost halves the amount of required transceiver modules, this significantly reducing capital investment and cost for the subscriber. As a common transmission medium is shared between the subscribers and the central office, a multiplexing scheme is required to send data downstream (from the OLT to the ONUs) as well as upstream (from the ONUs to the OLT). In the downstream direction, time division multiplexing can be used. In the upstream direction, an access protocol is required to avoid interference of data

between different subscribers. Time division multiple access (TDMA) is widely used in PONs as it provides very low cost. In such systems exclusive, non-overlapping time slots are allocated to each subscriber in which their data can be transferred in upstream direction.

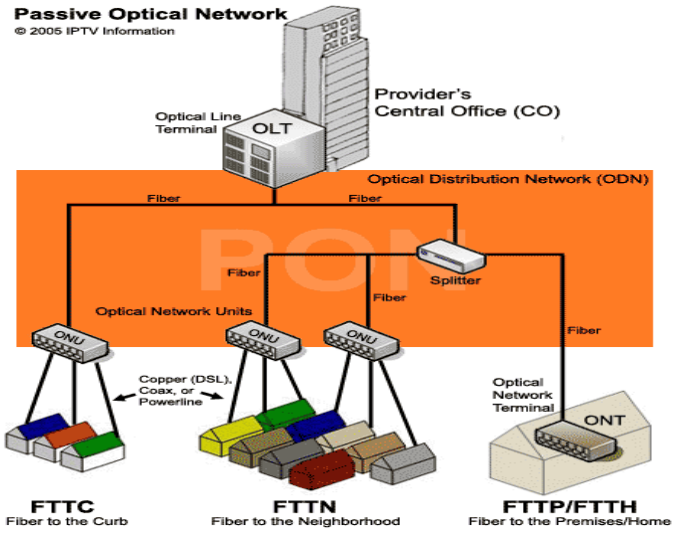


Fig.1.11 A typical PON system

This means that the central office receiver and the subscriber transmitter need to operate in burst mode where they are switched on only during their designated time slot. The receiver in the central office needs to be a burst-mode receiver (BMRx). The BMRx in such a system is a very critical component as its sensitivity (optical power that is required for a given bit-error-rate) and dynamic range determine the reach and split (amount of subscribers connected to central office) of the system. The burst-mode receiver needs to be able to handle a signal which consists of a quick sequence of bursts. These bursts exhibit a wide dynamic range from burst to burst due to two main reasons. One is the distance between the subscribers and the central office may vary resulting in different attenuation in the fibre path and second is the launched power from the subscriber's transmitter may vary as well. Which makes the requirement of the receiver very stringent as it need to be able to quickly change its gain and decision threshold (distinction between 1 and 0 transmitted) from one burst to the next. As no data is received when the BMRx is changing its gain settings, which could lower the traffic efficiency, the quick

adjustment (within a few tens of nanoseconds to hundreds of nanoseconds) is very vital for the operation of the whole system.

Chapter 6 presents the details of the designed burst mode receiver which is to be used for the application explained above.

2

COMPONENTS OF SHORT REACH OPTICAL INTERCONNECT

This chapter provides a brief theoretical background of components that are used in the short reach optical interconnects which includes the types of fibre used, explanation of various types of light sources (lasers and photo-diodes), their properties detailing their advantages and disadvantages. It briefly touches the electronics that is used in designing such type of transceivers and also outlines the challenges faced in such designs.

2.1 OPTICAL LINK

An optical link is a part of an optical fibre based communication network which transmits and receives data between two points. It is essentially made up of a transmitter which converts electrical current pulses into light pulses (usually generated by a laser diode) where it is converted into light and transmitted to the receiver through fibre. At the receiver it is detected by a detector (PIN or APD diode) converting it back into current from light which is then further processed by the receiver circuitry as shown in Fig 2.1.

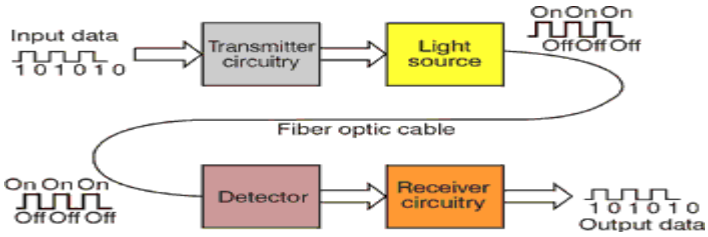


Fig.2.1 A basic Fibre optic communication system (non-return to zero modulation).

The advantages [41] of using optical links for communication for long distances (several kilometres up to thousands of kilometres) as well as smaller distances are listed below

1. Enormous bandwidth: large amounts of data can be transferred through an optical fibre compared to e.g. wireless or copper-based cables [42].

2. Small size and weight: Optical fibres are small in size and are lighter than corresponding copper cables[43].

3. Electrical isolation: Optical fibres are fabricated from glass or sometimes a plastic polymer and the light signals are guided inside a core, hence signals travelling in separate fibre are electrically insulated which makes them ideal for communication in hazardous environment [44, 45].

4. Signal Security: lack of significant radiation makes an optical link ideally suited for military, banking and general data transmission by providing a high degree of signal security[46].

5. Low transmission loss: Optical cables which are fabricated now a days have very low attenuation or transmission loss in comparison to copper: this characteristic of optical fibre is indeed the fundamental reason for its wide deployment

Optical fibre based communication of course also have some disadvantages, which even today make application of optical fibre links in e.g. mass-market consumer applications quite challenging:

1. Highly specialized mechanical assembly techniques (splicing, fibre welding with submicron accuracy): (single-mode) optical fibres have a very small core (8 µm diameter) which requires very tight tolerances when aligning these with active optical components such as lasers or modulators. Mechanical assembly still requires substantial manual effort. This is to be contrasted with the highly established (solder-based and pick-and-place) technologies required for assembling electrical links. It means that optical links can be quite expensive.

2. Complex fabrication and material systems: manufacturing of lasers, modulators, photo-detectors require complex material systems (e.g. III-V materials) and sophisticated fabrication flows, unlike electronics where e.g. integration in monolithic Silicon chips has been hugely successful. The result is relatively low yields, requiring manual cherry picking of devices, with obvious impact on cost.

2.1.1 OPTICAL FIBRE

In an optical link light is transferred from one point to another point through fibre, which essentially is a cylindrical dielectric non-conducting waveguide. It transmits light along its axis[47] by the process of total internal reflection (TIR) i.e. When light hits a boundary at a steep angle which is larger than the critical angle for the boundary while travelling in a dense medium, it gets completely reflected. This is how light is confined in the core of the fibre and it travels along the fibre bouncing back and forth off the boundary[48]. The fibre is made up of a core surrounded by a cladding layer as shown in Fig. 2.2, both of which are dielectric materials. The refractive index of the core must be greater than that of the cladding[49] to keep the optical signal propagating in the core.

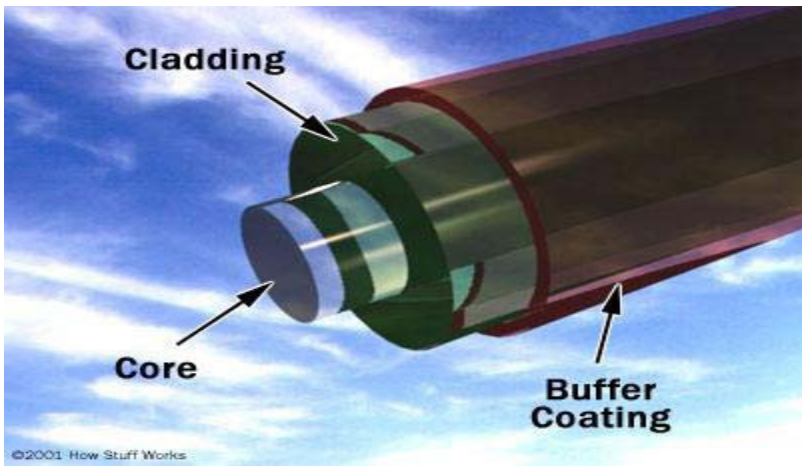


Fig.2.2 Makeup of an optical fibre.

Only the light which strikes the boundary with an angle greater than the critical angle can travel down the fibre without leaking out so there is a certain range of angles with which light must enter the fibre, such range of angles is called the acceptance core of the fibre. It is a function of the refractive index difference between the fibre's core and cladding. In a layman's term there is a maximum angle at which light must enter the fibre for it to remain in the core and propagate through the fibre. The Sine of this maximum angle is the Numerical Aperture (NA) of the fibre. Fibre with a larger NA required less precision to splice and work than fibre with a smaller NA.

2.1.1.1 MULTI–MODE FIBRE

A fibre which allows multiple rays/modes to couple and propagate simultaneously is known as multi-mode fibre as shown in Fig. 2.3

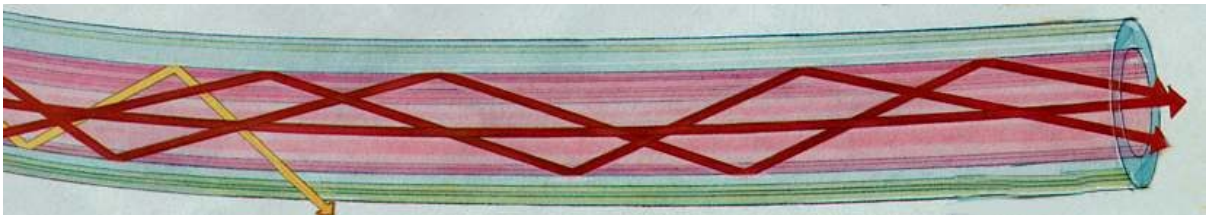


Fig.2.3 light travelling in multi-mode fibre

It has a larger core diameter than single-mode fibre (e.g. 50µm and 65µm are two standard core diameters, contrasting with the 8µm single-mode fibre core). From the figure it can be seen that three rays travelling through the multi-mode fibre arrive at different times as they take three different paths: this leads to inter symbol interference which broadens the input pulse (and ultimately limits the bandwidth of the fibre). This dispersion is corrected in multi-mode fibre by making the refractive index of the core greatest at the centre and decrease rapidly until it becomes constant near the core/cladding interface. This makes the light travel helically rather than taking the zigzag route as shown in Fig. 2.4 and this shortened path allows the light to arrive at the receiver at the same time.

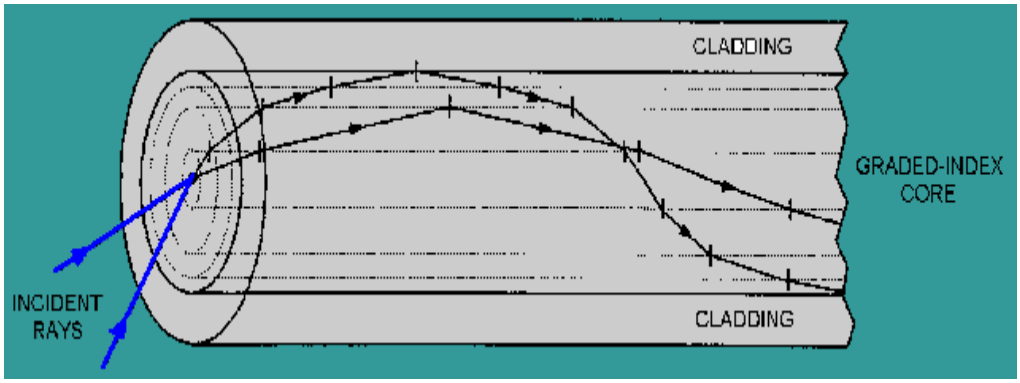


Fig.2.4 light travelling in Multi-mode graded index fibre.

2.1.1.2 SINGLE MODE FIBRE

As the name suggests a single mode fibre only allows one mode to propagate through the fibre, this is normally accomplished by shrinking the dimensions of the core of the fibre (8-10 µm). Unlike multi-mode fibre, only a single mode can propagate in this fibre therefore no modal dispersion can occur: single-mode fibre can therefore support much larger bandwidths compared to multi-mode fibre. Again, dispersion limits the ultimate bandwidth: indeed due to material dispersion (variation of the refractive index with wavelength) a light pulse (which in practice is never purely monochromatic) will experience chromatic dispersion which again broadens (or narrows) the pulse limiting the bandwidth.

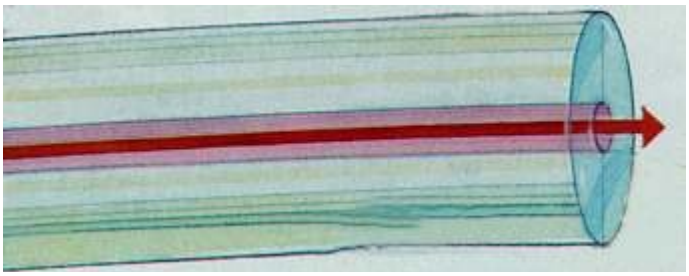


Fig.2.5 light propagating through single mode Fibre

2.1.1.3 MULTI−MODE VS SINGLE MODE

As this work is concentrated on short-reach optical interconnect, the choice of using the type of fibre is also based on that. We are moving in an era where data rates in short reach optical interconnect are pushing towards 40 to 100 Gbps in various applications of HDTV, data centres and high-performance computing which raises the question which type of fibre is best suited for such applications.

Fibre in Short-reach optical interconnects are mainly driven by the cost factor [50] as they need to replace the existing copper cables which means that they should be cheap in production, lower in cost in installation, should have low cost connectors, should have better performance at target distances (a few hundred meters up to maximum e.g. 2 km), should have low system cost and be easy to manufacture. The difference in the cost between multimode and single mode fibre with relation to the system perspective is presented in Table 2.1[51]

	Multimode	**Single Mode**
Light Sources	Low	High
Connectors	Low	High
Installation	Low	High
Fibre	High	Low
System	Low	High
Loss	High	Low
Distance	Low	High

Table 2.1 Differences in the cost and performance of Multi and Single mode Fibres with systems perspective

Single-mode fibres have a small core size (< 10 µm) which requires precision alignment to inject light from the transceiver into the core, significantly increasing

the cost of the transceiver, whereas the multimode fibre have larger cores and thus makes it much easier for it to capture the light from the transmitter.

The requirements over alignment for the single mode connectors are very stringent in comparison to the multi-mode fibres which make the cost of using multimode fibres lesser than the single mode fibres.

Loss in multi-mode fibres is more than the single mode fibres but it is relevant to the distance at which data needs to travel. Since it is short reach multimode fibres can easily support short distances with data transmission at 100 Gbps[52] and with bend insensitive multimode fibre (BIMMF) [53] such losses are becoming more and more minimal. Usually fibre loss in short-reach optical interconnect is almost negligible.

Light sources for single mode fibres are available at wavelength of 1310 and 1550 nm which are expensive in comparison to the multimode fibres which are available at 850 nm and 1310 nm thus nullifying the advantage of cable cost that single mode fibre has over multimode fibre.

While current systems mainly use multimode fibre, a shift towards single-mode fibre for short-reach optical interconnect is being debated in the industry. It is not clear what the choices will be.

2.1.2 Light Sources

2.1.2.1 Transmitters

Today, two different types of semiconductor lasers are widely used: one is edge-emitting and the other is surface-emitting. Among high speed edge-emitting lasers, prominent are FP (Fabry Perot) and DFB (Distributed Feedback) lasers. The VCSEL

(Vertical Cavity Surface emitting Laser) is the surface emitting type. Table 2.2[54] provides a comparison between the VCSELs and other lasers which highlights the point that why VCSELs are gaining recognition in short reach optical interconnect.

Attribute	**VCSEL**	**DFB and FP**
Cost	Low	High
Optical output power	Low	High
Power consumption	Low	High
Size	Small	Large
Testing	On Chip at wafer-level	Difficult
Manufacturing	Easy(20,000 devices on 3 inch wafer)	Difficult
Packaging	Easy	Difficult
Coupling to Fibre	Efficient	Inefficient
Modulation	Direct	Direct or external
Driver Circuitry	Simple	Complicated

Table 2.2 VCSEL advantage over other Lasers

Key advantages that VCSELs have over other lasers for short reach optical interconnect are the following

- **High Yield:** 20,000 individual VCSELs can be processed in a 3 inch wafer so even if 10 or 20 percent of them are lost, this is still a high yield compared to other laser types , thus making VCSELs more cost-effective as well.
- **Wafer Level Testing:** VCSELs are easily tested before the wafer is diced where as DFB and FP lasers must be cleaved from the wafer and packaged before being tested which increases the processing cost of such lasers. Again it is an advantage for VCSELs to be used in short reach optical interconnect
- **Easier Coupling and Packaging:** The circular cross-section of VCSELs gives it better control for easier coupling and alignment with fibre during packaging than DFB and FP lasers.
- **Driver circuitry:** typically, DFB and FP laser diodes have very low impedances compared to VCSELs (which have an impedance in the range of 50Ω to 100Ω) and require rather high bias and modulation currents (tens of milliamperes rather than a few milliampere), making the design of the driver circuitry of a laser diode quite challenging (switching large currents at high-speeds)

2.1.2.1.1 VCSEL Parameters

The parameters of the VCSEL light source which are used in the design are based upon the devices received by the partners in the VISIT project tested at Tyndall National Institute and are listed in Table 2.3

Parameter	Units	Value
Threshold Current	mA	<0.5 mA

Slope Effeciency	mW/mA	>0.6
Slope Effecient Temp. Variation	%/°C	0.17 %/K (0.82 W/A at 20oC to 0.73 W/A at 85oC)
Output Optical Power	mW	2
Operating Current	mA	5
Forward Voltage @5mA	V	2.0
Differential Resistance	Ω	50
Rise and Fall time	ps	<15
Total Parasitic Capacitance	fF	90-110 fF
Data Rate	Gb/s	BER $<10^{-12}$ @40 Gb/s

Table 2.3 VCSEL parameters from the VCSEL diode used in the design

It should be noted that the devices from which these values are extracted are still to be tested for reliability.

- **Threshold current :** The threshold current of a VCSEL is defined as the current which is needed to start the lasing in the VCSEL (stimulated emission rather than spontaneous emission). Most of the 850 nm VCSEL have threshold current in the range of 1-2 mA [55]. The threshold current of the VCSEL is dependent upon temperature; different VCSELs can have different threshold currents Fig. 2.6 shows how the emitted power from the VCSEL depends upon its bias current (both the measured output and a fitted model output are shown)

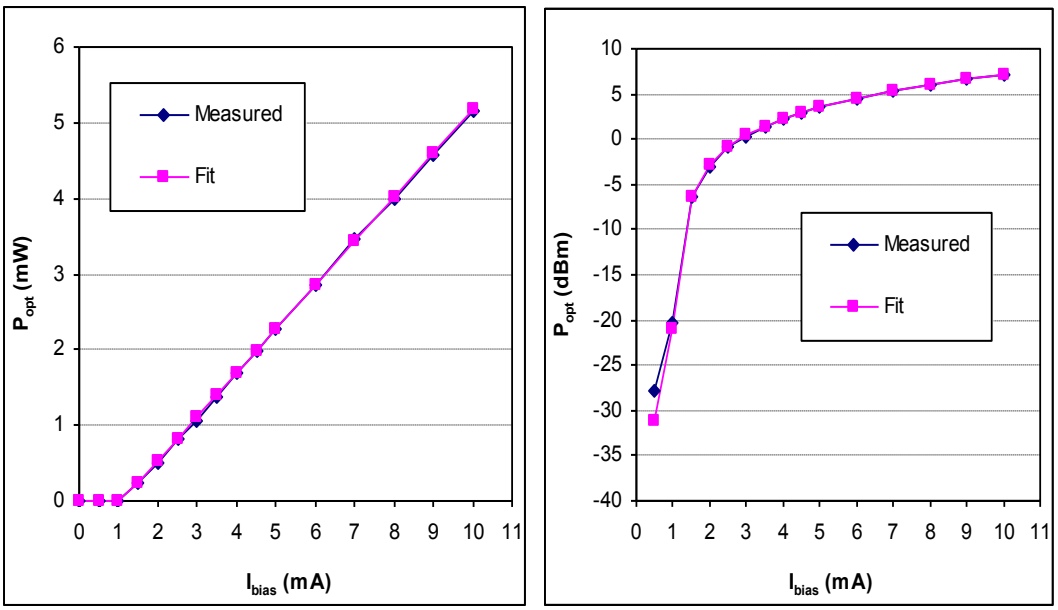


Fig.2.6 Emitted power as a function of current.

- **Slope Efficiency:** The slope efficiency of the VCSEL is given as the ratio of incremental increase in power to the incremental increase in current. Fig. 2.7 shows the general idea of what slope efficiency is

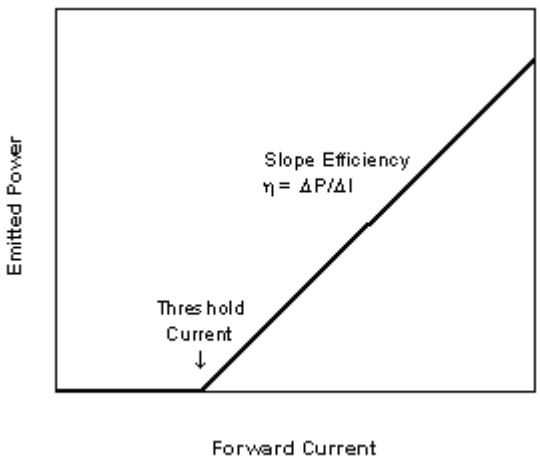


Fig.2.7 Understanding slope effeciency

- **Series resistance:** For most diodes the junction voltage at a fixed current decreases as the temperature increases, however the VCSEL series resistance cannot be ignored in the circuit design as it normally within the range of 20-100 ohms. Fig. 2.8 shows the variation of the VCSEL resistance with bias current: it consists of a parasitic series resistance (usually due to the contact structures) and the diode differential resistance. Similarly, the total capacitance of a VCSEL consists of the junction capacitance (which increases with increasing bias current) and a part due to the metal contact structures.

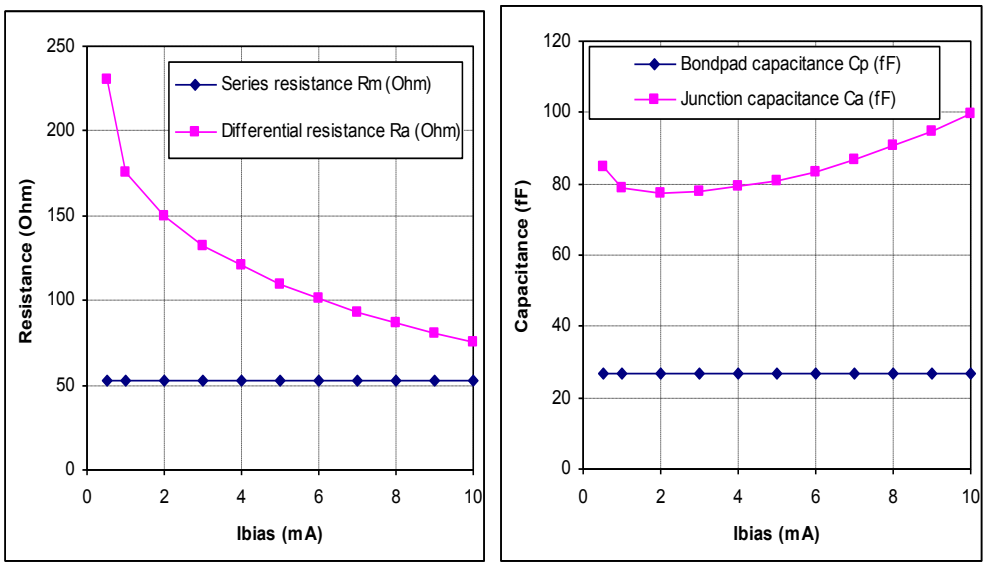


Fig.2.8 Series resistance and Junction Capacitance with Ibias of VCSEL

- **Thermal Rollover:** The thermal rollover of the VCSEL is the point at which the emitted power starts to reduce after a certain amount of current [56]is pumped into it. The corresponding excess electrical power is dissipated as heat and warms the VCSEL up, so it is always advisable to operate the VCSEL below this current. Fig. 2.9 shows the variation of output power with the ambient temperature.

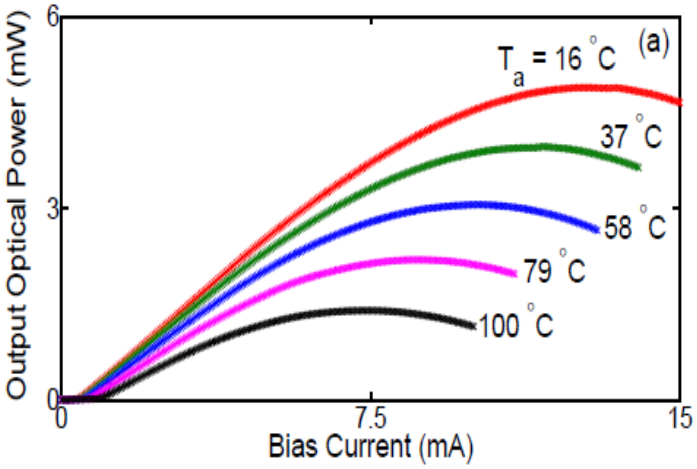


Fig.2.9 Thermal rollover phenomena of VCSEL

- **VCSEL electrical parasitic and equivalent model:** Fig. 2.10 shows a simplified model of the electrical parasitics of the VCSEL. C_{BP} is the parasitic capacitance stemming from the VCSEL bondpad structure. R_S is the active region series resistance and C_J is the capacitance of the forward biased junction. R_{act} is the differential resistance of the active region (the forward bias diode).

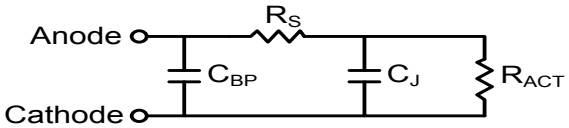


Fig.2.10 VCSEL parasitics.

Fig 2.10 shows the final VCSEL model, which is fully compatible with transistor-level circuit simulators. The parasitics have been implemented using standard components, the electro-optic properties are described using rate equations which have been implemented using Verilog-A (see Appendix A). The driving current for the Verilog-A model is the current through the active region differential resistance. In the Verilog-A model, both the normalized electron density and the VCSEL optical output power are represented as voltages. It is to be noted that the transformed

VCSEL rate equations offer a significant advantage when implemented in a Verilog-A model. Indeed the actual numbers representing the optical output power and normalized electron density are similar to the numerical values of voltages encountered in typical CMOS circuits.

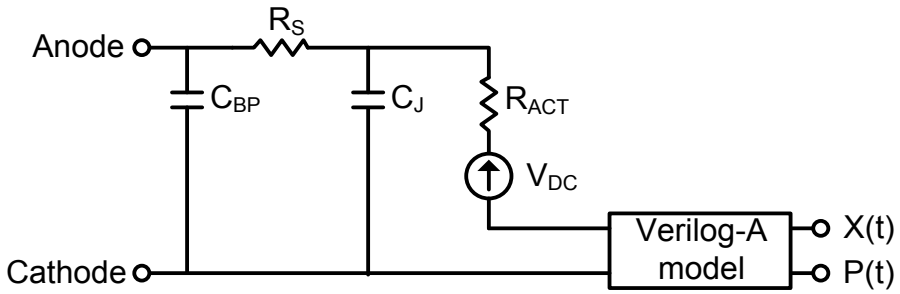


Fig.2.11 Complete VCSEL model.

2.1.2.2 Receivers or Photo Detectors

These are opto-electric devices which convert the light signal coming from fibre to electrical pulses. When the light strikes the detector a current is produced which is proportional to the intensity of the incident light. In general the photodetectors should have high responsivity, minimum noise, fast response, and low cost.

- PIN Photodiode: It consists of a p and n semiconductor region which is separated by a lightly (almost intrinsic) doped n- region. A reverse bias voltage is applied across the device to make sure there are no free electrons or holes present in the intrinsic region. The photons in the incident light having greater energy than the bandgap energy of the semiconductor material excite an electron from the valence back to the conduction band.

- Avalanche Photodiodes: APDs (Avalanche Photodiodes) have an internal region where electron (and or hole) multiplication occurs, by application of an external reverse voltage. Incident photons create electron – hole pairs in the depletion layer of the APD structure and these move towards the

multiplication region where a high electric field is present. If the external bias is sufficiently high then the carriers in the semi-conductor collide with atoms in the crystal lattice, and the resultant ionization creates more electron – hole pairs.

2.2 TRANSIMPEDANCE AMPLIFIERS

A transimpedance amplifier is the preamplifier block which converts the current signal from the photodetectors into a voltage and passes it to post amplifiers for further processing. Its transresistance is defined as the change in the output voltage to the change in input current. Below are some important parameters being discussed for the transimpedance amplifier

- Input Overload current: Transimpedance amplifier exhibits severe pulse width distortion and deterministic jitter, if the input current exceeds a limit. This limit is defined as the input overload current.
- Maximum Input current for linear operation: The maximum input current for which the output of the transimpedance amplifier is not saturated is defined as the maximum input current for linear operation. A more precise definition can be based upon total harmonic distortion (THD), a practice adopted in industry.

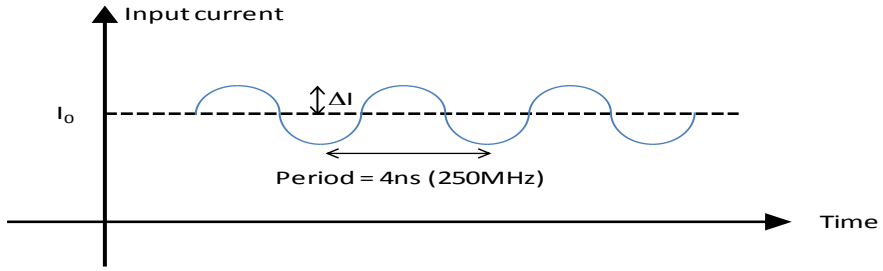


Fig.2.12 Input current for THD testing

To test the linearity of an optical receiver (or transimpedance amplifier), a sinusoidally modulated current is injected into the optical receiver (see Fig.2.12). Using a spectrum analyzer the harmonic components at the output are then measured. The THD is then calculated as:

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_{10}^2}}{V_1}$$

where V_1 is the amplitude of the fundamental component, and $V_{2\ldots10}$ are the amplitudes of the 2nd till the 10th harmonic (usually, contributions from harmonics beyond the 3rd harmonic are negligible).

The extinction ratio of the input ($\Delta I / I_0$, see Fig.2.12) is usually maintained at 6dB. The THD needs to be sufficiently low for the application at hand: a typical value is for example 5%.

- Input referred noise current: The noise contributed by TIA (transimpedance amplifier) is known as the input referred noise and is a very crucial parameter for determining the electrical receiver sensitivity. It is defined as $i_{n,TIA}^{rms} = {i_s^{p-p}}/{2Q}$. where Q is a factor which is related with BER (Bit error rate) and it is values is given in Table 2.4 [57] and I^{p-p} is defined as the peak to peak input current

Q	**BER**	**Q**	**BER**
0.0	½	5.998	10-9
3.090	10^{-3}	6.361	10^{-10}
3..719	10^{-4}	6.706	10^{-11}
4.265	10^{-5}	7.035	10^{-12}
4.753	10^{-6}	7.349	10^{-13}
5.199	10^{-7}	7.651	10^{-14}
5.612	10^{-8}	7.942	10^{-15}

Table 2.4 relationship of Q and BER

- Bit Error Rate: The ratio of wrong bit decisions to the total number of transmitted bits. It should not exceed a given value (e.g. 10^{-3} if forward error correction (FEC) is used, or e.g. 10^{-12} for high-speed short-reach interconnect applications which cannot afford the overhead of FEC). The BER defines the Q-factor as above, and then sets the maximum allowable input referred noise current.
- Sensitivity: Sensitivity is defined as the minimum input signal detected by TIA at the permissible bit error rate of the system
- Bandwidth: TIA bandwidth is defined as the frequency at which the amplitude response of the system drops by 3 dB.
- Group delay variation: Group delay is defined as the transit time of a signal through TIA versus frequency. It gives an indication how much the TIA distorts the input signal. A typical specification would be for example to have no more than 10 ps ($1/10^{th}$ of the bit period) group delay variation from 0 to 7.5 GHz for a 10 Gb/s TIA.

2.3 DESIGN IN DEEP SUBMICRON CMOS TECHNOLOGY

Fig.2.13 provides the flow chart which outlines the methodology followed while designing the circuits in the deep submicron CMOS technology. A lot of focus is given to the verification of the circuits to ensure that the specification is met at every step of the designing process. It starts with the feasibility study of the projects which deals with the selection of the process technology and overall system specifications. Once the feasibility study is done then the whole system is further divided into blocks and the design at the transistor level of the blocks begins.

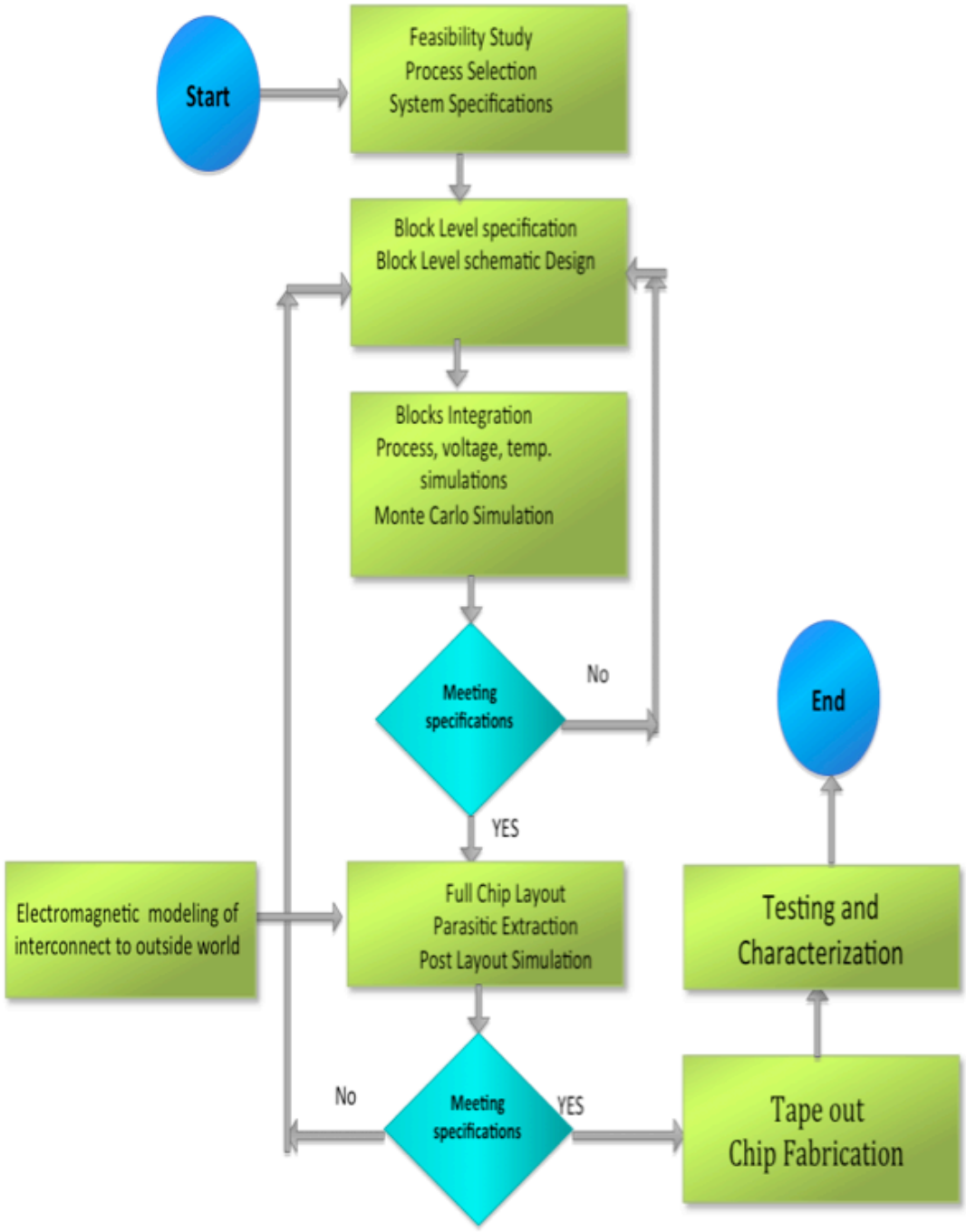


Fig2.13 Circuit Design Flow Chart.

The blocks go through various set of standard simulations which are the PVT (Process, Voltage and Temperature) variations, Monte Carlo simulations and then all the blocks are integrated and the same set of simulations processed on the

entire system. If the system meets the specifications as defined earlier then the next step is to start the layout of the chip and extract the interconnect (R and C for 'small' blocks, with full R, L and C extraction if there are long lines in the layout; additionally STI effects can now also be taken into account). Simulations with the back annotated netlists are then performed and the circuit schematic and layout are fine-tuned to meet the specification. After the completion of the layout next big step is to run simulation replicating the environment in which the chip will be tested. Especially the impact of bond wires and other packaging parasitics need to be taken into here, if required 3D electromagnetic tools can be used to extract equivalent circuits. The blocks which fail to meet the specification at this stage is then redesigned again. After all the verifications are done and the designer is satisfied with the results then the chip is sent for fabrication after which when it comes back it is tested.

The bandwidth of the circuit designs for the short reach optical interconnects presented in this work are above 25 GHz hence the choice for the process technology in which these have to be implemented is an important consideration. As the digital technologies is moving very fast towards deep submicron 65 nm and 28 nm CMOS it is essential that the analogue and mixed signal chips also use the same technologies to build up the analogue functions. There are both advantages and challenges faced while designing circuits using deep submicron CMOS technologies and they are listed below.

2.3.1 Advantages of designing circuits in deep sub-micron technologies

- Higher transition frequency f_T: the f_T of a transistor is defined as the maximum frequency for which the amplitude of the current gain is equal to 1, after this frequency the current gain starts to fall down below 1 so it is not feasible to design circuits with bandwidths close to the f_T of a transistor.

Usually broadband circuits (operating from eg. dc up to many GHz) require transistors with f_T's that are several times higher than the maximum frequency that needs to be handled. The speed at which the optical communication circuits functions it is needed to use a deep sub micron technology for their designs[58]. The f_T of the process technology that is used in the design is more than 100 GHz and there are designs fabricated and tested at very high speed. One such design is the LNA (Low noise amplifier) for 100 Gbps fibre optic SCM transceiver [59]. Fig. 2.14 shows a trend in f_T of transistors in future.

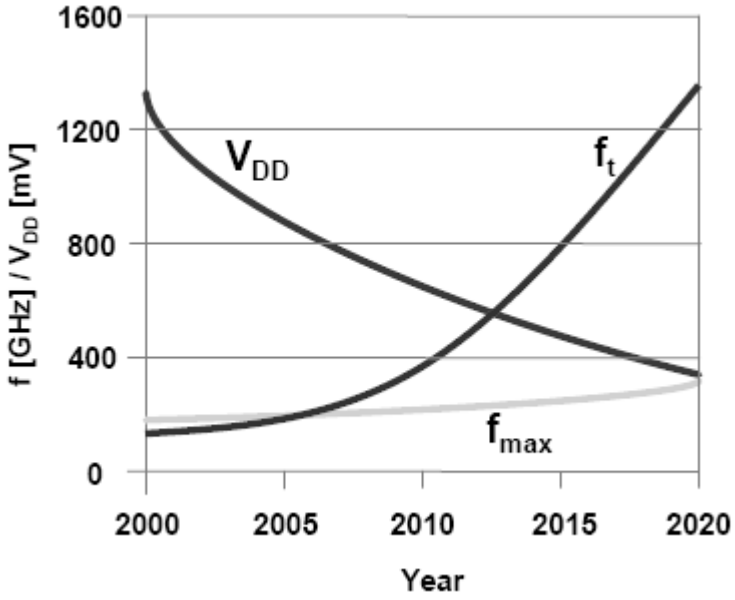


Fig.2.14 Trends of the MOSFET scaling

- Deep (triple) N-well process: Deep N-well is a process in which the bulk of the NMOS transistors are isolated from the substrate, see Fig.2.15. It gives the designer a choice to bias the NMOS bulk at higher voltages than the normal substrate voltages. It also allows to isolate the transistors of the analogue block from switching noise of digital parts or other analogue parts being coupled into them. Deep submicron technologies have these

transistors and it increases the performance of the circuits with more control over threshold voltage variation by tuning the well voltage [60, 61].

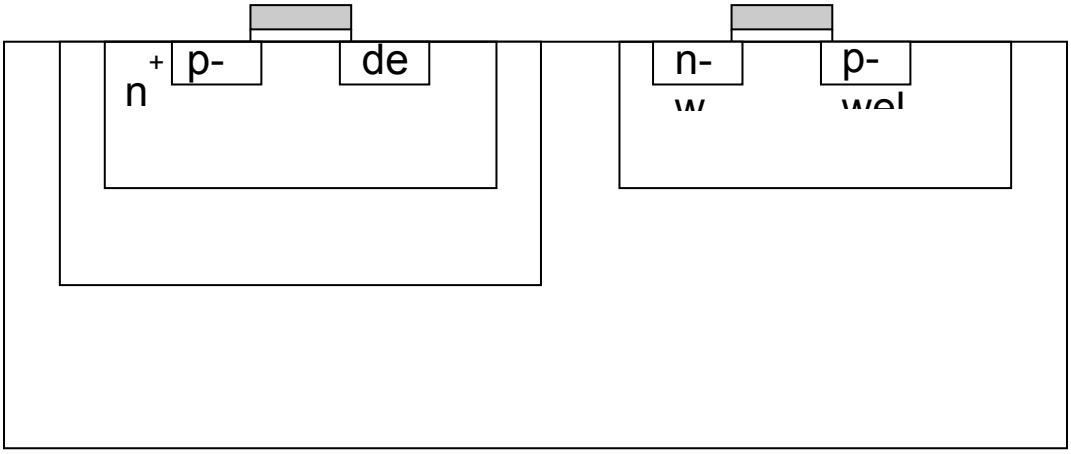


Fig.2.15 Triple N-well Process

- Low supply voltages: Short reach optical interconnect needs a very competitive figure for power consumption for it to replace copper. Deep submicron technologies have fast switching transistors available which function at low supply voltages (e.g. 1V for 65 nm CMOS) enabling the designer to design circuits having lower power consumption [62].

- Passive Components: Eight layers of metals available are available in deep sub-micron technologies which enables the designers to have various useful passive components such as inductors, MoM capacitors, and transmission lines [63]. Apart from that these many metal layers may also make these passive components small and hence help in reducing the size of the chip. One example are the creation of differential inductors [64].

2.3.2 Challenges faced while designing circuits in deep sub−micron CMOS technologies

While shrinking the size of transistors in general increases the performance of digital circuits (although for example also digital circuits suffer from new effects, such as for example leakage currents), it is also recognized that analog circuit performance does not scale well with shrinking transistor sizes: indeed apart from

having a high f_T, there may be more challenges attached to designing circuits in deepsubmicron CMOS than advantages:

- Increased process and mismatch spread: especially for technology nodes below 90 nm, process and mismatch have become considerably worse. Deep sub-micron technologies have a lot of parameters in their models and for designers to verify the design under process, temperature and power supply variations, one has to run thousands and thousands of simulations for one design. For example to verify a design in 65nm ST micro technology which uses two components (one transistor and one resistor) across PVT (process, voltage and temperature) variations designer has to run 768 simulations for one condition.

- Low voltage headroom: while a low supply voltage is an advantage for the designers to design circuit for low power consumption, it also creates a challenge as it becomes very difficult to stack the transistors in the design. Additionally, wide voltage swings are challenging to handle. The fact that one cannot easily stack transistors for example has consequences for widely used cascode stages which can be used of high gain is required. Instead of stacking transistors, the design should cascade several stages in series to achieve high gain, for example in operational amplifiers. Such multistage amplifiers are very difficult to compensate in a feedback loop.

- Tools: As the length of the gate is shortened as in the case of deep sub-micron technologies there are many short channel effects that start to take place[65, 66] which cannot be captured in a simple model nor formula: for example the BSIM4 model contains a few hundred parameters. While simple models and hand calculations are still invaluable to provide insight in the circuit operation, on the other hand the design process needs to rely extensively on the simulations tools available to the designers. Especially for analog functions, this requires long design times and a lot of iterations. This is even worse for high-speed design since the impact of layout parasitics needs to be taken into account, hence iterations between schematic design and layout are required.

- Parasitics: As the transistors scale down, the width of metal wires connecting them needs to shrink accordingly: this implies that resistance becomes a major issue on top of the interconnect capacitance[67]. This is especially a challenge for wideband circuits and requires the designer to layout the design very carefully and estimate the parasitic elements of every node.

- Impact of the layout arrangement on the transistor parameters (eg short trench isolation, well proximity effects): in the deep submicron nodes (65nm or lower) not only the interconnect parasitics need to be backannotated, but there are also effects from the transistor mask layout on e.g. its threshold voltage. Such effects can have a dramatic effect on the performance of the circuit and need to be carefully considered.

2.4 SUMMARY

For the circuits that are designed to be implemented in the optical links used in the short reach optical interconnect application with speed ranging from 40 G to 100 G one needs to use deep sub-micron technologies such as 65 nm or 28 nm with VCSEL as the light source transferring data using multi-mode fibre. The chip designed must have techniques implemented for lower power consumption and must have small sizes. The transmitter must be designed for currents that take into account all the losses in the link and should have extinction ratio varying between 6-10 dB. The receiver for the optical links must be designed to have minimum noise at the input of TIA so as to detect the minimum input signal and should have high bandwidth and small group delay for low jitter requirements of the link. Additionally, the receiver may need to be linear especially for multilevel modulation formats.

3
40G NRZ VCSEL DRIVER

In this chapter, the design of the high-speed, low power VCSEL driver for non-return to zero modulation is reported. First, the main functionality and requirements are outlined. Next, the transistor level circuit design is addressed, concluding with simulation and experimental results.

3.1 INTRODUCTION AND OVERVIEW OF STATE-OF-THE-ART

As reported in Chapter 2, it is anticipated that within the next five years, short-reach optical links (with a distance ranging from a few meters to hundreds of meters, in some cases going up to 2 km) will need to be able to support >100 Gb/s/fibre on a single wavelength. Applications include datacenters/local area networks (100 G Ethernet and beyond) and high-performance supercomputers (Infiniband, Fibre Channel) and new consumer links such as Thunderbolt. On top of the high-speed requirements, these links must also comply with stringent power consumption, cost and size requirements. The power consumption and size requirements are important to allow for example integration of highly parallel optical interconnects to further increase capacity. The majority of today's deployed short-reach optical links for these applications are typically based on a directly modulated, short-wavelength (e.g. 850 nm) vertical cavity surface emitting laser (VCSEL) and multimode fibres. Pushing the bitrate on such links beyond today's commercially available 10 Gb/s/fibre will require new generations of VCSELs and their driver and receiver electronics. Parallel optical interconnects operating at 10 Gb/s per channel have long provided the solutions for such links as shown in [19, 20] and [18] and at slower data rates for 2-D arrays [21], but for higher level of

integration and cost effectiveness single channel VCSEL drivers operating at higher speed are required.

A 12.5 Gb/s CMOS VCSEL driver was reported in [68]. Due to the parasitic capacitance and non-linear response of VCSELs the optical waveform gets degraded a lot at higher bit rates. To mitigate these issues, VCSEL driver ICs use so-called pre- or de-emphasis circuits or a pre-distortion circuit which can compensate for the distortion introduced by the bandwidth-limited and nonlinear VCSEL.

Pre-emphasis in electro-optical systems operating at 10 Gb/s or higher is needed to compensate for the non-linear characteristics of the VCSEL (Vertical Cavity Surface Emitting Laser). Pre-emphasis allows to pre distort the signal at the electrical driver to compensate for the distortion produced by the non linear behaviour of the VCSEL diode.

The predistortion can be implemented at the electrical driver by superimposing a weighted current signal on the original current signal to speed up the rising and falling edges of the original waveform.

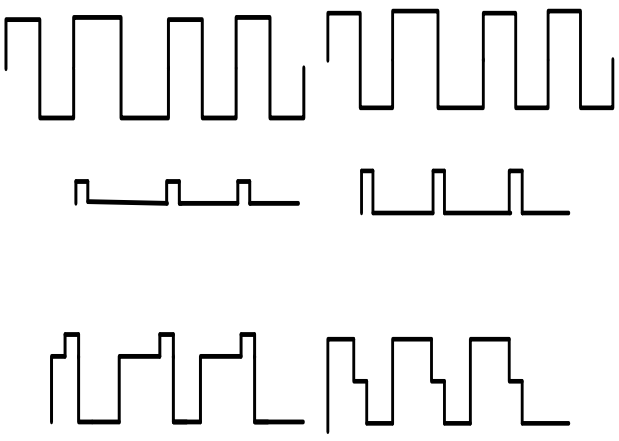


Fig.3.1 Emphasis operation at rising and falling edge

Fig. 3.1 shows the principle of pre-emphasis: an extra pulse of current is injected into the VCSEL during each 1 to 0 transition. As shown in Fig. 3.1, this technique opens up the eye. A 17 Gb/s driver with double pulse pre-emphasis circuit to lessen both parasitic capacitance and ringing is presented in [69]. A 18 Gb/s CMOS VCSEL driver is proposed in [23] which provides digital control of the pre-emphasis pulse duration, modulation current and pre-emphasis current. The fastest CMOS VCSEL driver reported to date operates at 20 Gb/s [24]: falling edge pre-emphasis was implemented. However in [76], [23] and [24] the pre-emphasis techniques relies on differential amplifiers that switched a constant current either to or from the VCSEL (during the data transitions). As this current is always on (regardless wether there is a data transition or not), the reported techniques are not very power efficient. Further in [26] a stack of four transistors, as shown in Fig. 3.2, is used making it very difficult to use this topology at low power supply voltages.

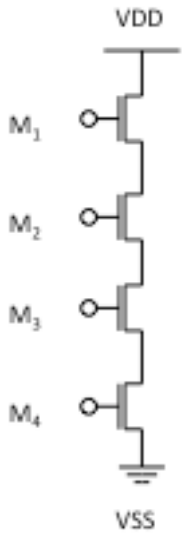


Fig.3.2 Stack of four transistors

The threshold voltage of the transistors which are used in the design is around 250 mV which makes it impossible to maintain the stacked transistors in their saturation region for a deep sub micron process which has a power supply voltage as low as 1.2V.

The design proposed in this work uses both rising and falling edge emphasis to maximize the vertical eye opening, facilitating operation at 40 Gb/s. Additionally, the emphasis circuit is constructed in a such a way that current is mainly drawn when the emphasis pulses are present thus reducing the power consumption. Finally, pulse-width control is added to widen the horizontal eye by reducing the offset or threshold error in the driving circuit and by shortening the turn-on delay time of the VCSEL diode[57].

3.2 GENERAL DESCRIPTION

The VCSEL driver is designed to directly modulate VCSEL chips at speeds up to 40 Gb/s. Low power consumption is achieved by using a low core supply voltage (1.2V).

The VCSEL driver is intended to be connected to the VCSEL with very short bonding wires in a common-anode configuration, see {Fig. 3.3}.

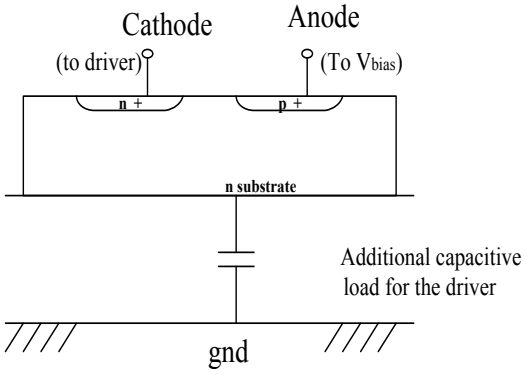


Fig.3.3 Common-Anode Connection

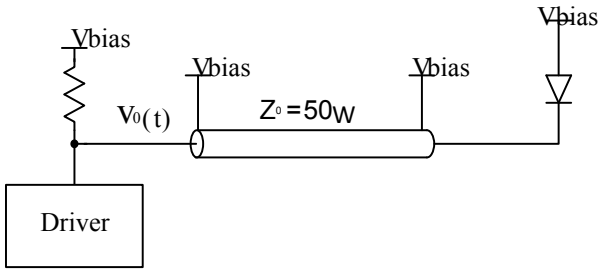


Fig.3.4 VCSEL driver with termination resistor

If the connection between the driver and VCSEL is long, and as the characteristic impedance of the VCSEL is not well defined, a driver-side termination resistor is required to absorb any reflections from the VCSEL as shown in Fig. 3.4. In the VCSEL driver which is designed and presented here the connection between the driver and the VCSEL are with very short bonding wires, shown in Fig. 3.5, thus allowing the elimination of termination resistor and hence significant additional power savings. If 10 mA of bias and 10 mA of modulation current is needed for the VCSEL to operate then the same amount of extra current is needed which goes through the termination resistor. So if the termination resistor is eliminated then atleast 50% of current consumption is saved. A decoupling capacitor is foreseen on-chip to provide a clean bias voltage to the VCSEL anode.

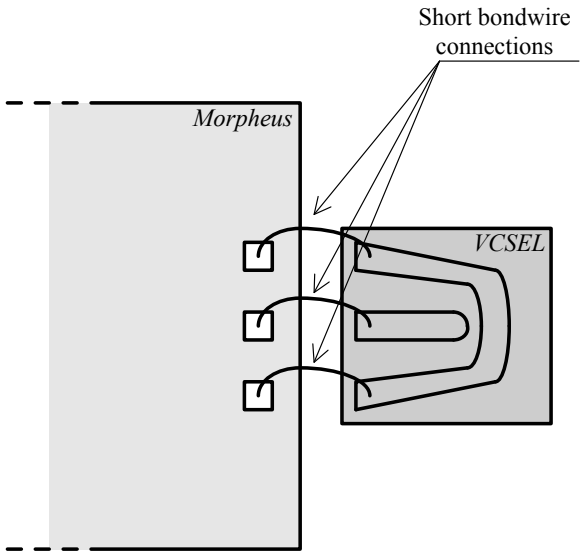


Fig.3.5 Driver Connection with VCSEL

The driver features adjustable rising and falling edge pre-emphasis, as well as an adjustable eye cross-point, all programmable via on-chip registers. These features allow optimization of the eye opening. Bias and modulation currents can also be programmed through on-chip registers.

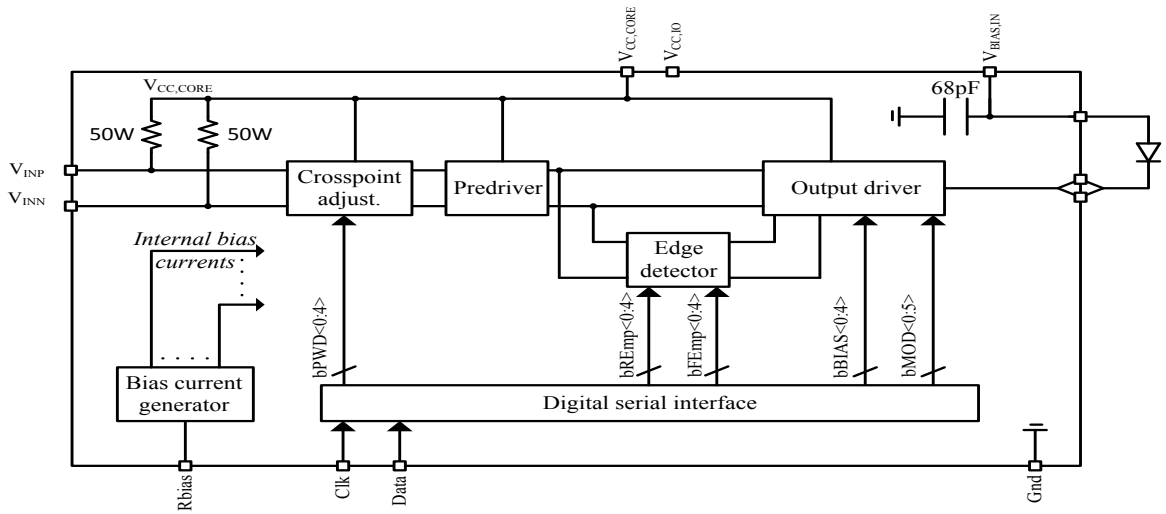


Fig.3.6 Functional block diagram of the VCSEL driver.

A functional block diagram is given in Fig. 3.6. The differential input signal (VINP,VINN) is provided to the 'Pulse-Width adjust.' block, where the horizontal crossing point is shifted by an amount programmable through a register (bPWD<0:4>). This signal in turn is provided to a pre-driver, which drives both an edge detector, as well as the output driver. The edge detector signals the edges in the input signal and has two outputs, V_{RE} and V_{FE}. Whenever a positive edge is detected, a short pulse is generated on the V_{RE} line, whenever a negative edge is detected; a short pulse is generated on the V_{FE} line, as shown in Fig. 3.7. These signals are then combined with the actual data signals in the output driver to generate a current whose general shape is shown on Fig.3.8.

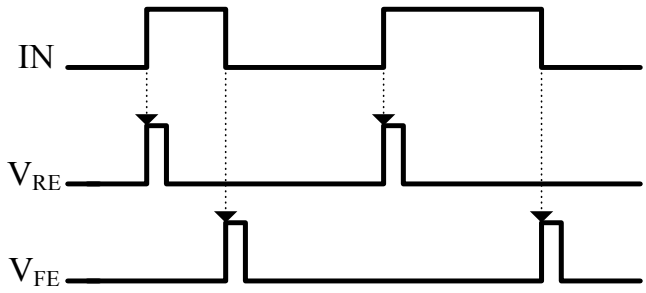


Fig.3.7 Functionality of the edge detector.

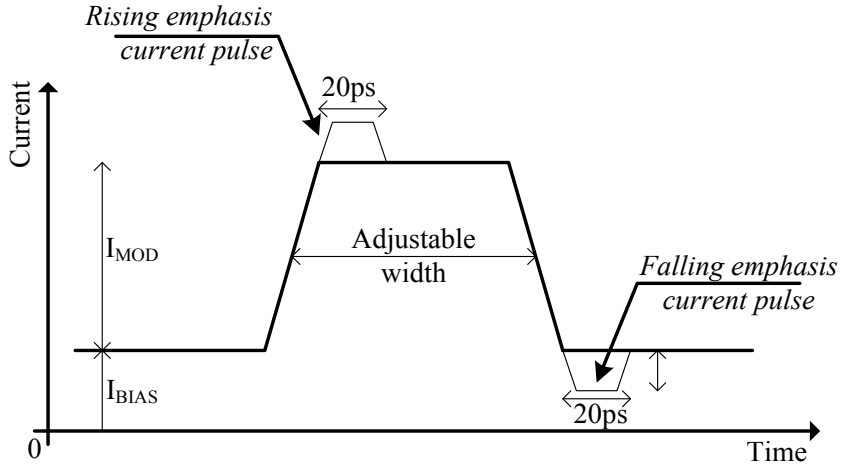


Fig.3.8 Shape of the output current waveform.

The output driver combines the programmable bias, modulation, rising and falling edge currents and switches them towards the VCSEL cathode. An on-chip 68 pF decoupling capacitor is provided to provide a clean bias voltage to the VCSEL anode. Table 3.1 provides the required specifications of the designed VCSEL driver.

Parameter	Min.	Typ.	Max.	Unit	Remarks
BIAS CURRENT (I_{BIAS}) Full-scale current Resolution		 5.1 20		 mA µA	 +/- 5%
MODULATION CURRENT (I_{MOD}) Full-scale current Resolution		 100		 µA	
RISING EDGE PRE-EMPHASIS I_R Full-scale current Resolution		 3.75 250		 mA µA	 +/- 5%
FALLING EDGE PRE-EMPHASIS I_F Full-scale current Resolution		 3.75 250		 mA µA	 +/- 5%
Input data range	20		40	Gb/s	
Differential input swing	0.4		0.8	V	ac-coupled
Common-mode input voltage	0.8	0.6	0.4	V	
Differential input resistance		100		Ω	
Single-ended input resistance		50		Ω	

Table 3.1: Specification of VCSEL Driver

3.2.1 Pulse–Width Adjustment block

Electrical output pulses can be lengthened or shortened (compared to the bit period) by unavoidable dc-offsets or threshold errors in the driver circuitry. Additionally the turn-on delay of the VCSEL will shorten the optical pulses as represented in Fig. 3.9

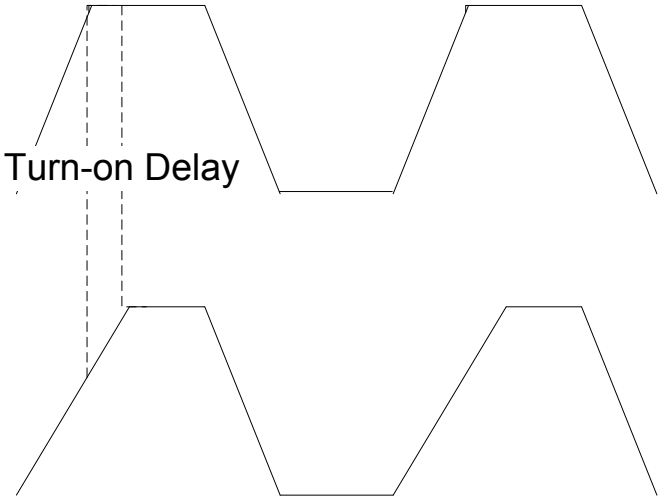


Fig.3.9 Optical pulse shortening due to turn- on delay in VCSEL

This kind of pulse lengthening or shortening is known as pulse-width distortion (PWD). If the crossing point is vertically centered, the PWD is zero as shown in Fig. 3.10.

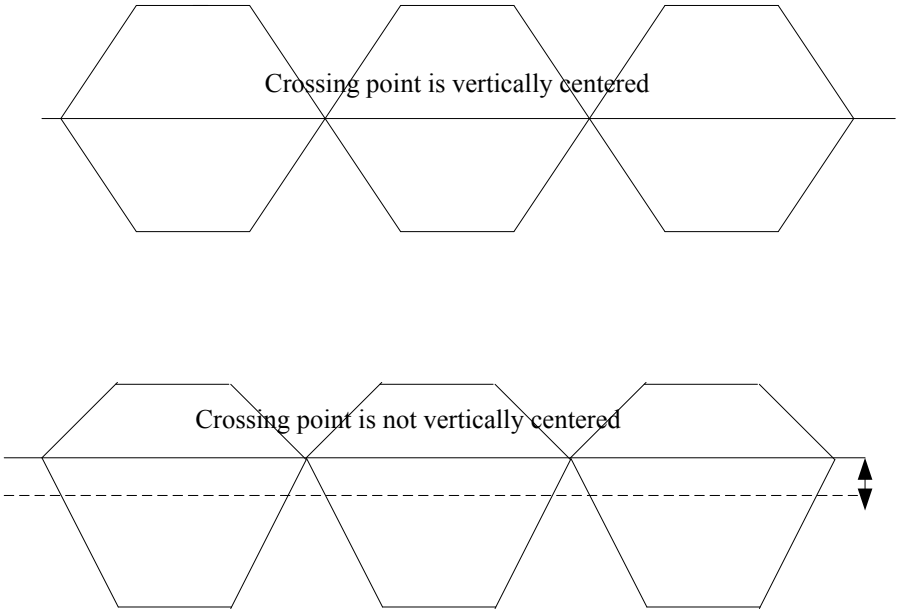


Fig.3.10 Pulse Width Distortion due to pulse lengthening or shortening

Under this condition the horizontal eye opening is maximized as well. To accomplish this despite imperfections in the driver circuitry and the turn-on delay of the VCSEL, the VCSEL can be driven with a pre-distorted signal. Fig.3.11 shows the circuit diagram of the Pulse-Width adjustment block, where the pulse-width pre-distortion is introduced.

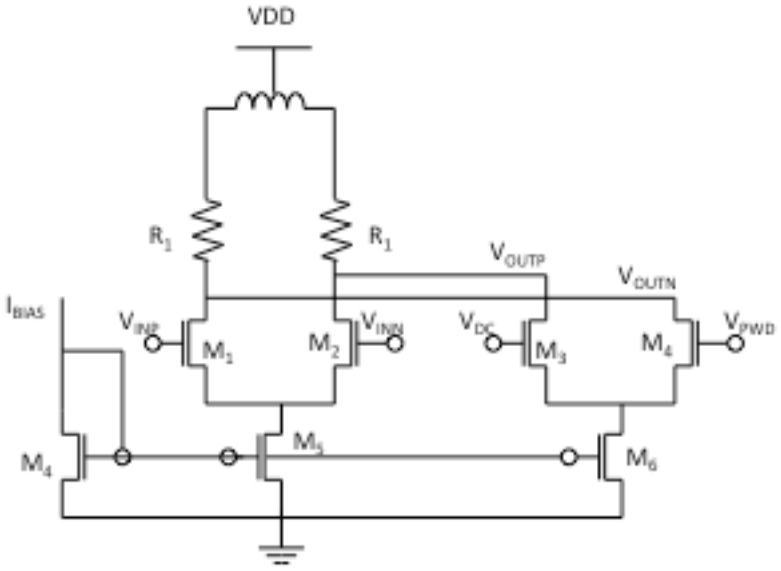


Fig.3.11 Cross-point adjustment block.

It has a differential pair M_1,M_2, load resistors R_1,R_2 and a peaking inductor L_1 (supply connection through a center tap). Adjustment of the pulse-width is provided by differential pair M_3,M_4 which create an imbalance in the currents provided to the load resistors R_1,R_2 and peaking inductor L_1[70]. The voltage at the input (VDC) of M_3 is fixed and the voltage at the gate of M_4 (VPWD) is varied which is controlled by a programmable register as shown in Fig.1. When VPWD is varied higher or lower than VDC it creates an offset due to the different amount of current sinked by the differential pair M_1, M_2. Finally this signal is recovered by passing it through a limiting circuit, which also acts as a pre-driver. Fig.3.12 gives a graphic illustration of how this block works.

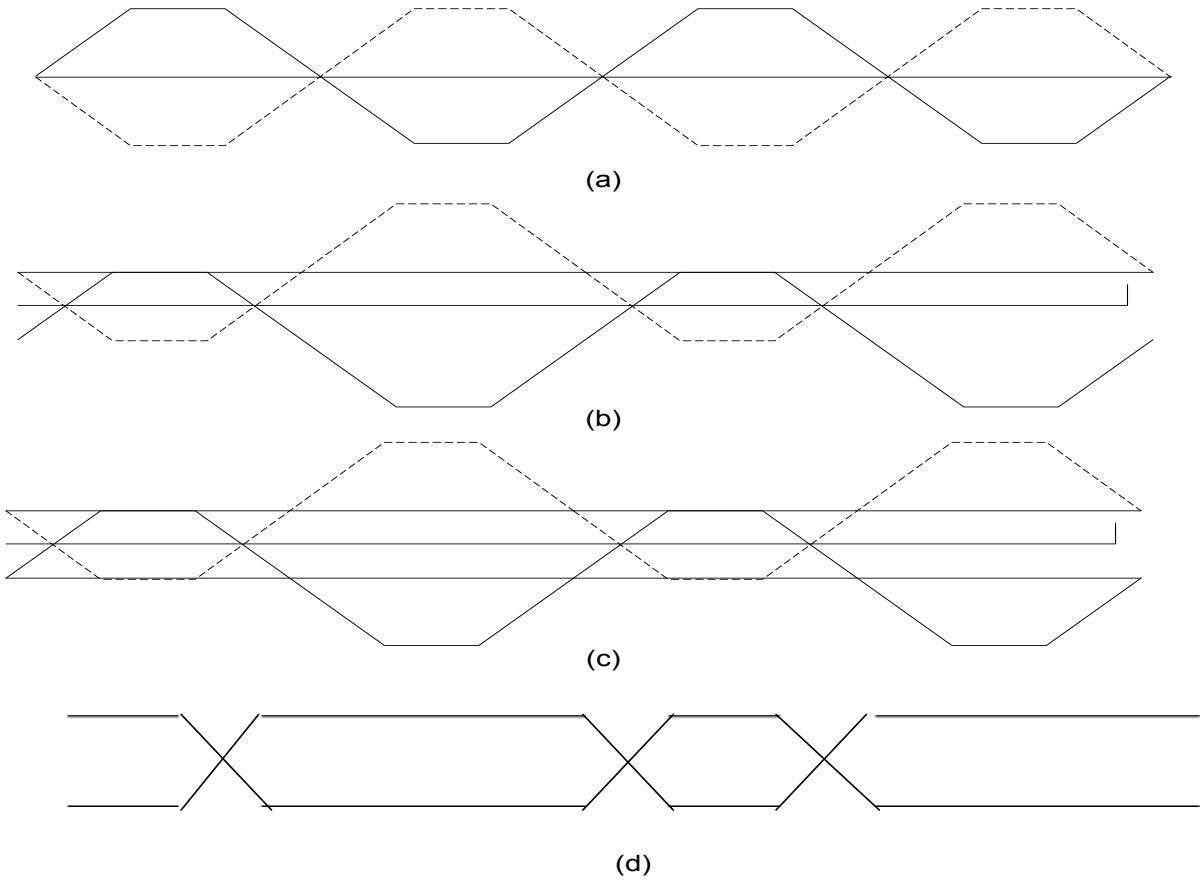


Fig.3.12 Pulse-Width adjustment signal flow. (a) Signal at the output of the differential amplifier M_1 and M_2. (b) Signal at the output of the differential amplifier after applying the dc offset through the second differential amplifier M_3 and M_4 by varying VPWD. (c) Amplitude limiting function of the next stage (Pre-Driver Block). (d) Final signal with modified pulse-width.

3.2.2 PRE–DRIVER BLOCK

To drive the large transistors in the main driver and to act as a limiter for the pulse-width adjustment circuit, an additional stage is added. Inductive peaking and local feedback is used to enhance the bandwidth Fig. 3.13 shows the circuit diagram of this pre-driver block. The local feedback works by returning a fraction of the output back to the input using transconductance stage M_5 and M_6.

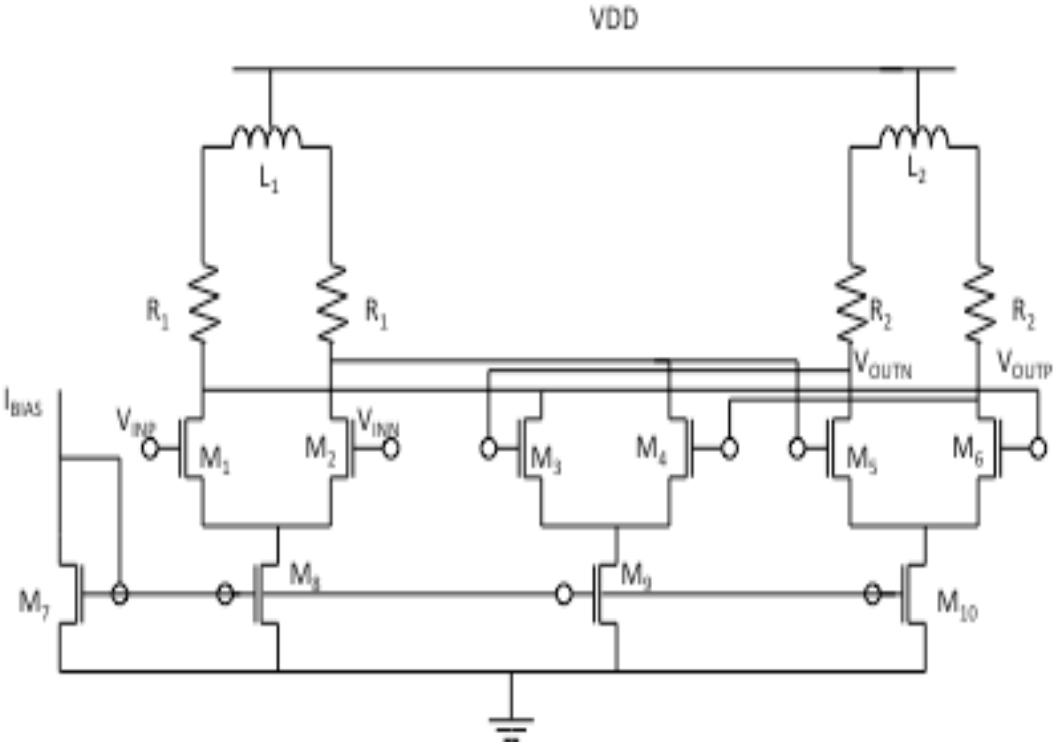


Fig.3.13 Pre-Driver

For analysis purpose an active feedback structure is presented in Fig. 3.14

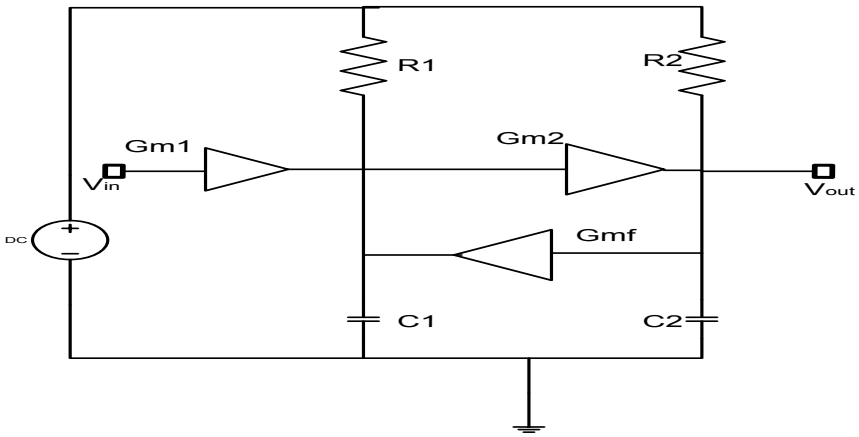


Fig.3.14 Active feedback structure

A single-ended, small signal equivalent of the local feedback structure is given in Fig. 3.14. The transfer function of the circuit is given by: [71]

$$\frac{V_{out}}{V_{in}} = A_{vo}\frac{\omega_n^2}{s^2+2\zeta s+\omega_n^2} \qquad (3.1)$$

where

$$A_{vo}=\frac{G_{m1}G_{m2}R_1R_2}{1+G_{m2}G_{mf}R_1R_2} \qquad (3.2)$$

$$\zeta = \frac{1}{2}\frac{R_1C_1+R_2C_2}{\sqrt{R_1C_1R_2C_2\left(1+G_{m1}G_{mf}R_1R_2\right)}} \qquad (3.3)$$

$$\omega_n^2 = \frac{1+G_{m2}G_{mf}R_1R_2}{R_1C_1R_2C_2} \qquad (3.4)$$

ζ is given as $1/\sqrt{2}$ for maximally flat response and 3 dB bandwidth is $f_{-3dB} = \omega_n/2\pi$

Multiplying (3.2) and (3.4) we get

$$A_{vo}\omega_n^2 = \frac{G_{m1}G_{m2}}{C_1C_2} \qquad (3.5)$$

Since ${G_{m1}}/{C_1}$ and ${G_{m2}}/{C_2}$ nearly equals $2\pi f_t$, (3.5) can be rewritten as:

$$A_{vo}\omega_n = f_t \frac{f_t}{f_{-3dB}} \qquad (3.6)$$

Since$f_t > f_{-3dB}$, the local feedback can increase the gain bandwidth product beyond f_t.

Since the transfer function has two poles (a 1st pole at the drains of M_1,M_2 and a 2nd pole at the drains of M_5,M_6), without the local feedback the bandwidth would be limited.. However, the feedback stage consisting of M_3 and M_4 introduces a peaking in the gain response of first stage (M_1 and M_2). If this peaking falls into the frequency range where the voltage gain of second stage starts to decrease, then it compensates the gain roll-off of the second stage, therefore improving the gain bandwidth product.

3.2.3 Rising and Falling Edge Detector

The schematic of the pulse generators are shown in Fig. 3.15. The design works on the principle that when both the inputs to the gates are low then the output is pulled to high. For that the NOR gate has opposite phase inputs with one of its input is delayed in relation to the second input.

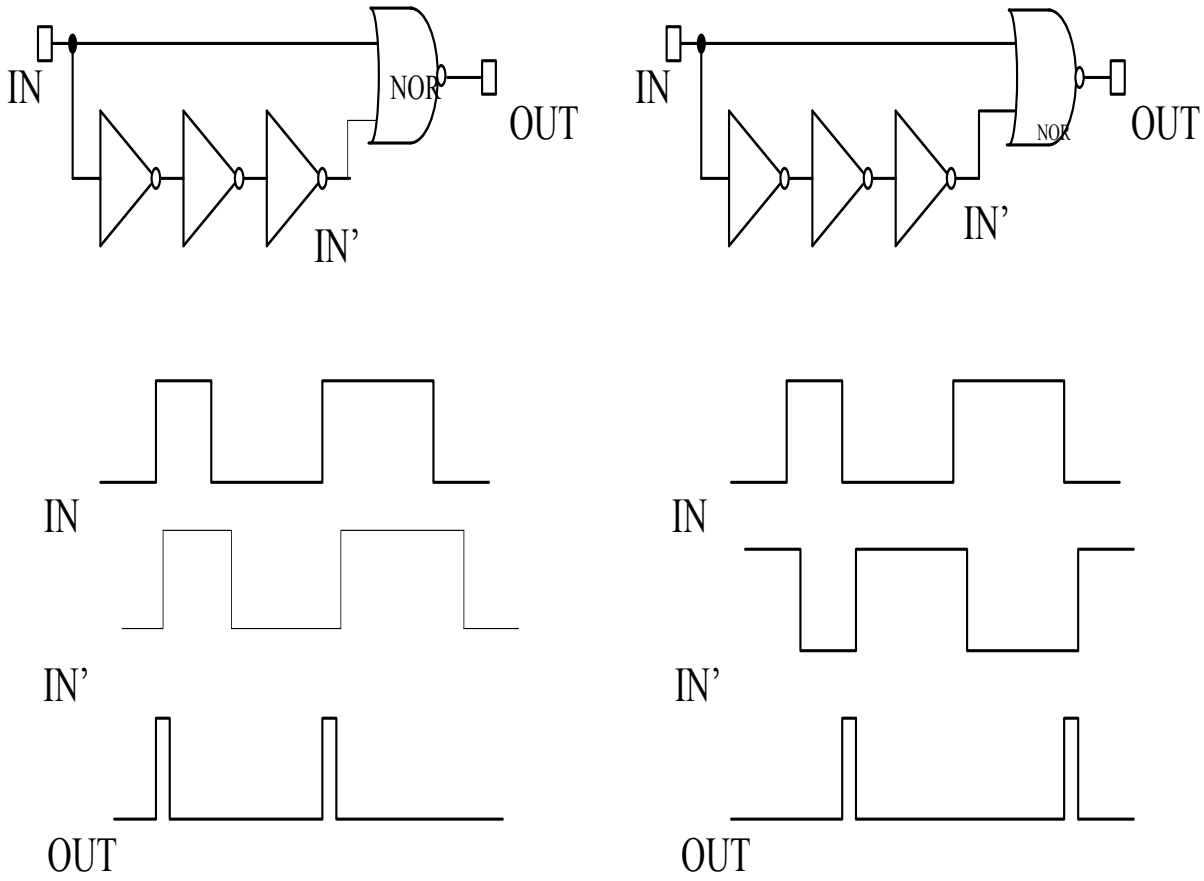


Fig.3.15 Pulse Generator schematic

Conventional CMOS logic is not fast enough, hence CML NOR gates [72] were used here as shown in Fig. 3.16.

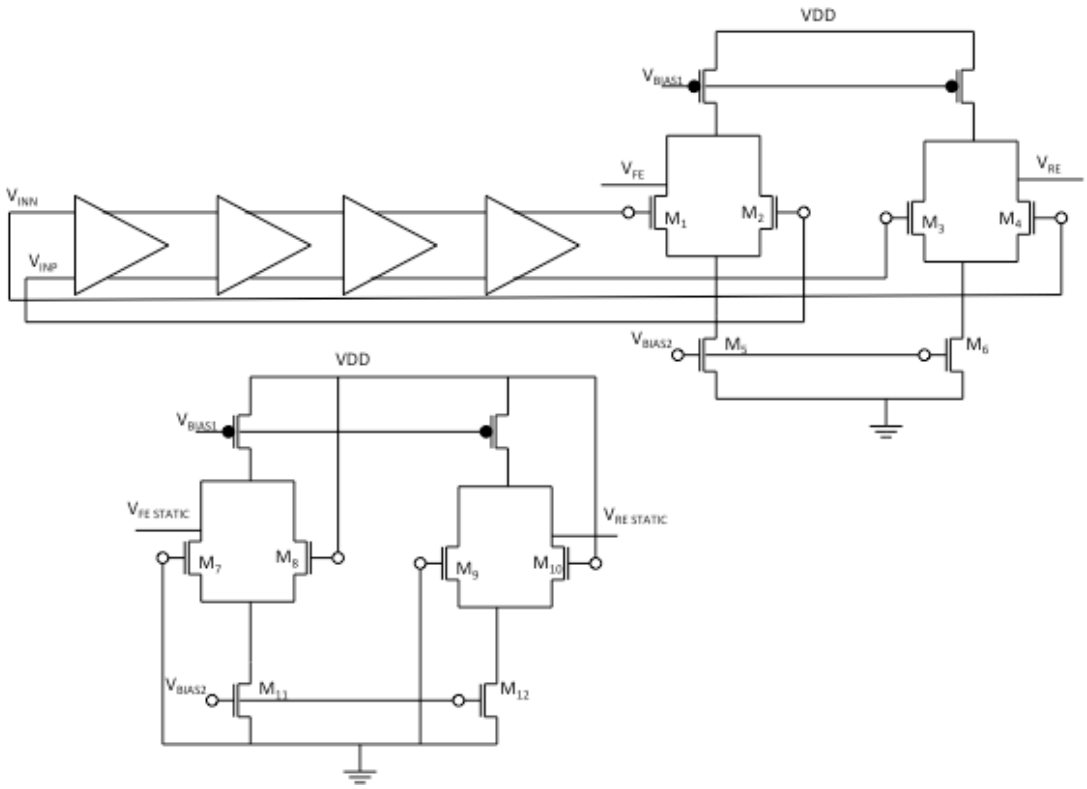


Fig.3.16 Rising and falling edge detector.

Four buffers constitute the delay required for the pulses, and gates (M_1,M_2), (M_3,M_4) constitute the CML NOR gates. To maintain the differential nature of the design and to have similar loads both phases of the CML input signal are used in the edge generation.

Fig.3.17 shows how the rising and the falling edge are generated.

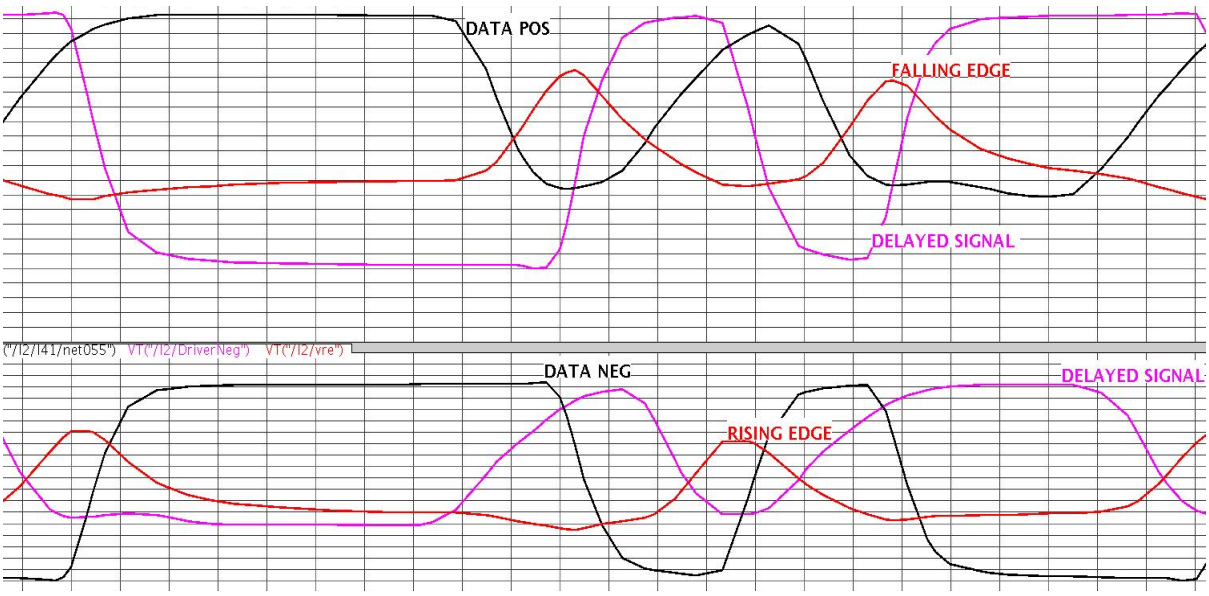


Fig.3.17 Rising and Falling edge generated from Pulse Generator block

The magnitude of the rising and falling edges are adjusted by adjusting $V_{BIAS,1}$ and $V_{BIAS,2}$ which are generated using D/A converters.

3.2.4 MAIN DRIVER WITH EMPHASIS

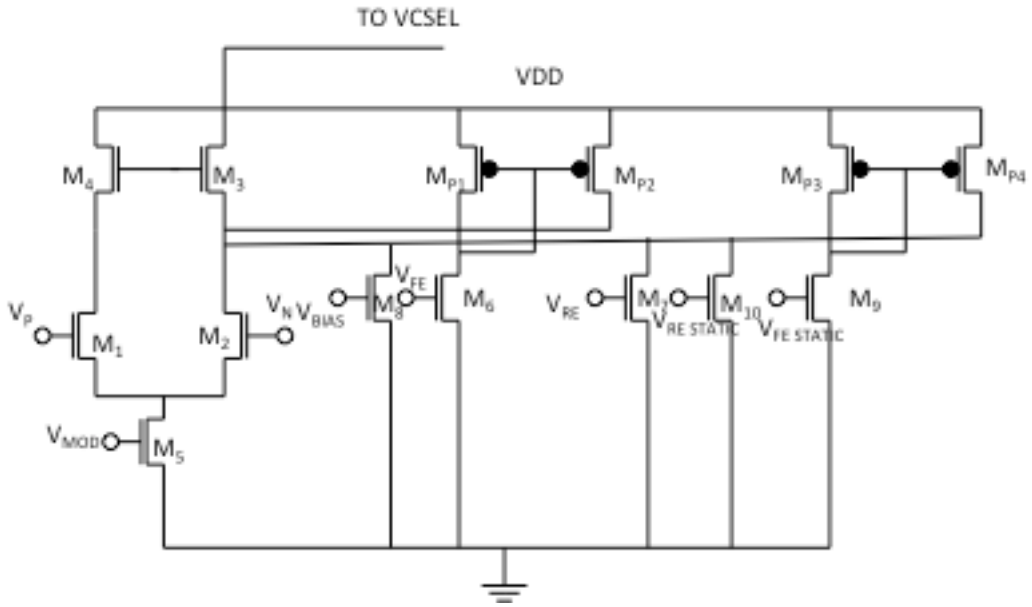


Fig.3.18 Main driver circuit.

Fig. 3.18 shows the schematics of the main driver circuit which provides the modulation current to the VCSEL diode. Transistor M1 and M2 switches the modulation current either towards (for a logical 1) or away (for a logical 0) from the VCSEL. Cascode transistors M3 and M4 are used to isolate the output capacitance of the VCSEL and bondpads from the switching transistors and increase the output impedance of the driver, thus reducing the changes in modulation current as the voltage drop across the VCSEL varies. Modulation current is provided through the tail transistor M_5 of the amplifier and its amplitude is controlled by adjusting V_{MOD} through a DAC (Digital to Analog converters). Higher DC voltage at drain of M_3 does not allow the bias current to be added at that point, and hence has been added at the drain and source connection of M_3 and M_2 respectively through transistor M_8

In this driver the pre-emphasis is implemented using common-source transistors M_6 (falling edge pre-emphasis) and M_7 (rising edge pre-emphasis). If a pre-emphasis

pulse is needed, a pulse voltage is applied to the gate of M_6 or M_7. This pulse is generated by the edge detecting circuit. Due to the use of a CML logic gate the pulse generated do not swing between 0 and VDD, which in turns creates an undesirable DC current at the rising and falling edge emphasis as M_6 and M_7 are never completely switched off. To remove this DC current, an equivalent amount of DC bias voltage (a replica of V_{FE} and V_{RE}) is generated through the replica of CML NOR gates as shown in Fig. 3.16 at V_{FE} Static and V_{RE} Static which then provided to transistor M9 and M10 generates the undesirable DC bias current. Subtracting the two DC bias currents generated by V_{FE} and V_{FE} Static (V_{RE} and V_{RE} Static) brings the zero DC bias conditions which is then added to the VCSEL current. Fig.3.19 and Fig. 3.20 shows how the modulated signal is superimposed with the emphasis pulses and how the final pulse going to the VCSEL diode looks like. Fig. 3.21 shows the layout of the entire chip which was sent for fabrication.

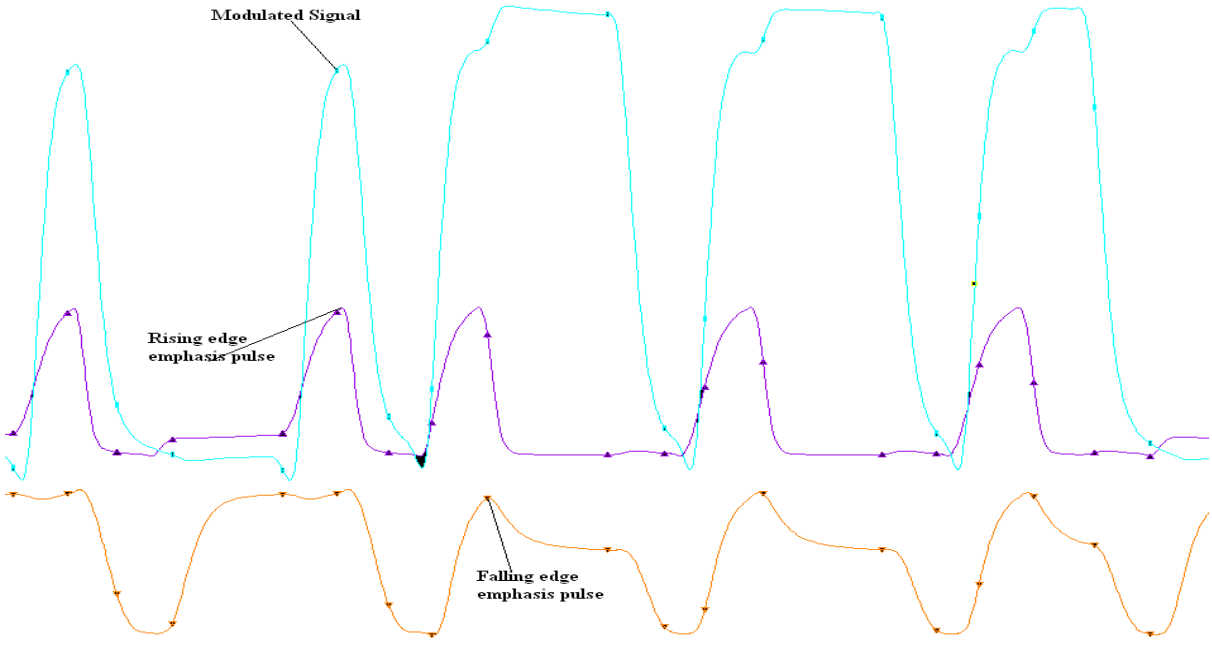


Fig.3.19 Rising and Falling edge emphasis pulses.

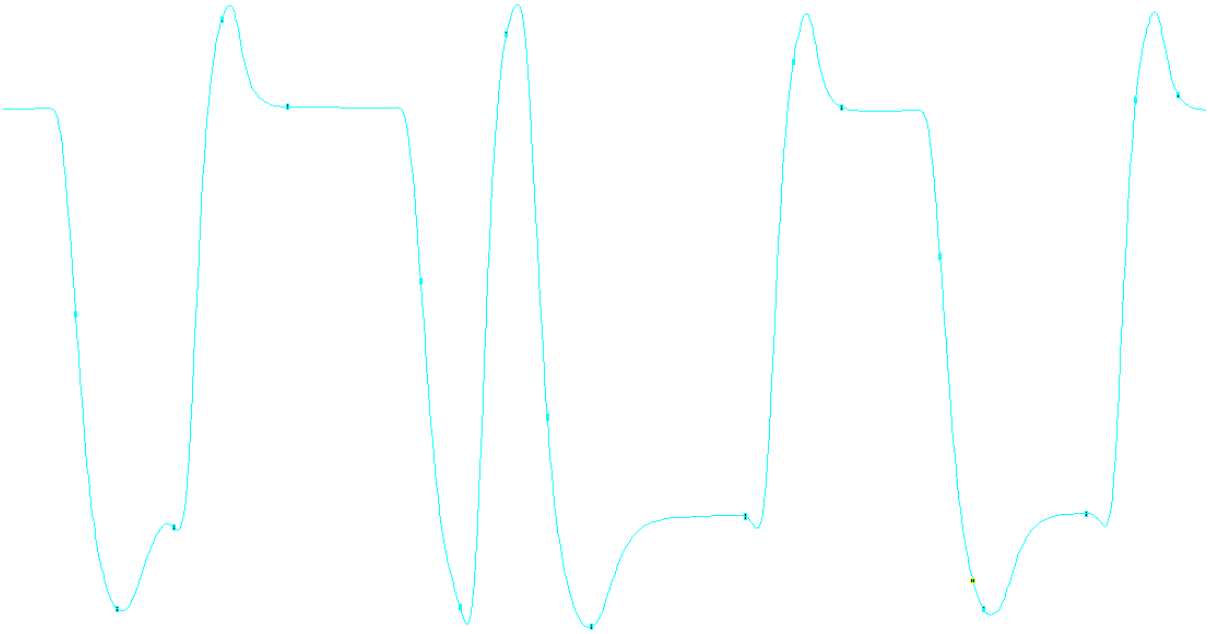


Fig.3.20 Modulated signal after the addition of pre-emphasis pulses

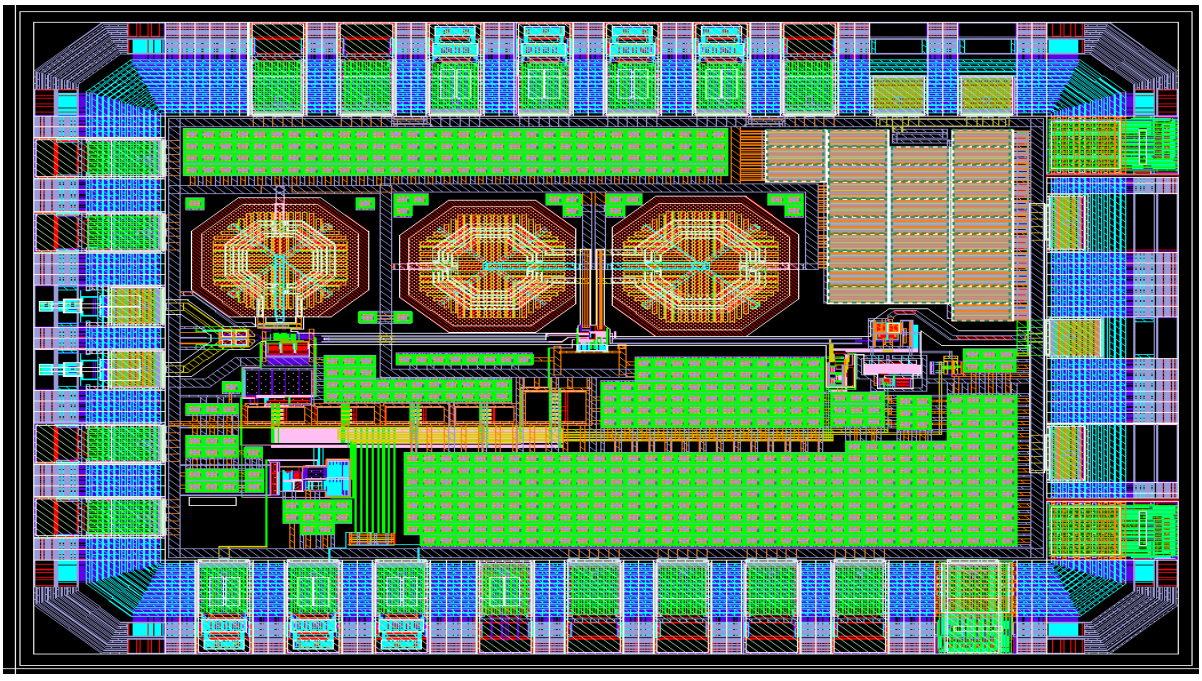


Fig.3.21 Layout of the complete 40Gbps VCSEL Driver for NRZ modulation.

3.3 SIMULATED RESULTS

For the testing of the chip it needs to be assembled on a PCB (Printed Circuit Board) where the chip I/O (input/output) pads will be connected to the PCB pads through wirebonds as shown in Fig.3.22.

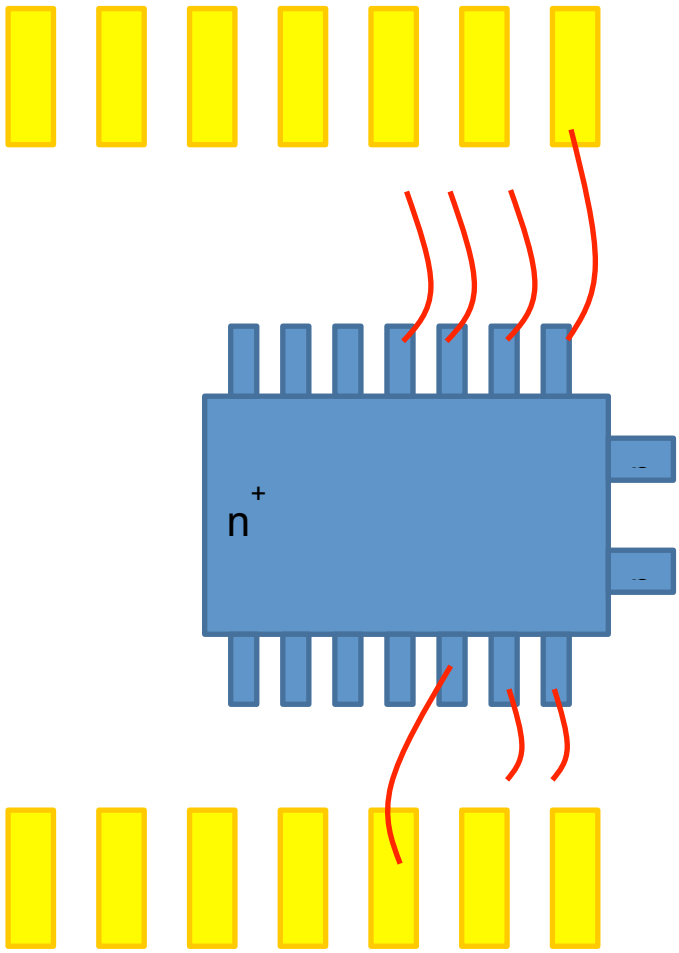


Fig.3.22 Chip Connections with PCB

Correct simulation of the chip requires careful modelling of these bondwires, a simple model (which also included mutual inductance is not shown here) is shown

in Fig.3.23. the bondwire resistance includes both the dc resistance as well as the frequency dependant resistance due to Skin effect.

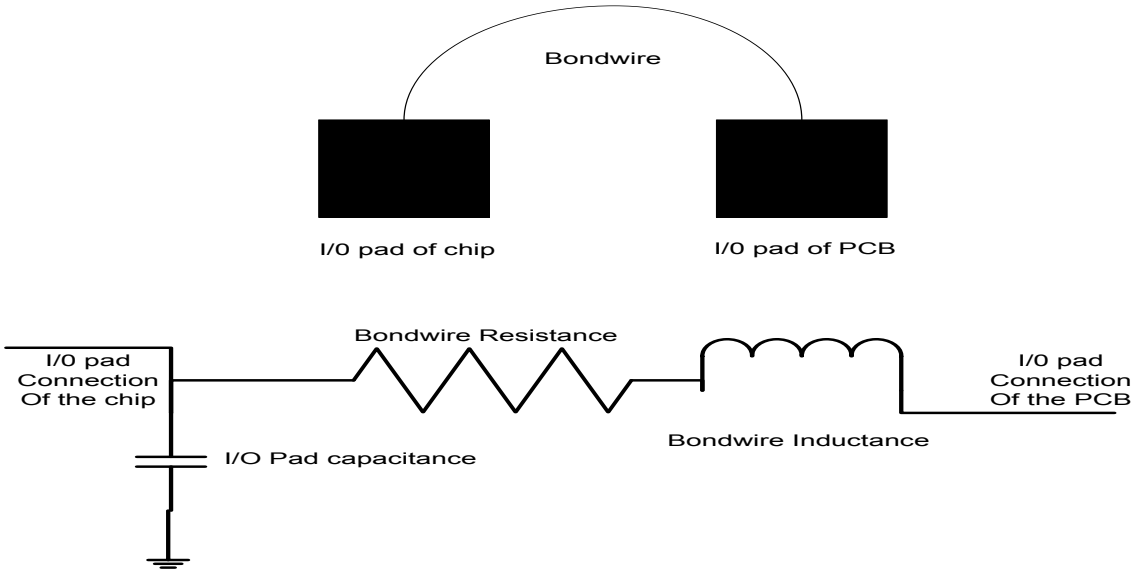


Fig.3.23 Modelling of I/O pads and Bondwires

For the final simulation results the entire chip layout is extracted, such that all parasitic capacitance, resistances, inductances (especially for long lines) are modelled in the design. Then the extracted design is simulated for DC, AC and transient behaviour. Below are some simulated graphs and eye diagrams that are presented as simulation results.

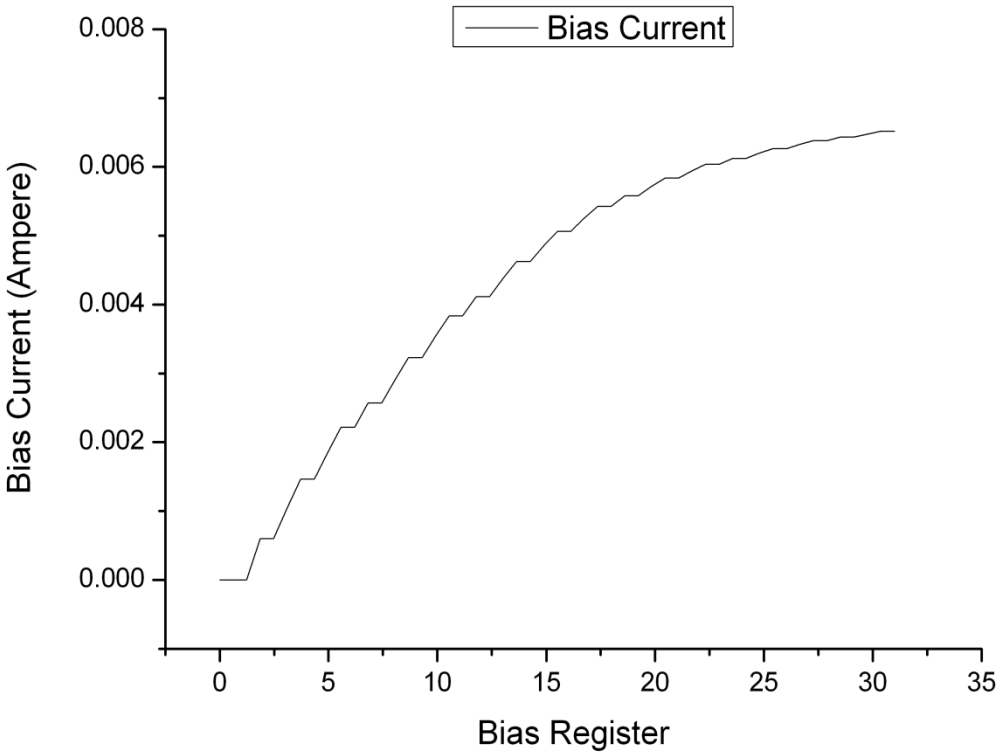


Fig.3.24 Bias current as a function of the bias register value.

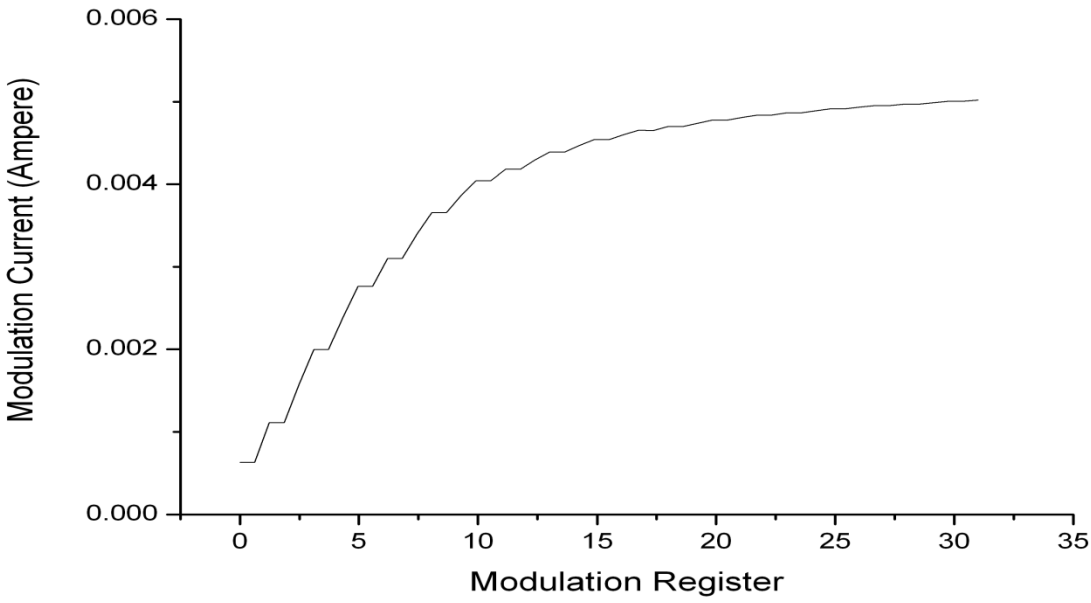


Fig.3.25 Modulation current as function of the modulation register value.

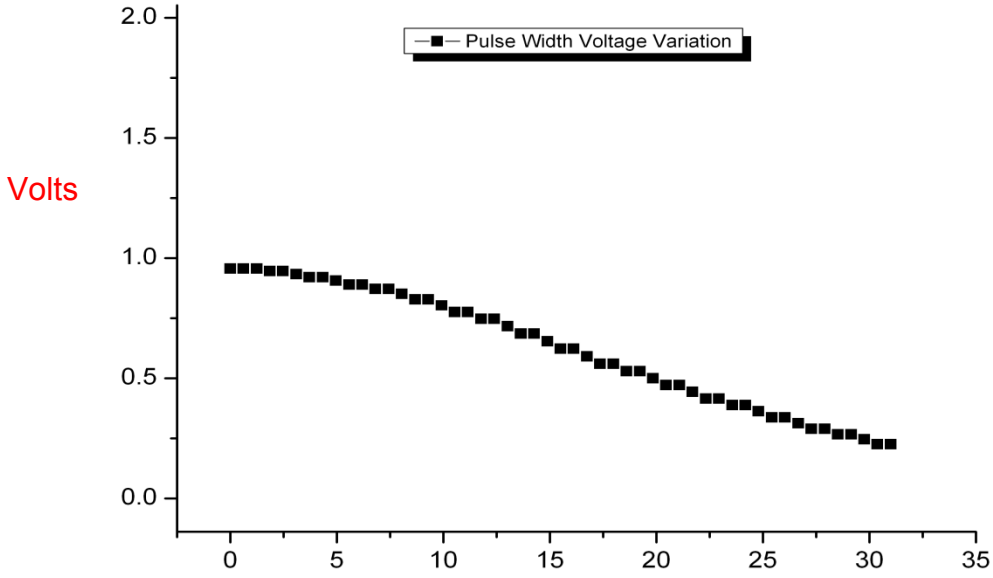


Fig.3.26 Pulse Width Voltage versus register value.

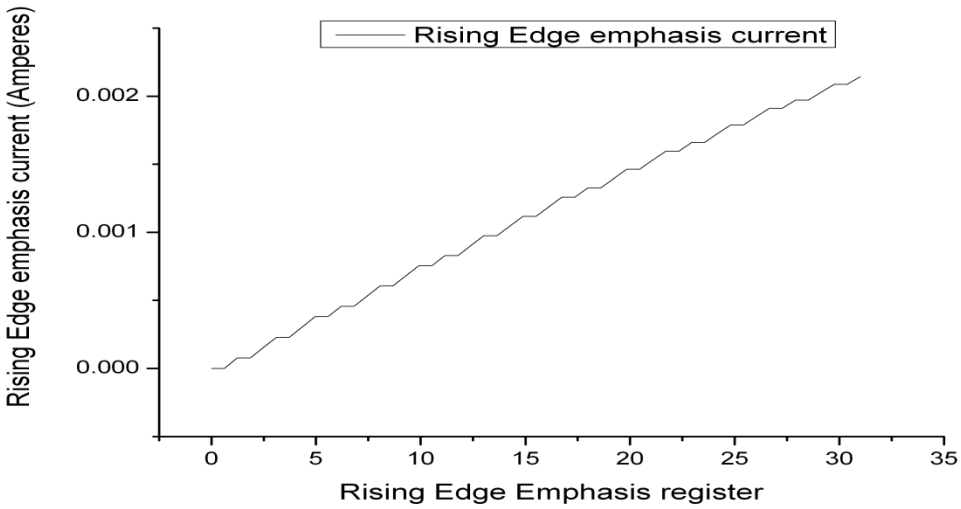


Fig.3.27 Rising edge emphasis current versus register value.

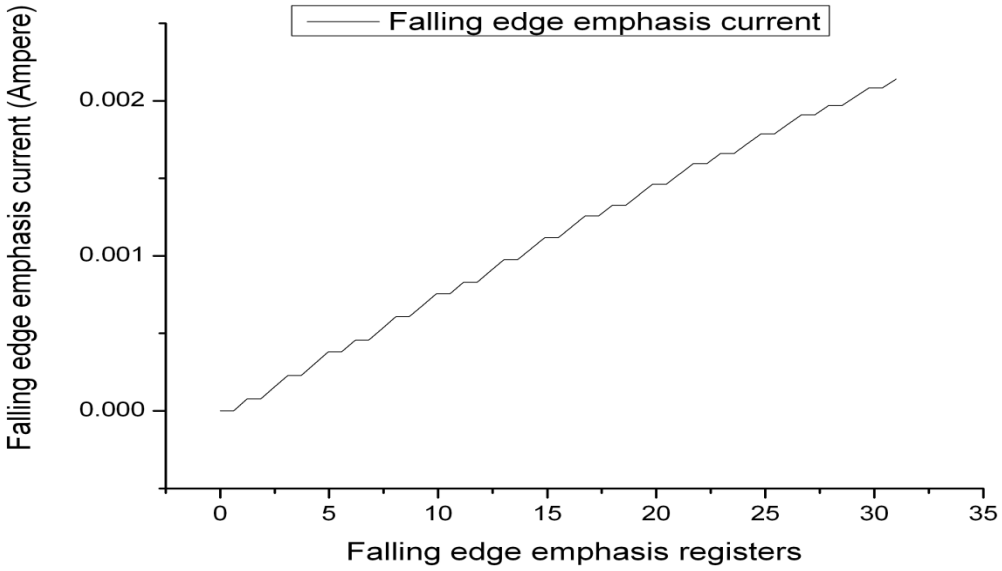


Fig.3.28 Falling edge emphasis current versus register value.

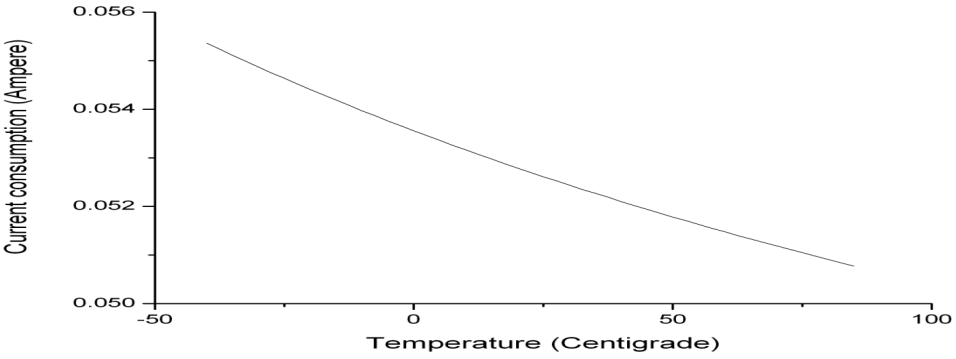


Fig.3.29 Maximum Current Consumption with Bias, Modulation, Falling and Rising edge emphasis currents set at maximum.

The eye diagrams shown in Fig.3.31 show how the eye opens up after the rising and falling edge emphasis are applied in the chip. These eyes are captured at 40Gbps for a modulation current of 5 mA and a bias current of 5 mA. These eyes show the current entering the cathode of the modelled VCSEL diode. The eye opening before emphasis is 0.4 mA as seen in Fig. 3.30 and eye opening after emphasis is 0.6mA (fig. 3.31) hence there is a percentage increase of 50% in the vertical eye opening. The horizontal eye opens from 13 p to 18 p after emphasis is applied which implies that there is around 40% horizontal eye opening.

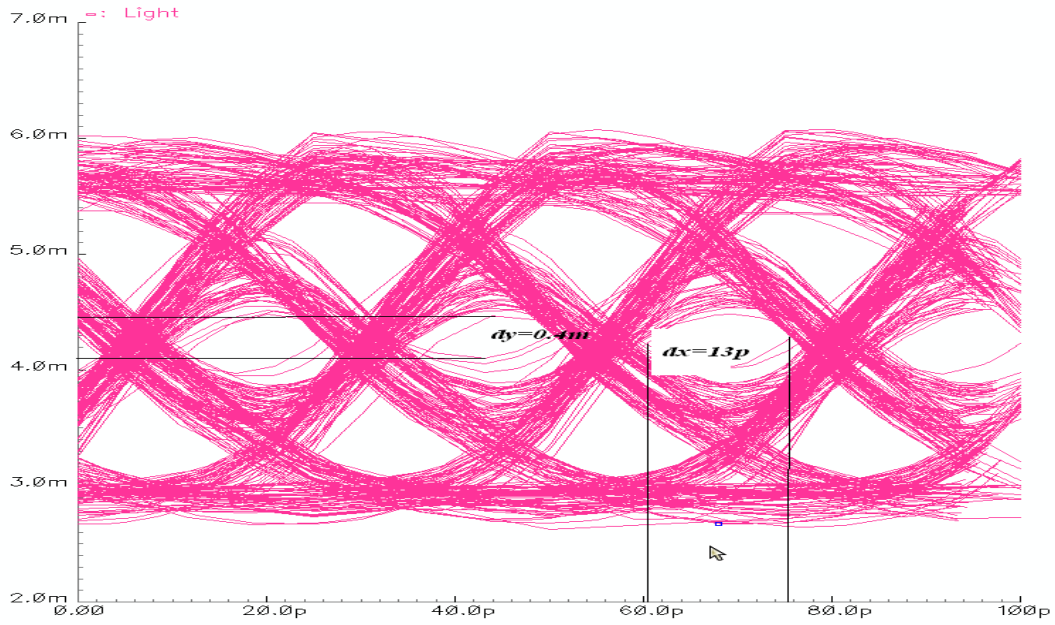


Fig.3.30 Eye diagram before emphasis

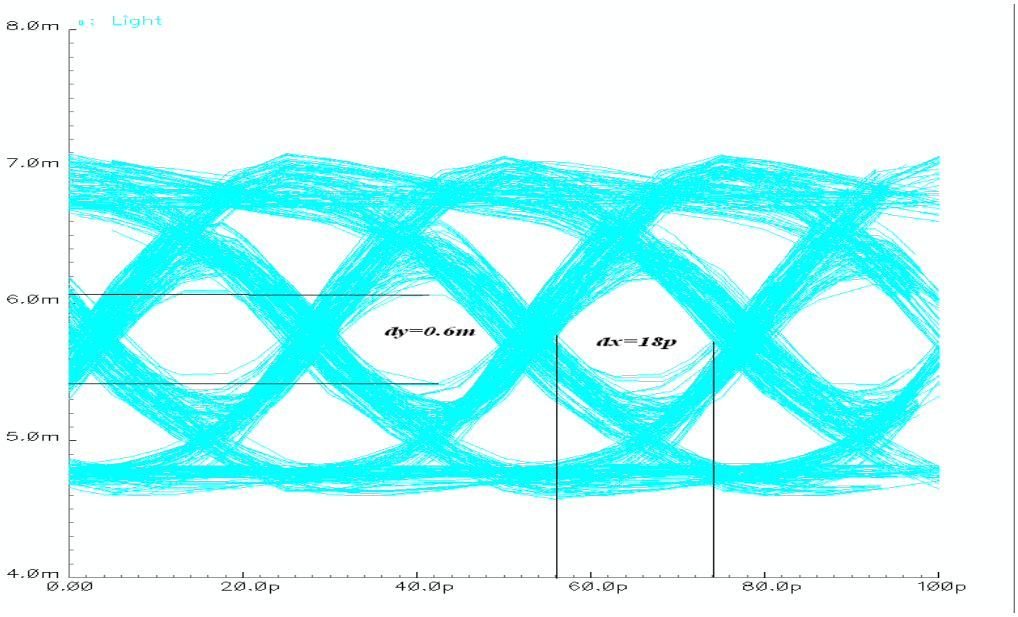


Fig.3.31 Eye diagram after emphasis has been applied

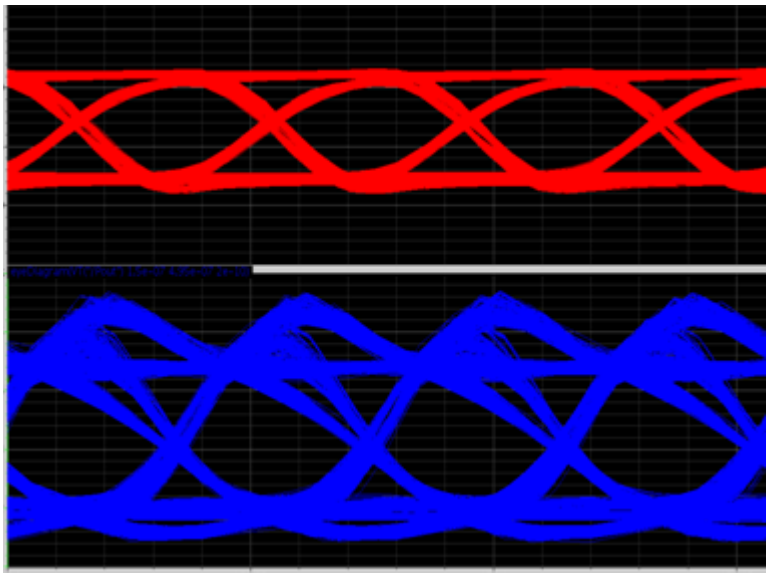


Fig.3.32 Simulated eye diagram electrical (red) and optical (blue)

3.4 PACKAGING AND TESTING

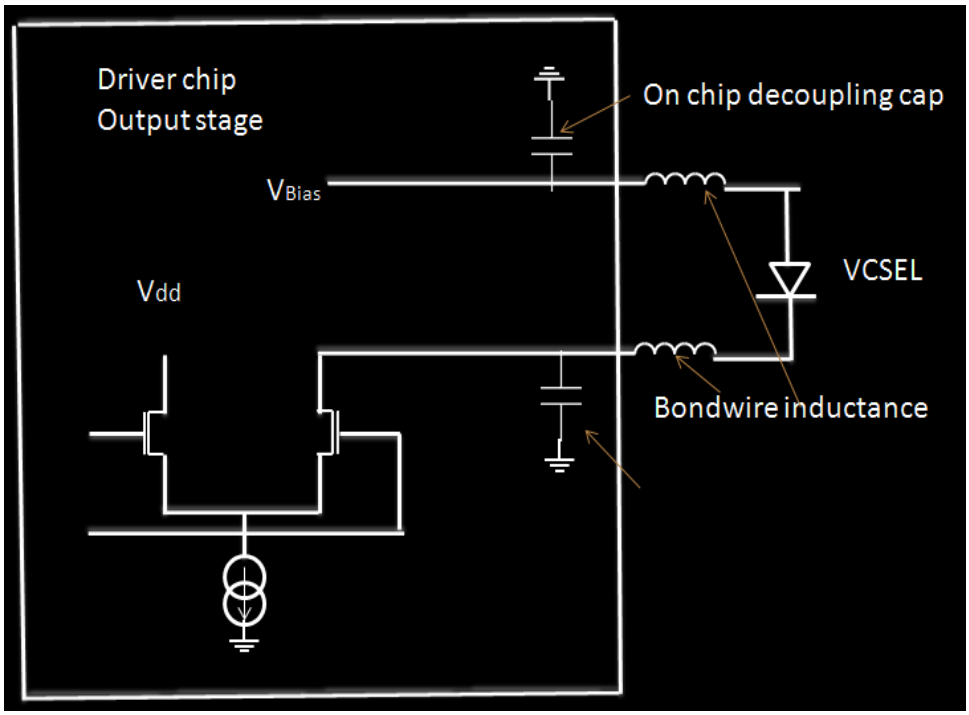


Fig.3.33 Connection of VCSEL and the driver

Figure 3.33 shows how the VCSEL will interface with the driver. Impedance matching resistors are omitted to reduce the power consumption. In designing the packaging, the main concern was to minimise the interconnect pararasitic that would lead to a degraded performance of the transmitter. The connection length between the driver output pads and VCSEL input bondpads was kept to a minimum to reduce the inductance to approx. 300pH.

To evaluate the VCSEL, a high performance GPPO connectorized butterfly package (see fig. 3.34) was selected as a packaging platform in order to avoid any degradation due to the parasitic and high-frequency losses.

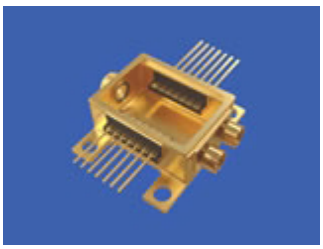
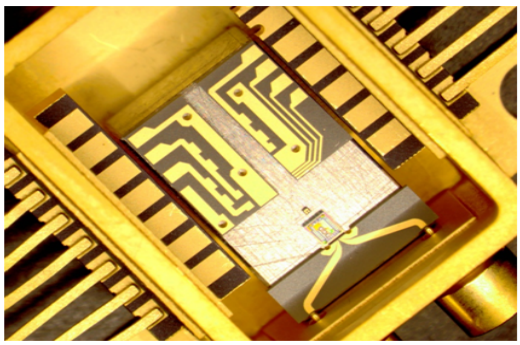


Fig.3.34 Butterfly Package

The next two figures show how the VCSEL and driver are mounted into the butterfly module



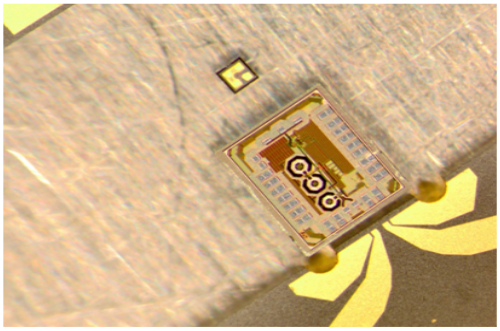


Fig.3.35 VCSEL Driver mounted on butterfly module

3.5 SUMMARY

A 40 G VCSEL driver is presented with falling and rising edge emphasis, which can improve the vertical eye opening by 50% and the horizontal eye opening by 40%. Pulse width distortion block is also added to the circuit to compensate for the distortion when converting from the electrical to the optical signals. Test result of this chip is ongoing.

Reference:	Technology	Emphasis	Power Consumption	Power supply	Eye Opening	Speed
[23]	90 nm	Pre-emphasis pulses	109 mW	1.2 V	76% Horizontal 122% Vertical	18 Gb/s
[24]	130 nm	Rising edge	70 mW	2.5 V	40% Vertical	20 Gb/s
[76]	90 nm	Rising and Falling edge	150 mW	1 V	Not Given	17 Gb/s
[This work]	65 nm CMOS	Rising and Falling edge	56 mW	1.2 V	50% horizontal 40% vertical	20 Gb/s

Table 3.1 Comparison with the state of the art VCSEL driver with emphasis.

4
56G PAM-4 VCSEL DRIVER

4.1 INTRODUCTION AND STATE-OF-THE-ART

As explained, short-reach optical interconnects face stringent requirements for power consumption, size and cost. Driven by requirements from e.g. datacentre operators, standard bodies are now looking at options to increase the throughput of short-reach optical interconnect beyond 100 Gb/s [25, 26]. To keep the number of space-multiplexed parallel lanes manageable, the bit-rate on a single (wavelength) channel must be increased beyond's today state-of-the-art 25 Gb/s. In the previous chapter, we presented work towards 40 Gb/s using non-return to zero modulation for VCSEL-based transceivers. However running VCSELs at such high speeds has serious drawbacks. First of all, 40 Gb/s VCSELs suffer from reliability problems due to the very high current densities which occur in their (necessarily small) active regions. Packaging parasitics also introduce bandwidth limitations which can be overcome but at significant (module) cost. Therefore, alternative methods to increase the bit-rate beyond non-return to zero modulation (NRZ, e.g. including pre-emphasis) need to be explored. One such way is to use four-level pulse amplitude modulation (PAM-4) signalling. As an approximate rule-of-thumb, this modulation format allows to transmit twice the bit-rate in the same bandwidth as the non-return to zero modulation, albeit at the expense of a three-fold reduction in difference between two adjacent power levels. PAM-4 signalling is an attractive solution for short-distance optical links which are constrained by data rate and power consumption, but typically have large enough received optical power that they are not noise limited [73] [74].

Electrical links based on PAM-4 signalling have been proposed in [28, 29, 75-78], as an alternative to NRZ links in high-speed serial applications. The severe frequency dependent losses of electrical links in backplane and cable applications (which is around 30 dB at 1e-15 of BER operating at 25 Gbps for 3-5m links) due to

skin effect and frequency dependent dielectric losses necessitate the use of equalization even though PAM-4 signalling is used. An optical based PAM-4 link which has VCSEL a driver is presented in [29]

In [28] the author designed a 32 Gb/s PAM4 transmitter in 130 nm CMOS technology for high-loss wireline channels. The authors implemented PAM-4 level signalling to cancel the effect of losses and used a pulse-width modulated pre emphasis block to increase the eye opening. However power consumption by the blocks which generate the emphasis pulses is 1.43 W which makes it unsuitable for the design of optical interconnects. Moreover the output driver is a cascoded structure and uses 3 stacked transistors which can't be used in nanoscale CMOS technologies due to their low power supplies. And their basic cell design consists of a differential pair which steers an always on tail current to either the positive or negative output rail thus making it not very power efficient since the tail currents corresponding to the different PAM symbols are always on irrespective of the currently transmitted PAM-symbol as shown in Fig. 4.1.

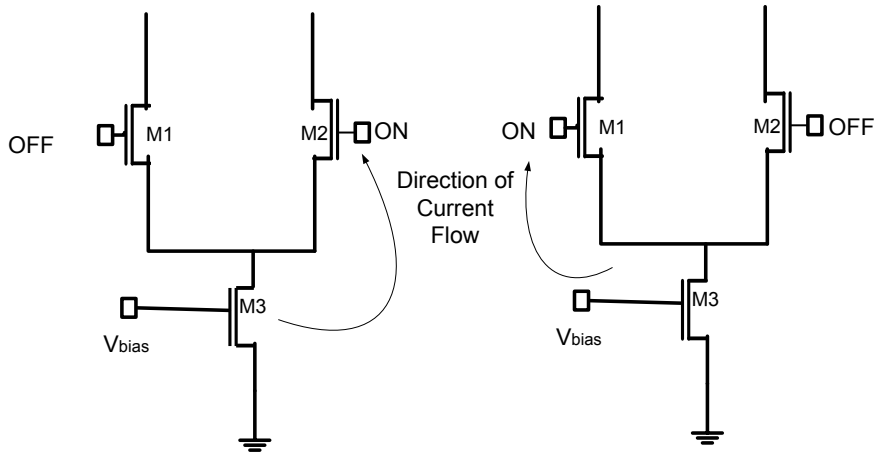


Fig.4.1 Tail current always flowing whether modulation signal is present or not

In [75] 10 Gbps PAM-4 transmitter in 180nm CMOS technology primarily intended for electrical backplane interconnect is reported. It uses a bipolar topology to reduce the power, where a unit voltage having ±RI can be switched on when it is transmitted and ±2IR is switched off and vice versa as shown in Fig. 4.2. It has a data-look-ahead scheme to settle the switching current at the tail as fast as possible to make it work at higher speed. To further reduce the power, the right unit can be

turned off whenever ±RI are to be transmitted. The top current source can be turned off by pulling up both B2p1 and B2p2 inputs, while for turning off the bottom current source, B2n1 and B2n2 signals should be pulled down.However if one wants to use the data-look-ahead technique at higher speeds above 10 Gb/s, CML gates will be required to implement the delays, as a conventional CMOS based inverter used in this design will not be able to work at higher speeds. This will significantly increase power consumption.

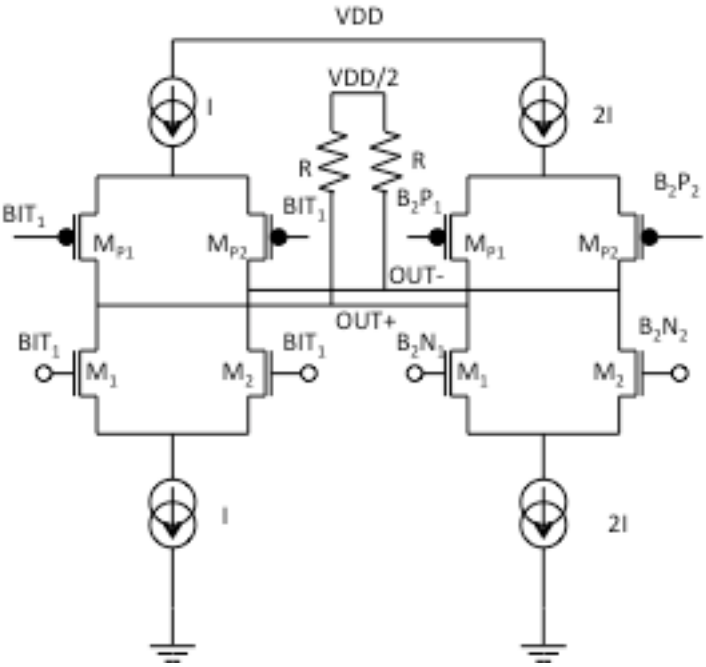


Fig.4.2 Bipolar topology presented to switch the current from ±RI to ±2RI

In [76] 20 Gbps PAM-4 transmitter for high-speed data serial link is presented. It has implemented pre-emphasis technique to mitigate the losses by using 3 taps of different currents. However the main driver uses a differential pair topology with always on tail currents which again has a drawback in terms of power consumption as explained earlier.

[29] also presents a PAM4 transmitter for serial interconnects operating at 25 Gbps designed using 90 nm CMOS technology. As with others it also has equalization implemented with taps of different source magnitudes. The

multiplexers and clock circuitry used in the design of these taps use CML gates which is not suitable for power saving purposes.

[77] presents 10 Gbps PAM4 serial link transmitter fabricated in 400 nm CMOS process. It also uses a pre-emphasis technique, based on a three-tap finite impulse response, to achieve the desired data rate. Most of the circuits that are used in the design are using differential architectures making it dissipate higher currents. It also has dummy driver topology with lesser sizes than the main driver to solve the Duty-Cycle error which also consumes power continuously thus making it unsuitable for the application of optical interconnects.

[78] compares the performances of transmitters used in three data formats of duo-binary, PAM4 and NRZ at 20Gbps using 90-nm CMOS technology. In its PAM4 transmitter the use of stacked transistor in its cascode based topology of its output driver is not suitable for technologies with low supply voltages. Moreover its differential based structure also uses continuously on tail currents irrespective of the transmitted PAM4 level.

PAM4 signalling in optical transmission is reported in [27] operating at 10 Gbps used for Ethernet standards using multi mode fibre. It has different drivers with its own precursor drivers as well to provide the equalization for different levels of PAM signal and the current is added at the output before transmitting to the VCSEL. It output driver is CML type with open-drain output which allows the tail current to remain on all the time, again requiring high power. The pre-cursor drivers used for equalization also have similar structure and hence similar disadvantage as well.

4.2 PAM SIGNALLING

PAM is a form of digital signal modulation where the information (a stream of bits) is encoded in the amplitude of a series of signal pulses. By transmitting multiple bits using a single symbol, the required bandwidth of the channel for a given bit rate decreases and the system spectral efficiency increases. A relatively simple multi-level modulation scheme is M-level pulse amplitude modulation, where each pulse conveys $\log_2(M)$ bits of information. For a given data rate the effective symbol rate is reduced by $\log_2(M)$ by using PAM.

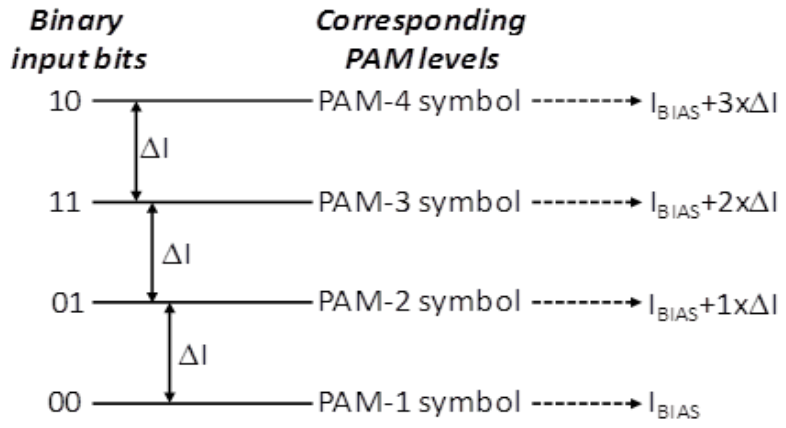


Fig.4.3 PAM-4 modulation and Gray encoding of binary input bits.

Fig. 4.3 gives a schematic representation of PAM-4 modulation. Bits are assigned to the PAM symbols using so-called Gray coding, whereby adjacent PAM symbols do not differ in more than a single bit, thus minimizing the bit-error rate at the receiver [79].

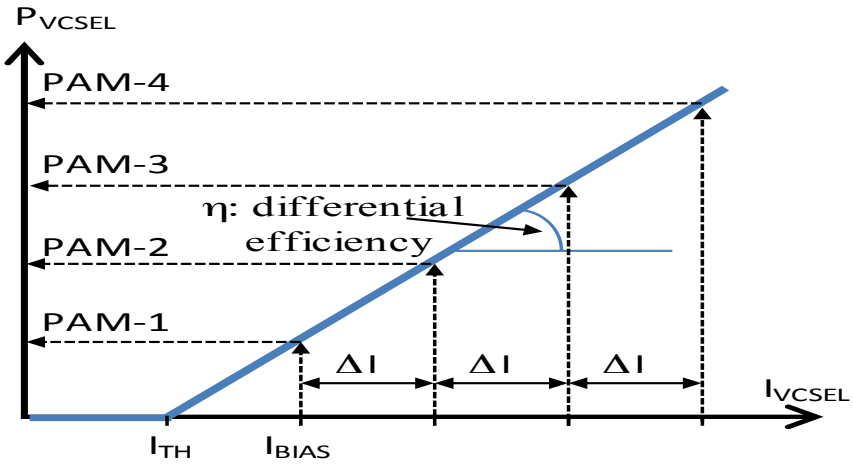


Fig.4.4 VCSEL Power vs. Current Relationship

Fig. 4.4 shows the optical output power of a VCSEL versus its bias current: note how a VCSEL only emits optical power when biased above its so-called threshold current. Hence, when modulating a VCSEL with a PAM-4 signal, the PAM-1 symbol (lowest order symbol) is generated by biasing the VCSEL with a current I_{BIAS}. This bias current needs to be sufficiently large compared to the VCSEL threshold current (thus minimizing jitter due to turn-on delay as well as decreasing the overshoot on the rising typical for laser diodes), but small enough to ensure sufficient modulation contrast. The other PAM symbols are generated by driving the VCSEL with an additional current ΔI per PAM level.

4.3 PAM−4 VCSEL DRIVER

Fig. 4.5 shows a block diagram of the PAM-4 VCSEL driver. The driver accepts two 28Gb/s bit streams A and B. To generate the corresponding PAM-4 symbols, these two bit streams are converted into three Gray and thermometer encoded bit streams X, Y and Z according to the truth table as shown in Table 4.1. Each of these bit streams X, Y and Z controls a slice of the driver circuit which can steer a current ΔI to the VCSEL if its logical input is high, and a zero current if its logical input is low.

In this way, the driver draws only modulation current for the PAM symbol being actually transmitted. The generation of the bias current is spread across all three driver slices, thus ensuring that each driver slice is loaded with the same output impedance. Both the bias current and modulation current ΔI are programmable through on-chip digital registers via the bias and modulation level controllers. An on-chip filtering capacitor is foreseen to provide the anode bias voltage to the VCSEL. The high-speed IO cells were specifically designed for very low capacitance (less than 100fF).

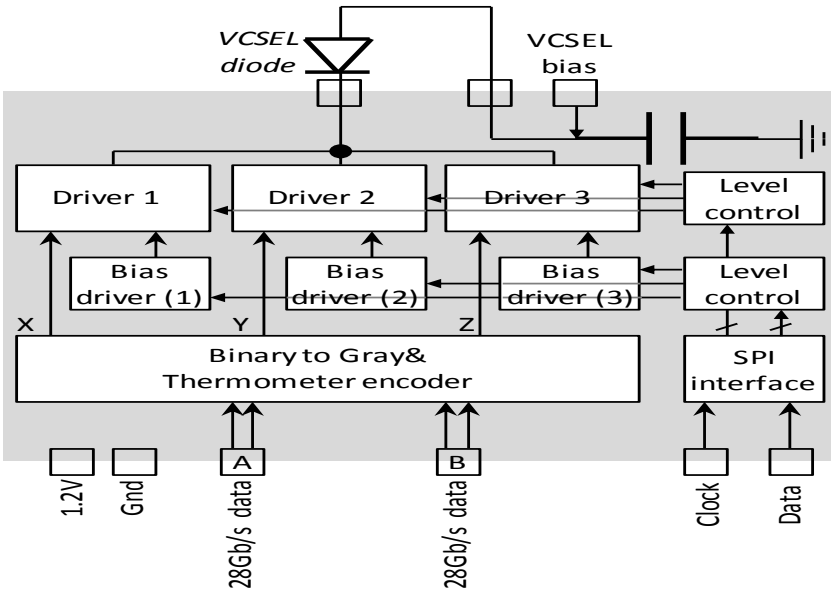


Fig.4.5 PAM-4 VCSEL driver diagram (SPI = serial peripheral interface).

4.3.1 Binary to Thermometer/Gray Encoding

In order to generate 4-level signals, the binary data (A,B) has to be converted to thermometer Code (X,Y,Z) as shown in Table 4.1.

A	B	PAM symbol	X	Y	Z
0	0	1	0	0	0
0	1	2	1	0	0
1	1	3	1	1	0
1	0	4	1	1	1

Table 4.1 Binary to Gray/thermometer encoding.

From Table 4.1, we can see that bits X, Y and Z can be implemented as: X=A OR B, Y=A, Z=A AND (NOT B) as shown in Fig. 4.6.

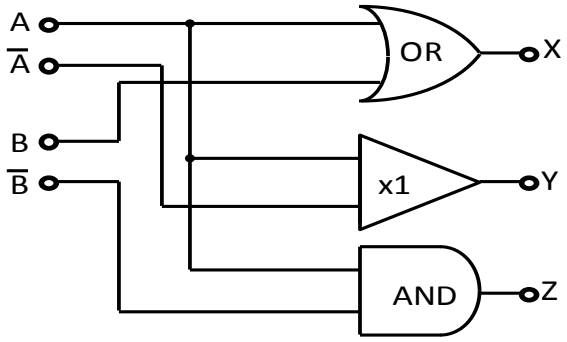


Fig.4.6 Binary to Thermometer Encoder

To generate bit X, Y and Z at speeds of 28 Gbps conventianol CMOS rail to rail logic gates are not a suitable choice as these do not have sufficient switching speed (especially when taking into consideration the worst-case process, supply and temperature corner) and are noisy in nature due to their current peaks and high voltage variations during the switching of logic gates. The latter is especially a problem in mixed signal chips containing sensitive receiver circuits as the noise

transmission from the noisy digital part to the analog part can affect the performance of the sensitive analog blocks. To solve this problem we have used so-called MCML (MOS Current Mode Logic) logic gates [72, 80, 81]. As shown on Fig. 4.7, MCML gates are composed of a pull up (passive) network, differential NMOS pairs and a tail transistor that serves as a current source. They are based on current steering wherein the bias current is steered to one of the output branches depending upon the inputs to the NMOS transistors. The branch with no current flowing through it generates a logic high output as the voltage drop across the load resistor is (ideally) zero. The voltage swing is decided by the resistance offered by the load device and the bias current provided through the tail transistor.

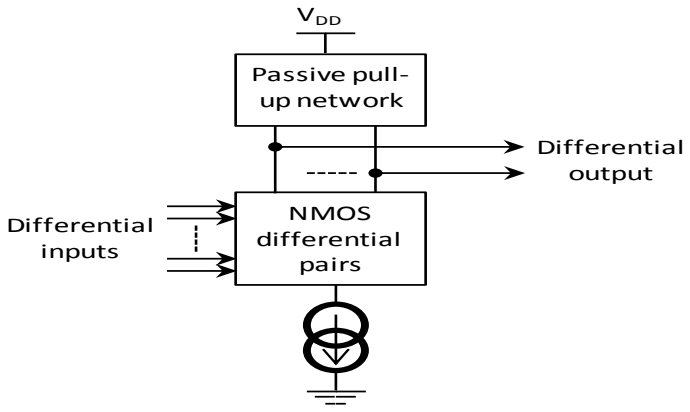


Fig.4.7 MCML gates.

Being fully differential and using a constant current source the voltage swing is reduced both which improve switching speed. Additionally, the differential nature in combination with the use of a constant current source largely eliminates voltage peaks during switching. Finally, MCML gates are more robust than conventional CMOS logic gates against process variation.

4.3.1.1 MCML OR GATE

Fig.4.8 provides a Circuit level diagram of MCML OR/NOR gate. Table 4.2 represents the truth table for an OR gate: when both the inputs A and B are low the OR output is pulled towards ground. In the other three cases, the output is pulled to VDD. Inductive peaking is used to increase the bandwidth of the block. To minimize the

area used by the inductors, centre tapped inductors are used [64]. Bit X of the encoder is implemented using this OR gate.

A	B	out
0	0	0
0	1	1
1	0	1
1	1	1

Table 4.2 Truth Table for OR gate

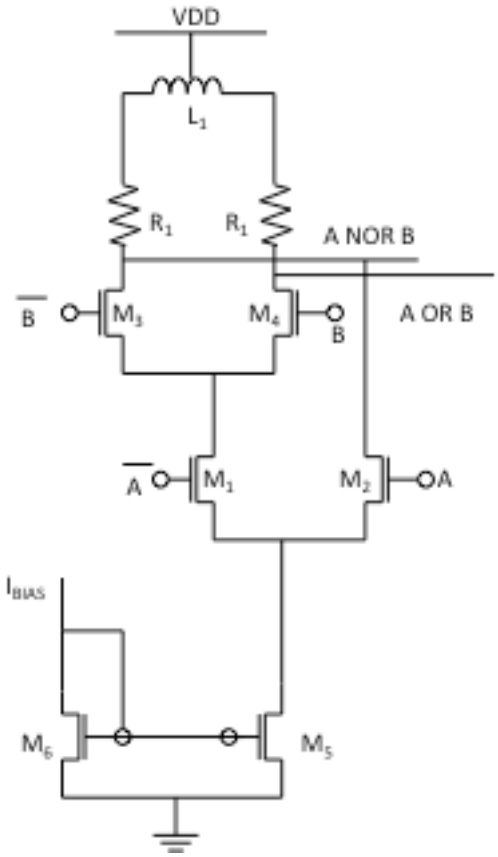


Fig.4.8 MCML OR/NOR gate

4.3.1.2 MCML INVERTER

An MCML inverter is simply a differential amplifier with appropriate connection of its output phases to the next block in the logic block. Fig. 4.9 shows the circuit diagram: again inductive peaking using a centre tapped inductor is used to increase the bandwidth. This block is used to generate bit Y of the encoder

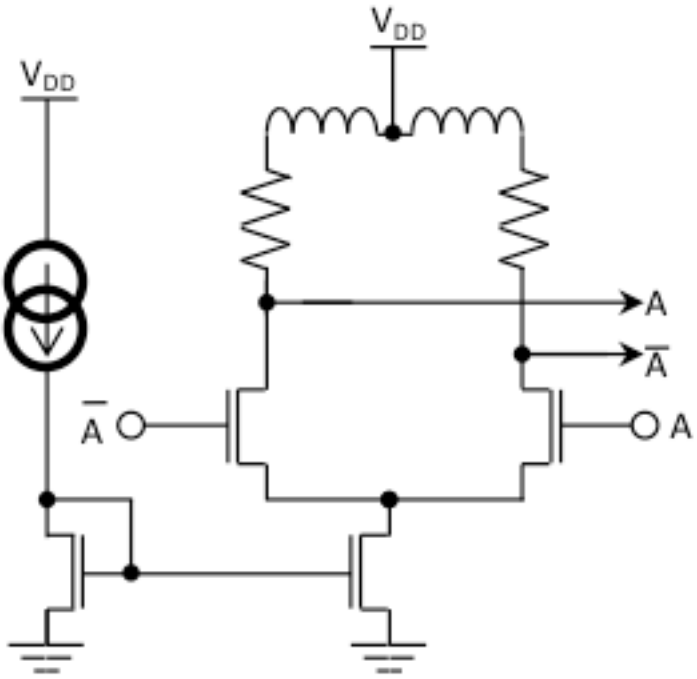


Fig.4.9 MCML inverter/buffer gate

4.3.1.3 MCML AND GATE

Bit Z of encoder is the AND product of A and B and is achieved by the circuit shown in Fig.4.10: when both A and B are high the output is pulled to VDD otherwise the output is pulled down with the voltage drop across the drain resistor

as shown in Table 4.3. Again note the use of a centre tapped inductor to increase the bandwidth of the design.

A	B	out
0	0	0
0	1	0
1	0	0
1	1	1

Table 4.3 Truth Table for AND gate

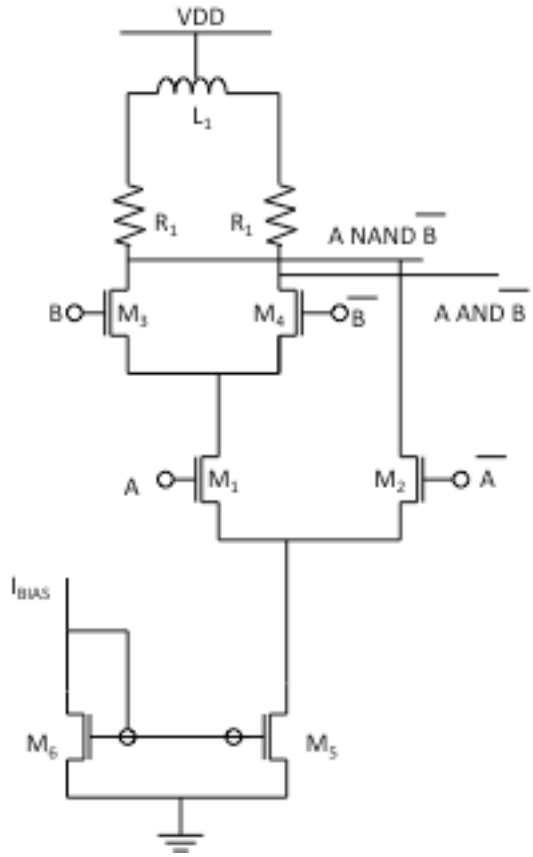


Fig.4.10 MCML AND gate

Since these MCML gates have different delays with respect to one another, it creates a glitch issue and causes the eye to distort significantly as shown in Fig.4.11

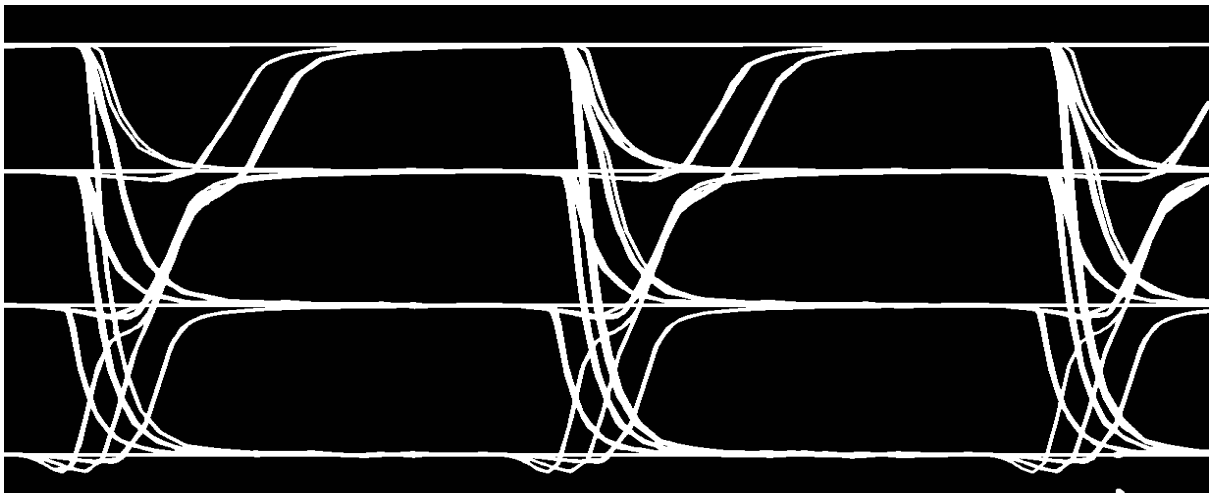


Fig.4.11 PAM4 VCSEL eye distorted due to different delays of MCML gates operating at 56 gbps.

To compensate for this issue we introduced CMOS inverters of different delays to ensure that all the three encoded bits arrive at the VCSEL driver in synchronization as shown in Fig. 4.12.

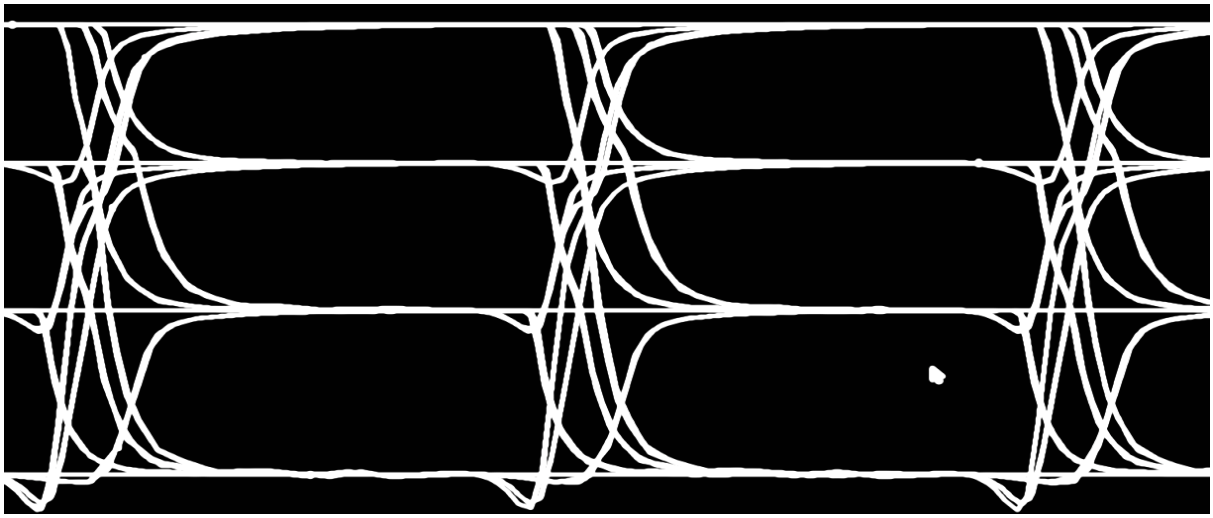


Fig.4.12 Synchronized data after inverters are placed.

For such designs it is very important to check the delays across process and temperatures corners as both the CMOS and MCML delays may vary significantly across corners. Fig. 4.12 shows eye diagrams for extreme corners: mainly SS (slow NMOS and slow PMOS), FF (Fast NMOS and Fast PMOS) SF (Slow NMOS and Fast PMOS) and FS (Fast NMOS and Slow PMOS). It also captures eye diagrams at the minimum and maximum temperature (0 and 85 degrees).

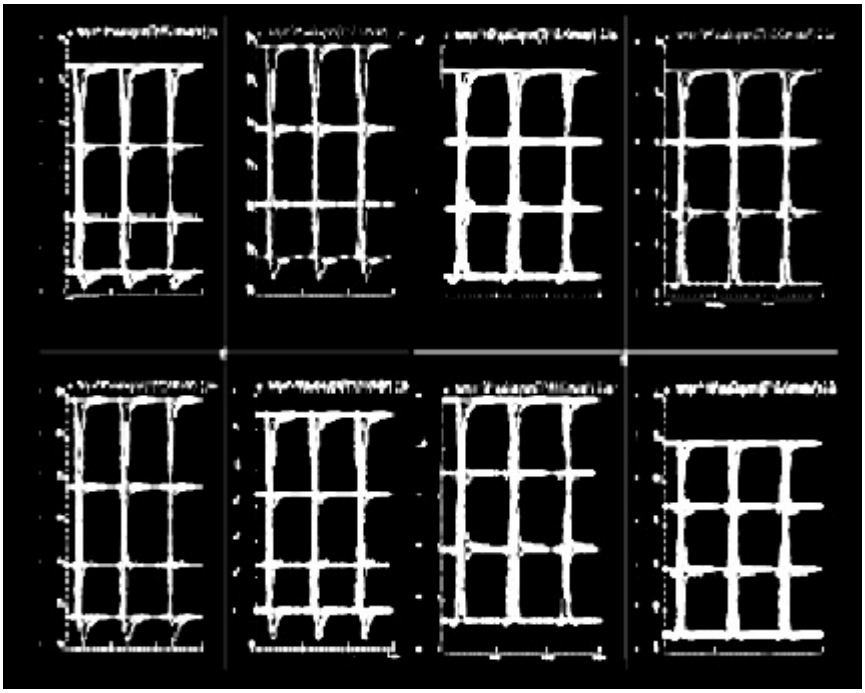


Fig.4.13 PAM-4 eye diagram at various temperature and corner variations.

Fig. 4.14 shows the eye diagram after Monte Carlo simulations, including both random process and mismatch variations. . In addition to including the impact of mismatch, Monte Carlo simulations give a better grasp of the spread of circuit parameters. 100 Monte Carlo simulations were run here: low spread of the delay can be seen:

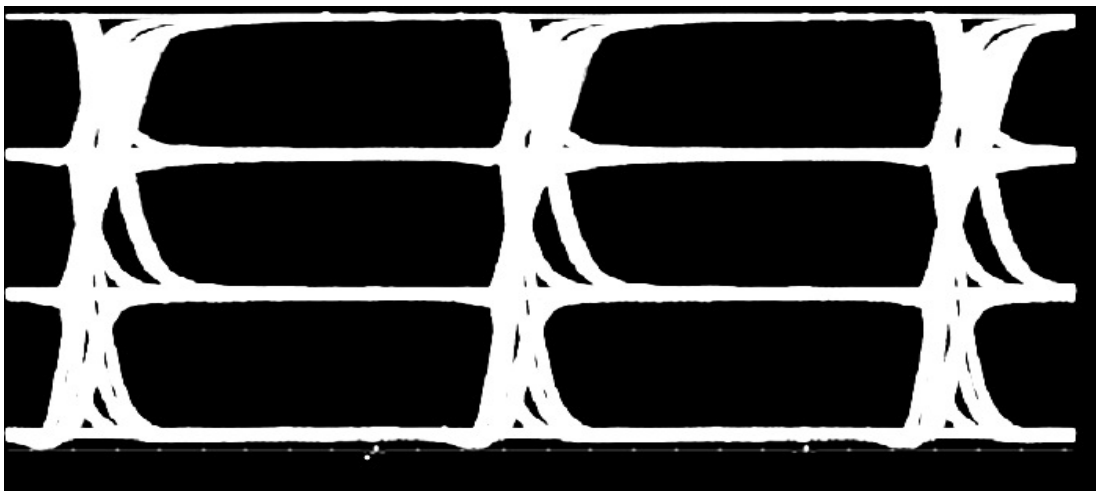


Fig.4.14 100 Monte-Carlo simulations to ensure that delays of all the MCML gates are the same at 56gbps.

4.3.2 THE VCSEL DRIVER CIRCUIT

As explained before, power consumption is an important consideration for the VCSEL driver. The most straightforward way to minimize the power consumption is reducing the supply voltage as much as possible. Coincidently, the deep-submicron 65 nm CMOS technology used in this work necessarily operates from a low 1.2 V supply voltage due to low (gate and drain) breakdown voltages of its core MOS transistors. These considerations however conflict with the voltage/current relationship of a typical VCSEL shown in Fig. 4.15. The VCSEL diode's threshold voltage is 1.55 V, and as shown the voltage drop across the VCSEL increases up to 2.6-2.8 V for the highest PAM level due to its relatively high differential resistance (high compared to e.g. conventional laser diodes).

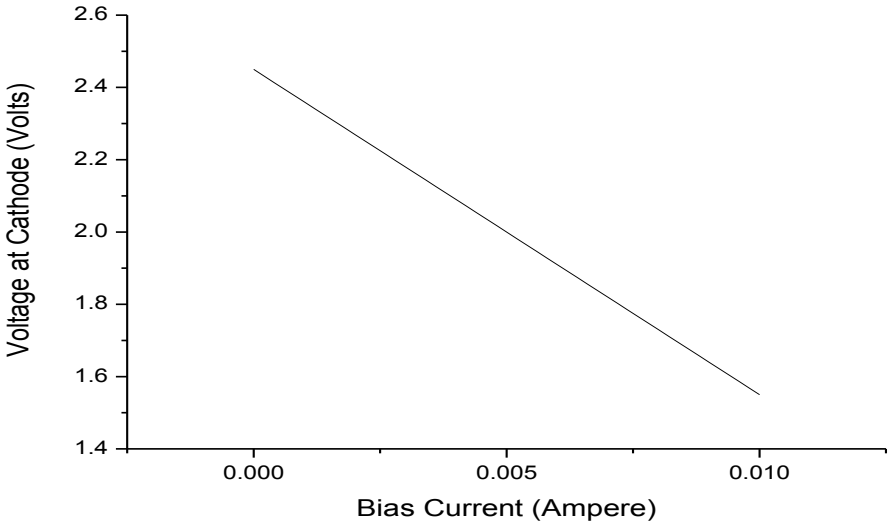


Fig.4.15 V-I curve of the VCSEL used in the design

To modulate the VCSEL, therefore a common-anode configuration was selected together with a separate (sufficiently high) bias voltage connected the VCSEL cathode.

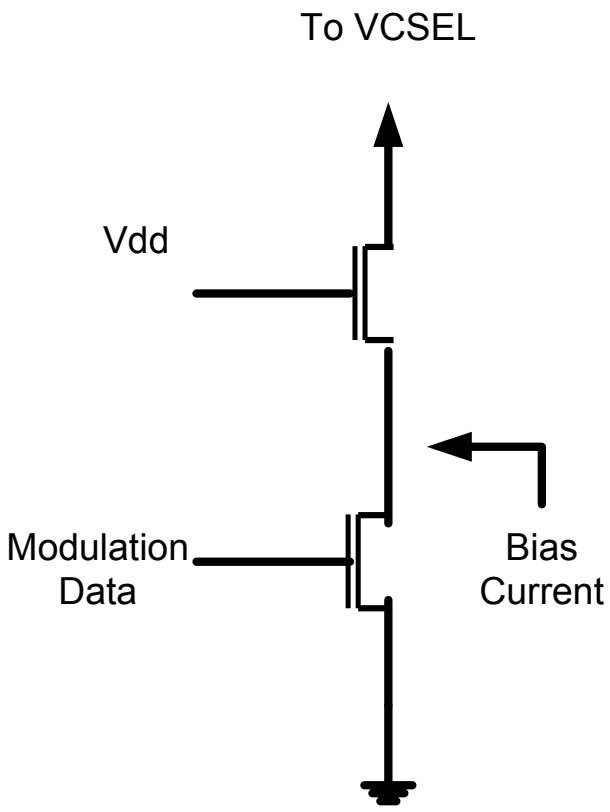


Fig.4.16 Conceptual view of VCSEL driver

Fig. 4.16 gives a conceptual view of the VCSEL driver: a cascoded structure was selected which serves the double purpose of improving the switching speed (see below) and also of spreading the drain-to-source voltage stress across the two stacked transistors as indicated. The maximum voltage that can be allowed at the output of the VCSEL driver is 2.5 V before breakdown can occur. When driving the VCSEL with the V,I curves as in Fig. 4.15 using a bias voltage of 4.5 V, the maximum expected voltage at the driver output is 2.5 V.

Most high-speed laser diode and VCSEL drivers use a differential structure as shown in Fig. 4.17 with the tail transistor setting the modulation current. In this way, a well known modulation current can be switched with fast rise and fall times. The bias current is added at the drain of the differential pair transistor (which could be at the source of an additional cascode transistor or directly at the VCSEL terminal). However note that the modulation current is always ‘on’ irrespective of the transmitted bit or symbol.

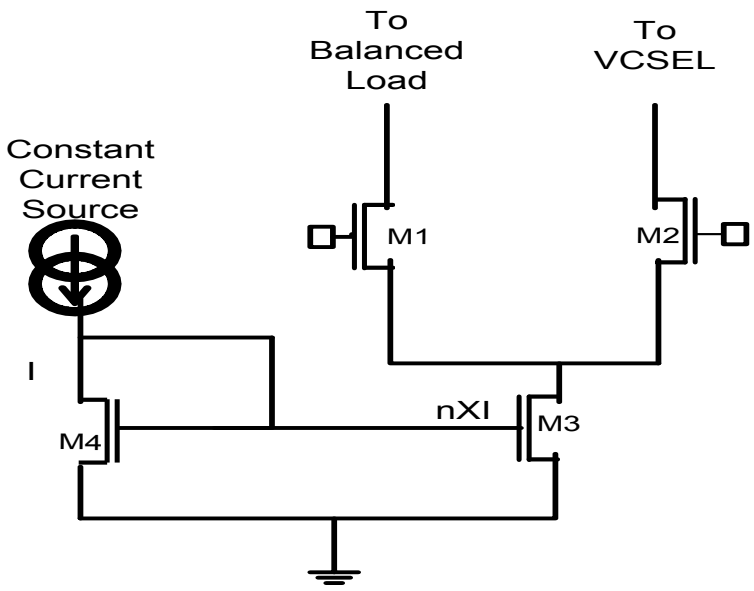


Fig.4.17 Differential structure for VCSEL driver

Another issue with this design is that when M2 is switched the drain voltage of M3 varies as well: this result in variation of the drain current of M3 and current spikes during the transitions. Better dc-accuracy can be obtained by increasing both the length and width of M3 (thus increasing its output impedance), however this results in larger current spikes due to the larger capacitive load at the source of M2.

In order to solve the above two problems and to reduce power consumption we have designed a common source based VCSEL driver as shown in Fig 4.16. This structure only draws the current corresponding to the symbol being transmitted.

Common-source based laser or VCSEL drivers have been reported before. In [82], a simple common-source based driver was presented (see Fig. 4.18): here the output transistor M_1 functions as a switch and is either off (transmitting a digital 0) or is switched on in its triode region (transmitting a digital 1). An additional current source transistor M_B supplies the bias current. This simple approach however does not allow to efficiently control the amount of current that is switched into the VCSEL. While one can for example adjust the supply voltage V_{DD} of the inverter string (thus changing the on resistance of the output transistor M_1 by adjusting its gate voltage) this gives rise to excessive rise and fall times in the inverter string for the low supply voltages, before any appreciable reduction in output current occurs.

Indeed it is well known that the rise and fall times of an inverter are inversely proportional to its supply voltage [[83], pp. 959-961].

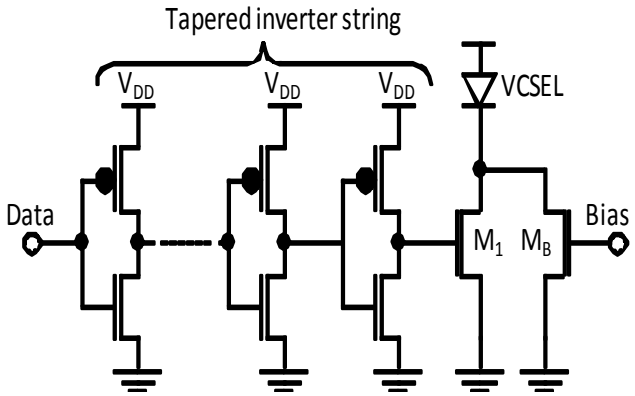


Fig.4.18 Simple common-source based driver from [82].

An alternative common-source topology was presented in [84, 85], see Fig. 4.19: the output transistor is now divided into a (binary weighted) transistor array. By using the AND gates and the selection signals $p_{0,1\ldots,5}$, one can selectively switch on or off output driver transistors, thus adjusting the amount of current switched to the VCSEL. This approach however does not scale very well to high bitrates: indeed even when some transistors are in their off state, these still contribute to the load capacitance at the output of the driver (for example, the drain to bulk junction capacitance), thus limiting the achievable bitrate.

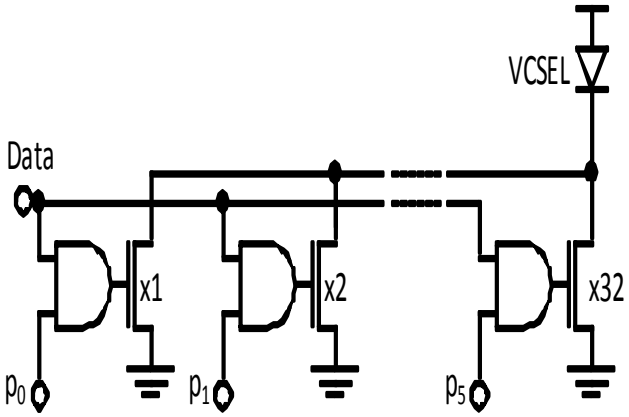


Fig.4.19 Binary weighted output transistor [84, 85].

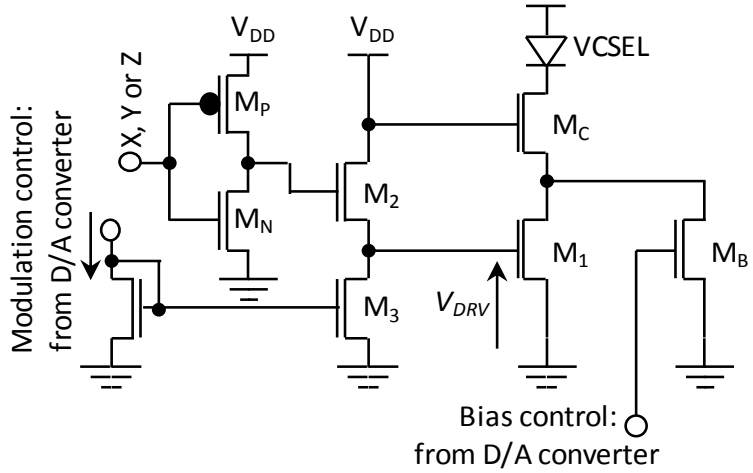


Fig.4.20 Proposed Driver Slice.

To solve these problems, the alternative topology shown in Fig. 4.20 is proposed. Similarly to [82], a single output transistor M_1 is used (per driver slice), however a source follower M_2 is inserted between the output switch transistor M_1 and the

inverter stage formed by transistors M_N and M_P. A full CMOS voltage swing (0 or V_{DD}) is supplied to the source follower M_2 using the inverter M_N, M_P. By adjusting the bias current of the source follower M_2 (which can be easily done by setting the gate voltage of current source transistor M_3, here done using a D/A converter), its voltage drop V_{GS} can be controlled, which in turn controls the gate voltage V_{DRV} of the output transistor M_1, thus changing the output driver current. The improved high-speed behaviour compared to the inverter string from [82] can be understood by considering the dominant pole frequency f_P of the source follower:

$$2\pi f_P = \frac{1}{R_S C_{GD2} + \frac{C_{GS1} + C_{GS2} + C_{DS3}}{g_{M2}}} \qquad (4.1)$$

where R_S is the resistance in the gate of source follower M_2, C_{GD2} its gate-to-drain capacitance, g_{M2} its transconductance, C_{GS2} its gate-to-source capacitance, C_{GS1} the gate-to-source capacitance of the output transistor M_1 and C_{DS3} the drain-to-source capacitance of M_3. Note how the denominator in (4.1) consists of a first part $R_S C_{GD2}$ which does not depend upon the bias current of M_2, and a second part which is inversely proportional to the bias current of M_2 (through the transcondutance g_{M2}). This indicates that by carefully designing the driving resistance R_S (determined by the width of the inverter transistors M_P and M_N), the dependence of the bandwidth of the source follower M_2 on its bias current can be reduced. This in turn limits the variation in rise and fall time when adjusting the bias current of M_2. The minimum allowable bias current is determined by the fact that when the gate of the source follower is pulled down by the inverter, the gate capacitance M_1 is discharged by current source transistor M_3 with a slew rate SR_{OFF} equal to:

$$SR_{OFF} = \frac{I_{DM3}}{C_{GS1} + C_{DS3}} \qquad (4.2)$$

with I_{DM3} the drain current from M_3. The maximum allowable bias current for M_2 is defined by the maximum tolerable on-resistance of M_1, which together with the load capacitance sets the bandwidth of the driver. Indeed note that when the bias current I_{DM3} of M_3 is increased, the gate-to-source voltage drop of source follower M_2 increases, which in turn reduces the gate voltage V_{DRV} of M_1 in its on state. An

additional cascode transistor M_C is used to isolate the output transistor from the capacitance of the VCSEL and the IO pad, improving switching speed. Finally, the bias current is added at the source of the cascode transistor, with each slice (see Fig. 4.5) delivering 1/3rd of the total bias current. In this way, no additional cascode transistor (which is essential to maintain sufficient output impedance) is needed for supplying the bias current, thus reducing the total load capacitance at the output of the driver.

4.3.2.1 Modulation Current Control

In a differential VCSEL driver the modulation currents are controlled by changing the tail current source, which can be done for example using a simple current mirror, as shown in Fig. 4.21. To reduce power consumption, a current mirror multiplication factor N is frequently used.

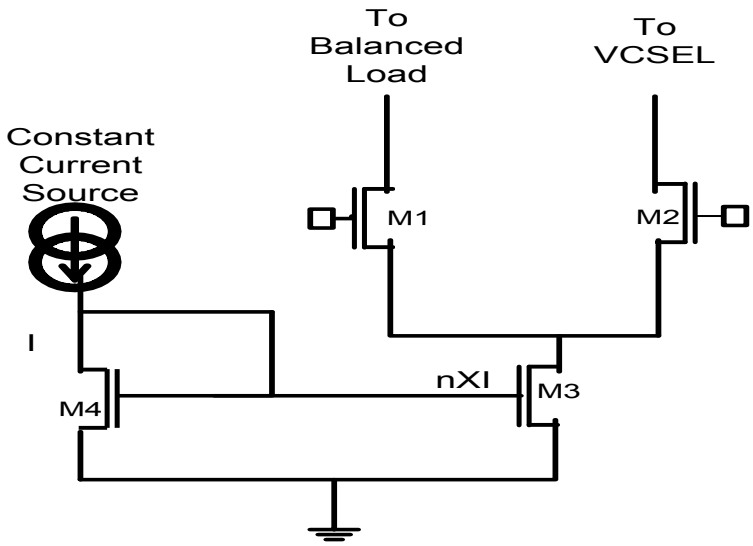


Fig.4.21 Modulation current control in Differential VCSEL driver.

Note how the switching functionality (provided by transistors M_1 and M_2) is completely separated from the modulation current control (provided by transistors M_3 and M_4). In our common-source scheme both functions must be provided by the

same transistor (M1 in Fig. 4.20), requiring a specialized control and switch pre-driver circuit. Three pre-driver stages were tested and finally the source follower stage was selected, see below.

4.3.2.1.1 Inverter Stage Modulation Current Control

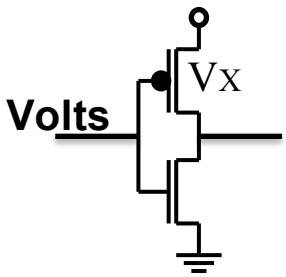


Fig.4.22 Inverter

Fig.4.22 shows an inverter stage: the high-speed data signal VIN is supplied from the thermometer encoder logic gates. The actual gate swing supplied to common-source transistor M1 in Fig.4.20 can be adjusted by varying 'supply voltage' V_X. The inverter's operation can be understood as a switch. When V_{IN} is sufficiently high NMOS M_1 is 'ON' and PMOS M_2 is 'OFF': V_{OUT} is shorted to the ground node and hence is 0V. When V_{IN} is low then PMOS transistor (M_2) is 'ON' and NMOS transistor (M_1) 'OFF' shorting V_X and V_{OUT}: V_{OUT} now equals V_X.

So to control the modulation current of the VCSEL V_X in Fig. 4.22 needs to varied which will provide different levels of swing. While this is conceptually very simple, this topology has several drawbacks which are listed below.

1. The threshold voltage V_{TH} is defined as the input voltage for which $V_{IN}=V_{OUT}$ and ideally for the signal to be perfect the desired value for the threshold voltage is $V_{DD}/2$.

So when $V_{IN}=V_{OUT}$ M_1 has $V_{DG}=0$ which means that it is in saturation region

So for Saturation region,

$$I_{D-2} = \frac{\mu_p C_{ox}}{2} \left(\frac{W}{L}\right)_2 \left(V_X - V_{th} + V_{tp}\right)^2 \qquad (4.3)$$

And for NMOS transistor

$$I_{D-1} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right)_1 (V_{th} + V_{tn})^2 \qquad (4.4)$$

Solving for V_{th} (threshold voltage) gives the following relationship

$$V_{th} = \frac{V_{tn} + (V_X + V_{tp}) \sqrt{\frac{\mu_p \left(\frac{W}{L}\right)_2}{\mu_n \left(\frac{W}{L}\right)_1}}}{1 + \sqrt{\frac{\mu_p \left(\frac{W}{L}\right)_2}{\mu_n \left(\frac{W}{L}\right)_1}}} \qquad (4.5)$$

2. So it can be seen that the threshold voltage is sensitive to the variations in the device parameters such as V_{tp} and V_{tn} and also V_X. Thus it becomes very difficult to control threshold voltage if the power supply of inverter is changing.

The small signal circuit for the inverter is shown in Fig.4.23 and is further simplified in Fig.4.24

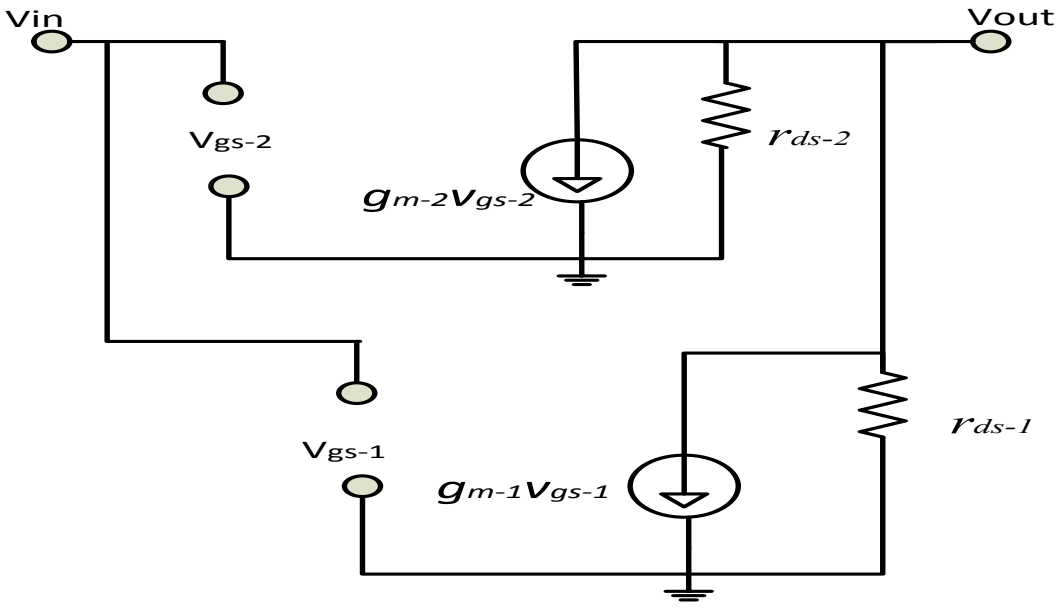


Fig.4.23 Small-Signal Model of Inverter

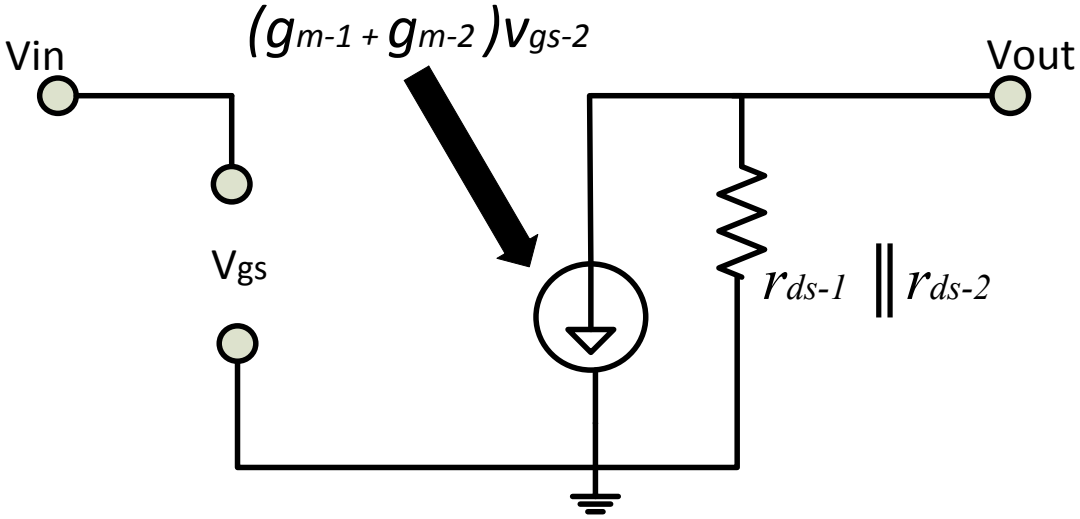


Fig.4.24 Simplified Small-Signal model of Inverter

Ignoring body effect and solving for the gain of the inverter we get

$$\frac{V_{OUT}}{V_{IN}} = -(g_{m1} + g_{m2})(r_{ds1} \parallel r_{ds2}) \qquad (4.6)$$

So it can be seen that changing the power supply increases the gain of the inverter. As both the threshold voltage and gain vary, significant jitter and pulse width distortion results as shown in Fig. 4.26

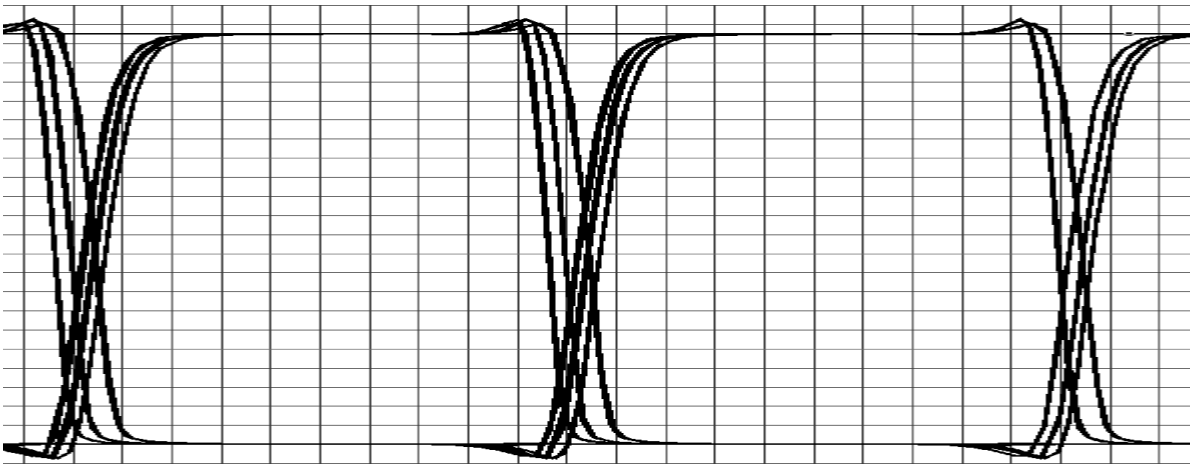


Fig.4.25 Pulse-Width Distortion in the eye diagram of inverter.

3. For different levels of modulation current we need to lower down the Power supply V_X as well. But lowering down the power supply means that the current is reducing and the charging and discharging of the capacitive load is directly proportional to the current. So if we vary the power supply then the delay of the inverter drastically increases which is not a desirable effect for the high speed design.

4.3.2.1.2 Common Source Stage Modulation Current Control

The second option that was looked into for the generation of modulation current control is a common source stage with a resistive load, see Fig. 4.26. Again, modulation control was provided by varying the supply voltage V_X was varied. In a second variant, the load resistor was replaced by a NMOS transistor as shown in Fig. 4.27 whose gate voltage V_B was changed to generate different swings for Modulation current.

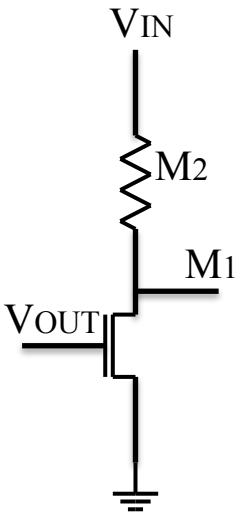


Figure 4.26 Common Source with Resistive load

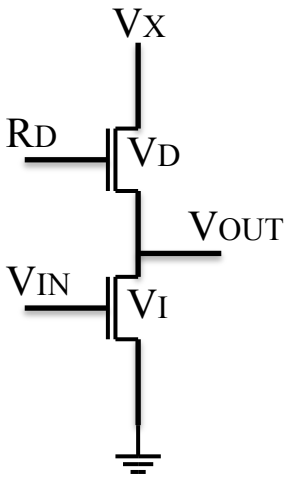


Fig.4.27 Common Source with NMOS transistor as a load

A small signal model for common source stage with resistive load is shown in Fig. 4.28

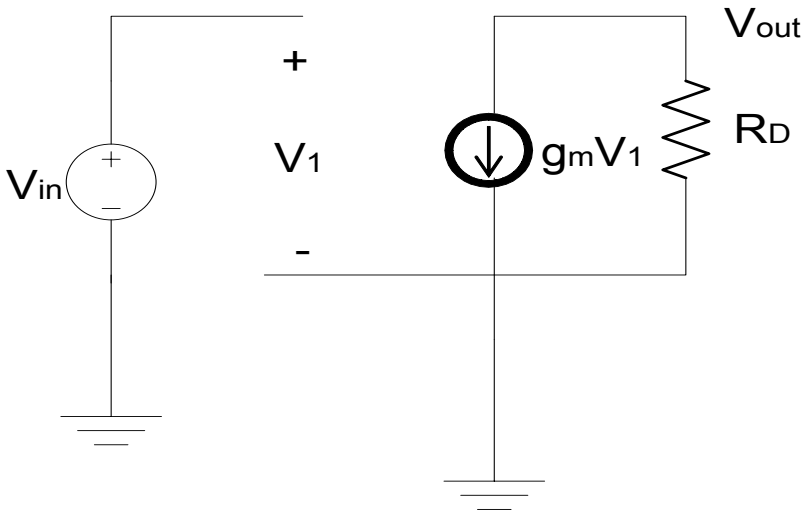


Fig.4.28 Small Signal model of a Common Source with resistor as a load

Assuming that the transistor is in saturation, the small signal current through resistor R_D is given by:

$$i_D = g_m V_{in} \quad (4.7)$$

Its output voltage is then:

$$V_{OUT} = -i_D . R_D = -g_m V_{in} R_D \quad (4.8)$$

and hence the small signal voltage gain is:

$$A_v = \frac{V_{OUT}}{V_{IN}} = -g_m R_D \quad (4.9)$$

The transconductance g_m is given by

$$g_m = \sqrt{2 \frac{W}{L} \mu_n C_{ox} I_D} \quad (4.10)$$

From Fig. 16, the bias current ID is given by:

$$I_D = \frac{V_X - V_{OUT}}{R_D} \quad (4.11)$$

As the input to the common source stage is rail to rail and the gain of the amplifier is always higher than 1 given by equation (4.7) the output saturates at lower supply voltages: it is therefore not a very good solution for the block that we desire as there is a need for lower swing voltages to generate lower levels of modulation current. This amount to shifting the problem from the common-source output to the common-source pre-driver stage.

Another issue with this block is that its bias current is directly dependent on the supply voltage as seen from equation (4.11). Hence if the supply voltage V_X is lowered, itsbias current also lowers, reducing the bandwidth and capability to drive the main driver (whose gate capacitance is fixed and therefore will take a longer time to charge for lower pre-driver bias currents)

If the resistive load is replaced by the transistor as shown in Fig. 4.27 then the gain of the amplifier is given by

$$A_v = -g_{m1} r_{ds1} \parallel r_{ds2} \qquad (4.12)$$

This is still typically (assuming similar W and L) gain as opposed to the requirements of the block. Moreover due to the extra transistor, the challenge to keep the transistor in saturation increases due to voltage headroom. And the current flowing in the circuit is now dependent on V_B which if reduced creates the problem for driving the next stage.

4.3.2.1.3 High Frequency analysis of Common Source Stage

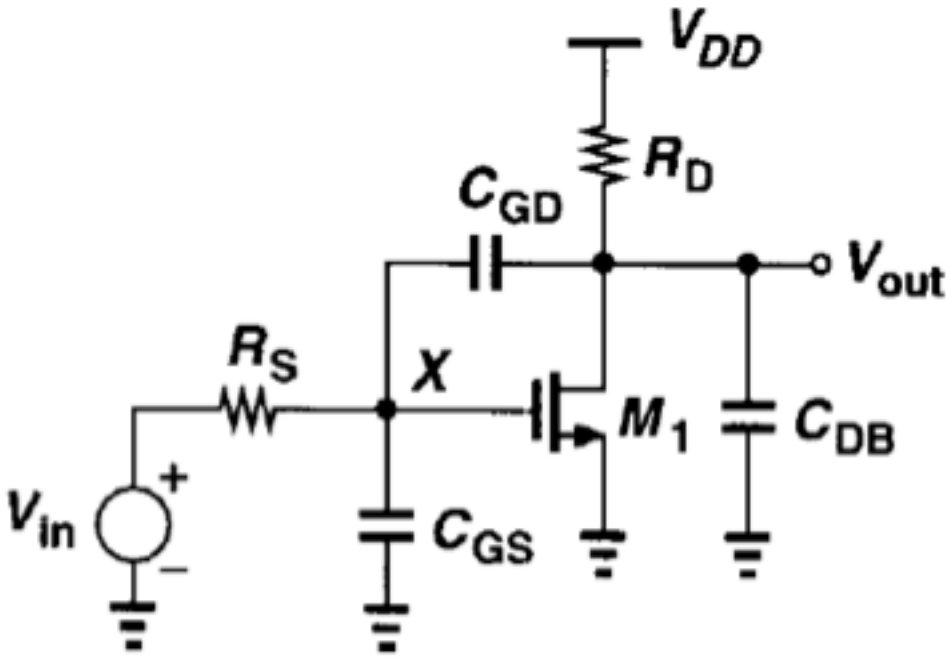


Fig.4.29 High Frequency Model of Common Source stage

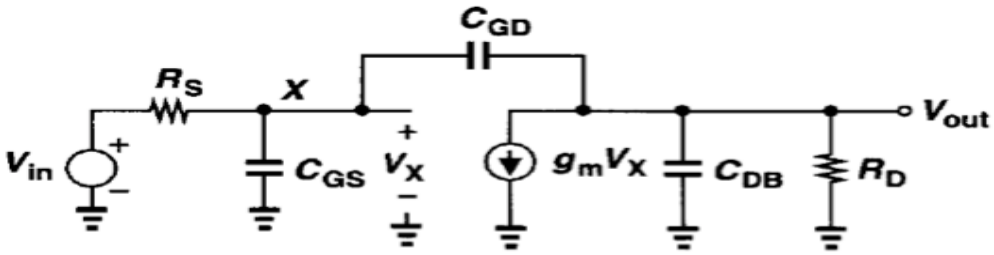


Fig.4.30 Equivalent Circuit of Common Source high frequency model

Gain Vout/Vin is give by the following equaition

$$\frac{V_{out}}{V_{in}}(s) = \frac{(C_{GD}s - g_m)R_D}{R_S R_D \xi s^2 + [R_S(1 + g_m R_D)C_{GD} + R_S C_{GS} + R_D(C_{GD} + C_{DB})]s + 1}$$

$$\xi = C_{GS}C_{GD} + C_{GS}C_{DB} + C_{GD}C_{DB} \tag{4.13}$$

It is difficult to achieve high speed using Common Source stage as the bandwidth of the common source gain stage contains all the possible parasitic capacitances from the MOS transistor. Hence it is not chosen as the driving stage for the VCSEL driver.

4.3.2.1.4 Source-Follower Stage

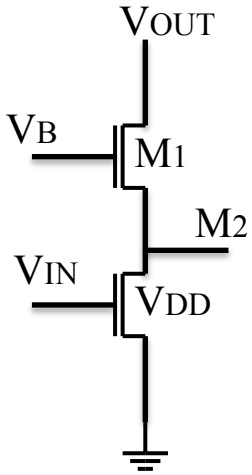


Fig.4.31 Source Follower with NMOS transistor as a load

Fig.4.31 shows a source follower M_1 with NMOS transistor M_2 as a load. We have used this stage as a block to control the modulation current as its gain is slightly less than unity and further to this it also acts a level shifter which is what we desire as the input driving this source follower is rail to rail.

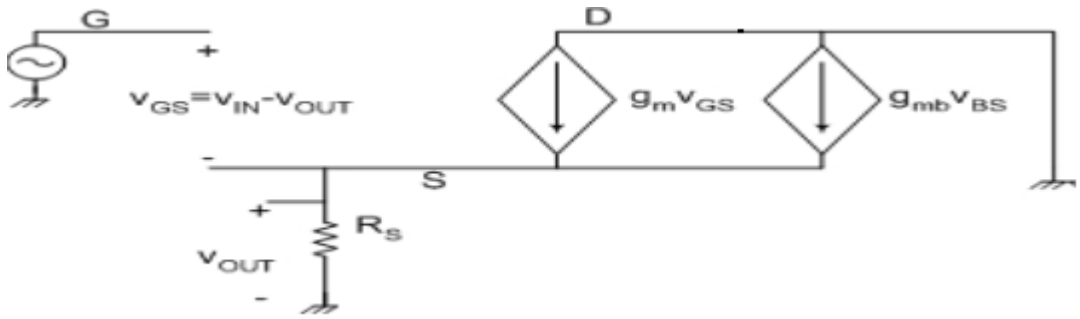


Fig.4.32 Small Signal Model of a source follower stage

Fig. 4.32 depicts the small signal model of source follower stage where R_S is the output resistance of transistor M_2.

For the gain of the amplifier we further simplify the small-signal model and is shown in Fig.4.33

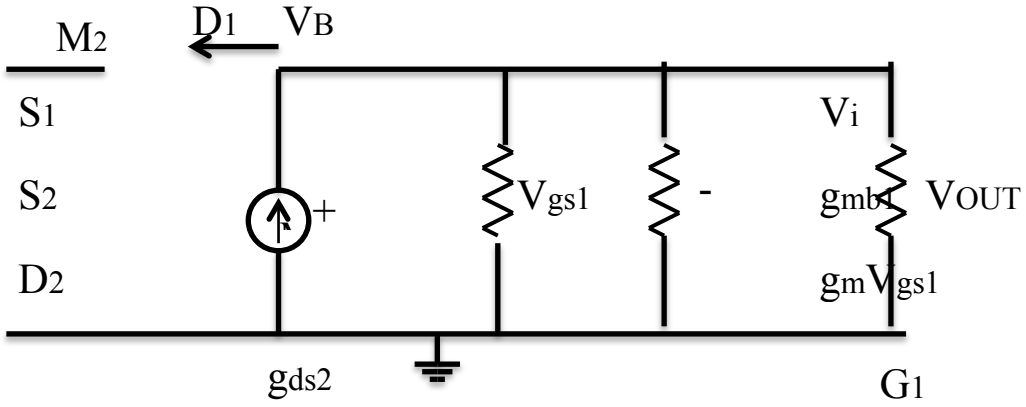


Fig.4.33 Simplified small signal model of source follower

So summing the current at the output V_O we get

$$g_{m1}V_{gs1} = V_O(g_{mb1} + g_{ds1} + g_{ds2}) \qquad (4.14)$$

$$V_{gs1} = V_i - V_o \tag{4.15}$$

Replacing the value of V_{gs1} in 4.13 we get

$$g_{m1}V_i = V_O(g_{mb1} + g_{ds1} + g_{ds2} + g_{m1}) \tag{4.16}$$

So the gain is then represented by

$$V_O/V_i = \quad g_{m1}/g_{mb1} + g_{ds1} + g_{ds2} + g_{m1} \tag{4.17}$$

So from equation 4.17 one can easily deduce that the gain of a source follower is always less than one.

With gain less than unity this stage is perfect for us to use for the modulation current control as the gain can be controlled by varying the DC voltage at V_B as it will shift the DC level of the amplifier and since V_{GS} of the input transistor is nothing but V_{IN}-V_{OUT} so if we change the V_{OUT} which is the voltage at the source of the input transistor the gain will change as g_m of the transistor will change.

4.3.2.1.5 High Frequency Analysis of Common Drain stage

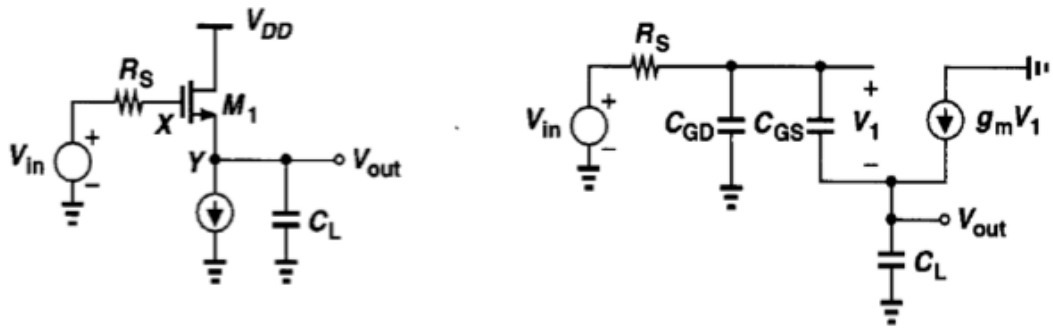


Fig.4.34 High frequency model of Common Drain Stage.

The gain is given by

$$\frac{V_{out}}{V_{in}}(s) = \frac{g_m + C_{GS}s}{R_S(C_{GS}C_L + C_{GS}C_{GD} + C_{GD}C_L)s^2 + (g_m R_S C_{GD} + C_L + C_{GS})s + g_m}$$

$$\omega_{p1} \approx \frac{g_m}{g_m R_S C_{GD} + C_L + C_{GS}} = \frac{1}{R_S C_{GD} + \dfrac{C_L + C_{GS}}{g_m}}.$$

(4.18)

If Rs is not too high this stage has a high bandwidth, which is the case in the amplifier that is designed. Hence this block gives us the perfect choice to be used as a buffer as well as a block where modulation control current could be possible

4.4 SIMULATED RESULTS

Fig. 4.35 shows the eye diagram at the schematic level operating at 56Gb/s with no parasitics included. Fig. 4.36 shows the transient current trace of the output.

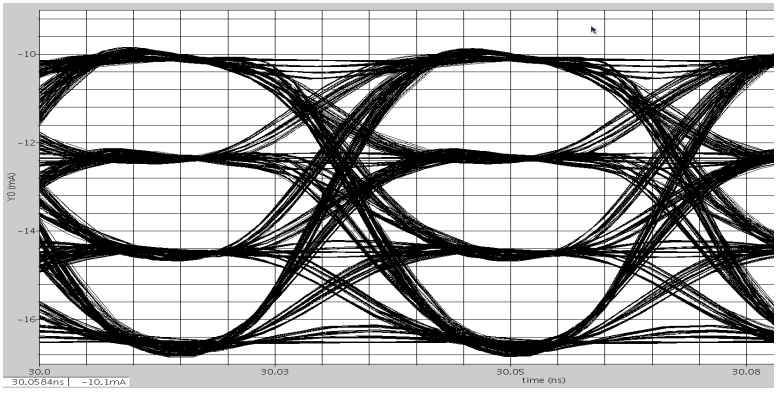


Fig.4.35 Eye diagram of the VCSEL current at 56Gb/s (28Gbaud).

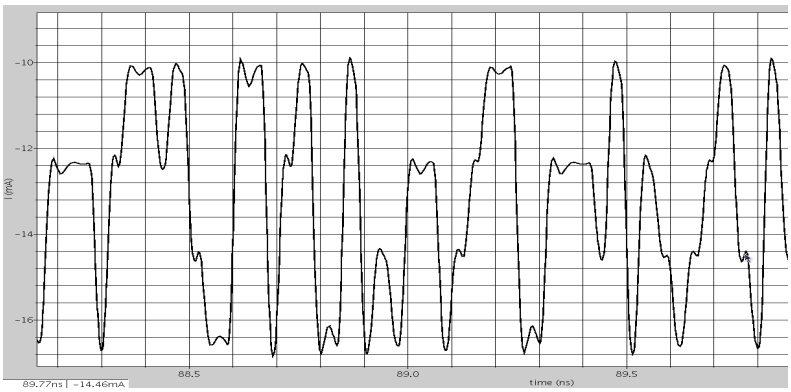
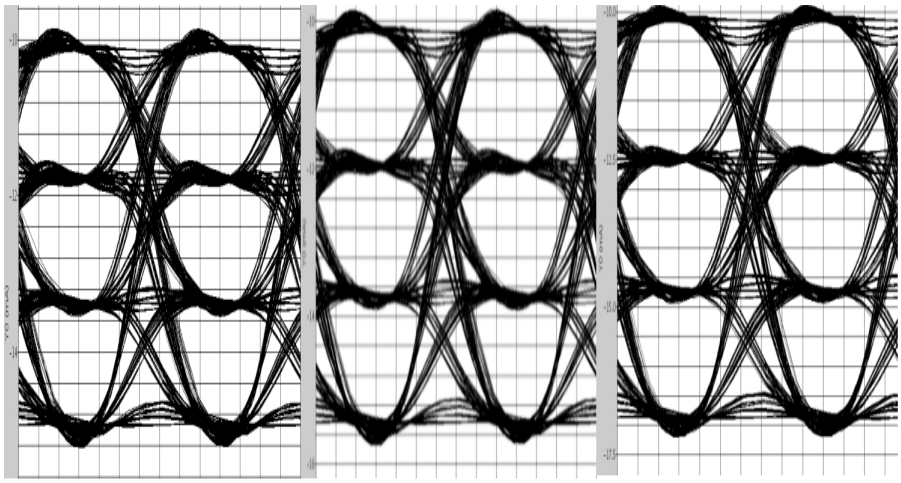


Fig.4.36 Time trace the of VCSEL current at 56Gb/s (28Gbaud).

Fig. 4.37 depicts the eye diagram of the output at the schematic level when the modulation current is varied from 4.5mA to 7.5mA.



3ΔI = 4.5mA 3ΔI = 6.0mA 3ΔI = 7.5mA

Fig.4.37 Eye diagram of VCSEL current @ 56Gb/s for different modulation levels.

Fig. 4.38 presents the eye diagram of the chip after the layout including all the possible parasitics (capacitor, resistor and inductor). Fig. 4.39 shows the compete layout of the chip.

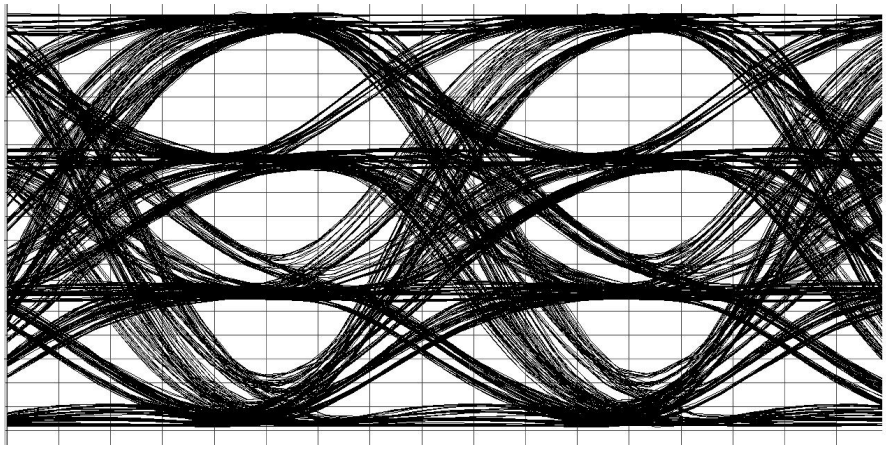


Fig.4.38 Post Layout eye diagram at 56Gb/s (28Gbaud).

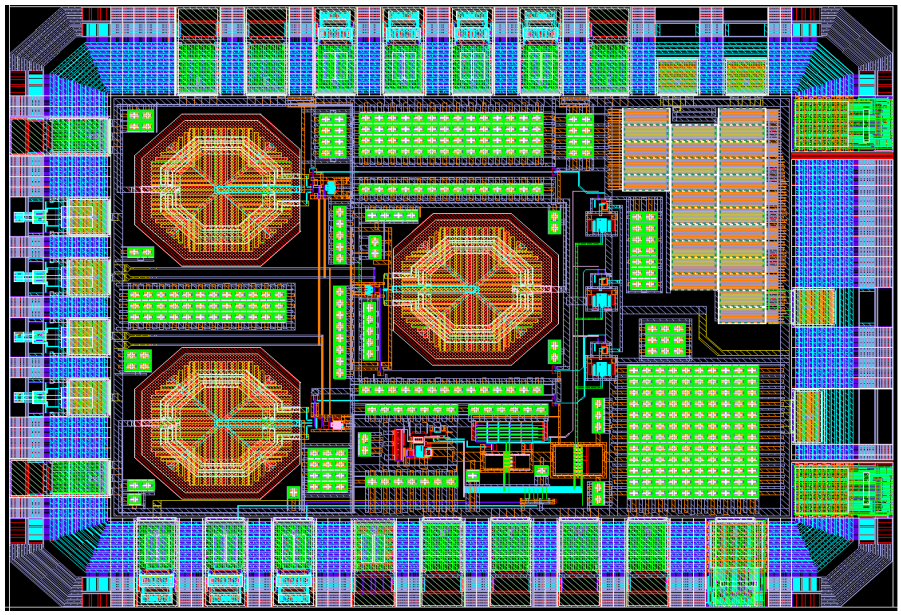


Fig.4.39 Mask Layout of PAM4-VCSEL driver

4.5 CONCLUSION

A novel topology for a PAM-4 VCSEL driver has been presented. The driver circuit only switches the current corresponding to the PAM symbol being transmitted thus saving significant power compared to conventional designs. For a bias current of 10 mA and a peak modulation current of 7.5 mA, the chip consumes only 32 mW. At a throughput of 56 Gb/s, this results in 0.5 6pJ/bit. Table 4.4 presents the comparison of our work with the state of the art PAM-4 based transmitters.

Ref	**Bitrate (Gb/s)**	**Baudrate (Gbaud)**	**Chip area (mm^2)**	**Technology**	**Supply Voltage(V)**	**Power Consumption (mW)**	**Energy Efficiency pj/bit**	**Reported with adjustable voltage swing or bias and modulation currents?**
[28]	32	16	1.7X1.8	130nmCMOS	1.8&3.0	1600	50	No
[75]	10	5	2.6X1.5	180nmCMOS	2.0	121	12.1	No
[76]	25	12.5	1.0X0.5	90nmCMOS	1.0	99.3	3.97	No
[29]	20	10	1.3X1.2	180nmCMOS	1.8	252	4.5	No
Our Work	**56**	**28**	**0.98X0.76**	**65nmCMOS**	**1.2**	**32**	**0.56**	**Limited**

Table 4.4 Comparison between our work and state of the art PAM-4 transmitters

5
AN INDUCTORLESS LINEAR OPTICAL RECEIVER FOR 20GBAUD PAM-4 MODULATION USING 28NM CMOS

5.1 INTRODUCTION

In the last few years, we have witnessed the emergence of large data centres that support internet applications such as cloud computing etc. Such data centres consist of large groups of servers connected together using high-speed optical links [86]. State-of-the-art transceivers for these links offer 100Gb/s bit-rates, achieved by multiplexing 10x 10 Gb/s or 4x 25 Gb/s channels [87]. In the next few years, data centre operators expect a need for 400 Gb/s and even 1 Tb/s links [88]. As continued multiplexing of channels is difficult to achieve, another option is to use advanced, multilevel signaling formats such as e.g. Multi level pulse-amplitude modulation (M-PAM) [89], whereby groups of bits are encoded into different signal levels. PAM-4 in particular is currently receiving attention due to its potential for power reduction and relative implementation simplicity.

Although multilevel signaling reduces the bandwidth requirements (e.g. ~20 GHz for a 56 Gb/s, 28Gbaud signal) for the optics and electronics for a given bitrate, on the other hand it requires the receiver to be linear over a wide dynamic range (typical dynamic ranges for short-reach links are ~15 dB) such that all the levels in the PAM symbol constellation are amplified equally. Such a linear optical receiver is significantly more complicated than a conventional (limiting) receiver. In addition, the use of parallel lanes sets tight constraints on the size and power consumption of the receiver. Power consumption is usually expressed as required energy per transmitted bit, and widely quoted targets are no more than a few picoJoule/bit. Here, it is proposed to use 28 nm CMOS technology to achieve these energy

efficiency targets. Additionally, such an advanced node has the advantage that inductorless operation is achievable, significantly reducing the required area for the receiver.

Several linear optical receivers have been reported in the literature. In [90], a 2.5 Gb/s receiver for PAM-4 is reported using a 0.35 µm BiCMOS. A 10 Gb/s linear TIA is reported in [91] but was optimized for burst-mode operation: it was implemented with a 0.25 µm SiGe BiCMOS technology. In [30] 40 Gb/s operation is achieved using a 0.13 µm SiGe BiCMOS technology. High-speed (up to 40 Gb/s) linear optical receivers have also been designed in 180 nm CMOS [32], 90 nm CMOS [33] and 65 nm CMOS [31]. All these receivers however used on-chip inductors to extend the bandwidth, which consumes large amounts of chip area. Inductorless transimpedance amplifiers (TIAs) have been reported in [92, 93], but have so far not achieved 10GHz bandwidth, nor have put much emphasis on high linearity (e.g. low harmonic distortion).

Our proposed TIA achieves high linearity through an optimized biasing scheme for a regulated gate cascode (RGC) based TIA. In addition, the required gain control is done such that the frequency response (bandwidth, peaking and group delay variation) remains relatively constant, irrespective of the actual gain.

5.2 ARCHITECTURE OF THE LINEAR RECEIVER

Fig. 5.1 shows the block diagram of the receiver: a photodiode converts light to a current, this current is next buffered using a regulated cascode stage (RGC_R) and provided to a differential TIA constructed around amplifier A_1. Using a second replica RGC (RGC_D) a voltage reference level is provided to A_1 to support the single-ended to differential conversion. The TIA gain can be adjusted by the MOSFETs M_1 and M_2 (biased in triode region) connected in parallel across the feedback resistors R_F. Three additional variable gain amplifiers (VGAs) $A_{2,3,4}$ further amplify the

differential voltage at the output of the TIA to full swing. These amplifiers were tapered and the final amplifier A4 drives 50 Ω termination resistors. To ensure proper operation of the receiver circuit across a wide dynamic range, two feedback loops have been added: a dc-offset compensation loop and an automatic gain control (AGC) loop. The dc-offset stems from both the unipolar character of the photodiode output, a deterministic offset current from the RGC buffer and random dc-offsets due to mismatch between assumed identical components.

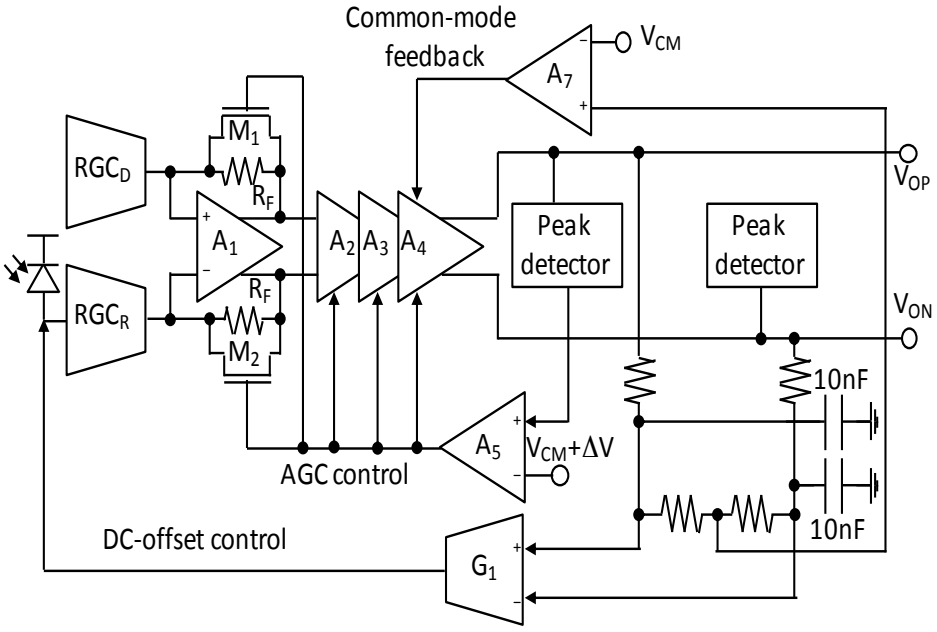


Fig.5.1 Top-level diagram of the linear optical receiver

The dc-offset compensation loop works by measuring the difference between the dc-levels of both output phases using the low-pass filter consisting of resistors R_{LP} and (off-chip) capacitors C_{LP}. Using transconductor G_1, this difference is amplified and converted into a current which is injected into the input of the TIA.

The AGC loop generates a control voltage V_{AGC} which simultaneously adjusts the gain of the TIA and the post-amplifiers $A_{2,3,4}$. Contrary to previously presented AGC

schemes for optical receivers [91, 94, 95], no complicated additional level shifting circuitry is required to adjust the gain control voltage to a range compatible with the TIA and various post-amplifiers. As explained in paragraphs below this is achieved by: 1) using the same topology for amplifiers $A_{1,2,3,4.}$; 2) using MOSFETs biased in their triode region to adjust the individual gains and 3) by ensuring the source voltages of the gain control MOSFETs are at nominally the same voltage. The advantage is a robust gain control scheme with repeatable behaviour, in particular this helps to maintain stable bandwidth versus gain setting. The control voltage V_{AGC} is generated by comparing the peak voltage of the output signal to the desired voltage swing. As a peak voltage is most readily detected single-ended using a peak detector, the entire AGC loop is single-ended in nature. This means that the absolute voltage corresponding to the desired output voltage swing needs to be referred to a given common-mode voltage V_{CM}. For the desired output voltage swing ΔV this can be simply done by adding ΔV to a reference voltage V_{CM}. The differential output of the final stage VGA is then referred to V_{CM} using common-mode feedback (CMFB): only the last stage A_4 uses CMFB to minimize die area. An error amplifier (A_5) is then used to amplify the difference between the desired peak voltage and the detected peak voltage. This difference is then fed back to the V_{AGC} input on all four VGAs. The bandwidth of the AGC loop is determined by the tracking behaviour of the peak detector, set by a deliberate leakage current designed to be ~10 nA. With a 5 pF peak hold capacitor resulting in a 2mV/µs droop rate, sufficient to track slow changes in the input power while at the same time avoiding unwanted interference with the dc-offset compensation loop. Optimum values for V_{CM} and ΔV were 0.75 V and 25 mV (limited to guarantee linearity) respectively. The total differential output swing equals 4ΔV.

5.2.1 TRANSIMPEDANCE AMPLIFIER

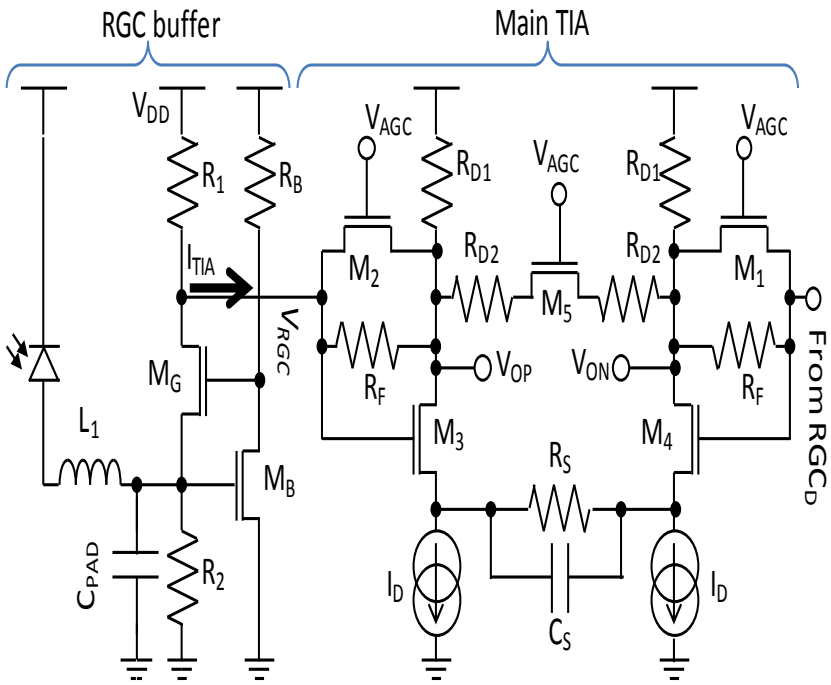


Fig.5.2 Regulated gate cascode TIA.

Fig. 5.2 shows the circuit diagram of the TIA: it uses a regulated gate cascode (RGC) input stage which lowers its input impedance using local negative feedback compared to conventional TIAs, in turn providing high bandwidth [96].

To ensure high linearity, it is important to consider the current I_{TIA} flowing through the feedback network (resistors R_F and MOSFETs M_1,M_2) of the main TIA. Indeed as shown the RGC current buffer exhibits an (here unwanted) dc current $I_{TIA,DC}$ defined by:

$$I_{TIA} = I_{TIA,DC} + i_{PD}(t) = \frac{V_{DD} - V_{RGC}}{R_1} - \frac{V_{GSB}}{R_2} + i_{PD}(t) \quad (5.1)$$

where V_{DD} is the supply voltage, V_{RGC} the voltage at the output of the RGC buffer, V_{GSB} the gate-to-source voltage of feedback transistor M_B and $i_{PD}(t)$ the photodiode current. As this dc current flows through the feedback network, it effectively adds

to the (wanted) photodiode current. Note how (see Fig. 5.1) this dc current is a common-mode input current for the main differential TIA. Indeed there is a second RGC buffer RGC_D connected to the other input terminal of the main TIA, which has nominally the same dc current $I_{TIA,DC}$. In principle, the differential TIA only amplifies the difference between the two currents. However, the input common-mode voltage of the main TIA contains a component which linearly increases with $I_{TIA,DC}$:

$$V_{CM,IN} = V_{DD} - R_{D1}I_D + R_F\left(I_{TIA,DC} + i_{PD}(t)/2\right) \qquad (5.2)$$

where R_{D1} is the drain resistor load of the differential amplifier and $2I_D$ its bias current. If $I_{TIA,DC}$ is too large, it can push the main TIA out of its linear operating regime resulting in strong non-linear distortion. However by noting that:

$$V_{GRC} = V_{DD} - R_{D1}I_D + \frac{R_F}{2}I_{TIA} \qquad (5.3)$$

and combining with (5.2), one can see that $I_{TIA,DC}$ is 0 if:

$$\frac{V_{GSB}}{R_2} = \frac{R_{D1}}{R_1}I_D \qquad (5.4)$$

This condition can be easily fulfilled by copying and suitably scaling the bias current of transistor M_B in the replica RGC buffer RGC_D (see Fig. 5.1). To ensure linear operation across a wide dynamic range, the gain of the main TIA needs to be reduced for large input signals, which as explained is done by turning on MOSFETs M_1 and M_2. It is well known that for a simple TIA model, its dominant pole is:

$$2\pi p_D = \frac{A}{R_{F,TOT}C_{IN}} \qquad (5.5)$$

where C_{IN} is the capacitance at the input node of the TIA, $R_{F,TOT}$ the total feedback resistance and A the forward voltage gain of the differential amplifier. Clearly by decreasing the feedback resistance the dominant pole moves to a higher frequency, closer to the secondary pole of the TIA, which is located at the drain of MOSFETs M_3 and M_4 of the differential amplifier. This results in ringing or even oscillations. By reducing the gain of the differential amplifier however, the dominant pole can be maintained at a constant frequency, thus maintaining stable bandwidth and minimizing peaking. An additional source feedback resistance R_S combined with a

capacitor C_S to create a zero, which if placed in the vicinity of the secondary pole (at the drains of MOSFETs M_3, M_4) helps to reduce peaking. It is important to note that the source voltage of the gain control MOSFETs M_1, M_2 and M_5 are roughly equal to each other, which allows to use the single gain control voltage V_{AGC} to adjust the gain of the TIA.

5.2.1.1 Small Signal Analysis of Regulated Gate Cascode Input Stage

Fig. 5.3 shows the RGC input stage of Transimpedance amplifier used in this design in which

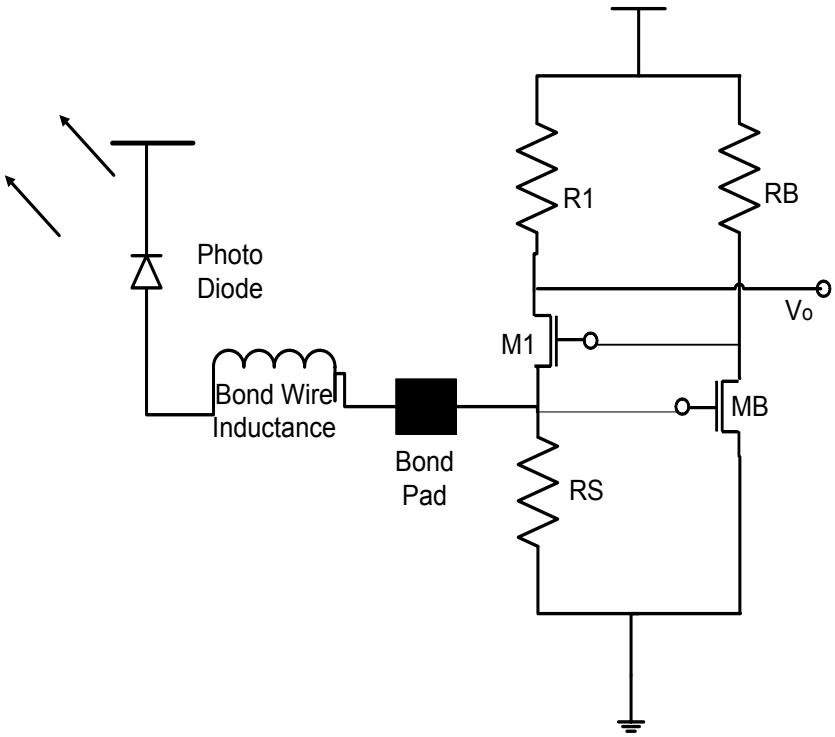


Fig.5.3 RGC input stage of the transimpedance amplifier.

The photodiode current is sent into the source of M_1 and further amplified into a voltage at the drain of M_1. The second stage (transistor M_B and resistor R_B) acts as a

local feedback stage which reduces the input impedance by a factor equal to its gain, see (5.6)

$$Z_{in} = 1/(g_{mG} + g_{mB} R_B) \qquad (5.6)$$

This reduced input impedance allows to achieve higher bandwidth. Fig. 5.4 represents the small signal diagram of the RGC stage.

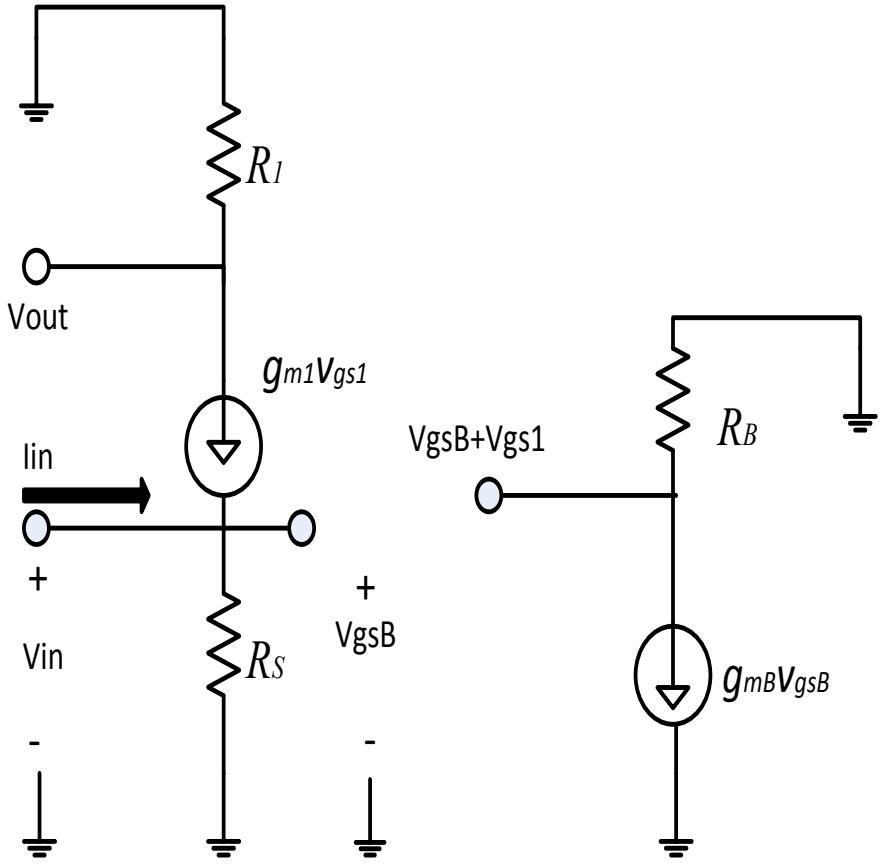


Fig.5.4 Small signal Diagram of RGC input stage.

Ignoring the parasitic capacitances it can be deduced from Fig 5.4 that

$$V_{GS1} + V_{GSB} = -g_{mB} V_{GSB} R_B \qquad (5.7)$$

Fig. 5.3 can also be redrawn as Fig. 5.4

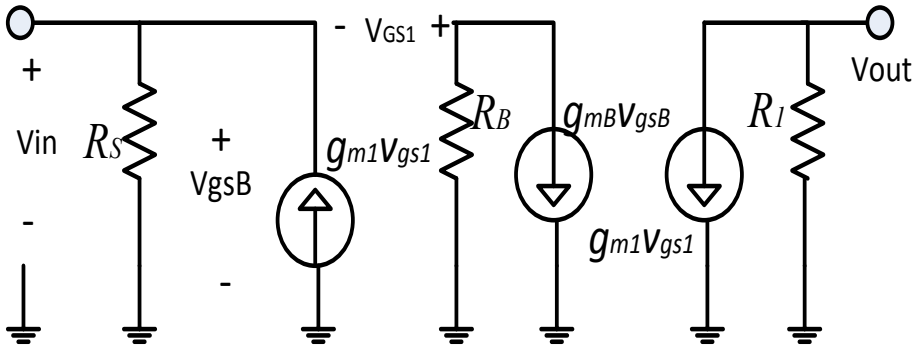


Fig.5.5 Redrawn structure of Fig. 5.4

From equation 5.7 it can be deduce that

$$V_{GS1} = -V_{GSB}(1 + g_{mB} R_B) \qquad (5.8)$$

Then the dependant current source is now rewritten as

$$g_{m1} V_{GS1} = -g_{m1} V_{GSB}(1 + g_{mB} R_B) \quad (5.9)$$

Since the voltage across this current source is proportional to the the current through the source by a factor of VGSB, the current source with its polarity reversed as shown in Fig. 5.5 can be replaced by an equivalent resistorof value $\frac{1}{g_{m1}(1+g_{mB}R_B)}$ as shown in Fig. 5.6

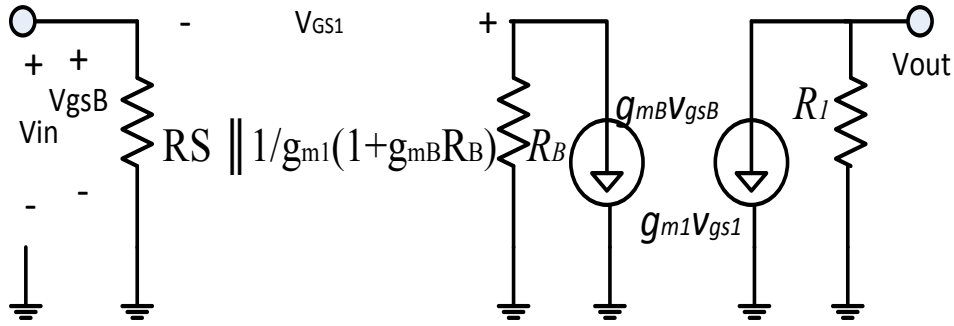


Fig.5.6 Replacing the current source with an equivalent resistor

Since $V_{GSB} = V_{in}$ it can be defined as

$$V_{GSB} = R_s \| \frac{1}{g_{m1}(1 + g_{mB}R_B)} * I_{in} \qquad (5.10)$$

$$Z_{in} = V_{GSB}/I_{in} = R_s \| \frac{1}{g_{m1}(1 + g_{mB}R_B)} \qquad (5.11)$$

Which can be approximated as

$$Z_{in} = \frac{1}{g_{m1}(1 + g_{mB}R_B)} \qquad (5.12)$$

5.2.2 Variable Gain Amplifier

Frequently, variable gain amplifiers for optical receivers are implemented as Cherry-Hooper stages to achieve high bandwidth and gain. Variable gain is then achieved by adding a Gilbert-like mixer acting as a multiplier, see e.g. [91]. Such a structure however is challenging to use at low supply voltages due to its stacking of the variable gain transistors (Gilbert mixer), transconductance and transimpedance stages. Additionally, the use of a Gilbert-style mixing stage for gain control requires

additional gain control circuitry, to translate the gain control voltage V_{AGC} to a suitable range.

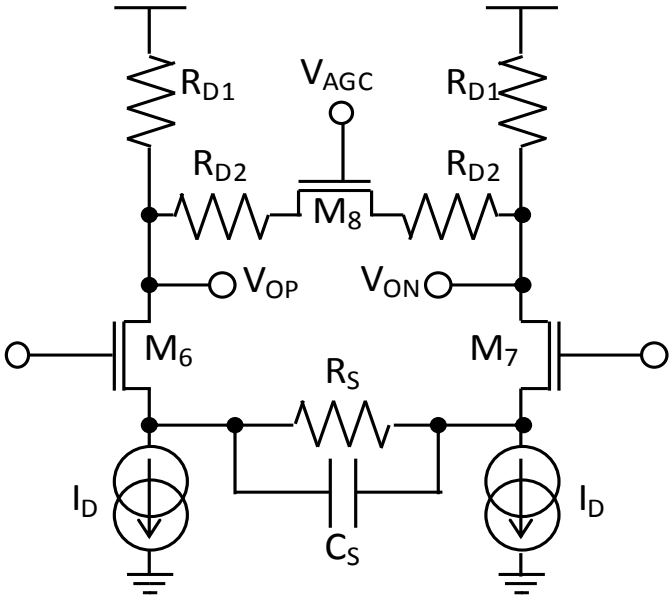


Fig.5.7 Variable Gain Amplifier

Fig. 5.7 shows the schematic of the VGA: using capacitor C_S and resistor R_S a zero is created such that the effective transconductance G_m of the input transistors M_1 and M_2 increases at high frequencies to compensate for the gain roll-off at the output node. Transistor M_8 is used to adjust the gain of the VGA via V_{AGC} by adjusting the effective differential load resistance without affecting its output common-mode voltage.

5.2.2.1 Analysis of Variable gain amplifier

For a differential amplifier to have a broadband response the amplifier used in this design has its differential pair transistors degenerated in such a way that the effective G_m increases at high frequencies compensating for the gain roll-off at the output node.

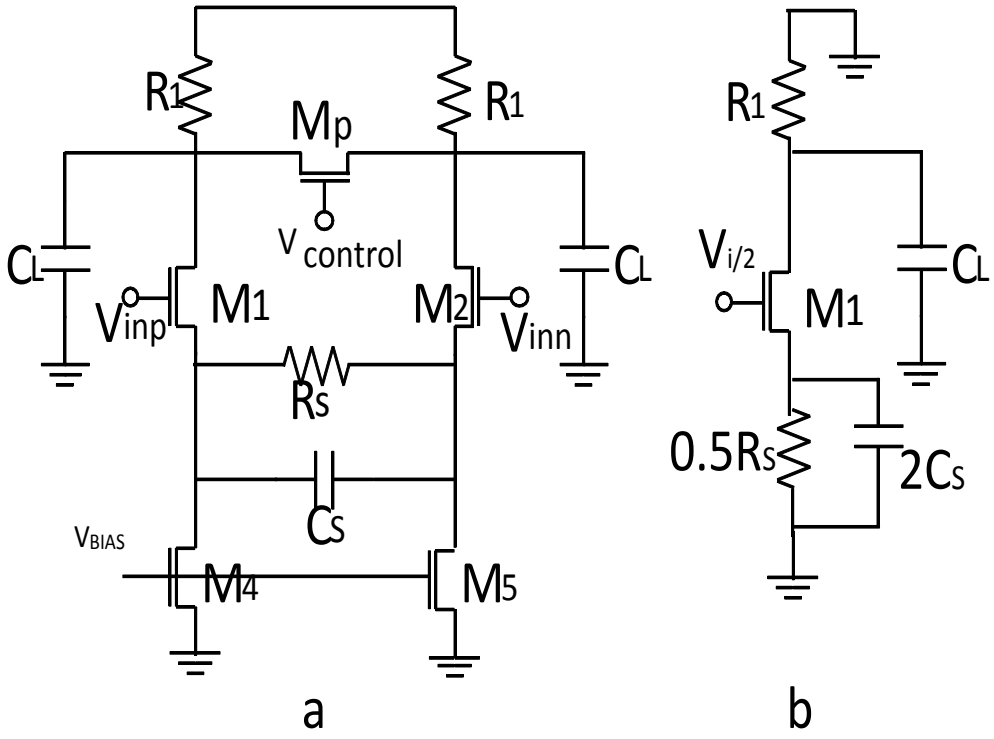


Fig.5.8 (a) Wide band Amplifier (b) Half circuit of Wide band amplifer

From the half circuit of Fig. 5.8 (b) the transconductance of the amplifier is given by [97]

$$G_m = \frac{g_m(R_S C_S S + 1)}{R_S C_S S + 1 + g_m \frac{R_S}{2}} \qquad (5.13)$$

From equation 5.13 it shows that the circuit has a zero at $\frac{1}{R_S C_S}$ and pole *p2* at $\frac{1+g_m\frac{R_S}{2}}{R_S C_S}$ frequencies. This value of zero is used to cancel the pole at the drain of the amplifier which is given by $\frac{1}{R_D C_L}$ in order to move the bandwidth of the amplifier to *p2*. However, if C_S is made too large which means that the zero is pushed to the lower frequency, peaking can be seen in the design and a large value of C_S can actually distort the multistage amplifier bandwidth response. So a care should be taken in selecting the value of this capacitance. Fig. 5.7 shows the wide band amplifier which is used in the design in which M_8 is the PMOS transistor used to control the gain of the multistage amplifier through the generated $V_{CONTROL}$ voltage.

5.3 EXTRACTED SIMULATION RESULTS

The optical receiver was designed for a 1.5 V supply voltage. All the simulation results included the backannotated RC layout parasitics. The photodiode capacitance was 30 fF, the ESD and IO bondpad capacitance was 160 fF and the bondwire connecting the photodiode to the TIA was modeled using a 250 pH inductance. The core of the optical receiver occupies just 180x100 μm^2 area, the total circuit area including IO pads is 0.5 mm^2. Its power consumption (including the final 50Ω terminated output stage) is 56 mW, of which 18 mW is used in the TIA front-end, 16 mW in the two mid-stage amplifiers and 22 mW in the final output stage.

Fig. 5.9 gives the frequency response for both highest (73 dBΩ) and lowest (46 dBΩ) gain setting.

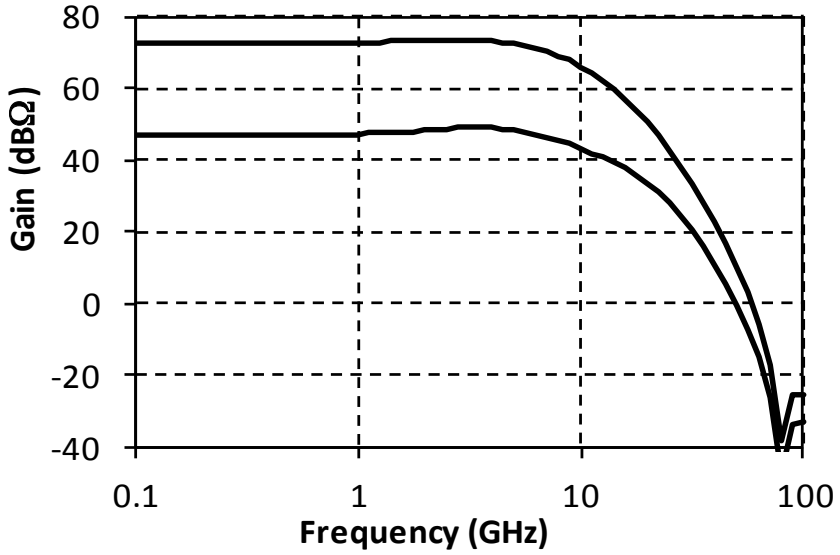


Fig.5.9 Frequency transfer curves for lowest and highest gain.

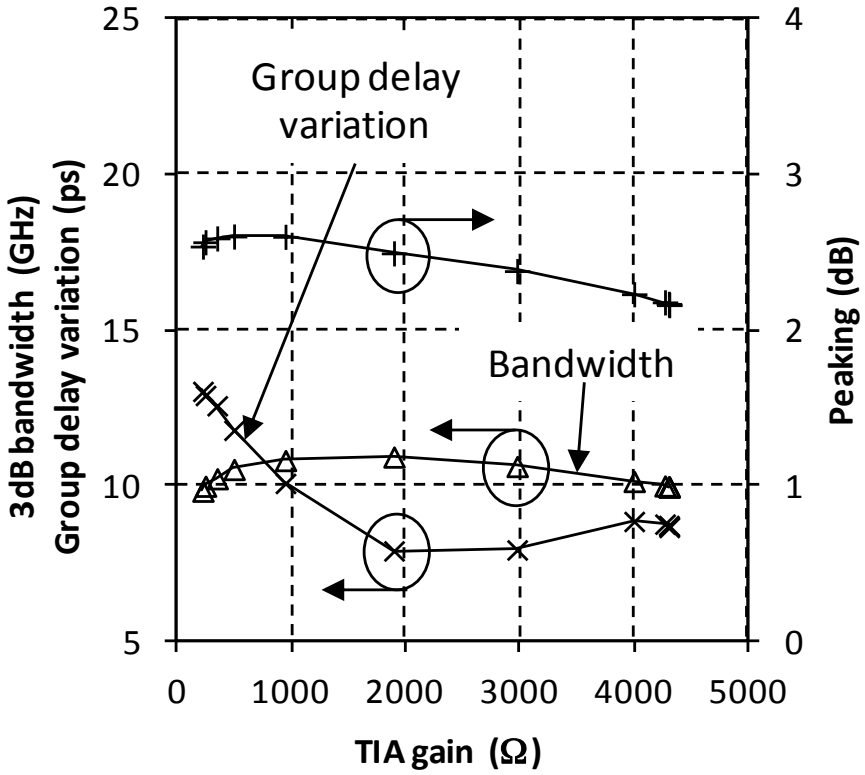


Fig.5.10 Bandwidth (GHz), peaking (dB) and group delay variation (ps) vs. optical receiver gain (Ω).

The 3dB bandwidth, peaking and group delay variation as a function of the gain control voltage V_{AGC} (see Fig. 1-3) is given in Fig. 5.10: note how the bandwidth varies by ~1 GHz despite the gain varying by a factor of 25. The input referred noise density (highest gain setting) at 10 GHz is 25 pA/Hz$^{1/2}$, the integrated (from 10 MHz to 20 GHz) noise current is 2.5 μA_{RMS}.

To test the linearity of the receiver, its total harmonic distortion (THD) was evaluated: the results are shown in Fig. 5.11. As shown in the inset, the input DC current is adjusted such that an extinction ratio of 6 dB is obtained, in accordance with standard industry practice [98]. Less than 5% THD was obtained up till

600μA_{PP}. For a low input current (< 100 μA_{PP}) none of the gain control MOSFETs are on, thus excellent linearity is obtained. In the input current region from 100 μA_{PP} to 200 μA_{PP}, the gain control MOSFETs start to turn on and are on the edge between triode and saturation region. For higher currents (up to 600 μA_{PP}) the gain control MOSFETs are deeper into their triode region which improves linearity again, hence the dropping THD for that region. After that, overload starts to occur in the receiver and the THD increases rapidly.

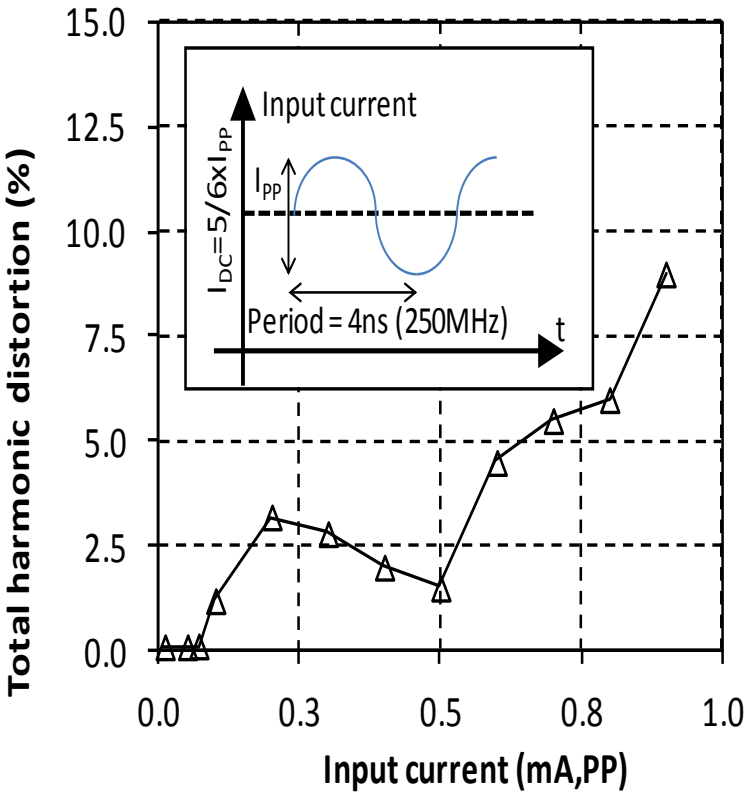


Fig.5.11 Total harmonic distortion versus input current amplitude.

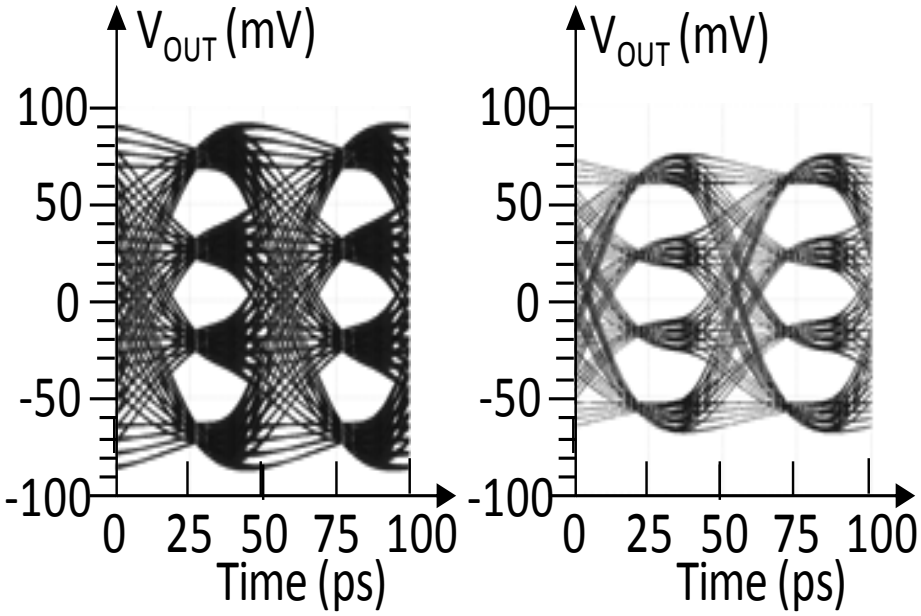


Fig.5.12 PAM-4 eye diagrams at 20Gbaud (40Gb/s): 20μA_{PP} (left), 500μA_{PP} (right)

Finally, Fig. 5.12 shows PAM-4 eye diagrams at 20 Gbaud (40 Gb/s) for the extreme input currents: clear open eyes can be observed with equidistant PAM symbols. Some minor variation in the peak output amplitude can be seen which is due to inaccuracy of the peak amplitude detection.

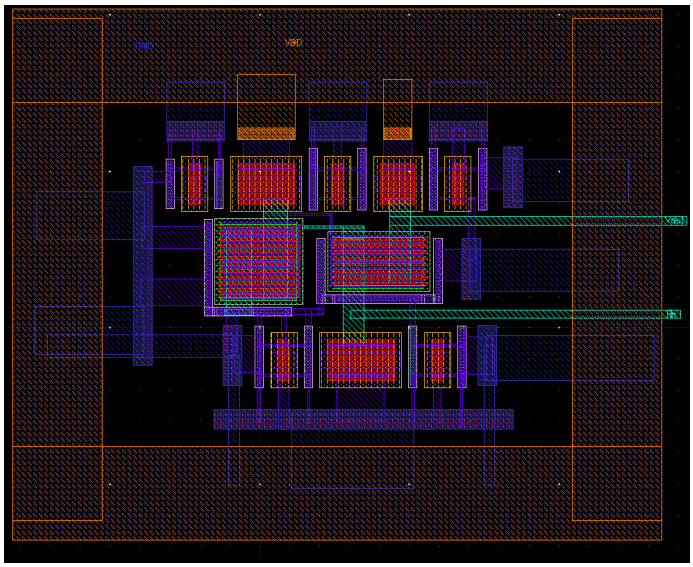


Fig.5.13 Layout of Transimpedance Amplifier

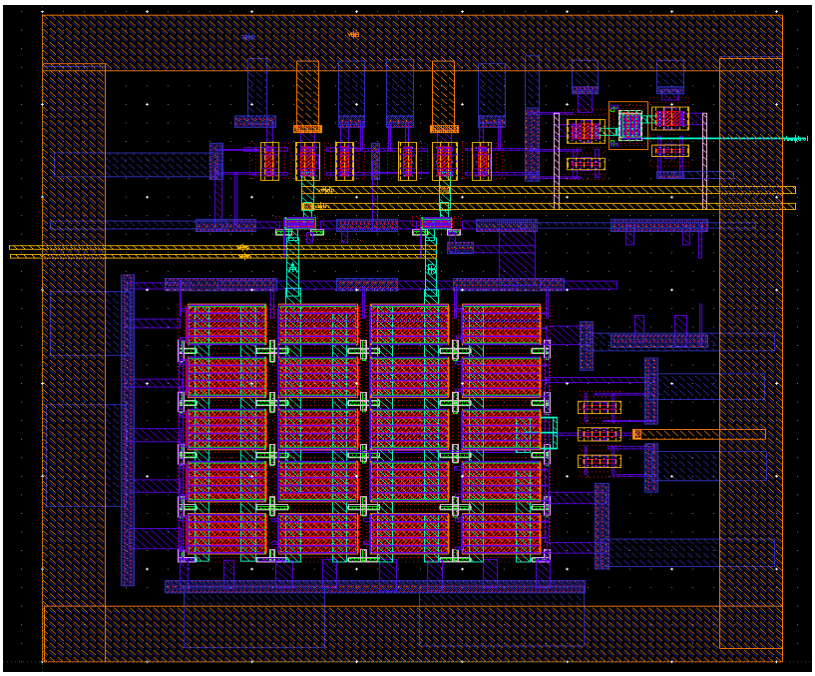


Fig.5.14 Layout of Variable Gain Amplifier

Fig. 5.13 and Fig. 5.14 shows the block layout of Transimpedance Amplifier and of the Variable Gain Amplifier

5.4 CONCLUSION

A linear optical receiver with 10 GHz bandwidth, sufficient for e.g. 20 Gbaud (40 Gb/s) PAM-4 modulation is presented using 28 nm CMOS. No on-chip inductors were required to achieve the bandwidth and high linearity is maintained through an optimized biasing scheme of an RGC-TIA. Table 5.1 shows the comparison of our work with the state of the art linear receivers.

Ref	Gain (dbΩ)	Bandwidth (GHz)	Technology	Area (mm^2)	Supply Voltage (V)	Power Consumption	Input referred Noise density ($pA/Hz^{½}$)	On Chip Inductors	Linearity (THD)
[91]	17.7K	~8	0.25µm SiGe BiCMOS	4.2	3.3/2.5	625	N.A.	No	<5%
[30]	1800	34	0.13µm SiGe BiCMOS	0.5	2.5	80	25.0	No	<5%
[32]	354	30.5	0.18µm CMOS	0.53	1.8	60	34.3	Yes	N.A.
[33]	2K	~20	90nm CMOS	0.56	1.2	75	N.A.	Yes	Limiting
[31]	216	~20	65nm CMOS	0.4	1.2	31.5	30	Yes	N.A
[92]	1258	6	130nm CMOS	0.06	2.0	100	20	No	N.A.
[93]	794	8	130nm CMOS		1.1	16	23	No	N.A
Our Work	**4200**	**~10**	**28nm CMOS**	**0.5**	**1.5**	**56**	**25**	**No**	**<5%**

Table 5.1 presents the comparison between our work and state of the art receivers

6

SUPPORT CIRCUITS FOR LINEAR BURST MODE RECEIVER

6.1 INTRODUCTION

In the last decade, we have witnessed fast deploymentof access networks (which link individual users with the internet) based on fibre-to-the-home (FTTh) technology, especially in the Far East (Japan, China and South-Korea) of the world and US. Such FTTh access networks are usually based on passive optical networks (PONs), where a tree like fibre plant structure is used to connect a number of subscribers to a single central office, see Fig. 6.1

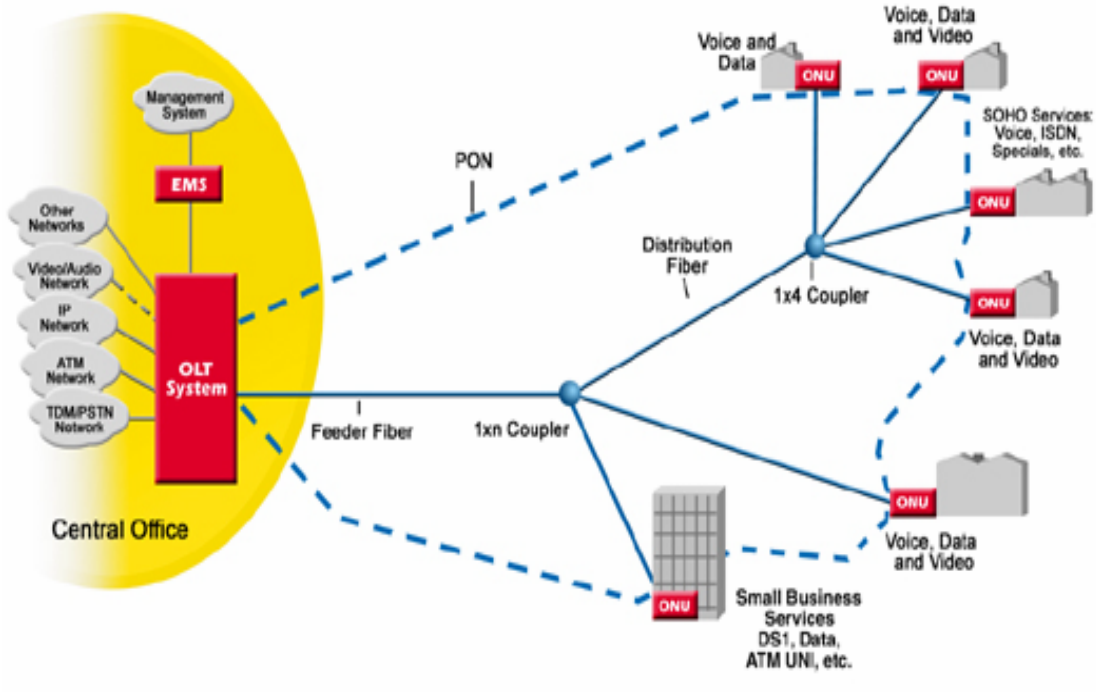


Fig.6.1 FTTh Access Network

A common transmission medium is shared between the subscribers while transmitting the data to the central office (the upstream direction) hence an access protocol is implemented to avoid interference of data between different subscribers. Time division multiple access (TDMA) is widely used, for the reason of low cost, in PONs. In such systems exclusive time slots are allotted to each subscriber in which their data can be transferred in upstream direction. This means the central office receiver and the subscriber transmitter operate in a burst mode where they are continuously switched on and off during its designated time slot. Burst mode receivers (BMRx) in such a system becomes a very critical component as its sensitivity (optical power that can be sampled at a given bit-error-rate) and dynamic range determine the reach and split (amount of subscribers connected to central office) of the system. Since the whole system is operating in burst mode so the receiver should be able to handle a signal which has a quick succession of bursts originating from different subscribers. These bursts exhibit a wide dynamic range from burst to burst due to two main reasons. One is the distance between the subscribers and the central office may vary resulting in different attenuation in the fibre path and second is the launched power from the subscriber's transmitter may vary as well. Which makes the requirement off the receiver very stringent as it need to be able to quickly change its gain and decision threshold (distinction between 1 and 0 transmitted) from one burst to the next. As no data is received when the BMRx is changing its gain settings, which could lower the traffic efficiency, the quick adjustment (within a few tens of nanoseconds to hundreds of nanoseconds) is very vital for the operation of the whole system. The different bursts are separated by the so called guard time as shown in Fig. 6.2, and each bursts start with a short preamble thus giving time for the receiver to adjust.

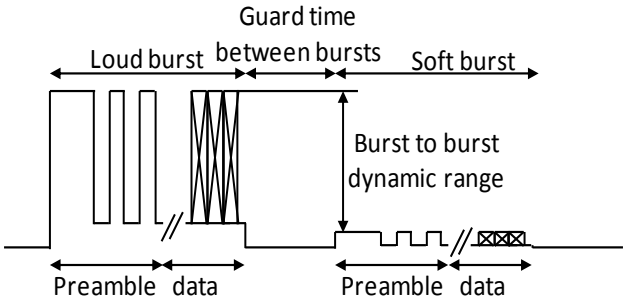


Fig.6.2 input signal of a BMRx consisting of bursts

Today, rapid adoption of new services such as video-on-demand, social 'media', e-government etc. are pushing customer bandwidth demands (both average and peak) ever higher. This is putting network operators under severe strain, as these need to deploy new systems to supply these bandwidth requirements while at the same time remaining profitable. In order to do so, network operators need to drive down their operational expenditure (OPEX) and capital expenditure (CAPEX). To achieve this , an important trend in optical access network research is to develop network technology that can merge today's separate access (linking customers to e.g. local exchanges) and metro systems (linking cities) [99]. Such systems require fibre reaches much longer (over 100 km) to conventional PON systems. To achieve the optical budget including now not only high splitting losses but also fibre losses due to this long reach, optical amplification is a necessity. C-band wavelengths are a preferred option [100, 101] as this enables the use of low-noise, high-gain and high output power erbium doped fibre amplifiers (EDFAs). Due to the much longer reach signal quality will be severely degraded, mainly due to chromatic dispersion , hence some form of dispersion compensation will be required[99]. As the transmission characteristics (such as the chirp, extinction ratio, duty cycle distortion) of different ONUs may be different and as the total fibre length between each ONU and the OLT may vary, the amount of dispersion compensation needs to be adjustable from burst to burst. Electronic Dispersion Compensation (EDC) is then a natural candidate, as adaptability can be achieved by adjusting the tap settings[102]. EDC requires a linear optical receiver which preserves the photodiode current shape (note that we are assuming direct detection: the optical receiver is then linear in terms of the detected photocurrent, however it is quadratic in relation to the detected optical field, which would be required for 'perfect' compensation of chromatic dispersion. These considerations are outside the scope of this text, the interested reader is referred to [ ] for a complete explanation), and hence a linear burst-mode receiver is now required (LBMRx). Continuous-mode limiting and linear RXs up to at least 40 Gb/s are widely available. Until recently, BMRx's were all limiting with speeds up to 10 Gb/s [103-106]. Tyndall designed and tested for the first time an LBMRx is [91]. A classification of different receiver types is given in Fig 6.3.

	Limiting front-ends	Linear front-ends
Continuous-mode	Commercially available	Commercially available
Burst-mode	Emerging	Development by Tyndall

Fig.6.3 Receiver classification.

This work is concentrated on the developing the circuitry for fast gain adaption in LBMRx [100, 101, 107]. Section 6.2 describes the top level architecture of LBMRx and section 6.3 details the circuit implementation of the blocks which I have designed in the system.

6.2 TOP LEVEL ARCHITECTURE

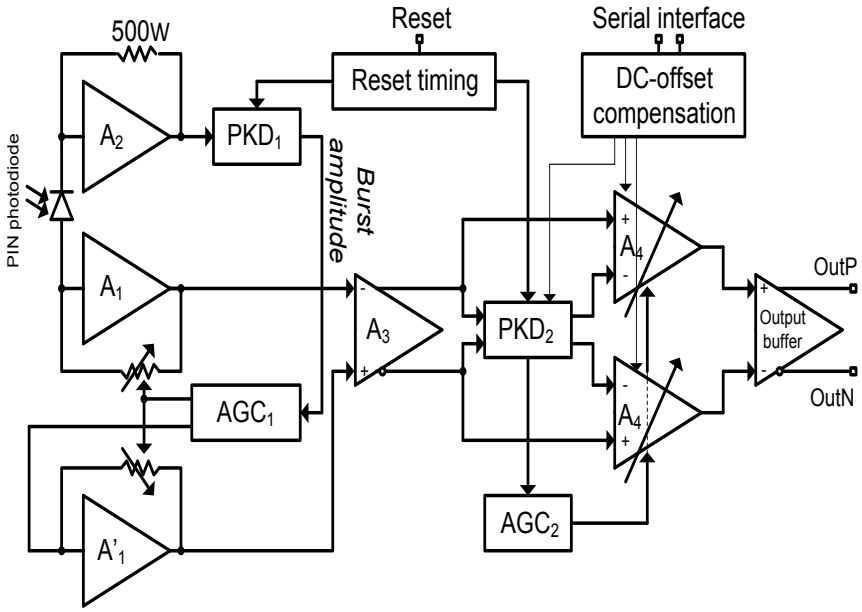


Fig.6.4 Block Diagram of LBMRx

The LBMRx (Fig. 6.4) consists of a transimpedance amplifier (TIA) A_1 with variable gain R_F, a single-ended to differential converter A_2, a differential post-amplification stage (A_{3P}, A_{3N} and peak detectors PKD_2) with variable gain and a 50Ω terminated output buffer A_4. To enable dc-coupling between the stages with wide dynamic range, A_2, A_{3P} and A_{3N} use common-mode feedback (CMFB) which fix their output common-mode (CM) to V_{CM1} and V_{CM2}, respectively. The TIA and the post-amplification stage feature fast automatic gain control (AGC) (AGC_1 and AGC_2), which adjust the gain of these stages such that these operate in their linear region. The peak detectors (see below for further details) for the AGC are reset between bursts using signals $Reset_1$ and $Reset_2$ generated from a timer and an external reset, which can be supplied from e.g. the Medium Access Control chip. A digital interface is used to program settings such as the signal swings (for testing purposes) and dc-offset calibration (see for example for a detailed explanation of the dc-offset compensation)[108] for the post-amplifiers.

The construction of an AGC loop around a TIA requires both the ability to adjust the gain of the TIA with a control signal, as well as a measurement of the signal power (usually at the TIA output). Adjustment of the TIA gain is typically achieved using a MOSFET (biased in its triode region) which is connected across the TIA feedback resistor. The gain can then be varied by tuning the gate voltage of this MOSFET. The signal strength at the output of the TIA can be measured using a peak detector or a low-pass filter with a sufficiently large time constant, usually a few orders of magnitude larger than the bit period. In the former case the AGC loop will adjust the gain of the TIA such that the peak voltage at its output equals a given reference, in the latter case the AGC loop will force the average output of the TIA equal to a reference. When trying to use either of these techniques for fast adjustment of the TIA gain on a burst basis, several problems arise. When using a peak detector, note that in order to reliably detect the weakest burst, the TIA is set to its maximum gain at the start of a burst. To ensure low noise operation, this maximum gain is usually so high that the TIA saturates for signals a few dB above its sensitivity level. Hence if a strong burst arrives, it will saturate the TIA which then takes tens of nanoseconds to recover (e.g. due to the slow response of bipolars when pushed into saturation). Moreover, the peak detector will lock to this saturated level. The AGC loop will react by reducing the TIA gain, however unless the droop rate of the peak detector

is high it will take an unacceptably long time (in the microsecond range) before the AGC loop has settled. While a high droop rate in the peak detector may help (but does not solve the problem of the slow recovery of a saturated TIA), this will lead to undesirable droop during long sequences of consecutive identical digits. Indeed these have a length of the same order of magnitude as the preamble. For example 64B/66B signals (widely used in 10 Gb/s PONs [109]) can have worst-case up to 64 consecutive identical digits corresponding to 6.4ns at 10Gb/s, while the preamble may have a length of a few tens of nanoseconds. A similar problem occurs when using a low pass filter to detect the average value of the signal: now the issue is conflicting requirements on the time constant of the low-pass filter. Here, these problems are addressed as follows. First, instead of using the main TIA A_1 to derive the signal strength, an auxiliary TIA (A_{AUX} in Fig. 6.4) is used which is designed to be linear across the entire dynamic range, and hence does not saturate for strong bursts. As shown in Fig. 6.3, this TIA can be connected to the cathode of the photodetector. This eliminates the problem of the slow response due to saturation of the main TIA during the preamble of strong bursts. Secondly, a peak detector (PKD_1) at the output of A_{AUX} is used to detect the peak signal strength, thus eliminating the trade-offs associated with a low-pass filter. This peak signal strength is measured on a series of consecutive 1s embedded in the preamble of each burst. As the gain of the auxiliary TIA is independent of the input power, at no time will the peak detector lock to a level stronger than the intended swing (after settling of the AGC loop), thus avoiding the previously mentioned trade-offs regarding the droop rate of the peak detector.

6.3 AUXILLIARY TRANSIMPEDANCE AMPLIFIER

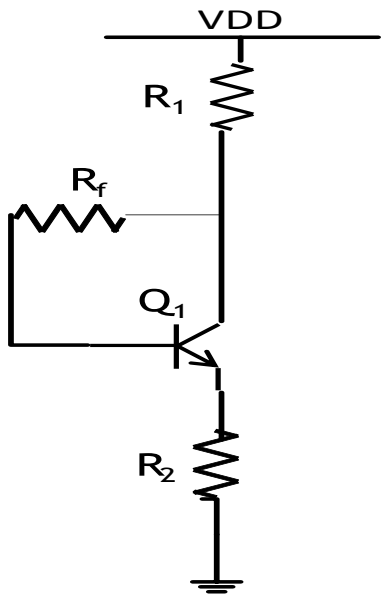


Fig.6.5 Circuit Diagram of Auxiliary TIA

Auxiliary TIA is a standard shunt feedback transimpedance amplifier with emitter degenerated resistor. It bandwidth is determined by equation 6.1

$$f_{3-db} = \frac{A_v}{2\pi R_f(C_{pd}+C_{in})} \qquad (6.1)$$

Where A_v is the open circuit voltage gain of the amplifier, $R_f$is the feedback resistor, $C_{pd}$is the photodiode's junction capacitance and $C_{in}$is the input parasistic capacitance.

As explained above that the Auxiliary TIA is needed to derive the signal strength without getting saturated. To guarantee a linear response across the input dynamic range, the gain of the auxiliary TIA is limited by choosing a relatively low value for its feedback resistor (Rf in Fig. 6.5). While this increases its input-referred noise

current, this is mitigated by the fact that the bandwidth of the auxiliary TIA can be reduced compared to the main TIA. For example, while the main TIA bandwidth must be >7 GHz for 10 Gb/s (non return to zero) operation, the bandwidth of the auxiliary TIA is set by the requirement that its output needs to settle during the 1s at the start of each burst. Here 60 1s (6ns at 10 Gb/s) were used for detecting the peak level. To ensure settling within 5% of the final value (resulting in a 0.2 dB penalty) within 6 ns and assuming a 1^{st} order RC-transfer of the auxiliary TIA, a bandwidth of 80 MHz is required. The final design of the auxiliary TIA had a gain of 530 Ω, a bandwidth of 150 MHz (to improve robustness against process, supply voltage and temperature (PVT) corners) and an input-referred noise current of 135nA_{rms}; more details are provided hereafter. For a weak input burst with an average power of −25dBm a negligible penalty of 0.5dB is incurred due to the noise of this auxiliary TIA.

6.4 PEAK DETECTOR

The peak detector needs to have the following characteristics:

1) Fast “attack” time (time required to acquire a peak), no longer than 10 ns
2) Negligible droop rate
3) Small dc-offsets, below 25 mV

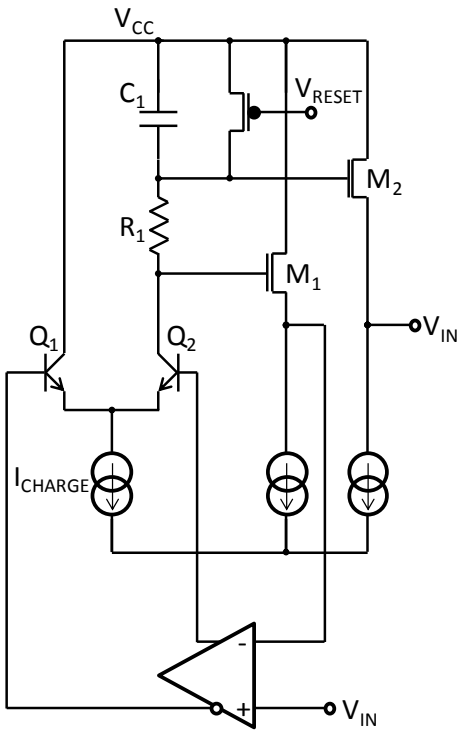


Fig.6.6 Peak Detector

To explain the peak detector operation we consider the circuit in Fig. 6.6 [110]. When the peak detector is released after a reset (i.e. when "V_{reset}" becomes high, and the PMOS switch P_1 is open), V_1 will be higher than V_{in}, and the comparator will switch on transistor Q_2 and steer the current I_{CHARGE} completely to the hold capacitor C_1. This will charge C_1 and V_1 will start to go down. When V_1 crosses V_{in} the comparator switches transistor Q_2 off and switches transistor Q1 on thus steering the charge current to the supply rail. The hold capacitor will hold the acquired peak level until a reset is given to the peak detector. As the comparator cannot instantly switch the current from Q_2 to Q_1 a small offset error will be incurred (See Fig. 6.7).

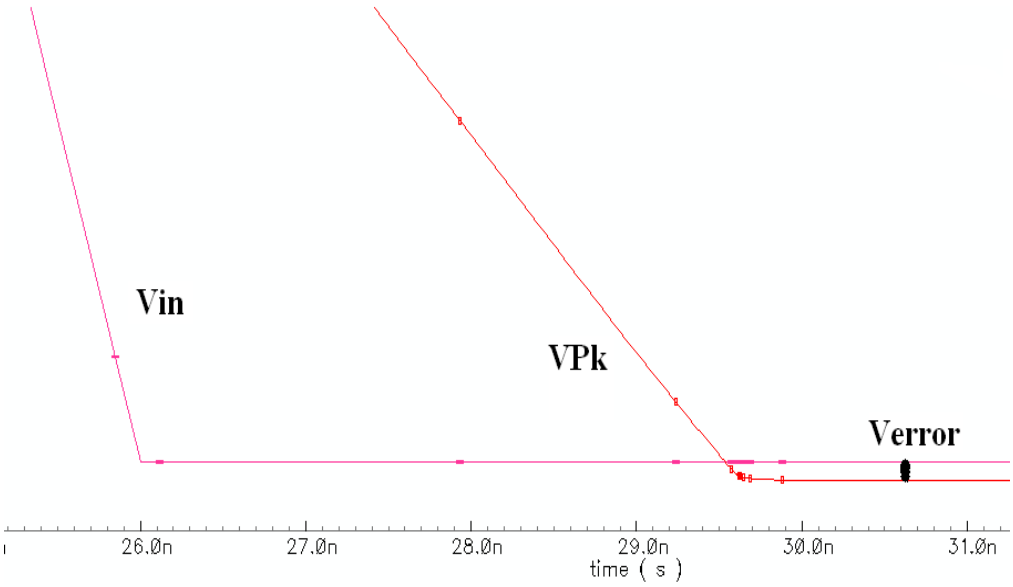


Fig.6.7 Output of Peak detector having small offset error due to delay of comparator (pink trace: peak detector input, red trace: peak detector output).

If the comparator has a delay δt this leads to an offset error V_{error} on the acquired peak level:

$$V_{error} = (I_{CHARGE}/C_1)\,\delta t \qquad (6.2)$$

If a resistor R_1 is placed in series with C_1, the comparator will switch before V_{pk} has reached the minimum level of input signal $V_{in}[110]$. The current is already steered to the supply rail before V_1 reaches the peak level and $V_{pk}=V_{in}$, hence R_1 reduces the error. This error is completely removed with the voltage drop across R_1 is equal to V_{error} (See Fig. 6.8). This leads to a value of R_1

$$R_1 = \delta t/C_1 \qquad (6.3)$$

In a practical implementation however, R_1 needs to be chosen slightly smaller than indicated by equation (6.3) to avoid any oscillations (indeed note that with R1 larger than the value in (6.3), the peak detector becomes an oscillator), and increase robustness against unavoidable process variations.

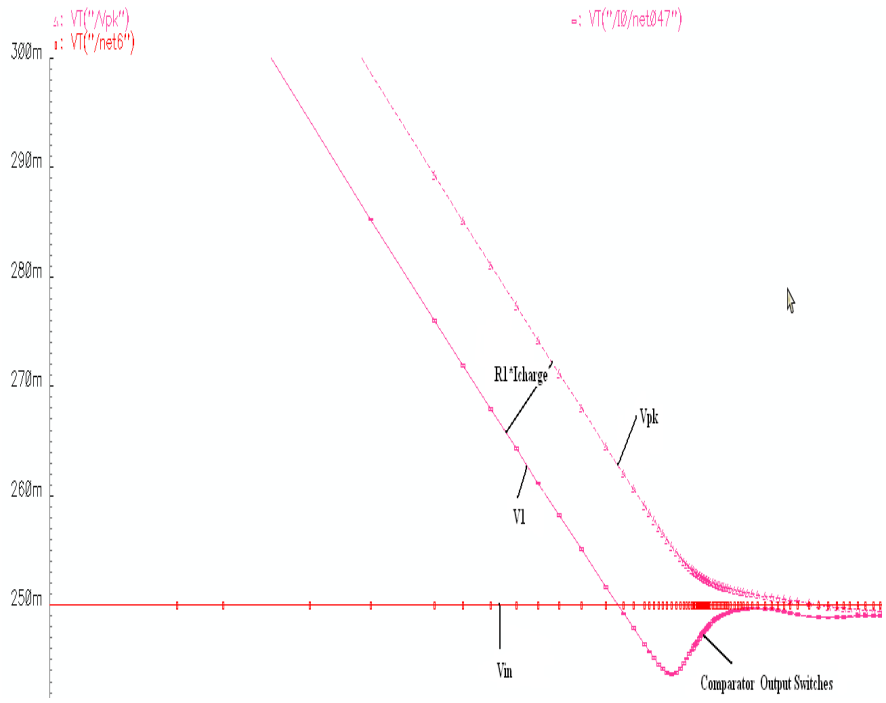


Fig.6.8 Use of R1 to reduce the error

The replica structure M_1-M_2 reduces the feed-through from Vin towards Vpk after the peak has been acquired. The current I_{CHARGE} was chosen as a compromise between speed and power consumption. The larger the charge current I_{CHARGE}, the faster the acquisition of the peak, however also the larger the offset error. Smaller capacitors yields a faster peak detector however the minimum value of hold capacitance C_1 is set by the stray capacitance, and leakage currents. Fig. 6.9 shows the peak detector output and Fig. 6.10 shows the peak detector output integrated with Transimpedance amplifier at various input currents.

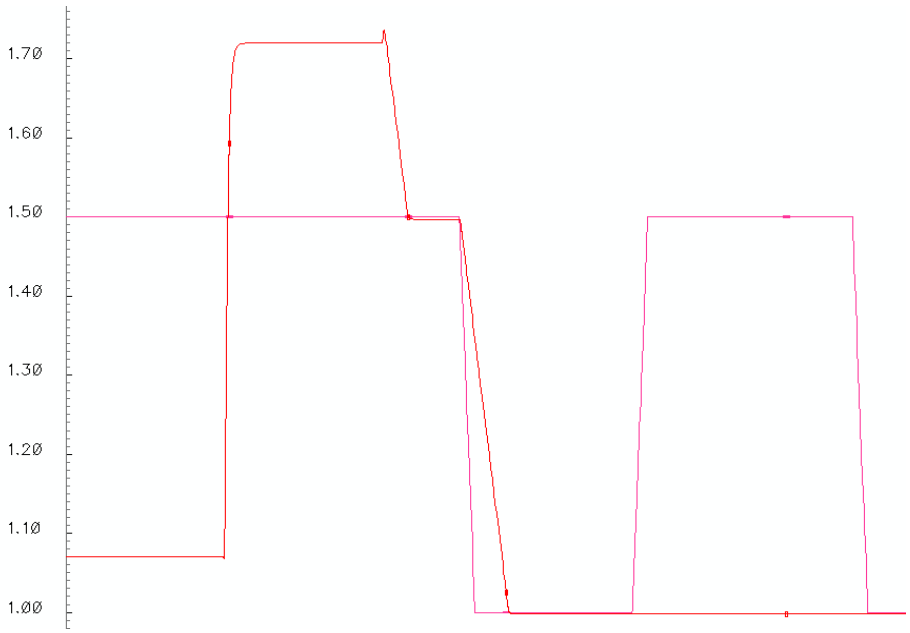


Fig.6.9 Peak Detector Output

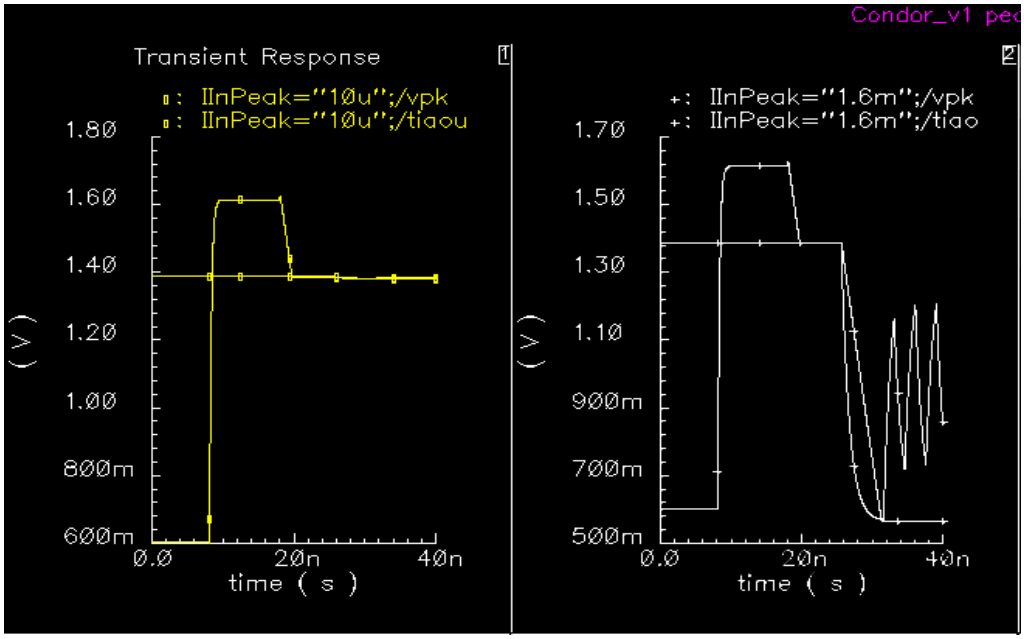


Fig.6.10 PKD output @minimum input current (10uA) and at maximum input current (1.6mA)

6.5 LBMRX MEASUREMENT RESULTS

The LBMRx was designed for a junction temperature range of 0°C to 110°C and a supply variation of +/-5% using a 0.25 mm SiGe:C BiCMOS process (transition frequency f_T of the heterojunction bipolar transistors: 110 GHz).

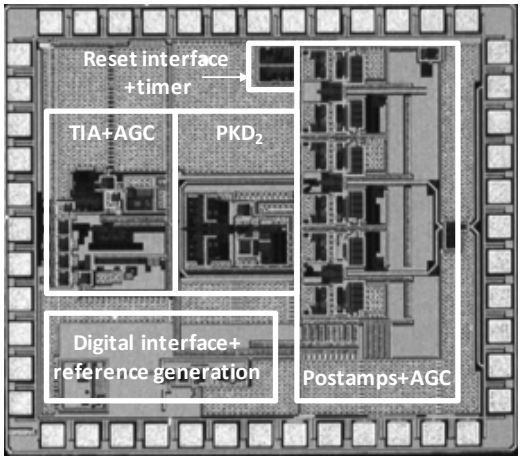


Fig.6.11 Die micrograph (2.4 x 2.1mm^2)

The die (Fig. 6.11) was flip-chipped onto an AlN ceramic substrate. The input was wire bonded to a 10 GHz PIN photodiode (responsivity: ~1A/W, capacitance: ~80fF). The substrate was probed using dc and RF probes; the output of the LBMRx was ac-coupled using 560 pF capacitors.

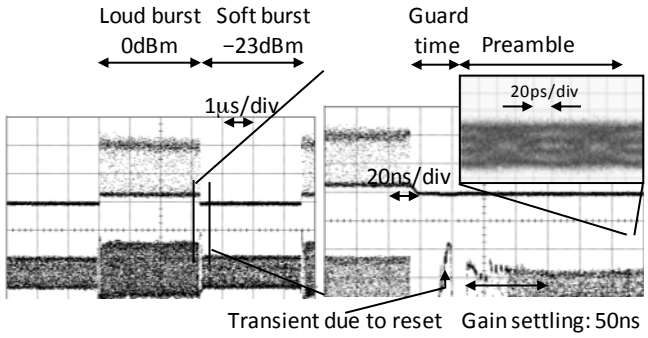


Fig.6.12 Input (upper traces) and output (lower traces) of the LBMRx + eye diagram after preamble (inset).

Fig. 6.12 shows the output of the LBMRx when the input consists of 10 Gb/s loud and soft bursts with ~23 dB dynamic range, generated using an externally modulated 1550 nm laser and semiconductor optical amplifiers. Each burst was 3.27 ms long and consisted of a 150 ns preamble (60 1s, 60 0s, five times 16 1s and 16 0s for gain settling, the remaining part consists of 2^{31}-1 pseudo random bit sequence (PRBS) data for settling of the transient across the coupling capacitors), followed by a 2^{31}-1 PRBS data, on which bit-error rates (BER) were measured. The guard time was 25.6 ns. The close-up shows gain settling within 50 ns. For the largest dynamic range (22.7 dB, see below) the overall settling increases to 150 ns, which is attributed to a transient from the ac-coupling capacitors.

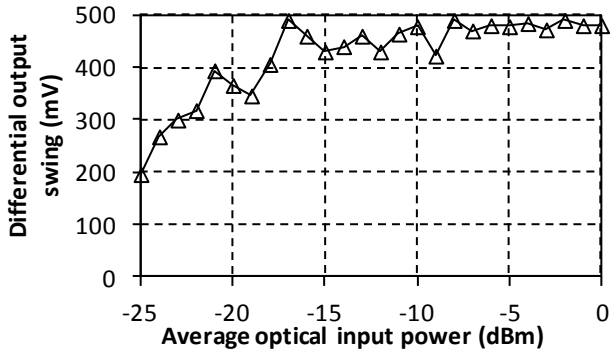


Fig.6.13 Output amplitude vs. average optical input power (dBm).

The output amplitude versus optical power is shown in Fig. 6.13: at least 200mV is achieved, sufficient to interface with EDC chips. To verify the dc-offset compensation of the post-amplifiers, three amplifiers were tested as a function of temperature; calibration was performed at 20°C (Fig. 6.14). The dc-offsets after calibration were always less than 5mV over a temperature ranging from 20°C to 50°C (limited by the setup), confirming correct operation.

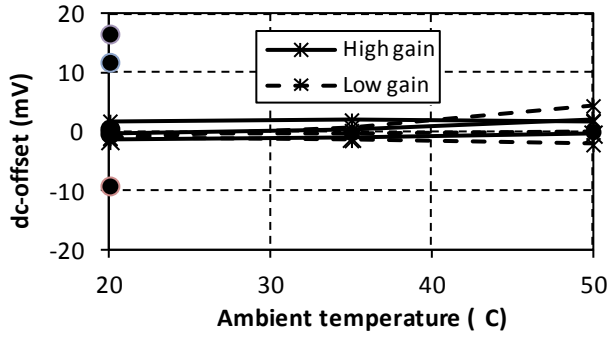


Fig.6.14. dc-offset (difference between both the output phases of the post-amplifiers for zero differential input signal at the output of the post-amplifiers A_{3P},A_{3N}) vs. temperature (dots at 20°C are the dc-offsets before calibration).

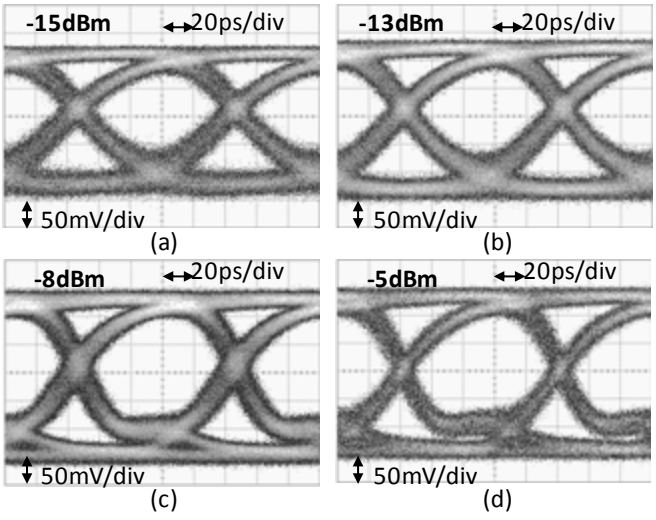


Fig.6.15 Output eye diagrams for various input powers.

Fig. 6.15 shows eye diagrams for various powers: open eyes can be observed, the artefacts in the eyes for −8 dBm and −5 dBm are attributed to a reduction of bandwidth of the PIN photodiode due to an unexpected drop in the PIN photodiode's bias voltage at these powers.

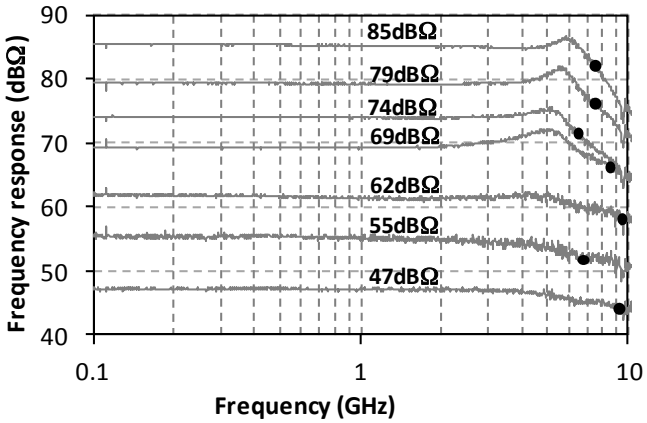


Fig.6.16 Opto-electronic response at various gain settings.

The opto-electric response (S_{21}), measured using a network analyzer is shown in Fig. 6.16. The 3dB bandwidth varies only from 6.8 GHz to 9.8 GHz over a gain ranging from 47 dBW to 85 dBW; limited peaking (4 dB at 69 dBW) can be seen, confirming the operation of the bandwidth control measures in the TIA.

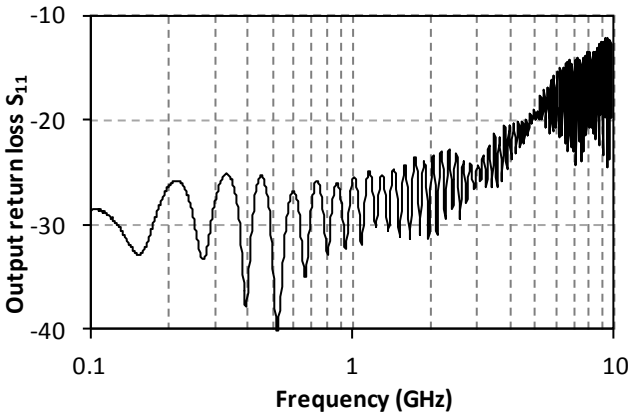


Fig.6.17 Output return loss.

The return loss (including the transmission lines on the ceramic substrate) measured at the output of a single phase is shown in Fig. 6.17: the return loss is better than 10 dB up to 10 GHz.

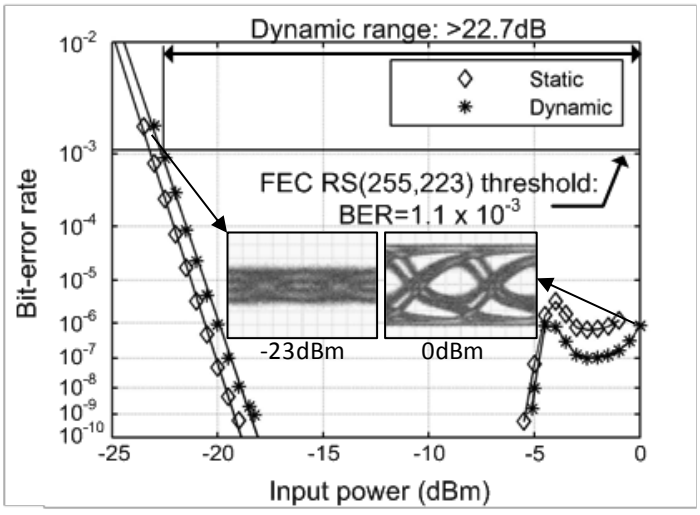


Fig.6.18 Bit-error rate vs. optical input power (insets: eye diagrams, horizontal scale: 20ps/div, vertical: 50mV/div).

The sensitivity and overload were evaluated by measuring the BER on the PRBS portion of the bursts as a function of optical power (Fig. 6.18). A sensitivity of −23.2 dBm was measured at a BER of $1.1x10^{-3}$ (the threshold for Reed-Solomon RS(255,223) forward error correction (FEC)) in the case where all bursts have the same amplitude (static case). When the burst under consideration is preceded by a 0dBm burst (dynamic case), the sensitivity is −22.7 dBm: the 0.5 dB penalty is attributed to a transient from the ac-coupling capacitors. Some bit errors appeared for high powers due to the unexpected drop of the bias voltage of the photodiode, an issue that will be fixed on a new chip. Assuming RS(255,223) FEC, a dynamic range of 22.7 dB can be supported (the maximum power was limited to 0dBm due to experimental limitations). According to accepted practice, THD was measured (Fig. 6.19) for an optical signal whose power was modulated with a 250 MHz sinewave (6 dB extinction ratio) to test linearity. THD less than 5% (comparable to state-of-the-art and compliant with recent industry standards) can be seen up to 0 dBm. For a power of −25 dBm, the harmonics were too weak to be measured and low THD can be assumed.

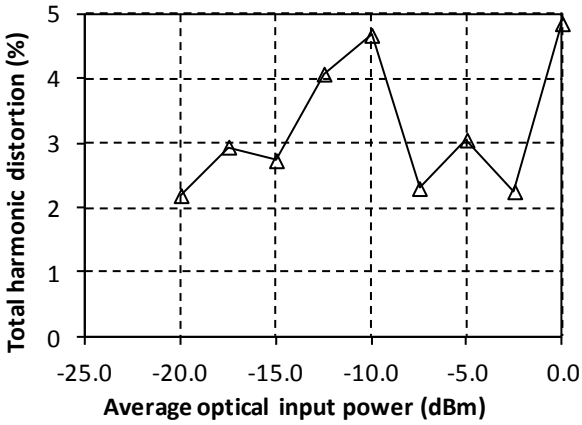


Fig.6.19 Total harmonic distortion vs. optical input power.

These values are somewhat higher than the simulation results which is attributed to distortion from the post-amplifiers. A performance summary is given in Table I. Table II gives a breakdown of the power consumption of the main LBMRx blocks. The AGC power consumption is dominated by the replicas, which can be reduced by scaling the bias currents if required

Table I. Summary of LBMRx performance.

Parameter	Value
Supply voltage	2.5V and 3.3V
Power dissipation	650mW
Die area	2.4 x 2.1 mm^2
Gain	47dBW - 85dBW
3dB bandwidth	6.8GHz – 9.8GHz
Sensitivity (bit-error rate = 1.1 x 10^{-3})	-23.3dBm
Dynamic range	> 22.7dB
Worst-case total harmonic distortion	5%

Table II. Breakdown of power consumption of main LBMRx blocks.

Block	Supply voltage (V)	Power consumption (mW)
Transimpedance amplifier front-end		
High-speed TIA A_1	3.3	32
Replicas A_{1a}, A_{1b}, A_{1c}	3.3	3 x 32
Auxiliary TIA A_{AUX}	3.3	11
Peak detector PKD_1	2.5	5
Opamp OA_1 and OTA G_A	2.5	4
Post-amplifier section		
Peak detectors PKD2,3	2.5	2 x 5
Post-amplifiers $A_{3P,3N}$	3.3	2 x 45
Replica post-amplifier A_{3A}	3.3	45
Opamp OA_2 and G_B	2.5	3

7
CONCLUSIONS AND FUTURE WORK

In this chapter a review of the major findings of this thesis is presented. Some possible Directions for future work are also outlined.

With the ever increasing demand for high information rates and advances in bandwidth intensive applications in the customer oriented applications and in the data centres which supports cloud computing, search engines, etc. the available copper based interconnection technology faces a lot of limitations due to lack of bandwidth, crosstalk in twisted pair cabling and physical space in coaxial based cabling. Due to these issues system integrators and operators are increasingly pushing towards fibre-optics as an alternative. Such optical links make use of short reach interconnects to connect their servers together. Transceivers for these applications achieve up to 100 Gb/s by multiplexing 10x 10 Gb/s or 4x 25 Gb/s channels. Future optical links will be needed which can support 400 Gb/s up to 1 Tb/s with the same footprint and similar power consumption as today's 100 Gb/s solutions. Straightforward scaling of the currently used space or wavelength division multiplexing may be difficult to achieve: indeed a 1 Tb/s transceiver would require integration of 40 VCSELs (vertical cavity surface emitting laser diode, widely used for short-reach optical interconnect), 40 photodiodes and the electronics operating at 25 Gb/s in the same module as today's 100 Gb/s transceiver.

The research discussed in this thesis focussed on developing high speed electronics with lower power consumption, small footprint and better performance with various techniques, such as pre-emphasis employed in rising and falling edges of the signal, bandwidth extensions by inductive peaking and different feedback techniques, which could significantly impact the design of the transceivers used in such systems in the foreseeable future. Apart from that driver and receiver electronics for advanced modulation formats such as PAM-4 (4 level pulse amplitude modulation) were also developed to counter any physical limitations that

one can face while using high speed serial links using NRZ (non- return to zero) modulations due to reliability and packaging issues at such a high serial speed.

I. In *Chapter 3*, pre-emphasis on rising and falling edges was employed to compensate the distortion caused in the VCSEL driver circuits due to large amount of parasitic capacitance and non-linear response of the VCSEL. To compensate for the turn-on delay of the VCSEL diode a pulse-width adjustment block is added which either shortens the pulse or lengthens it based on the requirement to minimize the pulse width distortion in the optical domain. Inductive peaking and local feedback techniques are employed to enhance the bandwidth of the driver. These techniques are implemented a 65nm CMOS. The pre-emphasis achieved an increase of 50% in the vertical eye opening and 40% increased horizontal eye opening.

- ***Future work:*** High serial link bandwidth with the stringent power requirements presents new challenges and opens the door to many possible research directions. One of the fascinating possibilities is to explore advanced modulation formats which will reduce the required bandwidth of the channel, pushing less the bandwidth requirement (which compromises VCSEL reliability) of the VCSEL. In addition, a next-generation deep-sub micron CMOS process (e.g. 28nm, bulk or FD-SOI) can be used to increase the bandwidth of the driver.

II. In *Chapter 4*, the lack of sufficient bandwidth is addressed by using PAM-4 modulation format which reduces the required bandwidth of the channel for a given data bit-rate by half. Further the transmitted binary bits are converted to Gray/thermometer encoded bits to ensure minimum bit error rate. A current mode logic style is used in the encoder which reduces the need for rail to rail swing helping to achieve high bandwith. The most important aspect which we solved in this chapter is the power consumption. By using a single-ended common source based VCSEL driver design we managed to reduce the power consumption of the system to half thus making it suitable to the needs of an optical interconnect transmitter.

- ***Future work:*** To reduce the error while transmitting, the binary bits were converted to thermometer encoded bits, in doing so different current mode logic gates were used. These gates have different delays which causes the different PAM sumbols to arrive at the output at different times. One of the recommended approaches that should be implemented is the use of re-timing flip flops which aligns the PAM symbols. Apart from this eye opening techniques such as emphasis could also be made a part of the system to increase the eye opening.

III. In *Chapter 5*, we have presented the design of an inductor less linear receiver suitable for PAM-4 modulation. The most critical aspect of such a receiver is that it needs to be linear for its entire dynamic range so that the entire PAM symbol constellation is amplified equally. The linearity is achieved by using an Automatic Gain control loop which generates a control voltage to adjust the gain of transimpedance amplifier and the post amplifiers. It has used similar post amplifiers with the same settings thus allowing it to have a robust gain control scheme with repeatable behaviour. To have a small footprint of the receiver, it is designed without any inductive peaking hence no (on-chip) inductors are used in the design.

- ***Future work:*** In terms of optical receiver, the ultimate goal is to have a similar footprint as the ones that are currently used. For the cancellation of the offset voltages originated through the main TIA and dummy TIA and all the post amplifiers external capacitors are used, thus it is imperative that they should be replaced with Gm-C filter type of design. Another aspect that can be further improved in the design is the peak detector to ensure it detects the amplitude of the signals fast and accurate.

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Appendix A

VCSEL rate Equations

The used VCSEL rate equations are:

$$\begin{aligned}\frac{dN}{dt} &= \frac{\eta_i I}{qN_w V_{ACT}} - R(N) - \Gamma v_{gr} G(N,S) S \\ \frac{dS}{dt} &= N_w R_\beta(N) + N_w \Gamma v_{gr} G(N,S) S - \frac{S}{\tau_P}\end{aligned} \tag{1}$$

with N the carrier density, I the driving current and S the normalized photon density $S = S_{TOT}/V_{act}$, S_{TOT} being the photon number. The various parameters are listed in Table 0.1.

Symbol	Description	Unit
η_i	Internal current efficiency	-
N_w	Number of quantum wells	
V_{act}	Volume of a single quantum well	m^3
R(N)	Carrier recombination rate	s^{-1}
G(N,S)	Gain function	-
Γ	Carrier confinement factor	-
v_{gr}	Velocity of light in the cavity	m/s
$R_\beta(N)$	Coupled spontaneous emission	s^{-1}
β	Spontaneous emission factor	-
τ_n	Carrier lifetime	S
τ_p	Photon lifetime	s
λ	Emission wavelength	m

Table 0.1 Rate equation parameters.

The gain function G(N,S) is assumed to have the following form:

$$G(N,S) = \frac{N(t) - N_0}{1 + \varepsilon S(t)} \tag{2}$$

with ε the gain saturation parameter and N_0 the carrier density at transparency. The carrier recombination rate is modelled as:

$$R(N) = \frac{N(t)}{\tau_n} \tag{3}$$

with τ_n the carrier lifetime. Finally, the coupled spontaneous emission is modelled as:

$$R_\beta(N) = \beta \frac{N(t)}{\tau_n} \tag{4}$$

with β the spontaneous emission factor. The VCSEL output power can be derived from the photon density using:

$$P(t) = \frac{V \eta_i h c}{2\Gamma \tau_p \lambda} S(t). \tag{5}$$

Parameter extraction for rate equations

The parameters for the rate equation model can be extracted using the following procedure. First the rate equations are transformed to the following form:

$$\begin{aligned} \frac{dP}{dt} &= \frac{B\tau_n I_{th}(X(t)-1) + \frac{1}{\tau_p}}{1 + \phi B \tau_p \tau_c P(t)} - \frac{P(t)}{\tau_p} + \frac{I_s I_{th} B \tau_n}{\phi} X(t) \\ \frac{dX}{dt} &= \frac{I(t)}{I_{th}\tau_n} - \frac{\phi B \tau_p (X(t)-1) + \frac{\phi}{I_{th}\tau_n}}{1 + \phi B \tau_p \tau_c P(t)} P(t) - \frac{X(t)}{\tau_n} \end{aligned} \tag{6}$$

where X(t) is the relative carrier density:

$$X(t) = \frac{N(t)}{N_{th}} \tag{7}$$

with N_{th} the carrier density that corresponds to the condition where cavity losses and cavity gain exactly balance each other:

$$\Gamma v_{gr} \frac{N_{th} - N_0}{1 + \varepsilon S} = \frac{1}{\tau_p}. \tag{8}$$

I_{th} is the threshold current density:

$$I_{th} = \frac{qN_w V_{act} N_{th}}{\tau_n} \tag{9}$$

and I_s is the spontaneous emission current:

$$I_s = \frac{\beta}{B\tau_n \tau_p}. \tag{10}$$

B and τ_c are given by:

$$B = \frac{\Gamma v_{gr}}{qN_w V_{act}}; \qquad \tau_c = \frac{\varepsilon}{v_{gr}}. \tag{11}$$

The rate equations are now completely defined by seven parameters I_{th}, I_s, B, τ_n, τ_p, τ_c and ϕ. I_{th}, I_s and ϕ can be extracted from the dc-characteristics, which can be obtained from (6) by setting the derivatives equal to zero:

$$(\phi P)^2 - (I - I_{th} - I_s)\phi P - I_s I = 0. \tag{12}$$

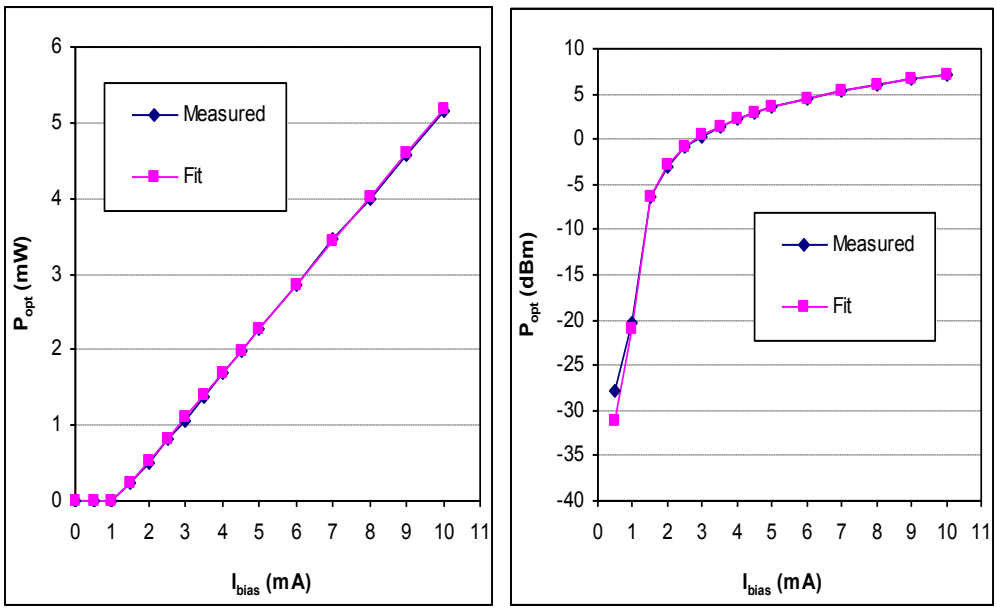

Fig.0.1 Measured and fitted (L,I) curves.

An example of such a fitting is shown in **Error! Reference source not found.**. The extracted values are given in

.

Parameter	Extracted value	Unit
I_s	1.62	µA
I_{th}	1.1	mA
ϕ	1.72	A/W

Table 0.2 – Extracted parameters from (L,I) curves.

The other parameters can be extracted using a frequency substraction method. This method consists of modulating the VCSEL bias with a small signal and measuring

the corresponding frequency response using a photodetector. The intrinsic VCSEL frequency response (i.e. the response obtained if the laser would not exhibit any electrical parasitics) can be shown to have a second-order behavior determined by a relaxation oscillation frequency f_r and a damping rate Γ_d:

$$|H(f)|^2 = \frac{f_r^4}{\left(f^2 - f_r^2\right)^2 + \left(\frac{\Gamma_d}{2\pi}\right)^2 f^2}. \tag{13}$$

While in principle one can directly measure H(f) (as a function of VCSEL bias current) using e.g. a network analyzer, a major problem is the fact that the bandwidth limitations (incurred by the laser parasitics and the photodetector response) reduce the accuracy of this measurement due to limitations in dynamic range of the vector network analyzer. An elegant solution consists of measuring the frequency response for a range of different bias currents. This range should start just above the threshold current of the VCSEL up to some upper boundary over which the VCSEL model should operate correctly. Then, the lowest bias frequency response is subtracted from the other responses. The thus obtained frequency response H'(f) (see (14)) is determined solely by the intrinsic laser response, as indeed the photodetector response and VCSEL parasitics are independent from the VCSEL bias current.

$$|H'(f)|^2 = \frac{f_{r1}^4}{\left(f^2 - f_{r1}^2\right)^2 + \left(\frac{\Gamma_{d1}}{2\pi}\right)^2 f^2} \frac{\left(f^2 - f_{r0}^2\right)^2 + \left(\frac{\Gamma_{d0}}{2\pi}\right)^2 f^2}{f_{r0}^4}. \tag{14}$$

By fitting a number of frequency responses to (14) the resonance frequency and damping factor can be extracted as a function of bias current. The frequency responses can be measured using the setup in Fig.0.2.

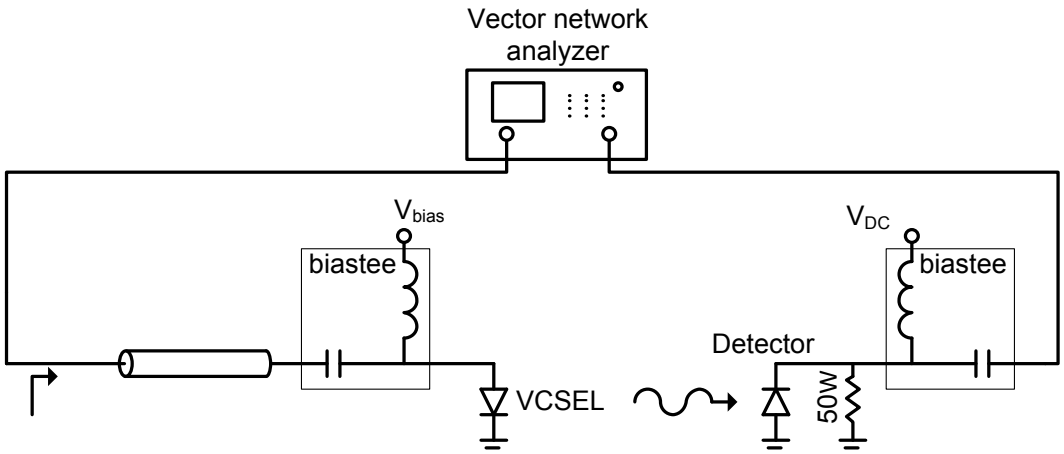

Fig.0.2 Measurement setup for measuring the VCSEL frequency response.

It can be shown that the relaxation oscillation frequency fr is related to the VCSEL bias current by (for sufficiently small bias currents):

$$f_r = \frac{\sqrt{B\left(I_{bias} - I_{th}\right)}}{2\pi}. \tag{15}$$

From (15) one can extract the parameter B. Next, it can be shown that the damping rate Γ_d is given by:

$$\Gamma_d = \frac{1}{\tau_n} + Kf_r^2. \tag{16}$$

with K the so-called universal K-factor:

$$K = 4\pi^2\left(\tau_p + \tau_c\right). \tag{17}$$

By plotting Γ_d as a function of I_{bias} we can extract K and τ_n. Finally, by assuming a value for the photon lifetime from e.g. literature, τ_c can be extracted using (17).