Semiconductor Nanowire Fabrication via Bottom-Up & Top-Down Paradigms

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Declaration

I, Richard George Hobbs, certify that this Thesis is my own work and I have not obtained a degree in this University or elsewhere on the basis of this PhD Thesis.

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Abstract

Semiconductor nanowires are pseudo 1-D structures where the magnitude of the semiconducting material is confined to a length of less than 100 nm in two dimensions. Semiconductor nanowires have a vast range of potential applications, including electronic (logic devices, diodes), photonic (laser, photodetector), biological (sensors, drug delivery), energy (batteries, solar cells, thermoelectric generators), and magnetic (spintronic, memory) devices. Semiconductor nanowires can be fabricated by a range of methods which can be categorised into one of two paradigms, bottom-up or top-down. Bottom-up processes can be defined as those where structures are assembled from their sub-components in an additive fashion. Top-down fabrication strategies use sculpting or etching to carve structures from a larger piece of material in a subtractive fashion. This thesis details a number of novel routes to fabricate semiconductor nanowires by both bottom-up and top-down paradigms. Chapter 3 describes a novel bottom-up route to fabricate Ge nanowires with controlled diameter distributions in the absence of a foreign metal catalyst. The nanowires produced by the method outlined in chapter 3 consist of highly crystalline Ge nanowire cores encapsulated in a shell of amorphous Si-based material derived from the hexakis(trimethylsilyl)digermane precursor compound. Furthermore, the diameter of the Ge nanowire core was found to be related to the nanowire synthesis temperature, and as such the nanowire diameter distribution may be controlled by careful control of the synthesis temperature.

Hydrogen silsesquioxane (HSQ) is a high resolution, negative tone, inorganic electron beam lithography (EBL) resist which is capable of producing features with

sub-10 nm dimensions on Si substrates. However, the use of HSQ to pattern non-Si based materials is less well developed. Chapter 4 outlines the importance of surface chemistry in high-resolution EBL using HSQ to fabricate arrays of Ge and Bi_2Se_3 nanowires. Finally, Chapter 5 describes the use of a high-resolution EBL process to produce arrays of Si nanowires from silicon-on-insulator (SOI) substrates. Additionally, chapter 5 details a process to create templates for the directed self-assembly of a diblock copolymer, in this case polystyrene-*b*-polydimethylsiloxane. Directed self-assembly of diblock copolymers is of interest for advanced lithography applications, whereby pattern multiplication can be achieved within sparsely patterned templates by directed self-assembly of suitable diblock copolymers.

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Dedicated to my parents

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Chapter 1

Introduction

"....whoever could make two ears of corn, or two blades of grass, to grow upon a spot of ground where only one grew before, would deserve better of mankind, and do more essential service to his country, than the whole race of politicians put together."

Jonathan Swift, Gulliver's Travels, 1726.

1.1. Semiconductor Nanowires

Semiconductor nanowires are pseudo 1-D structures where the magnitude of the semiconducting material is confined to a length of less than 100 nm in two dimensions. Semiconductor nanowires have a vast range of potential applications[1], including electronic (logic devices, diodes)[2], photonic (laser, photodetector)[3–5], biological (sensors, drug delivery)[6], energy (batteries, solar cells, thermoelectric generators)[7,8], and magnetic (spintronic, memory)[9–11] devices. Semiconductor nanowires can be fabricated by a range of methods which can be categorised into one of two paradigms, bottom-up or top-down. Bottom-up processes can be defined as those where structures are assembled from their sub-components in an additive fashion. Top-down fabrication strategies use sculpting or etching to carve structures from a larger piece of material in a subtractive fashion. The challenge of continuous microelectronic device scaling to meet industry targets, *e.g.* 'Moore's Law'[12], and the diversification of the microelectronics industry into new materials for specialised applications ('More than Moore')[12], has motivated research in semiconductor

nanowires for the past number of decades. The massive competition for a share of the global 304 billion USD semiconductor market[13], has driven the expansion of the semiconductor nanowire research area, resulting in the evolution of, new fabrication techniques, innovative processes, new materials and creative advancements in semiconductor nanowire device design.

This chapter aims to summarise and compartmentalise the various approaches taken by both the bottom-up and top-down paradigms in this field, whilst identifying potential spaces in which both top-down and bottom-up approaches may be used in tandem. Primarily, this chapter will focus on Si and promising high charge carrier mobility materials for logic device applications, although other noteworthy applications of semiconductor nanowires and nanoribbons for other applications will be discussed.

Firstly, the major fabrication routes to production of semiconductor nanowires in both paradigms will be discussed, whilst identifying recent advances and highlighting the benefits and drawbacks of these routes. The synergistic use of both top-down and bottom-up approaches to produce structures unattainable by either route alone will also be considered. Next, the most promising materials for high mobility logic device fabrication will be considered. The current issues with processing these materials within each fabrication paradigm will also be addressed. Lastly, the application of semiconductor nanowires in the field of thermoelectric materials will be discussed with respect to their use in energy recovery applications.

1.2. Bottom-Up Semiconductor Nanowire Fabrication

1.2.1. Semiconductor Nanowire Growth Methods

Numerous routes exist to the bottom-up fabrication of semiconductor nanowires. The vapour-liquid-solid (VLS) mechanism and analogues thereof, is the most commonly used route to semiconductor nanowire production.[14,15,1] The VLS mechanism relies on a vapour phase precursor of the nanowire material which impinges on a liquid phase seed particle, from which unidirectional nanowire growth proceeds. The choice of an appropriate seed material has the benefit of allowing control over the diameter of the nanowires produced, whilst the seed material can also significantly affect the crystalline quality of the nanowire.[16,17] At this point, the importance of selection of an appropriate precursor material should be highlighted. Within a given precursor, MR_x, where 'M' represents the semiconductor element, or elemental component of a compound semiconductor, and 'R', represents a protecting group, the M-R bond should be sufficiently labile under nanowire synthesis conditions to liberate reactive M species for nanowire growth. Furthermore, the R group liberated upon precursor decomposition should ideally exist as a gas phase species to prevent contamination of the nanowire product with liquid or solid phase by-product. Consequently, metal hydrides are often used as precursor compounds for nanowire growth, as H_2 gas is an especially clean by-product which has the benefit of inhibiting undesirable oxide formation for non-oxide semiconductor nanowire growth. Metal hydride precursors are commonly used in the growth of nanowires by chemical vapour deposition (CVD), given that metal hydrides such as SiH_4 and GeH_4 generally exist as gas phase compounds[18]. Metal-organic precursors, such as diphenylsilane and diphenylgermane, often used in solution phase and supercritical fluid phase nanowire synthesis can produce carbonaceous by-products

which may be difficult to completely separate from the nanowire product.[19,20] Semiconductor nanowire synthesis conditions often encourage the formation of reactive radical species which can initiate polymerisation reactions resulting in unwanted contaminating by-products,[21] and as such, precursor design should always be considered when designing an experiment for semiconductor nanowire synthesis. Analogues of the VLS mechanism include supercritical fluid-liquid-solid (SFLS)[15], solution-liquid-solid (SLS)[22], vapour-solid-solid (VSS)[23,24] and oxide assisted growth (OAG)[25] mechanisms. Common to all of these analogues is the existence of a collector or seed particle which acts as a sink for the nanowire material, and from which unidirectional growth proceeds.[26] Conventionally, the seed particle is a metal with which the nanowire material or component thereof forms an alloy. However, autocatalytic or self-seeded semiconductor growth has also been demonstrated.[27–33] Self-seeded VLS-type nanowire growth is most commonly observed for compound materials such as InP, GaN and SnO_2 whereby the metallic component of the material, In, Ga and Sn for InP, GaN and SnO_2 respectively, forms seed particles for nanowire growth of the compound material.[33,32,34] However, there have also been reports of self-seeded nanowire growth for elemental materials where a VLS-type mechanism has been invoked.[35] Chapter 3 of this thesis discusses a novel mechanism of Ge nanowire growth in the absence of a metal seed catalyst particle. The most commonly used metal catalyst for VLS-type nanowire growth is Au, prepared either as colloidal Au nanoparticles or as an evaporated or sputtered thin film. However, Au is inherently incompatible with semiconductor device manufacturing. Au has a high diffusivity in Si and also acts as a deep level acceptor and thus has detrimental effects on device performance.[36–38] Furthermore, Au is a highly inert material which makes cleaning of instrumentation contaminated with Au

extremely difficult. For example, traditional Au etchants include aqua regia (concentrated nitric acid and hydrochloric acid solution), KI/I_2 solution and alkali cyanide solutions, all of which would corrode stainless steel equipment and in the case of alkali solutions result in detrimental effects on semiconductor device performance, such as shifting of threshold voltage (V_t).[39,40] Consequently, there has been significant research into alternative, complementary metal-oxide-semiconductor (CMOS) production compatible, metal seeds for catalysed VLS semiconductor nanowire growth.[41–43] Acceptable metals should have ionisation energies far from the mid band-gap region of the semiconductor material. Si nanowire growth has been demonstrated using a number of Si CMOS compatible metals including Bi[22] and Al.[44]

One benefit of bottom-up nanowire growth over top-down processing is that nanowires grown by bottom-up methods may be doped in-situ during crystal growth by incorporating dopant precursors in the nanowire synthesis procedure. Consequently, bottom-up grown nanowires may not require destructive techniques such as ion implanting to generate additional charge carriers. Ion implanting can destroy atomic ordering in the implanted region of the semiconductor crystal and requires subsequent thermal annealing steps to restore crystal ordering.[45]

In addition to VLS-type nanowire growth mechanisms there exists a range of other routes to produce bottom-up grown nanowires. These routes include, oriented attachment,[46,47] metal organic vapour phase epitaxy (MOVPE),[48,49] molecular beam epitaxy (MBE),[50] soft templating,[51–53] dislocation driven unidirectional growth[29] and crystal habit modification.[54–56]

1.2.2. Nanowire Alignment Techniques

Bottom-up grown semiconductor nanowires fabricated by the methods outlined above are typically produced as entangled meshes of nanowires and as a result lack the periodic ordering and placement required for large-scale semiconductor device processing. Figure 1.1 displays an SEM image of an entangled mesh of SiO_2-coated Ge nanowires.

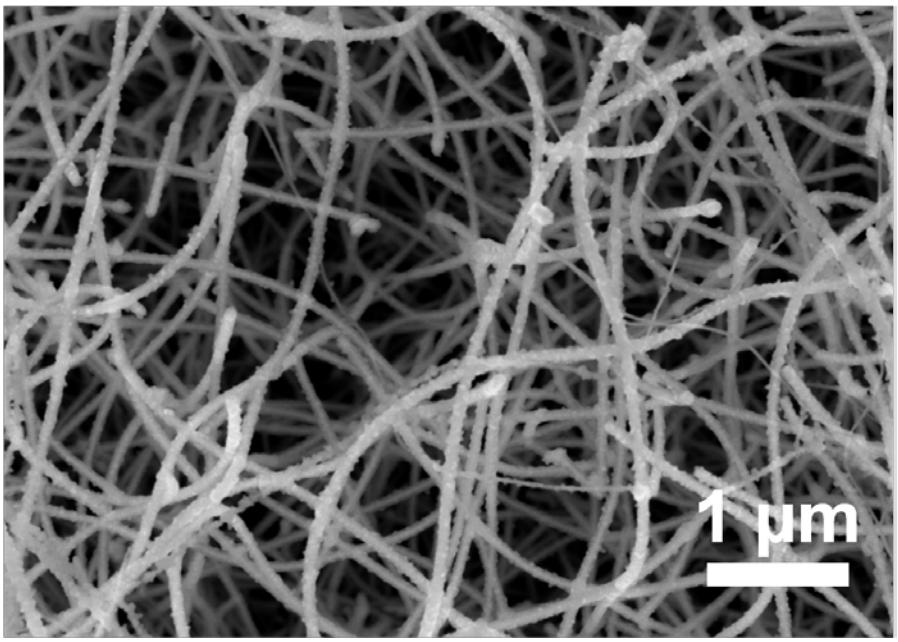

Figure 1.1. An SEM image of an entangled mesh of SiO_2-coated Ge nanowires grown from colloidal Au nanoparticles by the SFLS method.

Recently there have been a number of techniques developed to align semiconductor nanowires produced as entangled meshes. Examples include alignment of polar nanowires within strong electric fields,[57,58] dielectrophoresis,[59,60] microfluidic alignment,[61] lubricant assisted contact printing,[62–64] and evaporation-induced alignment.[65–67] Electric field-based alignment techniques, including dielectrophoresis, have been shown to allow precise control over nanowire position with respect to metallic contact pads, however, these techniques have not yet

demonstrated the high density of aligned nanowires required for high volume manufacturing (HVM), which is currently approaching a device half-pitch of 20 nm.[12] Figure 1.2 displays images of nanowires aligned by dielectrophoresis at a pitch of ~ 20 µm.

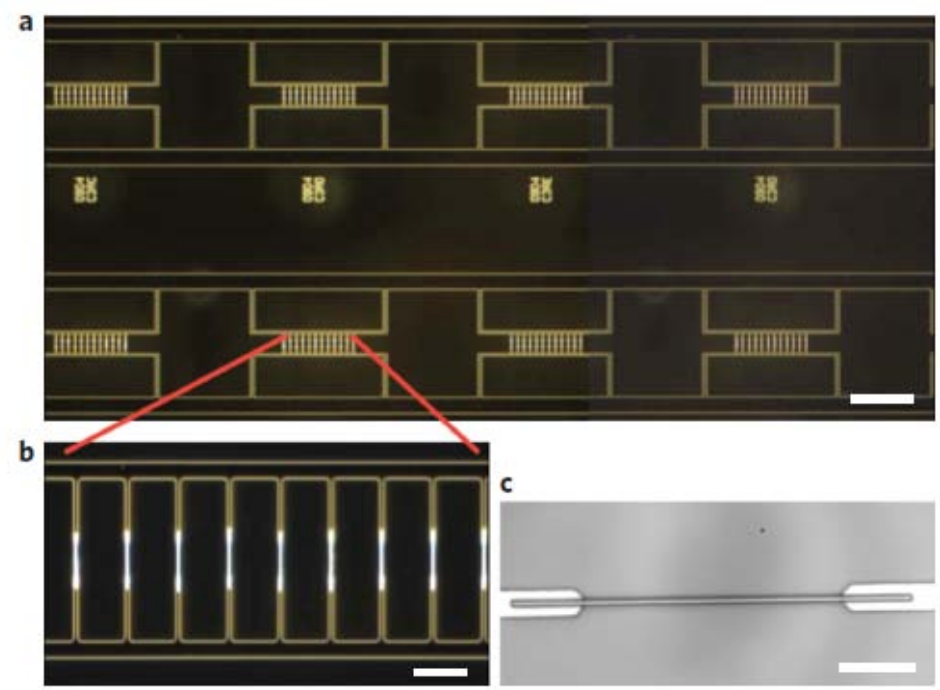

Figure 1.2. Optical dark-field and DUV images of nanowires assembled onto electrodes by dielectrophoresis: (a) dark-field image of defect-free nanowire assembly arranged on electrode arrays (scale bar = 200 µm), (b) high magnification dark-field image of nanowires aligned on 2 µm wide electrodes (scale bar = 20 µm) and (c) DUV image of a single nanowire aligned on electrodes separated by 12 µm (scale bar = 4 µm).[60]

Microfluidic alignment, contact printing and evaporation induced alignment techniques have all demonstrated the capability to create parallel nanowire arrays, in some cases with high areal density. Fan *et al.*, for example, have demonstrated aligned nanowires at a density of ~ 10 nanowires/µm.[62] However, these techniques

lack the prerequisite precision of control over nanowire placement, required for individual nanowire addressability within very large scale integrated circuit (VLSI) technology. Nevertheless, such techniques have been used not only to demonstrate successful individual device operation, but, also to demonstrate integrated devices in a fully functioning nano-processor.[63]

A change of direction may be required for bottom-up approaches to achieve the requisite nanowire density, placement control and alignment required for VLSI manufacturing. High density vertical semiconductor nanowire films have been produced using a range of bottom-up techniques. These techniques include, epitaxial nanowire growth,[68–70,16,71–73,44,49] and hard-templated nanowire growth.[74,75] Figure 1.3 shows an SEM image of vertically aligned epitaxially grown nanowires, where the diameter was controlled by an anodised aluminium oxide (AAO) template.

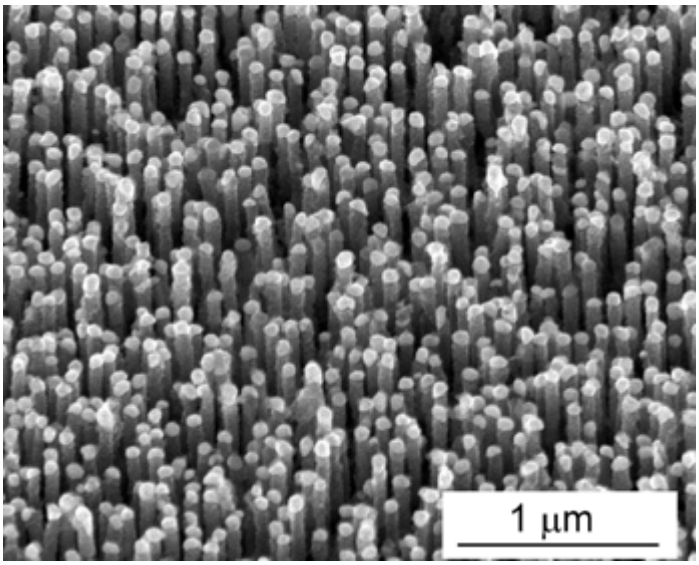

Figure 1.3. SEM image of epitaxial vertical Si nanowire arrays grown within an AAO hard template (template removed in image). Nanowire crystal orientation is controlled epitaxially by the substrate, whilst diameter and placement of the nanowires is controlled by the template.[74]

The epitaxial route to semiconductor nanowire synthesis has the advantage of controlling nanowire crystal orientation through the selection of an appropriate substrate crystal orientation. Wang *et al.* for example, have demonstrated the epitaxial growth of vertically aligned <111> oriented Si nanowires on a <111> Si substrate by CVD using an Al catalyst. Nanowires can also be produced epitaxially when there is a large lattice mismatch between the nanowire material and the substrate material. Tomioka *et al.* reported the growth of <111> oriented InAs nanowires on a Si <111> substrate, despite an 11.6 % lattice mismatch between the two crystals, by using a selective area MOVPE technique whereby lattice mismatch strain was dissipated by limiting the interfacial area between the two crystals.[49] Shimizu *et al.* have shown that the combined use of epitaxial nanowire growth and an ordered template such as AAO to control the position of these nanowires, allows a route to ordered arrays of vertically aligned, coaxial, Si nanowires suitable for use in vertical nanowire device fabrication (figure 1.3).[74] Ordering of pores in AAO spontaneously occurs during AAO formation as a mechanism to reduce internal strain in the AAO film.[76] The formation of AAO with hexagonally close packed (HCP) pores can be considered a bottom-up process, as the pores self-assemble into a HCP arrangement from an initial disordered state, pore by pore.[76]

1.2.3. Vertical Nanowire Field Effect Transistors

There have been several reports of field effect transistor (FET) devices produced using vertically aligned, bottom-up grown semiconductor nanowires.[77–84] Figure 1.4 shows electron microscopy images of vertical Si nanowires used to create vertical nanowire FET devices.

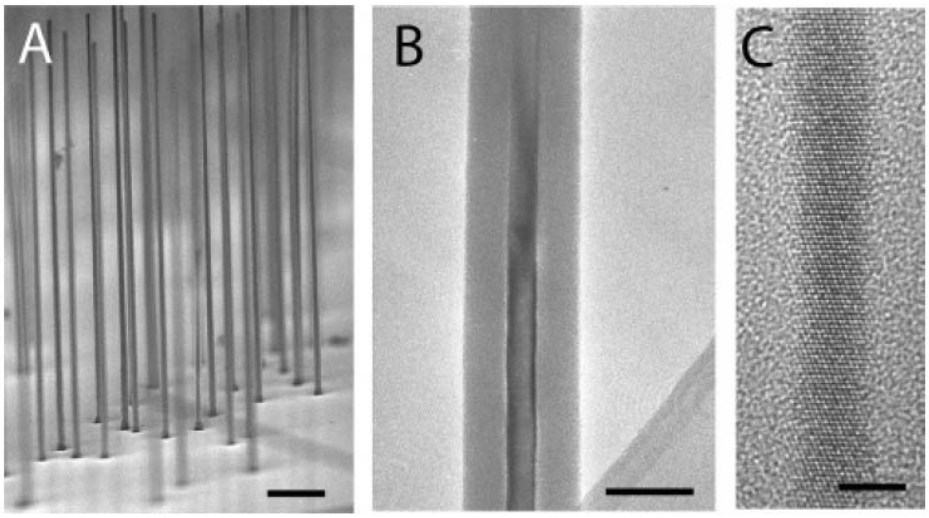

Figure 1.4. Vertically aligned, epitaxial, Au seeded, Si nanowires with thermally grown SiO_2 shells. Scale bars represent lengths of 1 µm, 75 nm and 4 nm in (a), (b) and (c) respectively.[83]

The reported devices showed reasonable performance characteristics with observed I_{ON}/I_{OFF} ratios > 10^5 and a sub-threshold slope of 120 mV/decade, although their performance was still significantly poorer than current state-of-the-art, top-down, strained Si devices.[85] The vertical nanowire devices demonstrated significantly lower on/off ratios and shallower sub-threshold slopes than their top-down counterparts. The reasons for their inferior performance can be attributed to a number of issues including, contact resistance at the source and drain interfaces, non-uniform dopant distribution within the nanowire channel, charge trapping at the gate dielectric interface, or charge carrier recombination due to Au incorporation within Au-seeded Si nanowires. Some of these issues may be rectified, for example, the choice of an appropriate seed metal for nanowire growth is important. Not only should the seed metal allow production of the desired nanowire structure, the metal should also have an appropriate work function to form an ohmic contact to the semiconductor nanowire.[86,87] Au tends to form Schottky contacts to n-Si resulting in

high contact resistance to the semiconductor nanowire channel.[88] The choice of metal also depends strongly on the majority charge carrier and carrier concentration in the nanowire device, for example p-type devices require metals with increased work function values compared to n-type devices, and higher semiconductor charge carrier concentrations result in reduced depletion layer widths at the metal-semiconductor junction which facilitates carrier tunnelling and thus reduced contact resistance.[88] Alternatively, the option exists to use a seed metal which has an inappropriate work function to produce the nanowires and subsequently strip this metal away by chemical etching, followed by the deposition of a suitable electrical contact metal. However, this approach introduces additional device processing steps and complete removal of the seed metal after chemical etching is unlikely, especially when alloys may have formed with the semiconductor during nanowire growth. The issue of dopant distribution is critical to device performance. A homogeneous, activated dopant distribution is desired within semiconductor devices in order to assure a stable threshold voltage (V_t).[89] Perea *et al.* have mapped the dopant distribution within an individual VLS grown Ge nanowire, and have shown the dopant distribution to be non-uniform along the nanowire growth axis and radially across the nanowire.[90] Techniques such as single ion implantation have been shown to improve the homogeneity of dopant incorporation in the nanowire structure resulting in improved V_t stability from device to device.[89] A number of approaches have been taken to improve semiconductor nanowire surface passivation to remove surface state charge trapping sites, which can have capacitive effects at the nanowire surface and hinder device performance. These approaches include organic passivation of the nanowire surface,[91] dielectric deposition of materials such as SiO_2, and Al_2O_3 and nitridation or sulfidation of the nanowire surface.[92,93] Finally, issues

arising due to metal dopants from the catalyst metal particle can be negated through the use of an appropriate metal for the semiconductor of choice. The metal should not have ionisation energies at or near the centre of the band-gap of the semiconductor. For example, Al and Bi seeds would be compatible with Si nanowire production for FET applications as both have ionisation energies near the centre of the band-gap of Si. Once the outstanding issues detailed above have been addressed, bottom-up grown vertical nanowire FETs may become a practical route toward continued device footprint scaling within VLSI technology.

1.2.4. Bottom-Up Semiconductor Nanowire Outlook

There are a number of outstanding issues associated with the integration of bottom-up grown semiconductor nanowires into conventional integrated circuit (IC) design and processing. Conventional IC design is based on the active channel of the logic devices lying coplanar to the Si wafer substrate, and requires a very high degree of control over placement of the devices so that they may be individually addressed for successful IC operation. Traditionally, bottom-up grown semiconductor nanowires are grown as entangled meshes and consequently lack the prerequisite ordering, and control of placement required for IC manufacturing.[15,27,94] Although there have been recent advances in extracting nanowires from such entangled meshes and aligning them on substrates, these approaches can produce neither the high density of nanowires desired, nor the large scale areal coverage required, for HVM.[60,59,63,58,95,65,61] As such, industrial applications of entangled meshes of semiconductor nanowires may be limited to the production of nanowire composites, which may have applications in areas such as batteries, flexible electrodes and thermoelectric generators.[96–98] However, there still remains significant value to be

gained from the study of individual, novel, nanoscale structures, from a conceptual standpoint. Given the issues associated with the alignment of bottom-up grown semiconductor nanowires in the substrate coplanar orientation, it seems imperative that another route to IC fabrication be devised. Perhaps the most promising route toward integration of bottom-up grown semiconductor nanowires into an IC compatible arrangement is that of a vertically oriented active channel with respect to the substrate. Transferring to a vertical orientation would be a huge change for a very mature technology. However, recent developments in the industry with the adoption of tri-gate and finFET structures have shown that movement out of the plane of the Si substrate is possible and as such presents an opportunity for the development of 3-D device architectures. Advances in CVD techniques for nanowire growth have allowed the production of epitaxial nanowires whereby the crystalline orientation of the nanowires with respect to a substrate is controlled at the epitaxial interface. Operational vertically integrated nanowire field effect transistors (VINFETs), produced using bottom-up grown semiconductor nanowires have been reported by several groups.[80,99,83,84] The VINFET concept remains a viable option for future semiconductor device processing as it potentially offers a route to high density stacks of gate all-around (GAA) nanowire FET devices. The vertical orientation with respect to the substrate allows devices to be stacked on the substrate which ultimately increases the density of devices and thus computing power per chip area. A wrap around gate or GAA structure also offers superior electrostatic control of the channel compared to current devices in production, which may allow improved switching of the device. However, a great amount of work is still required to individually contact each device within such a high density, stacked architecture and consequently IC fabrication using VINFET devices is still in its infancy.

Furthermore, the International Technology Roadmap for Semiconductors (ITRS) has targeted a line width roughness (LWR) value of 1.4 nm 3σ for device structures by 2015.[12] LWR values in the targeted range are not yet achievable in semiconductor nanowire fabrication by bottom-up means, where typical variation in nanowire diameter values are ~3 nm 3σ.[100,101] Consequently, further work is required in the areas of alloy engineering and nanowire catalyst control to achieve the targeted control of nanowire diameter for device components in future VLSI manufacturing.

1.3. Top-Down Semiconductor Nanowire Fabrication

1.3.1. Optical Lithography

Optical lithography has been the industry standard for semiconductor device definition and placement for decades. In that time there have been significant developments in optical lithography, both in terms of resist technology and optics.[102–105] There has been a general trend toward shorter wavelength radiation sources to achieve higher image resolution as given by the relationship in equation 1.1 derived from the Rayleigh criterion.[105]

$$CD = \frac{k\lambda}{NA} \tag{1.1}$$

CD represents the minimum critical dimension that can be imaged in a photoresist using a given process having a process latitude factor of *k*, an emission wavelength λ (nm), and a numerical aperture *NA*, where $NA = n\sin\theta$, where *n* represents the refractive index of the medium in which the final projection lens is operating and θ represents the half-angle of the maximum cone of light that exits the final lens of the system. In the 1970s, Hg G-line emission, at a wavelength of 436 nm, was the light-source of choice for optical lithography. Current VLSI manufacturing employs an

ArF laser with an emission wavelength of 193 nm. In addition to reducing the wavelength of the radiation source, other measures have also been taken to improve image resolution. DUV scanners and steppers regularly incorporate a reduction lens as the final projection lens of the lithography system. Reduction lenses typically allow 4 × or 5 × reduction of features in the photomask.[104] The use of reduction lenses in scanners and steppers results in a consequent scaling of the image field, which translates as an increase in the number of exposure fields per wafer and thus a lower throughput of wafers. Consequently, 2 × reduction lenses are often used as a compromise between reduced critical dimension (*CD*) and wafer throughput. Although reduction lenses do not increase the resolution of the lithography process, they can be used to scale larger features in the photomask to a fraction of that size in the image projected on the photoresist. This scaling reduces some of the demands placed on mask manufacturing, as low density larger features are typically produced with fewer defects than high density, smaller features in mask fabrication. Interference lithography can be used to create arrays of features with *CD* values a fraction of the wavelength of the radiation source.[106–108,104] Interference lithography requires a number of coherent beams of radiation to be focused on a spot to create an interference pattern, where the period of the pattern is a fraction of the initial radiation wavelength. Typically interference lithography is only used to produce arrays of structures such as gratings. Immersion lithography is a technique whereby the final projection lens of the radiation source is immersed in a medium with a higher refractive index than air, *e.g.* water 1.436 at 193 nm. Increasing the refractive index of the medium in which the final lens operates, effectively increases the *NA* value of the system and as such reduces the minimum *CD* of features that can be imaged in the photoresist.[104] Media with higher refractive indices than water are also

being investigated to further increase the process resolution.[104] The '*k*-factor' or process latitude factor given in equation 1.1, is a broad term which depends on a number of process dependant parameters. The '*k*-factor' accounts for photoresist effects, developer effects and reticle (photomask) effects, amongst others, and as such is a difficult term to predict for a new process. In essence, a high '*k*' value is representative of a lower resolution process, where process parameters limit the achievable resolution. Typical '*k*' values can be as low as 0.15, thus allowing features with dimensions a fraction of the wavelength of the incident light, to be imaged in the photoresist.[109,104] Techniques that can be used to reduce '*k*' values include the use of high resolution resists and resist trimming processes, as shown in figure 1.5.

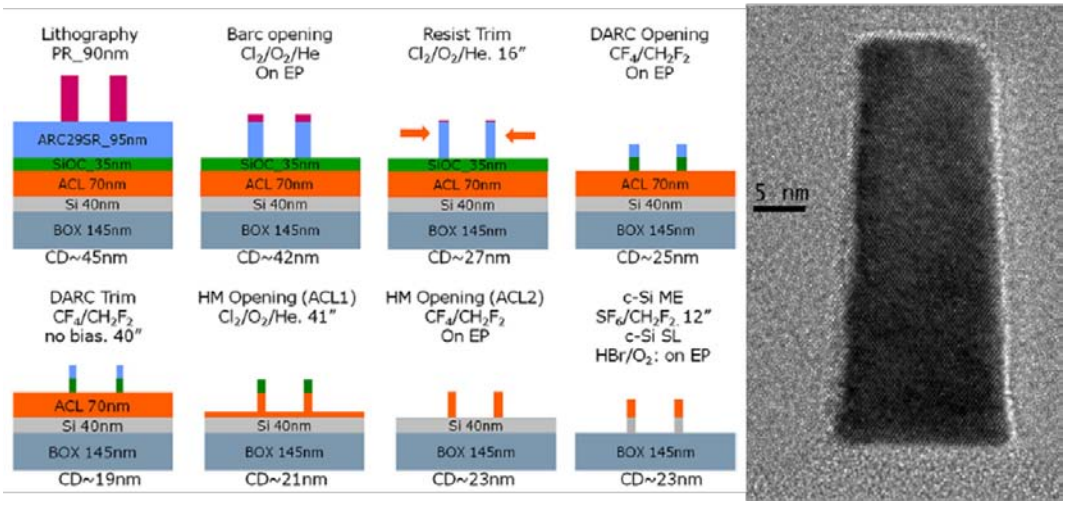

Figure 1.5. (Left) Schematic representation of a process flow used to trim photoresist features to achieve reduced critical dimensions in Si features. (Right) TEM image of a cross-section of a 10 nm × 40 nm Si nanowire produced from SOI using a 193 nm immersion lithography process incorporating resist trimming steps and overetching.[110]

However, even with such low '*k*' values, achieving the high feature densities desired for current semiconductor device production requires further process developments such as, optical proximity correction (OPC), phase shift masks (PSM),[111] and double patterning (figure 1.6).[112,110] Ultimately continued device scaling and increased device density may require extreme ultra-violet (EUV) or x-ray lithography (XRL) due to the dramatically reduced wavelengths of these techniques, typically 13.5 nm for EUV and < 1 nm for XRL, compared to current UV lithography techniques. Whilst short wavelength techniques like EUV and XRL offer significant potential for nanolithography, they do have drawbacks. EUV lithography tools have to operate in vacuum due to strong EUV absorption by air. Consequently, EUV resists should not be volatile or swell or under vacuum.[113] Additionally, the requirement for loading and unloading wafers from vacuum chambers puts significant time demands on the process. Furthermore, shot noise, proximity effects and flare issues remain outstanding, all of which will hinder the ultimate resolution of the lithography process. XRL too has a number of issues which may prove to be prohibitive for HVM. XRL requires synchrotron radiation sources which may prove to be too large an investment for an unproven manufacturing process with considerable associated risk. However, XRL does not demonstrate the significant, detrimental, radiation-material interactions observed for EUV and as such it remains a pursued and viable option for further technological development.[105]

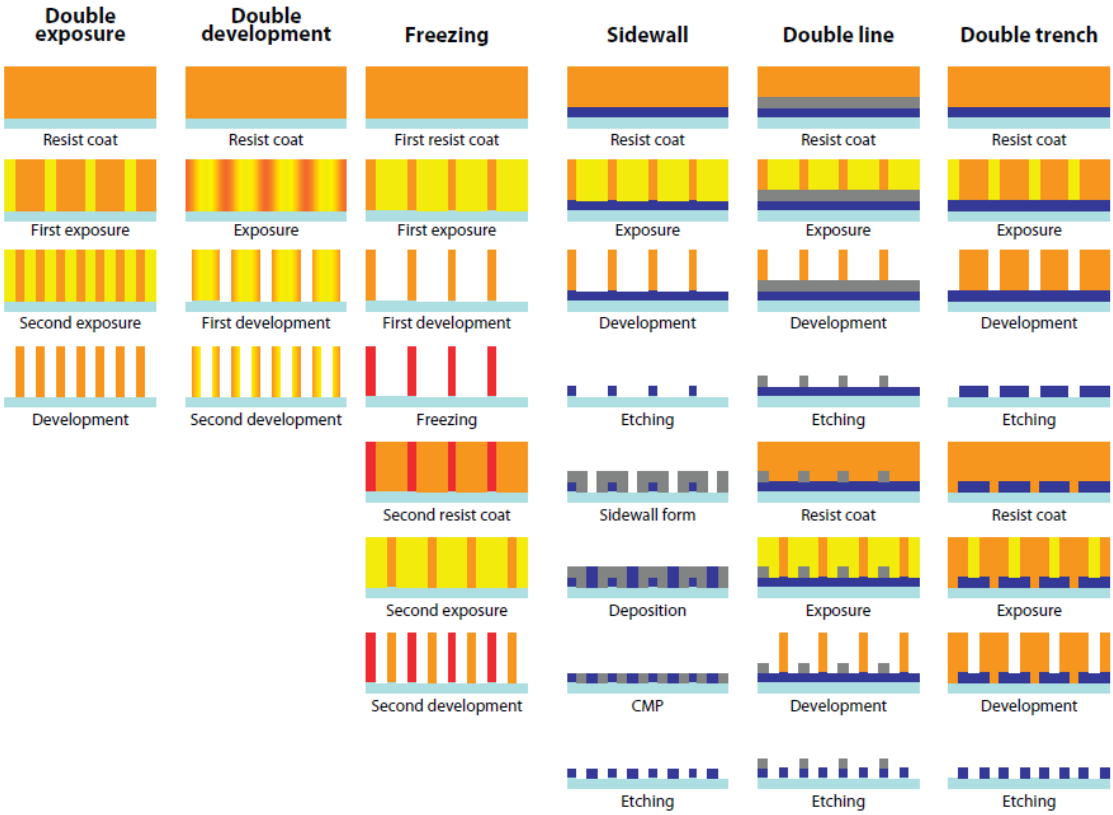

Figure 1.6. Schematic of a number of approaches for double-patterning lithography. CMP, refers to chemical mechanical planarisation.[104]

The significant technological advancements in the field of optical lithography outlined above demonstrate the suitability of these techniques to fabricate ordered arrays of semiconductor nanowires with excellent control over placement and feature-size. Lateral nanowires may be fabricated from layered substrates such as silicon-on-insulator (SOI), or epitaxial thin films, prepared by molecular beam epitaxy (MBE), or metal organic vapour phase epitaxy (MOVPE). Arrays of lateral nanowires can be prepared by fabricating gratings or line structures in the resist material and transferring the grating pattern to the substrate through the use of an appropriate etch process. Figure 1.5 displays a TEM image of a cross-section

through a 10 nm wide Si nanowire fabricated from SOI using 193 nm immersion lithography.

Similarly, vertical nanowires may be prepared from bulk or layered substrates by using a resist mask consisting of dot or polygonal structures with maximum lateral dimensions below 100 nm and transfer of the mask pattern deep in to the substrate, again using an appropriate anisotropic etch process.[114] Inductively coupled plasma (ICP) and reactive ion etch (RIE) techniques are most commonly used for pattern transfer, although anisotropic wet etch and metal assisted etch (MAE) procedures have also been used.[115,114]

1.3.2. Next Generation Lithography: Electron Beam Lithography and Competing Techniques

A number of lithography processes are being considered to extend lithography scaling beyond current UV lithography capabilities, for semiconductor device manufacturing. These techniques include, electron beam lithography (EBL),[116–118] nanoimprint lithography (NIL),[119,120] x-ray lithography (XRL),[121,122] extreme ultra-violet (EUV) lithography,[123,124] scanning probe lithography (SPL),[125] and electron beam induced deposition (EBID) lithography.[126–128] EBL is at the heart of many of these techniques, including the optical lithography processes. EBL is generally used for the fabrication of high-resolution photomasks for DUV, EUV and XRL. NIL stamps are also produced using EBL direct-write processes. EBID lithography is essentially an EBL process that incorporates the use of a gas injection system which disperses a gaseous precursor that decomposes under the electron beam and directionally deposits on the substrate surface forming a mask. As such, current and

future VLSI manufacturing is heavily dependent on the development of EBL processes and instrumentation. EBL has been shown to be capable of producing sub-10 nm features at sub-20 nm pitches.[129,130] Figure 1.7 displays examples of high-resolution EBL processes used to produce line-widths as small as 4.5 nm at pitches as low as 9 nm.

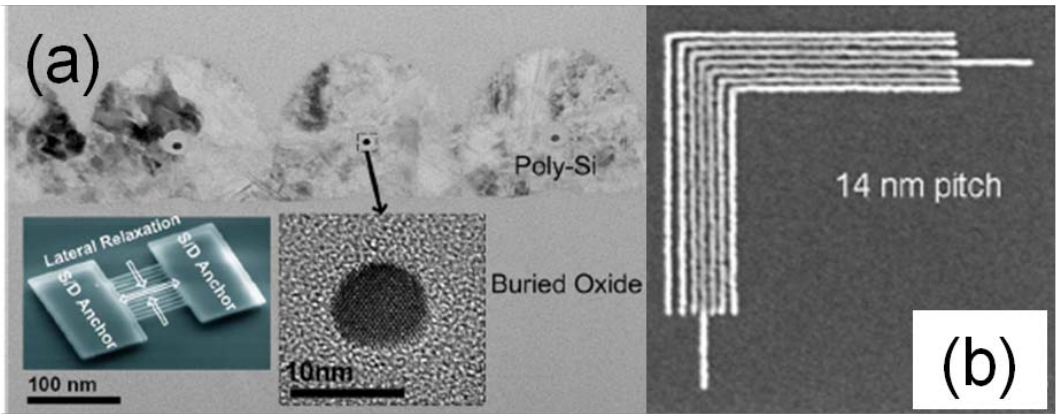

Figure 1.7. High resolution features produced by EBL: (a) 8 nm diameter strained n-Si nanowires produced using a hydrogen silsesquioxane (HSQ) EBL process for gate all-around FET devices and (b) nested lines at a pitch of 14 nm.[130,118]

However, the primary concern with the implementation of EBL techniques in HVM is the low throughput of wafers due to the exposure times required for full wafer layouts. Exposure times depend on several factors which include the tone of the resist, the area of the wafer to be exposed, the electron beam current, electron energy, and the sensitivity of the resist (electron dose required to completely chemically alter the resist).[105,131] Resist technology may have a significant role to play in the reduction of EBL exposure times. Increasing the resist sensitivity will significantly reduce the required time for exposure; however, increased sensitivity should not compromise the ultimate resolution of the resist. Hydrogen silsesquioxane (HSQ), the smallest member of the polyhedral oligomeric

silsesquioxane (POSS) family, is an example of one of the highest resolution negative-tone EBL resists. However, HSQ exposure doses are considered too high for use in HVM. Chemically amplified resists (CARs) have been developed with significantly increased sensitivity with respect to HSQ, but these resists offer lower ultimate resolution. The field of EBL resist research is an active one and recent demonstrations of EBL using analogues of HSQ with increased electron beam sensitivity are promising.[132]

Multi-beam EBL systems are under development which will increase wafer throughput either through beam-splitting techniques, or through the use of instruments with multiple electron sources, however, the technology is still not mature and as such has yet to be implemented on a HVM scale.[133] Lee *et al.*[134] have reported a particularly innovative example of multi-beam EBL using a Si crystal as an electron beam mask (figure 1.8). A transmission electron microscope (TEM) was used to create arrays of electron beams where the shape and separation of the beams was governed by the crystal structure and crystal orientation of the mask with respect to the incident electron beam. Atomic resolution images of the Si crystal lattice were magnified and projected onto HSQ films creating arrays of nanostructures in the resist. This technique shows promise for increased throughput where periodic arrays of simple nanoscale structures are desired.

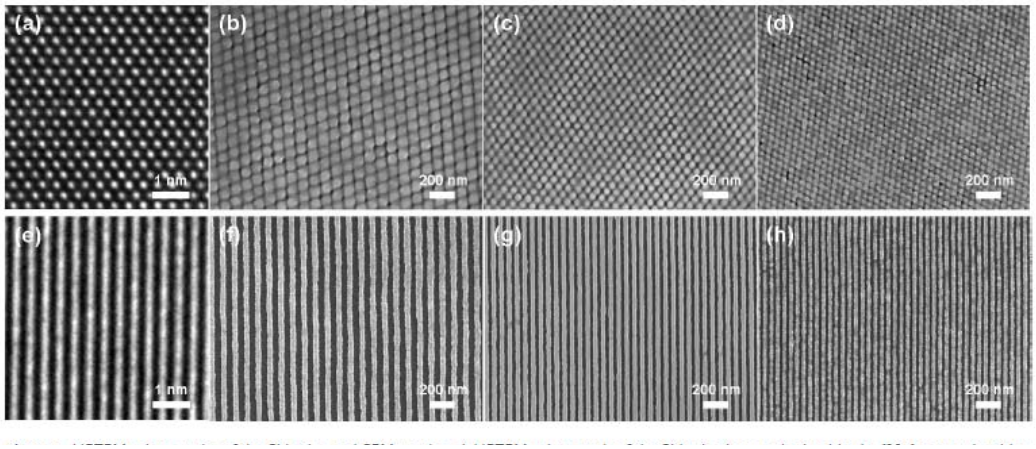

Figure 1.8. Arrays of HSQ nanostructures produced using projection of the atomic lattice of a Si crystal (a) and (e) in a TEM. SEM images (b-d) and (f-h) respectively show the critical dimension and pitch scaling of the structures with increasing TEM magnification, 160 × (b,f), 200 × (c,g) and 300 × (d,h).[134]

Arrays of dot structures produced by EBL can be used to fabricate vertical nanowire arrays through the use of a deep anisotropic etch.[135–137] The use of an etch resistant material to form the dot structures is paramount to facilitate deep etching to form high aspect ratio nanowires. Typically, Al_2O_3, Al, and SiN_x, have been used as etch masks for vertical Si nanowire fabrication. Figure 1.9 shows an SEM image of arrays of vertical Si nanowires produced using an EBL process.[137]

Commonly encountered issues for EBL processes include electron-substrate or electron-resist interactions and surface charging of insulating substrates. Electron-substrate and electron-resist effects can be grouped into three sub-classes, forward scattered electrons (scattering angle < 90°), back-scattered electrons (scattering angle > 90°) and secondary electrons.[105]

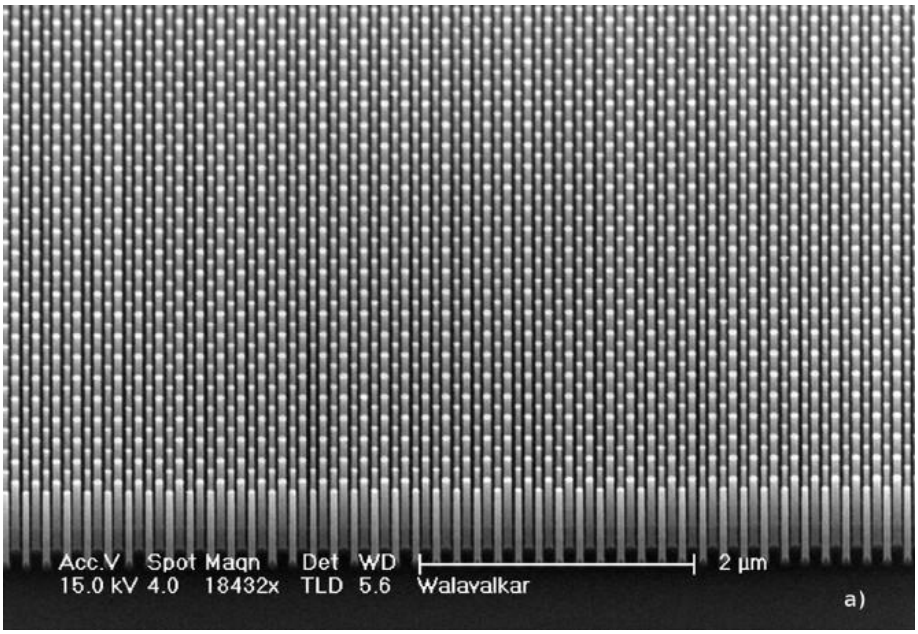

Figure 1.9. SEM image of an array of 50 nm diameter Si nanowires etched into a Si wafer. A sputtered Al_2O_3 hard mask, patterned by EBL was used as the Si etch mask.[137]

Forward scattered electron effects are most important within the resist as electrons which are forward scattered in the substrate have little contribution to resist exposure. Forward scattering can be minimised by using a high accelerating voltage (higher energy electrons) or a thinner resist layer. Backscattered electron exposure effects are more prominent for high atomic weight (*Z*) materials and as such are more commonly a consequence of electron-substrate interactions. Secondary electrons are the primary electron-solid interaction, and as such they make the largest contribution to resist exposure. Importantly, although secondary electrons are responsible for most of the resist exposure, their path length in the resist is short, typically < 10 nm, and as such these electrons do not have a significant contribution to proximity effects. Proximity effects can largely be attributed to backscattered electrons which experience large angle scattering and can commonly travel large

distances laterally in the substrate and resist (~ 1 μm for 10 keV incident beam energy). Proximity effects due to electron-solid interactions can be corrected through careful modelling of electron scattering, typically as a point spread function (PSF) and the use of appropriate electron dose contour maps based on these models.[133,138] Experimentally derived data can also be used to develop PSFs for use in proximity effect correction (PEC). PEC is particularly important for the exposure of high density features and large structures where electron scattering effects become prominent.

EBL on insulating substrates can be hampered due to surface charging upon electron beam exposure. Surface charging results in an associated electric field at the substrate surface which acts to deflect the incident electron beam with detrimental effects on the EBL process. Surface charging effects can be avoided by several methods. Deposition of a thin layer of conducting material (Au, Cr, Al or conducting polymers) atop the resist can remove surface charging effects, with the drawback of the introduction of an additional layer of material in the EBL process. Conducting polymers such as ESPACER (Showa-Denko), a member of the polythiophene family, are preferable to metals such as Au due to their superior process compatibility.[105] ESPACER is soluble in water and as such can be easily removed following electron beam exposure and prior to developing the resist, where as complete removal of Au and similar metals requires harsh etching conditions which may alter the resist, and the substrate. Much work has been performed in the field of electron-solid interactions and as such modelling and correcting undesired electron-solid interactions is now possible.[138] However, until EBL sample throughput times are reduced to acceptable levels for HVM, EBL will remain

confined to tasks such as quantum device demonstration, NIL stamp fabrication and high-resolution photomask fabrication.

Electron beam induced deposition (EBID) can be used as a lithographic tool to produce sub-10 nm features.[139,127] As stated previously, EBID essentially involves introducing a gaseous precursor species into the path of an electron beam in an EBL system. The precursor decomposes upon electron beam exposure and directionally deposits the solid decomposition product, typically a metal such as W, or Pt, on the substrate. EBID is a capable lithographic tool for the production of devices on a small scale.[126] However, EBID suffers from inherent drawbacks such as metal contamination of device structures and low throughput. EBID is more suited to small-scale applications such as photomask defect repair.

Many of the issues associated with the implementation of EUV, and XRL techniques in HVM have been discussed in the previous section. NIL is a mechanical lithography technique whereby a stamp or template created in a robust material, usually Ni or Si, for thermal NIL; PDMS for soft NIL; and quartz for step and flash NIL (S-FIL a trademark of Molecular Imprints Inc.), is pressed into a deformable resist on a substrate. The resist is then hardened so that when the template is removed the contours of the template are transferred to the resist. The patterned resist can then be used for subsequent pattern transfer procedures. NIL is a relatively inexpensive technique when compared to other nanolithography techniques and has demonstrated the production of very fine features at high areal densities.[119] Furthermore, NIL can be used to directly pattern interlayer dielectric (ILD) materials such as low-*k* silsesquioxanes (SSQs) thus reducing the number of process steps

required in the dual-damascene process typically used to form metallic interconnects.[140,141] However, there are outstanding issues concerning overlay accuracy, defect density and throughput. Additionally, NIL may not be compatible with pattern transfer to porous low-*k* materials used as back-end-of-line (BEOL) insulators, which are inherently brittle and may be deformed by the pressure applied during NIL.[119]

Scanning probe lithography (SPL) encompasses a range of lithography techniques including, dip-pen nanolithography (DPN), local oxidation nanolithography (LON), atomic force microscope (AFM) lithography and scanning tunnelling microscope (STM) lithography. Common to these techniques is the use of a scanning nanoscale probe, typically an AFM tip, to pattern a resist or substrate directly.[142,143] In the case of DPN an AFM tip is used to transfer a material to the surface which can subsequently act as an etch mask or may act as an active device component itself. LON is used to locally oxidise a material thus forming a patterned surface oxide by applying a voltage bias between a conductive AFM tip and the substrate material in the presence of water vapour to induce localised oxidation of the substrate through electrochemical reaction with the water vapour. AFM lithography can operate in contact mode or non-contact mode. Contact mode AFM lithography involves the mechanical patterning of a substrate much like NIL. An AFM tip can be used to scratch or stamp a pattern into a resist material or into the substrate itself. Non-contact mode AFM can be used to pattern materials through local oxidation of the substrate surface as in the case of LON, through local heating of a resist material using a heated AFM tip, or through local electron exposure via a field emission AFM tip.[142,143] STM lithography has been used to produce nanostructures by a variety of

means. Scappucci *et al*. have reported the use of STM to selectively dope regions on a H-terminated Ge (100) surface where H atoms have been removed by STM, thus creating doped nanowire structures.[125] STM can also be used for the individual manipulation of atoms on a surface to produced quantum structures, such as the quantum corral reported by Crommie *et al*. in 1993 (figure 1.10).[144] SPM lithography techniques are inherently slow even when multiple probes are used.[145] As such, low throughput will prevent such techniques from being used in HVM.[143]

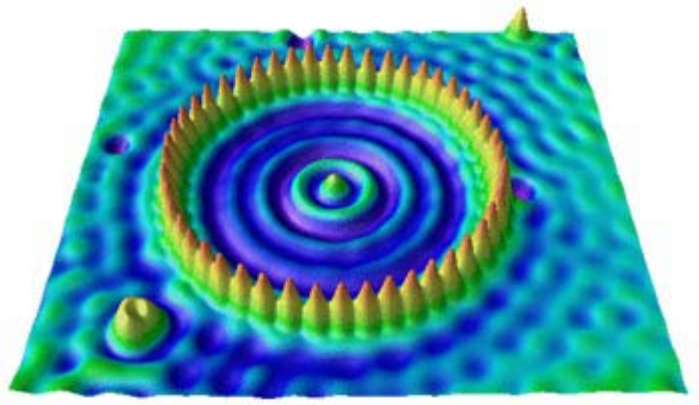

Figure 1.10. False colour STM image of a quantum corral structure created by the atomic manipulation of 48 Fe atoms on a Cu {111} surface. The Fe ring confines the surface electron wavefunction of the defect free Cu surface within.[144]

1.3.3. Top-Down Semiconductor Nanowire Fabrication Outlook

Top-down semiconductor lithography processes have dominated the area of semiconductor device definition and placement for decades. However, as the density of devices on a chip continues to scale significant difficulties are encountered. Techniques such as EBL and XRL with significantly reduced wavelengths, may readily achieve the high densities of devices desired by the semiconductor industry, however, there are a number of difficulties associated with the integration of these short wavelength techniques in VLSI manufacturing. Consequently, it seems

increasingly likely that current top-down processes may have to 'reach out' to a bottom-up technology to achieve the future goals of the semiconductor industry.

1.4. Integration of Bottom-Up and Top-Down Nanowire Fabrication Processes

1.4.1. Directed Self-Assembly

Directed self-assembly (DSA) is an advanced lithographic process based on the self-assembly of block copolymers (BCPs). BCP self-assembly involves the bottom-up, microphase separation of chemically different blocks within the BCP. Typically, A-B diblock copolymers are used for DSA, where an A-B diblock copolymer consists of a linear chain of a monomer A, joined at one end by a covalent bond, to a linear chain of monomer B. When the two blocks, A and B, are sufficiently chemically distinct from one another, they can microphase separate so as to minimise the interaction volume of blocks A and B, whilst maximising the interaction volume between similar blocks. The chemical interaction of the two blocks in a BCP is often quantised by the Flory-Huggins interaction parameter (χ) for that BCP system which is related to the enthalpy of mixing for that polymer system.[146] Self-consistent mean field theory has been used to generate theoretical phase diagrams for diblock copolymer melts (figure 1.11).[147] Mean field phase diagrams are presented as a plot of χN against f, where N is the degree of polymerisation of the BCP and f is the volume fraction of a reference block in the BCP. χN is representative of the thermodynamic driving force for microphase separation within the diblock copolymer melt. χ represents the enthalpic component and is inversely related to temperature and directly related to polymer chain length, whilst N represents the

entropic component, which depends on the chain length dependent number of conformations that can be adopted by the polymer.

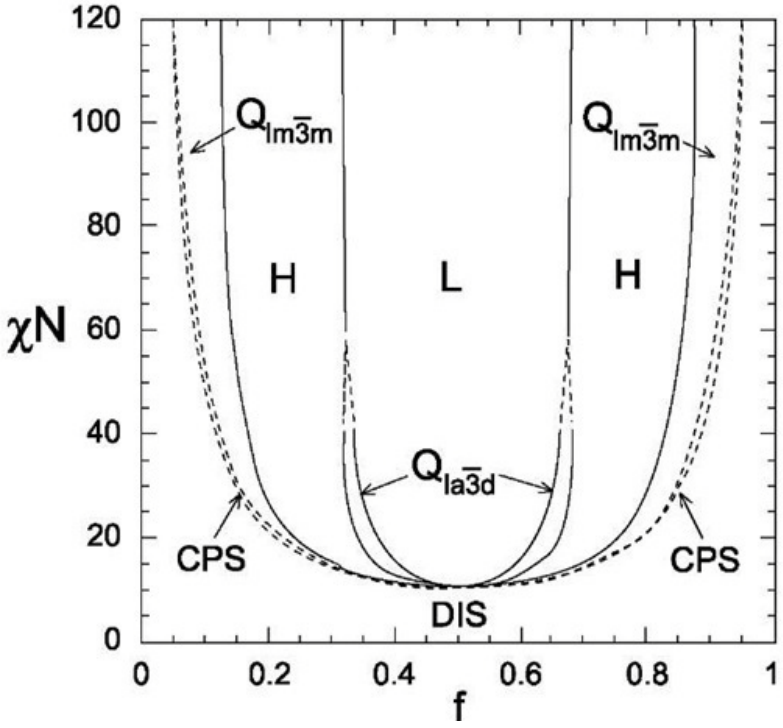

Figure 1.11. Phase diagram of a diblock copolymer as predicted by self-consistent mean field theory. Phases are labelled L (lamellar), H (hexagonally arranged cylinders), $Q_{Ia\bar{3}d}$ (bicontinuous $I_{a\bar{3}d}$ cubic), $Q_{Im\bar{3}m}$ (body centred cubic spheres), CPS (close packed spheres), and DIS (disordered).[147]

Figure 1.12 shows schematic examples of phase morphologies within a microphase separated A-B diblock copolymer with increasing number fraction of block A (f_A).[146]

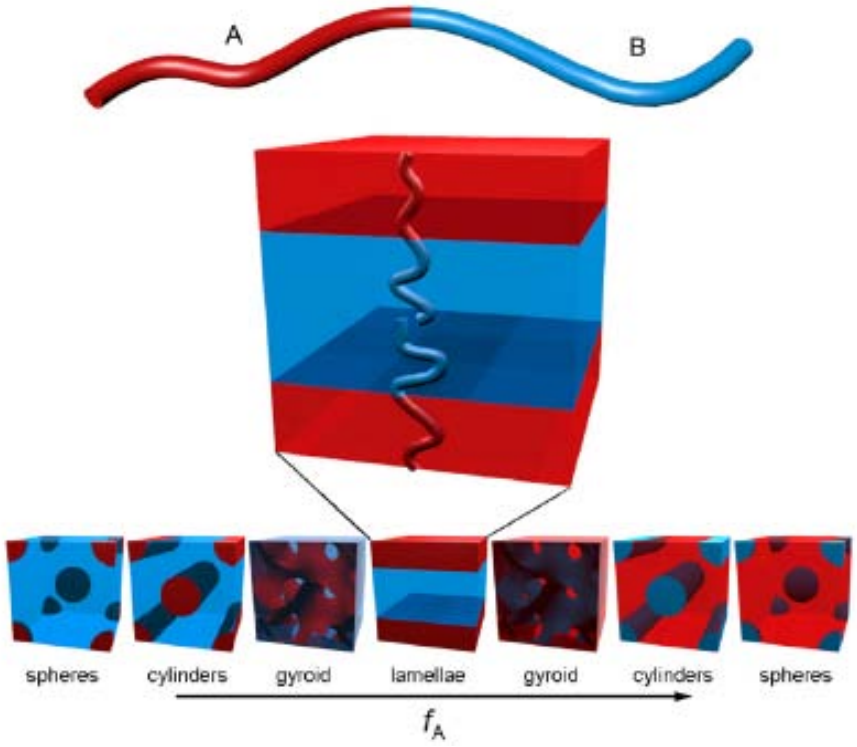

Figure 1.12. Schematic representation of the microphase morphologies of an A-B diblock copolymer with increasing number fraction of block A from left to right.[146]

Lamellar and hexagonally close packed cylinder phases of BCPs are typically used in DSA, where the phase of the BCP can be controlled through selection of appropriate polymer fractions in the BCP, and suitable polymer chain lengths. The microphase separation of BCPs can be guided both chemically and physically through the use of careful templating techniques, *i.e.* directed self-assembly. Physically guided microphase separation of a BCP is often termed graphoepitaxy. DSA of lamella forming BCPs by graphoepitaxy, is generally achieved by creating trenches on a substrate where the trench width is an integer multiple of the block length.[148,146] Similarly, chemically guided microphase separation of a BCP is termed chemical epitaxy. DSA by chemical epitaxy is achieved using a substrate that has been chemically patterned to induce ordering during microphase separation of the BCP.[149,150] Consequently, DSA by both graphoepitaxy and chemical epitaxy is

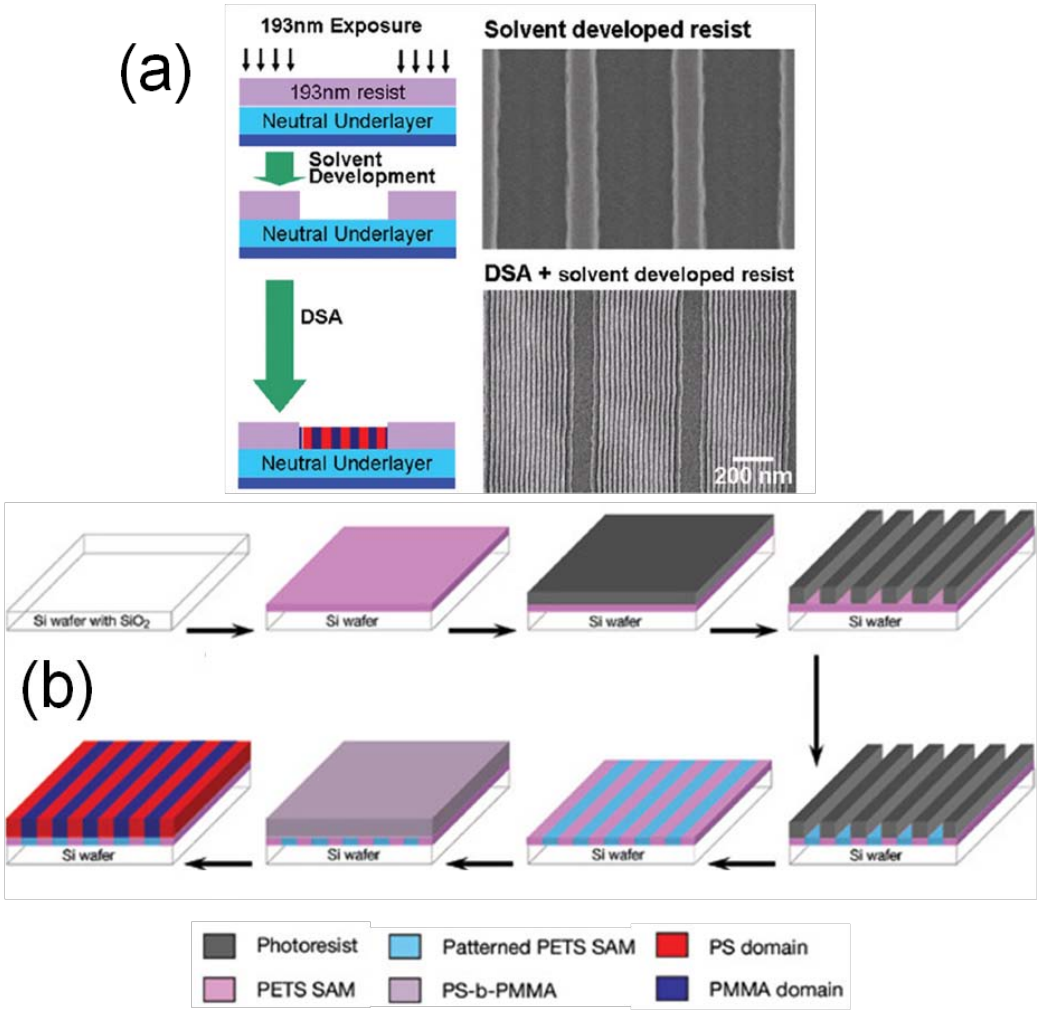

Figure 1.13. Typical process flows used to produce DSA of BCPs via (a) graphoepitaxy and (b) chemical epitaxy, respectively.[150,151]

heavily dependent on conventional lithographic techniques such as those outlined in Section 1.3.

Ordered diblock copolymer films produced by DSA can be used as high-resolution etch masks for semiconductor nanowire fabrication. As such, DSA has gained significant interest in the field of nanolithography in recent years. DSA offers a number of advantages over conventional optical or direct-write lithography techniques. Firstly, DSA can achieve sub-lithographic resolution by pattern

multiplication, thus increasing the density of features within low density patterns produced by conventional optical or mask-less lithography techniques.[152–155] Additionally, the resolution of block copolymer lithography can be controlled by tuning the length of the polymer chains in the BCP. Reduction of the polymer chain length results in an equivalent reduction in the domain dimensions within the microphase separated BCP. Implementation of a pattern multiplication process in current lithographic methods for VLSI manufacturing would remove the necessity for complicated techniques such as double patterning and high density lithography.[149] DSA by chemical epitaxy has also been shown to exhibit self-healing properties, whereby defects in templates used to guide microphase separation are corrected in the extended pattern of the mask produced by DSA.[156,157] Additionally, DSA is a relatively inexpensive technique, depending on the process used to guide microphase separation. DSA has the potential to offer very high throughput if it were incorporated with current optical lithography processes, and can readily achieve sub-20 nm critical dimensions by controlling the molecular weight of the polymer blocks in the BCP. Furthermore, DSA has been shown to be capable of producing device specific geometries such as bends, T-junctions and jogs.[158,152] Parameters such as line-edge-roughness (LER) for DSA masks are determined by the quality of the microphase separation and associated guiding technique as well as the quality of the etch used to selectively remove one of the blocks of the BCP. LER values as low as 1.95 nm (3σ) have been reported for lines produced by DSA of a lamella forming BCP.[149]

However, there are a number of outstanding concerns associated with DSA as a lithographic technique. The primary concern with the process is high defect density, attributable to contamination, BCP purity, BCP molecular weight distribution,

chemical uniformity of the substrate surface and defects within the DSA guiding template. Additionally, BCP layers are often prepared as thin monolayers and often have poor etch resistance, *e.g.* PMMA, PS.

Whilst the defect density in DSA masks is improving with increased research investment, DSA processes still require further optimisation before they can be integrated into a HVM landscape. Figure 1.14 shows an example of relatively large area patterning achieved via the graphoepitaxy of PS-*b*-PDMS.[153]

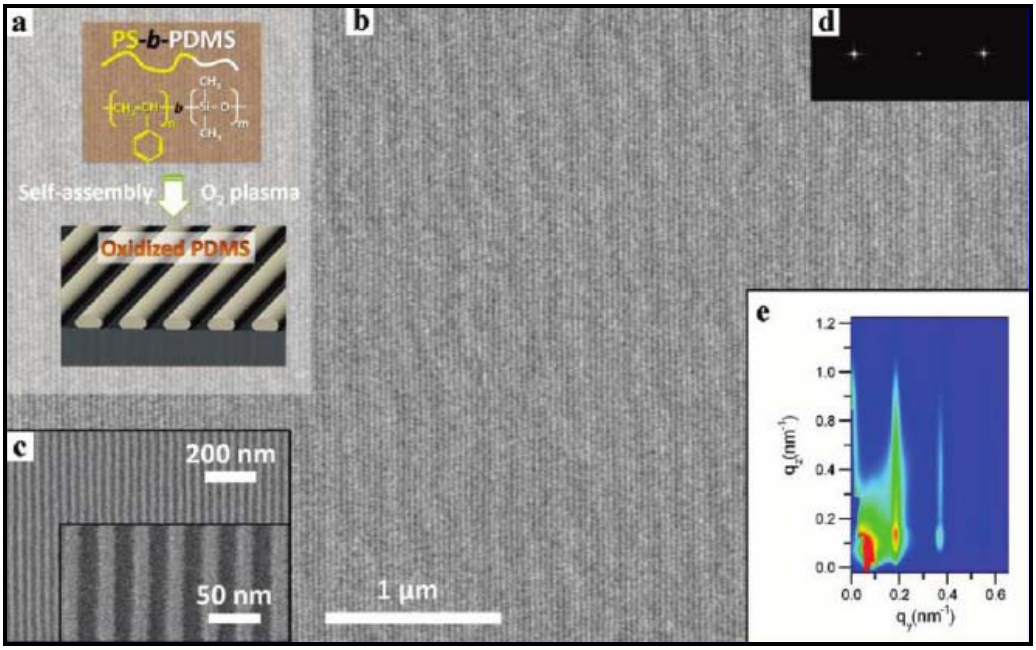

Figure 1.14. (a) A schematic of the structure of PS-*b*-PDMS and the structure formed by DSA. (b) SEM image showing large-scale alignment of PDMS lines produced by the graphoepitaxy of PS-*b*-PDMS within 10 µm wide, PDMS brush coated trenches etched in a Si wafer. (c) Higher magnification images of the aligned PDMS lines. (d) FFT of the image in (b) consistent with excellent long-range ordering. (e) Grazing incidence small angle x-ray scattering (GISAXS) pattern generated from a 1 cm^2 area of the PDMS line pattern.[153]

Chemical epitaxy DSA techniques can 'heal' defects present in the guiding template; however, chemical epitaxy has not yet demonstrated pattern multiplication to the extent of graphoepitaxy based techniques. Thus, it is likely that each approach, chemical epitaxy and graphoepitaxy, will find their own niche application within the semiconductor industry. Development of DSA masks with sufficient etch resistance will depend on the specific process requirements. PS-*b*-PDMS for example, is a promising material for DSA when a high etch resistance to Si etchants is required. PDMS has an inorganic Si-O backbone and as such offers superior etch resistance relative to organic polymers.

The outlook for DSA is promising. DSA has already demonstrated the requisite resolution capabilities for continued device scaling outlined within the International Technology Roadmap for Semiconductors (ITRS), defect density levels are dropping with continued research investment and issues regarding production of device specific geometries appear to be resolvable using chemical epitaxy approaches.[149] LER and CD control issues also need to be addressed to meet ITRS specifications.[149] Theoretical models predict LER to be related to $\chi^{-0.5}$, in which case, BCP systems with high χ values such as PS-*b*-PDMS ($\chi \sim 0.26$ at room temperature) are worthy of further investigation.[153]

Self-assembly of cylinder and sphere forming BCPs has also been used to produce ordered arrays of metal nanoparticles by both additive[159] and subtractive[160], processes. These metal nanoparticles may then be used to produce epitaxial growth of semiconductor nanowires by means of the relevant techniques outlined in Section 1.2. Furthermore, the metal nanoparticles may be used as etch masks to produced

ordered arrays of vertical nanowires by a top-down approach. The use of BCP films to template catalysts for epitaxial nanowire growth and to template hard masks for top-down vertical nanowire array formation is an example of a synergistic process, employing both bottom-up and top-down methods. This synergistic process is to date, a poorly explored application of BCP lithography which warrants further investigation.

DSA is a promising blend of top-down and bottom-up techniques for advanced lithography applications. DSA allows a route to increased pattern resolution and feature density relative to conventional optical lithographic means, and whilst concerns still exist over LER, CD control and reproducibility, these concerns are gradually being improved by continued advances in the field. DSA depends on conventional lithography techniques such as optical lithography, interference lithography and EBL to form guiding templates to direct the self-assembly of BCPs and as such it will remain a complementary lithography technique. However, if and when the issues associated with DSA are resolved, this lithography technique may alleviate the growing demands on optical lithography and EUV for continued device scaling, thus extending the use of current optical lithography techniques in VLSI manufacturing.

1.4.2. EBL Catalyst Placement for Bottom-Up Nanowire Growth

EBL is a suitable tool for the preparation of ordered arrays of metal nanoparticles by subtractive or additive processes. Ordered arrays of metal nanoparticles can be readily prepared using a positive tone EBL process to generate a metal lift-off mask.[161,16,81,72] This process can be used to produce epitaxial nanowire growth via a

VLS-type mechanism through careful control of the metal substrate interface, and choice of an appropriate substrate material, using nanowire growth methods such as those outlined in section 1.2. Coupling EBL and self-assembly of BCPs allows the production of defect free high-density arrays of dot structures.[162]

1.4.3. Nanosphere Lithography

Nanosphere lithography (NSL) can be used to produce ordered arrays of vertical nanowires. NSL uses the bottom-up self assembly of spherical particles, such as polystyrene spheres, to create dot/anti-dot arrays on the surface of a substrate, which then may be used to transfer the pattern to the substrate creating structures such as vertically aligned nanowire arrays.[163–166] NSL can be used to produce arrays of vertical Si nanowires using a metal-assisted etching approach as shown in figure 1.15 below. Combined use of NSL and metal-assisted etching (MAE) provides a route to forming arrays of long (> 10 μm) Si nanowires which have applications in fields such as vertical ICs and solar cells (figure 1.14).[166] NSL can also be used to create an anti-dot array mask for the evaporation of arrays of metal nanoparticles for use as catalysts for epitaxial nanowire growth.[163]

1.4.4. Miscellaneous Synergistic Nanowire Fabrication Processes

A range of processes exist which use both bottom-up and top-down techniques in tandem to produce semiconductor nanowires. One example of such a technique is the supperlattice nanowire pattern transfer (SNAP) technique.[167] The SNAP technique is based on the formation of a stamp by selectively etching one of the layers in a superlattice material grown by a bottom-up epitaxy technique, such as MBE. Angular deposition of a metal on the etched superlattice then allows creation

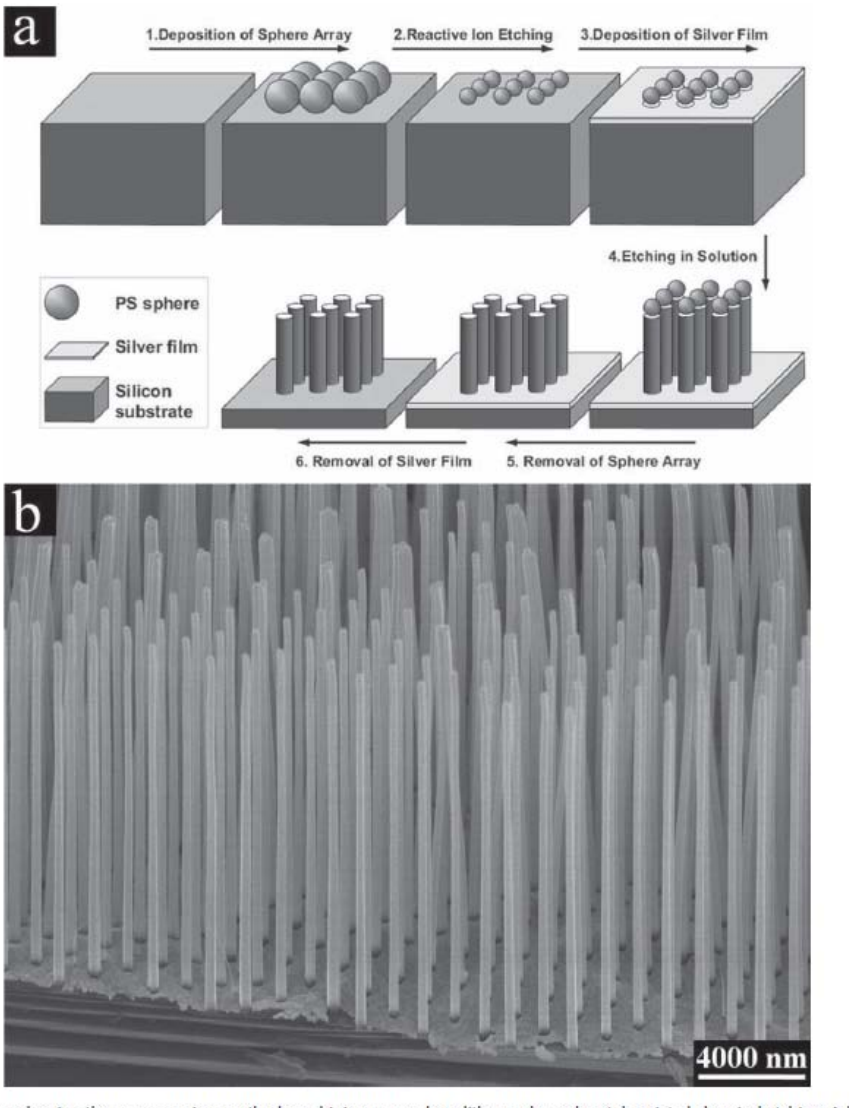

Figure 1.15. Schematic of NSL process for the fabrication of vertical Si nanowire arrays via MAE.[165,168]

of a metal stamp which is pressed against the material of choice producing a metal grating which acts as an etch mask for the fabrication of nanowire arrays by pattern transfer. Figure 1.16 shows a schematic of the SNAP process. The SNAP process has been used successfully to produce arrays of Si nanowires from SOI, as well as metal nanowires formed directly from the stamp. However, the technique is limited in terms of the geometries of the structures that can be produced, and the complexity of the process for large-scale nanowire fabrication. Furthermore, the SNAP

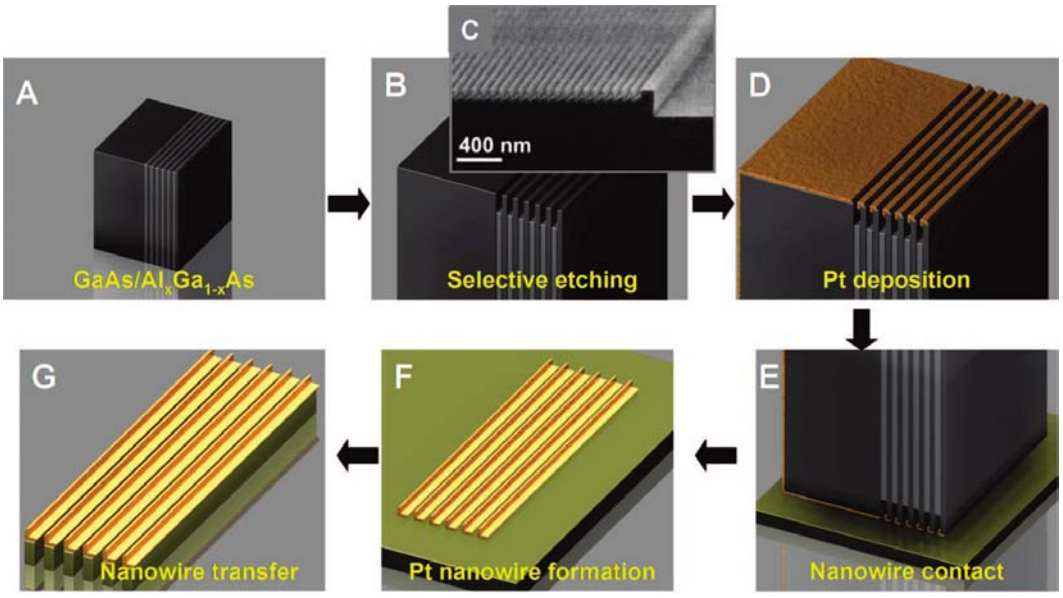

Figure 1.16. Schematic of the SNAP process for production of aligned nanowires.[167]

technique is susceptible to many of the pitfalls associated with NIL outlined in section 1.3.2.

NIL can be used to created arrays of metal nanoparticles for bottom-up nanowire growth.[169] This process involves imprinting a bilayer positive-tone resist, developing the imprinted resist and evaporating a metal layer to produce arrays of metal nanoparticles by lift-off. The metal nanoparticles can subsequently be used as catalysts for nanowire array production by standard nanowire growth procedures.

AAO membranes with HCP pore arrangements are formed by a bottom-up process, as discussed in Section 1.2.2. These ordered porous membranes can be used as masks to produce patterned metal films on Si substrates for MAE of Si, producing ordered arrays of vertical Si nanowires.[170,171] MAE techniques using patterned metal layers are successful at producing dense, ordered arrays of vertical nanowires with high aspect ratios. However, as with all MAE techniques, the nanowires produced

have rough sidewalls thus inhibiting their use in logic applications where surface scattering of charge carriers is a significant drawback.[165,172] Nanowires produced by these methods are likely to find applications in solar cell, thermoelectric generator, sensor or battery anode applications where the increased surface area of nanowires with rough sidewalls may be beneficial to device performance.[173,174]

Ion track-etched membranes are an example of another nanowire template material. These membranes are formed in a top-down process by ion etching of a polymer material, producing cylindrical or tapered pores. Infilling ion track-etched membranes by methods such as electrodeposition can produce arrays of nanowires.[175] Whilst this method can be used to produce some interesting network structures (figure 1.17), it is unlikely to find use in VLSI manufacturing due to the complexity of the process and the difficulty producing single-crystalline materials within these membranes.

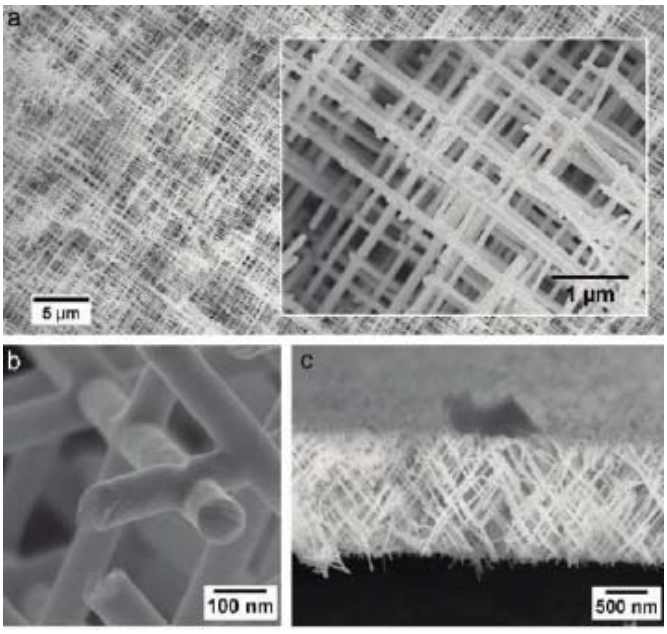

Figure 1.17. SEM images of polycrystalline Pt nanowire networks produced within ion track etched membranes: (a) low magnification SEM images of Pt nanowire

networks, (b) high magnification SEM image of nanowire junctions and (c) cross-section of a nanowire network composed of 35 nm diameter nanowires.[176]

1.5. Emerging Semiconductor Nanowire Materials

1.5.1. High Mobility Materials for Next Generation CMOS Devices

High charge carrier mobility materials have been subject to significant research investigation in the past few decades. These materials offer increased transconductance relative to Si, and as such, devices constructed from these materials may achieve similar drive current at lower power, or operate as high performance devices at equivalent power, to current Si devices.[177] Many materials are under consideration for integration in future CMOS devices due to their increased charge carrier mobility relative to Si.[177–179,12] Ge, for example, exhibits hole mobility over four times that of Si, and as such is a strong contender for use in future p-FET devices. Likewise, InSb, InAs and graphene demonstrate massively increased electron mobility relative to Si.[178,180] However, these high mobility materials are not without their drawbacks. Often, Ge and III-V materials possess complex native oxides with poor chemical or electrical properties for device fabrication.[93] GeO_2, a component of the complex native oxide on Ge crystals, is water soluble and as such must be removed or capped with a more suitable material to facilitate processing steps involved in device manufacturing. Additionally, GeO, another component of the native oxide on Ge, desorbs at temperatures above 400 °C, which may result in detrimental effects on overlying layers during annealing steps in device manufacturing. Chapter 3 considers issues associated with a high-resolution negative-tone EBL process on the complex native oxide of Ge surfaces.

Similar difficulties have been reported for III-V materials such as GaAs and $In_{1-x}Ga_xAs$, whose complex native oxides prevent the formation of a stable semiconductor-insulator interface. The result is a high density of interface states at the semiconductor-insulator interface in the gate stack.[92,181] Interface states often lie near the mid band-gap of the semiconductor and can lead to Fermi-level pinning at the semiconductor surface. Fermi-level pinning can result in a number of detrimental effects on device performance, including, rectifying characteristics in metal-semiconductor contacts, and depletion of free charge carriers in the device channel at the semiconductor-insulator interface.[182,88] Interface states result from unsaturated surface atoms, which act as charge acceptors and donors at the semiconductor surface. Consequently, reduction of the density of interface states is dependent on the formation of a stable and saturated semiconductor surface. There have been significant investigations into improvement of the electrical and chemical interfaces with these materials to facilitate their integration within next generation CMOS devices. The use of a capping Si layer of the order of a few monolayers thickness has been successful in reducing the density of interface states (D_{it}) in GaAs from 10^{13} cm^{-2} eV^{-1} to 10^{11} cm^{-2} eV^{-1}.[181] Similarly, deposition of SiO_2 directly on an untreated Ge surface results in a relatively high D_{it} of 10^{13} cm^{-2} eV^{-1}, whilst, formation of a $Ge_{(100)}/GeO_xN_y/HfO_2/Pt$ gate stack produced a D_{it} of 3×10^{11} cm^{-2} eV^{-1}.[92,93] A further promising route toward improving the interface of inorganic semiconductor materials with gate-dielectric layers may be through the use of an appropriate organic dielectric material chemically tethered to the semiconductor. Extensive research has been pursued in the field of chemical functionalisation of Ge and III-V surfaces with high coverage of organic ligands.[183–185] High-*k* organic gate-dielectrics have been investigated primarily for use with organic FET devices, and

have demonstrated competitive levels of performance when compared with current VLSI devices.[186] Consequently, the molecular tethering of high-*k* organic molecules directly to these surfaces may allow a route to high-*k* insulating layers with low D_{it}, thus improving device performance.

Graphene has demonstrated impressive electrical performance in reported device applications with charge carrier mobilities as high as 230000 $cm^2V^{-1}s^{-1}$.[187] However, there are a number of outstanding concerns with regard to the integration of graphene in VLSI manufacturing. Firstly, pristine graphene is a zero-gap semi-metal and as such exhibits poor switching behaviour for logic device applications. Significant efforts have been made to introduce a large and reproducible band-gap into graphene. These efforts have included quantum confinement of graphene within graphene nanoribbon (GNR) structures, doping, edge functionalisation and use of bilayer graphene.[187] Additionally, there are serious concerns regarding graphene processing for device fabrication. Production of large area, single layer graphene is a challenging task, and handling such a delicate material has associated difficulties. Metals and gate-oxides exhibit poor adhesion to graphene and graphene layers are extremely vulnerable to plasma induced damage.[188] Despite the many concerns regarding implementation of graphene in CMOS manufacturing, it maintains a massive research impetus and is firmly implanted on the ITRS for continued investigation.[12]

Similarly, carbon nanotube (CNT) structures have been investigated heavily for use as FET semiconductor channels and as metallic interconnect materials.[189] The primary difficulty with CNT material preparation for FET and interconnect

applications is controlling the electronic band structure of the material, which is dependent on CNT growth direction, and diameter.[190] Furthermore, CNTs are subject to alignment and integration issues inherent to bottom-up nanowire and nanotube synthesis techniques as outlined in section 1.2.2.

1.5.2. Thermoelectric Nanowires

Thermoelectric materials are of great interest for energy recovery devices. A massive amount of waste heat energy is generated annually by processes such as hydrocarbon fuelled heat engines and integrated circuits.[174] Thermoelectric materials may allow a route to recover large amounts of this waste energy by converting the waste heat energy to electricity. The efficiency of thermoelectric materials is characterised by their thermoelectric figure of merit ZT[191], which can be determined using equation 1.2, where S represents the Seebeck coefficient, T is absolute temperature, ρ is electrical resistivity and k_T is the total thermal conductivity, which is the sum of lattice and electronic thermal conductivities.

$$ZT = \frac{S^2 T}{\rho k_T} \tag{1.2}$$

Bi_2Te_3 and Bi_2Se_3 and alloys thereof, are promising materials for thermoelectric applications due to their high demonstrated values of ZT.[191,7] Dresselhaus and co-workers suggested over 20 years ago that one-dimensional forms of thermoelectric materials would display enhanced thermoelectric properties relative to bulk counterparts, due to reduced thermal conductivity in the 1-D structures associated with confinement of phonons in the material. Consequently, thermoelectric

nanowire materials are an area of great interest for heat energy recovery and conversion. Chapter 4 outlines a route to the production of Bi_2Se_3 nanoribbons from MBE grown thin films using high-resolution EBL. In particular, this work highlights the importance of surface preparation to facilitate the use of a HSQ EBL process.

1.6. Nanowire Fabrication Outlook

The continued scaling of semiconductor devices in the VLSI industry has created a landscape where the introduction of nanowire or nanoribbon devices into mass production seems increasingly likely. As the density of semiconductor devices in VLSI architectures increases there has been an associated shift of the semiconductor channel from a planar orientation, to the recently developed fin structure where the semiconductor channel is raised above the surface of the Si wafer. A natural progression from the finFET or tri-gate structure would appear to be a nanowire structure, be it lateral – parallel to the substrate – or vertical. The benefits of nanowires have been highlighted for a number of years now. Semiconductor nanowires allow production of gate all around (GAA) devices which offer superior control of the device channel and thus improved switching speed and on/off ratios. A nanowire structure can also be used to create quantum well, core-shell structures with improved electrical transport properties relative to standard structures. Nanowires may also incorporate strain, a prerequisite in current VLSI devices[192,112,193], through the incorporation of dopants or a lattice mismatched shell material.[194,195]

The exact fabrication route to future semiconductor nanowire-based integrated circuits is as yet, unclear; however, it is quite probable that the route will incorporate both top-down and bottom-up techniques in tandem to allow a scalable path to nanowire integrated circuit fabrication. Bottom-up nanowire growth processes allow routes to structures that may not be produced by top-down means. Bottom-up grown semiconductor nanowires often exhibit faceted surfaces that may not be achieved by top-down fabrication. Control of the crystal surface facets formed during nanowire growth, may allow control over the density of interface states formed at nanowire surfaces, which is particularly important for Ge and III-V materials to develop improved device performance. Top-down processes such as optical and electron beam lithography consistently demonstrate their superiority in the nanometre control of device definition and placement. DSA of BCP films is an example of the synergistic cooperation of a bottom-up self-assembly process and traditional top-down lithography, allowing routes to aligned pattern multiplication, which is not feasible by either technique alone. As such, a conservative prediction would be that future nanowire-based electronics will be fabricated by a cooperative mix of both bottom-up and top-down processes.

1.7. Thesis Summary

Chapter 3 of this thesis highlights a novel synthetic, bottom-up route to the production of Ge nanowires with controlled diameter distributions in the absence of metal seed catalyst particles. The research outlines a plausible crystal growth mechanism for the nanowires based on the observations during extensive structural characterisation of the nanowires.

Chapter 4 details a high-resolution top-down route to the fabrication of aligned Ge and Bi_2Se_3 nanowire arrays using electron beam lithography (EBL). In particular, this chapter details the careful chemical treatment of Ge and Bi_2Se_3 crystal surfaces to remove native oxide components that impede high-resolution EBL using a negative-tone hydrogen silsesquioxane (HSQ) EBL resist.

Chapter 5 highlights the capabilities of high resolution EBL in creating Si nanowire arrays and in the directed self-assembly (DSA) of a diblock copolymer for sub-20 nm advanced lithography applications.

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Chapter 2

Experimental

2.1. Self-Seeded Supercritical Fluid (SCF) Phase Synthesis of Ge Nanowires

Ge nanowire synthesis was achieved through the thermal decomposition of the organosilyl germane precursors, hexakis(trimethylsilyl)digermane ($Ge_2(TMS)_6$) and tris(trimethylsilyl)germane ($Ge(TMS)_3$). Hexakis(trimethylsilyl)digermane was synthesised as described in the literature through collaboration with Prof. Christoph Marschner at TU Graz, Austria,[1] and tris(trimethylsilyl)germane was used as purchased (ABCR GmbH & Co. KG). High temperature synthesis (> 703 K) of Ge nanowires was performed in a supercritical toluene medium using the setup shown schematically in figure 2.1.

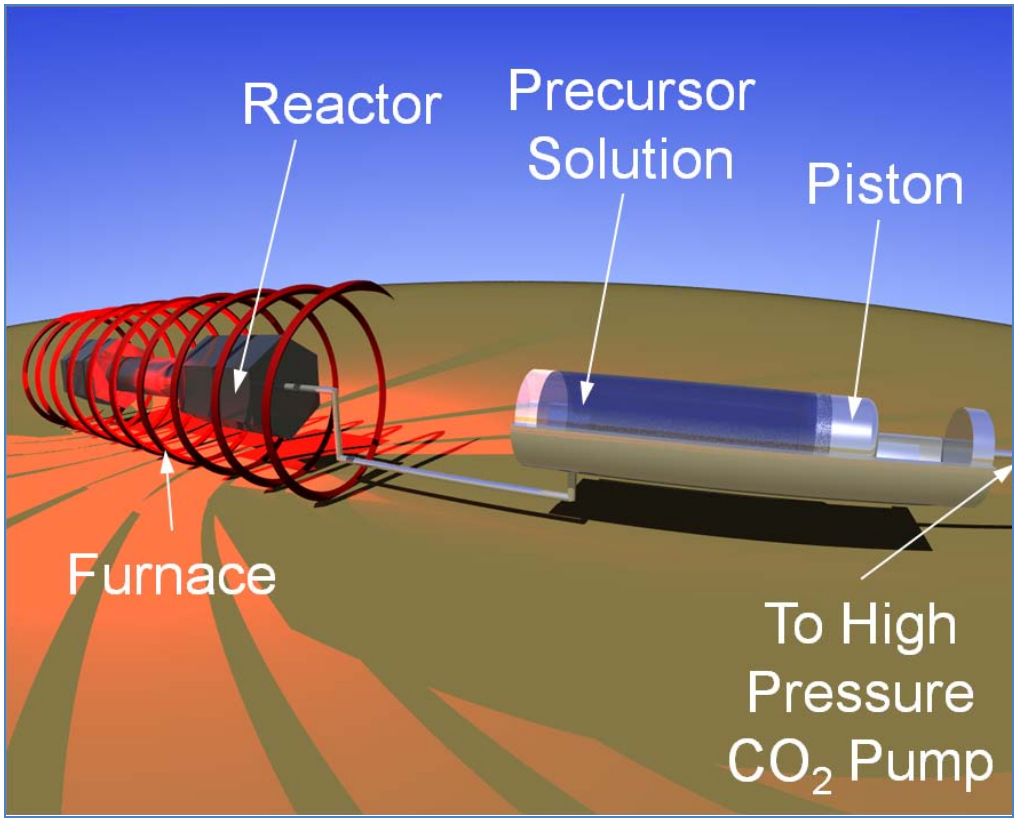

Figure 2.1. Schematic of reaction setup for the supercritical fluid phase synthesis of Ge nanowires.

In a typical experiment 100 mg of $Ge_2(TMS)_6$ was dissolved in 10 mL of dry, oxygen-free toluene and loaded into a 20 mL stainless steel precursor reservoir. Separately, 1 mL of toluene was loaded into a 5 mL volume, stainless steel reaction cell, which was connected to the precursor reservoir by 1/16" stainless steel tubing and valves. Precursor dissolution and loading was performed within a nitrogen filled glove-box (O_2 < 0.2 ppm, H_2O < 3 ppm) to help prevent the formation of GeO_2. The sealed reaction cell was then placed in a tube furnace and heated to the desired synthesis temperature, which was monitored by a thermocouple connected to the reaction vessel. Whilst the reaction cell was heating, 17.2 MPa pressure was applied to the precursor solution in the reservoir and injected at the chosen synthesis temperature using a 266 mL CO_2 pump (ISCO systems, Licoln, NE). The volume of the precursor solution injected into the cell was dependent on the pressure difference between the reaction cell and the pressure applied to the precursor reservoir by the CO_2 pump. This pressure difference could be controlled by the volume of toluene placed in the reaction cell prior to heating. Typically, 2.5 ± 0.3 mL of precursor solution was injected into the reaction cell and the holding time was adjusted according to the temperature employed for a high yield of Ge nanowires. Synthesis times required to produce Ge nanowires for each synthesis temperature are tabulated in the table 2.1.

Table 2.1. Synthesis time required to produce Ge nanowires from hexakis(trimethylsilyl)digermane in toluene.

Synthesis Temperature (K)	**Synthesis Time (h)**
573	48
673	24
723	4
773	1

The cell was opened at room temperature, the initial solvent collected and combined with an acetone solution used to collect the nanowire material attached to the side walls of the reactor. The red/brown nanowire product was isolated from the solvents by evaporation. Further purification of the nanowire material was performed by centrifugation at room temperature (7000 rpm for 15 min; 3 × toluene, and 2 × ethanol).

2.2. Self-Seeded Solution Phase Synthesis of Ge Nanowires

In a separate approach, in order to confirm that the wires were not seeded from Fe or Ni in the walls of the stainless steel cell, Ge nanowires exhibiting the same morphology as those synthesised by the SCF phase method described above, were prepared under atmospheric pressure using standard Schlenk line techniques, similar to the procedure described by Heitsch *et al.*,[2] for the preparation of Si nanowires from Au and Bi nanoparticles. A schematic of the apparatus used for the solution phase synthesis of Ge nanowires is shown in figure 2.2.

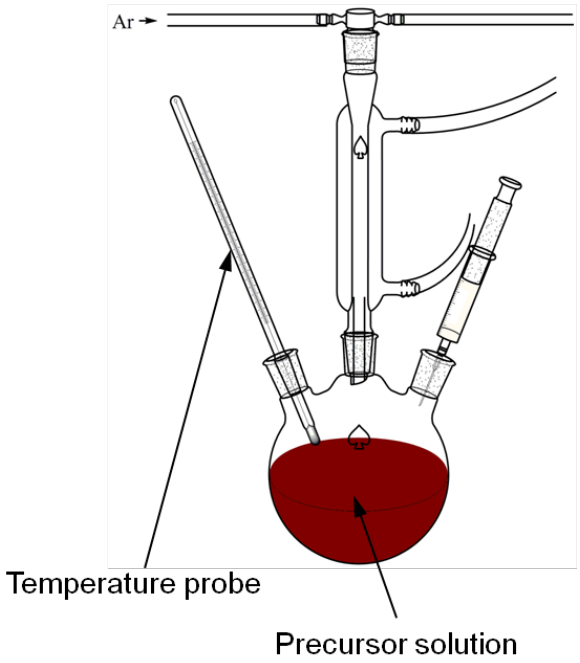

Figure 2.2. Schematic of the apparatus arrangement for the solution phase synthesis of Ge nanowires.

100 mg of $Ge_2(TMS)_6$ was placed in a 3-necked 50 mL round bottomed flask with 5 g of dried octacosane (b.p. 703 K) and connected to the Schlenk line via a Liebig condenser connected to the central neck of the flask using vacuum grease and clips. The remaining two necks of the flask were sealed with greased rubber septa for temperature probe access and hexane injection, respectively. The flask was then placed in a high temperature heating mantle (HORST GmbH) and heated to 473 K for 2 h under vacuum, in order to melt and degas the precursor solution, and to draw off any moisture in the system. Argon gas was then passed through the flask, the vacuum line closed, and the temperature of the solution was raised to 673 K for 24 h to enable the decomposition of the Ge precursor, and the growth of nanowires. During the cooling step 20 mL of hexane was injected at 343 K into the flask. The hexane helps to dissolve the octacosane (m.p. 330-335 K) which

begins to solidify below 333 K. The nanowire product was further purified by centrifugation (7000 rpm for 20 min; 2 × toluene and 2 × ethanol) to ensure maximum removal of octacosane.

2.3. Electron Beam Lithography

2.3.1. Background

Electron beam lithography (EBL) is a technique whereby a beam of electrons is scanned across a substrate covered with a film of resist material which is sensitive to electron beam exposure. Upon exposure to the electron beam, the resist undergoes a chemical change, usually cross-linking or bond breaking, thus resulting in chemical patterning of the resist. The exposed (positive tone resist) or unexposed (negative tone resist) resist can then be removed using an appropriate developer. The ability of electron optics to focus electron beams to nanoscale spots (typically < 10 nm), thus allows nanoscale patterns to be produced on materials using this technique. Figure 2.3 shows a schematic of a cross-section through a typical electron column, including a ray trace of the electrons as they pass through the electron optical components of the system before striking the sample surface. A typical Gaussian EBL system, where the electron beam spot has a Gaussian intensity profile, operates in a very similar fashion to a common SEM or even a traditional cathode ray tube (CRT) television.[3] As such, many EBL systems are manufactured by modification of SEM tools, *e.g.* Raith GmbH. In Gaussian EBL systems, the pattern to be exposed on a sample is produced dynamically, using the combination of a beam blanker and a beam deflector. A simple beam blanker consists of parallel, charged plates that are positioned at an intermediate focal point in the electron column, thus allowing high frequency

electrostatic removal of the beam from the electron optical axis. Thus, discontinuous structures can be patterned on the sample.

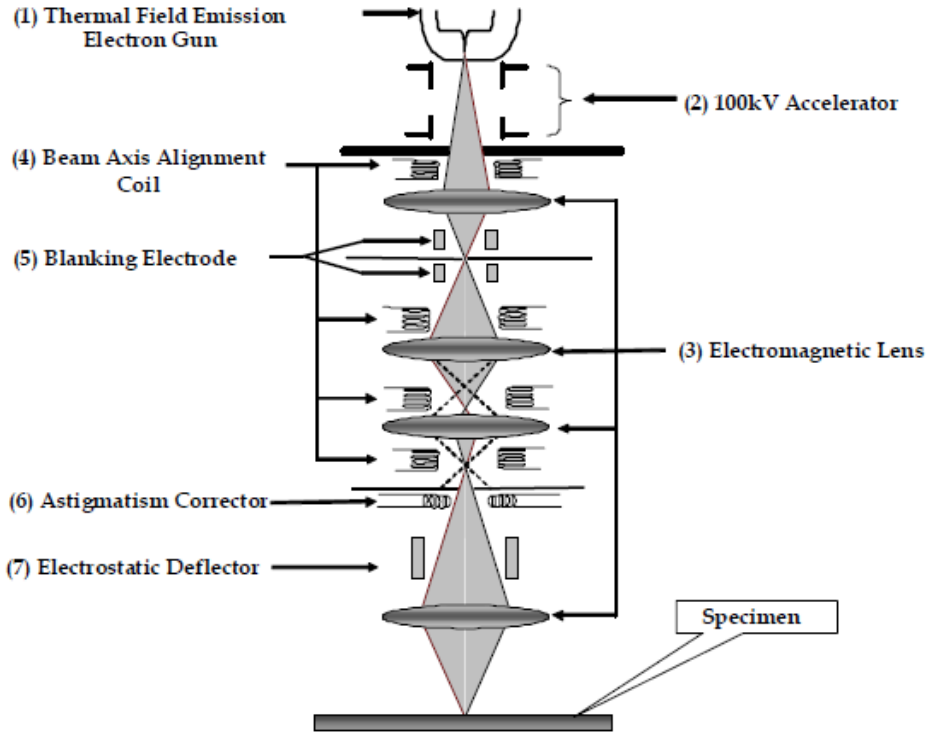

Figure 2.3. Cross-section diagram through an electron column in a typical high energy electron beam lithography system.[4]

The electron beam deflectors are positioned closer to the final lens of the electron column than the beam blanker, allowing greater control over the positioning of the beam as it is deflected. The electrostatic deflectors deflect the beam off-axis creating the desired pattern on the substrate from a computer generated pattern file. However, deflecting the beam off-axis by large angles introduces additional aberrations that cause deterioration of the beam spot. Consequently, pattern files are broken into square write-fields in order to circumvent issues associated with large angle beam deflection. The ultimate resolution of the EBL process scales

with decreasing write-field area at the expense of increased exposure time. Typically square write-fields with areas in the range 2500-10000 μm^2 are used for high resolution EBL. Movement between write-fields is controlled by the sample stage which is usually controlled by a laser interferometer with positioning control to within 1 nm.

Within a write-field, Gaussian EBL systems can scan in one of two modes, raster scan or vector scan as shown in figure 2.4.[4]

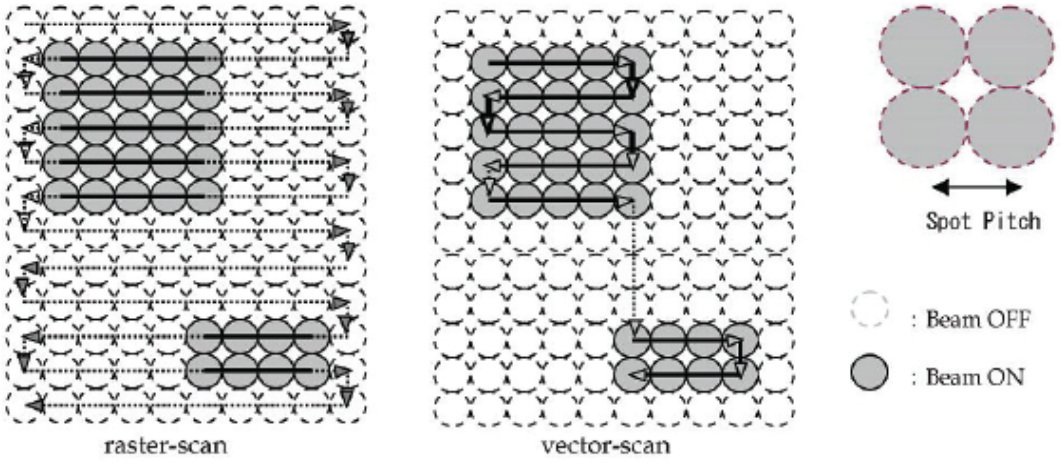

Figure 2.4. Raster scan and vector scan approaches to EBL pattern generation.[4]

Vector scan systems offer significantly increased exposure speeds relative to their raster scan analogues. The area traced by the deflector is significantly less for vector scan systems, as the deflector takes the shortest route between exposed regions.

Electron scattering due to electron-solid interactions is an important factor in high resolution EBL, and especially when a high density of features is desired. When electrons impinge on a solid surface they can experience a number of scattering

events. The various families of electron scattering are discussed in further detail in Section 1.3.2. Figure 2.5 shows a Monte-Carlo simulation of the trajectories of 20 keV electrons (electron energy in a standard CRT TV) scattered in Cu metal.[5] This simulation highlights the relative distances that electrons can travel in solids. The penetration depth of electrons increases significantly with increasing electron energy and decreasing atomic weight of the irradiated material. The intensity of high angle backscattered electrons increases with increasing atomic weight of the substrate material. High angle backscattered electrons are particularly important in EBL, as these electrons contribute most significantly to proximity effects, whereby areas of resist in close proximity to intentionally exposed regions are themselves exposed to backscattered electrons from the substrate. Proximity effects can lead to blurring of structures patterned by EBL resulting in low contrast patterns. Proximity effects are dependent on the area, shape and density of exposed structures, the resist material, the substrate material, the electron energy, and the electron beam spot size.

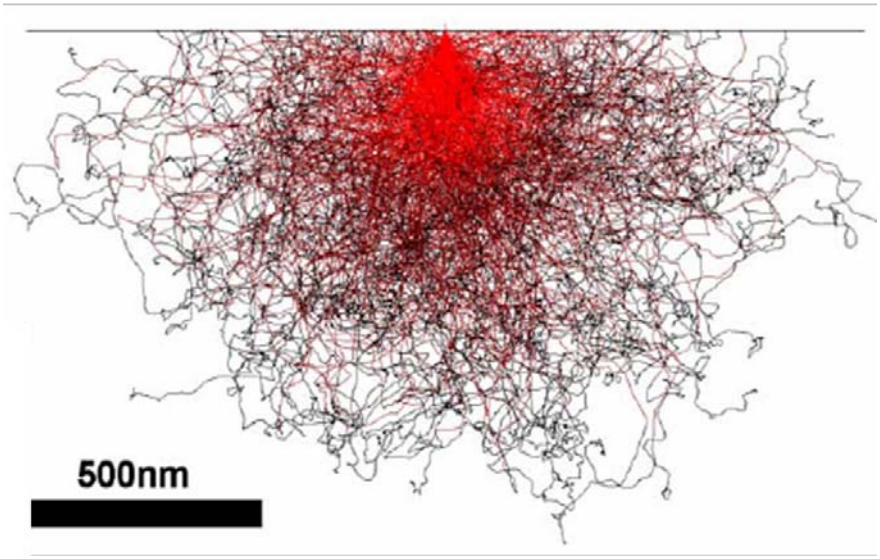

Figure 2.5. Trajectories of 20 keV electrons striking a Cu substrate as modeled by Monte-Carlo simulation.[5]

Careful modelling of the electron scattering within the given materials allows the elucidation of a point spread function (PSF) for the system. PSFs are typically modelled as a sum of two Gaussian functions, where one Gaussian term represents the width of the forward scattered electron distribution (α) and the second represents the width of the backscattered electron distribution (β).[3] A typical PSF given in terms of the distance *r* in the surface plane from the incident beam spot is given in equation 2.1, where η represents the intensity of the backscattered electron energy relative to the forward scattered electron energy.

$$PSF(r) = \frac{1}{1+\eta}\left(\frac{1}{\pi\alpha^2}\exp\left(-\frac{r^2}{\alpha^2}\right) + \frac{\eta}{\pi\beta^2}\exp\left(-\frac{r^2}{\beta^2}\right)\right) \qquad (2.1)$$

Proximity effect correction (PEC) is then achieved by fracturing the designed exposure pattern into regular polygons where each polygon is assigned a relative exposure dose based on the PSF and the location of the polygon within the larger pattern structure. These 'dose maps' can then be superimposed on the desired pattern, thus reducing proximity effects. PEC for example typically assigns higher doses to polygons at the edges of structures than those within the core of a structure, and higher doses to isolated structures than to grouped structures, thus improving the definition and contrast of the pattern.

2.3.2. PMMA Positive-Tone EBL

The most commonly used positive-tone EBL resist is polymethylmethacrylate (PMMA). Typically, PMMA with molecular weights of 950 k or 495 k dissolved

in anisole are used for EBL purposes.[6] The resist is spin coated on a substrate to the desired thickness, typically hundreds of nm. Film thickness can be controlled by adjusting the spin speed and resist solution concentration. The substrate is then baked at a temperature above its glass transition temperature (T_g).[7] Baking serves two purposes, firstly, it removes any residual solvent by evaporation, and secondly, heating the PMMA above its glass transition temperature (T_g = 373 K) allows the PMMA molecules to rearrange, thus releasing stress generated in the film during spin coating. An exposed and developed PMMA film will change its shape if there is any residual stress in the film remaining from the spin coating process.[8] The coated and baked sample is then transferred to the vacuum chamber of the EBL system for exposure. Bond scissions within the polymer backbone in PMMA can occur upon exposure to electrons with energy > 5 eV.[9] However, low energy electrons are impractical for high resolution EBL due to their sensitivity to stray magnetic fields, which prevent fine focusing and formation of a suitably small beam spot. Consequently, electron energies ranging from 1 – 100 keV are typically used for high-resolution EBL. Bond scissions in PMMA break the PMMA molecules up into lower molecular weight subcomponents ($< 2 \times 10^4$ amu.), which can be selectively removed by an appropriate solvent. Mixtures of 4-methylpentan-2-one (MIBK) and propan-2-ol (IPA), or IPA and deionised water, are typically used to dissolve the low molecular weight fragments. These mixtures allow sufficient solubility of low molecular weight PMMA fragments without swelling the remaining unexposed PMMA film.[10]

In this work, a PMMA EBL process was used to define metal gate structures on Si nanowire FETs. A bilayer resist process was used consisting of a low molecular

weight PMMA (MMA), methacrylic acid copolymer film (EL6 Microchem Corp.), topped with a high molecular weight (950 k) PMMA film (A7 Microchem Corp.). MMA/PMMA bilayer resist systems are suitable for preparing nanoscale features by an additive approach as shown in figure 2.6.

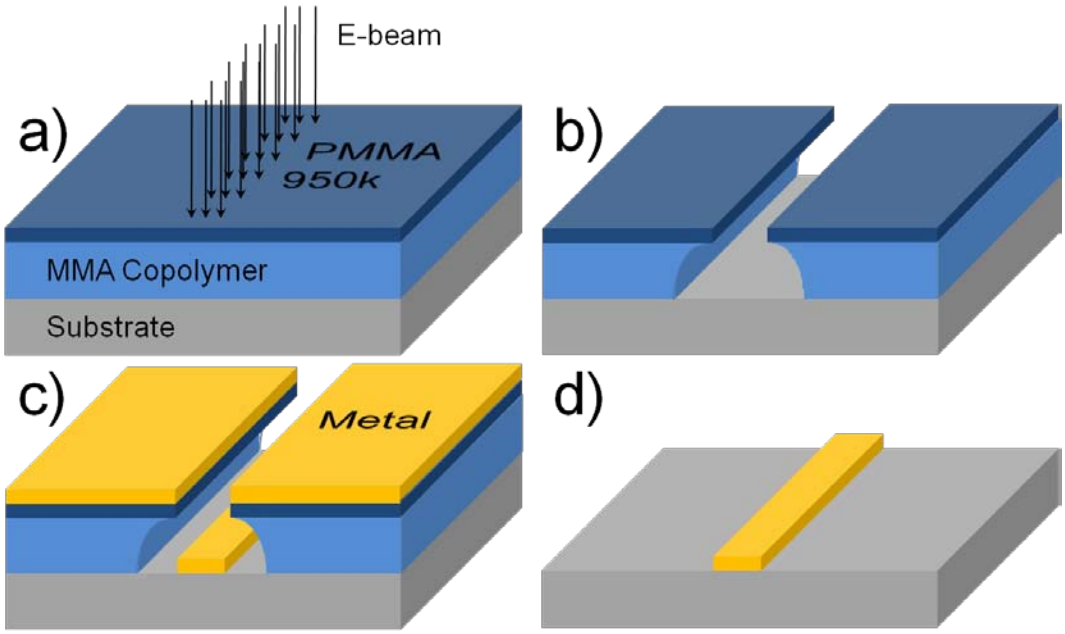

Figure 2.6. Process flow diagram of bi-layer MMA/PMMA EBL process for definition of metal gate structures. a) Electron beam exposure of bilayer resist, b) resist develop, c) metal evaporation and d) lift-off of resist to leave metal structure.

The lower molecular weight of the PMMA molecules in MMA results in a lower required electron dose to fragment these molecules to sizes where they may be removed by the developer. Figure 2.6 shows the pronounced proximity effect in the MMA resist layer relative to the surface PMMA layer. This proximity effect in the MMA layer results in a desirable undercut suited to lift off of nanoscale

metal features. Table 2.1 gives details of the preparation of the MMA/PMMA bilayer resist films for EBL lift-off of Al gate metal on Si nanowire devices.

Table 2.2. Process run sheet for MMA/PMMA bilayer EBL metal lift-off mask

Step	**Description**	**Process Parameters**
1	Substrate dehydration	Bake 5 min, 453 K
2	Substrate cooling	30 s, heat sink
3	MMA coating, 250 nm	10 s 500 rpm, 60 s 1000 rpm
4	MMA baking	2 min, 453 K
5	Substrate cooling	30 s, heat sink
6	2^{nd} MMA coat repeat steps 3-5	As above
7	PMMA 950k coating	10 s 500 rpm, 60 s 1500 rpm
8	PMMA 950k baking	2 min, 453 K
9	Substrate cooling	30 s, heat sink
10	Electron beam exposure	Areal dose 400-500 μC cm^{-2}
11	Develop	90 s, 3:1 IPA:MIBK

Figure 2.7 displays an SEM image of a cross-section through line structures in an MMA/PMMA bilayer after exposure and development. The lines are exposed at different electron doses and as such have different widths, with increasing width representative of increasing dose.

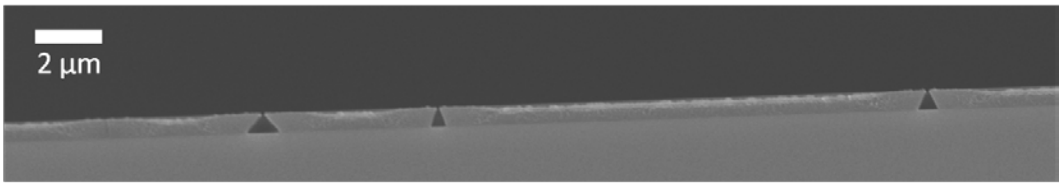

Figure 2.7. A cross-section SEM image through exposed and developed lines in an MMA/PMMA bilyer film. Observed linewidth increases with increasing dose.

Figure 2.8 displays an SEM image of an array of 40 nm wide Al lines prepared using the PMMA/MMA process outlined above. The PMMA/MMA bilayer resist was exposed at an electron dose of 500 µC cm^{-2} and the lines were designed with a width of 20 nm. Al metal was deposited to a depth of 100 nm using a Temescal FC2000 electron beam evaporator.

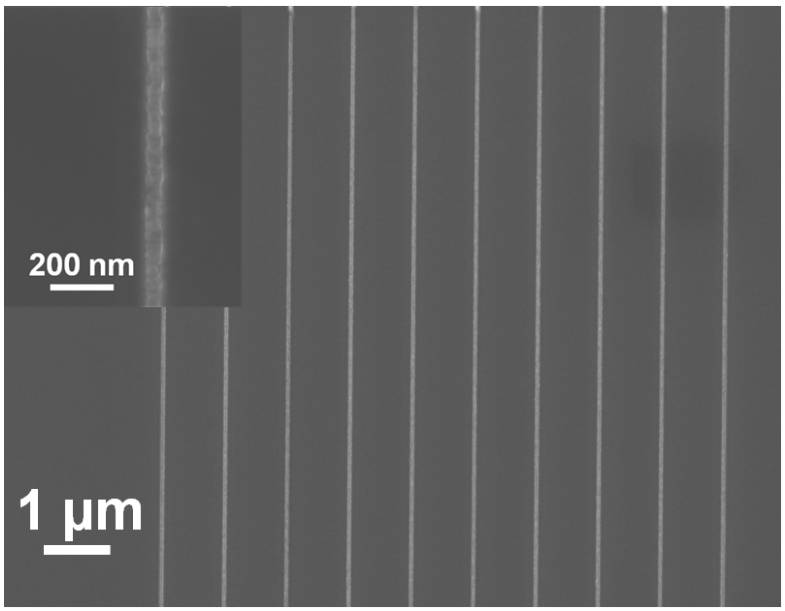

Figure 2.8. SEM image of 40 nm wide Al lines at a pitch of 1 µm fabricated via the PMMA/MMA EBL lift-off process. Inset, a higher magnification SEM image of a single 40 nm wide Al line.

2.3.3. Hydrogen Silsesquioxane Negative-Tone EBL

Hydrogen silsesquioxane (HSQ) is a high resolution, negative-tone, inorganic, EBL resist, which is capable of producing high density features in the sub-20 nm regime.[11,12] Silsesquioxanes have a general chemical formula $(RSiO_{1.5})_n$, where 'R' represents an organic functional group, H in the case of HSQ. The name silsesquioxane is derived from the O:Si ratio of 1.5, where the prefix *sesqui* means one and a half, from the Latin *semisque*, meaning "and a half". HSQ is the smallest member of the polyhedral oligosilsesquioxane (POSS, trademarked by Hybrid Plastics) family, and has a cubic structure of formula $(HSiO_{3/2})_8$. HSQ is an electron beam sensitive material, and upon exposure the cubic HSQ molecules cross-link forming network structures as shown schematically in figure 2.8.[13]

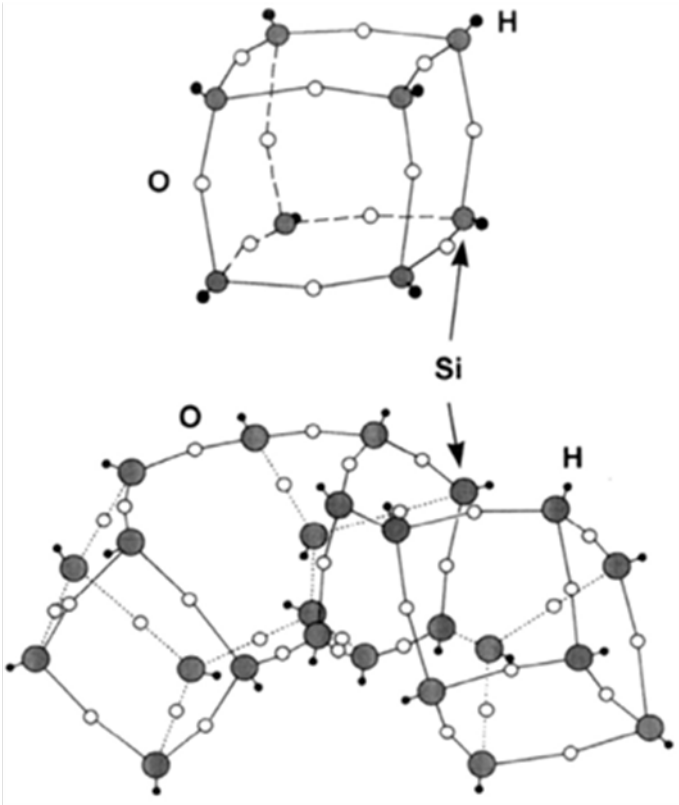

Figure 2.8. Cubic HSQ structure (top), and formation of network structure (bottom).[13]

The degree of HSQ cross-linking can be investigated by Fourier Transform Infrared (FTIR) analysis, as Si-O moieties for both cage and network morphologies can be distinguished.[14] The cross-linking mechanism for HSQ upon electron beam exposure has not been completely verified and as such is still under examination. Electron beam induced desorption studies, using a mass spectrometer coupled to an SEM, have shown that both H_2 and SiH_x are evolved during electron beam exposure of HSQ films. Furthermore, Raman studies show the formation of $=SiH_2$, and $-SiH_3$, groups upon electron beam exposure, whilst Si-O concentration increases. The observed increase in Si-O bond formation and the existence of di- and trihydride species suggests that the redistribution of H within HSQ may be crucial to the cross-linking mechanism. The redistribution reaction can be summarised as given in equation 2.2. Reports suggest that the redistribution reaction arises due to electron beam induced oxygen radical formation, resulting in the formation of Si-O-Si bridges between neighbouring HSQ cubes, thus forming a network structure.[15,16]

$$2HSiO_{1.5} \rightarrow H_2SiO + SiO_2 \qquad (2.2)$$

The observed H_2 and SiH_x evolution can then be attributed to further reaction of H_2SiO groups forming SiH_4 by equation 2.3.

$$3H_2SiO + 6HSiO_{1.5} \rightarrow H_8Si_4O_4 + SiH_4 + 4SiO_2 \qquad (2.3)$$

SiH_4 can then produce H_2 by reaction with water adsorbed on the substrate or water produced via condensation reactions between silanol groups formed in the film during thin film preparation in an ambient environment. SiH_4 can also produce H_2 through electron beam induced ionisation.[17] Another plausible mechanism for the observed H redistribution during HSQ exposure, may involve H sputtering by the incident electron beam. Low energy electrons are capable of sputtering lightweight species such as H and D.[18,19] Electron beam exposure of HSQ is therefore likely to produce H radical and ion species which may subsequently react with neighboring Si groups resulting in the observed H redistribution.

Unexposed HSQ can be removed by a strong aqueous base such as tetramethylammonium hydroxide (TMAH) or NaOH. Nucleophilic attack of the Si atoms in HSQ by the hydroxide ions of the developer results in the formation of silanol groups with the evolution of H_2. The silanol groups are then deprotonated by another hydroxide anion and solvated as a salt of the counter-ion (TMA^+ or Na^+). The salt is soluble in aqueous base and as such can be washed away by the developer solution leaving the exposed cross-linked HSQ structures.[20] The addition of alkali salts such as NaCl to the developer solutions has been found to improve the contrast of the HSQ developer process.[21] The addition of alkali salts increases the alkali cation concentration. Alkali cations such as Na^+ can act as Lewis acids with O atoms in HSQ thus drawing electron density away from the Si-O bond through the O atom, and increasing the relative positive charge on the Si atom. The increased positive charge on the Si atom increases the rate of nucleophilic attack by the hydroxide ion and consequently

increases the rate of development. As a result, HSQ development processes employing the use of an alkali salt often require higher exposure doses than their salt-free analogues.[20]

2.3.4. Ge Patterning

A 15 mm × 15 mm piece of p-doped (P, 10^{17} cm^{-3}) or n-doped (As, 10^{17} cm^{-3}) Ge <100> oriented wafer (Umicore) was first degreased via ultrasonication in acetone and iso-propanol (IPA) solutions (2 × 2 min), dried in flowing N_2 gas and baked for 2 min at 393 K in an ambient atmosphere to remove any residual IPA. Immediately prior to deposition of the HSQ resist layer the Ge surface was Cl terminated. The process used to achieve Cl termination was similar to that reported by *Sun* et al.[22] Firstly, the Ge wafer was immersed in deionised water for 30 s, and then 4.5 M HNO_3 for 30 s followed by drying in flowing N_2 gas for 15 s. The Ge piece was then immersed in a 10 wt. % HCl solution for 10 min. The wafer was then dried in flowing N_2 for 10 s, and spin coated (500 rpm, 5 s, 2000 rpm, 32 s, lid closed) with a 1.2 wt. % solution of HSQ (XR-1541 Dow Corning Corp.) in methylisobutyl ketone (MIBK) to produce a 25 nm film of HSQ. The wafer was baked at 393 K in an ambient atmosphere for 3 min prior to transfer to the EBL system for exposure. The pre-exposure bake served two purposes: (i) the HSQ oligomers in the resist film thermally increase in size due to cross-linking during baking, thus lowering the required electron dose for high-resolution EBL and (ii) baking removes any residual MIBK solvent. Electron beam exposure was performed using a Zeiss Supra 40 FESEM equipped with a Raith Elphy digital pattern generator. All Ge samples were developed in a 0.125 M NaOH, 0.35 M NaCl solution for 30 s followed by a rinse in flowing DI water for 60 s. The

samples were then dried in flowing N_2 gas. A reactive ion etch (RIE) using Cl_2 was performed in an Oxford Instruments Plasmalab 100, to transfer the HSQ pattern to the underlying Ge substrate. Process parameters used for the Cl_2 RIE included a Cl_2 flow rate of 30.0 sccm, radio frequency (RF) power of 80 W, 10 mTorr working pressure, 20 °C chuck temperature, and a 15 s etch time. Furthermore, the sample to be etched was thermally contacted to the stage of the RIE instrument via a thin layer of *Cool-Grease* (Amerasia International Technology Inc.) applied to the underside of the sample.

2.3.5. Bi_2Se_3 Patterning

MBE grown Bi_2Se_3 thin films were produced by Dr. Faxian Xiu at U.C.L.A., CA, U.S.A as described previously.[23] MBE allows production of highly crystalline films on lattice-matched substrates. Prior to HSQ deposition the native oxide on the Bi_2Se_3 films was dissolved by immersing the substrate in an aqueous solution of 0.25 v/v developer/deionised water, 0.023 M TMAH, 0.006 M NaOH, 0.016 M NaCl, for 15 s, rinsed in flowing DI water for 30 s and dried in flowing N_2 gas for 10 s. A 1.2 wt. % HSQ solution was immediately dispersed on the substrate and spin coated as above. The sample was then baked at 393 K in an ambient atmosphere for 3 min prior to transferring to the EBL system for exposure. The sample was developed by manual immersion in an aqueous developer solution of 0.116 M TMAH, 0.028 M NaOH, 0.078 M NaCl for 15 s, rinsed in flowing DI water for 60 s and dried in a flow of N_2 gas for 15 s. The HSQ pattern was transferred to the Bi_2Se_3 film using an Ar^+ reactive ion etch (RIE) in an Oxford Instruments Plasmalab 100. The RIE process used an RF power of 400 W, 30

sccm Ar flow, 100 mTorr working pressure and an etch time dependent on the Bi_2Se_3 film thickness. The etch rate was estimated at 40 nm min^{-1}.

2.3.6. Silicon-on-Insulator Patterning

The substrates used for all nanolithography experiments were silicon-on-insulator (SOI) wafers (SOITEC). The active device layer in the SOI wafer was n-doped (As, 10^{19} cm^{-3}) Si <100>, thinned to a thickness of 13 nm by cyclic oxidation and oxide etching. The active device layer was thermally bonded to a 150 nm buried oxide (BOX) on a <100> Si carrier wafer. The 15 mm × 15 mm dies of SOI wafer used for nanolithography experiments were first degreased via ultrasonication in acetone and iso-propanol (IPA) solutions (2 × 2 min), dried in flowing N_2 gas and baked for 2 min at 120 °C in an ambient atmosphere to remove any residual IPA. The wafer was then allowed to cool on a heat sink for 10 s, and spin coated (500 rpm, 5 s, 2000 rpm, 32 s, lid closed) with a 1.2 wt. % solution of HSQ (XR-1541 Dow Corning Corp.) in methylisobutyl ketone (MIBK) to produce a 25 nm film of HSQ. The HSQ films on SOI were then prepared for EBL in an identical process to that used for Ge and Bi_2Se_3 substrates as detailed above. Exposure doses used to pattern HSQ films on SOI are specified in Chapter 5. Exposed films were developed using an identical process to that used on Ge substrates.

Line edge roughness (LER) measurements of the exposed and developed HSQ lines were performed using *Image J*, image processing software. SEM images of the line structures were processed sequentially as shown in figure 2.9. Typically a line section ~500 nm in length was processed using an SEM image recorded at 10

kV, 140 pA beam current, 6 mm working distance and a magnification of 123300x.

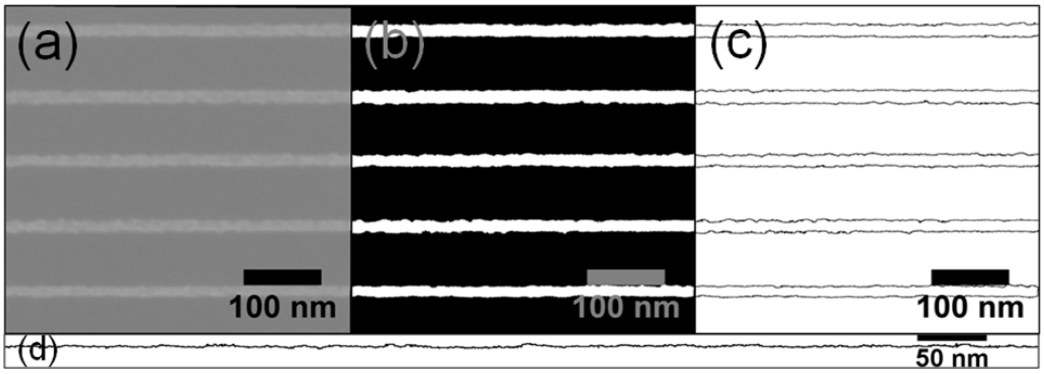

Figure 2.9. Image processing used to obtain LER values from SEM images. (a) Original SEM image. (b) SEM image converted to binary image and (c) edges of lines extracted. (d) Single lines edges were then extracted and plotted as a line graph to determine the standard deviation of the line edge values.

Standard deviation (σ) values were obtained from line plots of individual line edges, averaged for 20 line edges measured and multiplied by three to give the stated 3σ values.

A Cl_2 reactive ion etch (RIE) was performed in an Oxford Instruments Plasmalab 100, to transfer the HSQ pattern to the underlying Si device layer. The RIE process used was identical to that used for Ge (Section 2.3.4.). The HSQ resist was subsequently removed by manual immersion in a solution of 1 wt. % HF for 30 s, and rinsed in flowing DI for 30 s. The HSQ etch process was optimised to allow complete removal of the HSQ resist without significantly etching the BOX layer of the SOI substrate.

A 10 nm Al_2O_3 dielectric layer was then deposited by atomic layer deposition (ALD) to act as a gate dielectric for future FET measurements using the Si nanowires as the active device channel in a transistor architecture without p-n junctions, similar to that described previously.[24] ALD was performed in a Cambridge Nanotech Fiji F200LLC ALD reactor at a deposition temperature of 250°C in Ar carrier gas. Alternating pulses of trimethylaluminium (TMA) and H_2O precursors were used to grow Al_2O_3 layers, with 100 cycles required to prepare a 10 nm Al_2O_3 layer.

2.3.7. Directed Self-Assembly of PS-*b*-PDMS within EBL Defined Channels

20 mm × 20 mm bulk Si substrates, nominal resistivity 0.001 Ω cm, were used for all directed self-assembly (DSA) experiments. The substrates were patterned using a HSQ EBL process prior to deposition of the PS-*b*-PDMS block copolymer (BCP). The substrates were firstly degreased via ultrasonication in acetone and iso-propanol (IPA) solutions (2 × 2 min), dried in flowing N_2 gas and baked for 2 min at 120 °C in an ambient atmosphere to remove any residual IPA. The substrates were then spin coated (500 rpm, 5 s, 2000 rpm, 32 s, lid closed) with a 2.4 wt. % solution of HSQ (XR-1541 Dow Corning Corp.) in methylisobutyl ketone (MIBK) to produce a ~50 nm film of HSQ. The wafer was then baked at 393 K in an ambient atmosphere for 3 min prior to transfer to the EBL system for exposure. Arrays of 15 nm wide lines at pitches of (35n + 15) nm were exposed, where *n* is an integer and $0<n<11$. Following electron beam exposure the samples were developed in an aqueous solution of 0.25 M NaOH, 0.7 M NaCl for 20 s, followed by rinsing in flowing DI water for 60 s. The samples were then blown dry in flowing N_2 gas.

Prior to BCP deposition two approaches were taken to improve PDMS wettability of the surface of the substrates. In both cases the surface was first cleaned with piranha solution (3/1 v/v 98 wt. % H_2SO_4:30 wt. % H_2O_2) for 30 min at 358 K, rinsed with DI water, acetone, and ethanol, and finally blown dry in flowing N_2 gas. The first approach to improve PDMS wettability was to apply a brush layer of monocarbinol terminated PDMS (PDMS-OH) to the substrate. The substrate was first covered with the working solvent, CCl_4, and spun dry to improve adhesion of the PDMS-OH solution. Filtered PDMS-OH was then deposited by spin coating (3000 rpm, 20 s) a solution of 0.5 wt. % PDMS-OH in CCl_4. The substrate was then annealed at 423 K for 15 h under vacuum to facilitate chemical grafting of PDMS-OH to the Si-OH surface. The substrate was then allowed to cool and the excess PDMS-OH was removed by rinsing in chloroform and ultrasonication in toluene at 323 K for 30 min. A second approach to improve PDMS adhesion was to coat the substrate with hexamethyldisilazane (HMDS). HMDS reacts with hydroxyl terminated Si according to the reaction scheme given in equation 2.4.[25]

$$2{\equiv}SiOH + (CH_3)_3Si\text{-}NH\text{-}Si(CH_3)_3 \rightarrow 2{\equiv}SiOSi(CH_3)_3 + NH_3 \qquad (2.4)$$

The reaction scheme given in equation 2.4 yields a trimethysilyl terminated surface. Following PDMS brush or HMDS deposition the substrate surface was partially oxidised using an O_2 RIE in an Oxford Plasmalab 100 using the following parameters: platen power 100 W, chamber pressure 1 mTorr, and O_2 flow rate 40 sccm for 20 s. The O_2 RIE was required to optimise wetting and flow

of the diblock copolymer during BCP deposition and solvent annealing to facilitate DSA.

Following surface treatment of the patterned substrates the PS-*b*-PDMS BCP (34 kg mol^{-1}-b-11 kg mol^{-1}) was deposited according to the following procedure: PS-*b*-PDMS (0.5 wt. % in CCl_4) was spin coated onto the treated substrates (6000 rpm, 20 s) and annealed in toluene vapour for 4-16 h using an apparatus such as that shown in figure 2.10.

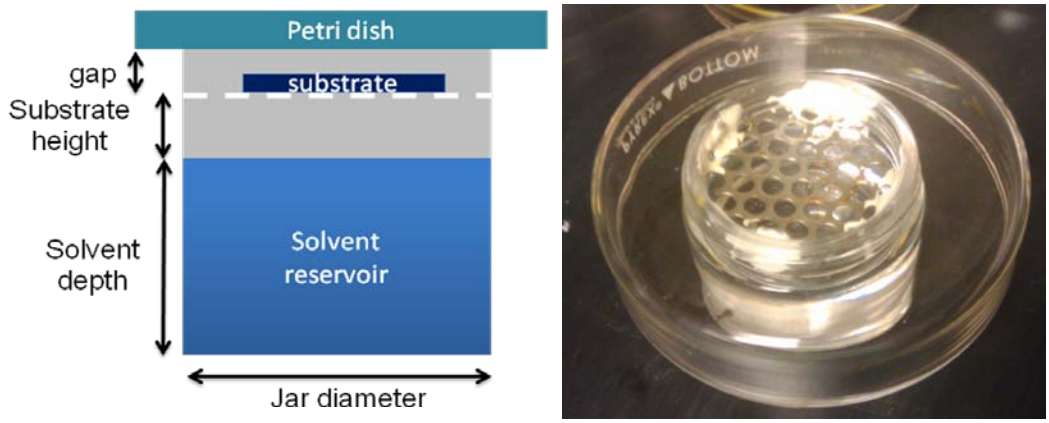

Figure 2.10. Schematic of apparatus used for solvent annealing of PS-*b*-PDMS films (left), and a photograph of the apparatus (right).

Solvent annealing was performed in 5 cm inner diameter glass jar containing toluene. The substrate was placed on a steel mesh sitting 1 cm above the surface of the toluene reservoir and 2-3 mm below the lip of the jar. The jar is capped with a downturned glass petri dish so as to allow a slow leak of toluene vapour. The samples were then etched, anisotropically, in two steps following solvent annealing, as shown schematically in figure 2.11.

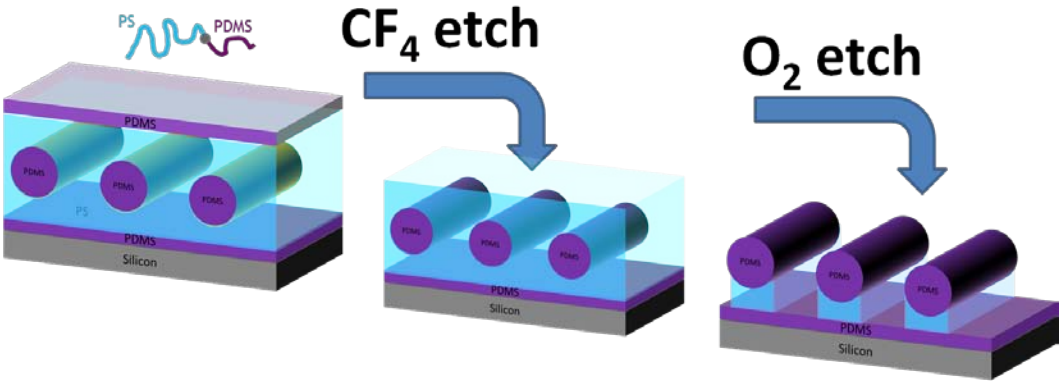

Figure 2.11. Schematic depiction of a microphase separated PS-*b*-PDMS film formed by DSA (left) and subsequent etch process to remove PDMS surface layer (centre) and anisotropic PS etch (right).

The first etch step used a CF_4/O_2 reactive ion etch (RIE) in an STS Advanced Oxide Etcher system to etch the surface PDMS layer. The etch used 100 W platen power, 1 mTorr chamber pressure, CF_4 flow rate of 30 sccm, and O_2 flow rate of 8 sccm for 30 s. The second RIE step to anisotropically etch the PS layer through to the underlying PDMS layer, used the following parameters: platen power 100 W, chamber pressure 1 mTorr, and O_2 flow rate 40 sccm for 20 s.

2.4. Structural Characterisation Techniques

2.4.1. X-ray Diffraction

X-ray diffraction (XRD) is a structural characterisation technique based on the constructive interference of elastically scattered X-rays in a crystal. XRD occurs when the inter-planar distance d in a crystal is of the order of the wavelength λ of the X-ray radiation, usually the Cu K_α emission line with a wavelength of 1.54 Å. Diffraction at an angle θ then occurs when Bragg's law is satisfied. Bragg's law is given in equation 2.5 where n is an integer value.[26]

$$n\lambda = 2d\sin\theta \tag{2.5}$$

A plot of diffraction intensity against angle of reflection (2θ) produces a diffraction pattern from which the crystallographic structure of materials can be determined. X-ray diffraction patterns were collected on a Philips Xpert PW3719 diffractometer using Cu K_α radiation (40 kV and 35 mA) over the range $20 \leq 2\theta \leq 70$, using a step size of 0.0005° and a scan rate of 0.02 s step.

2.4.2. Electron Microscopy

An electron microscope is capable of imaging materials at very high magnifications, > 10^6 times, and at high resolution, < 1 Å.[27] The high resolution capabilities of electron microscopy are due primarily to the very short wavelengths of electrons employed, typically 50 pm – 1 nm for scanning electron microscopy (SEM) and 4 – 15 pm for transmission electron microscopy (TEM). SEM involves rastering a narrow beam of electrons across the surface of a sample to generate an image of that surface through electron solid interactions. As such, SEM can provide analysis of surface topography and subsurface structures to a resolution of ~ 1 nm. Furthermore, the intensity of elastically backscattered electrons depends strongly on the atomic weight of the material with which the electron beam interacts and consequently, can provide information on the composition of the surface material. TEM allows analysis of the bulk structure of thin samples, typically < 100 nm thick. TEM uses higher energy electrons, usually 80-300 keV, with greater penetration depths than those used in SEM. The higher energy electrons can transmit through thin samples generating an image of the bulk structure of the material. Additionally, the shorter wavelength of the high

energy electrons allows improved resolution relative to SEM.[28,29] SEM images were collected on a Zeiss Supra 40 FESEM operating at 10 kV. A JEOL 2000FX TEM operating at an acceleration voltage of 200 kV was used for bright field imaging as well as selective area electron diffraction (SAED). Energy dispersive X-ray (EDX) analysis was performed using an Oxford Instruments INCA energy system fitted to the TEM. High resolution TEM (HRTEM) images were acquired using JEOL 2010 and JEOL 2010F HRTEM instruments operating at 200 kV and an FEI Titan HRTEM operating at 300 kV. High-angle annular dark-field (HAADF) scanning TEM images were collected using a JEOL 2010F HRTEM instrument operating at an acceleration voltage of 200 kV and an FEI Titan HRTEM operating at 300 kV.

Samples of Ge nanowires synthesised in solution and SCF phase experiments were prepared for TEM analysis by ultrasonication of nanowire material in acetone and drop-casting of the nanowire solution onto lacey carbon films on 400 mesh Cu TEM grids. Samples of nanostructures prepared using EBL were prepared for TEM analysis as cross-sections using a standard focused ion beam (FIB) mill and lift-out technique on a FEI Helios Nanolab 600i dual-beam SEM/FIB equipped with an Omniprobe micromanipulator. Figure 2.12 displays an SEM image of a lamella used for TEM analysis of a cross-section through Si nanowires prepared using EBL.

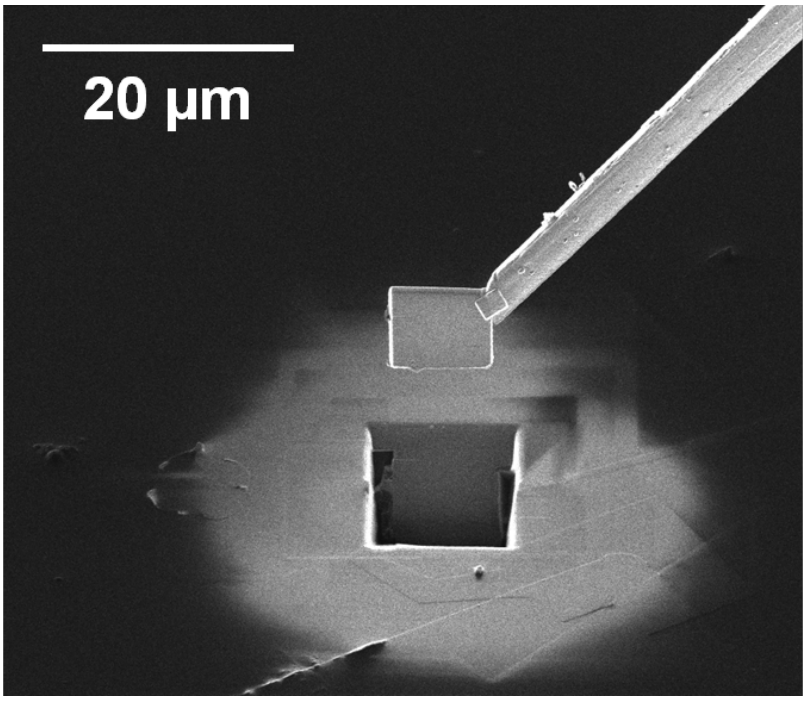

Figure 2.12. SEM image of a lamella extracted from a patterned substrate and attached to the tip of the Omniprobe micromanipulator for transfer to a Cu TEM grid for TEM analysis.

2.4.3. X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) is based on the fact that X-rays have sufficient energy to ionise atoms by removing core level electrons. The kinetic energy of the ejected electrons (E_k) can then be measured at a detector. The binding energy (E_b) can then be determined via the expression in equation 2.6, where $h\nu$ represents the energy of the X-ray photon, and φ represents the work function of the spectrometer.[30]

$$E_b = h\nu - E_k - \varphi \tag{2.6}$$

A plot of E_b against intensity results in an XPS spectrum where peaks arise due to core-level electrons emitted and detected without energy loss due to scattering. These core-level electrons possess characteristic values of E_b inherent to the electronic structure of the atom in the material analysed. The position and relative intensity of these peaks can provide an insight into the chemical composition of the material such as elemental oxidation state, relative elemental concentration and local chemical environment. Electrons can also experience inelastic scattering events prior to detection and these electrons will contribute to the background signal.

XPS is a surface sensitive technique as core-level electrons ejected upon X-ray absorption can travel only short distances before experiencing an inelastic scattering event. This distance is termed the inelastic mean free path and is typically less than 2 nm.[30] XPS analysis was performed on a VSW Atomtech system with twin anode (Al/Mg) X-ray source. Survey spectra were collected at a pass-energy of 100 eV, step size of 0.7 eV and a dwell time of 100 µs. Core-level spectra were acquired as an average of 15 scans at a pass-energy of 50 eV, step size of 0.2 eV and a dwell time of 100 µs.

2.4.4. Fourier Transform Infrared Spectroscopy

Infrared spectroscopy can be used to investigate the presence of different chemical functional groups within materials. Infrared radiation can be absorbed resulting in characteristic rotational and vibrational transitions in different functional groups. The vibrational and rotational transitions manifest themselves as absorption peaks in the infrared spectrum. Infrared absorption spectra can then be used to identify

specific functional groups according to their absorption 'fingerprint'.[31] Fourier transform infrared spectroscopy (FTIR) uses an interferometer to analyse all IR wavelengths simultaneously. The resultant interference pattern can then be converted to a spectrum by a Fourier transformation. FTIR spectra in Chapter 3 were collected on a BioRad FTS-40A FTIR spectrometer at a resolution of 2 cm^{-1}. FTIR spectra in Chapter 4 were collected on a Thermo Scientific Nicolet 6700 FTIR spectrometer with a resolution of 4 cm^{-1} equipped with an attenuated total reflectance (ATR) accessory (Harrick Scientific). The ATR accessory utilised a Ge ATR crystal, and spectra were collected between 650 cm^{-1} and 3000 cm^{-1} using p-polarised light and averaged for 200 scans.

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Chapter 3

Self-Seeded Growth of Sub-10 nm Germanium Nanowires

3.1. Abstract

We report the self-seeded growth of highly crystalline Ge nanowires, with a mean diameter as small as 6 nm without the need for a metal catalyst. The nanowires, synthesized using the purpose-built precursor hexakis(trimethylsilyl)digermane, exhibit high aspect ratios (> 1000) whilst maintaining a uniform core diameter along their length. Additionally, the nanowires are encased in an amorphous shell of material derived from the precursor, which acts to passivate their surfaces and isolate the Ge seed particles from which the nanowires grow. The diameter of the nanowires was found to depend on the synthesis temperature employed. Specifically, there is a linear relationship between the inverse radius of the nanowires and the synthesis temperature, which can be explained by a model for the size-dependent melting of simple cubic crystals.

3.2. Germanium Nanowire Growth

The bottom-up assembly of semiconductor nanowires could potentially lead to the future miniaturization of microelectronic devices.[1,2] Semiconductors which are compatible with current Si processing techniques are of particular interest, in order to minimize the cost and number of processing steps required for their integration into current manufacturing procedures. Si and Ge are examples of two such semiconductors, where Ge offers a number of distinct advantages over Si. For instance, charge carriers in Ge have lower effective masses than in Si

resulting in two important connotations. Firstly, the effective mass of the charge carrier is inversely related to carrier mobility, giving charge carriers in Ge increased mobility relative to Si.[3] Likewise, the exciton Bohr radius is inversely proportional to the effective mass of the charge carrier pair (exciton), implying that Ge will begin to exhibit potentially exploitable quantum confinement properties at larger dimensions (24.3 nm) compared to Si (4.9 nm). However, significant quantum confinement effects will not be observed until dimensions well below these exciton Bohr radii values are achieved. For example, Ge nanowires do not display noticeable quantum confinement effects at diameters above 10 nm.[4]

Gold or similar catalytic colloidal metal particles are generally used to seed the growth of semiconductor nanowires, in accordance with the vapor-liquid-solid (VLS) growth mechanism proposed by Wagner and Ellis.[5] A high solubility of the semiconductor material in the catalytic metal seed is crucial to enable the VLS pathway to crystalline nanowire formation. However, the high solubility of the semiconductor material in the metal seed means that metal atoms are inevitably drawn into the crystalline nanowire matrix, resulting in detrimental effects on the electrical properties of the nanowires.[6] Perea *et al.*[7] have recently made attempts to detect and measure the concentration of dopant metal atoms in semiconductor nanowires introduced by the VLS method.[8]

This work demonstrates for the first time, that high aspect ratio Ge nanowires with mean diameters below 10 nm and lengths up to 20 μm, can be synthesized by bottom-up techniques in the absence of a metal catalyst seed. Instead the nanowires grow directly from liquid Ge droplets within a silicon-based matrix. Few reports of Ge nanowires produced in the absence of a foreign catalytic seed particle exist and none of these studies have produced long, straight, Ge nanowires with mean diameters below 10 nm and a low defect density. Ge *et al.*[9] reported the synthesis of Ge nanowires by the decomposition of the Ge salt $[(CH_3(CH_2)_7CHCH(CH_2)_7CH_2NH_2)_4Ge]^{4+}(Cl^-)_4$, in trioctylamine at 360 °C. They found a correlation between the amount of precursor used in the reaction and the mean diameter of the nanowires obtained (≥ 15 nm as determined using the Scherrer expression), and suggested a VLS-type growth mechanism from liquid Ge droplets. Zaitseva *et al.*[10] reported the synthesis of Ge nanowires from tetraethylgermane, and attributed nanowire growth to a VLS mechanism whereby the liquid seed took the form of nanoscale droplets of high boiling point hydrocarbon material produced from the polymerization of the ethyl radicals liberated during the precursor decomposition process. These nanowires exhibited a broad range of diameters, spanning from 5 to 700 nm. Zhang *et al.*[11] have applied an oxide assisted growth (OAG) technique to synthesize Ge nanowires. The technique, which involves laser ablating Ge in the presence of GeO_2 has been used to produce Ge-GeO_2 core-shell nanowires with core diameters ranging from 6 to 17 nm, and which possess an undulating core-shell interface. Meng *et al.*[12]

have also produced Ge-SiO_x core-shell nanowires with crystalline Ge nanowire core diameters between 30-100 nm. These nanowires were grown by thermal evaporation of SiO and Ge powders, and a combined OAG/VLS growth mechanism was suggested. Ge/SiC_xN_y core/shell nanocables have been synthesized by Mathur *et al.*[13] from $Ge(N(SiMe_3)_2)_2$ using a chemical vapor deposition (CVD) approach. They assumed a self-seeded VLS-type growth mechanism for these nanocables, which had a core diameter of ~ 60 nm. Lastly, Gerung *et al.*[14] have produced kinked Ge nanowires using a Ge^{2+} alkoxide precursor. They suggested two possible growth mechanisms; VLS growth from Ge nanoparticles and self assembly via homogeneous nucleation. The lowest mean nanowire diameter achieved using this approach was 6 nm, with a mean nanowire length of 50 nm. These reports, apart from the OAG method, suggest a VLS growth mechanism for the formation of Ge nanowires. Furthermore, only the work of Gerung *et al.* reports a mean Ge nanowire diameter as low as that reported here. However, these nanowires had low aspect ratios (< 10) and the crystals produced contained many defects.

As stated earlier, a liquid seed droplet is a prerequisite for the VLS growth of Ge nanowires. The aim of this work was therefore, not only to demonstrate the synthesis of Ge nanowires in the absence of a foreign metal seed catalyst, but also to exploit the exaggerated melting point depression of Ge at the nanoscale in order to control the diameter of the nanowires produced. The choice and design of a

suitable precursor is key, in order to prevent aggregation and coarsening of Ge nanocrystals resulting in undesirable microparticles. In addition, the selection of an appropriate synthesis temperature is essential to optimize the quality and quantity of the nanowires produced. The temperature chosen must be sufficiently high to allow precursor decomposition, and liberation of Ge atoms, but also be low enough to prevent coagulation of Ge nuclei forming particles of larger diameters. To date, nanowire diameter control has been achieved either through the use of pre-synthesized colloidal seed metal particles[15] or porous substrates which act as templates or moulds for the nanowires.[16,17] This work demonstrates that a pre-synthesized metal seed particle is not required to exert control over the diameter of Ge nanowires. Exploitation of the melting point depression of materials at the nanoscale to control the dimensions of nanowires has previously been suggested.[18,19] However, these suggestions were again made for metal-catalyzed nanowire growth and specifically the use of the depressed Au-Ge eutectic point at the nanoscale to control nanowire diameters.

The nanowires reported here were produced in solution and within a supercritical fluid (SCF) medium using the metalorganic precursors hexakis(trimethylsilyl)digermane ($Ge_2(TMS)_6$) and tris(trimethylsilyl)germane ($HGe(TMS)_3$). The nanowires were sheathed in a layer of amorphous material, composed of Si, C, O and Ge. This shell is representative of the decomposed precursor material that did not form Ge nanowires, and acted to passivate the

nanowires. This work follows on from the previous report made by our group on the growth of Ge/SiO_x, core/shell nanocables, from $Ge_2(TMS)_6$ via gold and nickel-catalyzed VLS growth.[20] The gold and nickel catalyzed nanowires were found to grow faster and with larger diameters than those grown from $Ge_2(TMS)_6$ in the absence of such metal seeds.

3.3. Results

A selection of TEM and STEM micrographs of Ge nanowires grown at each of the synthesis temperatures employed in this work are shown in figures 3.1-3.4. Many of the nanowires shown in figures 3.1-3.4 exhibit a core-shell morphology, with a highly crystalline Ge nanowire core of uniform diameter, and a non-uniformly thick, amorphous shell material. The Ge nanowire core is typically less than 20 nm in diameter for all synthesis temperatures employed.

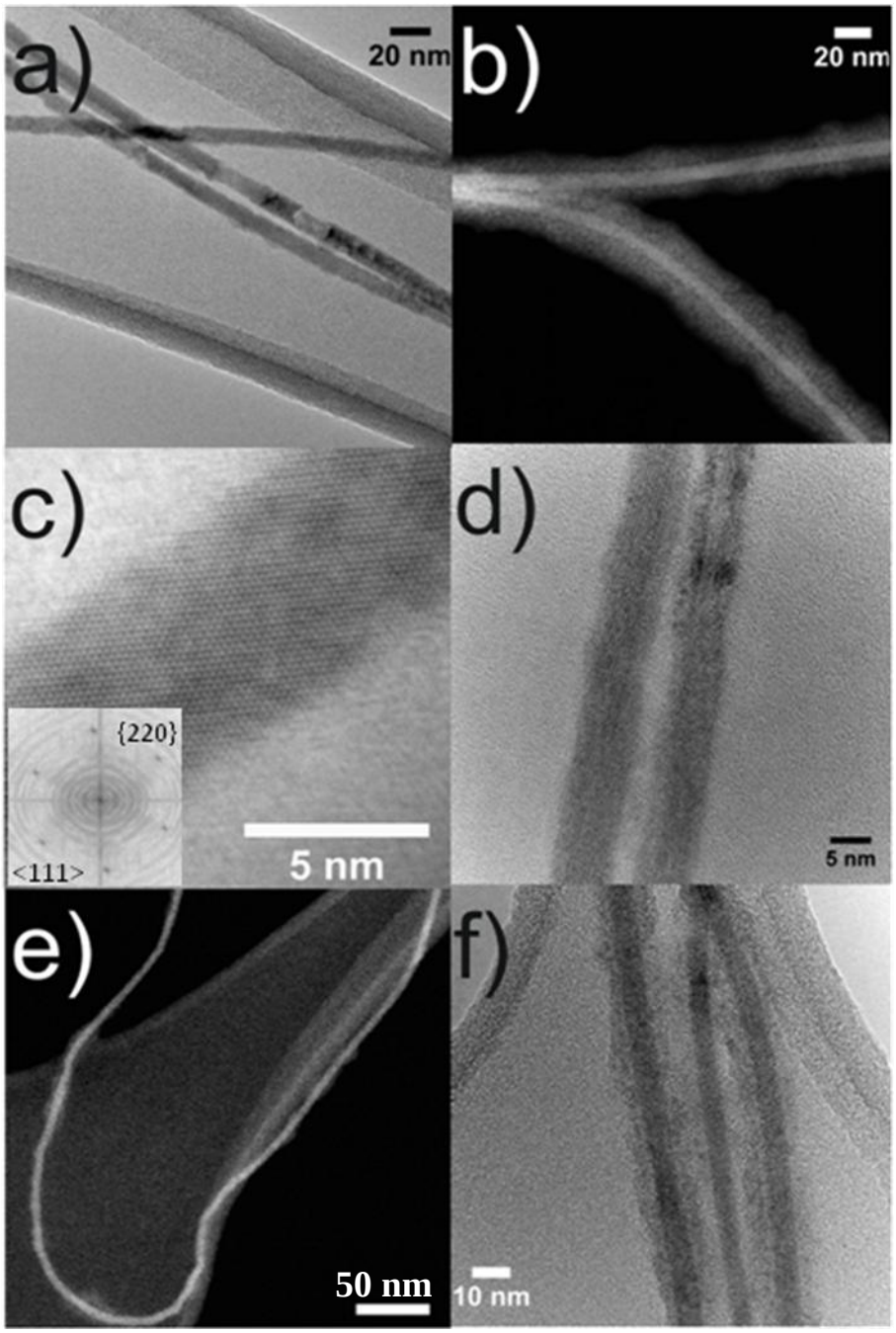

Figure 3.1. a), c), d) and f) bright field TEM micrographs of Ge nanowires synthesised at 573 K. b) and e), HAADF STEM micrographs of Ge nanowires synthesised at 573 K showing the Z contrast difference between the Ge nanowire

core and the Si-based shell. Inset (c), FFT pattern obtained from nanowire in (c) showing the <110> growth direction.

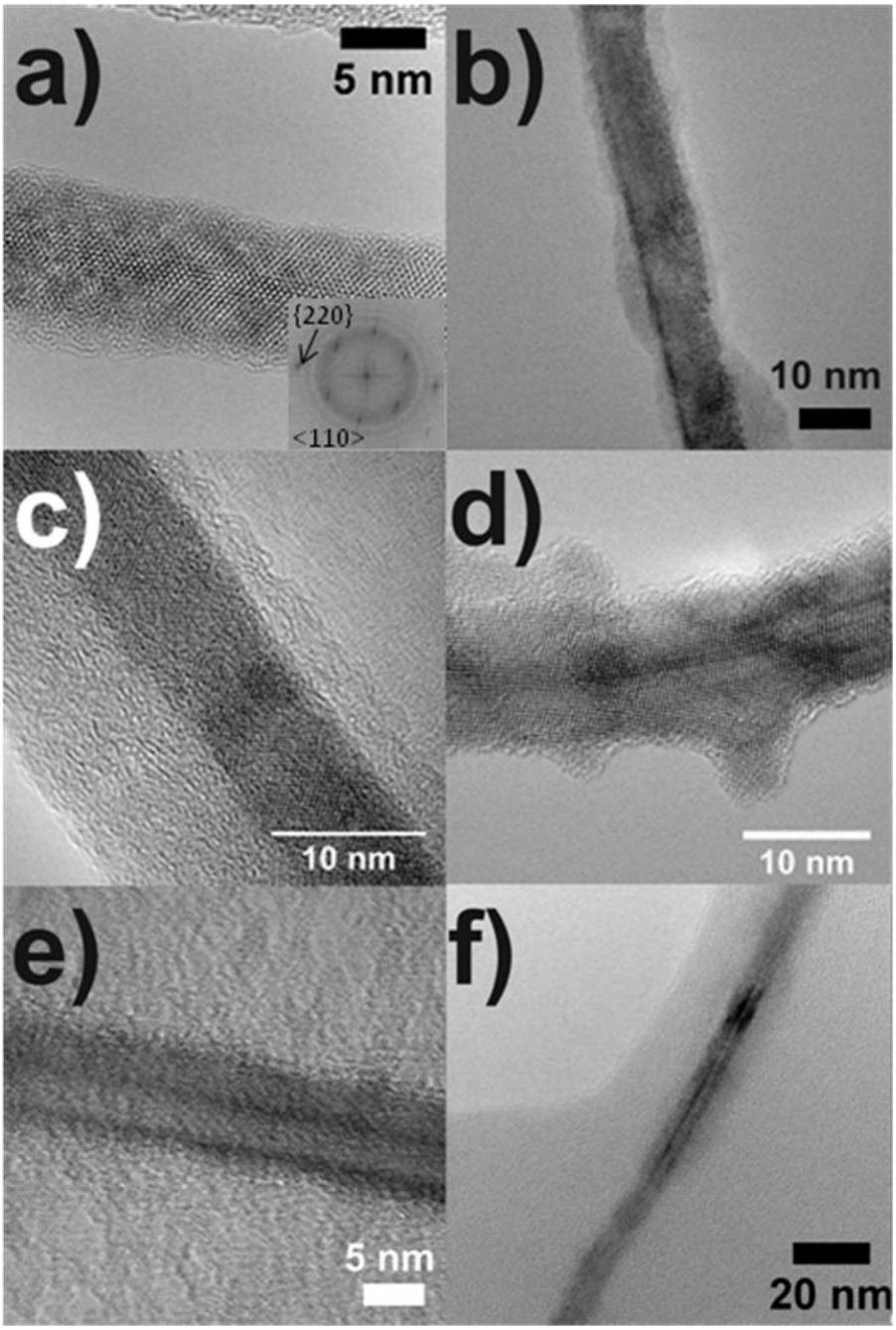

Figure 3.2. a-f) Bright-field HRTEM micrographs of Ge nanowires synthesised at 673 K. Inset (a), FFT of Ge nanowire in (a) indicating <110> growth axis.

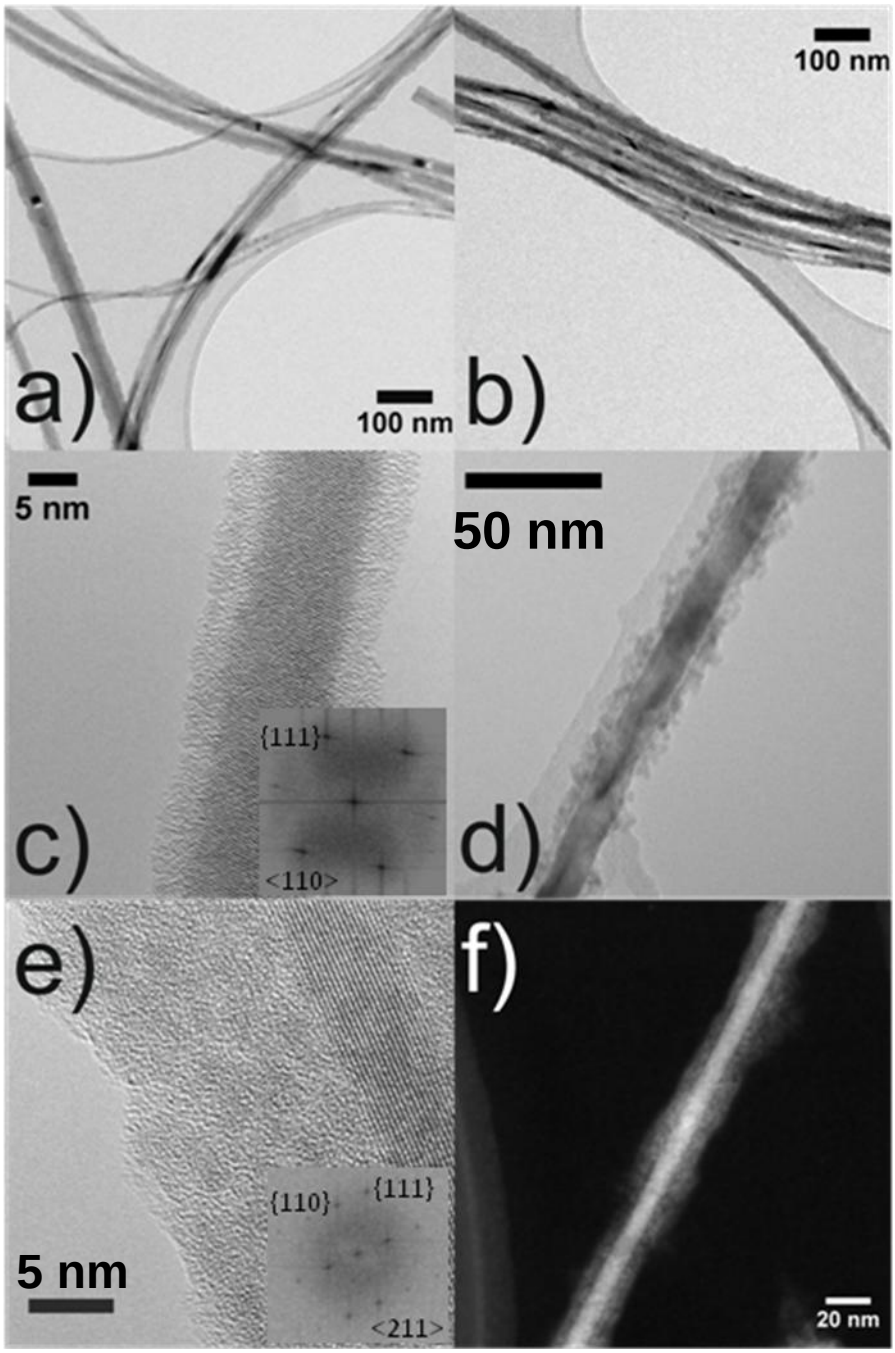

Figure 3.3. a-e) Bright-field TEM micrographs of Ge nanowires synthesised at 523 K. f) HAADF STEM micrograph of a Ge nanowire synthesised at 523 K showing the Z contrast difference between the Ge nanowire core and the Si-based shell. Inset in (c) and (e) are FFT patterns generated from the TEM images of the

nanowires in (c) and (e) respectively. <110> growth directions for both nanowires can be inferred from the FFT patterns.

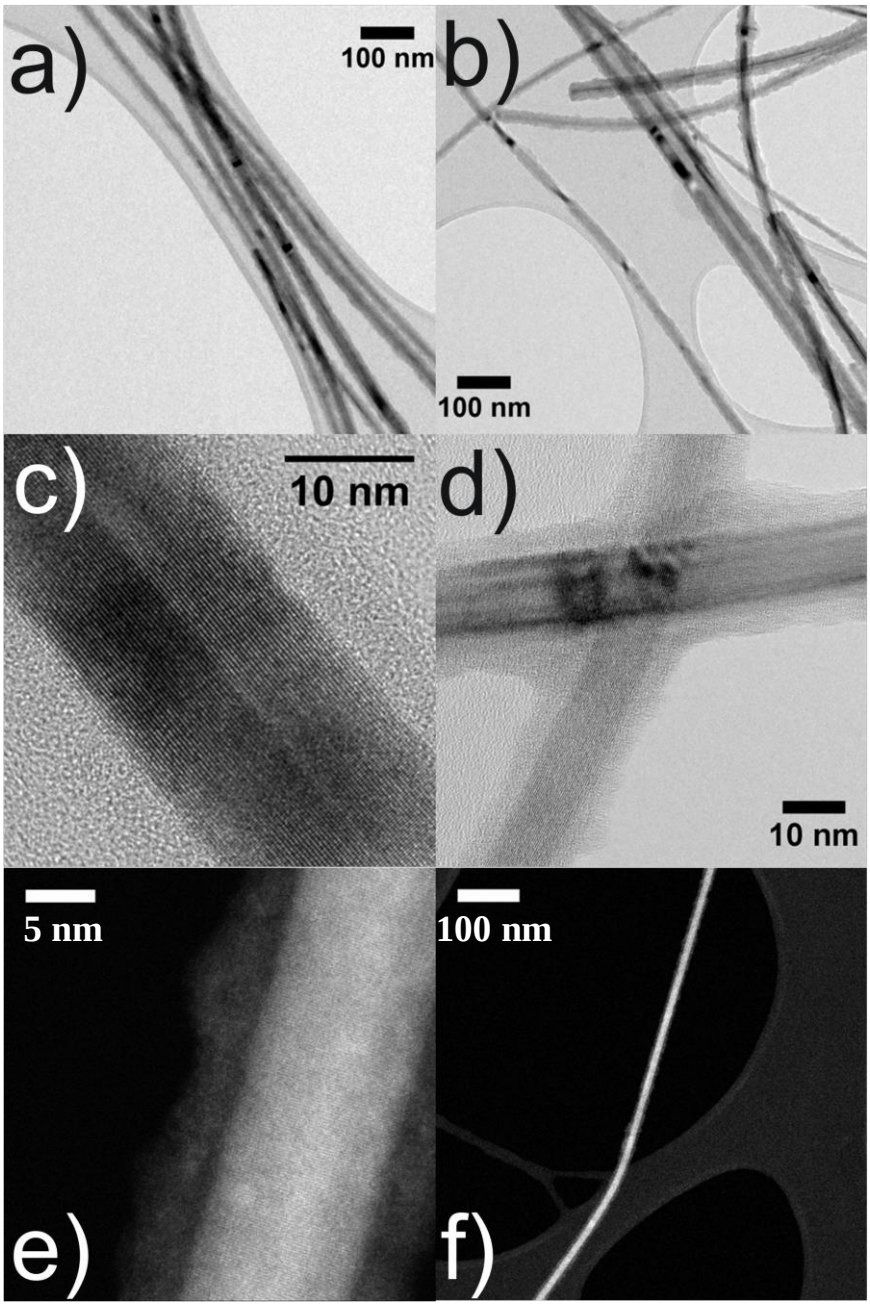

Figure 3.4. a-d) Bright-field TEM micrographs of Ge nanowires synthesised at 5573 K. e) and f) HAADF STEM micrographs of Ge nanowires synthesised at

573 K showing the Z-contrast difference between the Ge nanowire core and the Si-based shell.

TEM analysis of the nanowires produced in this work revealed a relationship between the chosen synthesis temperature and the diameter distribution of the Ge nanowires produced from $Ge_2(TMS)_6$. This relationship is highlighted in figures 3.5 and 3.6.

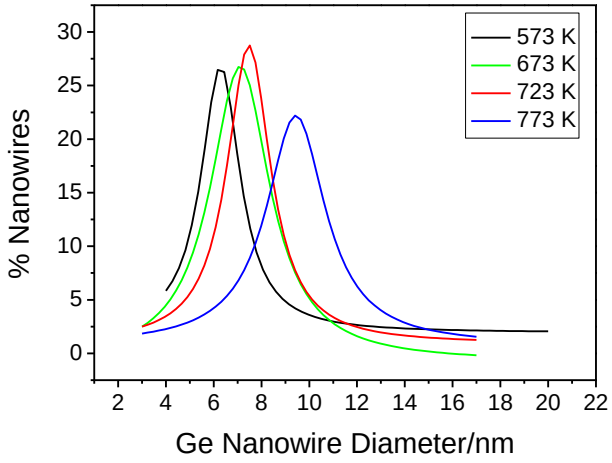

Figure 3.5. Lorentzian Ge nanowire diameter distributions obtained at four different synthesis temperatures. The centers of the distributions are 6.3 nm, 7.1 nm, 7.5 nm, and 9.4 nm for temperatures of 573 K, 673 K, 723 K and 773 K respectively.

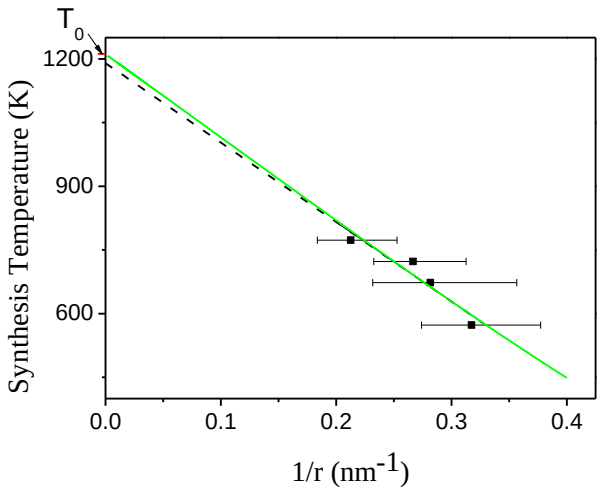

Figure 3.6. Plot of synthesis temperature against the inverse of the corresponding nanowire radius. The four data points from this work are highlighted. Error bars represent the full width at half maximum (FWHM) of the Lorentzian fits in figure 3.5. The dashed line represents a linear regression of these four points, extrapolated to intercept the y-axis. The green trace represents the theoretical melting point at the nanoparticle-nanowire interface in a VLS grown Ge nanowire by the Lindemann model. The bulk melting point of Ge (1211 K) is clearly marked on the y-axis.

Figure 3.5 shows a plot of the percentage of nanowires obtained with a given diameter for each of the four synthesis temperatures employed. Each trace in this plot represents a Lorentzian fit to the raw data which was obtained by direct measurement of the nanowire diameters using TEM. A Lorentzian model was found to display the best overall fit to the raw nanowire distribution data shown in figure 3.7 when all temperatures were considered. However, a change in the shape of the nanowire diameter distribution curve with increasing temperature

should not be discounted. For example, a log-normal model shows slightly improved fitting when applied to the distributions obtained from lower synthesis temperatures (R^2 = 0.94 at 573 K, R^2 = 0.93 at 673 K). R^2 values for a Lorentzian model are shown in the caption for figure 3.7. Application of a log-normal model to the data in figure 3.7 does not however, result in a change in the centres of the obtained distributions. A distinct increase in the centre of the Lorentzian distribution was observed as the synthesis temperature increased. The observed relationship between temperature and nanowire radius is indicative of a thermally controlled nanowire growth process.

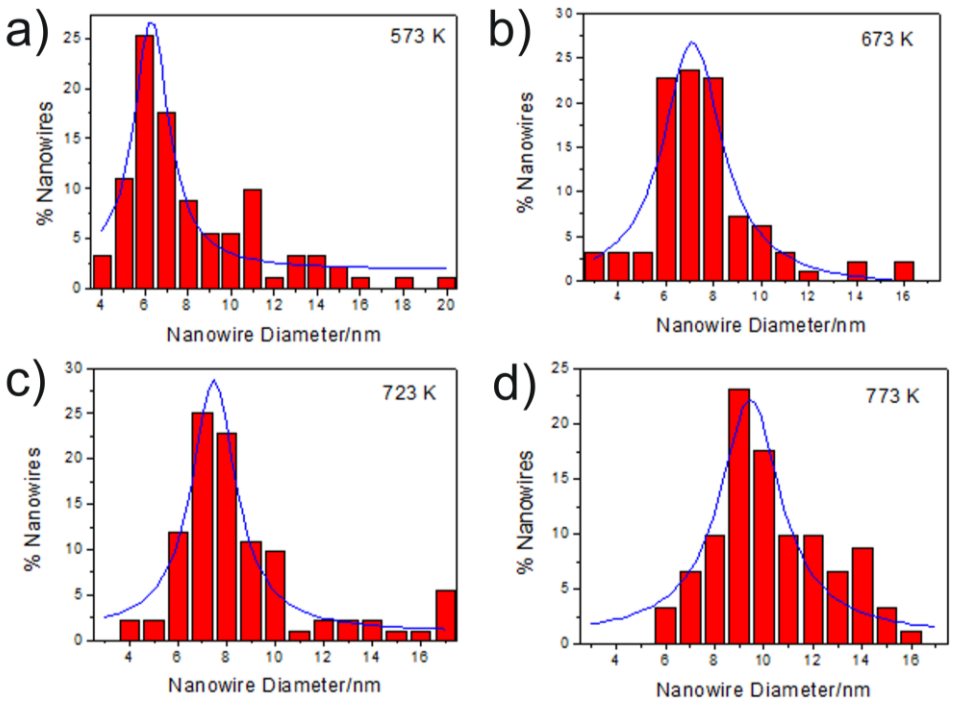

Figure 3.7. A plot of percentage of Ge nanowires measured against Ge nanowire diameter for synthesis temperatures of 573 K, 673 K, 723 K and 773 K. The blue trace represents a Lorentzian fit to the data. (a) 91 nanowires were measured by

TEM. Lorentzian curve centred at 6.3 nm (R^2 = 0.90) and has a FWHM of 2.0 nm. (b) 97 nanowires were measured by TEM. Lorentzian curve centred at 7.1 nm (R^2 = 0.91) and has a FWHM of 3.0 nm. (c) 92 nanowires were measured by TEM. Lorentzian curve centred at 7.5 nm (R^2 = 0.93) and has a FWHM of 2.2 nm. (d) 91 nanowires were measured by TEM. Lorentzian curve centred at 9.4 nm (R^2 = 0.86) and has a FWHM of 3.0 nm.

Since its conception in 1910 the Lindeman criterion has been shown to accurately describe the melting of simple metals, *i.e.* close-packed arrangements of atoms.[21] Central to the Lindemann criterion is the relationship between the root-mean-square thermal average amplitude of vibration of an atom in a crystal, and temperature. The criterion states that when the amplitude of vibration of an atom in a material reaches a threshold value, melting ensues. This threshold value for the vibrational amplitude is ~ 10 % of the mean interatomic separation in that material. Melting is known in many cases to initiate at the surface of materials where separation of atoms differs significantly from that within the bulk.[22] Nanoscale materials such as nanowires and nanoparticles exhibit a high surface to volume ratio, and as such can be expected to melt at lower temperatures than their bulk counterparts. Recently, a model has been derived to describe the relationship between the melting temperature and particle size based on the Lindeman criterion,[23] as represented by equation 3.1 where T_r and T_0 are the melting points of the nanocrystal and the bulk material respectively, r_0 represents the critical

radius at which all of the atoms of the nanocrystal are at the surface, r denotes the particle/wire radius, R is the ideal gas constant, and S_m is the bulk melting entropy (31.1 $JK^{-1}mol^{-1}$ for Ge).[24]

$$\frac{T_r}{T_0} = \exp\left(-2\frac{(S_m - R)}{3R(r/r_0 - 1)}\right) \tag{3.1}$$

The critical radius r_0 can be determined from the expression, $r_0 = (3 - d)(6\Omega/\pi)^{1/3}$, where d denotes the dimension of the solid (d = 0 for nanoparticles, d = 1 for nanowires and d = 2 for thin films), and Ω denotes the volume per atom in the bulk solid material. The choice of an appropriate value of r_0 for the nanowires produced in this work requires a number of considerations. If we assume a supercritical fluid-liquid-solid (SFLS) or solution-liquid-solid (SLS) growth mechanism for the nanowires, the Ge nanoparticles should preferentially exist in a liquid state at the synthesis temperature to act as seeds for the SFLS/SLS growth of Ge nanowires. Furthermore, the nanowires produced must be sufficiently large in diameter to exist as a solid at the synthesis temperature. It is well known that the interface between a solid wire and a liquid particle is important in the VLS growth of nanowires, and ultimately that it can determine the diameter of the nanowires formed.[25] Given that during the VLS growth of a Ge nanowire from a Ge seed, where the seed particle is in the liquid state and the nanowire is in the solid state, the interface of the wire and seed must be exactly at the melting point, *i.e.* at the phase boundary between liquid Ge and solid Ge. Therefore, the value of r_o chosen must lie between that of a nanowire (r_o = 0.702 nm) and that of a

nanoparticle (r_o = 1.053 nm). The value of r_o used here was 0.88 nm, midway between that of a nanoparticle a nanowire. The solid trace in figure 3.6 represents a plot of T_r against 1/r using the model outlined above. The model is pseudo-linear for the range of values of 1/r shown in figure 3.6. The plot intercepts the y-axis at 1211 K, the bulk melting temperature of Ge. The dashed trace represents a linear fit to the four mean radii obtained from the plots in figure 3.5, and correlates well with the model described herein.

A distinct increase in the diameter distribution with increasing temperature is also apparent from the data shown in figure 3.5. The full-width at half maximum (FWHM) of the Lorentzian distribution of diameters for nanowires synthesized at 573 K was 2.0 nm, compared to a FWHM value of 3.0 nm for nanowires produced at 773 K. The broader distribution at 773 K may be attributed to two factors. Smaller diameter wires may form at temperatures below 773 K as the room temperature precursor solution is injected into the reactor. Also, larger diameter wires may form by a solid-phase seeding mechanism as larger Ge particles would exist in the solid phase at 773 K.

Figure 3.8 (a) shows a TEM micrograph of a typical Ge nanowire grown at 773 K from $Ge_2(TMS)_6$ using the high pressure method outlined above. This micrograph clearly shows the core-shell morphology of the nanowires produced at these temperatures, as observed by the contrast difference between the dark Ge core,

and the lighter amorphous shell. The nanowire has a 10 nm diameter, crystalline Ge core. Figure 3.8 (c) (inset) shows a higher magnification HRTEM micrograph of a similar 10 nm diameter nanowire with a 3 nm thick shell. This HRTEM micrograph was recorded along the <111> zone axis of the crystalline nanowire. Figure 3.8 (b) displays a FFT image of figure 3.8 (c) and highlights the low defect density present in the Ge nanowire core. A <211> crystal growth direction can be inferred from the FFT of the HRTEM micrograph. The Ge nanowires produced in this work generally exhibit <110> growth directions, whilst approximately 25 % of the nanowires analysed were oriented along the <211> crystal axes. No <111> oriented nanowires were observed amongst the nanowires produced in this work. This observation is consistent with reports on the diameter dependent growth direction of Si nanowires produced by CVD using Au catalyst. Schmidt *et al.*[26] found that growth of <110> oriented Si nanowires is more prevalent than growth of <211> or <111> oriented nanowires, for nanowires less than 20 nm in diameter. Given that Si and Ge share the same crystal symmetry, a similar size-dependent nanowire growth direction may be expected for Ge.

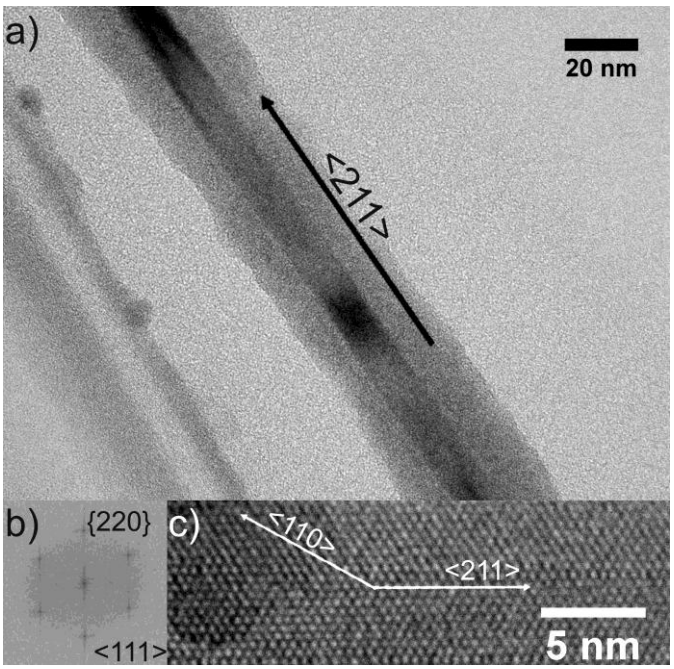

Figure 3.8. (a) TEM micrograph of a typical nanocable synthesized at 773 K, showing the distinct core-shell morphology. (b) Inset, a fast Fourier transform (FFT) of the HRTEM image in (c), highlighting a low defect density in the crystalline Ge nanowires, (c) HRTEM micrograph of a similar 10 nm diameter Ge nanowire to that shown in (a). The image was obtained along the <111> zone axis of the Ge nanowire.

Figure 3.9 displays a SEM micrograph highlighting the high density of nanowires produced using the methods outlined above. The SEM micrograph also emphasizes the high aspect ratio of the nanowires produced. Inset in figure 3.9 is a HAADF STEM micrograph of three Ge nanowires produced at 673 K. The distinct contrast difference between the Ge nanowire core and the amorphous Si-based shell emphasizes the core-shell morphology of the nanowires. The image

also highlights the uniformity of the core diameter relative to the shell thickness. Hence, whilst the amorphous shell is non-uniform in thickness the core diameter remains uniform along the length of the nanowires.

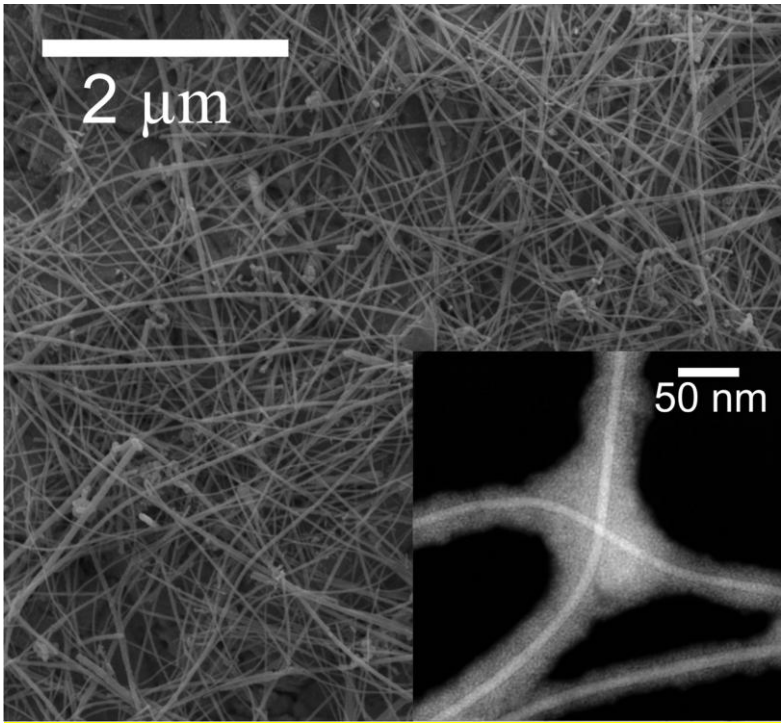

Figure 3.9. A SEM micrograph of the Ge nanowires produced in this work. Inset is a HAADF STEM micrograph of Ge nanowires synthesised at 673 K, clearly displaying the core-shell morphology of several Ge nanowires. Including shell, the nanowires shown are 20 to 50 nm in diameter, whilst the cores are 8 to 10 nm in diameter and show good uniformity along the wires.

An XRD pattern of a sample of these nanowires is shown in figure 3.10. The most intense reflections can be indexed to cubic Ge (JCPDS, reference pattern 04-0545, space group *Fd3m*). The broad reflections are characteristic of the

nanoscale dimensions of small diameter nanowires and minor Ge nanoparticle by-products. The broad hump in the baseline of the XRD pattern between 40 and 60 °2θ could be attributed to the amorphous Si-based matrix present in the nanowire sample. This Si-based by-product has been investigated by EDX and TEM, and was found to be composed of Ge, Si, C, & O. SAED of some of the smaller particulate by-product revealed that the material was largely amorphous in nature although it did have some polycrystalline component. The polycrystalline component could be attributed to Ge nanoparticles present within an amorphous matrix.

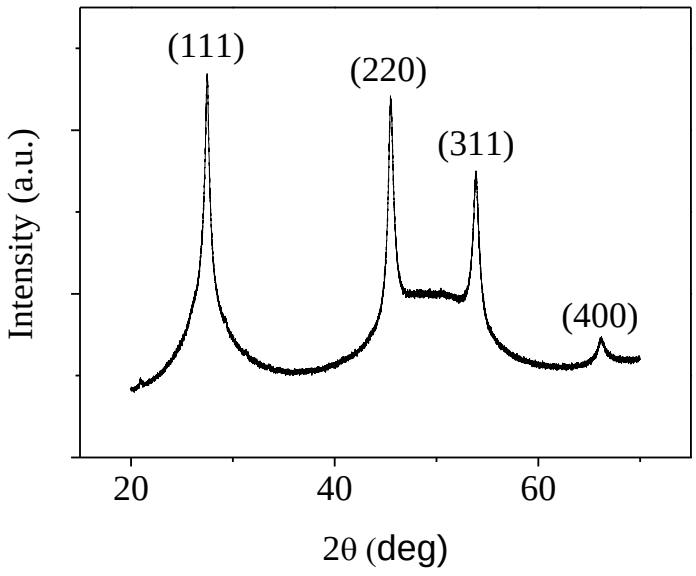

Figure 3.10. PXRD pattern of a sample of Ge nanowires synthesized at 673 K. All reflections can be indexed to cubic Ge (JCPDS, reference pattern 04-0545, space group *Fd3m*). The broad hump in the background observed between the (220) and (311) reflections is due to amorphous Si-based material present in the sample.

The shell of the amorphous material found on Ge nanowires produced at higher temperatures was investigated by EDX analysis. Three 8 nm diameter nanowires with different shell thicknesses (5 nm, 10 nm, and 20 nm) were examined. EDX revealed Si/Ge atomic ratios of 4.0, 4.5 and 5.5 for the wires with 5 nm, 10 nm and 20 nm shells respectively. This investigation suggests that the amorphous shell is largely composed of Si. However, the Si/Ge ratio would be expected to increase more significantly if the shell was purely amorphous Si or SiO_2, suggesting that Ge or C are also present. Furthermore, FTIR analysis of a sample of nanowires produced at 723 K (figure 3.11) revealed strong Si-O vibrational modes at 460 cm^{-1}, and 1080 cm^{-1}. Weaker Si-O vibrational modes were also observed at 565 cm^{-1}, 798 cm^{-1}, and 1153 cm^{-1}. The broad peak at approximately 1225 cm^{-1} could be attributed to a Si-O-C vibrational mode. The weak peak at 1489 cm^{-1} may be attributed to a Si-CH_2 scissor mode and the other weak peaks at 2855 cm^{-1} and 2927 cm^{-1} can be assigned to the vibrational modes of alkyl groups.[27,28] The FTIR data tentatively suggests that the trimethylsilyl (TMS) groups in the precursor are partially decomposed during the synthesis process. The weak Si-CH_2 and alkyl vibrational modes suggest that some of the TMS groups remain intact following nanowire synthesis, but, the intense Si-O vibrational modes suggest that many of the TMS groups decompose to produce Si which is subsequently partially oxidized by reaction with trace levels of water present in the system. The composition of the shell material coating the Ge nanowires cannot be stated conclusively as the FTIR spectrum was recorded for

all the material present in the sample which includes Ge nanowires coated in an amorphous shell, as well as the particulate by-product.

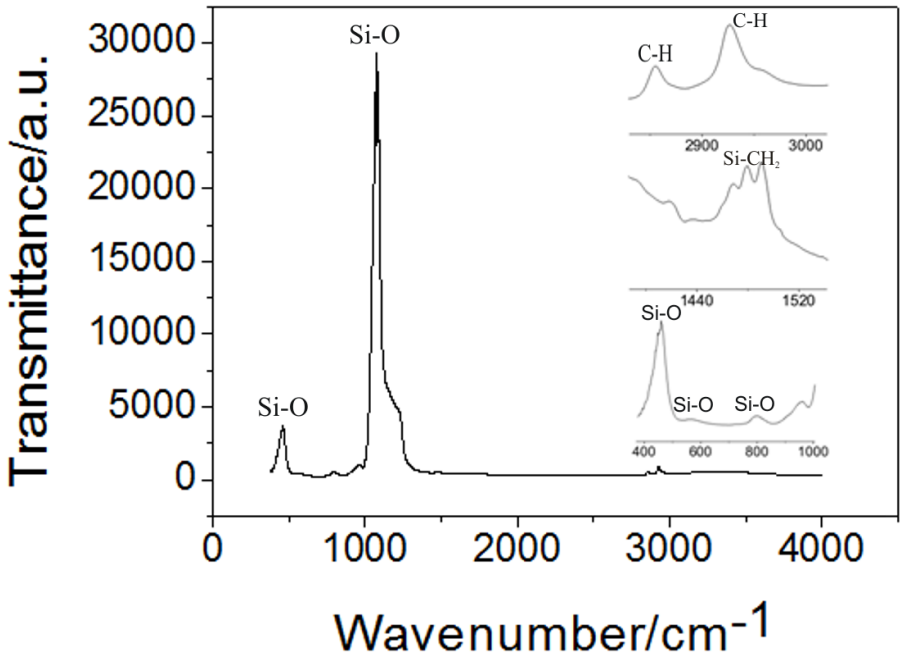

Figure 3.11 FTIR spectrum of a sample of Ge nanowires produced from $Ge_2(TMS)_6$ at 450 °C. Inset, magnified views of weaker absorption bands.

Experiments using $HGe(TMS)_3$ as a precursor to generate Ge nanowires were found to require longer synthesis times than those required for $Ge_2(TMS)_6$ to produce an identical nanowire product, although in lower yield. The longer synthesis time, approximately double that required for $Ge_2(TMS)_6$ to produce nanowires, may be attributed to the slower decomposition kinetics of the precursor. However, it is also possible that the evolution of hydrogen upon cleavage of the Ge-H bond in $HGe(TMS)_3$ has an adverse effect on the nanowire growth process. A TEM micrograph of a typical nanowire produced at 673 K

from this precursor can be seen in figure 3.12. The nanowire closely resembles those produced from $Ge_2(TMS)_6$. A Lorentzian fit (R^2 = 0.73, FWHM = 3.0 nm) to a plot of percentage nanowires against Ge nanowire diameter, for these nanowires was centered at a diameter of 7.1 nm. This is in good agreement with the value of 7.1 nm obtained for Ge nanowires produced from $Ge_2(TMS)_6$ at 673 K.

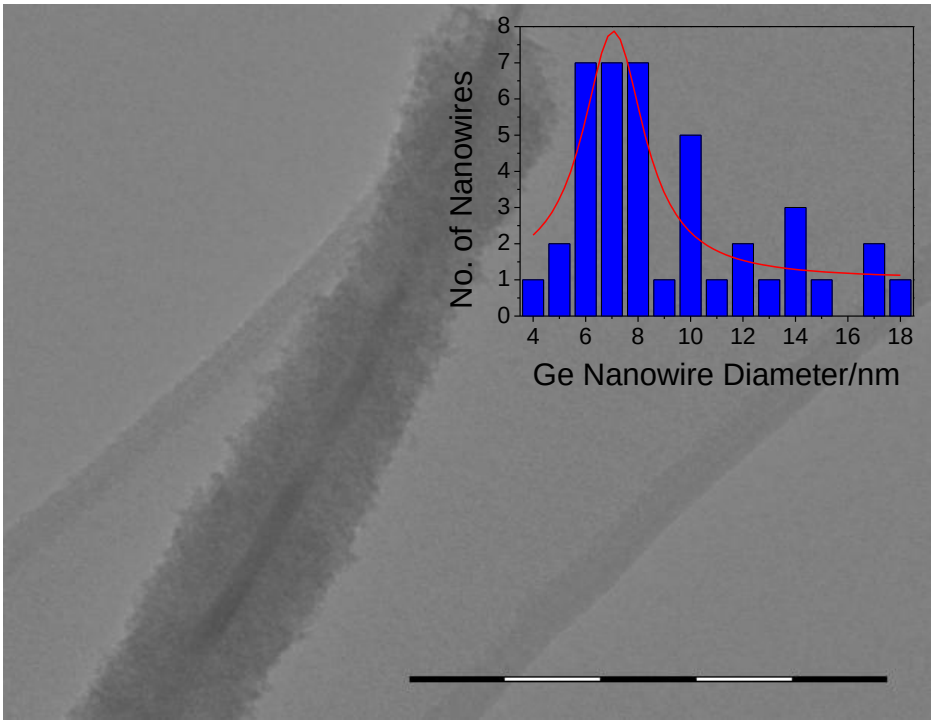

Figure 3.12. A TEM micrograph of a typical nanowire produced from $Ge(TMS)_3$. Scale bar represents a length of 200 nm. Inset, is a bar graph showing the observed diameters of the crystalline Ge nanowire cores as measured by TEM.

In an attempt to clarify the growth mechanism of the Ge nanowires a number of other experiments were performed. Firstly, experiments using synthesis temperatures below 703 K were performed in glassware as described in detail

above, in order to eliminate the possibility of Ge nanowire growth occurring from iron, chromium or nickel in the stainless steel cell walls. These experiments proved to be successful as Ge nanowires were produced with a similar yield and quality to those produced in the higher pressure experiments. An example of a nanowire synthesized at 673 K can be seen in the HRTEM micrograph in figure 3.13 (a). The nanowire is 8 nm in diameter and exhibits a <110> crystal growth direction. Worthy of note here is that the high pressure approach is still required for synthesis at temperatures above 703 K due to thermal limitations of conventional high boiling point solvents (octacosane (b.p. 703 K) and squalane (b.p. 693 K)) thus ruling out a solution phase approach. All glassware was cleaned with aqua regia prior to use in these experiments to remove any trace metals present. Furthermore, the precursor solution was not brought into contact with any metals prior to, or during the nanowire synthesis. Every effort was also made to ensure the absence of impurities in the precursor solution which might induce nanowire growth. Previously, Chockla *et al.*[29] reported the growth of Ge nanowires via the thermal dissociation of diphenylgermane in dotriacontane. Detailed investigations of this process revealed that NaCl impurities were responsible for initiating nanowire growth. However, thermal decomposition of diphenylgermane in each of the solvents used in our study did not produce any nanowires, suggesting that the presence of a Si-based material is crucial to facilitate nanowire growth in the absence of a foreign metal catalyst.

In order to investigate the early stages of Ge nanowire growth from $Ge_2(TMS)_6$, a precursor solution was heated to 573 K for 24 h. The resulting product was composed primarily of large particles from which Ge nanowires, with a mean diameter of approximately 6 nm, protruded. Figure 3.13 (b) shows a HRTEM micrograph of a nanowire synthesized at 573 K. The nanowire does not possess an amorphous coating and has no apparent surface oxide. No seed particles were observed at the tips of the nanowires protruding from the microparticles suggesting that a root growth process is in operation here if a VLS-type growth mechanism is to be invoked. Figure 3.13 (c) shows a HRTEM image of the tip of one such nanowire. The nanowire was 4.3 nm in diameter and a <110> growth direction can be elucidated from the lattice spacing in the HRTEM image.

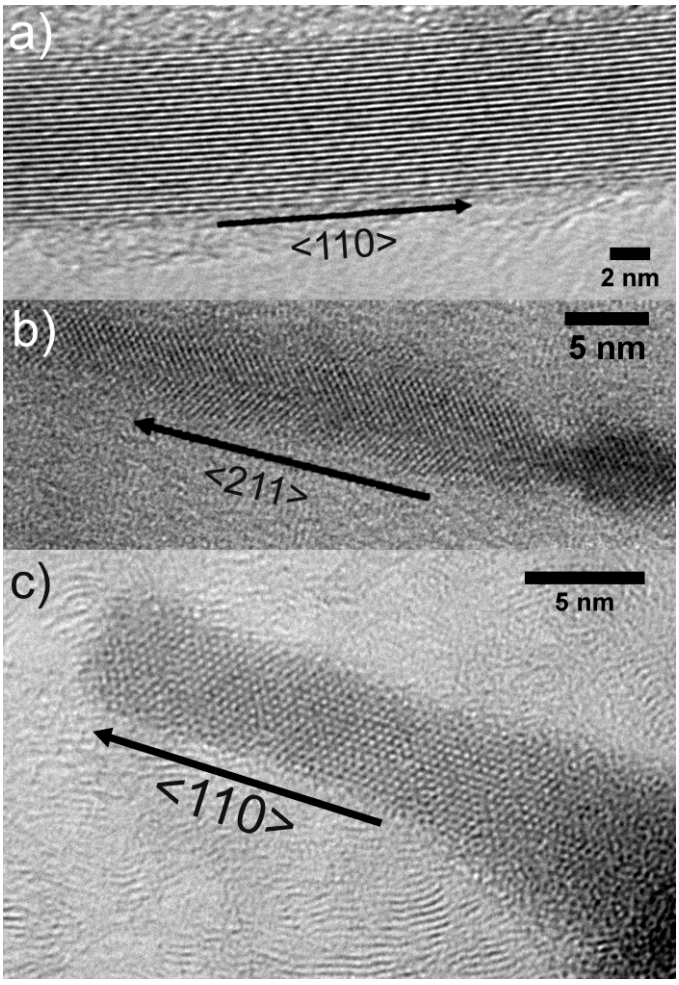

Figure 3.13. (a) HRTEM micrograph of an 8 nm diameter Ge nanowire synthesized at 673 K, (b) HRTEM micrograph of a Ge nanowire observed during the early stages of growth. The wire has a <211> growth direction and the {110} atomic planes are visible at 60° to the growth axis. No surface oxide layer was observed on the nanowire surface. (c) The tip of a <110> oriented Ge nanowire protruding from a largely amorphous microparticle.

A HRTEM micrograph of Ge nanoparticles which are abundant within the silicon-based matrix at the early stages of nanowire growth is shown in figure 3.14. The nanoparticles are essentially Ge nuclei that did not produce nanowires, either because there was insufficient Ge feedstock remaining to fuel the particles for nanowire growth, or because the particles were isolated from the Ge feedstock by the silicon-based matrix. The nanoparticles reveal an interplanar spacing of 0.4 nm, which corresponds to {110} planes in cubic Ge. The lower magnification TEM image (inset lower left) in figure 3.14 shows the relative abundance of these nanoparticles at the early stages of nanowire growth. The presence of the silicon-based matrix is critical to separate these Ge nanoparticle seeds, thus preventing aggregation of nanoparticles and promoting Ge nanowire growth. It is for this reason that the structure, and the Si:Ge ratio of the $Ge_2(TMS)_6$ and $HGe(TMS)_3$ precursors is important.

A further experiment was performed in order to investigate the influence of the cooling rate on the products recovered when shorter synthesis times were used. This involved heating the precursor solution to 673 K for 24 h, at which point the solution was quenched in a flask of liquid nitrogen. The product observed was similar to that observed in figure 3.14, and an example of this product can be found in figure 3.15.

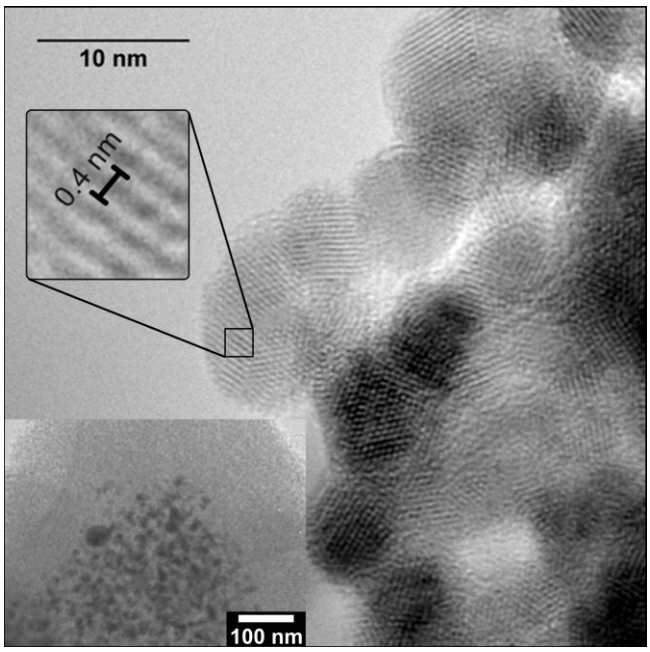

Figure 3.14. HRTEM micrograph of aggregated Ge nanoparticles observed at the surface of Si rich microparticles. Inset bottom left, a lower magnification TEM image of similar nanoparticles showing the surrounding Si based matrix, scale bar 100 nm.

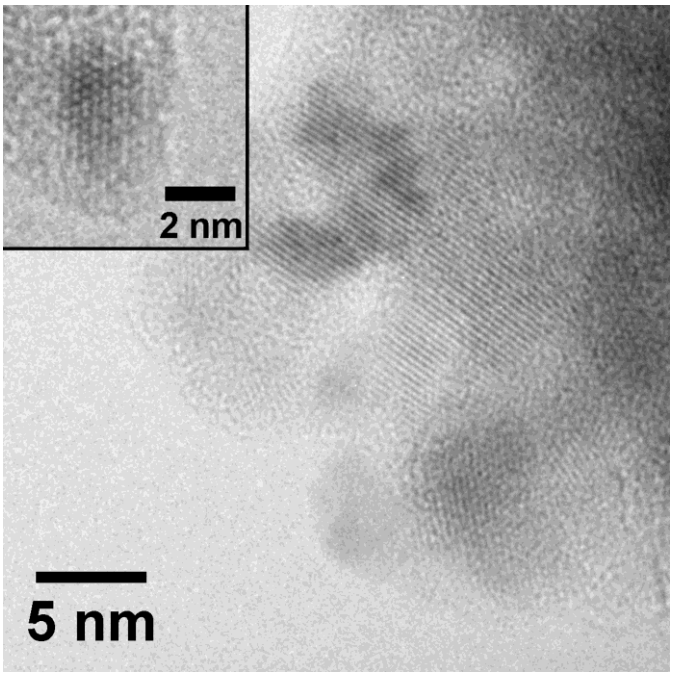

Figure 3.15. Ge nanoparticles within a Si-based matrix. The nanoparticles were collected from a precursor solution which was heated to 300 °C for 24 h and quench cooled in liquid nitrogen. Inset, a HRTEM micrograph of a 3 nm diameter Ge nanoparticle within the Si rich matrix material.

The growth of Ge nanowires from $Ge_2(TMS)_6$ and $HGe(TMS)_3$ can be divided into a number of stages. Firstly, the precursor must decompose to liberate Ge atoms. The strengths of the bonds present in this compound reveal that the Ge-Ge bond is the weakest (D_0(298 K) = 263.6 kJ mol^{-1}) followed by the Ge-Si bond (D_0(298 K) = 296.4 kJ mol^{-1}). The bond dissociation energy for a Si-C bond is significantly higher (D_0(298 K) = 451.5 kJ mol^{-1}).[24] Therefore Ge atoms will be liberated first prior to the decomposition of the trimethylsilyl groups. The Ge atoms then begin to nucleate and exist as liquid droplets at a synthesis temperature

of 673 K until they reach a critical diameter of ~7 nm, at which point they begin to solidify.[9,30] Silicon-based material derived from the trimethylsilyl groups of the precursor, forms a matrix and essentially acts to separate the Ge nuclei preventing them from aggregating and forming solid particles. This matrix thus allows molten Ge droplets to exist, as it prevents the Ge particles from sintering. It is unclear why Ge nanowires would spontaneously form from Ge droplets via a VLS-type mechanism given the cubic symmetry of the Ge crystal lattice. As such, a conventional VLS mechanism may not be applicable here, and unidirectional crystal growth may involve another less conventional growth mechanism which shall be discussed later.

Coagulation of nuclei to diameters greater than 7 nm could result in two possible outcomes. Firstly, these nuclei could continue aggregating and form larger particles which have been observed in samples of the nanowire material produced here. Another possibility is that these larger nuclei which are expected to exist in a solid state at the synthesis temperature could produce nanowires via a solid phase seeding mechanism. Ge nanowires seeded from solid particles have been shown to exhibit slower growth kinetics than those seeded from liquid seed droplets.[31] Larger diameter nanowires may therefore be expected to be shorter in length due to their slower growth kinetics. However, studies have also shown that the nanowire growth rate to be proportional to diameter, giving larger diameter nanowires faster growth kinetics in CVD-based experiments.[32] The result is that

no significant variation in the length of nanowires was observed for the range of diameters produced here.

Following nanowire growth, a non-uniform amorphous shell of the matrix material was found to deposit around the nanowires. This shell material is composed of Si, Ge, C and O and can be thought of as decomposed precursor material that did not produce nanowires. The shell acts to passivate the crystalline Ge nanowire surface rendering the nanowires resistant to atmospheric oxidation. For example, the nanowire displayed in figure 3.8 (c) was stored in air for 6 months prior to TEM analysis, and as shown by the FFT pattern (figure 3.8 (b)), its crystallinity remains. The amorphous shell may also improve the electrical transport properties of the nanowires by saturating any dangling bonds at the surface of the Ge crystal, thus potentially removing surface states which can act to trap charge carriers in the crystal. The Si-based shell would also prevent the formation of a Ge/GeO_x interface which is undesirable due to the instability of GeO_x.[33] Notably, nanowires produced at higher temperatures invariably possessed thicker amorphous shells than those produced at lower temperatures. In fact, many nanowires produced at 573 K (figure 3.13 (b)) did not exhibit any visible amorphous shell, suggesting that the amorphous shell forms in a separate step after growth of the nanowire core.

As stated earlier, a VLS growth mechanism is not a likely explanation for the production of Ge nanowires from Ge nanoparticles observed in the present work. However, a number of other nanowire growth mechanisms should also be considered. A similar formation mechanism as described for oxide-assisted growth (OAG) could be possible, as the amorphous shell material here could also be considered as an inert backbone facilitating nanowire growth. Reports on the OAG mechanism state that a monoxide species such as SiO is a prerequisite for nanowire growth. This oxide acts as a sink for the vapor phase feedstock needed for nanowire growth, whilst also capping lateral growth of the nanowire.[12,34] To date, there have been no reports of solution phase or supercritical fluid phase OAG of semiconductor nanowires, nor has there been any report of diameter control in nanowires produced by the OAG method. However, OAG of Ge nanowires requires the presence of a Ge species and an oxide species in equal measures to facilitate nanowire growth. As such, an OAG mechanism cannot explain the nanowire growth observed here, given the great care taken to eliminate water and oxygen from the synthesis process.

Soft templating is another potential route to nanowire production in the absence of catalytic growth seeds. This approach involves ligand control strategies for nanowire synthesis. Essentially, a ligand or surfactant is used to cap crystal growth in certain directions, thus facilitating unidirectional nanowire growth.[35,36] An inherent structural anisotropy is generally required to allow unidirectional

growth of crystals by this method. However, reports do exist for cubic metals such as Au.[37] Consequently, it is possible that the Si-based matrix present in this work plays the role of a soft template, thus guiding nanowire growth.

Nucleation of nanowires by oriented attachment has also been reported for a number of compound semiconductors such as CdS,[38] CdTe,[39] and PbS.[40] The oriented attachment of nanoparticles of these compounds to form unidirectional structures has been attributed to the formation of a permanent or temporary electric (or magnetic) dipole in each nanocrystal. This mechanism is plausible for ionic structures consisting of layers of cations and anions, but unlikely for cubic Ge. However, oriented attachment has also been observed for metals such as Au where long-lived dipoles are unexpected.[41,42] A complete understanding of oriented attachment in the case of highly symmetric cubic materials such as Au has not yet been achieved. Halder *et. al.*[42] suggested that a smoothing process at the interface between two fusing particles would provide sufficient asymmetry in the structure to produce a temporary electric dipole which would then act as the driving force for further particle attachment forming an elongated nanowire structure. Such a smoothing effect could be explained by the negative chemical potential expected at the interface between the particles due to the concave curvature at this interface. This negative chemical potential would provide a thermodynamic driving force for the smoothing effect and facilitate an oriented attachment growth mechanism for nanowires of cubic crystalline materials. If the

observed correlation between nanowire diameter and the depressed melting point of Ge at the nanoscale is coupled to the possibility of an oriented attachment growth mechanism for Ge nanowires, a plausible growth mechanism for the nanowires produced in this study can be formulated.

As stated earlier, the Ge nanoparticles observed at the early stages of Ge nanowire growth, as shown in figure 3.14, are expected to exist in a semi-molten state as they are near to their theoretical melting point. These particles should readily fuse with one another, solidifying as they do so. Smoothing of the elongated structure formed, would then allow further particle attachment in accordance with previous reports on the oriented attachment of nanoparticles. Furthermore, the high curvature at the ends of these elongated structures would suggest that their tips would exist in a semi-molten state during nanowire growth. These semi-molten regions would encourage further particle attachment and one-dimensional growth. The nanowire shown in figure 3.13 (b) displays a hallmark of this mechanism to the right of the image where two thicker sections of nanowire are separated by a thinner section suggesting that two particles may have fused at this point. Ge nanoparticles are rarely seen when nanowire growth is complete. This suggests that the nanoparticles are involved in the nanowire growth process and oriented attachment is a viable route to nanowire formation. It is suggested that the process of semi-molten particle fusion is the likely nanowire growth mechanism at play in the present work.

Additional support for the mechanism outlined above may be found when the shapes of the nanowire diameter distributions shown in figure 3.7 are considered. As stated previously a log-normal model best describes the nanowire diameter distributions at lower temperatures (573 K and 673 K). A log-normal diameter distribution has been shown previously to be indicative of coalescence.[43] Consequently, the shape of the nanowire diameter distribution curves also supports the nanowire growth mechanism outlined above, whereby coalescence of Ge nanoparticles, which are near their melting point due to the depressed melting point of nanoparticles with respect to analogous bulk material, leads to formation of Ge nanowires. The change in the shape of the nanowire diameter distribution curves with increasing temperature suggests that an additional crystal growth mode may be involved at higher synthesis temperatures. For example, the diameter distribution curve for nanowires synthesized at 773 K shown in figure 3.7 (d) displays a broader diameter distribution than for nanowires synthesized at lower temperatures. Future work may involve deconvolution of the nanowire distribution curves in parallel with in-situ nanowire growth studies to further confirm the underlying nanowire growth mechanism in operation for the system shown here.

3.4. Conclusions

In conclusion, this work has demonstrated that highly crystalline Ge nanowires exhibiting diameters as small as 4 nm can be synthesized in the absence of a conventional foreign metal catalyst such as colloidal gold nanoparticles.

Conventionally, foreign seed crystals and porous templates have been the only routes that allow diameter control of Ge nanowires. This report suggests that the significant melting point depression of Ge and other semiconductors at the nanoscale may provide a means to predict and control the diameters of semiconductor nanowires, by careful control of synthesis temperature, and precursor design.

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Chapter 4

Resist-Substrate Interface Tailoring for Generating High Density Arrays of Ge and Bi_2Se_3 Nanowires by Electron Beam Lithography

4.1. Abstract

In this chapter a chemical process to remove the native oxide on Ge and Bi_2Se_3 crystals, thus facilitating high-resolution electron beam lithography (EBL) on their surfaces using a hydrogen silsesquioxane (HSQ) resist is reported. HSQ offers the highest resolution of all the commercially available EBL resists. However, aqueous HSQ developers such as NaOH and tetramethylammonium hydroxide (TMAH) have thus far prevented the fabrication of high-resolution structures via the direct application of HSQ to Ge and Bi_2Se_3, due to the solubility of components of their respective native oxides in these strong aqueous bases. This work thus provides a route to ordered, high resolution, high density Ge and Bi_2Se_3 nanostructures with potential applications in the microelectronics, thermoelectrics and photonics devices.

4.2. Introduction

4.2.1. Hydrogen Silsesquioxane

Hydrogen silsesquioxane (HSQ) is a high resolution, negative-tone, inorganic, electron beam lithography (EBL) resist, which is capable of producing high density features in the sub-20 nm regime.[1,2] Additionally, following electron beam exposure, HSQ physically and chemically, closely resembles SiO_2.[3] This

similarity to SiO_2 ensures that HSQ is inherently compatible with current microelectronics processing. To date, the use of HSQ has been largely limited to Si processing, although the application of HSQ to several other materials has been reported.[4–6]

This work describes the application of a HSQ EBL process to single crystal Ge wafers, and Ge and Bi_2Se_3 thin films grown by molecular beam epitaxy (MBE). To date, the use of a high resolution HSQ process on these materials has been hindered by the high solubility of their respective native oxides in the aqueous bases of traditional HSQ developers, *e.g.* tetramethylammonium hydroxide (TMAH) and NaOH. The present work highlights successful routes toward removing the native oxides of these materials immediately prior to HSQ deposition to facilitate high-resolution EBL.

4.2.2. Germanium

Ge is an intrinsic Group 14 semiconductor which offers a number of distinct advantages over Si for microelectronic device applications.[7,8] Namely, Ge exhibits superior electron and hole mobilities relative to Si and has a lower band gap energy.[9] Ge possesses a complex native oxide (GeO_x) consisting of GeO and GeO_2 components. Both GeO and GeO_2 are soluble in TMAH and NaOH. Consequently, if a GeO_x layer exists between the Ge crystal and the HSQ EBL resist, dissolution of the underlying GeO_x layer during development of the resist will result in lift-off of any high resolution features written by EBL. Removal of

the native Ge oxide is thus imperative prior to HSQ deposition, to facilitate the use of traditional aqueous HSQ developers. Although non-aqueous developers do exist for HSQ, these have been shown to offer significantly lower resolution than their aqueous counterparts.[10]

4.2.3. Bismuth Selenide

Bi_2Se_3 has attracted much attention due to recently discovered topological insulating properties in the material.[11,12] Topological insulator nanowires and nanoribbons may have applications in quantum computing.[13] Bi_2Se_3 has also been extensively studied for thermoelectric devices and infra-red detector applications.[14] Dresselhaus and co-workers proposed in the early 1990s that one-dimensional thermoelectric materials would display enhanced thermoelectric performance relative to bulk materials, due to reduced thermal conductivity in the 1 D structures caused by confinement effects on the mean free path of phonons in the confined material. As a result, 1 D thermoelectric materials such as Bi_2Se_3 nanowires and nanoribbons have been increasingly researched as potentially useful materials in next generation thermoelectric generators.[15] Kong *et al*. recently showed that the native oxide on Bi_2Se_3 is composed of both BiO_x and SeO_x, and while the BiO_x component forms rapidly on oxide free Bi_2Se_3 surfaces, the SeO_x component forms more slowly.[16] Importantly, at room temperature, the SeO_x component of the native oxide is soluble in aqueous bases, whilst the BiO_x component is not.[17] Consequently, application of a HSQ EBL process to Bi_2Se_3 requires removal of SeO_x prior to HSQ deposition. This work thus details a

reproducible route to the production of high resolution features on Ge and Bi_2Se_3 using a HSQ direct-write, negative-tone, EBL process.

4.3. Results

4.3.1. Ge Lithography

Cl-terminated Ge was found to successfully eliminate the presence of an interfacial Ge oxide between the Ge substrate and the HSQ EBL resist. Elimination of the native oxide on Ge thus allowed for the production of ordered arrays of 20 nm wide HSQ lines directly onto the Ge surface. Figure 4.1 shows a SEM micrograph of 20 nm wide HSQ lines produced on Cl-terminated p-Ge. Chlorination of Ge substrates is detailed in section 2.3.4. Inset in figure 4.1 is a SEM micrograph of a Ge sample for which the native oxide was not removed prior to HSQ deposition and EBL exposure. Comparing the two SEM micrographs in figure 4.1, it is apparent that removal of the native Ge oxide prior to EBL is necessary to produce ordered arrays of high-resolution HSQ features on Ge surfaces. The requirement for removal of the native Ge oxide prior to EBL processing can be attributed to the high solubility of GeO_2, and to a lesser extent GeO, in strong aqueous bases such as NaOH. When the sample shown in the inset of figure 4.1 is placed in the developer solution after electron beam exposure, the native Ge oxide between the Ge crystal and the exposed HSQ is dissolved. Dissolution of the native Ge oxide in the developer solution results in partial lift-off of the HSQ lines and consequently a loss of order in the resultant HSQ mask as shown in the SEM micrograph inset in figure 4.1. Line edge

roughness (LER) of the 20 nm wide HSQ lines (pitch 70 nm) was measured at 3.4 nm (3σ) by analysis of high magnification SEM images using *ImageJ* image processing software as described in chapter 2.

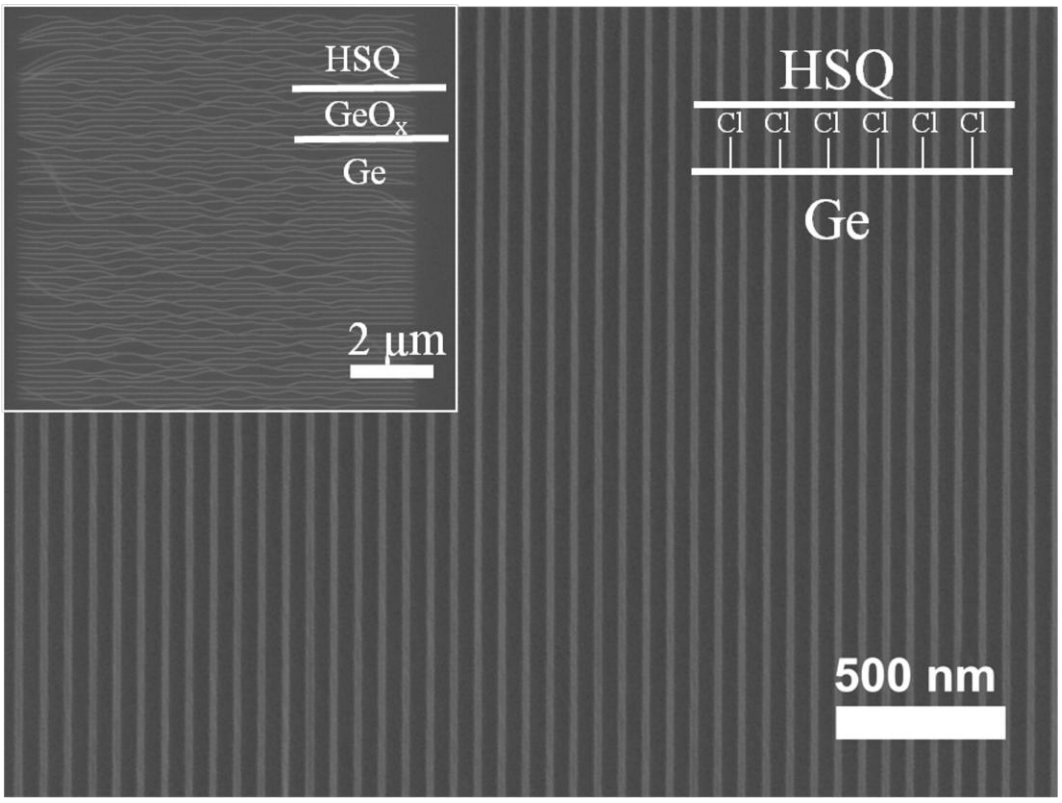

Figure 4.1. 20 nm wide HSQ lines at a pitch of 70 nm, written on a Ge <100> substrate at an area dose of 900 µC cm^{-2}. Inset, 20 nm wide HSQ lines at a pitch of 70 nm, written on a Ge <100> (GeO_x surface) substrate at an area dose of 900 µC cm^{-2}.

Figure 4.2 shows Ge 3d core level XPS spectra for Ge samples before and after chemical treatment to remove the native Ge oxides. The Ge 3d peak has been deconvoluted to reveal the contributions from the $3d_{5/2}$ and $3d_{3/2}$ levels in Ge^0, as

well as higher oxidation states of Ge. Prior to chemical treatment to remove the native oxide there is an observed broadening of the Ge 3d core level peak (FWHM 2.48 eV) due to the contribution from GeO_x which results in additional blue shifted Ge 3d peaks relative to bulk Ge^0. After chemical treatment to remove the native Ge oxides the Ge 3d core level peak is observed to narrow (FWHM 2.08) as the contribution from higher oxidation states of Ge is removed. Similarly, there is a significant change in the O 1s core level spectrum (figure 4.3) before and after chemical treatment to remove the native oxide. Whilst there is a clear O 1s peak observed at ~532 eV in the sample prior to chemical treatment, any signal due to O 1s is below the level of the background noise of the spectrum after chemical treatment to remove the native oxide.

The HSQ pattern produced using the process outlined above, was subsequently transferred to a p-Ge substrate using a Cl_2 reactive ion etch (RIE). An example of a sample where the pattern was transferred to the substrate is shown in figure 4.4. Figure 4.4 shows a SEM micrograph of 15 nm wide Ge fins at a pitch of 120 nm. Details of electron exposure doses for the HSQ mask used to produce these structures are included in figure 4.5.

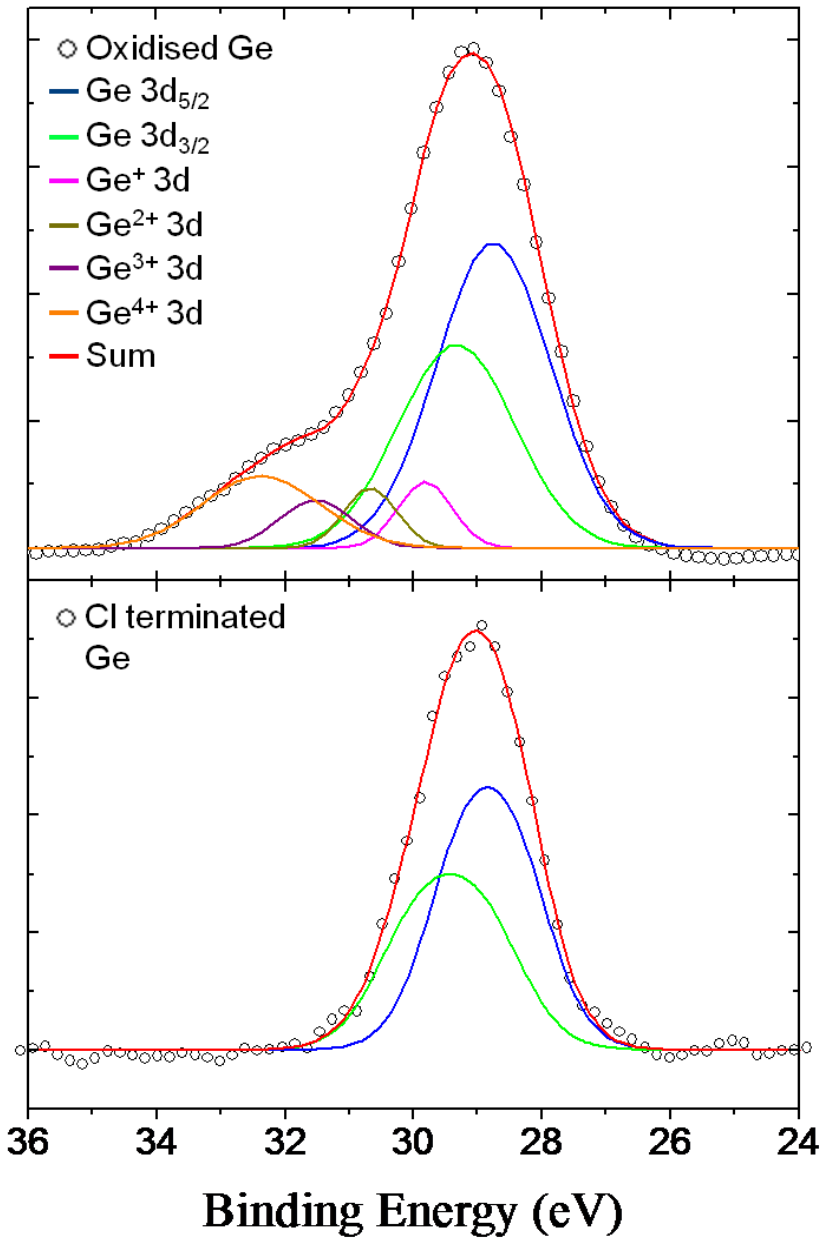

Figure 4.2. Ge 3d core-level XPS spectra of <100> Ge wafer before (upper spectrum) and after (lower spectrum) chemical treatment to remove the native oxide. The untreated wafer exhibits significant peak broadening and a blue shifted shoulder consistent with the presence of a native Ge oxide at the surface of the sample.

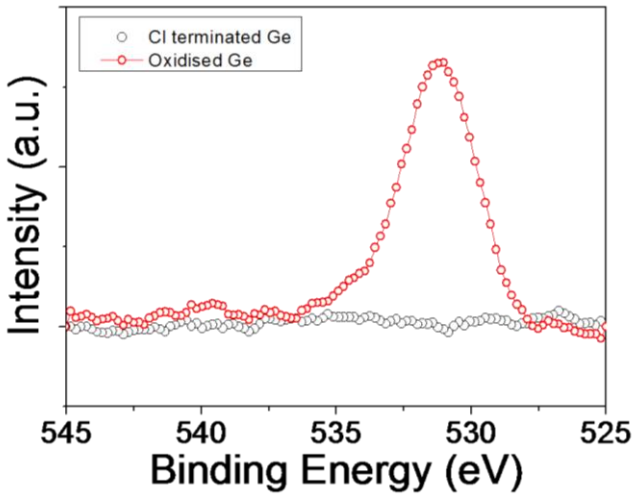

Figure 4.3: O 1s core-level XPS spectra of Ge samples before and after treatment to remove the native oxide and terminate the crystal with Cl.

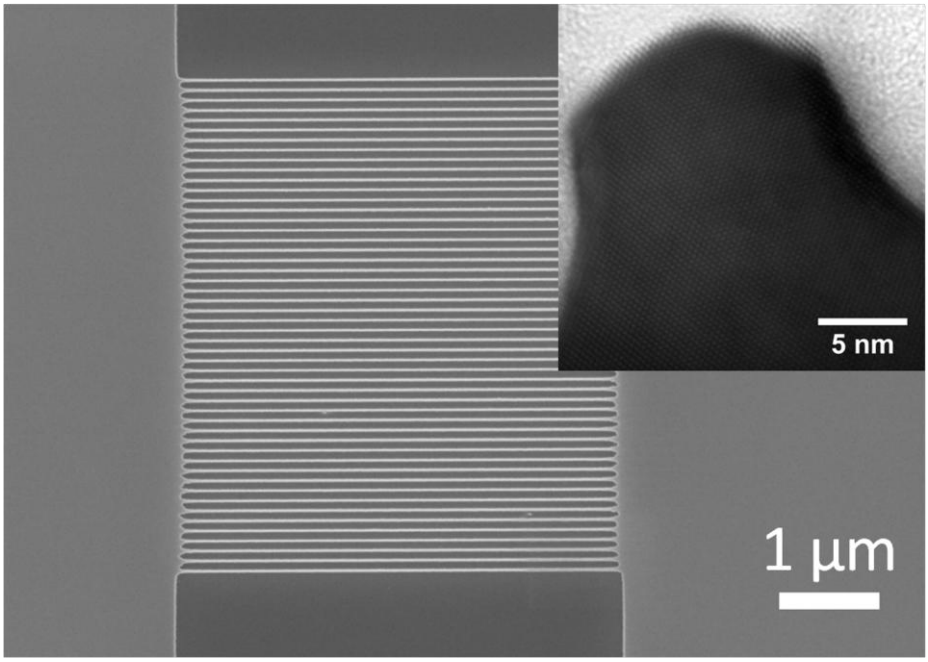

Figure 4.4. 15 nm wide Ge fins at a pitch of 120 nm, etched to a depth of 20 nm. Fin length is 4.5 µm and fins are integrated with Ge pads (shown left and right) in device-ready architecture. Inset, a TEM micrograph displaying a cross-section of one such 15 nm wide Ge fin.

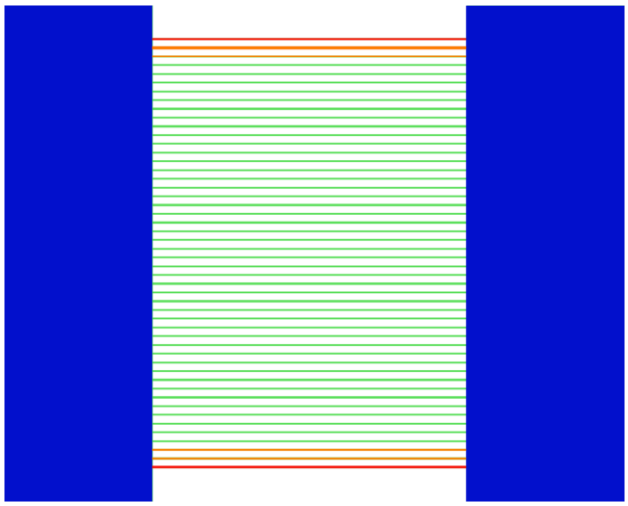

Figure 4.5. Areal dose map of pattern used to generate 15 nm HSQ lines, at a pitch of 100 nm, integrated with contact pads (shown in blue). Relative areal doses are colour coded as follows, blue 0.8, green 1.0, amber 1.1, red 1.2. Base areal dose used for the exposure was 900 μC cm^{-2}.

The fins have been etched into the Ge wafer to a depth of 20 nm. The inset of figure 4.4 is a HRTEM micrograph of a cross-section of a 15 nm wide fin. The fin shown in the HRTEM micrograph in figure 4.4 was purposely produced along a <110> axis of the Ge crystal. The family of <110> axes are known to offer the highest charge carrier mobility within p-type Ge (Fd3m crystal system), and are thus preferable for device fabrication.[18]

Fabrication of arrays of high-resolution HSQ lines on a Ge wafer using the HSQ EBL process outlined above was also observed to depend on the age of the HSQ resist. HSQ has a shelf life of 6 months when stored in a sealed container at 5 °C. The process for producing high resolution HSQ lines on Ge is reproducible and repeatable up to ~ 1 month after the stated expiry date of the HSQ resist.

However, after this time, effects like those shown in the inset of figure 4.1 were observed, where exposed lines partially delaminate from the substrate during development. This observation suggests that the hydrogen groups in the HSQ resist play an important role in the adhesion of the HSQ resist to the Cl-terminated Ge surface. As the HSQ resist ages, the cage-like oligomers within the resist cross-link forming a network structure with the evolution of hydrogen gas. The hydrogen sites in HSQ have been reported to be the sites involved in HSQ network formation.[19] Consequently, as the resist ages fewer H sites are available to interact with the substrate to which the resist is applied.

Fourier transform infrared (FTIR) spectroscopy was used to investigate the presence of any chemical interaction between the HSQ resist and a Cl-terminated Ge substrate (figure 4.6), following electron beam exposure or thermal treatment. Figure 4.6 shows an FTIR spectrum of a 25 nm HSQ film deposited on a 20 nm Ge film prepared on a Si substrate by MBE (Ge-Si) prior to electron beam exposure or thermal annealing. Preparation of the Ge-Si substrates has been described elsewhere.[20] The native Ge surface oxide was removed, and the Ge film was terminated with Cl prior to HSQ deposition. The spectrum in figure 4.6 was produced by subtracting the spectrum produced by a clean Ge-Si substrate from that of a Ge-Si substrate coated with a 25 nm HSQ film. The HSQ film was prepared on the Ge-Si substrate as detailed in Chapter 2 (Section 2.3.4.) for Ge substrates. The spectrum shows the hallmark absorbance peaks associated with HSQ. The Si-H stretch is observed at 2256 cm^{-1} which is characteristic of a Si-H species whereby the Si atom is bound to three electronegative O atoms leading to

a blue shift in the Si-H absorbance peak relative to a Si-H species present on a hydride terminated Si wafer, for example. The asymmetric Si-O-Si stretching modes for cage and network HSQ structures have absorbance peaks labelled $\nu_{as}(Si\text{-}O\text{-}Si)_{cage}$ and $\nu_{as}(Si\text{-}O\text{-}Si)_{net}$ and are visible at 1122 cm^{-1}, and 1065 cm^{-1} respectively, whilst Si-O bending modes are observed at 860 cm^{-1}, and 827 cm^{-1} and are labelled d(H-Si-O) and d(O-Si-O) respectively. The bending modes d(H-Si-O) and d(O-Si-O) can be attributed to the cage and network structures respectively.[21,22]

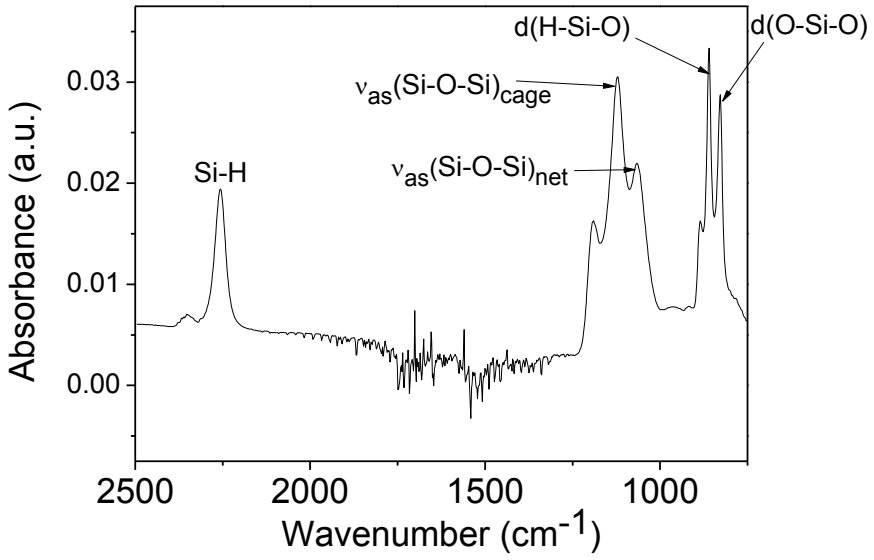

Figure 4.6. FTIR spectrum of a 25 nm HSQ film deposited on a MBE grown Ge thin film following subtraction of substrate absorbance spectrum.

The greater intensity of the $\nu_{as}(Si\text{-}O\text{-}Si)_{cage}$ and d(H-Si-O) absorbance peaks in figure 4.6 with respect to the $\nu_{as}(Si\text{-}O\text{-}Si)_{net}$ and d(O-Si-O) peaks respectively, is consistent with a high concentration of the cage species with respect to that of the network species prior to electron beam exposure or high temperature thermal

treatment. Figure 4.7 displays FTIR spectra of 25 nm HSQ films on Ge-Si and Si substrates after annealing at 673 K for 1 h in a N_2 atmosphere. The peaks associated with the cage structure of HSQ seen in figure 4.6 are notably absent from the spectra in figure 4.7, these include the Si-H stretch, $\nu_{as}(Si\text{-}O\text{-}Si)_{cage}$, and d(H-Si-O) at 2256, 1122 and 860 cm^{-1} respectively. The dominant feature of the spectra in figure 4.7 is the absorbance peak at 1060 cm^{-1}, associated with asymmetric stretching of the Si-O-Si moiety in a SiO_2 glass. Another feature present in the FTIR spectra of the HSQ films on Ge-Si and Si shown in figure 4.7, is the peak denoted '*' at 879 cm^{-1} associated with a Si-O bending mode in a Si rich silicon oxide.[22] The blue trace in figure 4.7 represents the difference between the red and black traces, and the absorbance values in the blue trace have been magnified for clarity. The blue trace shown in figure 4.7 shows a broad peak centred at approximately 1000 cm^{-1}, which can be partially attributed to the presence of a Ge-O-Si moiety.[23,24]

Similar FTIR analyses were also performed on electron beam exposed HSQ films on Si and Ge-Si substrates. A 2 mm × 1.5 mm area was exposed at a dose of 800 μC cm^{-2} on 25 nm HSQ films on both Si and Ge-Si substrates, requiring an exposure time of 48 h each. Figure 4.8 shows FTIR spectra obtained from the exposed and developed HSQ films on both Si and Ge-Si substrates.

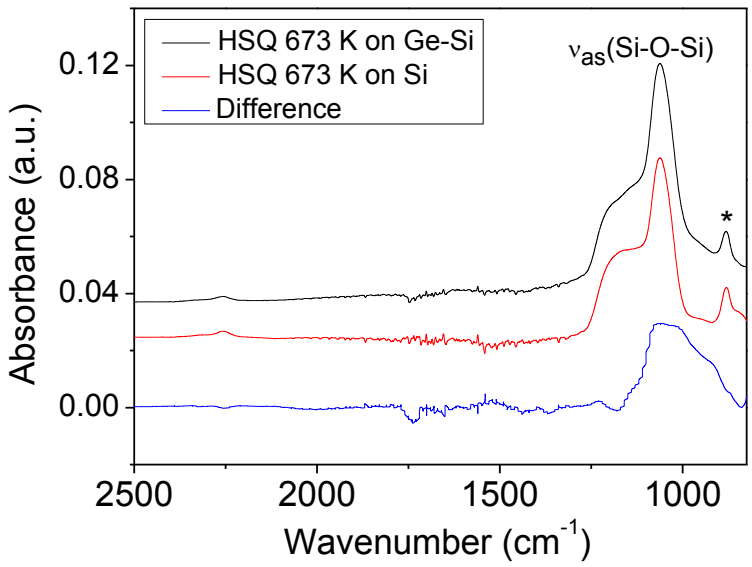

Figure 4.7. FTIR spectra of 25 nm HSQ films deposited on an MBE grown Ge thin film (black trace), and a Si substrate (red trace) annealed in a N_2 atmosphere at 673 K. The peak labelled '*' is associated with a Si-O bending mode in a Si rich oxide. The blue trace represents the difference between the red and black traces, and the broad absorption peak at ~1000 cm^{-1} can be attributed to a combination of Si-O-Si and Ge-O-Si moieties. Spectra are offset along the absorbance axis for clarity.

The spectra shown in figure 4.8 very closely resemble those of the annealed HSQ films, shown in figure 4.7. The most significant peaks in the spectra in figure 4.8 are the same as those highlighted in figure 4.7, those being the asymmetric Si-O-Si stretch at 1060 cm^{-1}, and the Si-O bend at 879 cm^{-1}. When the difference between the FTIR spectra obtained from the electron beam exposed samples was considered (blue trace figure 4.8), only a very low intensity absorbance peak at 1030 cm^{-1} consistent with a Ge-O-Si vibrational mode[24] was observed, however,

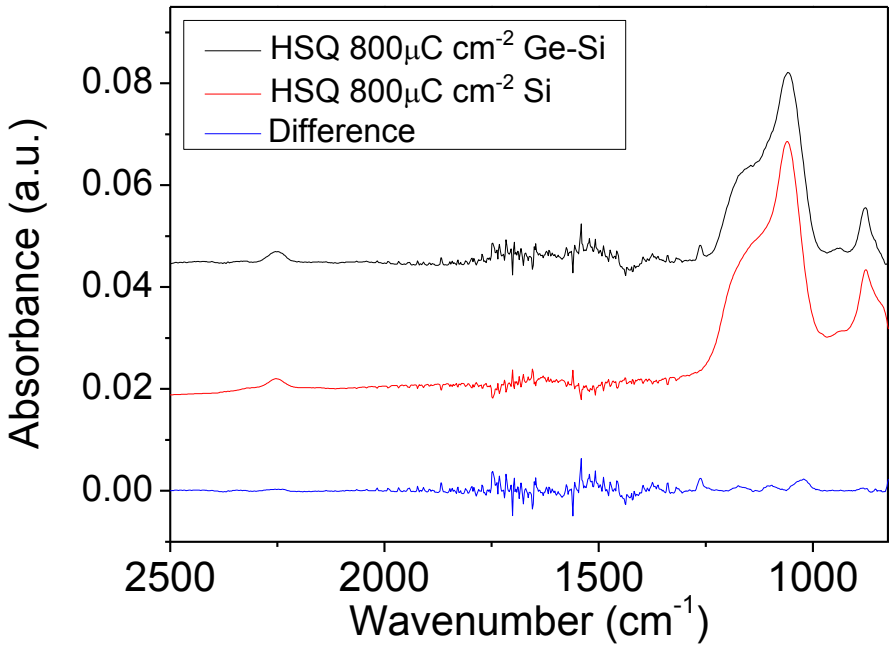

Figure 4.8. FTIR spectra of electron beam exposed (800 μC cm^{-2}) 25 nm HSQ films on an MBE grown Ge thin film (black trace), and a Si substrate (red trace). The blue trace represents the difference between the red and black traces. Spectra are offset along the absorbance axis for clarity.

this peak is almost at the noise level of the spectrum. Electron beam exposure of a larger area of HSQ film may facilitate detection of a more significant signal from the HSQ interface with Ge, however, this would require electron beam exposure times of a week or more for each of the Si and Ge-Si samples. Consequently, a flood electron exposure technique should be the subject of further investigation in future work on this materials system.

Electron beam exposure and thermal curing of HSQ films have been shown previously to result in similar Si-H and Si-O bond redistribution effects, thus thermal curing can be considered to produce comparable effects to electron beam

exposure in HSQ films.[3] Consequently, the Ge-O-Si moiety observed in HSQ films deposited on Cl-terminated Ge after thermal curing suggests that HSQ patterns produced on Cl-terminated Ge by EBL are covalently bound to the Ge crystal, thus preventing lift-off of high-resolution HSQ patterns during HSQ development.

4.3.2. Bi_2Se_3 Lithography

Figure 4.9 (a) shows a SEM image of a cubic array of 20 nm diameter Bi_2Se_3 disks at a pitch of 100 nm. Figure 4.9 (b) displays a SEM image of 30 nm wide and 2 nm deep Bi_2Se_3 nanoribbons produced using the HSQ EBL process outlined above. The HSQ etch mask remains on top of the Bi_2Se_3 structures in figures 4.9 (a-b). Figures 4.9 (c) and (d) show a comparison of HSQ lines exposed on an untreated Bi_2Se_3 surface (figure 4.9 (c)) and a Bi_2Se_3 surface which has been washed with a NaOH/TMAH solution to dissolve surface SeO_2 (figure 4.9 (d)). Comparing figures 4.9 (c) and (d) it is again apparent that the presence of a surface oxide, which is soluble in the HSQ developer, inhibits the production of ordered arrays of high-resolution HSQ structures using a HSQ EBL process.

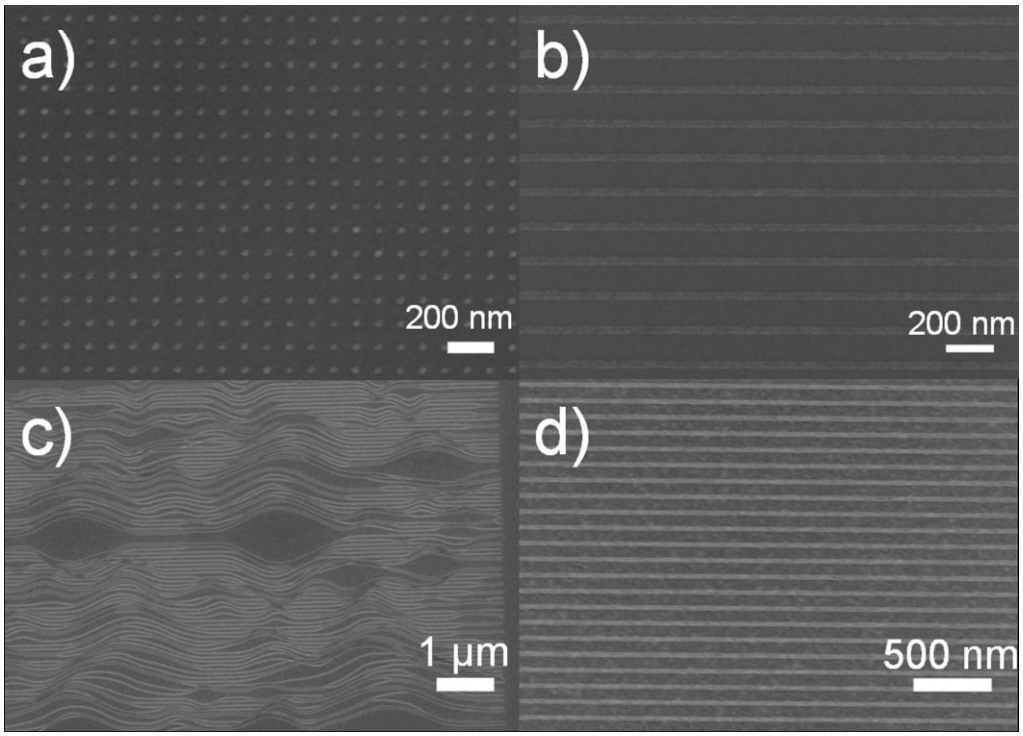

Figure 4.9. (a) Cubic array of 20 nm diameter, 2 nm high Bi_2Se_3 disks at 100 nm pitch. (b) 30 nm wide Bi_2Se_3 nanoribbons at a pitch of 140 nm. (c) 20 nm wide HSQ lines exposed at a pitch of 70 nm on an untreated Bi_2Se_3 surface. (d) 20 nm wide HSQ lines exposed at a pitch of 100 nm on a Bi_2Se_3 surface washed with a NaOH/TMAH solution prior to HSQ deposition to remove surface SeO_2.

Figure 4.10 displays a selection of cross-sectional TEM micrographs of Bi_2Se_3 nanoribbons produced from an 8 nm Bi_2Se_3 film grown by MBE. The Bi_2Se_3 film was patterned using the HSQ EBL process outlined above and the pattern was transferred to the film using an Ar ion beam etch. Figure 4.10 (a) displays 30 nm wide nanoribbons at a pitch of 60 nm produced from an 8 nm thick Bi_2Se_3 film. Figure 4.10 (b) shows a HRTEM micrograph of the crystal lattice of a single Bi_2Se_3 nanoribbon. The HRTEM micrograph clearly shows the layered crystal

structure of rhombohedral Bi_2Se_3 with the c-axis of the crystal oriented orthogonally to the Si <111> substrate. The repeating units in the layered structure of Bi_2Se_3 are known as quintuple layers (QL) and are stacked along the c-axis. Each QL is so-called as it consists of five layers of atoms in the sequence Se-Bi-Se-Bi-Se. Within each QL, strong covalent and ionic bonding dominates, however, only weak Van der Waals-type bonding exists between the two Se layers at the QL-QL interface.[25] The observed QLs in figure 4.10 (b) are ~1 nm thick as described in previous reports. Figure 4.10 (c) shows a HRTEM micrograph of a cross-section of an 18 nm wide, 7 nm thick, Bi_2Se_3 nanoribbon. An amorphous layer of material is observed at the interface between the nanoribbon (dark region) and the Si substrate (lower left) in figure 4.10 (c) which can be attributed to the formation of a layer of amorphous SiO_2 which is formed following MBE Bi_2Se_3 thin film growth. Amorphous SiO_2 formation can be attributed to the diffusion of oxygen through the Bi_2Se_3 thin film when the Bi_2Se_3 film is exposed to an ambient atmosphere.[26]

XPS analysis of a Bi_2Se_3 thin film sample before and after treatment with the TMAH/NaOH/NaCl solution revealed a change in the composition of the surface of the sample. A Bi_2Se_3 thin film sample which had been exposed to ambient atmosphere for 6 months was analyzed by XPS as shown in the upper spectra in figure 4.11. Deconvolution of the Bi 4f core level peaks (upper spectrum figure 4.11 (b)) revealed the presence of the $4f_{7/2}$ and $4f_{5/2}$ peaks from Bi_2Se_3 at 157.4 eV and 162.8 eV respectively (peak area ratio of 1.32 measured for $4f_{7/2}/4f_{5/2}$).

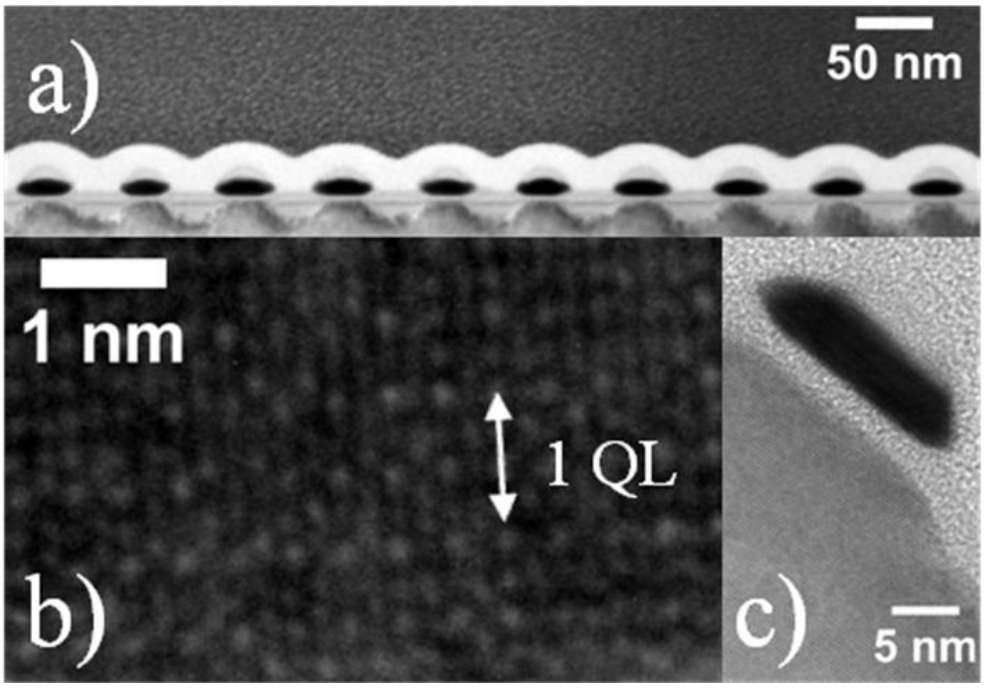

Figure 4.10. (a) Cross-sectional TEM micrograph of 30 nm wide, 8 nm high, Bi_2Se_3 nanoribbons at a pitch of 60 nm. HSQ mask remains atop the Bi_2Se_3 nanoribbons. (b) HRTEM micrograph of a cross-section of a Bi_2Se_3 nanoribbon. The image was recorded along the <1-10> zone axis of the crystal, showing the stacks of quintuple layers (QL) in the c-axis of the crystal as shown. (c) HRTEM micrograph of a cross-section through a 6 nm thick Bi_2Se_3 nanoribbon and the underlying Si <111> substrate.

Furthermore, the deconvolution reveals Bi $4f_{7/2}$ and $4f_{5/2}$ peaks blue shifted by 1.3 eV relative to the Bi 4f core level peaks attributed to Bi_2Se_3. These blue shifted peaks can be attributed to Bi interacting with a more electronegative species than Se, *i.e.* forming Bi_2O_3. The blue shift of 1.3 eV for Bi_2O_3 is consistent with recent observations reported for Bi_2Se_3 nanowires with a similar native oxide.[16] Comparison of the 4f core level peak areas for Bi_2Se_3 and Bi_2O_3 suggests a

Bi_2Se_3/Bi_2O_3 ratio of 3/1. Thus, a Se/O ratio of 3/1 at the surface of the Bi_2Se_3 film can be inferred from the XPS spectra. Figure 4.11 also shows XPS spectra of the Se component of the native oxide. The spectra in figure 4.11 (a) display Se 3d core level peaks attributable to Se^{2-} in Bi_2Se_3 at a binding energy of 52.8 eV. Deconvolution of the peak at 52.8 eV reveals contributions from the Se $3d_{5/2}$ and $3d_{3/2}$ levels at binding energies of 52.4 eV and 53.2 eV respectively suggesting a crystal field splitting energy of 0.8 eV. The sample analysed prior to washing with the TMAH/NaOH/NaCl solution, also revealed a lower intensity Se 3d core level peak at a binding energy of 58.3 eV. The blue shift of the peak attributed to SeO_2 relative to that attributed to Bi_2Se_3 is a consequence of the large difference in oxidation of Se in the two species in question, Se^{4+} in SeO_2, and Se^{2-} in Bi_2Se_3.

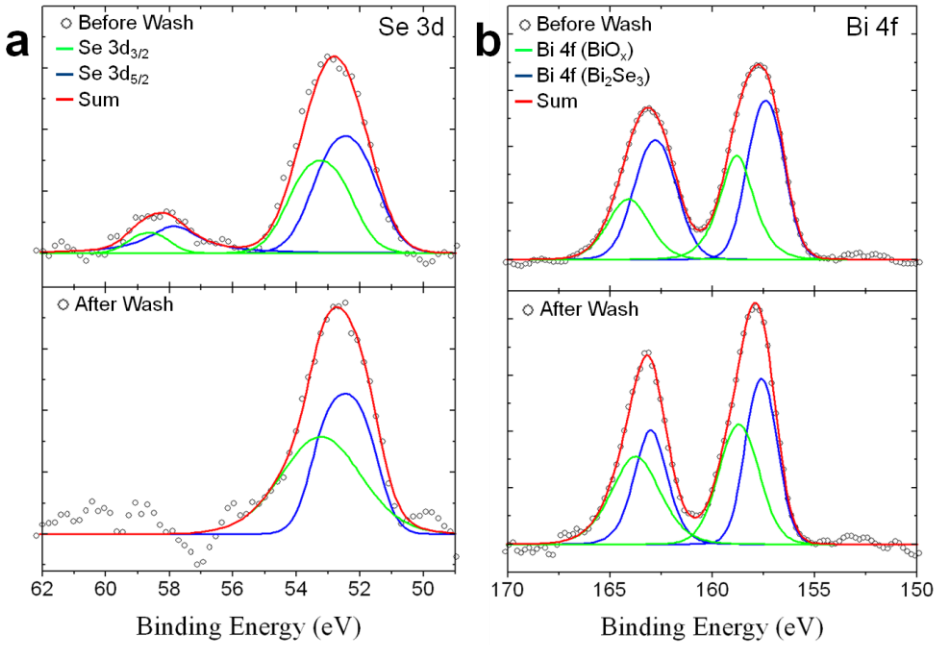

Figure 4.11. XPS core-level spectra of Bi_2Se_3 thin films before and after TMAH/NaOH/NaCl washing to remove SeO_2 (a) Se 3d core level XPS spectra showing a Se 3d peak attributable to Bi_2Se_3 at ~52.8 eV and a lower intensity

peak attributable to SeO_2 at ~58.3 eV prior to washing. Red trace represents sum of the Se $3d_{3/2}$ (green trace) and $3d_{5/2}$(blue trace) peaks obtained through deconvolution of the raw data. (b) Bi 4f core level XPS spectra showing peaks attributable to the Bi $4f_{5/2}$ and $4f_{7/2}$ core levels at approximately 158 eV and 163 eV respectively. Red trace represents sum of Bi $4f_{5/2}$ and $4f_{7/2}$ peaks from Bi_2Se_3 (blue trace) and Bi $4f_{5/2}$ and $4f_{7/2}$ peaks from Bi_2O_3 (green trace).

4.4. Conclusions

To conclude, successful chemical routes to remove the native oxides of both Ge and Bi_2Se_3 prior to the application of HSQ EBL resist have been demonstrated. The chemical processing of Ge and Bi_2Se_3 described herein is imperative to produce ordered arrays of high-resolution nanostructures in both of these materials using a HSQ EBL process. Consequently, where a material possesses a native oxide which is soluble in HSQ developers, the limiting factors to achieving high resolution HSQ nanostructures on the surface of such a material, is the availability of a viable route to remove the native oxide and the adhesion of HSQ to the oxide-free surface of the underlying material.

Furthermore, a route to the production of covalently bound SiO_x films on Ge has been demonstrated by thermal curing of HSQ films deposited on Cl-terminated Ge crystals. This route may find applications in the fabrication of Ge-on-insulator (GeOI) substrates as well as in the production of low-*k* dielectric films on Ge materials.

4.5. Bibliography

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Chapter 5

High Resolution Electron Beam Lithography for the Fabrication of Si Nanowire Arrays and the Directed Self Assembly of Block Copolymers

5.1. Abstract

Arrays of Si nanowires have been fabricated in FET device architectures using high resolution electron beam lithography (EBL) with the negative-tone, inorganic, electron beam resist, hydrogen silsesquioxane (HSQ). Additionally, this chapter describes a process for the directed self-assembly of a cylinder-forming poly(styrene-*b*-dimethylsiloxane) (PS-PDMS) diblock copolymer within EBL defined HSQ templates. PDMS and HSQ are hard inorganic etch mask materials and thus offer high contrast when etching traditional CMOS materials such as Si and Ge. Consequently, the process outlined in this work is particularly applicable to nanolithography for continued device scaling towards the end-of-roadmap era.

5.2. Introduction

The drive for continued scaling of semiconductor devices over the last number of decades has put significant pressure on the key enabling technologies within the very large scale integrated circuit (VLSI) manufacturing industry, and particularly on the optical lithography techniques used to define semiconductor devices and integrated circuits (ICs).[1–3] The use of optical lithography has been extended far beyond the limits of the radiation wavelength through the use of several resolution enhancement techniques (RETs).[4] However, as continued scaling becomes significantly more difficult, alternatives to optical lithography are gaining in promise as potential routes to facilitate further scaling. Two such alternatives to optical lithography are, electron beam lithography (EBL), and directed self-

assembly (DSA) of diblock copolymers. This chapter describes the use of two promising examples of EBL and DSA processes for nanolithography applications, with a view to fabricating high-density arrays of Si nanowires with critical dimensions (CDs) less than 20 nm.

This chapter details the use of hydrogen silsesquioxane (HSQ) as a high-resolution EBL resist for Si nanowire fabrication and also on the use of HSQ gratings, prepared by EBL, as templates for the DSA of a cylinder-forming PS-*b*-PDMS diblock copolymer. HSQ is the highest resolution, commercially available, negative-tone EBL resist[5], and as such is suited to the fabrication of nanoscale structures with sub-20 nm CDs.[6] DSA of block copolymers (BCPs) using templates fabricated by traditional lithographic methods is the subject of significant research investment in the field of advanced lithography.[7,8] PS-*b*-PDMS is a BCP of particular interest in the field of DSA due to its relatively high Flory-Huggins interaction parameter (χ ~0.26 at STP) which may facilitate reduced line edge roughness (LER) in PS-*b*-PDMS derived structures.[9] The Flory-Huggins interaction parameter is essentially a measure of the degree of immiscibility of the blocks in a BCP. Consequently, the thickness of the intermaterial dividing surface (IMDS) at the interface between the two blocks in a BCP can be reduced by increasing the χ value of the BCP. A reduction in the IMDS inherently results in a reduction of the edge roughness of the polymer microphases.[10,11] In addition to a large χ value, PDMS offers improved etch resistance relative to analogous organic polymers when etched in conventional Si

or Ge etching processes.[9] DSA of PS-*b*-PDMS to produce substrate coplanar PDMS gratings has not yet been demonstrated using an EBL defined HSQ template. However, vertical PDMS pillar arrays have been produced via the DSA of PS-*b*-PDMS within an EBL defined HSQ pillar array template.[12] Furthermore, DSA of PS-*b*-PDMS to produce substrate coplanar PDMS gratings has been demonstrated within Si trenches patterned by interference lithography[9,13], however, this method is not suited to lithography on substrates such as silicon-on-insulator (SOI), where Si trench formation would result in undesirable consumption of the Si device layer.

5.3. Fabrication of Si Nanowire Arrays

Arrays of 11 nm wide HSQ lines were produced on SOI substrates using the HSQ EBL process outlined in Chapter 2.

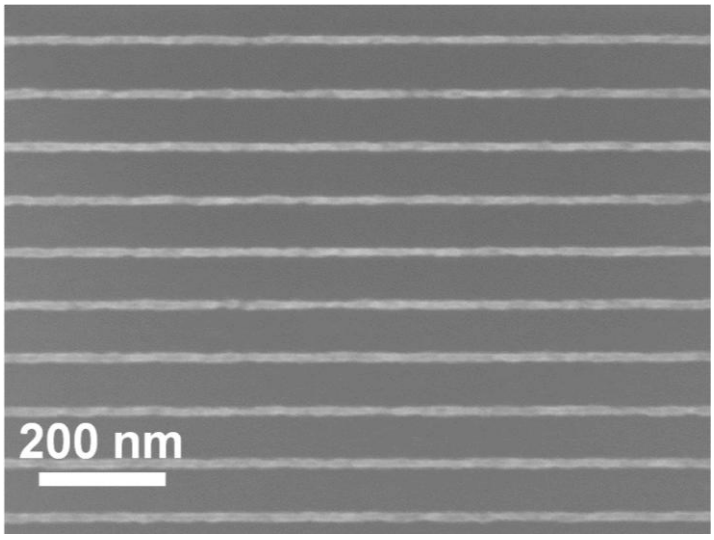

Figure 5.1. SEM image of 11 nm wide HSQ lines fabricated at a pitch of 85 nm on an SOI substrate. Lines were exposed at an areal dose of 1320 μC cm^{-2}.

The line edge roughness (LER) of the structures was extrapolated from SEM images, using *Image J* image processing software as detailed in Chapter 2, and was determined to be an average of 2.8 nm (3σ) for the 20 HSQ lines measured. An example of 11 nm wide HSQ lines, fabricated at a pitch of 85 nm, is shown in the SEM image in figure 5.1.

Figure 5.2 shows cross-sectional TEM images of Si nanowires produced using the HSQ EBL process. The nanowires had mean dimensions of 11 nm width and 12 nm thickness, and were produced at a pitch of 120 nm. The axes of the nanowires was designed to lie along the <100> crystal axis, as shown by the selected area electron diffraction (SAED) pattern in figure 5.2(c). The Cl_2 RIE, used to transfer the HSQ etch mask pattern to the SOI substrate, resulted in a pseudo-orthogonal etch profile as shown in figure 5.2(b). Consequently, all four exposed crystal faces of the nanowire were <100> oriented. The <100> crystal axis has been shown to exhibit the highest electron mobility for n-doped Si nanowires with high donor dopant concentrations[14], consequently <100> oriented n-Si nanowires are desirable for nanowire field effect transistor (FET) devices.

Large pads were also incorporated in the EBL mask design to facilitate future electrical contact to the nanowires as shown in the optical microscope image in figure 5.3. The presence of the Si pads allowed a larger contact area to the Si device layer on the SOI substrate, and thus lower electrical resistance in any resultant device.

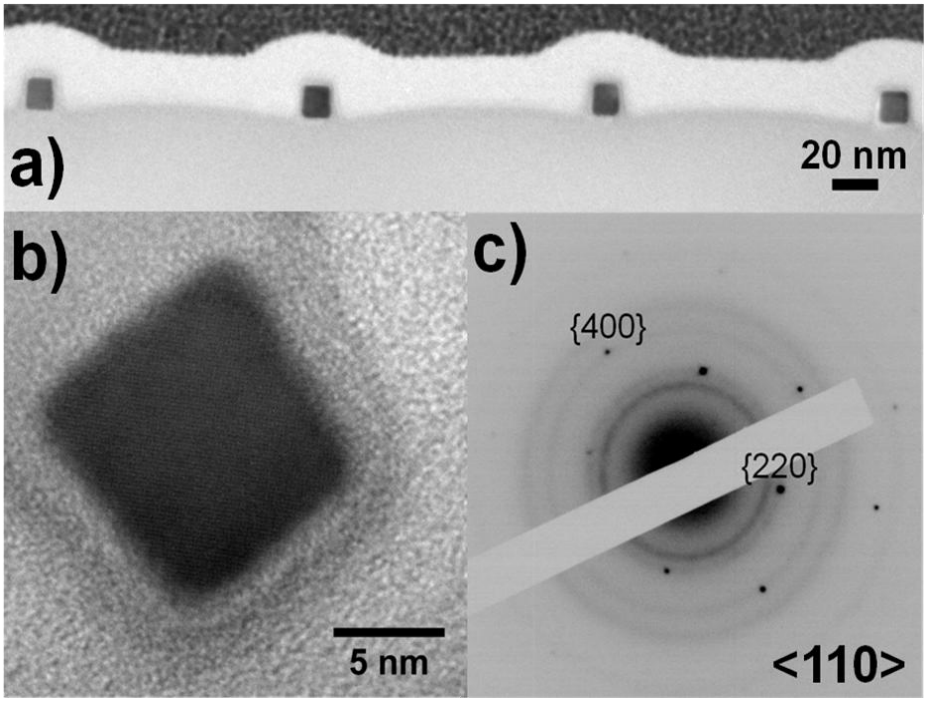

Figure 5.2 (a) TEM image of a cross-section through arrays of 11 nm wide Si nanowires at a pitch of 120 nm. (b) HRTEM image of a cross-section through a single nanowire highlighting the pseudo-orthogonal etch profile. (c) SAED pattern retrieved along the long axis of a Si nanowire confirming the <100> orientation.

The nanowire and pad pattern were transferred to the substrate using a Cl_2 RIE as detailed in Chapter 2, and the remaining HSQ mask was removed using 1 wt. % HF as detailed previously (Chapter 2, Section 2.3.6.). A uniform 10 nm thick film of Al_2O_3 was then deposited by atomic layer deposition (ALD) to act as a gate dielectric layer in field effect transistor (FET) devices prepared from the fabricated nanowire structures. Finally an Al gate was defined by EBL using a PMMA/MMA bilayer resist process (Chapter 2, Section 2.3.2.), via electron beam

induced Al evaporation and lift-off of the positive-tone PMMA resist. Figure 5.3 shows an optical microscope image of a single 10 nm wide Si nanowire bridging two Si pads. Figure 5.3 also shows a 40 nm wide Al gate perpendicular to the nanowire, thus producing a tri-gate type structure which has been shown to demonstrate superior control over charge carriers in the device channel and thus improved switching characteristics in devices implementing this type of gate structure.[15,16]

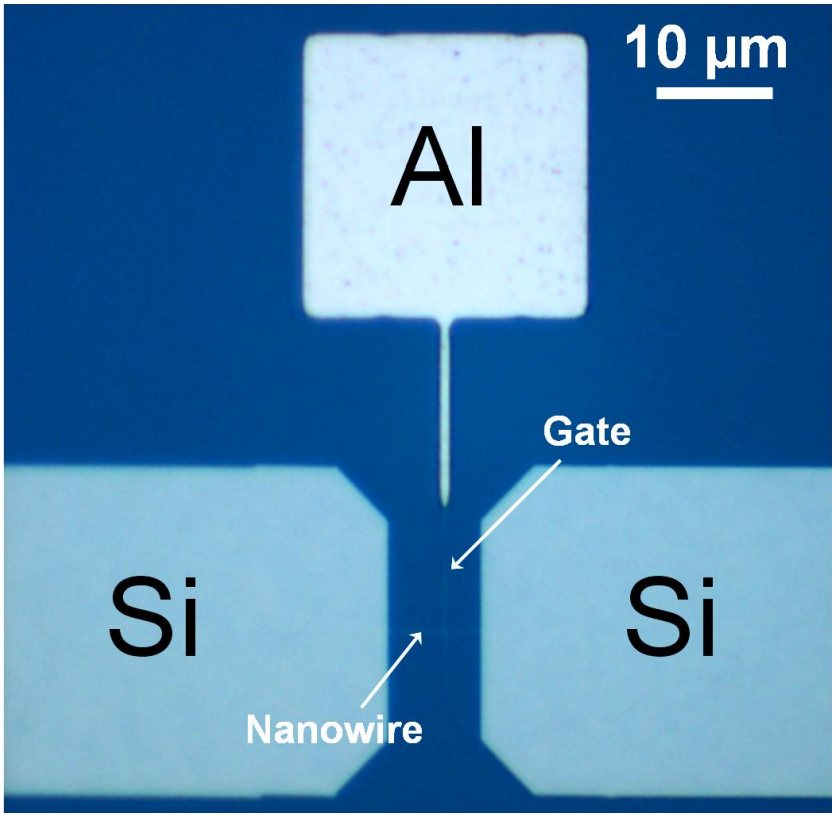

Figure 5.3. Optical microscope image of two Si pads connected by a single 10 nm diameter, 8 µm long, Si nanowire. The pad and nanowire have been coated in a 10 nm layer of Al_2O_3 by ALD, and a 40 nm wide Al gate has been deposited orthogonal to the Si nanowire.

5.4. Directed Self-Assembly of PS-*b*-PDMS

HSQ gratings prepared by EBL were also used as templates to direct the self-assembly of PS-*b*-PDMS diblock copolymer films. Figure 5.4 illustrates a schematic representation of the molecular structure of the PS-*b*-PDMS diblock copolymer and the morphology of the diblock copolymer film after microphase separation.[13]

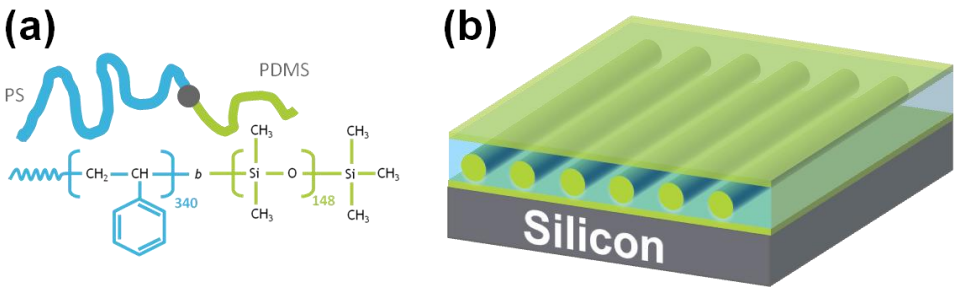

Figure 5.4. (a) A schematic representation of the structure of a PS-*b*-PDMS diblock copolymer molecule. The grey dot in the illustration represents the covalent bond between the PS and PDMS blocks. (b) Schematic portrayal of a PS-*b*-PDMS film following microphase separation by solvent annealing.

Figure 5.5 shows an SEM image of a PDMS 'fingerprint' pattern typically produced in the absence of a directing template. The SEM image in figure 5.5 was recorded following a sequential CF_4 and O_2 RIE to remove the upper PDMS layer and underlying PS layer respectively. Details of the RIE process steps are presented in section 2.3.7.

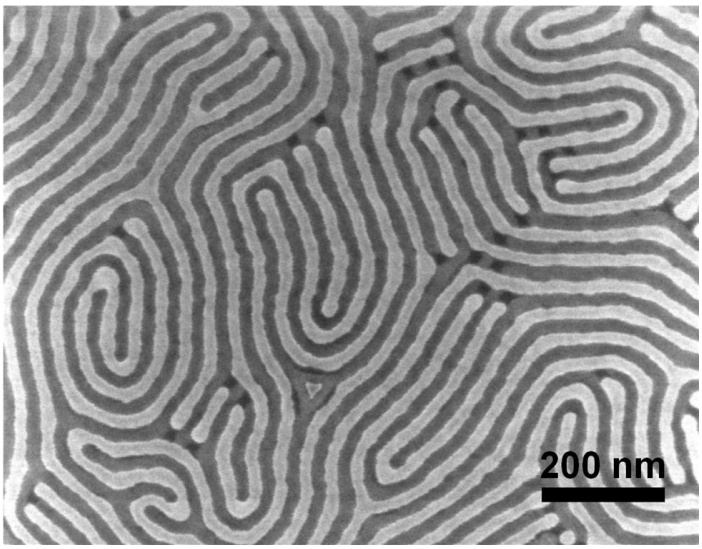

Figure 5.5. SEM image of a PDMS 'fingerprint' pattern produced by the self-assembly of PS-*b*-PDMS on a Si substrate using the solvent annealing process outlined in Chapter 2.

A range of different HSQ line patterns were prepared by EBL for DSA experiments. HSQ line arrays (10 × 10 μm) were exposed with a line-width of 15-20 nm, at pitches of 65, 100, 135, 205, 275, 345 and 415 nm which required exposure doses of 1100, 1400, 1700, 2000, 2400, 2700 and 3000 μC cm^{-2} respectively. The HSQ line pitch was increased in multiples of the expected 35 nm PDMS periodicity.[17] Two approaches were used to prepare aligned BCP films by DSA. In the first approach, a hydroxyl-terminated PDMS brush layer was chemically grafted to the patterned Si substrate as detailed in Chapter 2 (Section 2.3.7.). The PDMS brush layer binds to the hydroxyl terminated substrate via a condensation reaction.[18] The PDMS component of the BCP then preferentially wets the PDMS brush layer when the BCP is deposited on the substrate, as shown

schematically in figure 5.4 (b). However, as the PDMS brush is deposited globally, *i.e.* on both the trench floor and HSQ sidewalls of the patterned substrate, it was observed that the PDMS component of the BCP preferentially adhered to the HSQ sidewalls, as shown in figure 5.6. PDMS is chemically very similar to HSQ given that they both consist of an inorganic $(SiO)_n$ core. This chemical similarity between HSQ and PDMS makes selective etching of one with respect to the other very difficult, and as such HSQ lines cannot be selectively removed to allow production of a uniform grating after PS etching. Figure 5.6 shows an SEM image of the result of PS-*b*-PDMS alignment within PDMS brush-coated HSQ gratings, following a CF_4 RIE to remove the top PDMS layer and an O_2 RIE to remove PS lines. The result shows a repeating 60 nm wide PDMS-HSQ-PDMS line structure interspersed within the array of 20 nm wide PDMS lines. The average measured PDMS line period, width and edge roughness were 38.5 19.6, and 4.3 nm respectively.

A uniform linewidth is preferred for advanced lithography applications and as such, another approach had to be considered to prevent PDMS adhesion to the HSQ sidewalls. One possible approach would be to deposit the PDMS brush layer prior to HSQ deposition and EBL, however, the increased hydrophobicity of the PDMS-coated substrate impedes HSQ deposition which requires a more hydrophilic surface. As an alternative to the use of a PDMS brush, hexamethyldisilazane (HMDS) was applied to a patterned substrate as described in Chapter 2. The additional surface methyl groups produced at a HMDS treated

surface, relative to a PDMS treated surface, were expected to improve wetting of the organic PS component of the BCP. Figure 5.7 displays an SEM image of BCP alignment within HMDS coated HSQ gratings, following CF_4 and O_2 RIE processes. The SEM image clearly shows that PDMS no longer preferentially wets the sidewalls of the HSQ lines and as such facilitates the fabrication of a uniform mask grating.

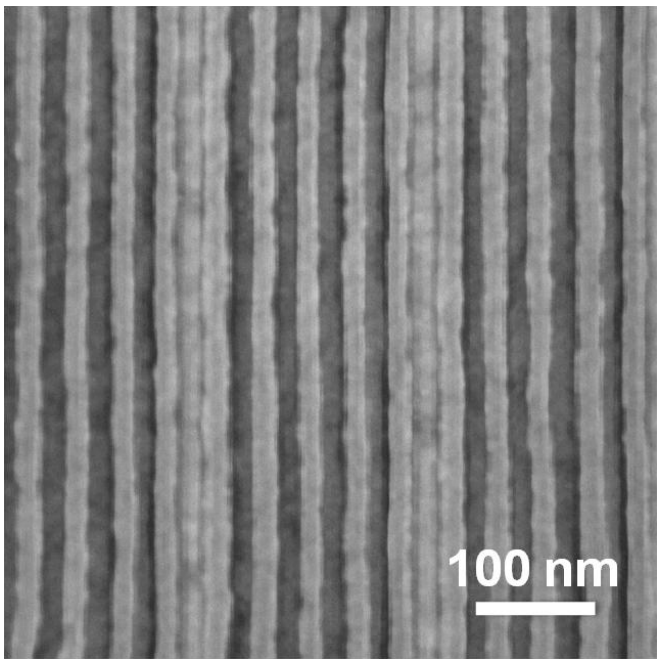

Figure 5.6. SEM image of aligned PDMS lines within a grating of 22 nm wide HSQ lines at a pitch of 205 nm on a PDMS brush coated surface.

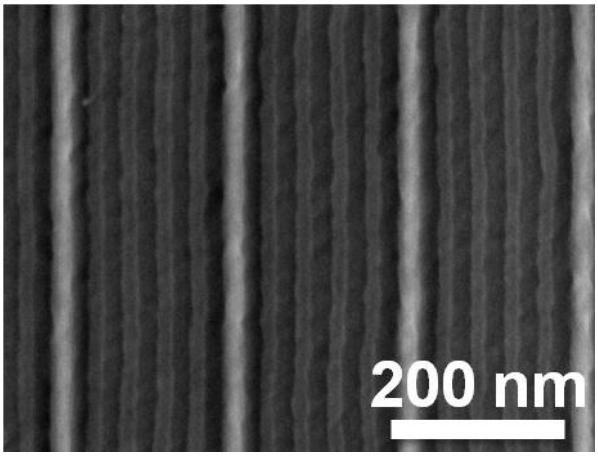

Figure 5.7. SEM image of aligned PDMS lines within a grating of 22 nm wide HSQ lines at a pitch of 205 nm on a HMDS treated surface.

The average PDMS line period, width and edge roughness were measured at 39.4, 19.3, and 5.0 nm respectively for this process. Figure 5.8 displays a TEM image of a cross-section through the line grating shown in figure 5.7. The TEM image clearly shows the uniform 5 nm thick PDMS layer on the trench floor. The TEM image also shows the profile of the HSQ and PDMS line grating. The PS/PDMS lines are 10 nm high and approximately 17 nm wide at the base. The HSQ line is 22 nm high, which is significantly less than the initial thickness of 50 nm expected after EBL. However, HSQ is known to etch at a rate of over 20 nm min^{-1} in a similar CF_4 RIE to that used in this work.[19] Consequently, significant consumption of the HSQ template can be expected during the CF_4 RIE procedure.

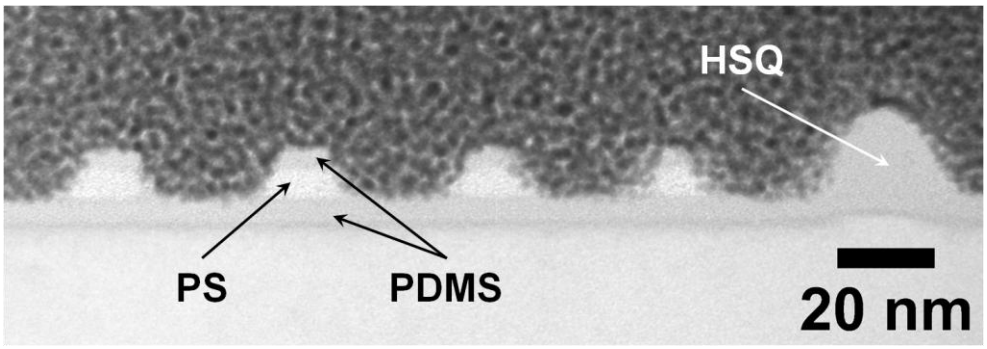

Figure 5.8. TEM image of a cross-section through aligned PDMS lines within a grating of 22 nm wide HSQ lines at a pitch of 205 nm on a HMDS treated surface.

A pitch of 205 nm was observed to produce the best alignment of BCP for both HMDS and PDMS-treated substrates, due to the observed PDMS line period of ~39 nm seen in figures 5.6 and 5.7. The PS-*b*-PDMS film produced consists of 19 nm diameter PDMS cylinders separated by 20 nm PS lines, in contrast to the 35 nm periodicity that had been expected. Taking the actual PS-*b*-PDMS periodicity of 39 nm into account, a HSQ template of 15 nm lines at pitches of 73, 112, 151, 190, 268, 346 and 424 nm would now be expected to support DSA and agrees with the observed DSA within the template having a pitch of 205 nm. The HSQ lines are 22 nm wide in figures 5.6-5.8 and not the 15 nm designed, resulting in an effective HSQ pitch of 198 nm. When the additional thickness of the PDMS or HMDS brush layers are further taken into account the effective HSQ line pitch is almost the desired 190 nm. Figure 5.9 shows an SEM image of PDMS lines within a template of 15 nm HSQ lines at a pitch of 190 nm. The sample has been partially etched as shown in figures 5.6 and 5.7, however, some of the overlying

PDMS layer still remains. Despite the incomplete PDMS etch, alignment of PDMS can be seen over the ~5 μm^2 area.

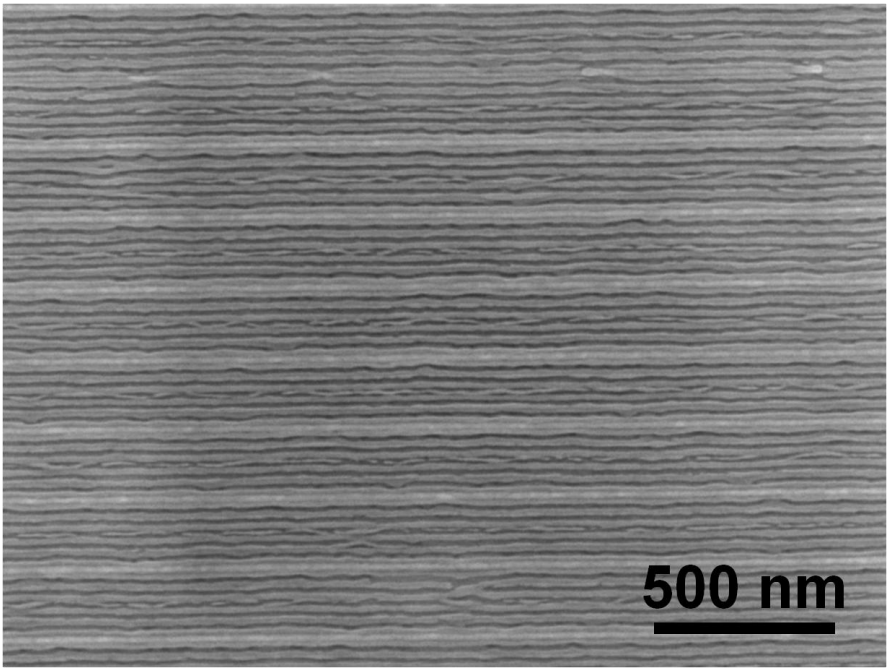

Figure 5.9. SEM image of a ~5 μm^2 area of aligned PDMS lines, within a template of 15 nm HSQ lines, at a pitch of 190 nm.

5.5. Conclusions

High resolution EBL using a HSQ EBL resist has been used to produce 10 nm diameter Si nanowires in FET device architectures. The EBL process demonstrated, is suited to the formation of fully depleted SOI, high-*k*, metal gate devices, with tri-gate architectures as demonstrated by the Si nanowire cross-section profile shown in this work. The high resolution EBL process shown here has also been used to guide the microphase separation of PS-*b*-PDMS by a

process of DSA. A process has been developed to improve wetting of PS to the HSQ template with respect to PDMS, thus allowing the fabrication of uniform 20 nm lines at a pitch of ~40 nm. The degree of BCP alignment within the HSQ templates was observed to depend significantly on the trench width of the template. The demonstrated importance of template dimensions and surface treatment suggests that both graphoepitaxy and chemical epitaxy mechanisms of DSA are at play in the present work.

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Chapter 6

Conclusions

6.1. Conclusions

Semiconductor nanowires have been the subject of extensive research investigation in the past number of decades for microelectronic applications and hybrids thereof. Chapter 1 of this thesis has summarised many of the routes toward semiconductor nanowire fabrication, and their integration in device architectures, with a primary focus on their application in the area of very large scale integrated circuits (VLSI).

Chapter 2 outlined the experimental processes used in the synthesis and fabrication of nanowires detailed in chapters 3-5. Chapter 2 also briefly introduced the analytical techniques used to probe the structure of the nanowires and nanopatterned surfaces produced in this body of research work.

Chapter 3 described a novel route toward the fabrication of Ge nanowires in the absence of a foreign seed metal catalyst. The work demonstrated control over the nanowire diameter through careful control of the synthesis temperature in the solvothermal nanowire synthesis process. Ge nanowires with diameters smaller than 10 nm have been prepared, which are of great interest for both fundamental quantum confinement studies as well as for potential applications in microelectronic devices. However, as with many bottom-up nanowire fabrication methods, the nanowires produced, exist as entangled meshes, thus inhibiting their integration into a VLSI manufacturing platform. Furthermore, the nanowires produced were encapsulated in an amorphous material composed of

decomposition by-product from the nanowire precursor compound. Whilst this amorphous material may act to passivate the nanowire surface, it may also impair electrical contact to the Ge nanowires and as such, a route to selectively remove this material is desirable. Additionally, identification of a suitable template, which is compatible with the solvothermal process used to produce these nanowires, may allow production of these nanowires in aligned arrays which are preferred for device fabrication.

The importance of surface chemistry in the fabrication of nanowire arrays by a top-down electron beam lithography (EBL) process was highlighted in Chapter 4. Therein, issues associated with the complex surface oxides of Ge and Bi_2Se_3 were discussed with respect to their effect on a high resolution EBL process using a hydrogen silsesquioxane (HSQ) EBL resist. Careful treatment of the surfaces of Ge and Bi_2Se_3 to remove oxide material which is soluble in HSQ developers, allowed the fabrication of array of features with critical dimensions less than 20 nm. Spectroscopic analysis of the surfaces of these materials confirmed the relationship between specific oxides at their surfaces and observations during inspection of the HSQ EBL process. Ultimately a greater understanding of the effect of specific surface oxides on EBL using HSQ has been developed, which may facilitate high resolution lithography with a HSQ resist on other industrially important materials. These materials may include arsenides such as GaAs, InAs and $In_{1-x}Ga_xAs$, and germanides or selenides such as GeSbTe and $Bi_2(Te_{0.8}Se_{0.2})_3$ due to the high solubility of As_2O_3, GeO_2 and SeO_2, respectively, in aqueous

bases, such as NaOH, and TMAH based HSQ developers.[1–3] The observations made in Chapter 4 are not specific to the use of HSQ as an EBL resist and so may also be important to the future use of HSQ in EUV lithography or ion beam lithography.[4,5] Application of the results reported in Chapter 5 to FET device fabrication should be the subject of future investigation. Such an investigation would rely on the availability of Ge or a similar high charge carrier mobility material on an insulating substrate such as Ge-on-insulator (GeOI).

In Chapter 5 a HSQ EBL process is detailed for the fabrication of Si nanowire arrays with sub-20 nm diameters and for the directed self-assembly (DSA) of a PS-*b*-PDMS diblock copolymer. Both DSA and EBL have received significant consideration as techniques to extend semiconductor device scaling. Whilst direct inclusion of EBL in VLSI manufacturing has been hindered by low wafer throughput, a hybrid process of EBL and DSA of BCPs may find favour. DSA of BCPs allows pattern multiplication and thus reduces the resist area to be exposed during the EBL step and so increases throughput. However, DSA is not yet a mature technology. The DSA process outlined in Chapter 5 has demonstrated successful alignment of PDMS domains over an area of a few square micrometres, however, more extensive patterns will be required for DSA to be implemented on an industrial scale. Additionally, DSA will have to be demonstrated on different materials, such as Cu for definition of interconnects in VLSI manufacturing, for example.

Continued scaling of semiconductor devices alone will not allow perpetual advancement in computing power, speed and efficiency of VLSIs. Although device scaling is expected to continue for a decade or more, new materials and architectures are expected to dominate future VLSI developments.[6] Throughout this thesis, fabrication routes facilitating continued device scaling have been emphasised. However, candidate materials for future devices have also been stressed. For example, Ge exhibits significantly higher charge carrier mobility than Si. In this thesis, bottom-up and top-down routes to Ge nanowire structures with CDs below 20 nm have been developed. However, even with the improved carrier mobility of Ge with respect to Si, current strained Si devices are expected to outperform equivalent unstrained Ge analogues.[7] Consequently, future areas of semiconductor nanowire research may be directed toward strain engineering of materials with inherently high charge carrier mobility. Doping Ge with Sn is one possible route to achieve a strained Ge material with improved electrical performance.[8,9] Another route, is the fabrication of a quantum well structure with a lattice mismatched material such as layered $In_xGa_{1-x}As$.[10] In the short-term, strain engineering looks likely to play a pivotal role in semiconductor device research and consequently should be the subject of continued consideration in future nanowire research.

Future logic devices such as those found in VLSI technology may not rely on charge alone to function. Devices based on spin transport have been the subject of significant research investment in recent years. Spin transport has been

demonstrated in both conventional semiconductor nanowires and those doped with magnetic elements.[11–13] Spin-based devices may offer a route to low power logic circuits desirable in future VLSI technology. Topological insulators such as Bi_2Se_3 and Bi_2Te_3 are also of significant interest for quantum computing applications, whereby information can be transferred as quantum bits built from topological surface states.[14,15] Nanowires of these materials are then desirable to create high density arrays of quantum computing structures.

The data reported in this thesis has outlined routes to overcome significant hurdles to the future integration of semiconductor nanowires in VLSI technology. The results herein will support future investigations in semiconductor nanowire fabrication, which is a field of great importance to a vast number of applications.

6.2. Bibliography

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