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Electrical Characterization of High Performance, Liquid Gated Vertically Stacked SiNW-Based 3D FET for Biosensing Applications

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Abstract

A 3D vertically stacked silicon nanowire (SiNW) field effect transistor featuring a high density array of fully depleted channels gated by a backgate and one or two symmetrical platinum side-gates through a liquid has been electrically characterized for their implementation into a robust biosensing system. The structures have also been characterized electrically under vacuum when completely surrounded by a thick oxide layer. When fully suspended, the SiNWs may be surrounded by a conformal high-κ gate dielectric (HfO_2) or silicon dioxide. The high density array of nanowires (up to 7 or 8 × 20 SiNWs in the vertical and horizontal direction, respectively) provides for high drive currents (1.3 mA/μm, normalized to an average NW diameter of 30 nm at V_{SG} = 3V, and V_d = 50 mV, for a standard structure with 7 × 10 NWs stacked) and high chances of biomolecule interaction and detection. The use of silicon on insulator substrates with a low doped device layer significantly reduces leakage currents for excellent I_{on}/I_{off} ratios > 10^6 of particular importance for low power applications. When the nanowires are submerged in a liquid, they feature a gate all around architecture with improved electrostatics that provides steep subthreshold slopes (SS < 75 mV/dec), low drain induced barrier lowering (DIBL < 20 mV/V) and high transconductances (g_m > 10 μS) while allowing for the entire surface area of the nanowire to be available for biomolecule sensing. The fabricated devices have small SiNW diameters (down

to d_{NW} ~ 15-30 nm) in order to be fully depleted and provide also high surface to volume ratios for high sensitivities.

Silicon nanowire field effect transistors (SiNW FETs) have provided a versatile platform for the ultra-sensitive and selective detection (through surface modification) of simple molecules [1, 2], ions [1, 3], and biological entities such as viruses [2], proteins [1], and DNA [4], ever since Cui et al., [1] produced the first SiNW pH sensor based on the pioneering work of Bergveld [5, 6]. The interest in nanostructures for sensing stems from their ultra-small dimensions that give rise to large surface to volume ratios (S/V). For such structures, a small number of charged biomolecules on the surface can efficiently modulate the conduction channel making the devices greatly sensitive in comparison to the planar (surface only) ion sensitive field effect transistor (ISFET) sensor that Bergveld introduced. SiNWs have therefore been widely utilized as FET-based biosensors since their first implementation. Nonetheless, their transistor characteristics in a liquid environment have seldom been thoroughly studied. Therefore in the present work, a 3D vertically stacked SiNW-based structure has been electrically characterized as gated through a liquid by a backgate and one or two symmetrical platinum side-gates (SG_1, SG_2, Fig. 1). Our results were briefly introduced previously [7] but more thoroughly explained here.

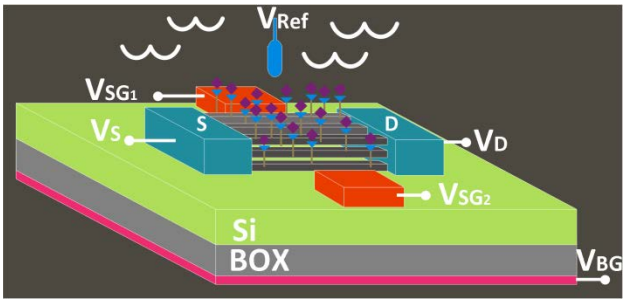

Figure 1. Schematic of 3D vertically stacked SiNW FET biosensor. Three rows of three NWs vertically stacked in between source and drain anchors, two side-gates and a reference electrode (not used here) on a SOI substrate.

Principle of operation

An ISFET is a device analogous to a metal oxide semiconductor field effect transistor (MOSFET) for which the metal gate has been separated from the gate oxide and replaced by a reference electrode (RE) or local side-gate electrode. The electrode makes contact with the gate dielectric through the liquid that contains the analyte to be sensed (e.g., pH concentration).

For a conventional MOSFET, in the linear region when $V_G > V_{th}$ (and $V_d < V_G - V_{th}$) the drain current I_d relationship with respect to V_G (with V_G being the gate voltage, V_d the drain voltage and V_{th} the threshold voltage) is given in Eq. 1 [8]:

$$I_d = C_{ox}\mu\frac{W}{L}\left[(V_G - V_{th})V_d - \frac{1}{2}V_d^2\right] \qquad \text{Equation (1)}$$

C_{ox} is gate oxide the capacitance per unit area, W and L are the width and length of the channel, μ is the electron mobility. With the threshold voltage (Eq. 2):

$$V_{th} = \frac{\phi_M - \phi_{Si}}{q} - \frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}} + 2\phi_f \qquad \text{Equation (2)}$$

ϕ_M and ϕ_{Si} are the work function of the gate electrode and the silicon respectively, q is the elementary charge and Q_{ox}, Q_{SS} and Q_B are the oxide charge, interface charge and depletion layer charge in the silicon accordingly. Finally, ϕ_f is the Fermi level difference between doped and intrinsic silicon.

In analogy, for an equivalent ISFET device, adsorbed charged molecules (e.g., H^+ ions) produce a surface potential φ_0 on the gate oxide resulting in V_{th} change (Eq. 3):

$$V_{th} = V_{ref} - \varphi_0 + \chi^{sol} - \frac{\phi_{Si}}{q} - \frac{Q_{ox}+Q_{ss}+Q_B}{C_{ox}} + 2\phi_f \qquad \text{Equation (3)}$$

V_{ref} is the reference electrode potential, φ_0 is the surface potential and χ_{sol} the solution's dipole moment. For a fixed V_{ref}, only the surface potential changes as a function of pH. The drain current for an ISFET then becomes (Eq. 4):

$$I_d = C_{ox}\frac{W}{L}\left[\left(V_G - V_{ref} - \varphi_0 + \chi^{sol} - \frac{\phi_{Si}}{q} - \frac{Q_{ox}+Q_{SS}+Q_B}{C_{ox}} + 2\phi_f\right)V_d - \frac{1}{2}V_d^2\right] \qquad \text{Equation (4)}$$

The surface potential change $\Delta\varphi_0$ with respect to a pH value change$\left(\frac{d\varphi_0}{dpH}\right)$ has been derived from the site-binding (SB) and Gouy-Chapman-Stern (GCS) model [9-13], Eq. 5:

$$\frac{d\varphi_0}{dpH} = 2.303\alpha\frac{kT}{q} \quad \text{Equation (5)}$$

With κ being the Boltzmann constant, T the absolute temperature and α is the dimensionless sensitivity parameter (α = 0 – 1), Eq. 6:

$$\alpha = \frac{1}{(2.3\kappa T C_{diff}/q^2\beta_{int})+1} \qquad \text{Equation (6)}$$

C_{diff} is the differential capacitance that depends on the sensing solution's ion concentration and the β_{int} is the intrinsic buffer capacitance of the dielectric. The sensitivity parameter therefore reaches unity depending on the gate dielectric utilized, the ionic concentration of the solution and temperature. The resulting threshold voltage shift ΔV_{th} in the I_d-V_{ref} characteristic reaches the thermodynamic Nernst limit of 59.5 mV/pH (at room temperature T = 300 K) as the sensitivity parameter α approaches unity.

Sensitivity

Typically in literature, the sensitivity S is defined as the absolute $S = \left(I_{d\psi 0} - I_{d\psi 1}\right)$ or the relative variation of current or conductance G, $S = (I_{d\psi 0} - I_{d\psi 1})/\, I_{d\psi 0}$ due to a difference in the external potential (sensing event) with $I_{d\varphi 0}$ being the baseline current and $I_{d\varphi 1}$ being the current induced by the sensing event. Fig. 2 illustrates how the inherent transistor characteristics of the

FET device, namely the subthreshold slope $SS = dV_{SG}/d(\log_{10} I_d)$ and the ΔV_{th} shift resulting from the electric field induced by a sensing event both represent an upper limit to the sensitivity of a given device when biased in the subthreshold region. It is well known that for a field effect transistor the subthreshold slope is limited to ~ 60 mV/dec (at room temperature). The current change per pH (and hence the sensitivity of the device) reaches a maximum of 1 dec/pH for a device with a SS of 60 mV/dec for which a pH change induces an ideal Nerstenian V_{th} shift of almost 60 mV/pH at room temperature (grey-solid curves, Fig. 2). Even if the sensing surface can provide a Nerstenian response of ~ 60 mV/pH ($\alpha \rightarrow 1$) if the subthreshold slope of the device increases, the sensitivity suffers (pink-dashed curves, Fig. 2).

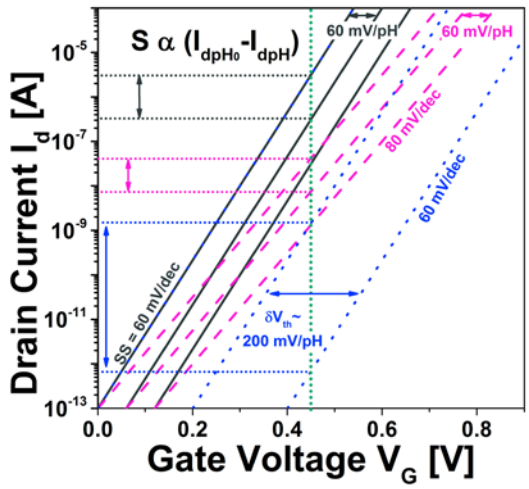

Figure 2. I_d -V_G curves illustrating how the drain current and hence the sensitivity changes with a change of pH that induces a V_{th} shift of 60 mV/pH (grey-solid and pink-dashed curves) and 200 mV/pH (blue-dotted), for a transistor with a SS slope of 60 mV/dec (grey) and 80 mV/dec (pink), in the subthreshold region.

SiNW based FET sensors in a double gate configuration (e.g., local liquid side-gate V_{SG} and backgate V_{BG}) have been shown to have I_d-V_{SG} characteristics for which the threshold voltage

shifts surpasses the Nernst limit as the pH changes [3, 14-18]. The dual gate configuration allows for the amplification of the surface potential when one gate acts as the tuning gate and the other as the driving gate of the FET. In the backgate-liquid gate configuration one gate acts as a driving gate that controls the current flow within the NW while the other acts a supporting gate that amplifies the threshold voltage shift as a function of pH [17, 18]. Fig. 2 (blue-dotted curves) illustrates how a threshold voltage shift beyond the Nerst limit (in here 200 mV/pH) results in gigantic drain current change and hence enhanced sensitivities.

The 3D vertically stacked SiNW FET

In here, 3D vertically stacked SiNW FET devices (Fig. 3a top side view of device and b, c close-up) fabricated using conventional, top-down clean room processes [19, 20] have been characterized electrically in a dry and liquid environment. The device consists of a high density array (up to 8 × 20 SiNWs) of ultra-thin (d_{NW} < 35 nm) suspended SiNWs anchored in between highly doped (n^+ phosphorous > 10^{18} cm^{-3}) extensions that act as a source and drain and one or two symmetrical Pt gate electrodes to the sides (Fig. 3b, c, d). The high SiNW density (Fig. 3e) guarantees the high utilization of the bulk silicon substrate, high output currents [21, 22] and high opportunities for biomolecule interactions as the number of conduction channels increases in more than one direction. The entire surface area of the SiNWs is exposed to the sensing environment as the NWs are suspended. Electrostatic control can be achieved by the use of one or both local side-gates or the backgate through the liquid surrounding the NWs in a gate all around (GAA) configuration or an integrated reference electrode (not used here). The entire wafer/chip is covered with an SU-8 epoxy layer except for small windows (30 × 30 μm^2) where the NWs will have contact with the sensing or gating liquid (Fig. 3b). The contact pad areas (100 × 100 μm^2) located on either side of the chip and 1 mm away from the sensing window are also left open (Fig 3a),.

Wire bonding to a printed circuit board (PCB) or direct electrical probing can then be easily accomplished. The chip layout allows for enough space for a microfluidic channel to be directly bonded to the top of the structures (Fig. 3f). A droplet can also be simply placed on top of the NW window to allow for liquid gating and quick electrical characterization as done here.

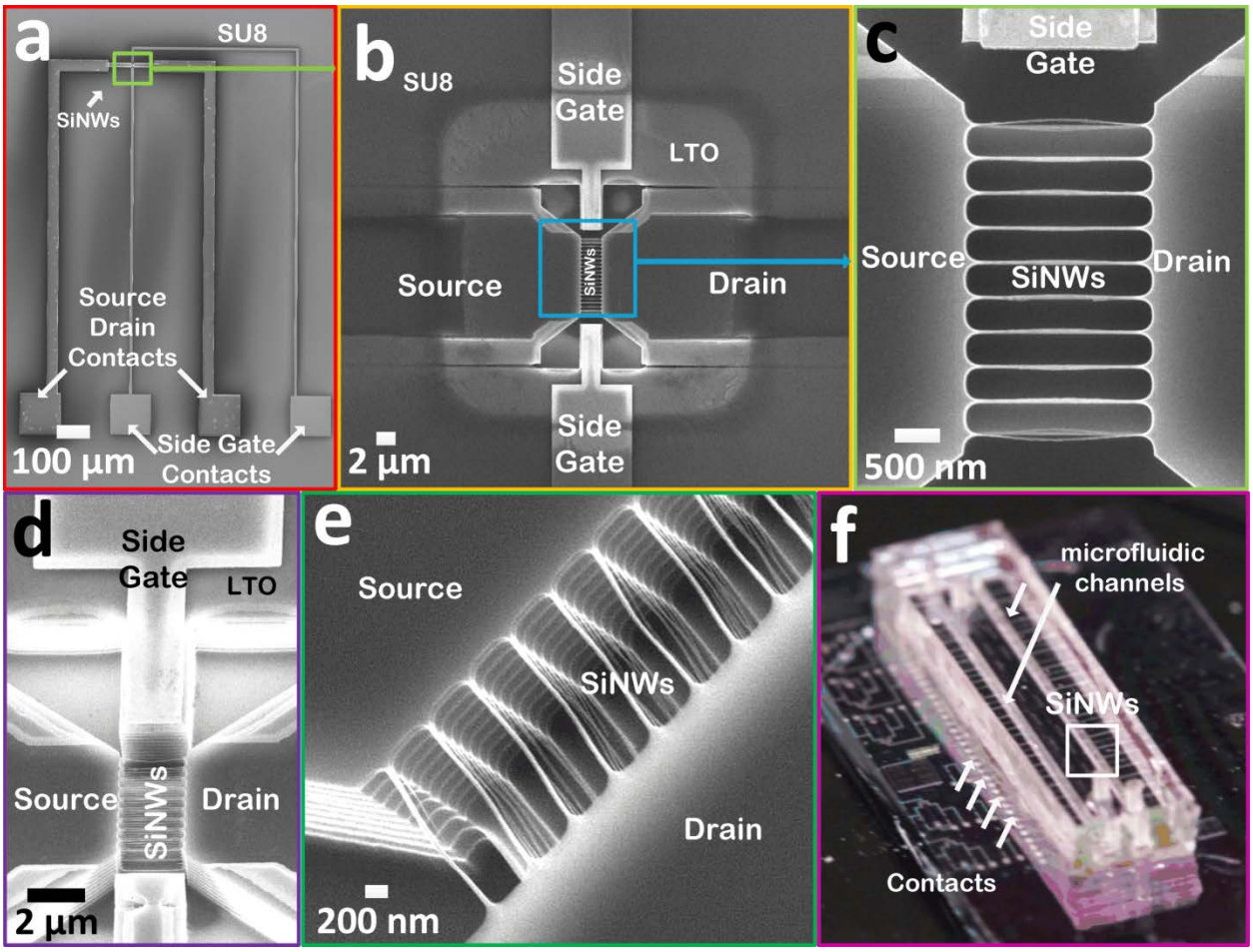

Figure 3(a) SEM top-side view of the entire device with two side-gates, source and drain contacts shown, **(b, c)** close-up shows source, drain, side-gates and NW area. The entire structure except for a small area is covered with SU-8, **(d)** top-side tilted view of suspended SiNWs, **(e)** close-up showing the silicon nanowires vertically stacked, **(f)** PDMS microfluidic channels on top of devices with contact openings shown.

The 3D FET structures were fabricated by using the natural scalloping effect resulting from consecutive BOSCH cycles and thermal oxidation [7, 20]. In order to accomplish electrical isolation from the bulk Si, the outline that defines each device was designed to have a width larger than the trench openings used to form the NW precursor scallops by the BOSCH process (T = 300 nm or 200 nm), Fig. 4a, b. This guarantees that as the last NW scallop is formed it will touch the silicon on insulator's (SOI) BOX so that every device "floats" on top of an SiO_2 layer (1 µm, Fig. 4b). Also, the ion implantation hard mask (low thermal oxide, LTO) that serves to protect the NWs during the fabrication process further isolates each FET (Fig. 4c).

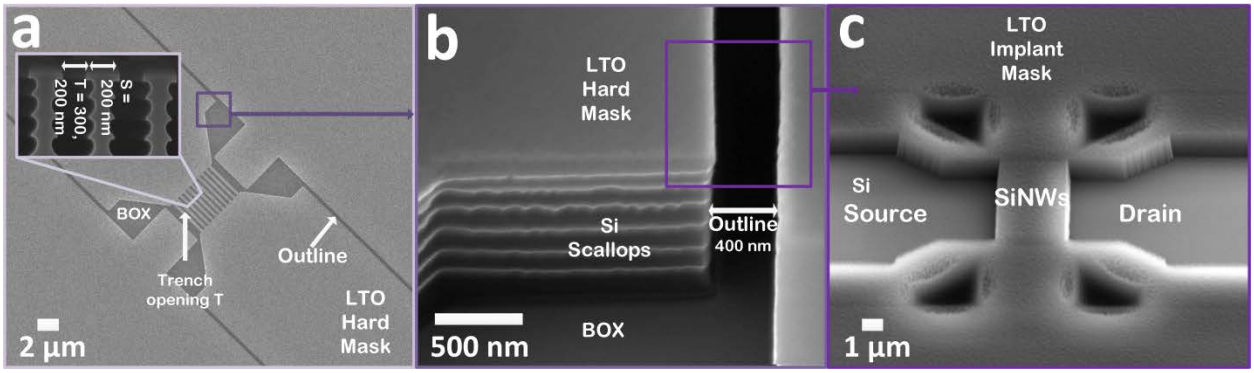

Figure 4(a) Top-side view of etched structure's outline, inset shows the scallops produced by BOSCH (S = 200 nm and T = 200 or 300 nm), **(b)** tilted-side view of scalloped outline right on top the SOI's BOX layer, **(c)** tilted-side view of structure after LTO hard mask is deposited and S/D openings are etched for implantation.

The oxide (thermal oxide + LTO) surrounding the SiNWs that protects them during the long fabrication is removed in a buffered oxide etch (BOE) bath at the end of the process. The SiNW vertical and lateral density is determined by the BOSCH process parameters and initial mask dimensions (S and T, Fig. 4a inset) [19, 20]. The number of NWs that can be stacked in the vertical direction is limited by the SOI's device layer thickness (1 µm in here) but the number of NWs that

can be fabricated in the horizontal direction is for all practical purposes unconstrained. Fig. 5a, b shows the two types of arrays of SiNWs that were fabricated here. The first one has a constant density of 7 SiNW/µm in the vertical direction and 1.9 SiNW/µm in the horizontal direction. The second structure has a density of 8 SiNW/µm in the vertical direction and 2.4 SiNW/µm in the horizontal direction. Devices with varying number of SiNWs in the horizontal direction (10, 15 and 20 NWs) and source to drain lengths (2, 3, 4 µm) were fabricated. The fabrication process has been presented in detail in an earlier publication [19].

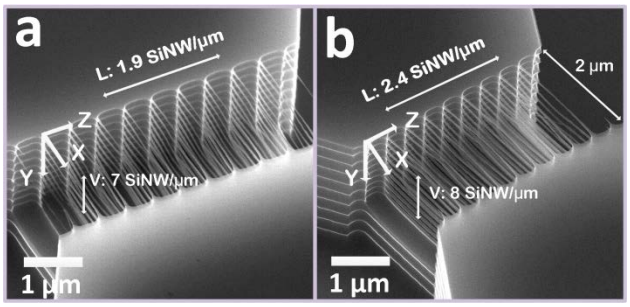

Figure 5. SEM top-side tilted views of SiNWs arrays with two different vertical and horizontal SiNW densities and diameters: **(a)** V = 7 SiNW/µm, H = 1.9 SiNWs/µm, d_{NW} = 15-30 nm and **(b)** V = 8 SiNW/µm, H = 2.4 SiNWs/µm, d_{NW} = 25-35 nm (L = 2 µm).

Results and Discussion

The 3D FET device output and transfer characteristics were first obtained in ambient conditions (dry) prior to removing the SiO_2 that surrounds the NWs. The measured drain current curves as a function of drain potential (I_d – V_d) with increasing backgate voltage values (V_{BG} = 0 – 40 V, V_{SG} = 0 V) for an array with 7 × 10 SiNWs (number of NWs in the vertical and horizontal directions, respectively) and d_{NW} ~ 45 – 55 nm are shown in Fig. 6. The curves are representative of the behavior of all measured devices.

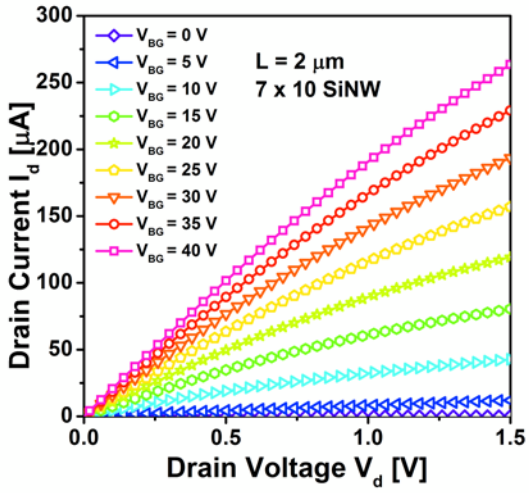

Figure 6. I_d-V_d curves with increasing backgate potentials (V_{BG} from 0 to 40 V) for a 7 × 10 SiNWs structure prior to thermal oxide removal by BOE, (V_{SG} = 0 V, L = 2 μm).

The I_d-V_{BG} curves at high (V_d = 1 V) and low (V_d = 50 mV) drain voltages for the same structure (7 × 10 SiNWs) are shown in Fig. 7.

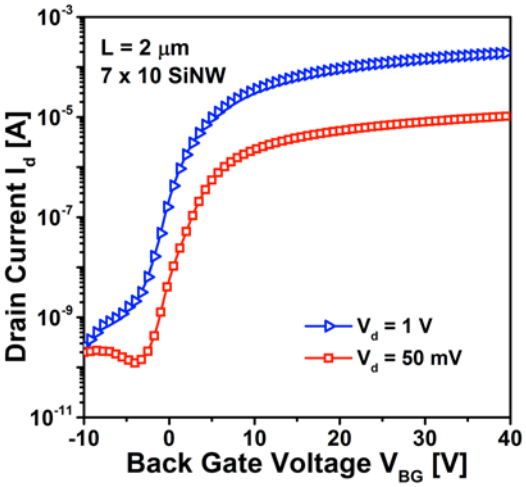

Figure 7. I_d-V_{BG} curves for high (V_d = 1 V) and low (V_d = 50 mV) drain potentials for 7 × 10 SiNWs structure with L = 2 μm, d_{NW} = 45 – 55 nm prior thermal oxide removal by BOE.

The I_{on} current, defined as the current at which V_{BG} = 10 V and V_d = 50 mV, normalized to NW diameter d_{NW} = 55 nm for this structure (7 × 10 SiNWs, L = 2 μm), was found to be 40.5 μA/μm. The leakage current (I_{off}), defined as the I_d at V_{BG} = 0 V, V_d =50 mV was found to be 0.1 μA/μm (normalized to d_{NW} = 55 nm). The threshold voltage V_{th} is defined as the voltage for which the drain current reaches a value of $I_d = (100\ \mu A * d_{NW}/L)$ as it is typically defined in industry [23]. A high backgate potential is needed in order to operate the device with a V_{th} = 11.6 V. A subthreshold slope of 1.6 V/dec was extracted from Fig. 7. As can be seen in Fig. 8, approximately 70 nm of silicon oxide surround the SiNWs prior to oxide removal. Electrostatic control through the thick oxide (ε = 3.9) under dry conditions was therefore found to be poor as the high SS and V_{th} values and transfer characteristics indicate.

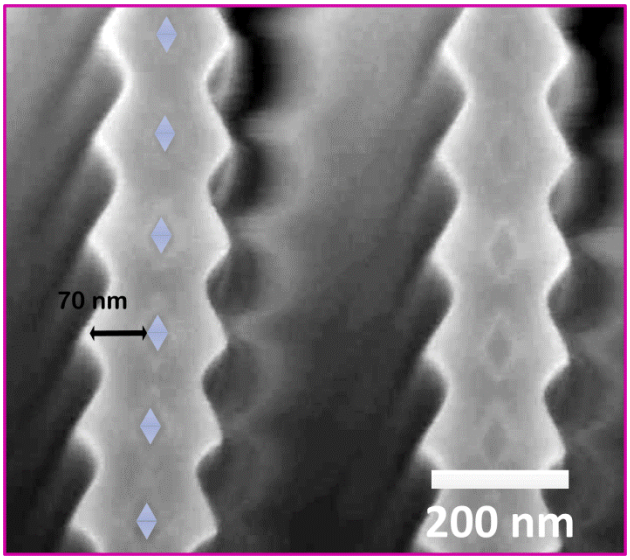

Figure 8. SEM cross section views of the SiNWs still within their SiO_2 enclosure from [20].

Liquid gated experiments

After the oxide was removed to produce suspended SiNWs, the devices were characterized electrically in a liquid environment (isopropanol IPA, ε = 18) by the use of the backgate or Pt side-gates (SG). Native oxide forms spontaneously (~ 2 nm) around the suspended nanowires after they

are exposed to ambient air, acting as a gate dielectric. The measurements were repeated several times (Fig. 9, for 8 × 10 SiNW, L = 2 μm). The use of the Pt electrode to gate the SiNW array through a liquid environment proved to produce repeatable measurements. Moreover, the transistor characteristics were obtained for different devices with the same parameters (length and number of NW) within the same die and were found to be comparable (Fig. 10).

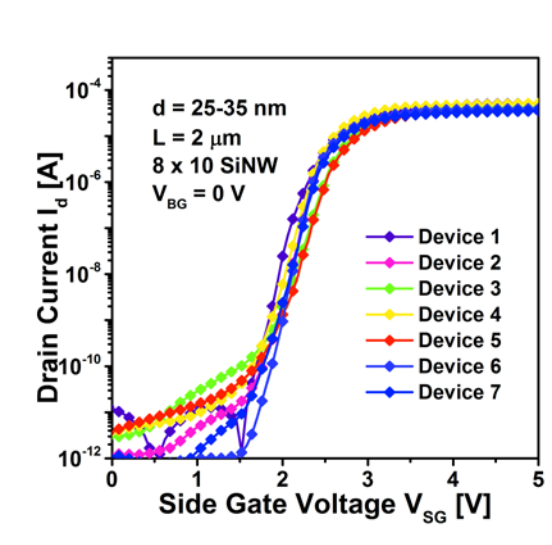

Figure 9. I_d-V_{SG} measurement repeated several times for an 8 × 10 SiNWs structure, L = 2 μm, d_{NW} = 25-35 nm, V_d = 50 mV and native oxide gate dielectric tested in a liquid environment with a Pt side-gate.

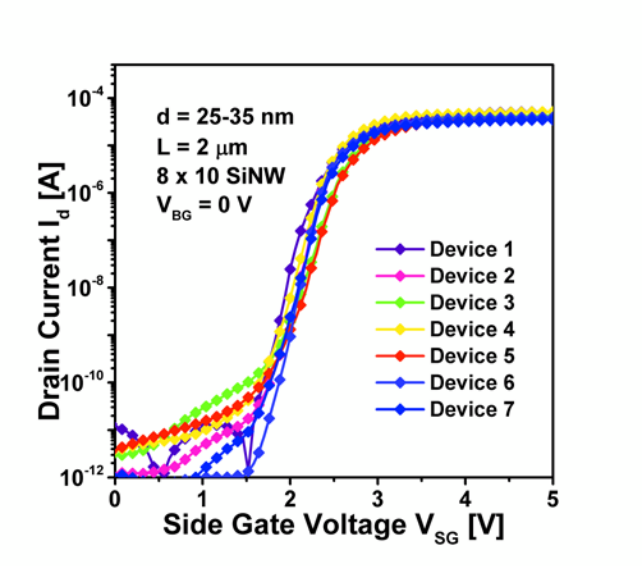

Figure 10. I_d-V_{SG} measurements for different devices with the same geometric characteristics within the same die: 8 × 10 SiNWs structures, L = 2 μm, d_{NW} = 25-35 nm, V_d = 50 mV, native oxide gate dielectric tested in a liquid environment with a Pt side-gate.

The I_d vs. V_{SG} curves for a forward (solid) and reverse (open) sweep are shown in Fig. 11 for a 8 × 15 SiNW structure with L = 2 μm. The V_{th} shifts slightly towards the left indicating a positive charge accumulation. Injected interface charges that do not dissipate as the gate bias polarity changes lead to a shift in the threshold voltage [24]. Hysteresis can affect the short term, and long term drift of the sensor response [25]. In here little hysteresis (< 15 mV) is found indicating small surface and interface (Si/SiO_2) defect induced charge trapping [24].

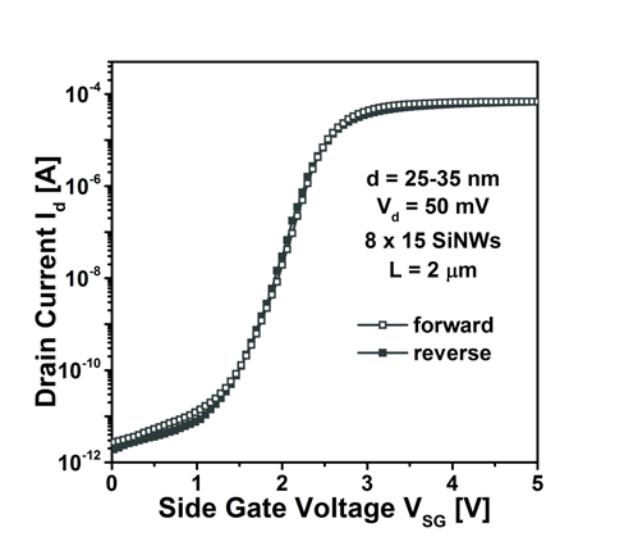

Figure 11. I_d-V_{SG} curves for forward (solid) and reverse (open) sweep for a 8 × 10 SiNWs structure, L = 2 μm, d_{NW} = 25-35 nm and native oxide gate dielectric tested in a liquid environment.

The I_d-V_{SG} (V_S = V_{BG} = 0 V) for increasing drain potentials (V_d = 50 mV – V_d = 1 V) for structures with 7 × 10, L = 2 μm are presented in Fig. 12 and Fig. S1 (supplementary information), respectively.

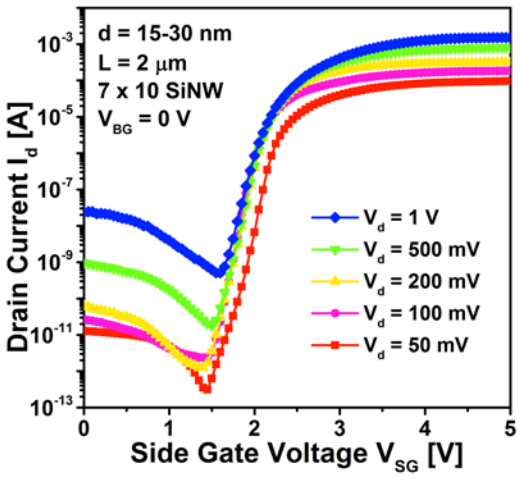

Figure 12. I_d-V_{SG} curves for increasing drain potentials (V_d =50 mV – 1 V) of 7 × 10 SiNWs structure, L = 2 μm, d_{NW} = 15-30 nm and native oxide gate dielectric tested in a liquid environment.

The drain-leakage current here is the current at V_{SG} = 0 V. The I_{on} current is defined as the value of I_d at V_{SG} = 3 V (normalized to average NW diameter). In terms of device performance, at low drain potentials V_d < 500 mV, the devices show very low drain leakage currents (I_{off} < 2.1 × 10^{-6} mA/μm), high I_{on} (> 2 mA/μm) and high I_{on}/I_{off} ratios (> 10^6) as can be seen in Fig. 13. At high drain potentials nevertheless, the I_{off} increases dramatically (e.g., I_{off} > 7 × 10^{-4} mA/μm when V_d = 1 V) degrading the I_{on}/I_{off} ratio down to < 1.7 × 10^4 (V_d = 1 V). Large leakage currents through the liquid from source to drain ~~are~~ have successfully being reduced by covering all but a small area around the NWs with an SU-8 layer. Fabrication process variations account for the small differences in performance (I_{on}, I_{off}, SS) and seemingly contradictory results (higher I_{on} currents for the 7 × 10 structures) between the 7 × 10 and 8 × 10 SiNW structures (and in general) as the two types of devices were fabricated at different times in a research setting. Therefore we do not try to compare the two but analyze the trends seen for both types of structures. As will be seen, the trends are comparable and speak of the robustness of the fabrication process.

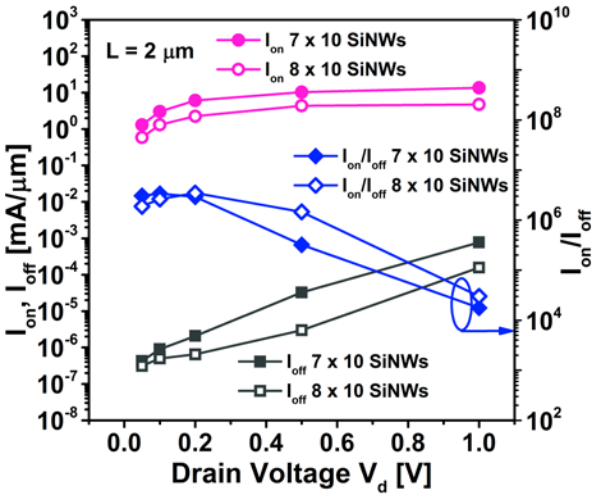

Figure 13. I_{on} and I_{off} (left) normalized to nanowire diameter (d_{NW} = 15-30 for 7 × 10 SiNWs and d_{NW} = 25-35 for 8 × 10 SiNWs FET) and I_{on}/I_{off} current ratios (right) as a function of drain voltage with L = 2 μm, native oxide as a gate dielectric and tested in a liquid environment.

The drain induced barrier lowering (DIBL) is defined as the induced reduction in threshold voltage at high drain voltages. The DIBL occurs when the height of the energy barrier that impedes carrier's flow through the channel for a gate potential below threshold is reduced by the electric field induced by the drain potential, an effect of particular importance for short channel devices. Higher drain bias decreases the potential barrier and a conduction channel will form at lower gate potentials therefore decreasing the threshold voltage. The DIBL is defined here as DIBL = $\frac{V_{th}|V_{d,low} - V_{th}|V_{d,high}}{V_{d,low} - V_{d,high}}$ with $V_{d,high}$ = 1 V and $V_{d,low}$ = 100 mV. The DIBL for all devices was found to be relatively small (< 70 mV/V). Though the NWs are long (L = 2, 3, 4 μm) by any standards, as the drain potential increases, it can also have a bigger influence on the surface potential along the NW gate channel through the liquid (drain/source parasitic capacitance through the liquid to the NW stack) resulting in an increase of electron injection from source to drain through the NWs. The low DIBL nevertheless points out to the fact that the leakage current occurs mostly from source to drain through the liquid. This can be mitigated by using low drain voltage potentials that are also favorable for low power applications.

The SS values calculated from I_d-V_{SG} curves (V_{BG} = 0 V and V_d = 50 mV) were found to be steep SS < 100 mV/dec and < 130 mV/dec for both 7 × 10 and 8 × 10 SiNWs structures, respectively (Fig. 13 and Fig. S1, supplementary information). These values are comparable to the lowest subthreshold slope values reported in literature for liquid gated SiNW FET devices (~ 100 mV/dec) [26].

The configuration of the 3D vertically stacked sensor permits an enhanced electrostatic control of the SiNW channels by the possibility of applying symmetric or asymmetric gate potentials through the liquid. Fig. 14 shows the I_d-V_{SG} with increasing V_{BG}, while keeping the V_d = 50 mV constant for a 7 × 10 SiNWs structure. Similarly, the I_d-V_{BG} characteristics are shown in Fig. 15 for increasing side-gate potentials.

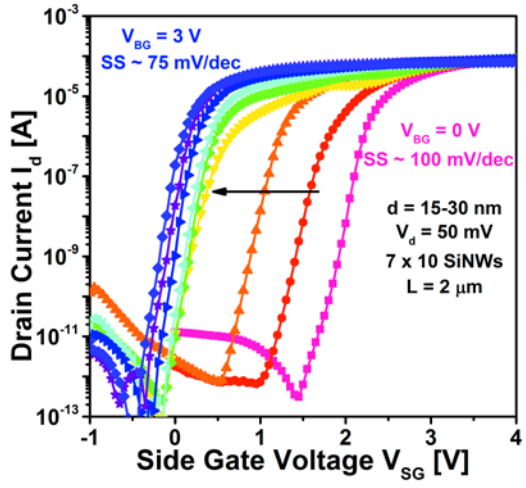

Figure 14. I_d-V_{SG} curves (left axis) for different backgate potentials (V_{BG} from 0 V to 3 V) for a 7 × 10 SiNWs structure, L = 2 µm, d_{NW} = 15-30 nm, V_d =50 mV, tested in a liquid environment.

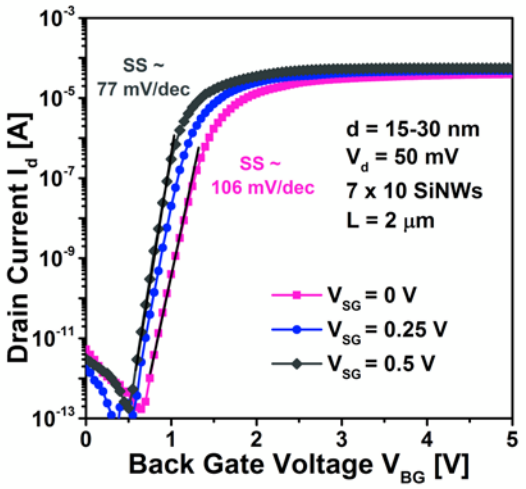

Figure 15. I_d-V_{BG} curves for different side-gate potentials (V_{SG} from 0 V to 0.5 V) for a 7 × 10 SiNWs structure, L = 2 μm, d_{NW} = 15-25 nm, tested in a liquid environment.

Fig. 14 shows that as the V_{BG} potential increases from 0 to 3 V, the V_{th} shifts significantly towards the left (from ~2.24 V to ~0.13 V for 7 × 10 SiNWs). The V_{th} changes (Fig. S2 supplementary information) the most when the tuning gate voltage is low (V_{BG} < 1.5 V) and then remains almost unchanged for higher V_{BG}. As the V_{BG} increases, the I_d-V_{SG} slope becomes steeper with the SS decreasing (i.e., from ~100 mV/dec to the excellent value of ~ 75 mV/dec at V_{BG} = 1.75 V, for a 7 × 10 SiNW structure, L = 2 μm), Fig. 16.

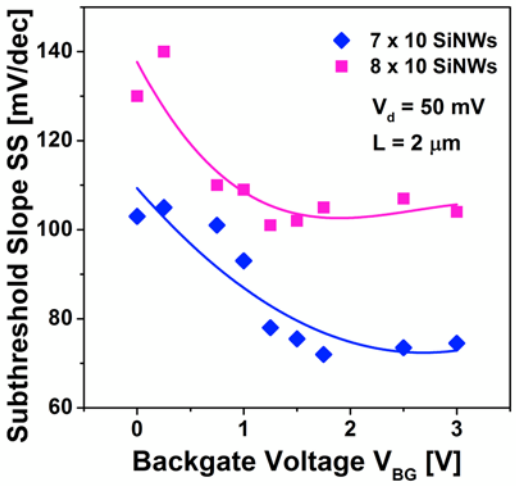

Figure 16. Subthreshold slope from I_d-V_{SG} curves as a function of backgate potential for both 7 × 10 and 8 × 10 SiNWs structure, L = 2 μm, V_d =50 mV, tested in a liquid environment.

When a side-gate is used as a tuning gate and the backgate as the primary gate, a threshold voltage shift and subthreshold slope improvement are also observed in the I_d-V_{BG} curves (Fig. 15). The V_{th} shifts to the left from 1.6 V to 1.1 V and the SS decreases from SS ~ 106 mV/dec to ~77 mV/dec (7 × 10 SiNW structure, L = 2 μm) as the V_{SG} increases from 0 to 0.5 V. Fig. 17 shows the drain current as one (single gate) or two side-gates (double gate, DG) are swept (7 × 10 SiNW structure, L = 2 μm, V_d = 50 mV) with the V_{th} being reduced by 300 mV but in comparison to the asymmetric front-back gating it does not change/improve the subthreshold slope significantly.

The coupling efficiency, typically defined by parameter α' as the ratio between the ideal SS at room temperature (60 mV/dec) and the measured SS ($\alpha' = SS_{ideal}/SS_{measured}$), for the same tuning gate potential (0.5 V), can be compared when either the backgate or the side-gates are used as the primary gates. The backgate coupling when V_{SG} = 0.5 V is α' = 0.8 in comparison to the side-gate coupling α' = 0.6 for the same tuning gate potential (V_{BG} = 0.5). This, together with the lower threshold voltages values found when the backgate is used as the primary gate indicates a more

efficient backgate coupling. The SU8 sensing window is designed to be small to reduce side-gate coupling through the liquid to the source and drain anchors. Nevertheless, part of the source and drain anchors are exposed to the solution as well. Both, the backgate and side-gates can accumulate or deplete the source and drain too. In particular, the backgate can not only influence the S/D indirectly through the liquid but directly as the structure sits on top of the BOX layer. Therefore, two competing effects happen as we apply a positive potential through any of the gates. First, an inversion channel that extends to the whole NW cross section can be easily formed. Second, as this potential is also felt at the source and drain, electrons can also be pulled away from the NW channels and towards the BOX oxide or S/D anchor surfaces as the potential increases. In traditional SOI based SiNW systems, the backgate capacitance C_{BG} is dominated by the BOX layer and the solution gate capacitance C_{LG} depends on the double layer capacitance of the solution C_{dl} as well as the native oxide capacitance [18]. Since the backgate in our system can also influence the SiNW gate channels through the solution, the double layer capacitance, native oxide capacitance and BOX layer capacitance all contribute to backgate capacitance and hence the higher backgate coupling efficiency.

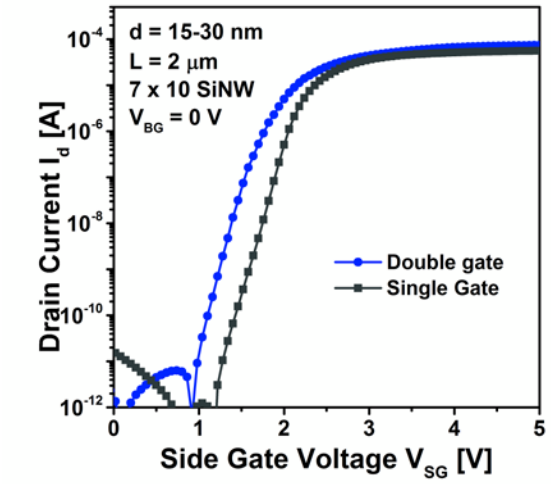

Figure 17. I_d as either one or both side-gates (DG) are swept for a 7 × 10 SiNWs structure, L = 2 μm tested in a liquid environment.

When ideal bias conditions are utilized, it is possible to gate the stack of NWs more efficiently from different sides in order to achieve excellent transistor characteristics for high sensitivities and a low power operation. The surface potential induced by a backgate can result in an amplified threshold voltage shift and a large sensing signal (current change) by the use of a dual gate configuration [17]. The driving voltage (side-gate) determines the FET characteristics and the signal produced by the sensing event (e.g., pH) is amplified through the use of the backgate or vise-versa [15, 17, 27]. Therefore the devices presented here show great potential for biosensing applications.

The electrical characteristics of devices with increasing number of NW channels and increasing length L dimensions are also compared. The devices with the highest number of nanowires 7 × 20 and 8 × 20 (Fig. 18 and S3, supplementary information respectively) and the shortest lengths (Fig. S4, supplementary information) have the highest on state currents.

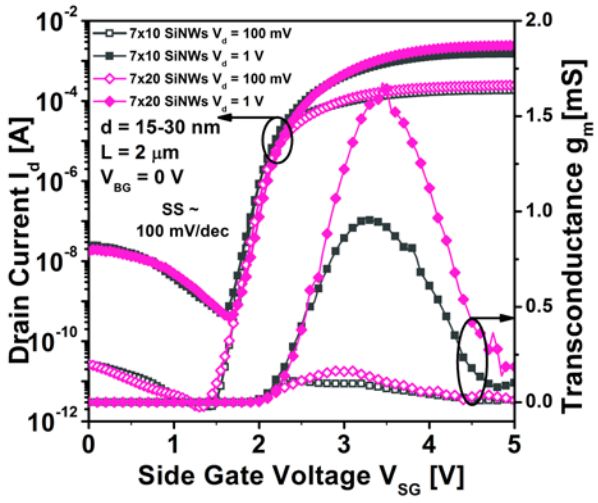

Figure 18. I_d-V_{SG} curves at high and low drain potentials for 7 × 10 and 7 × 20 SiNWs structures with L = 2 µm, d_{NW} = 15-30 nm, tested in a liquid environment (left). Transconductances for the same devices are shown on the right axis.

The maximum transconductance $g_{m,max}$ values were extracted from the measured I_d *vs.* V_{SG} curves. The transconductance $g_m = (dI_d/dV_{SG})$ is a measure of the sensitivity to surface charges. A high transconductance value means a bigger change in drain current for a given change in surface charge which can translate to higher device sensitivities when measuring the sensitivity in the strong inversion regime. High maximum transconductance values > 10 µS were found for all devices, Fig. 18 (right axis).

The SiNW-dielectric interface is important for the electrical stability of the device. An inner oxide (native oxide) would provide a stable contact with the electrical domain whereas the outer dielectric provides a stable contact with the liquid. SiO_2 is not the best pH selective material, and does not provide stable contact between the liquid and the sensor [11] since protons can penetrate the Si-oxide layers leading possibly to large leakage currents [3]. For that reason, HfO_2 (10 nm) was deposited as a gate dielectric.

From Equation 7 one can see that the SS is affected by the insulator dielectric constant ε_r and the thickness t_{ox} [28]. For fully depleted devices the depletion width W_{dm} extends through the bulk of the semiconductor channel and the capacitance ratio $C_{dm}/C_{ox} \sim (\varepsilon_{si} t_{ox}/\varepsilon_r W_{dm})$ should be relatively small making the SS small. ALD layers of high κ dielectrics are typically necessary to prevent charge penetration through the native oxide to the SiNWs and to reduce leakage currents through the liquid from (ε_r = 15.6 for HfO_2 *vs.* ε_r = 3.9 for SiO_2). The equivalent oxide thickness $EOT = t_{HfO_2}\left(\frac{\varepsilon_{SiO_2}}{\varepsilon_{HfO_2-\kappa}}\right)$ was calculated to be 2.5 nm for the HfO_2 dielectric layer. Though a higher gate capacitance should be expected for the (lower?) EOT, it is clear from Fig. 19 (7 × 20 SiNWs,

L = 2µm, 10 nm HfO_2 gate dielectric) that the deposition of the HfO_2 in fact degraded the transistor characteristics of our devices. The SS increased from ~100 mV/dec to ~ 150 mV/dec for HfO_2 is possibly due to the unstable process conditions of the ALD deposition. The V_{th} also increases to > 3 V.

$$SS = \frac{kT}{q}\left(\frac{d(log_{10}I_d)}{dV_G}\right)^{-1} = 2.3\frac{kT}{q}\left(1+\frac{C_{dm}}{C_{ox}}\right) \qquad \text{Equation (7)}$$

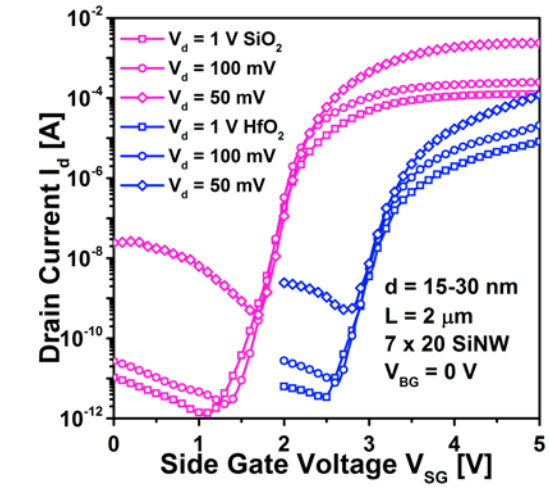

Figure 19. I_d-V_{SG} curves at high and low drain potentials for 7 × 10 SiNWs (V_d = 50, 100 mV, 1 V) with and without HfO_2, L = 2 µm, d = 15-30 nm, tested in a liquid environment.

Finally, Fig. 20 shows the I_d-V_{SG} transfer characteristics (V_d = 50 mV and 1 V) for a 7 × 10 SiNW structure with L = 2 µm, d = 15-30 nm and native oxide as a gate dielectric measured in a buffered saline solution (PBS) with pH ~ 7.4 (ε ~ 80). The SS decreases to the excellent value of 87 mV/dec and the V_{th} shifts to 1.93 V (vs. 2.24 for device gated in IPA), as expected since the PBS has a higher dielectric constant.

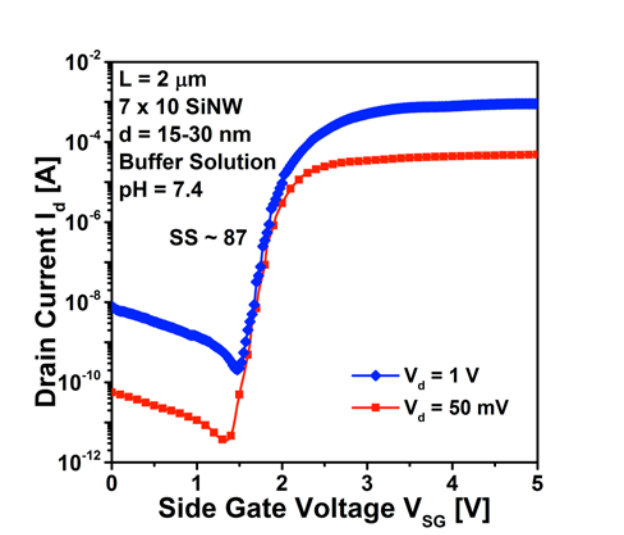

Figure 20. I_d-V_{SG} curves at high and low drain potentials for 7 × 10 SiNWs (V_d = 50 mV, 1 V), L = 2 µm, d_{NW} = 15-30 nm, tested in PBS (pH ~ 7.4).

Conclusion

3D vertically stacked silicon nanowire (SiNW) field effect transistors (FET) featuring a high density array (7 or 8 × 20 SiNW) of fully depleted channels, varying number of NWs in the horizontal direction (10, 15 and 20 NWs) and different channel lengths (2, 3, 4 µm) have been successfully fabricated by a CMOS compatible process on silicon on insulator (SOI). The structures were characterized electrically in a liquid for their implementation into a robust biosensing system for the first time. The channels can be surrounded by conformal high-κ gate dielectrics (HfO_2), and their conductivity can be uniquely tuned by three gates: a backgate (BG) and two symmetrical Pt side-gates (SG) through a liquid, offering unique sensitivity tuning with high gate coupling. They feature ultra-small SiNW diameters (down to d_{NW} ~ 15-30 nm) for full depletion and high S/V ratios for maximum sensitivities. The configuration of the 3D sensor offers excellent electrostatic control of the SiNW channels by the possibility of applying symmetric or asymmetric gate potentials while allowing for the optimization of the sensitivity and power

consumption trade-off. The lightly doped SOI substrate reduces $I_{off} < 10^{-11}$ A for all the devices for excellent I_{on}/I_{off} ratios > 10^6 at low V_d < 500 mV (pertinent to sensing experiments), low DIBL (< 20 mV/V) and high transconductance (gm > 10 μS) of particular importance for low power biomolecule sensing applications have been demonstrated. The operating point of the device can be optimized by working in the subthreshold region (steepest subthreshold swing). As V_{BG} increases, the I_d-V_{SG} slope becomes steeper with SS decreasing from ~100 mV/dec (V_{BG} =0 V) to the excellent value of ~ 75 mV/dec V_{BG} < 1.5 V. The threshold voltage is shifting as well towards lower values due to an improved electrostatic control by the two gates.

Methods

Fabrication of Vertically Stacked SiNW Devices:

ZEP-520A (Nippon-Zeon), a positive high resolution e-beam resist is first used to pattern silicon spacer (S = 200 nm) and trench (T = 300 nm and 200 nm) openings in a low thermal oxide (LTO) hard mask (100 nm). Scallops that serve as the basis of the SiNW structures are formed by a BOSCH process in an Alcatel AMS 200 inductively coupled plasma (ICP) etching system. The NWs are then formed by thermal oxidation in a dry oxygen atmosphere. A thick layer of LTO (> 1 μm) is deposited as hard mask for ion implantation. More details on the fabrication of the vertically stacked stand-alone structures can be found in a previous article [20]. S/D areas for ion implantation are defined by e-beam lithography and a SiO_2 anisotropic dry etch process. In the next masking levels the side-gates (Ti/Pt) and source/drain contact areas (Ti/Al/Pt) are defined for lift-off metallization by e-beam and optical lithography respectively. A thermal anneal process (30 min at 425 ^oC in forming gas 10% H_2/90 % N_2) was performed to produce ohmic contacts. Isolation of the sensor structure is achieved by the optical lithography patterning of SU8. A last e-beam lithography step is necessary to define a window to selectively remove the SiO_2 around the SiNWs

with a buffered HF acid bath (7:1, water: BHF) and avoid over etching of neighboring areas. The whole structure can be covered with a dielectric (HfO_2) by atomic layer deposition (ALD).

Electrical Characterization:

The electrical characterization is carried out at room temperature using a Microtech Cascade probe station and an HP 4155B semiconductor parameter analyzer. A droplet of isopropanol (IPA) is placed on top of the device of interest in order to allow liquid gating with the suspended NWs and then covered with a glass slide to prevent fast evaporation of the liquid during the measurements.

Vitae:

Elizabeth Buitrago received her B.Sc. degree in chemical engineering from the University of California San Diego (UCSD), in La Jolla, California and her M.Sc. degree in process engineering from the Eidgenössische Technische Hochschule Zürich (ETHZ) with an emphasis in particle technology. Currently, she is a Ph.D. Student-Researcher at the Ecole Polytechnique Fédérale de Lausanne (EPFL), in Switzerland, developing vertically stacked silicon nanostructure devices for biosensing applications. Through her internship and work experiences as a Process Engineer at AMI Semiconductor and Micron Technology in the United States, she became highly interested in the semiconductor industry.

Montserrat Fernández-Bolaños Badía received her M.Sc. degree in telecommunication engineering from the University of Seville, Seville, Spain, in 2005, and her Ph.D. degree in microsystems and microelectronics from the Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland, in 2010. Since receiving the Ph.D. degree, she worked as a Scientific Collaborator in the Nanoelectronic Device Laboratory at EPFL and since June 2013 she joined IBM Research Zurich as a senior researcher. The focus of her research is in the field of NEM relays for ultra-low

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Yordan Georgiev holds a Ph.D. in physics since 1997. He worked in some of the best research institutions in Russia, Bulgaria, Germany, and now Ireland and has a rich experience in fabrication of nanostructures and devices down to the 10 nm region for semiconductor electronics, optoelectronics, nanoimprint lithography, bionanotechnology, etc. His current research interes~~s~~ts include design, fabrication, and characterization of novel Si and Ge nanowire devices for digital electronics, ~~and~~ sensing, and quantum computing applications.

Adrian Nightingale received his undergraduate degree in Chemistry from the University of Oxford in 2003. After working for ICI Paints and then Johnson Matthey, he came to Imperial College London- first studying for an MRes in nanomaterials and then a PhD in microfluidic reactor technology. He is currently employed as a postdoctoral researcher in Imperial's Department of Chemistry looking at the application of microfluidics to different analytical and synthetic chemical problems.

Adrian Mihai Ionescu received his Ph.D. degree from the National Polytechnic Institute of Grenoble in France. He is a full Professor at the Swiss Federal Institute of Technology, Lausanne (EPFL) in Switzerland. He has held staff and/or visiting positions at LETI-CEA, Grenoble, LPCS-ENSERG, and Stanford University during 1998 and 1999. His research interests focus on micro- and Nanoelectronic devices aimed at integrated circuit design, particularly process development, modeling, and electrical characterization. He has published more than 250 articles in international journals and conference proceedings. He is the Director of the Laboratory of Micro/Nanoelectronic Devices (Nanolab) at EFPL. **Supporting Information**

More figures and supplemental findings can be found online. This material is available free of charge *via* the Internet at http://www.sciencedirect.com.

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

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REFERENCES

[1] Y. Cui, Q. Wei, H. Park, C.M. Lieber, Nanowire Nanosensors for Highly Sensitive and Selective Detection of Biological and Chemical Species, Science, 293(2001) 1289.
[2] M. Curreli, Z. Rui, F.N. Ishikawa, C. Hsiao-Kang, R.J. Cote, Z. Chongwu, et al., Real-Time, Label-Free Detection of Biological Entities Using Nanowire-Based FETs, Ieee Transactions on Nanotechnology, 7(2008) 651.
[3] O. Knopfmacher, A. Tarasov, W.Y. Fu, M. Wipf, B. Niesen, M. Calame, et al., Nernst Limit in Dual-Gated Si-Nanowire FET Sensors, Nano Letters, 10(2010) 2268.

[4] E. Stern, J.F. Klemic, D.A. Routenberg, P.N. Wyrembak, D.B. Turner-Evans, A.D. Hamilton, et al., Label-free Immunodetection with CMOS-Compatible Semiconducting Nanowires, Nature, 445(2007) 519.
[5] P. Bergveld, Development of an Ion-Sensitive Solid-State Device for Neurophysiological Measurements, IEEE Transactions on Biomedical Engineering, BME-17(1970) 70.
[6] P. Bergveld, The Development and Application of FET-Based Biosensors, Biosensors, 2(1986) 15.
[7] E. Buitrago, M.F.-B. Badia, Y.M. Georgiev, R. Yu, O. Lotty, J.D. Holmes, et al., Functionalized 3D 7x20 array of Vertically Stacked SiNW FET for Streptavidin Sensing, Device Research Conference DRC, Notre-Dame, IN (2013), p.
[8] P. Bergveld, The operation of an ISFET as an electronic device, Sensors and Actuators, 1(1981) 17.
[9] D.E. Yates, S. Levine, T.W. Healy, Site-binding Model of the Electrical Double Layer at the Oxide/Water Interface, Journal of the Chemical Society, Faraday Transactions 1: Physical Chemistry in Condensed Phases, 70(1974) 1807.
[10] L. Bousse, N.F. De Rooij, P. Bergveld, Operation of Chemically Sensitive Field-Effect Sensors as a Function of the Insulator-Electrolyte Interface, IEEE Transactions on Electron Devices, 30(1983) 1263.
[11] P. Bergveld, Thirty Years of ISFETOLOGY - What happened in the Past 30 Years and What May Happen in the Next 30 Years, Sensors and Actuators B, 88(2003) 1.
[12] R.E.G. Vanhal, J.C.T. Eijkel, P. Bergveld, Novel Description of ISFET Sensitivity with the Buffer Capacity and Double-Layer Capacitance as Key Parameters, Sensors and Actuators B, 24(1995) 201.
[13] S.K. Yoo, S. Yang, J. Lee, Hydrogen Ion Sensing Using Schottky Contacted Silicon Nanowire FETs, Ieee Transactions on Nanotechnology, 7(2008) 745.
[14] O.G. Elibol, J.R. Reddy, R. Bashir, Nanoscale Thickness Double-gated Field Effect Silicon Sensors for Sensitive pH Detection in Fluid, Applied Physics Letters, 92(2008) 193904.
[15] H. Jang, W. Cho, Fabrication of High-Performance Fully Depleted Silicon-on-Insulator Based Dual-Gate Ion-Sensitive Field-Effect Transistor Beyond the Nernstian Limit, Applied Physics Letters, 100(2012) 073701.
[16] J. Go, P.R. Nair, B. Reddy, B. Dorvel, R. Bashir, M.A. Alam, Coupled Heterogeneous Nanowire–Nanoplate Planar Transistor Sensors for Giant (>10 V/pH) Nernst Response, ACS Nano, 6(2012) 5972.
[17] J. Ahn, J. Kim, M. Seol, D. Baek, Z. Guo, C. Kim, et al., A pH Sensor with a Double-Gate Silicon Nanowire Field Effect Transistor, Applied Physics Letters, 102(2013) 083701.
[18] O. Knopfmacher, D. Keller, M. Calame, C. Schönenberger, Dual Gated Silicon Nanowire Field Effect Transistors, Procedia Chemistry, 1(2009) 678.
[19] E. Buitrago, M. Fernández-Bolaños, S. Rigante, C.F. Zilch, N.S. Schröter, A.M. Nightingale, et al., The Top-down Fabrication of a 3D-integrated, Fully CMOS-compatible FET Biosensor Based on Vertically Stacked SiNWs and FinFETs, Sensors and Actuators B, (2013).
[20] E. Buitrago, M. Fernández-Bolaños, A.M. Ionescu, Vertically Stacked Si Nanostructures for Biosensing Applications, Microelectronic Engineering, 97(2012) 345.
[21] N. Singh, K.D. Buddharaju, S.K. Manhas, A. Agarwal, S.C. Rustagi, G.Q. Lo, et al., Si, SiGe Nanowire Devices by Top-Down Technology and their Applications, IEEE Transactions on Electron Devices, 55(2008) 3107.

[22] L.K. Bera, H.S. Nguyen, N. Singh, T.Y. Liow, D.X. Huang, K.M. Hoe, et al., Three dimensionally stacked SiGe nanowire array and gate-all-around p-MOSFETs, Electron Devices Meeting IEDM, San Francisco (2006), p. 1.
[23] S.J. Choi, D. Moon, S. Kim, J.P. Duarte, Y.K. Choi, Sensitivity of Threshold Voltage to Nanowire Width Variation in Junctionless Transistors, IEEE Electron Device Letters, 32(2011) 125.
[24] H.G. Ong, J.W. Cheah, X. Zou, B. Li, X.H. Cao, H. Tantang, et al., Origin of Hysteresis in the Transfer Characteristic of Carbon Nanotube Field Effect Transistor, Journal of Physics D: Applied Physics, 44(2011) 285301.
[25] I.Y. Park, Z.Y. Li, A.P. Pisano, R.S. Williams, Top-down Fabricated Silicon Nanowire Sensors for Real-time Chemical Detection, Nanotechnology, 21(2010) 015501.
[26] S. Kim, T. Rim, K. Kim, U. Lee, E. Baek, H. Lee, et al., Silicon Nanowire Ion Sensitive Field Effect Transistor with Integrated Ag/AgCl Electrode: pH Sensing and Noise Characteristics, Analyst, 136(2011) 5012.
[27] G. Shalev, A. Doron, U. Virobnik, A. Cohen, Y. Sanhedrai, I. Levy, Gain Optimization in Ion Sensitive Field-Effect Transistor Based Sensor with Fully Depleted Silicon on Insulator, Applied Physics Letters, 93(2008) 083902.
[28] Y. Taur, T.H. Ning, Fundamentals of Modern VLSI Devices: Cambridge University Press; 2009.