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Publication date	2014-06
Original Citation	LONG, B., VERNI, G. A., O'CONNELL, J., HOLMES, J. D., SHAYESTEH, M., O'CONNELL, D. & DUFFY, R. (2014) Molecular Layer Doping: Non-destructive doping of silicon and germanium. 2014 20th International Conference on Ion Implantation Technology (IIT). Portland, Oregon, 26 June - 4 July. IEEE, pp. 1-4 http://dx.doi.org/10.1109/IIT.2014.6939995
Type of publication	Conference item
Link to publisher's version	http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=6927586 - 10.1109/IIT.2014.6939995
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Molecular Layer Doping: Non-destructive Doping of Silicon and Germanium

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Abstract — **This work describes a non-destructive method to introduce impurity atoms into silicon (Si) and germanium (Ge) using Molecular Layer Doping (MLD). Molecules containing dopant atoms (arsenic) were designed, synthesized and chemically bound in self-limiting monolayers to the semiconductor surface. Subsequent annealing enabled diffusion of the dopant atom into the substrate. Material characterization included assessment of surface analysis (AFM) and impurity and carrier concentrations (ECV). Record carrier concentration levels of arsenic (As) in Si ($\sim 5 \times 10^{20}$ atoms/cm^3) by diffusion doping have been achieved, and to the best of our knowledge this work is the first demonstration of doping Ge by MLD. Furthermore due to the ever increasing surface to bulk ratio of future devices (FinFets, MugFETs, nanowire-FETS) surface packing spacing requirements of MLD dopant molecules is becoming more relaxed. It is estimated that a molecular spacing of 2 nm and 3 nm is required to achieve doping concentration of 10^{20} atoms/cm^3 in a 5 nm wide fin and 5 nm diameter nanowire respectively. From a molecular perspective this is readily achievable.**

Keywords— Silicon, Germanium, Molecular Layer Doping, Chemistry, Doping, Surface Functionalisation.

I. INTRODUCTION

This work focuses on developing a foundationally new technique for doping semiconductor materials. Current state-of-the-art doping technologies, ion implantation, and plasma doping, have unresolved issues that hinder performance in thin-body semiconductor devices. These issues include the crystal damage introduced by ion implantation [1], lack of conformality and dramatic dopant trapping at the oxide interface in plasma doped processes [2, 3].

To date the semiconductor industry has achieved improved performance through transistor scaling with the economic benefit of reusing existing infrastructure. As scaling continues transistor architecture has had to evolve, as traditional architectures, with planar bulk substrates and highly doped channels for short-channel-effect (SCE) control, are problematic due to excessive leakage currents. To overcome this, thin-body architectures (e.g. multigate FETs such as FinFETS) are being considered. However as the device body
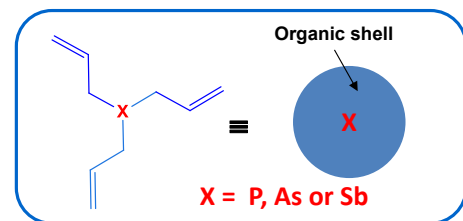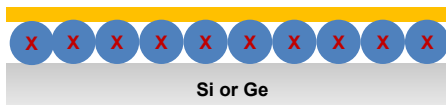

Scheme 1: Structure of doping molecule (top) and process steps 1-5 for Molecular Layer Doping of Si or Ge

thins, the ratio of surface: bulk atoms increases dramatically.

Moving toward all-surface structures makes control of the surface chemistry critical to transistor performance. Doping thin-body features can be quite a substantial challenge, as it is difficult to get the impurity atoms uniformly into the structure,

activate them, and prevent them from escaping during thermal treatments, while maintaining good crystalline integrity of the semiconductor crystal.

A potential solution to this problem is MLD, pioneered by the Javey group [4] in 2008 for doping Si. This is a method based on surface functionalisation using molecules that contain dopant atoms. Thermal decomposition of this molecular layer will enable freed-up dopant atoms to diffuse into the underlying semiconductor. Furthermore, minimal damage to the crystal structure of the underlying substrate will occur due to the gentle nature of the process while opening a path to *Deterministic Doping* techniques which have been recognized as an emerging candidate for regulated dopant delivery, ordered on the nanometre scale.

Silicon has been the cornerstone of the semiconductor industry for 5 decades, however, with an estimated 6 billion mobile device subscriptions worldwide there is a massive demand on power supplies.[5] As a reduction in the global demand for energy is a grand-challenge of the 21st Century, moving from Si to a high carrier mobility material which can enable reduced power consumption (by delivering a fixed drive current and circuit speed at a reduced power supply voltage) is a priority. Several high mobility materials are being considered as potential candidates including graphene, TMDs (define) and III-Vs. Germanium, however, has received a lot of research and industrial interest as it is CMOS (complementary metal oxide semiconductor) compatible and can be processed side-by-side with Si on existing technology platforms. Ge, a high mobility material with a narrow band gap, can produce increased electron and hole mobility over Si, i.e. theoretically Ge has a mobility enhancement at least 2× for electrons and nearly 4× for holes.

Though several papers have been published showing MLD on Si and several III-V materials there has be no report to date of MLD on Ge [6].

This paper presents results showing record levels of diffusion doping Si and the first demonstration of doping germanium, by MLD. This study focuses on arsenic for a variety of reasons 1) Its relatively high equilibrium solubility 2) Its ability to in-diffuse and 3) based on results from an alternative in-diffusion techniques it is significantly better than other n-type dopants. Given that this MLD is designed for doping small dimension devices, packing density requirements for doping nanostructures are also considered..

II. EXPERIMENTAL

All chemicals were purchased from Sigma-Aldrich. Germanium wafers, p-type, were purchased from the Umicore Group. Triallyarsine (TAA) was synthesized using a published procedure [7]. The procedure for MLD is outlined in Scheme 1. Si or Ge wafers, cut to 1x1 cm^2 pieces, were cleaned by sonicating in acetone for 180 s, rinsed in IPA and dried under a stream of nitrogen before immersing them in HF (10 %) for 10 minutes. They were removed from HF and dried under a stream of nitrogen before transferring them to a quartz flask. For Si, a solution of degassed TAA in mesitylene (1:5) was added to the flask with the substrate and heated to 160 °C for 3 h. For Ge, a solution of degassed TAA in IPA (1:5) was added to the flask with the substrate and irradiated using 254 nm UV light for 3 h. The samples were then rinsed several times in a series of solvents to remove any unbound molecules (Step 1 and 2, Scheme1). They were stored under nitrogen until a 50 nm layer of sputtered SiO_2 (step 3, Scheme 1) was deposited on top. The Si was then annealed at 1000 °C for 5 s and the Ge was annealed at 650 °C for 1, 10 or 100 s (Step 4, Scheme 1). The SiO_2 layer was removed by immersing in BOE for 60 s (Step 5 Scheme 1).

III. RESULTS AND DISCUSSION

The procedure used for doping Si and Ge using molecules is outlined in Scheme 1. The cleaning step is critical to remove as much carbon contamination and native oxide as possible to free up germanium atoms so they can react with the target molecule. HF treatment of the substrate removes the native oxide while leaving the surface H-terminated which is reactive towards the dopant containing molecule. UV radiation of the molecule in the presence of the substrate leads to the formation of a C-Si or C-Ge bond. A "capping" layer is then applied (sputtered SiO_2 has given the best results) to prevent the evaporation of the molecules during the annealing step.
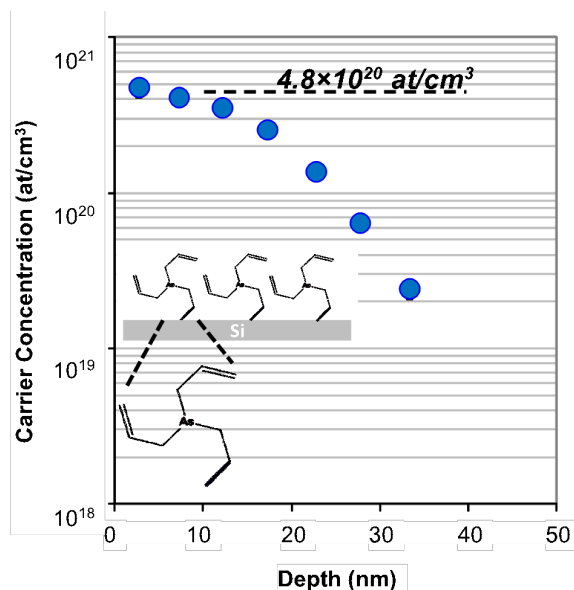

Fig. 1: Active carrier concentration vs depth extracted by Electrochemical Capacitance-Voltage (ECV) profiling of As-doped Si. The peak active carrier concentration is 4.8×10^{20} atoms/cm^3. The inset shows triallylarsine (TAA) bound to a Si surface. TAA provides a source of As that diffuses into Ge or Si upon annealing.

As Si was previously doped with P the annealing conditions could be replicated for doping with arsenic [4] however for Ge it was necessary to establish a thermal budget that would give the best results. Using the RTA available to us the maximum annealing temperature was 650 °C (0.7 x melting point of Ge (938 °C)). Using this temperature the

thermal budget was adjusted by changing the annealing times (1, 10 and 100 s).

Si and Ge doped by MLD were characterized by electrochemical capacitance voltage (ECV) measurements and by AFM. Fig 1 shows a peak active carrier concentration of 4.8×10^{20} atoms/cm^3 for Si. This is the highest reported active profile for diffusion doping reported to date. Fig 2 shows the ECV results for Ge annealed for 1, 10 and 100 s at 650 ^{o}C. All curves show a peak carrier concentration of 6×10^{18} atoms/cm^3. The fact that the peak carrier concentrations are the same for all thermal budgets suggests that we have reached the limit of solubility of As in Ge at 650 ^{o}C. There is no difference in the depth profile after annealing for 1 and 10 s. After 100 s the depth profile increases from ~150 nm to 350 nm indicating that the depth of the dopant diffusion cannot be controlled below 10 s. In short, in order to increase the carrier concentration of active dopants in Ge more advance annealing methods need to be explored.
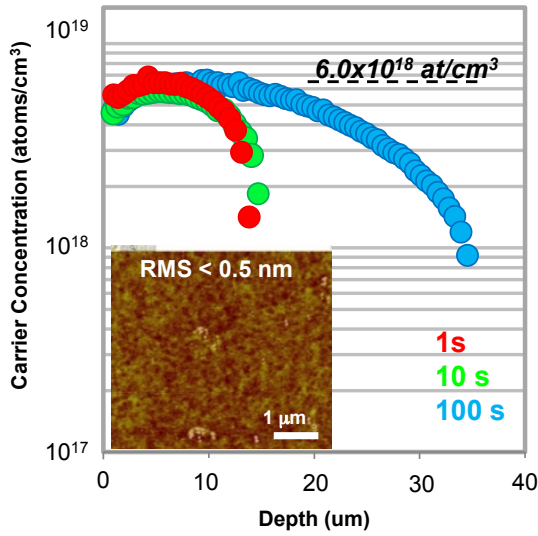

Fig 2: Active carrier concentration vs depth extracted by Electrochemical Capacitance-Voltage (ECV) profiling of As-doped Ge. The peak active carrier concentration is 6.0×10^{18} atoms/cm^3. The inset shows an AFM of the germanium substrate post MLD processing.

Fig 2 (inset) shows an AFM image of Ge after processing by MLD. It shows that the RMS roughness is less than 0.5 nm. Which is well within the acceptable limits (<1 nm) required for processes that will be transferred to nanostructured devices.

As MLD is designed for doping small dimension devices it is important to put in perspective the requirements for packing density to achieve adequate carrier concentrations for device performance. Assume that a highly doped semiconductor region, say as in the source and drain of a MOSFET, requires a doping concentration, C, of approximately 1×10^{20} atoms/cm^3. The surface coverage (or dose, D) can be calculated depending on the thickness of the semiconductor that has to be doped. For example a realistic future MOSFET device technology may require a semiconductor body thickness, t, in the range of 10 nm. Typical MOS technologies in the digital logic field may rely on multi-gate FET devices (MugFETs) such as the FinFET, or planar fully-depleted SOI (FDSOI) devices, in order to control short channel effects (SCE).
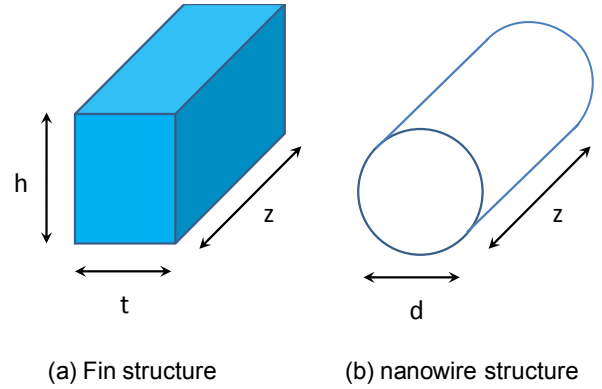

(a) Fin structure   (b) nanowire structure

Fig 3 : Schematics of a fin and a nanowire structure.

In the fin structure of Fig. 3 (a) with a single side surface doped

$$C = \frac{atoms}{volume} = \frac{atoms}{h.t.z}$$

$$D = \frac{atoms}{area} = \frac{atoms}{h.z}$$

$$D = C.t$$

where h is the height, t is the fin thickness (or width), and z is length.

$$D = \frac{atoms}{area} = \frac{atoms}{2.h.z}$$

$$D = \frac{C.t}{2}$$

In the nanowire structure of Fig. 3(b):

$$C = \frac{atoms}{volume} = \frac{atoms}{\pi r^2.z}$$

$$D = \frac{atoms}{area} = \frac{atoms}{2\pi r.z}$$

$$D = C.\frac{r}{2} = C.\frac{d}{4}$$

where d is the nanowire diameter (or width), and z is length. Subsequently molecular packing density (spacing between dopant atoms) on the surfaces can be calculated from the required dose values:

$$Packing\ Density = \frac{1}{\sqrt{D}}$$

Initially assuming a single surface as our source of dopant, then $D = C \times t = 1020$ atoms/cm3 $\times$ 10 nm = 1014 atoms/cm2 . In other words the dose coverage needs to be 1 atom/cm2, or 1 nm spacing between dopant atoms on the Ge sss steps for MLD on Si and Geedn before transferring them to a quartz flask.   has be no report to date of MLD on surface.
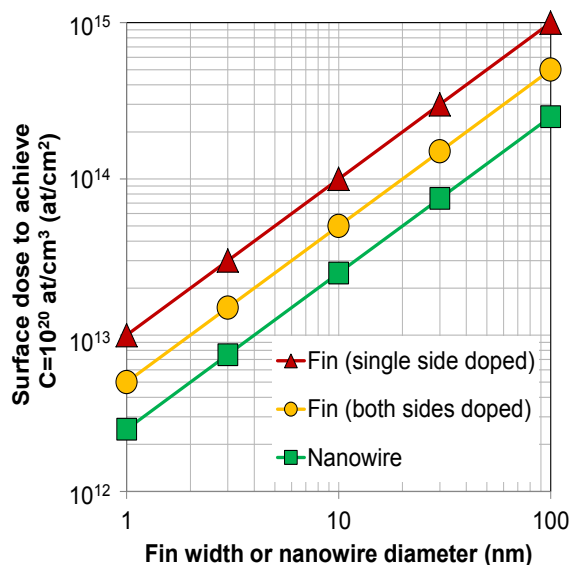

Fig. 4: Required surface dose to achieve $C = 10^{20}$ atoms/cm^3 for a single sided functionalised fin, a double sided functionalised fin, and for a cylindrical nanowire.

If there are multiple sources of dopants, such as in a FinFET, where two sides of the semiconductor can be doped simultaneously by the MLD process, and assuming the same values for C and t, the target value for D becomes 5×10^{13} atoms/cm^2, which is the equivalent of 1.41 nm spacing between dopant atoms on each of the surfaces.

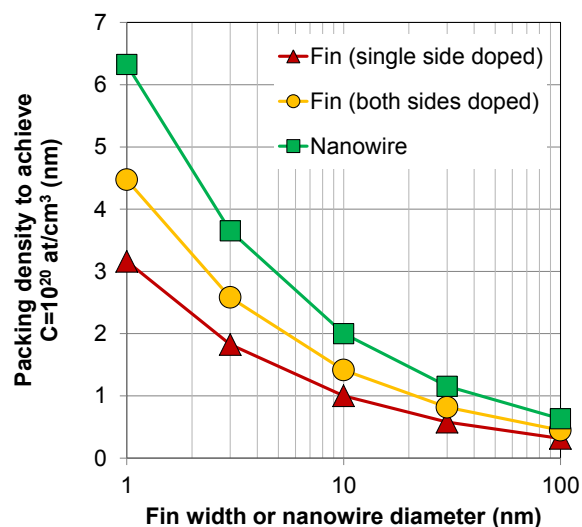Fig. 5: Required surface packing of dopant atoms, in terms of spacing, in order to achieve C=1020 atoms/cm3 for a single sided functionalised fin, a double sided functionalised fin, and for a cylindrical nanowire..

Finally, if a future technology requires a 3 nm thick semiconductor body, the single surface dopant source should have $D = C \times t = 10^{20}$ atoms/cm^3 $\times$ 3 nm = 3×10^{13} atoms/cm^2, and the double sided doped case (FinFET) should have a dose coverage of 1.5×10^{13} atoms/cm^2, which equates to 2.58 nm spacing between dopant atoms on each of the surfaces.

IV. CONCLUSIONS

Molecules containing dopant atoms were chemically bound to a semiconductor surface and have been used to dope Si and Ge using a process known as MLD. Record values for diffusion doping of Si, $\sim 5 \times 10^{20}$ atoms/cm^3, have been presented. Also, this is the first demonstration of MLD on Ge where peak carrier concentrations of 6×10^{18} atoms/cm^3 achieved. It was ascertained that more advanced annealing methods would be required for achieving higher doping levels in Ge by MLD, as the solid solubility limits of As in Ge had been reached at the maximum allowed thermal annealing temperature of 650 ^{o}C.   AFM measurements post MLD processing showed an average RMS of <0.5 nm for Ge, which is in the range of acceptable values for processing devices on the nano-scale. Finally, calculations to ascertain the feasibility of MLD as a processing technique were carried out to determine the packing density of molecule required to achieve carrier concentrations of 1×10^{20} atoms/cm^3, showing that a 2 nm and 3 nm spacing for fins and nanowires respectively, was adequate and compatible with molecular size.

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