Engineering Interfacial Silicon Dioxide for Improved MIS Silicon Photoanode Water Splitting Performance

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Keywords

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Abstract

Silicon photoanodes protected by atomic layer deposited (ALD) TiO_2 show promise as components of water splitting devices that may enable the large-scale production of solar fuels and chemicals. Minimizing the resistance of the oxide corrosion protection layer is essential for fabricating efficient devices with good fill factor. Recent literature reports have shown that the interfacial SiO_2 layer, interposed between the protective ALD-TiO_2 and the Si anode, acts as a tunnel oxide that limits hole conduction from the photo-absorbing substrate to the surface oxygen evolution catalyst. Here-in we report a significant reduction of bilayer resistance, achieved by forming stable, ultrathin (< 1.3 nm) SiO_2 layers, allowing fabrication of water splitting photoanodes with hole conductances near the maximum achievable with the given catalyst and Si substrate. Three methods for controlling the SiO_2 interlayer thickness on the Si(100) surface for ALD-TiO_2 protected anodes were employed: (1) TiO_2 deposition directly on an HF-etched Si(100) surface, (2) TiO_2 deposition after SiO_2 atomic layer deposition on an HF-etched Si(100) surface, and (3) oxygen scavenging, post-TiO_2 deposition to decompose the SiO_2 layer using a Ti overlayer. Each of these methods provides a progressively superior means of reliably thinning the interfacial SiO_2 layer, enabling the fabrication of efficient and stable water oxidation silicon anodes.

I. Introduction

Photoelectrochemical (PEC) water splitting cells have attracted research interest because of their potential to simultaneously harvest and store solar energy.[1-5] Silicon is a good candidate

light absorber in such devices due to its wide availability as a low cost, high purity crystalline material, and its band gap near the Schockley-Queisser ideal band gap, making it a nearly ideal bottom-cell for a tandem device combined with a larger, ~1.8 eV band gap top cell.[6] An unprotected Si photoanode will, however, oxidize under water splitting conditions, reducing Faradaic efficiency and forming an insulating SiO_2 layer that progressively shuts down the water oxidation reaction.[7] Previously reported research has shown that atomic layer deposited (ALD) TiO_2 can effectively protect Si photoanodes, yielding efficient, stable devices.[7-9]

Recently, we have investigated the tunnel barrier to hole transport presented by an interfacial layer (IL) of SiO_2 in TiO_2-protected Si photoanodes.[10] The SiO_2 tunnel oxide can easily dominate the device resistance due to its large bandgap and relative lack of bulk oxide traps, compared to the TiO_2 corrosion protection layer. Photovoltage design principles for two types of photoanodes, those employing nSi metal-insulator-semiconductor Schottky junctions and those employing p^+nSi buried junctions (detailed diagrams in supporting S1), have also recently been characterized. Thicker insulator layers were shown to not only increase series resistance but also to impose photovoltage penalties in MIS Schottky junction nSi cells.[11] The observed photovoltage decrease with increasing oxide thickness is a consequence of the voltage required for sufficient hole accumulation at the semiconductor/oxide interface to sustain hole conduction through the MIS junction.[11] The measured photovoltage penalty for increased thickness of the SiO_2 IL in a metal/TiO_2/SiO_2/nSi architecture was ~449 mV/nm ,[11] highlighting the importance of making the interfacial layer ultrathin (here defined as < 1.3 nm, the approximate average thickness of the surface oxide provided on vendor-supplied Si wafers). The lower dielectric constant of SiO_2 relative to TiO_2 means that any increase in SiO_2

thickness will also incur a much greater photovoltage penalty than the same increase in TiO_2 thickness.[11] This strong dependence of both photovoltage and series resistance on SiO_2 thickness makes reducing SiO_2 thickness one of the most effective methods for improving silicon MIS photoanode performance.

While reducing SiO_2 thickness has the potential to improve hole transport and photovoltage, eliminating this interfacial layer altogether is impractical and can lead to even worse device performance if the silicon/oxide interface quality is degraded as a result. High interface trap densities approaching ~1% of silicon surface sites (~10^{13} cm^{-2} states) may pin the Fermi level at an energy in the Si band gap, as determined by the interface state energy distribution, and severely reduce the built-in voltage of an MIS junction.[12] An oxide layer that produces a high interface state density can also increase Shockley-Read-Hall recombination, further lowering photovoltage. An ultrathin SiO_2 layer that forms a low interface defect density with Si can, however, reduce the density of interface traps (D_{it}) and minimize these effects. A thin SiO_2 layer on a silicon substrate also provides a surface that allows for the facile initiation of a thermal TiO_2 ALD process. Dendooven et al. have shown that, while ALD-TiO_2 does not exhibit a nucleation delay on -OH terminated SiO_2 layers, deposition on an –H terminated, HF-last bare Si surface shows a lower growth rate during the initial cycles.[13] When initiation of ALD is limited, the film forms in an islanded morphology, leading to high RMS roughness and incomplete film coverage for ultrathin films.[14-15]

In our prior research,[7-8] TiO_2 films were most often deposited on a 1.3-1.5 nm (thickness measured ellipsometrically) chemically-derived vendor chemical (vc) oxide layer, as provided by the silicon wafer vendor. Thicker SiO_2 films were formed using slot-plane antenna (SPA) plasma oxidation of the HF-last Si (100) surface, allowing the investigation of MIS silicon photoanodes with SiO_2 interlayer films of 1.5 nm to 11.5 nm thickness, with low D_{it} values and good thickness uniformity.[10-11] Recently, Hu et. al used a peroxide SiO_2 growth process on HF-last Si(100), which should form an oxide similar to the vc oxide used in our work.[9] In another report, it was demonstrated that functionalizing the Si(111) surface with methane (CH_3-) and propyl aldehyde ($HC(O)CH_2CH_2$-) groups prior to ALD deposition of Al_2O_3 and MnO can lead to reduced interfacial SiO_x thickness and higher photogenerated carrier lifespans.[16] However, methods of reliably producing ultrathin (< 1.3 nm) SiO_2 interlayers between an ALD-TiO_2 protective film and the Si(100) substrate, and their effects on anode Si anode performance, have yet to be reported.

In order to optimize performance of TiO_2 passivated Si photoanodes, we first investigate (1) the limitations of removal of the initial vc-oxide by HF etching and depositing the ALD-TiO_2 protective coating directly on the H-terminated Si(100) surface. We then explore two alternative methods for the controlled formation of ultrathin SiO_2 ILs: (2) Plasma enhanced ALD (PEALD) of SiO_2 onto HF-etched silicon, followed by deposition of the TiO_2 protection layer; and (3) post-TiO_2 ALD thinning of SiO_2 interlayers by using a titanium film to scavenge oxygen through the interposed TiO_2 layer.

In this report, we find that thermal ALD-TiO_2 deposition on an HF-last surface, PEALD SiO_2 interfacial layer deposition on such a surface, and oxygen scavenging after the formation of a TiO_2/SiO_2 oxide stack can all produce ALD-TiO_2 protected Si photoanodes with thinner SiO_2 ILs and reduced series resistance. Only ALD-SiO_2 interlayers and oxygen scavenging, however, also ensure facile ALD-TiO_2 initiation and achieve high (~500 mV) photovoltages, likely because they produce a relatively low interface trap density. In particular, the oxygen scavenging method is capable of achieving stable anode operation combined with near-maximal conductances from anodes with varying TiO_2 and initial SiO_2 thickness.

II. Results and Discussion

2.i TiO_2 Deposition on HF-Last Silicon Surface

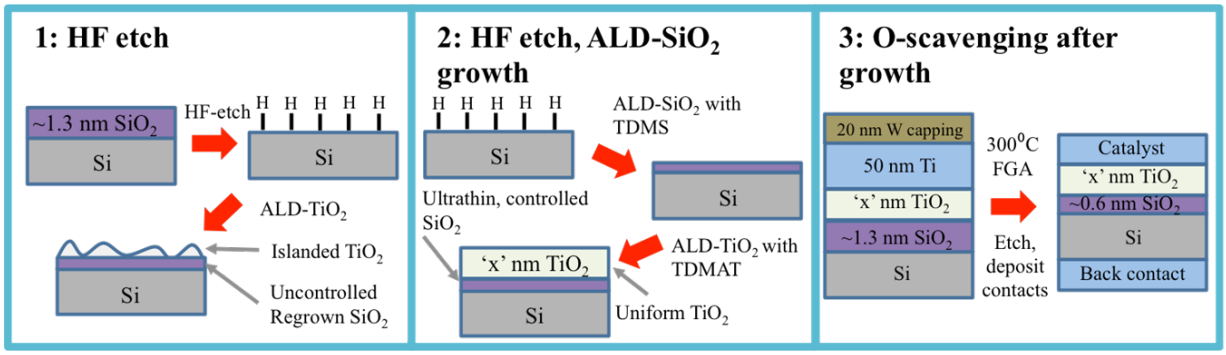

Figure 1. Fabrication Methods (1) Growth on an HF-last surface, resulting in regrowth of the SiO_2 IL and uneven, islanded TiO_2 growth. **(2)** SiO_2 ALD using the tris(dimethylamino)silane (TDMS) precursor on an HF-last surface resulting in an ultrathin, controlled SiO_2 IL after TiO_2 ALD using the TDMAT precursor **(3)** Titanium assisted oxygen-scavenging post-TiO_2 deposition allows thinning of the SiO_2 IL

To characterize the growth of ALD-TiO_2 on hydrogen terminated Si (100) surfaces, the vendor chemical oxide was removed with a 15s 50:1 H_2O:HF dip (Figure 1). Thermal TiO_2 ALD was performed using tetrakis(dimethylamido)titanium (TDMAT) precursor and water vapor oxidant immediately following the HF dip (see experimental section for more information on TiO_2 ALD). Two hundred cycles of ALD were performed, resulting in ellipsometrically derived film thicknesses ranging from 6.3 to 13.9 nm, indicating varying local ALD initiation kinetics across the wafer surface. This ± 38% thickness variability (Figure 2a) stands in stark contrast to results obtained in the qualification runs performed on vendor chemical (vc) oxide Si (100) wafers immediately prior to and after the deposition experiments on HF-last silicon, which showed a ± 4% variation in thickness (Figure 2a and Supporting S2), ruling out the possibility of non-ideal deposition conditions causing this variation. The extreme thickness variation observed for ALD on HF-last Si is indicative of initially inhibited deposition of TiO_2 over much of the silicon surface due to local variations in the density of precursor adsorption sites on a partially H-terminated Si (100) surface.[14-15]

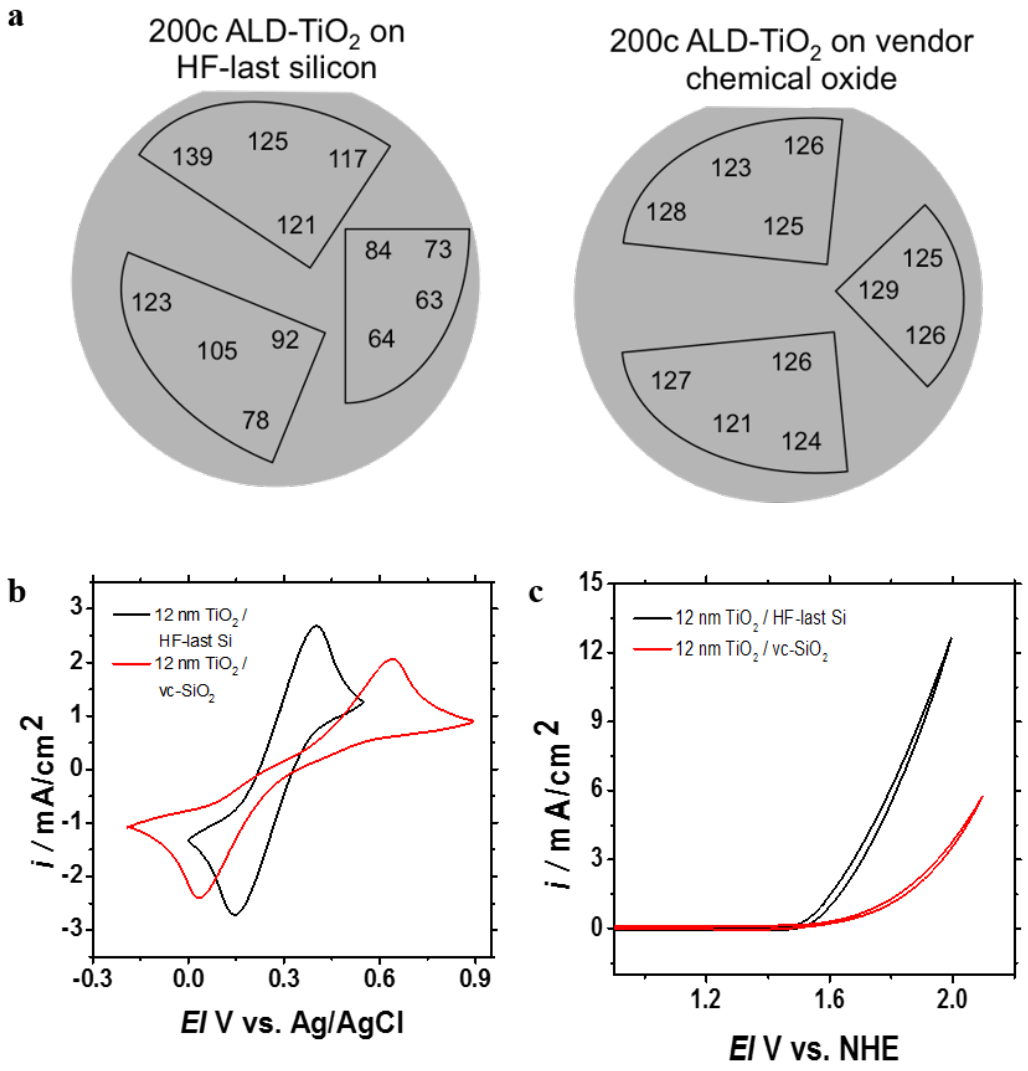

Figure 2 | Thickness variation and electrochemical performance of ALD TiO_2 photoanodes grown on HF-last surface (a) Thickness maps of 200 cycles of ALD TiO_2 grown on an HF-last surface, and a typical run on vendor chemical oxide for silicon pieces on a 4" silicon wafer. Thickness variations are ± 38% on the HF last surface and ± 3% on the vendor chemical oxide. (b) Ferri/ferrocyanide (FFC) cyclic voltammograms of p^+Si demonstrating a 180 mV reduction in half peak to peak splitting of an HF-last sample compared

to a vendor chemical oxide. (c) Water oxidation cyclic voltammograms showing a 198 mV decrease in overpotential as measured in pH 0 1M H_2SO_4 solution.

To characterize the interfacial layer between the Si surface and the TiO_2, X-ray photoelectron spectroscopy (XPS) analysis was performed using Al *K*-α radiation. Figure 3a shows the XPS Si 2p feature for the different silicon surface structures explored in this paper, providing a measure of interfacial SiO_2 thickness. Thicknesses were calculated using equation (1).[17] The take-off angle (θ) was 90º in this experiment and values of a mean escape depth of λ_{SiO2} = 27±2 Å, and a theoretical SiO_2:Si bulk intensity ratio (derived from the differences in densities) of K = 0.988 were used (typical values for Al *K*-α radiation).[17]

$$t_{ox} = \lambda_{SiO_2} \ln\left(\frac{I_{SiO_2}/I_{Si}}{K} + 1\right)\sin\theta \quad (1)$$

The chemically-shifted peak detected at 103.3 eV in the bottom four spectra in Fig. 3a occurs at a binding energy consistent with Si^{4+} bonding to O in an SiO_2 layer.[18] The second from the top spectrum (grey trace) demonstrates the regrowth of an SiO_2 interfacial layer of 6.6 Å average thickness when ALD-TiO_2 is deposited on an HF-last surface. Though this oxide is, on average, significantly thinner than the vendor chemical oxide (bottom XPS spectra showing 11.9 Å of SiO_2), its regrowth is uncontrolled, leading to uncertain electrical properties and variable SiO_2 thickness.

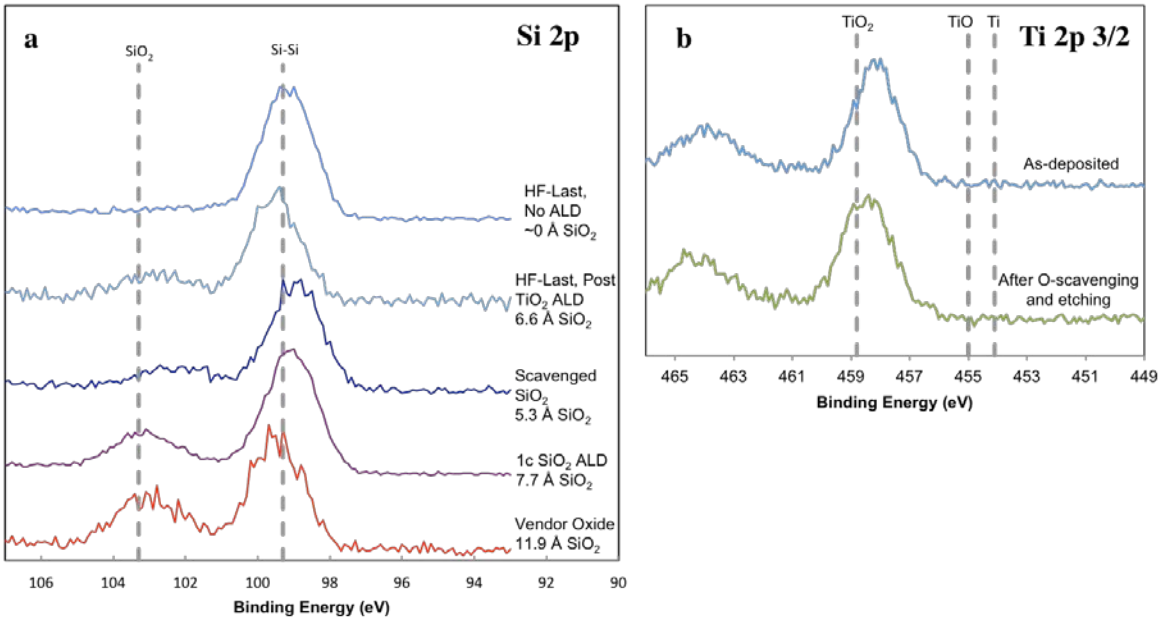

Figure 3. XPS Analysis of Si and Ti peaks of a TiO_2-protected silicon anode (a) Si 2p peak showing the different oxide thicknesses observed in different samples fabricated. HF-last, ALD-SiO_2 and O scavenging samples all show less intense peaks at 103.3 eV than vendor chemical oxide, demonstrating thinned oxide layers. **(b)** Ti 2p 3/2 peak of an as-deposited, non-O-scavenged sample (top) and an O-scavenged sample (bottom) showing no signal at 455 eV or 454.1 eV, the binding energies of Ti^{2+} and metallic Ti, respectively. The feature at 463.5 eV is the Ti 2p 1/2 peak. Energy calibration is performed using the C 1s peak as a reference.

MIS anodes were fabricated using HF-last Si substrates, including a 2 nm thick electron beam evaporated Ir surface oxygen evolution reaction (OER) catalyst layer and a 20 nm Pt back contact. An ALD-TiO_2 protection layer of ~12 nm thickness, as measured ellipsometrically, was deposited. Figures 2b & c show electrochemical cyclic voltammetry data from the HF-

last sample, compared to data from a 200 cycle Si anode coated with vendor chemical oxide. Both samples use a degenerately doped p^+Si substrate (details given in the experimental section). Voltammetry was performed in 10 mM ferri/ferrocyanide (FFC) 1M KCl solution and pH 0 1M H_2SO_4 as described in the experimental section. An FFC half peak-to-peak splitting decrease from 310 mV to 130 mV (Figure 2b) was observed, indicating that the ~5.3 Å reduction of SiO_2 thickness of the HF-last sample significantly reduced its resistance. Similarly, a 150 mV reduction in water splitting overpotential to reach a current density of 1 mA/cm^2 in pH 0 solution is observed for the HF-last versus the vendor chemical (vc) oxide sample (Figure 2c).

Samples were also fabricated with the same oxide and catalyst layers on an nSi substrate with an Al back contact. Photovoltage can be inferred from the difference in water oxidation over-potential (here defined as the voltage difference between the nSi photoanode and p^+Si reference anode when the current reaches 1 $mA \bullet cm^{-2}$). It can also be inferred from the shift of the center of FFC hysteretic cyclic voltammogram between otherwise identical samples on a p^+Si reference substrate tested in the dark and on an n-Si or a p^+nSi buried junction substrate tested under simulated solar illumination. The nSi photoanodes with ~10 nm average thickness of ALD-TiO_2 grown on HF-last silicon exhibit a -230 mV photovoltage (Supporting S3). These photoanodes had an average of ~2 nm thinner TiO_2 protection layer than the p^+Si reference, which was exposed to the same HF etch and was coated in the same TiO_2 run. The average thickness variation between samples from the same run is ascribed to nucleation delays incurred from deposition on an HF-last surface. Because reducing the ALD-TiO_2 thickness by 2 nm decreases the water oxidation overpotential by ~40 mV[8], the inferred photovoltage for

samples without these variations in TiO_2 thickness should be even less than the measured -230 mV. When photovoltage analysis is performed on samples with Ir/12 nm TiO_2/vc-SiO_2/nSi a -260 mV photovoltage is inferred (Supporting S3). Observation of negative photovoltage in nSi anodes with ALD-TiO_2 thicknesses > 10 nm has been reported previously.[11] It results from the voltage required to maintain a relatively high hole density at the silicon surface to sustain the photocurrent density at which turn-on of the anode is defined (in this study, 1 mA•cm^{-2}). Though the sample grown on an HF-last surface has a smaller SiO_2 thickness, which should improve photovoltage, it still has a negative inferred photovoltage. It is likely that a high density of interface traps contributes to the greater effective photovoltage reduction of the HF-last silicon samples. Regrowth of a defective and non-uniform SiO_2 interlayer between the ALD-TiO_2 and HF-etched nSi substrate will increase Shockley-Read-Hall recombination and decrease the photovoltage. These observations demonstrate that thinning the SiO_2 interlayer can dramatically improve conductivity; however, the large ALD-TiO_2 thickness variations and low photovoltage of these samples suggest that HF-etching of the initially oxidized Si (100) surface is, by itself, an impractical approach for reducing Si photoanode resistance and improving overall performance.

2.ii ALD-SiO_2 Interfacial Layer

Plasma enhanced atomic layer deposition (PEALD) of SiO_2 has been shown previously to produce highly conformal SiO_2 films with low D_{it} values.[19-20] PEALD SiO_2 films have also been demonstrated to have very low carbon content (< 0.5%) and no oxygen deficiency detectable by XPS.[21] They also exhibit high breakdown fields of ~10 MV/cm.[21] PEALD of

SiO_2 has been used previously to form an interfacial layer for Al_2O_3 passivated Si(100) photovoltaics, and it has been shown that engineering the SiO_2 IL thickness can tune the fixed negative charge density of such devices.[22]

Silicon dioxide interfacial layers of well-controlled thickness were formed by PEALD using tris(dimethylamino)silane precursor and oxygen plasma oxidant on an HF-last Si(100) surface (details in experimental section). The thicknesses of these layers were characterized using ellipsometry and XPS (Supporting S4). ALD-SiO_2 with this silicon precursor displays a typical growth rate of ~0.8 Å/cycle; however, XPS data are consistent with the formation of 7.7 Å of SiO_2 after only one ALD cycle (Figure 3a). This suggests that the oxygen plasma oxidizes the HF-last Si surface during the initial cycle, in addition to any first-cycle deposition of SiO_2. Subsequent increases in SiO_2 film thickness vary linearly with ALD cycle number, indicating that ALD after this initial substrate surface oxidation is capable of precise SiO_2 thickness control (Supporting S4). Despite the initial surface oxidation, the 7.7 Å oxide layer formed is still significantly thinner than the thinnest layers formed in our previous research employing SPA oxidation (14.6 Å), where fast initial SiO_2 growth was also observed.[9] MIS anode fabrication was completed by depositing ALD-TiO_2, followed by electron beam evaporation of a blanket 2 nm Ir water oxidation catalyst and Pt (for p^+Si substrate) or Al (for nSi and p^+nSi substrate) back-contact (more details in the experimental section).

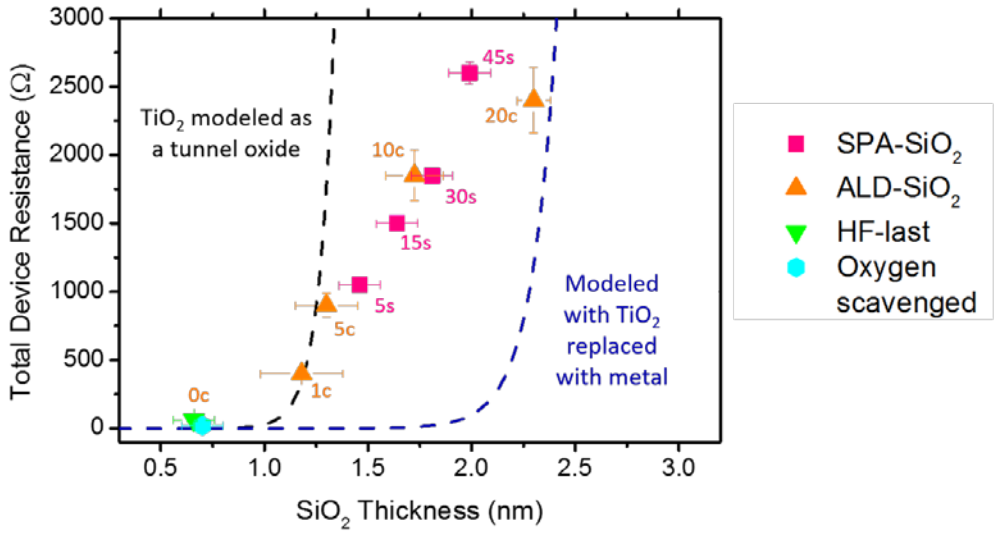

Figure 4. Resistance dependence for various interface layer preparations Plot of modelled total device resistance vs. thickness for samples with 2 nm Ir / ~1.5-2.0 nm TiO_2 / 'x' nm SiO_2 / nSi under 1 sun illumination fabricated with various methods. Thickness was determined ellipsometrically for the ALD-SiO_2 samples (shown with the number of cycles in orange) and SPA samples (shown with the number of seconds of plasma treatment in pink), and using XPS for HF-last (green) and O-scavenged samples (blue). See Supporting S6 for corresponding electrochemistry results.

Figure 4 shows the resistance calculated from n-type Si anodes with ALD-SiO_2 interlayer and from similar silicon anodes that include a SPA-derived SiO_2 interlayer (from previous reference 10) on which TiO_2 ALD was performed. Also plotted are the resistance values measured for anodes with ALD-TiO_2 deposition on an HF-last surface, and a sample fabricated using post-TiO_2 deposition oxygen scavenging (see next section) of the initial vc SiO_2 interlayer. The anode series resistance is measured by fitting the empirical cyclic

voltammograms in ferri/ferrocyanide solution to a theoretical profile with a variable series resistance parameter, as described in detail in the experimental section. The ALD-SiO_2 interlayer, HF-last and oxygen scavenged samples all have ~2.0 nm of TiO_2, whereas all SPA samples have ~1.5 nm TiO_2. The bounding curves represent Sentaurus modeling of series resistance scaling with SiO_2 thickness, assuming the TiO_2 layer behaves as a tunnel barrier (left bound) or as a metallic contact (right bound).[23] Both SPA and PEALD interfacial SiO_2 exhibit similar thickness scaling between these two extremes, indicating the TiO_2/SiO_2 oxide stack has similar electrical properties regardless of which method was employed for SiO_2 formation. The thinnest (1 cycle) PEALD-SiO_2 sample, with less than ~0.77 nm of SiO_2, achieved a total device resistance ~650 Ω less than the most conductive SPA sample, which had ~ 1.5 nm of SiO_2 interlayer growth. This improvement occurs despite the fact that the ALD-SiO_2 sample had a thicker overlying TiO_2 layer, highlighting the role of the interfacial SiO_2 tunnel oxide in limiting hole transport.

The effect of a thinned SiO_2 interlayer produced via ALD on photovoltage was also explored. Figure 5 shows water oxidation overpotential, defined for a photocurrent of 1 mA/cm^2, for anodes with 2 nm Ir/~ 2.0 nm TiO_2/'x' nm ALD-SiO_2 on p^+Si (measured in the dark), and the corresponding nSi MIS junction, and p^+n buried junction photoanodes, both measured in AM1.5 light. The p^+nSi and p^+Si MIS anodes exhibit the same overpotential scaling with SiO_2 thickness and the p^+n photoanodes exhibit a nearly constant photovoltage in the range 490 to 550 mV. The nSi samples show a strong photovoltage penalty with increasing SiO_2 thickness, giving a photovoltage of 500 mV for the sample with the thinnest SiO_2 layer, to a negative inferred photovoltage of -200 mV for the thickest oxides. This trend is consistent with previous

results for photovoltage loss in n-Si MIS Schottky junction photoanodes demonstrated with increasing ALD-TiO_2 thickness.[11] The buried junction p^+nSi structure decouples the insulator layers from the junction, such that the p^+Si surface layer ensures that the hole concentration remains high at the Si/oxide interface, eliminating the photovoltage loss.[11].

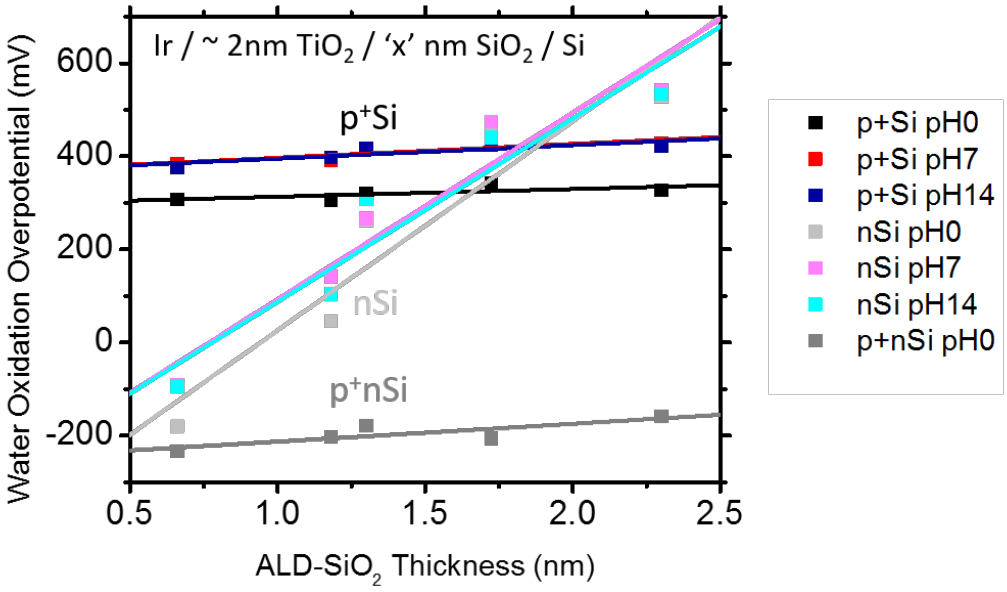

Figure 5. Photovoltage vs. SiO_2 thickness scaling for photoanodes and anodes fabricated with the ALD-SiO_2 method. Water oxidation overpotential plotted versus ALD-SiO_2 thickness, showing parallel trends for p^+Si and p^+n buried junction anodes. nSi samples show a greater photovoltage penalty with insulator thickness, consistent with previous reports.[10-11] See Supporting S5-S7 for corresponding electrochemistry results.

2.iii Oxide Thickness Reduction Through Titanium Oxygen Scavenging

Titanium assisted oxygen scavenging has been used in the past to reduce the equivalent oxide thickness (EOT) of MIS capacitors.[24-25] This technique takes advantage of the thermodynamic stability of TiO_2 and the ability of Ti to interstitially absorb large amounts of oxygen without forming an oxide phase, to scavenge oxygen from the SiO_2 IL into the Ti overlayer.[24] Oxygen scavenging reduces the thickness of the SiO_2 interlayer, but does not significantly increase D_{it}, suggesting that the remaining Si regrows epitaxially on the underlying substrate,[25] a hypothesis supported by TEM data.[24] The reduction of EOT that oxygen scavenging provides can benefit TiO_2 passivated photoanodes by decreasing the tunnel barrier to hole conduction.

Reducing the SiO_2 thickness after TiO_2 atomic layer deposition was studied by using an overlying titanium layer to scavenge the oxygen from the SiO_2 interlayer, similar to techniques employed in previous work.[24-25] A Ti film of 50 nm thickness was e-beam evaporated on the TiO_2 surface and then capped with 20 nm of W (Figure 1 3rd pane). The sample was then annealed in forming gas (95 % N_2/5 % H_2) at 300º C for 30 min. Following the forming gas anneal, the tungsten cap was etched in 30 wt % H_2O_2 aqueous solution for 5 minutes. The Ti layer was then removed using a 15 sec 50:1 DI water : HF etch. Based on the calculated etch rates (see experimental section), it was determined that a maximum of 0.9 nm of TiO_2 may be lost during etching. Titanium scavenging of oxygen was performed on p^+Si anodes with both thick and thin TiO_2, and both thick and thin SiO_2. Figure 3b shows XPS analysis performed on an as-deposited standard and an oxygen-scavenged sample. Both samples show no peaks at 455 eV or 454.1 eV, the energies of 2p 3/2 features for Ti^{2+} (TiO stoichiometry) or metallic Ti, respectively.[26] This indicates that oxygen scavenging does not significantly change the bulk stoichiometry of the TiO_2 layer, suggesting that any conductance improvements for the anode

are due to the thinning of the SiO_2 layer (slight energy shift between two traces is attributed to measurement drift due to the spectra being recorded on different days, which is not fully compensated for by energy calibration to the C 1s peak). The middle trace (dark blue) of Figure 3a shows the Si peak of an O-scavenged sample. Its SiO_2 thickness is calculated using equation (1) to be 5.3 Å, significantly thinner than the initial thickness of ~12 Å (bottom trace). This interfacial layer is even thinner than the 6.6 Å layer (also calculated from XPS data) formed by the uncontrolled regrowth of SiO_2 when TiO_2 ALD is performed on an HF-last silicon surface. This thickness is similar to the ~6.5 Å previously reported for Ti-based oxygen scavenging of SiO_2 through an interposed ALD-HfO_2 layer.[25] The present sample has 7.5 nm of TiO_2 overlying the SiO_2, demonstrating that oxygen diffusion through the TiO_2 overlayer does not limit O-scavenging based decomposition of the interface oxide.

Resistance modeling of the ferri/ferrocyanide cyclic voltammograms for these anodes can be performed, as described in the experimental section, allowing for the trend of the total device resistance to be quantified from electrochemistry data. The resistance of a sample with Ir/~2.0 nm TiO_2/vc-SiO_2 is ~12 Ω, substantially less than the 60 Ω seen in the HF-last sample (Figure 4). This resistance is comparable to the 10 - 15 Ω uncompensated series resistance measured by electrochemical impedance spectroscopy in ferri/ferrocyanide solution of an 'ideal' Ir/p^+Si sample formed by depositing metal directly on HF-last degenerately doped silicon resulting in no significant interfacial oxide (as confirmed via XPS), which represents the maximum achievable conductance with the given catalyst and substrate. Ti-based oxygen scavenging was performed on anodes protected by thin 2.0 nm TiO_2 and thicker 6.0 nm TiO_2 grown on vc-oxide, reducing the resistance of both to near ideal values (the black trace in Figure 6a/b). The

same procedure was also performed on ALD-SiO_2 samples with 1.5 nm ALD TiO_2 and thicker SiO_2 interlayers of 2.3 nm and 5.5 nm. The post-scavenging resistance of the initially 5.5 nm SiO_2 anode was slightly higher than that of the thinner oxides, suggesting that the scavenging method reduced SiO_2 thickness, but not to the 5.3 Å thickness achieved in the other samples. Based on the densities of amorphous SiO_2 and α-Ti, 2.20 g•cm^{-3} and 4.51 g•cm^{-3} respectively,[27] and the thicknesses of the two layers (5.5 nm and 50 nm respectively), the Ti film would have to absorb 7.2 at. % oxygen to reduce the SiO_2 thickness from 5.5 nm to the 5.3 Å minimum. This is significantly less than the 33 at. % maximum solubility of oxygen atoms in β-phase Ti,[28] suggesting that oxygen dissolution in the Ti overlayer is not limiting the scavenging of oxygen from the interlayer. The inability of the samples with thicker SiO_2 to reach the same minimum SiO_2 thickness under the same scavenging conditions must thus be due to diffusion limitations for O and/or the residual Si through the initially thick SiO_2. The SiO_2 interlayer thickness reduction achieved led to a significant series resistance reduction, yielding the greatest performance improvement of any photoanodes tested in this study, as Figure 6c illustrates. Figure 6c also shows that oxygen scavenging lowers the pH 0 water splitting overpotential for all samples. Some of this loss can be accounted for by the reduction of up to ~1 nm in TiO_2 thickness due to over-etching during the HF removal of the overlying titanium. However, based on previously reported values,[8] this thickness reduction will only improve overpotential by ~20 mV, which is significantly less than the observed improvements, so the majority of the improvement is due to the reduction in SiO_2 thickness.

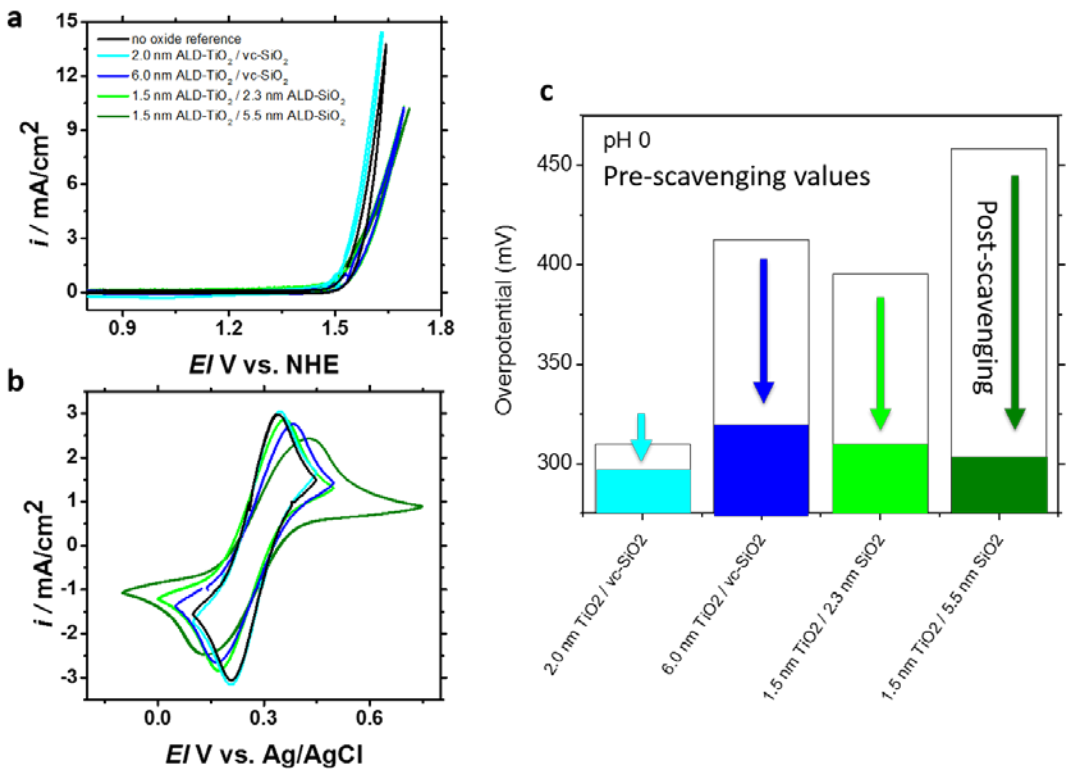

Figure 6. Conductivity improvements from oxygen scavenging (a) They key shows the initial anode stack composition before scavenging and the CV curve gives the result of the post-scavenged anode. These water oxidation curves in pH 0 acid show that regardless of initial SiO_2 thickness, all samples ended up with similar near-ideal overpotential post-scavenging **(b)** FFC curves for the same anodes show that all samples with $\leq$ 2.3 nm of SiO_2 initially have near ideal peak to peak splitting (black curve). Legend is the same as (a) **(c)** Bar graph representation of the overpotential improvement to reach 1mA/cm^2 of each oxide bilayer sample post-scavenging (solid colors) as compared to its own initial overpotential before scavenging (empty bar).

An oxygen-scavenged sample, fabricated using Ir/2.0 nm TiO_2/vc-SiO_2/nSi, was characterized under AM1.5 simulated solar illumination and compared with an otherwise identical sample on p^+Si tested in the dark to quantify the effect of oxygen scavenging on photovoltage. The nSi sample had a measured photovoltage of 450 mV in FFC (Supporting S3). This value is comparable to the 470 mV measured for nSi MIS photoanodes fabricated in these experiments during the same TiO_2 deposition on vc-oxide, without the oxygen scavenging treatment and without the requisite forming gas anneal, and is slightly less than the ~550 mV achieved with the buried junction p^+nSi substrate. Previous research on similar TiO_2-protected nSi photoanodes that included a forming gas anneal after OER catalyst deposition also achieved maximum photovoltages of ~550 mV, but with an anneal temperature of 450^0C, rather than the 300^0C oxygen scavenging anneal performed in the present experiments.[7] The effect of forming gas temperature on TiO_2-protected photoanode performance is a topic of ongoing study. Regardless, the fact that that the photovoltage after oxygen scavenging is not significantly decreased compared to the as-deposited case is consistent with previous reports demonstrating that this technique results in the epitaxial regrowth of a high quality Si crystal and does not significantly increase the oxide/semiconductor interface trap density[25].

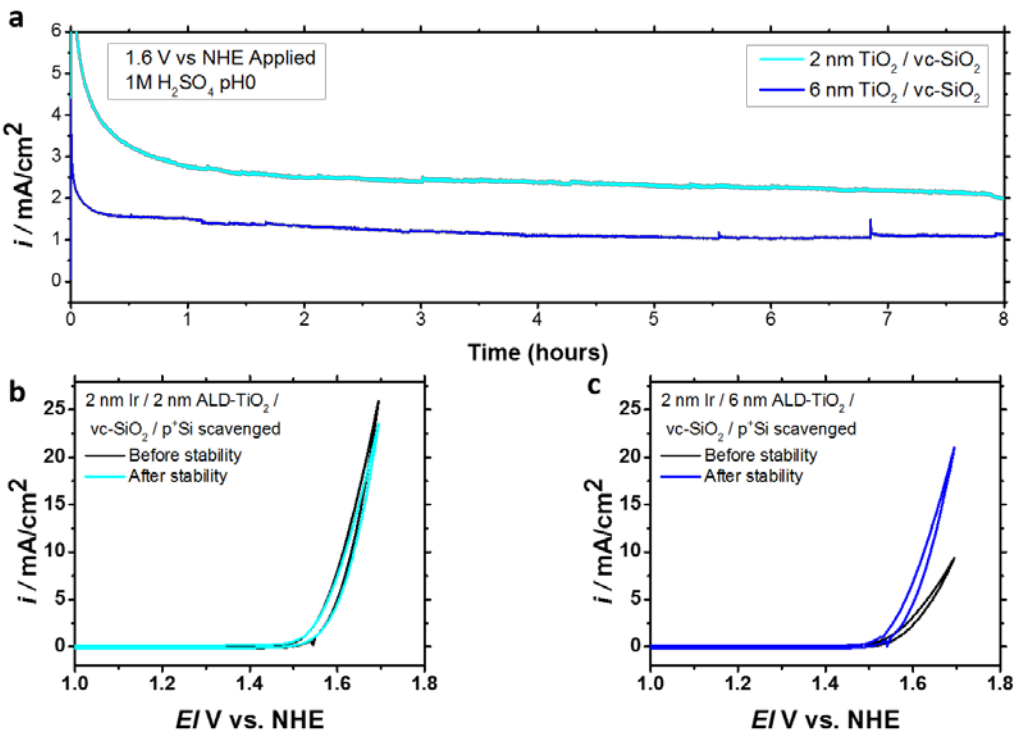

Figure 7. Stability of Ir/TiO_2/scavenged-SiO_2/p^+Si anodes with SiO_2 thinned through oxygen scavenging (a) Both samples with thinned SiO_2 show stable current after initial losses due to bubble formation and imperfect mass transport of product away from surface. **(b, c)** Both samples show lowered overpotential after the stability test.

Improvements in conductivity brought about by reducing SiO_2 thickness are, however, only significant if they do not degrade the stability of anodes during water splitting. Figure 7 shows 8 hour chronoamperometry tests of oxygen-scavenged Ir/TiO_2/scavenged-SiO_2/p^+Si anodes measured in the dark with varying deposited TiO_2 thickness performed at pH 0 and 1.6 V vs. NHE. The initial reduction in current is due to bubble formation in the test cell, which adds an additional overpotential, resulting in less potential dropped across the anode.[29] After steady

state is reached for bubble formation and mass transport of the electrolyte to the anode surface, both samples show stable current. Overpotential measurements, performed in acid before and after the stability test (Figure 7a and 7b), show slightly reduced overpotential for water splitting after the chronoamperometry test of both samples, particularly with thicker TiO_2. As long term stability is a crucial aspect in the development of viable MIS based water splitting anodes, deeper analysis of microstructure, chemical bonding, and failure mechanisms is an important area of ongoing study. This is beyond the scope of this paper and is the subject of ongoing research. Given the endurance results of figure 7, the ability of MIS anodes with thinned SiO_2 on silicon to perform water oxidation without degradation for 8 hours suggests that a >1.2 nm SiO_2 IL is not necessary for the long-term stability of TiO_2 passivated silicon anodes.

III. Conclusions

We report the beneficial effects of an ultrathin SiO_2 interfacial layer on the performance of ALD-TiO_2 protected Si anodes for water splitting, based on measurements of two types of photoanodes (nSi MIS Schottky junction and p^+nSi MIS buried junction photovoltaic-biased photoelectrosynthetic cells), and supporting evidence provided by measurements of p^+Si anodes in the dark. ALD of TiO_2 on an H-terminated, Si(100) surface leads to anodes with higher conductance than those fabricated on the wafer vendor-supplied chemical SiO_2 surface. However, this improvement comes at the penalty of film thickness variations unacceptable for most applications. In addition, XPS analysis showed that a thin SiO_2 interfacial layer regrows on the HF-last Si (100) surface during TiO_2 ALD. In order to fabricate devices with controlled, and very small IL, thicknesses, SiO_2 ALD was studied, allowing formation of interlayer oxides < 1.3 nm in thickness. To form even thinner SiO_2 layers, titanium coating and annealing to

scavenge oxygen from an initial SiO_2 interlayer was performed after TiO_2 ALD, allowing the formation of IL thicknesses less than the observed SiO_2 regrowth that occurs during ALD on an HF-last Si (100) surface. This oxygen scavenging technique is capable of reducing the series resistance of anodes with initial SiO_2 IL thicknesses of up to 5.5 nm, to values consistent with Ir/p^+Si contacts having no significant interfacial oxide interlayers present. It is also capable of reducing the resistance of bilayer oxide coated anodes with thicker TiO_2 protective coatings, due to the dominant effect of the SiO_2 tunnel barrier on overall resistance. Finally, when performed on anodes that have ≤ 2.3 nm of initial SiO_2 and a 2.0 nm TiO_2 protective coating, oxygen scavenging via a reactive Ti metal overlayer produces anodes with comparable overpotential to a reference anode where the catalyst metal is deposited directly on HF-etched, degenerately doped p^+Si reaching near-ideal conductivity.

Experimental Section

Silicon Substrates

Three substrates were used in this study: p^+Si for conductivity studies, nSi for MIS Schottky photoanodes, and p^+nSi for MIS buried-junction photoanodes. The conductivity studies are performed with heavily boron-doped (100) p-type silicon wafers (ρ=0.001-0.002 Ω·cm, thickness 505-545 μm). The MIS Schottky photoanodes are fabricated with moderately phosphorous-doped (100) n-type silicon wafers (ρ=0.14-0.24 Ω·cm, thickness 450 μm). MIS p^+n buried-junction photoanodes are fabricated with n-type silicon base wafers that are subjected to a standard clean using a Semitool Spray Acid: first the wafers are subjected to ozone and DI water, then NH_4OH (2000:1) is added to help remove particles and organics, and

lastly ozone, DI water, and HF (1150:1) are used to etch the chemical oxide and regenerate the surface oxide also removing any metallic species. The implant is performed with a 4 x 10^{15} cm^2 dose of boron at 15 keV. Following the implantation, the samples were annealed at 950^0C for 40 minutes. The junction depth was characterized in two ways. First the surface was beveled at a known angle through the p^+ surface region and the nSi was stained allowing for an optical measurement to determine the depth. This resulted in a calculated depth of 448 nm. Secondly, the p^+ region was preferentially etched using a HNO_3:HF solution and scanning electron microscopy (SEM) was utilized to directly measure a junction depth of ~460 nm.

Slot-Plane-Antenna (SPA) SiO_2 and Sentaurus Modelling for Figure 4

Figure 4 is an adaption from reference 10 taking the previously obtained theoretical bounding curves and SPA-SiO_2 data to directly compare the HF-last results, ALD-SiO_2 results, and oxygen scavenging results of this work. For the SPA-SiO_2 series, prime grade Si (100) wafers were prepared using a three part clean: 10 minutes at 50°C in 5:1:1 H_2O:H_2O_2:NH_4OH to remove trace organics, 10 minutes at 50°C in 5:1:1 H_2O:H_2O_2:HCl to remove trace metal ions, and then 30 seconds in 2% HF to remove the silicon dioxide layer. The SiO_2 layer is regrown with precise thickness control using the slot plane antenna (SPA) method, which utilizes radical oxidation to grow ultrathin oxide layers. The bounding curves are simulations performed using Synopsys Sentaurus (Version I-2013.12-SP1). All details for both SPA-SiO_2 and the Sentaurus modelling can be found in reference 10.

TiO_2 Thermal Atomic Layer Deposition with TDMAT

Titanium dioxide layers were deposited by a custom home-built ALD instrument with tetrakis(dimethylamido)titanium (TDMAT) as the metal precursor and water as the oxidant. The bubbler is kept at 70^0C and a gradient is maintained between the bubbler and chamber reaching 120^0C at the inlet. The substrate temperature was approximately 170^0C for all deposition in accordance with the ALD window reported previously, the TDMAT was pulse time was 0.7s and the H_2O pulse time was 0.5s. The equilibrium purge pressure was approximately 600mTorr. These depositions had stable growth rates of ~0.5Å/cycle over the thickness ranges studied. Details of the ALD system and process have been published previously.[30]

SiO_2 Plasma Enhanced Atomic Layer Deposition with TDMS

ALD of SiO_2 was performed in a Cambridge Nanotech Fiji F202 system with tris(dimethylamino)silane (TDMS) precursor and an oxygen plasma oxidant. This tool is in a shared research facility, Stanford Nano-Fabrication (SNF) and is used for the deposition of a variety of oxides and nitrides on cleaned Si/SiO_2 substrates. Analogous wafer cleans as performed for the slot-plane-antenna (SPA) treated samples and detailed above are performed on all substrates prior to ALD. The TDMAS is unheated, and a positive temperature gradient is maintained from the bubbler to the chamber, which is held, along with the substrate, at 200^o C throughout the deposition. O_2 plasma is derived from a 300 W RF plasma source. Each cycle consists of a 0.4 second TDMAS pulse followed by a 5 second wait, 20 second exposure to 50 sccm of O_2 plasma and 25 second wait. A constant flow of Ar and N is maintained throughout the deposition.

Oxygen Scavenging Process

After TiO_2 ALD, a 50 nm Ti overlayer and 20 nm W capping layer were electron beam evaporated onto the TiO_2 surface, without breaking vacuum between the two evaporations. The W serves to prevent the Ti from oxidizing on exposure to the atmosphere. Scavenging was performed by annealing the samples for 30 minutes at 300º C in forming gas (95 % N_2:5% H_2). Following the forming gas anneal, the tungsten cap was etched in 30 wt % H_2O_2 solution for 5 minutes. The etch rate of Ti in H_2O_2 was experimentally determined to be < 0.5 nm/min, meaning that this etch will not significantly attack the underlying Ti. The Ti layer was then removed using a 15 sec 50:1 DI water:HF etch. Dilute HF had the highest etch selectivity of Ti over TiO_2 of any of the etches tested (etch rates of ~300 nm/min of Ti[25] and ~11 nm/min for TiO_2). The etch time is carefully controlled to remove all Ti without sacrificing the TiO_2 protection layer and thicknesses were checked by ellipsometry after etching. Based on the calculated etch rates, it was determined that a maximum of 0.92 nm of TiO_2 may be lost during etching. After etching the front and back contacts were deposited. No anneals were performed after contact deposition.

Deposition of Catalyst and Back-Contact

Iridium metal catalysts and platinum and aluminum back-contact metals were deposited by electron beam evaporation. The surface catalyst was a 2 nm layer of iridium for all water splitting cells. Previous work has shown that even with these very thin layers, the catalyst is uniform in thickness.[4] All p^+Si samples had a back-side contact of 20 nm of e-beam Pt

deposited and n-Si samples had an e-beam deposited 100 nm Al backside contact to provide an Ohmic contact.

Ellipsometry

The TiO_2 thickness was measured using a Gaertner ellipsometer calibrated by cross-sectional transmission electron microscopy (TEM) analysis as described in previous work.[8] The thickness of a film in the TiO_2/SiO_2 bilayer is calculated from ψ and Δ given the thickness of the other layer and the indices of refraction. In previous work[8], a set of TiO_2 films was analysed by TEM and these thicknesses were used to fit the index of refraction of 2.4 as also used in this work, similar to values of 2.3 – 2.4 found for other ALD amorphous films, and 2.4 – 2.5 for anatase films, but less than the 2.6 – 2.9 recorded for rutile films.[31-32]

Aqueous Solution Preparation

Aqueous solutions of pH 0, 7, and 14 were prepared to study performance across the pH range. Solutions were 1 M H_2SO_4, 1 M NaH_2PO_4/Na_2HPO_4 buffer, and 1 M NaOH respectively. All solutions were prepared with MilliQ water and checked against both a bench top glass pH electrode and the reversible hydrogen potential using Pt electrodes. All plotted water oxidation curves and ferri/ferrocyanide cyclic voltammograms are the raw data from the three electrode measurement, not corrected for uncompensated series resistance.

Ferri/Ferrocyanide Preparation

The reversible redox couple ferri/ferrocyanide was prepared to study electronic carrier transport in these anodes. Potassium ferricyanide and potassium ferrocyanide trihydrate were used to make a 1:1 solution containing 10 mM of each species with 1M potassium chloride. MilliQ water was used for these solutions.

Cyclic Voltammetry

Electrochemical measurements were carried out using a glass frit isolated Ag/AgCl/saturated KCl reference electrode and a platinum wire counter electrode, as detailed by Chen et al..[7] The active area of 0.196 cm^2 was defined by a bored Teflon cone pressed down onto the nano-layered anode. All ferri/ferrocyanide CV's were measured at a scan rate of 100 mV/s in a static solution. A peristaltic pump was used during water oxidation to circulate the solution at 1 mL/s; water oxidation current vs. potential data were also collected at a scan rate of 100 mV/s.

Resistance Modeling of Cyclic Voltammograms

Resistance is extracted from ferri/ferrocyanide cyclic voltammograms by fitting to theoretically determined profiles simulated by EC-lab software V10.21. The initial parameter set is obtained by fitting an ideal-device with the electrochemical impedance spectroscopy determined uncompensated series resistance subtracted and assuming no additional resistance. Physical parameters used are that of the actual system, namely a surface area of 0.196 cm^2, Fe^{2+}/Fe^{3+} concentrations of 10mM, a scan rate of 100mV/s, room temperature, and the charge transfer coefficient α=0.50. The best fit is obtained with k_0 = 0.01 cm/s, $D_O = 8.5 \times 10^{-6}$ cm^2/s, and $D_R = 3.5 \times 10^{-6}$ cm^2/s as described previously.[8] Additional cyclic voltammograms are then

fit by varying only the uncompensated series resistance, called the 'total device resistance' on the figures here representing the differential anode resistance from the ideal measured about the zero voltage point. The EIS of an ideal anode provides a value of 10 – 15 Ω, thus measurements in this range, such as the 12 Ω obtained for the oxygen scavenged device, represent an ideal or near-zero resistance value for the anode structure.

Associated Content

Detailed description of cell types, further thickness characterizations and all referenced cyclic voltammetry are given in the supporting information.

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Author Contributions

P.S. and A.S. prepared all HF-last and oxygen scavenging samples. P.S. prepared all ALD-SiO_2 samples. P.S. and A.S. performed all electrochemical measurements. P.S. performed all XPS analysis. A.S. performed all resistance modeling of cyclic voltammograms. A.S. maintained and qualified the TiO_2 ALD chamber. All authors designed the experiments and helped in the preparation of this manuscript.

Notes

The authors declare no competing financial interests.

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