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## A combined hard x-ray photoelectron spectroscopy and electrical characterisation study of metal/SiO<sub>2</sub>/Si(100) metal-oxide-semiconductor structures

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Combined hard x-ray photoelectron spectroscopy (HAXPES) and electrical characterisation measurements on identical Si based metal-oxide-semiconductor structures have been performed. The results obtained indicate that surface potential changes at the Si/SiO<sub>2</sub> interface due to the presence of a thin Al or Ni gate layer can be detected with HAXPES. Changes in the Si/SiO<sub>2</sub> band bending at zero gate voltage and the flat band voltage for the case of Al and Ni gate layers derived from the silicon core levels shifts observed in the HAXPES spectra are in agreement with values derived from capacitance-voltage measurements. © 2012 American Institute of Physics.

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Hard x-ray photoelectron spectroscopy (HAXPES) is emerging as a technique which has the capability of providing chemical and electronic information on much larger depth scales than conventional x-ray photoelectron spectroscopy.<sup>1–3</sup> This has potential application in the study of buried interfaces as found at the oxide/semiconductor interface, particularly if changes at this interface are of interest following the subsequent deposition of a metal capping layer in the fabrication of metal-oxide-semiconductor (MOS) structures. Photoemission sampling depths in excess of 10 nm (Ref. 4) allow for direct comparison between results obtained from electrical characterisation techniques and photoemission experiments, as these measurements can be made on identical structures thereby bridging the gap between interface chemistry and electrical properties at buried interfaces.

For this study exploring the combination of HAXPES and electrical characterisation techniques, the experiments were performed on Si(100)/SiO<sub>2</sub> MOS structures. This system was selected as the interpretation of the multi-frequency capacitance-voltage (CV) response is well developed,<sup>5</sup> the interface is representative of an unpinning surface Fermi level, and the structure allows accurate determination ( $\pm 50$  meV (Ref. 6)) of surface potential for a given gate voltage based on CV measurements. The samples were formed over *n* and *p*-doped silicon substrates and were capped with high (Ni) and low (Al) work function metals to induce surface potential shifts at the Si(100)/SiO<sub>2</sub> interface for examination by the HAXPES and CV methods. Using a photon energy of 4150 eV in these investigations allowed for the simultaneous detection of photoemission signals from metal, oxide, and substrate core levels. The band gap of Si (1.1 eV) is wide enough to allow differences in the binding energy (BE) of the *n* and *p*-doped substrate core levels to be detected, which directly reflect different Fermi level positions in the band gap.<sup>7</sup>

In this paper, we illustrate the ability of HAXPES to measure Fermi level movements in the semiconductor substrate and potential differences across the oxide for MOS

structures, and explain how these results compare with CV measurements on identical structures.

High quality thermally grown SiO<sub>2</sub> layers, with a thickness of 8 nm, were grown using a dry oxidation process in a furnace at 850 °C on both *n* ( $2\text{--}4 \Omega \text{ cm}$ ,  $\sim 1 \times 10^{15} \text{ cm}^{-3}$ ) and *p* ( $10\text{--}20 \Omega \text{ cm}$ ,  $\sim 1 \times 10^{15} \text{ cm}^{-3}$ ) doped silicon(100) substrates following a standard silicon surface clean. The samples for HAXPES analysis were capped with 5 nm Ni or 5 nm Al blanket films by electron beam evaporation. For electrical characterisation, Ni/Au (90 nm/70 nm) and Al (160 nm) gate electrodes were formed by electron beam evaporation and a lift off lithography process. The Si/SiO<sub>2</sub> samples did not receive a final forming gas (H<sub>2</sub>/N<sub>2</sub>) anneal.

HAXPES work is usually performed at synchrotron radiation sources due to the need for high brilliance to compensate for the rapid decrease in subshell photo-ionization cross-section with increasing excitation energy.<sup>8</sup> HAXPES measurements were carried out on the NIST beamline X24A at the National Synchrotron Light Source (NSLS) at Brookhaven National laboratory (BNL). A double Si(111) crystal monochromator allowed for photon energy selection in the range of 2.1–5.0 keV. An electron energy analyser was operated at a pass energy of 200 eV giving an overall instrumental energy resolution of  $\sim 0.35$  eV at the chosen photon energy of 4150 eV. Samples were fixed on a grounded Al sample holder with stainless steel clips, which connected the front of the samples to the sample holder. In order to ensure correct energy calibration throughout the experiment, metallic Ni Fermi edge reference spectra were acquired immediately before and after the acquisition of the SiO<sub>2</sub> and Si substrate core level peaks. The resultant error associated with this photon energy correction procedure is estimated to be no more than  $\pm 50$  meV. The maximum depletion region width for the  $1 \times 10^{15} \text{ cm}^{-3}$  doped Si substrate is  $\sim 800$  nm and the total sampling depth of the HAXPES measurements is estimated to be no more than 23 nm (Ref. 9) for the substrate Si 1s which has a kinetic energy of  $\sim 2310.5$  eV for the 4150 eV photon energy used in these studies,<sup>10</sup> where the

total sampling depth includes the ability to detect the whole of the 5 nm of metal, 8 nm of oxide, and no more than 10 nm sampling depth into the Si. Therefore, the BE of the acquired Si substrate core level peaks directly reflect the position of the Fermi level in the silicon at the Si/SiO<sub>2</sub> interface, i.e., the surface Fermi level position. However, it is noted that for Si samples in inversion, which exhibit strong surface band bending, the sampling depth of the HAXPES may cause the peaks to shift by up to 0.1 eV to lower BE.<sup>11</sup> The CV measurements were recorded using a CV enabled meter following open calibration. The measurements were performed on-wafer at room temperature (22 °C) in a probe station in a dry air environment (dew point  $\leq -65$  °C).

Figure 1 shows the Si 1s core level spectra originating from the substrate and the 8 nm SiO<sub>2</sub> layer for both *n* and *p*-doped Si, with and without the presence of a metal gate. The BE positions of the core level peaks are measured and the difference between the *n* and *p* type Si substrates is used to estimate the Fermi level separation at the Si/SiO<sub>2</sub> interface. HAXPES measurements on the uncapped Si/SiO<sub>2</sub> samples revealed that the BE position for the *p*-type Si peaks was  $\sim 0.32$  eV lower than the *n*-type substrate consistent with the Fermi level residing closer to the valence band edge for *p* type and closer to the conduction band edge for *n* type. The difference is however less than the expected value of 0.57 eV, which is calculated from the theoretical Fermi level position difference for *n* and *p* silicon with a doping concentration of  $1 \times 10^{15} \text{ cm}^{-3}$ .<sup>4</sup>

The reduction in measured difference in the Si 1s core level BE indicates that there is band bending present at the SiO<sub>2</sub>/Si interface even in the absence of a metal overlayer. In order to establish the approximate position of the Fermi level in the band gap with respect to the valence band edge prior to metal deposition, valence band spectra were acquired at the same photon energy. An extrapolation of the Si valence band to a zero signal intensity yields the approximate

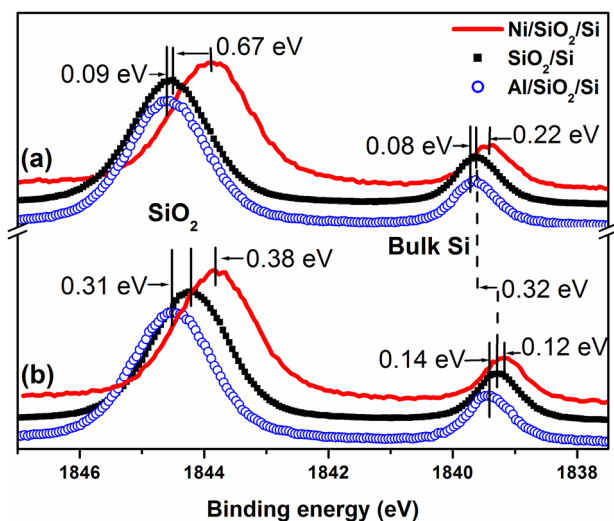


FIG. 1. Normalised Si 1s core level spectra acquired at a photon energy of 4150 eV for the uncapped Si/SiO<sub>2</sub>, Ni (5 nm) capped Si/SiO<sub>2</sub> and Al (5 nm) capped Si/SiO<sub>2</sub> samples, showing the shifts in the core level after metal deposition and the changes in the potential across the SiO<sub>2</sub> layer cause by different work function metals for (a) *n*-type, and (b) *p*-type Si substrates. The dotted lines show the energy separation between *n* and *p* type samples without metal gates.

position of the valence band edge.<sup>12</sup> Although more accurate methods have been recently employed,<sup>13</sup> this method is sufficient to provide the accuracy required here. Reference spectra of a sample with a Ni gate were subsequently taken, and the nickel metallic edge was used to establish the Fermi level position at 0 eV BE on the *x*-axis. These measurements show that the Fermi level of the *n*-type sample is  $\sim 0.95$  eV above the valence band edge, indicating an accumulated surface with the surface Fermi level above its flat band position of 0.85 eV above the valence band. Similar measurements for the *p*-type sample show the Fermi level is  $\sim 0.66$  eV above the valence band edge, above its flat band position of 0.28 eV, indicating that the *p*-type surface is weakly inverted. Both of these observations are consistent with fixed positive charge in the SiO<sub>2</sub> which is expected based on the oxidation temperature of 850 °C and the absence of any post deposition annealing.<sup>14</sup>

The effect of the deposition of high (Ni—5.15 eV (Ref. 15)) and low (Al—4.1 eV (Ref. 15)) work function metals (5 nm) on the SiO<sub>2</sub> surface on the Si 1s binding energy is also shown in Figure 1. If the Fermi level at the SiO<sub>2</sub>/Si interface is free to move, it would be expected to align with the metal Fermi levels resulting in a slight increase in band bending (increase in core level BE) for the *n*-type substrate with the low work function Al contact, given that the electron affinity of Si is 4.05 eV. For the Ni contact, a large increase in band bending (reduction in core level BE) would occur as Ni has a high work function. Alternatively, for the *p*-type substrate, an Al contact would result in an increase in band bending (increase in core level BE), while a Ni contact would result in a decrease in band bending (decrease in core level BE). HAXPES measurements in Figure 1 for samples with Al gates show that the Si 1s signal originating from the silicon substrate, located at a BE of 1839 eV, shifts 0.14 eV for the *p*-type, and 0.08 eV for the *n*-type to higher BE. While for the Ni gate, the Si 1s peak shifts  $\sim 0.12$  eV for the *p*-type and  $\sim 0.22$  eV for the *n*-type to lower BE energy. The experimentally observed shifts for the samples with metal gates are therefore consistent with the direction of expected surface Fermi level movement, while not matching the expected shift magnitudes.

The limited ability to move the Fermi level closer to the valence band edge with the high work function Ni is consistent with fixed positive charge in the SiO<sub>2</sub> which will tend to accumulate electrons at the Si/SiO<sub>2</sub> interface. In addition, as the samples received no final forming gas (H<sub>2</sub>/N<sub>2</sub>) anneal, it is expected that interface defects originating from silicon dangling bonds (P<sub>b</sub> centres) will be present, which will also restrict somewhat the movement of the surface Fermi level. The P<sub>b</sub> centres at the Si(100)/SiO<sub>2</sub> interface have levels in both the lower and upper energy gap regions.<sup>16–18</sup>

Work function differences between the metal and the partially pinned Si Fermi level should also result in a potential difference across the oxide layer which should manifest as a BE shift of the associated oxide core levels.<sup>3,7</sup> These changes would be expected to be most apparent between the *n*-type Si and the Ni, or the *p*-type Si and the Al, as these both represent the largest difference in work functions. The spectra in Figure 1 also show the changes in BE of the Si 1s

oxide peak (located at  $\sim 1844$  eV) for both dopant types resulting from metal deposition. For a  $p$ -type sample the deposition of the low work function Al results in an increase in the Si 1s oxide peak BE of 0.31 eV reflecting a potential decrease consistent with the alignment of the Fermi levels. For the Ni capped  $p$ -type sample, a decrease in the BE of 0.38 eV is measured reflecting a potential increase across the oxide caused by the high work function Ni contact after Fermi level alignment. The corresponding BE shift for the  $n$ -type sample was 0.09 eV to higher BE, and 0.67 eV to lower BE for the Al and Ni cap, respectively. All of these changes are consistent with the expected polarity of the potential difference across the oxide layer caused by the low and high work function metals. Figures 2(a) and 2(b) show a schematic diagram illustrating the changes in BE due to Fermi level movements and changes in the potential field across the oxide for a  $p$ -type Si substrate following the deposition of Al and Ni contacts, respectively. The centre of the Si 1s oxide peak is located at a weighted average of the photoemission signal intensity from the different depths into the oxide.<sup>3</sup> Note that the shift resulting from Fermi level movement in the bulk Si is also present in the oxide peaks, so any shift in the oxide peaks is a combination of the Fermi level movement and a potential difference across the oxide.

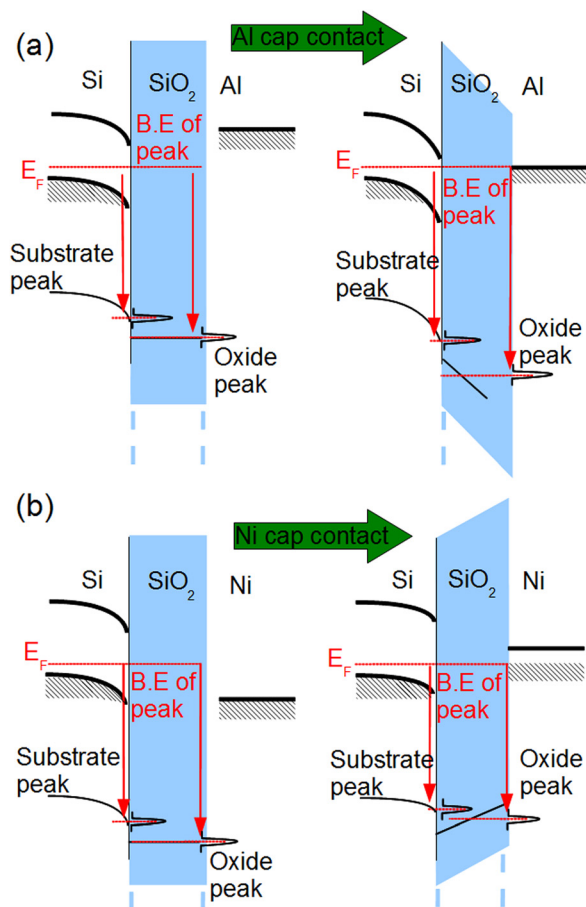


FIG. 2. (a) Band diagram illustrating the BE shifts due to an electric field across the oxide caused by metal deposition, for  $p$ -type Si showing a potential difference across the oxide for a  $p$ -type sample with an Al gate. (b) Band diagram showing a potential difference of the opposite polarity for a  $p$ -type sample with a Ni gate.

The CV responses recorded at an ac signal frequency of 1 MHz for the corresponding Al (160 nm) and Ni/Au (160 nm) gate Si/SiO<sub>2</sub> MOS capacitors for the  $n$  and  $p$ -type silicon are shown in Figures 3(a) and 3(b), respectively. The multi-frequency CV responses from 1 kHz to 1 MHz (not shown) exhibit the features associated with P<sub>b</sub> defects at the Si/SiO<sub>2</sub> interface, consistent with previous publications.<sup>17</sup> The presence of unpassivated silicon dangling bonds (P<sub>b</sub> defects) is expected as the samples did not receive a final forming gas anneal. The ac signal frequency of 1 MHz, shown in Figures 3(a) and 3(b), was selected to minimise the effect of the silicon dangling bond defects on the CV response. Considering first the surface potential at 0 V, which is the condition for the HAXPES measurements, the CV observations match the expected results, and are consistent with the HAXPES measurements, indicating: surface accumulation for the Al gate over the  $n$ -type, inversion of the surface for the Al gate over  $p$ -type, and depletion of the surface for the Ni gate over both  $n$  and  $p$ -types. From the CV responses, the surface potential at 0 V can also be calculated by fitting the CV with a Poisson CV solver.<sup>19,20</sup> From the resulting surface potentials ( $\Phi_s$ ), the values of  $E_F - E_v$  at 0 V are shown in Figure 3, and compared with the corresponding HAXPES measurements in Table I. The shift in surface potential for the Al with respect to the Ni gate samples on

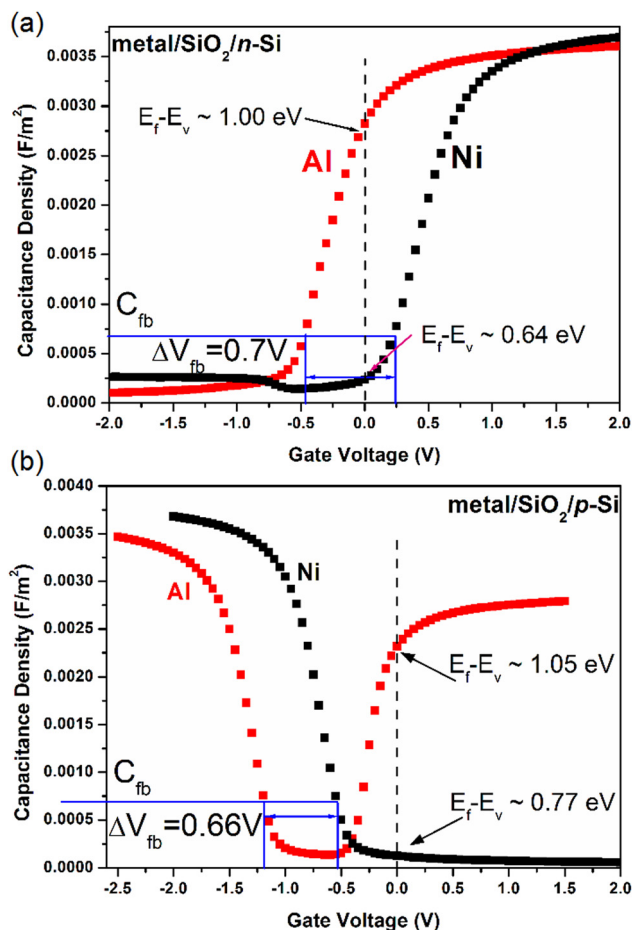


FIG. 3. CV characteristics (1 MHz) for the metal/SiO<sub>2</sub>/Si samples with Al and Ni gates for both (a)  $n$ -type, and (b)  $p$ -type substrates, displaying both the flat band shifts  $\Delta V_{fb}$  and the calculated surface Fermi level ( $E_f$ ) position at zero gate voltage. The Fermi level position is with respect to the valence band ( $E_f - E_v$ ).

TABLE I. Summary of the HAXPES and CV results.

Sample	$E_F-E_v$ (SiO <sub>2</sub> /Si)	$E_F-E_v$ (Al/SiO <sub>2</sub> /Si)	$E_F-E_v$ (Ni/SiO <sub>2</sub> /Si)	$\Delta E_f$ (Al-Ni shift)	Flat band (Al-Ni shift)
<i>n</i> -type (CV)	N/a	1.00 eV	0.64 eV	0.36 eV	0.7 V
<i>n</i> -type (HAXPES)	0.95 eV	1.03 eV	0.73 eV	0.3 eV	0.76 eV
<i>p</i> -type (CV)	N/a	1.05 eV	0.77 eV	0.28 eV	0.66 V
<i>p</i> -type (HAXPES)	0.66 eV	0.8 eV	0.54 eV	0.26 eV	0.69 eV

*n*-type silicon is 0.36 eV which compares to the value of 0.3 eV from HAXPES. For the *p*-type sample the surface potential shift from the Al to the Ni gate is 0.28 eV which compares to 0.26 eV from the HAXPES as shown in Table I. When taking into account the errors in surface potential for the two methods which are  $\pm 50$  meV for both the HAXPES and CV fitting, this is a good agreement between the HAXPES and CV analysis. The increase in capacitance observed in Figure 3(b) for the *p*-type Al/SiO<sub>2</sub>/Si MOS structure at positive gate bias is attributed to peripheral inversion effects.<sup>21</sup>

As well as providing information on the surface potential at zero gate voltage, the HAXPES method can also detect the flat band voltage difference between the Ni and Al gate samples. The flat band voltage in a MOS capacitor is the gate voltage required to offset the built in potential, which is across the oxide and the silicon substrate at 0 V, to achieve a flat band condition. As a consequence, the difference in the flat band voltage in the CV for the Ni and Al gate samples should relate to the BE shifts measured in the HAXPES Si 1s oxide signal, as these spectra include both the Fermi level shifts in the substrate and the potential difference across the oxide. The calculated flat band capacitance ( $C_{fb}$ ) is indicated in Figures 3(a) and 3(b), and the flat band voltage difference for the Al and Ni gate samples is 0.7 V for the *n*-type and 0.66 V for the *p*-type. This is in very good agreement with the combined Al-Ni shifts in the Si 1s oxide spectra in Figure 1, which are 0.69 eV and 0.76 eV for the *p* and *n*-type substrates, respectively. The agreement between the surface potential differences and the flat band voltage differences for the two measurement techniques are shown in Table I. There is very good agreement in the relative shifts between samples with Al and Ni gates, however, there is a discrepancy between the *p*-type Fermi level positions determined by the two techniques. The results in Figure 3 provide a possible explanation. The *p* type samples are either at the onset of strong inversion (Ni) or in strong inversion (Al) at 0 V and consequently have larger surface band bending than the *n* type samples which are in depletion (Ni) or slight accumulation (Al). If we assume a maximum sampling depth into the Si substrate of 10 nm, the band-bending will vary by 0.1–0.15 eV for a *p* type sample in inversion based on a Poisson-Schrodinger simulation.<sup>11</sup> This variation would be apparent in the HAXPES measurement resulting in a lower  $E_F-E_v$  than obtained from the CV analysis.

In conclusion, the large sampling depth of HAXPES has been exploited to characterise band bending in metal/SiO<sub>2</sub>/Si

MOS structures fabricated with both high (Ni) and low (Al) work function metals. The HAXPES measurements of the Si 1s core level have been shown to be sensitive to changes in band bending at the Si/SiO<sub>2</sub> interface due to the presence of high (Ni) and low (Al) work function metals. The Si 1s core level originating from the SiO<sub>2</sub> layer indicates the presence of a potential difference across the SiO<sub>2</sub> layer. The changes in the band bending at the Si/SiO<sub>2</sub> interface and the potential difference across the SiO<sub>2</sub> are consistent with the difference in metal work functions and are in agreement with the results derived from CV measurements.

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