Title	Analysis of effective mobility and hall effect mobility in high-k based In0.75Ga0.25As metal-oxide-semiconductor high-electron-mobility transistors
Authors	Negara, Muhammad A.;Veksler, D.;Huang, J.;Ghibaudo, G.;Hurley, Paul K.;Bersuker, G.;Goel, N.;Kirsch, P.
Publication date	2011
Original Citation	Negara, M. A., Veksler, D., Huang, J., Ghibaudo, G., Hurley, P. K., Bersuker, G., Goel, N. and Kirsch, P. (2011) 'Analysis of effective mobility and hall effect mobility in high-k based In0.75Ga0.25As metal-oxide-semiconductor high-electron-mobility transistors', Applied Physics Letters, 99(23), pp. 232101. doi: 10.1063/1.3665033
Type of publication	Article (peer-reviewed)
Link to publisher's version	http://aip.scitation.org/doi/abs/10.1063/1.3665033 - 10.1063/1.3665033
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Citation: Appl. Phys. Lett. **99**, 232101 (2011); doi: 10.1063/1.3665033
View online: http://dx.doi.org/10.1063/1.3665033
View Table of Contents: http://aip.scitation.org/toc/apl/99/23
Published by the American Institute of Physics

Analysis of effective mobility and hall effect mobility in high-*k* based $In_{0.75}Ga_{0.25}As$ metal-oxide-semiconductor high-electron-mobility transistors

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(Received 13 July 2011; accepted 9 November 2011; published online 5 December 2011)

We report an $In_{0.75}Ga_{0.25}As$ metal-oxide-semiconductor high-electron-mobility transistor with a peak Hall mobility of 8300 cm^2/Vs at a carrier density of $2 \times 10^{12}\,cm^{-2}$. Comparison of split capacitance-voltage (CV) and Hall Effect measurements for the extracted electron mobility have shown that the split-CV can lead to an overestimation of the channel carrier concentration and a corresponding underestimation of electron mobility. An analysis of the electron density dependence versus gate voltage allows quantifying the inaccuracy of the split-CV technique. Finally, the analysis supported by multi-channel conduction simulations indicates presence of carriers spill over into the top InP barrier layer at high gate voltages. © *2011 American Institute of Physics*. [doi:10.1063/1.3665033]

In recent years, significant research efforts have focused on exploring the use of high mobility materials such as III-V, Ge, and graphene as replacements for Si channels in future complementary metal-oxide-semiconductor (CMOS) technology nodes. In the case of III-V channel materials there has been a growing interest in quantum well field-effect transistors (QW-FETs) or metal-oxide-semiconductor high-electron-mobility transistors (MOSHEMTs) due to the high intrinsic electron mobility of III-V materials.[1–5] The use of $In_{0.7}Ga_{0.3}As$ MOSFETs with an Al_2O_3 gate oxide and $InP/In_{0.52}Al_{0.48}As$ double-barrier layer structures have been reported with a peak channel mobility of 4729 cm^2/Vs at a density of $1.5 \times 10^{12}\,cm^{-2}$ and capacitance equivalent thickness (CET) ~ 3 nm.[1] High-*k* InGaAs MOSFETs employing a flat band architecture, with a GaAs/AlGaAs barrier layer and bottom Si-δ doping, exhibited a peak mobility reaching 5500 cm^2/Vs, at density of $2-3 \times 10^{12}\,cm^{-2}$ for a CET around 5 nm.[2] The electron mobilities reported were extracted using the split capacitance-voltage (CV) technique,[6] which assumes that the integral of the gate-to-channel capacitance (C_{gc}) yields the charge density contributing to conduction. However, for device structures that exhibit high interface state densities (D_{it}), the interface states can affect the calculated mobility,[7] which must be taken into account when using the split CV method. When the energies of interface defects in the high-*k*/InGaAs system align with the InGaAs conduction band, the evaluation of true effective mobility (μ_{eff}) from the split CV is further complicated.[8,9] As the Hall voltage is developed by mobile charges only, the Hall Effect technique can yield values for the conduction charge density and the carrier mobility that are *not* impacted by the interface states/defects. This study applied both techniques to extract and compare the carrier density and mobility values determined using the split CV method and the gated Hall bar approach for InGaAs MOSHEMT devices.

Lattice-matched buffer layers of InAlAs were grown on a semi-insulating InP substrate using molecular beam epitaxy. The channel was 10 nm $In_{0.75}Ga_{0.25}As$. Carriers in the channel were separated from the dopants to reduce Coulomb scattering due to ionized impurities. This was achieved by placing a $3 \times 10^{12}\,cm^{-2}$ silicon delta-doped layer into the lower InAlAs barrier and by introducing an undoped spacer layer between the delta-doped layer and the channel. The channel was then buried using a 2 nm thin undoped large band gap InP barrier layer and thick n^+ InGaAs capping layer. After growth, an active region was patterned, the n^+ capping layer was etched out in the active region, and 1 nm Al_2O_3/5 nm ZrO_2/TiN films were deposited by atomic layer deposition (ALD). The use of Al_2O_3/high-*k* bilayers has been shown to reduce gate leakage and interface defect density in $In_{0.53}Ga_{0.47}As$ MOS systems.[10] A high resolution cross-sectional transmission electron microscopy (HRTEM) image through the gate stack region of the high-*k* $In_{0.75}Ga_{0.25}As$ MOSHEMT is shown in the inset to Fig. 1. The n^+ InGaAs cap remained in the source-drain junctions, and a metal was used for making ohmic contacts. After device lithography, Hall bar-type MOSHEMTs with a gate length (L) = 170 μm and width (W) = 20 μm were used for electrical measurements. A long channel device was chosen to minimize the effect of series resistance.

Fig. 1 shows the temperature dependence of the MOSHEMT transfer characteristics at a drain voltage (V_{ds}) = 50 mV over a range of temperatures (77 K to 300 K). The gate leakage current was found to be less than 3×10^{-9} A at a gate voltage (V_g) = 1 V, which is negligible compared to the drain current (I_d). The drain current for $V_g > 0$ is reduced at higher temperatures, and the influence of temperature on the drain current tends to diminish as the gate voltage increases. This effect could be associated with the carriers spilling over into the InP barrier layer, which is more effective at elevated temperatures, and preventing the channel carrier concentration from increasing at higher gate voltages. Such population of the barrier layer may result in

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the formation of a parallel channel, and is considered later in this letter.

The off-current (I_{off}) is significantly reduced at lower temperatures, whereas I_{gate} is much less than I_{off} at all temperatures. At $V_g = -1$ V, the activation energy of ~0.14 eV was extracted, similar to that reported for trap assisted tunneling (TAT) in an InP film,[11] suggesting a defect-related conduction through the InP barrier layer may be the source of the high I_{off} current. From the high resolution TEM inset in Figure 1, no interfacial layer between the Al_2O_3 and III-V substrate or between TiN and ZrO_2 was observed within the resolution limits. However, D_{it} in the lower band gap region is on the order of 10^{13} $cm^{-2}eV^{-1}$ (not shown), which degrades the subthreshold slope (SS) and could also contribute to the I_{off}.

To delineate contributions from gate stack defects and/or carrier spill over into the barrier layer to electron mobility, the μ_{eff} is compared to the Hall mobility (μ_{Hall}) extracted using the Hall Effect measurement at room temperature.[12,13] For the Hall Effect measurements, a magnetic field (B) up to 0.58 T was applied. A linear relationship between V_{Hall} and B for various V_g was observed, and the Hall carrier density (n_{Hall}) values were extracted. The μ_{Hall} values deduced from the conductance measurements along the channel using the extracted n_{Hall} are presented in Fig. 2.

In agreement with previous reports in Refs. 1, 4, and 5, high-*k*/$In_{0.75}Ga_{0.25}As$ devices with an InP barrier layer exhibit a high peak channel mobility ($\mu_{eff} \sim 5300$ cm^2/Vs and $\mu_{Hall} \sim 8300$ cm^2/Vs at room temperature), mainly due to: (1) charge transport occurring primarily at the epitaxial InP/$In_{0.75}Ga_{0.25}As$ interface as opposed to an high-*k*/$In_xGa_{1-x}As$ interface, (2) better interface passivation using a composite high-*k*/Al_2O_3 bilayer structure[10,14] and the use of an undoped InP barrier, and (3) separation of the channel carriers from the scattering centers in the high-*k* dielectric and/or along the high-*k*/III-V interface due to the barrier layer (InP) with a large band gap.

The maximum difference between μ_{Hall} and μ_{eff} (as measured by the split CV method) is typically less than 10%-20% for Si MOSFETs,[12] while the measurements on our devices exhibited a much greater difference (~56%). This could be related to a significant capacitance contribution to the measured C_{gc} from immobile charges when using the split CV technique and/or to the presence of parallel conduction channels in the $In_{0.75}Ga_{0.25}As$ channel and the InP capping layer. Considering first the case of mobile and immobile charges, the carrier density extracted from the split CV measurements consists of the total charges: in the channel, barrier layers, and charge trapping sites at the high-*k*/InP interface. The split CV method, when employed at room temperature, can lead to an overestimation of the channel carrier density, which, in turn, leads to an underestimation of the extracted electron mobility values.

Considering next the case of parallel transport, at higher gate voltages carriers can spill into the low mobility InP barrier layer, the parallel conduction channels should then be taken into account on the mobility extraction. The difference in the measured μ_{Hall} and μ_{eff} mobilities, described by the Eqs. (1) and (2), respectively, can be understood when multi-channel transport is assumed.[15] With two parallel transport channels (m = 2), the higher mobility layer (an intended channel = μ_1) dominates the Hall mobility due to the μ^2 dependency in the numerator of Eq. (1). The unintended parallel channel (a conducting layer with relatively lower mobility = μ_2) provides only a small contribution to the total μ_{Hall} compared to μ_{eff}.

$$\mu_{Hall} = \frac{\sum_{i=1}^{m} \mu_i \times \sigma_i}{\sum_{i=1}^{m} \sigma_i}, \quad \text{for m} = 2 \quad \mu_{Hall} = \frac{n_1 \times \mu_1^2 + n_2 \times \mu_2^2}{n_1 \times \mu_1 + n_2 \times \mu_2}, \quad (1)$$

$$\mu_{eff} = \frac{\sum_{i=1}^{m} \mu_i \times n_i}{\sum_{i=1}^{m} n_i}, \quad \text{for m} = 2 \quad \mu_{eff} = \frac{n_1 \times \mu_1 + n_2 \times \mu_2}{n_1 + n_2}, \quad (2)$$

$$n_{Hall} = \frac{I_d L}{W q \mu_{Hall} V_{ds}}, \quad (3)$$

where m = the number of parallel transport channels, n = the number of carriers, and $\sigma = qn\mu$ represents the conductivity

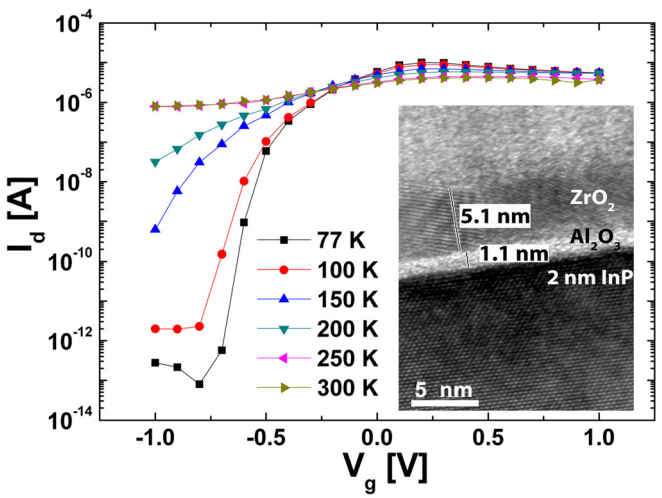

FIG. 1. (Color online) Typical transfer characteristics of high-*k*/$In_{0.75}Ga_{0.25}As$ MOSHEMTs for L = 170 μm and W = 20 μm for various temperatures and V_{ds} = 50 mV with a TEM image of the gate stack region shown in the inset.

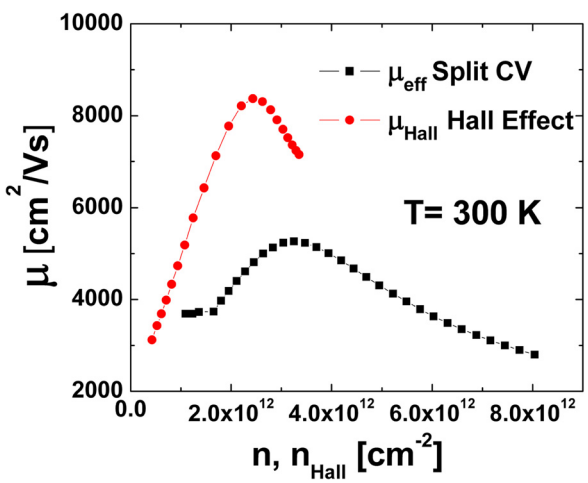

FIG. 2. (Color online) Comparison of μ_{Hall} and μ_{eff} (f = 1 MHz) versus the corresponding carrier density (n, n_{Hall}) at room temperature for a high-*k*/$In_{0.75}Ga_{0.25}As$ MOSHEMT with 2 nm InP top barrier layer, L = 170 μm, W = 20 μm, $V_g = -1$ V to 1 V range, and V_{ds} = 50 mV.

inside each device layer, I_d = drain current, L = device length, W = device width, and V_{ds} = drain source voltage.

The carrier density extracted by these two methods is shown in Fig. 3(a). For the same V_g, the maximum channel carrier density obtained from the Hall Effect measurement is $\sim 3.4 \times 10^{12}\,cm^{-2}$ compared to $8 \times 10^{12}\,cm^{-2}$ obtained using the split CV technique. Earlier, we hypothesized that at higher gate voltages, the channel confinement is lost and that carriers can spill into the low mobility InP barrier layer over the channel region. This suggestion finds support in the n and n_{Hall} dependencies on the gate voltage, Fig. 3(a). A plateau in the n_{Hall}-V_g plot observed at higher gate voltages might be caused by screening of the channel when charges spill over into the barrier layer. These charges may form a parallel channel for carrier transport.

When there are trapped charges (m = 3), an additional term of n_3 is added to Eqs. (1) and (2) with a mobility $\mu_3 = 0$. From inspection of Eqs. (1) and (2), this has no impact on μ_{hall}, due to the product of n_3 and u_3. However, it will reduce μ_{eff} as there is an additional term in the denominator of Eq. (2). The influence of the trapped charges should be detected experimentally as a shift in the electron density versus vs V_g characteristics obtained from the split CV approach when compared to the electron density obtained from the Hall mobility and Eq. (3). A shift ($\sim$0.2 V) is observed experimentally in Fig. 3(a) corresponding to a charge density of $1.23 \times 10^{12}\,cm^{-2}$. This alone is not sufficient to explain the difference in the electron density from split CV ($3.4 \times 10^{12}\,cm^{-2}$) and from the Hall measurements ($8.0 \times 10^{12}\,cm^{-2}$).

Eqs. (1)–(3) and Fig. 3(b) illustrate the n_{Hall} vs. V_g characteristics solved using classical Poisson equation with a constant InP/$In_{0.75}Ga_{0.25}As$ barrier offset = 0.2 eV for three cases of $\mu_2 = \mu_1 = 7000\ cm^2/Vs$ (comparable to single channel), $\mu_2 = 1/4\,\mu_1$ and $\mu_2 = 1/10\,\mu_1$ in bilayer semiconductors.[15] The n_{Hall} characteristics in Fig. 3(a) compared to the simulations in Fig. 3(b) suggest carrier spill over into the InP barrier does occurs in the devices for $V_g > 0$ and that the total measured n_{Hall} is dominated by the high mobility channel with $\mu_1 \gg \mu_2$.

Comparison of electron density and mobility obtained from the gated Hall effect measurements versus split-CV indicates that the split CV method results in significant (by a factor of x2) overestimation of the channel carrier concentration and a corresponding underestimation of the electron mobility. Gated channel devices designed for Hall Effect measurements allow for more confident extraction of the electron density and mobility. It was also confirmed that the real space transfer of charge carriers from the channel into the top barrier takes place at $V_g > 0$ V (Figs. 3(a) and 3(b)). However, even with parallel conduction channels, the average Hall effect mobility is still dominated by the high mobility channel. The spill over may be suppressed by choosing the barrier layers with the higher band offset. These findings should be considered in the design of the III-V quantum well structure and the gate stack.

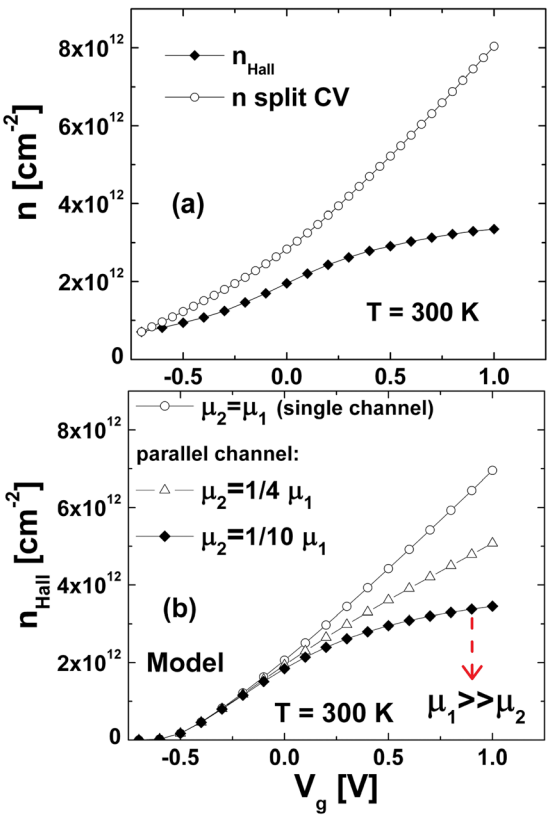

FIG. 3. (a) (Color online) Comparison of Hall channel carrier density (n_{Hall}) and split CV carrier density (n) at room temperature in a high-*k*/$In_{0.75}Ga_{0.25}As$ MOSHEMT with L = 170 μm and W = 20 μm and V_{ds} = 50 mV (b) Simulated n_{Hall} with a constant InP/$In_{0.75}Ga_{0.25}As$ barrier offset = 0.2 eV for three cases of $\mu_2 = \mu_1 = 7000\ cm^2/Vs$ (comparable to single channel), $\mu_2 = 1/4\,\mu_1$ and $\mu_2 = 1/10\,\mu_1$ in bilayer semiconductors (see Ref. 15).

This work is supported by the Irish Research Council for Science, Engineering and Technology (IRCSET)-Marie Curie International Mobility Fellowship in Science, Engineering and Technology, and Science Foundation Ireland under Grant No. 08/US/I1546.

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