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Authors	Dobaczewski, L.;Bernardini, S.;Kruszewski, P.;Hurley, Paul K.;Markevich, V. P.;Hawkins, I. D.;Peaker, A. R.
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Energy state distributions of the P_b centers at the (100), (110), and (111) Si/SiO_2 interfaces investigated by Laplace deep level transient spectroscopy

L. Dobaczewski,[1,2,a)] S. Bernardini,[2] P. Kruszewski,[1] P. K. Hurley,[3] V. P. Markevich,[2] I. D. Hawkins,[2] and A. R. Peaker[2]

[1]*Institute of Physics Polish Academy of Sciences, al. Lotników 32/46, 02-668 Warsaw, Poland*
[2]*Microelectronics and Nanostructure Group, School of Electrical and Electronic Engineering, University of Manchester, M60 1QD Manchester, United Kingdom*
[3]*Tyndall National Institute, University College Cork, Lee Maltings, Prospect Row, Cork, Ireland*

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The energy distribution of the P_b centers at the Si/SiO_2 interface has been determined using isothermal laplace deep level transient spectroscopy. For the (111) and (110) interface orientations, the distributions are similar and centered at 0.38 eV below the silicon conduction band. This is consistent with only P_{b0} states being present. For the (100) orientation, two types of the interface states are observed: one similar to the (111) and (110) orientations while the other has a negative-U character in which the emission rate versus surface potential dependence is qualitatively different from that observed for P_{b0} and is presumed to be P_{b1}. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2939001]

It is known that the quality of the Si/SiO_2 interface plays a key role in the metal-oxide-silicon field effect transistor performance. Over 30 years ago, it was observed that the thermal growth of an oxide on a silicon surface is accompanied by the appearance of interface defects, referred to as P_b centers, which are an inherent consequence of the lattice mismatching between silicon and the oxide.[1] electron-spin resonance (ESR) measurements revealed the existence of two types of centers, termed P_{b0} and P_{b1}, only slightly differing in the structure.[2] The P_{b0} state has been identified as related to a ⟨111⟩ oriented dangling bond (DB) of the interfacial silicon atom bonded to three other silicon atoms,[1] while in the case of P_{b1}, the DB orientation is ⟨211⟩, as a result of the oxygen atom(s) bridging the second nearest bond(s) to the silicon DB.[3–5] Only P_{b0} states were observed at the (111) and (110) oriented Si/SiO_2 interfaces while both types of P_b's were observed at (100) Si/SiO_2.[2]

The DB represents one specific case among the various point defects observed in bulk silicon[6] and these defects have well-defined electronic levels in the band gap. At disordered interfaces, the lattice mismatching results in DB forming a rather broad distribution of energy states. The experimental methods, which have adequate detectivity of the P_b states, do not perform well in revealing the energy distribution of these states.[7,8] For example, deep level transient spectroscopic (DLTS) measurements are performed during sample temperature ramping and this fact makes the results fundamentally ambiguous. The interface states, on which a DLTS measurement is performed, contribute substantially to the background sample capacitance. This causes a data normalization problem[9] and makes the energy distribution evaluation unreliable.

In this study, we have determined precisely the energy distributions of the P_b centers at the Si/SiO_2 interfaces with the crystallographic orientations (100), (110), and (111). This is possible due to the experimental procedure which is based on current transient measurements using isothermal Laplace DLTS.[10,11] Our results contribute to the debate on the electrical activities of the P_b defect family, in general.[12] MOS capacitors used for this study have been made on the n-type (100), (110), and (111) silicon materials with a carrier concentration of $\sim 10^{15}$ cm^{-3}. Full details of the sample preparation procedures and preliminary characterization were given elsewhere.[13]

High-frequency 1 MHz capacitance-voltage (CV) measurements [Fig. 1(a)] showed a shift of the plot toward higher voltages as the measurement temperature decreases. This is typical of a MOS device containing Si/SiO_2 interface states.[14] This is due to these states capturing and emitting carriers sufficiently fast at higher temperatures to contribute to the capacitance. However, when the temperature de-

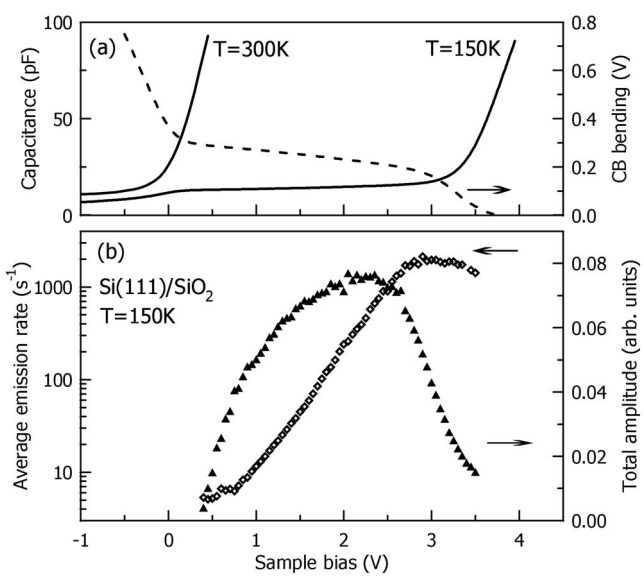

FIG. 1. (a) The low-voltage parts of the 1 MHz CV curves observed for the $Si(111)/SiO_2$ MOS device (solid lines, the accumulation capacitance is ~180 pF) and the voltage-CB bending curve (dashed line) calculated according to Ref. 14 for the CV curve measured at 150 K. (b) The total amplitudes (triangles) and average emission rates (squares) measured for the $Si(111)/SiO_2$ MOS sample at 150 K with the current Laplace DLTS.

a)Electronic mail: dobacz@ifpan.edu.pl.

creases, these capture and emission processes cannot follow the 1 MHz test signal and the charge trapped at the interface states becomes static within the time scale of the measurement frequency. At lower temperatures, this static charge trapped at the interface screens the external voltage and more voltage must be applied to overcome the electric field produced by this charge in order to reach the charge accumulation regime. The *CV* curves shown in Fig. 1(a) illustrate this effect where a steep increase in capacitance measured at 300 K starts at around 0 V while at 150 K, it is around 3.5 V. The *CV* curve measured at 150 K has another characteristic feature. Namely, while below 0.2 V, the capacitance increases characteristically for a MOS capacitor in the depletion regime, between 0.4 and 3.2 V, it changes only slightly. This effect is well known.[15,16] During the *CV* measurement, when the Fermi level approaches the interface defect level, the defects start to trap carriers charging the interface and pinning the Fermi level at the crossing point. When all defects are filled, then more carriers can reach the interface forming the accumulation layer. The magnitude of the Fermi level pinning effect seen as a plateau on the *CV* curve depends on the carrier exchange rate between the defects and the semiconductor conduction band (CB), i.e., on the sample temperature. In the extreme case of very low temperatures, the charge exchange between the defect level and the CB is so slow that the trapped charge affects the MOS device similarly as a fixed charge in the oxide. Conventional DLTS measurements are realized with the sample temperature ramping and assuming that the measured defects make only a small contribution to the sample total capacitance. Although this may be true in some situations, it is not the general case and it is definitely not correct for these measurements realized for interface defects in these unpassivated MOS capacitors. Moreover, a proper interpretation of conventional DLTS data also needs a good knowledge of the Fermi level position at the interface during the measurements. The varying Fermi level pinning effect with temperature makes conventional DLTS data very difficult to interpret in a precise way.

Our approach is based on the analysis of the DLTS signals measured at a constant temperature. Instead of a capacitance meter commonly used for the transient measurements, we have observed current transients. This approach has two main advantages: first, the problem of the capacitance transient normalization is avoided, second, in capacitance meters, an ac test signal is superimposed on the dc bias, which for the 100 mV rms test level typically used at 1 MHz introduces an uncertainty of $2\sqrt{2}\times 100$ mV (283 mV) and, consequently, limits the resolution of the observed energy distributions. At a fixed voltage bias (V_r), if the interface states are in a thermodynamic equilibrium with the CB, the states below the Fermi level crossing point energy at the interface are occupied with carriers. In the experiments, small filling pulses with a voltage of $V_p = V_r + 50$ mV are used to disturb this steady-state conditions in order to observe the thermal emission process as a current transient. The emission rates of these transients are analyzed using the same procedures as in the high-resolution Laplace DLTS measurements.[10,11] For each current transient, an average emission rate and a total amplitude from the Laplace spectrum have been calculated and used for further analysis.

Figure 1(b) shows the average emission rates and the total amplitudes measured at 150 K and for the sample biases corresponding to the plateau observed on the *CV* curve

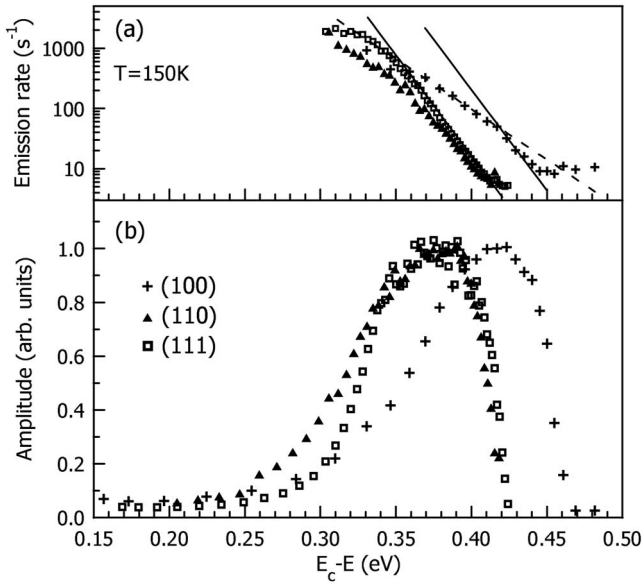

FIG. 2. (a) The emission rates and (b) normalized DLTS signal amplitudes observed for the P_b states at the Si/SiO_2 interface with different orientations. The absolute values of the amplitudes are 12, 6.0, and 2.8 $\times 10^{12}$ eV^{-1} cm^{-2}, for the (111), (110), and (100) samples, respectively. The energy on the horizontal axis is the difference between the bottom of the CB and the Fermi level cross-point at the interface. The solid lines slope in (a) is $1/(k_B T)$ (T=150 K), while for the dashed line is $1/(2k_B T)$.

taken at the same temperature. For biases between 0.8 and 2.8 V, the average emission rate increases by almost three orders of magnitude while the amplitude passes through a maximum. The emission rates change with temperature in a way characteristic for a thermal emission process. The signals described here are not observed in reference samples where the P_b centers have been eliminated, for example, by a forming gas ambient anneal. In the reference samples irrespective of orientation, no shift of the *CV* curve toward higher voltages, and no plateau, at low temperatures have been seen.

Based on the *CV* curve measured at 150 K [Fig. 1(a)] the voltage scale has been converted to the surface potential (the Fermi level cross point) at the Si/SiO_2 interface according to the procedure described by Nicollian and Brews.[14] This procedure enabled the Si CB bending depicted in Fig. 1(a) (the dashed line) to be calculated. For the voltage scale recalculation, the CB bending values have to be shifted additionally by the value of the Fermi level position in silicon at the measurement temperature and for the carrier concentration. Figure 2 shows the average emission rates [Fig. 2(a)] and the normalized distributions of the P_b centers [Fig. 2(b)] measured for three interface orientations.

A fundamental question arises regarding the physical character of the emission process observed in the Laplace DLTS experiments performed on the interface states. The solid lines in Fig. 2(a) are $A\exp[-(E_c - E)/k_B T]$ (T=150 K) functions drawn for some values of the A constant to fit the data sets. For the (111) sample, the emission rates almost perfectly follow this function, which clearly indicates that the carriers thermally emitted from the interface come directly from the Fermi level at the interface. Shifting the Fermi level results in *exactly* the same change of energy which activates the emission process. It means that in order to leave the interface, the carriers need to overcome an energy equal to the difference between the bottom of the silicon

CB and the Fermi level. For the (100) sample, the emission rate changes with energy in a different way. For larger energies, the emission rates have the same slope as the one for the (111) sample; however, for energies less than around 0.42 eV, the slope is exactly half of the one for energies above this value [the dashed line in Fig. 2(a)]. Thus, in this energy range, the emission process leading to the equilibrium recovery is activated by half of the energy distance between the Fermi level crossing point and the bottom of the CB and, consequently, in a single emission process, two carriers are released. This is a characteristic of a defect having a negative-U character.[17] For the (110) sample the data slope is predominately similar to the one observed for the (111) sample with some deviation towards a half of its value at lower energies.

The normalized amplitude distributions [Fig. 2(b)] for the (111) and (110) samples are almost identical and are centered at 0.38 eV with tails toward smaller energies (closer to the CB). The distribution for the (100) sample is shifted toward larger energies by 0.05 eV maintaining a similar shape. The P_b center peak densities are 12.0, 6.0, and 2.8 $\times 10^{12}$ eV^{-1} cm^{-2}, for the (111), (110), and (100) samples, respectively. The ratios between the peak densities for different interface orientations are almost identical to the ones derived from the ESR measurements [3:2:1 (Ref. 18)].

For comparison, a series of conventional capacitance DLTS measurements (1 MHz 100 mV test signal) have been performed on the same samples using biases between 0 and 1 V and a small filling pulse of a 0.05 V amplitude. For each sample bias, the Arrhenius plot gave an emission activation energy of 0.3 eV with the pre-exponential parameter increasing with the sample bias. This value of 0.3 eV is quoted in a large number of papers where conventional DLTS measurements on the P_b centers are reported. The difference between the results of the isothermal Laplace DLTS and the conventional DLTS with the temperature ramp is a systematic error committed in a latter case where the capacitance base line shift and the Fermi level pinning effect are not taken into account.

The energy state distributions observed for the P_b centers formed on the Si/SiO_2 interfaces with different interface configurations do not enable the contributions coming from the P_{b0} and P_{b1} states to be distinguished directly; however, some conclusions can be drawn indirectly. For the (111) interface orientation, the ESR data show that only P_{b0} states are observed, thus, almost identical energy distributions observed in the Laplace DLTS measurements for the (111) and (110) samples would also mean that in the (110) sample, there is no P_{b1}. On the other hand, a clear double slope observed on the emission versus energy graph indicates that on the (110) interface, there could be some P_{b1} present but with a concentration so low that it is not seen on the density of state distribution shape and position. For the (100) interface orientation, the energy state distribution is shifted and the emission rate versus energy dependence slope has clearly two regions, however, the relative participation of both of them in the amplitude distribution cannot be evaluated. The states contributing to the energy state distribution observed for the (100) sample orientation have different identities. The one seen at higher energies seems to be a single-electron state similar to the one observed in the (111) sample, the other one contributing to the energy distribution at lower energies is a state which emits two electrons in the process of reaching the thermal equilibrium.

The energy states of the P_b centers observed in this study charge negatively demonstrating an acceptor two electron, presumably diamagnetic character, and as such cannot be the ones so widely reported in the ESR studies but are seen in the CV and DLTS measurements. When the P_{b0} state observed in the (111) sample changes charge state, it releases a single electron thus, in the lower part of the Si band gap, a donor state should exist. This state is seen in the lower half of the band gap for the p-type silicon samples. The P_{b1} state observed in the (100) sample in a single emission act releases two electrons and, thus, according to the negative-U character, should have no single-electron donor state in thermal equilibrium. This could explain why the distribution of the interface density of state across the energy gap for the $(100)Si/SiO_2$ system is asymmetric in the lower half of the band gap while it is symmetric in the upper half.[13,19] It could also explain why for the (111) and (110) silicon, the density of states peaks in the lower and upper gaps have almost the same magnitudes while for (100), they do not.[13] On the other hand, it is known that under nonequilibrium conditions, some occupancies of the single-electron state of the negative-U defect can be observed.[20] As a result, depending on the experimental conditions, some disturbances of equilibrium could explain the controversy as to whether the P_{b1} center has an energy level in the Si band gap.[12]

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