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Observation of peripheral charge induced low frequency capacitance-voltage behaviour in metal-oxide-semiconductor capacitors on Si and GaAs substrates

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We report on experimental observations of room temperature low frequency capacitance-voltage (CV) behaviour in metal oxide semiconductor (MOS) capacitors incorporating high dielectric constant (high-*k*) gate oxides, measured at ac signal frequencies (2 kHz to 1 MHz), where a low frequency response is not typically expected for Si or GaAs MOS devices. An analysis of the inversion regions of the CV characteristics as a function of area and ac signal frequency for both *n* and *p* doped Si and GaAs substrates indicates that the source of the low frequency CV response is an inversion of the semiconductor/high-*k* interface in the peripheral regions outside the area defined by the metal gate electrode, which is caused by charge in the high-*k* oxide and/or residual charge on the high-*k* oxide surface. This effect is reported for MOS capacitors incorporating either MgO or $GdSiO_x$ as the high-*k* layers on Si and also for Al_2O_3 layers on GaAs(111B). In the case of NiSi/MgO/Si structures, a low frequency CV response is observed on the *p*-type devices, but is absent in the *n*-type devices, consistent with positive charge ($>8 \times 10^{10}$ cm^{-2}) on the MgO oxide surface. In the case of the TiN/$GdSiO_x$/Si structures, the peripheral inversion effect is observed for *n*-type devices, in this case confirmed by the absence of such effects on the *p*-type devices. Finally, for the case of Au/Ni/Al_2O_3/GaAs(111B) structures, a low-frequency CV response is observed for *n*-type devices only, indicating that negative charge ($>3 \times 10^{12}$ cm^{-2}) on the surface or in the bulk of the oxide is responsible for the peripheral inversion effect. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4729331]

INTRODUCTION

During the development of high-*k* processes on silicon or other semiconductor surfaces, it is typical to have a metal gate patterned on the high-*k* oxide surface with no additional passivation, leaving the oxide regions outside the gate area exposed to ambient conditions as well as processing steps such as reactive ion etching, rapid thermal processing, and forming gas annealing. These processing steps, which are widely employed during fabrication of metal-oxide-semiconductor (MOS) capacitors and MOS field-effect transistors (MOSFETs), have the potential to induce charge within the oxide or leave residual charge on oxide surfaces, in particular where the oxide is exposed during such a processing step. If this oxide charge results in depletion of the semiconductor surface and the density of the residual charge is higher than the semiconductor charge associated with the maximum depletion width ($\sim 8 \times 10^{10}$ cm^{-2} for 1×10^{15} cm^{-3} Si substrate doping concentration), then peripheral inversion will be present outside the area defined by the gate electrode.

It is therefore necessary to be aware of the potential effect of this phenomenon in order to avoid incorrect analysis of device behaviour, particularly with regard to MOSFETs, where multiple processing steps are used and there is the possibility for residual charge from processing to affect subsequent electrical characterization of the devices, e.g., the charge could contribute to an artificially high off-state leakage current.[1] In the case of MOS capacitors, what appears to be low frequency inversion-like behaviour due to generation and recombination of minority carriers in the depletion region within the area defined by the gate electrode may in fact be directly attributable to this peripheral inversion charge, which can provide a source of minority carriers. By performing simple capacitance-voltage characterization at multiple ac signal frequencies in conjunction with measuring devices of different areas, over both *n*-type and *p*-type semiconductor substrates, it is possible to establish conclusively if the low frequency inversion-like behaviour is due to peripheral inversion effects which may have arisen during device fabrication, or if it is due to generation and recombination of minority carriers in the semiconductor within the region defined by the gate electrode. In this work, such an approach is presented where peripheral charge induced low frequency CV responses have been observed for the simple

case of MOS capacitors incorporating either MgO or $GdSiO_x$ dielectric layers on silicon. MgO (Refs. 2–7) or $GdSiO_x$ (Refs. 8–12) thin films are of interest as high-*k* oxides on silicon. Experimental results are also presented for Al_2O_3 layers on GaAs, which is of relevance to the development of III-V MOSFETs.

EXPERIMENTAL

20 nm thick MgO films were deposited by electron beam evaporation from 99.9% MgO pellets at a rate of 0.2 Å/s at 180 °C, on *n*-type and *p*-type Si wafers ($1 \times 10^{15}/cm^3$). MOS structures were formed using a fully silicided (FUSI)[13] gate process where the MgO was capped with 100 nm of amorphous silicon in the same deposition system as that used for the MgO deposition, in order to prevent ambient exposure of the film. Nickel was subsequently deposited *ex-situ* by e-beam evaporation (80 nm) through a patterned resist mask and subsequent lift-off process, to define square capacitors of various areas. Rapid thermal annealing (RTA) was then performed in a one step process at 500 °C for 30 s in N_2 to form the NiSi gates. Following the removal of excess Ni using H_2O:H_2SO_4 (1:3), the silicon outside the square capacitor area was removed by reactive ion etching using sulfur hexafluoride (SF_6). From the capacitance measured in accumulation, the permittivity of these MgO films was calculated as ~8.1.[13]

For the second sample set examined, $GdSiO_x$ layers were prepared by the intermixing of thermally grown silicon oxide (SiO_2) interlayers and evaporated gadolinium oxide (Gd_2O_3).[15,16] Si surfaces were prepared by RCA cleaning followed by dry thermal oxidation to form SiO_2 interlayers ~4 nm thick. 10 nm thick Gd_2O_3 films were then deposited by electron beam evaporation from granular Gd_2O_3 at a deposition rate of 0.01 nm/s and molecular nitrogen was present during deposition. The samples then underwent RTA for 1 s at 900 °C to form $GdSiO_x$ from the initial Gd_2O_3/SiO_2 bilayer.[15,16] TiN electrodes (50 nm thick) were deposited by reactive sputtering from Ti, and circular capacitors of various areas were defined using a lift-off process. Finally, backside contacts were formed by deposition of Al. A k-value of ~16 is estimated for the $GdSiO_x$ layers.[15,16]

For the third sample set examined, the substrates used were (1) *n*-type GaAs(111B) (Si at $\sim 5 \times 10^{17}\,cm^{-3}$) or (2) ~*p*-type GaAs(111B) (Zn at $\sim 7 \times 10^{17}\,cm^{-3}$). GaAs(111B) surfaces were initially rinsed for 1 min each in acetone, methanol, and isopropanol, prior to immersion in $(NH_4)_2S$ with a concentration of 10% in deionised H_2O (20 min, ~295 K). The Al_2O_3 layers (8 nm) were grown by atomic layer deposition (ALD) at 300 °C (Cambridge NanoTech, Fiji F200LLC), using alternating pulses of TMA ($Al(CH_3)_3$) and H_2O. Samples were loaded into the ALD reactor within ~14 min after removal from the $(NH_4)_2S$ solution. Finally, gate contacts ~160 nm thick were formed by e-beam evaporation of Ni (70nm) and Au (90nm), using a lift-off process.

The capacitance-voltage (CV) and conductance-voltage (GV) measurements were recorded using a Hewlett Packard 4284A LCR meter or Agilent B1500A Semiconductor Device Analyser. The measurements were performed at room temperature on-wafer in a microchamber probe station (Cascade Microtech, model Summit 12971B) in a dry air, dark environment (dew point $\leq$ 203 K). Conventional transmission electron microscopy (TEM) samples were prepared using focused ion beam (FIB) thinning procedures in an FEI 200 Workstation and examined at 200 kV in a JEOL2000FX.[17]

RESULTS AND DISCUSSION

A TEM micrograph for a *p*-type NiSi/MgO/Si device is shown in Figure 1(a). This indicates a MgO thickness of 21.7 nm, close to the nominal value, with good layer uniformity. The TEM also shows the presence of an amorphous interfacial oxide layer (IL) with a thickness of just 1 nm. TEM micrographs for the *n*-type TiN/$GdSiO_x$/Si structure are shown in Figure 1(b). It is evident from the TEM micrograph that as a result of the RTA treatment, there is very good inter-diffusion of the SiO_2 (4 nm) and Gd_2O_3 (10 nm) layers to form $GdSiO_x$, with the thickness of the SiO_2 layer reducing to ~1.6 nm, while the thickness of the Gd based region remains approximately the same at 9.7 nm.

The CV response at room temperature (295 K) with ac signal frequencies from 2 kHz to 1 MHz for the NiSi/MgO/*p*-Si devices is shown in Figures 2(a)–2(c) for capacitor squares with dimensions of 30×30 μm, 60×60 μm, and 90×90 μm, respectively. The multifrequency CV responses for the corresponding *n*-type devices are shown as insets to Figures 2(a)–2(c). First, in analyzing the CV response in Figure 2(a) for the smallest device area (30×30 μm), what appears to be a low frequency response is observed in the gate bias range of ~−0.5 V to 4 V, at the lowest measured frequency of 2 kHz. However, the capacitance in this bias range still remains high for the 1 MHz curve, which is not expected for typical minority carrier lifetimes in silicon.[18,19] In the case of a low frequency CV response due to the generation and recombination of minority carriers in the depletion region of the silicon, low frequency CV characteristics are not typically recorded at frequencies above 100 Hz.[18,19]

A possible explanation for this effect is shown in Figure 3, which shows plan and cross sectional views of MOS capacitors with different gate areas, where charge exists on the oxide surface, or within the oxide, in the region outside the area defined by the gate electrode. This could be present due to processing steps such as reactive ion etching (RIE),

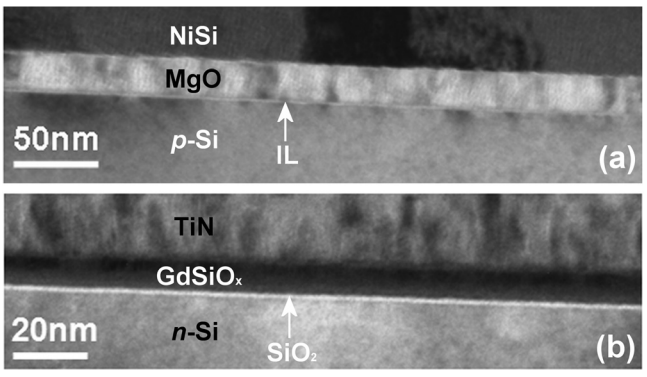

FIG. 1. Cross-sectional TEM micrographs of (a) NiSi/MgO/*p*-Si and (b) TiN/$GdSiO_x$/*n*-Si, device structures.

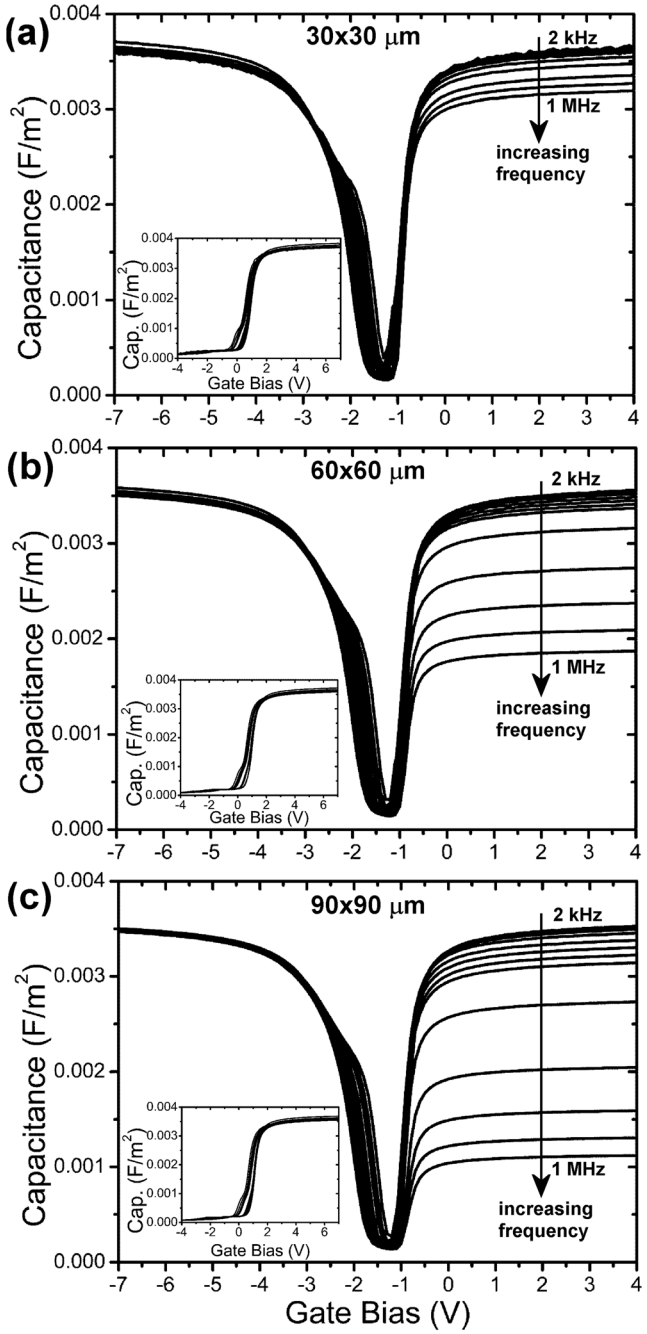

FIG. 2. The CV multi-frequency response at room temperature (295 K) of the NiSi/MgO/*p*-Si devices for capacitor squares with dimensions of (a) 30×30 μm, (b) 60×60 μm, and (c) 90×90 μm, respectively. The multi-frequency CV responses for the corresponding *n*-type devices are shown as insets. The ac signal frequencies range from 2 kHz to 1 MHz in all cases.

forming gas annealing (FGA), or RTA. If this oxide surface charge is of the same type as the semiconductor doping, it will induce a corresponding charge of the opposite sign in the semiconductor at the oxide/semiconductor interface and will give rise to an inversion region in the peripheral area outside the area defined by the gate oxide (termed "peripheral inversion"), if the oxide charge density [cm^{-2}] is larger than the product of the doping concentration in the semiconductor and the maximum depletion width. The resulting peripheral inversion layer is a source of minority carriers, which can be supplied to the area under the gate

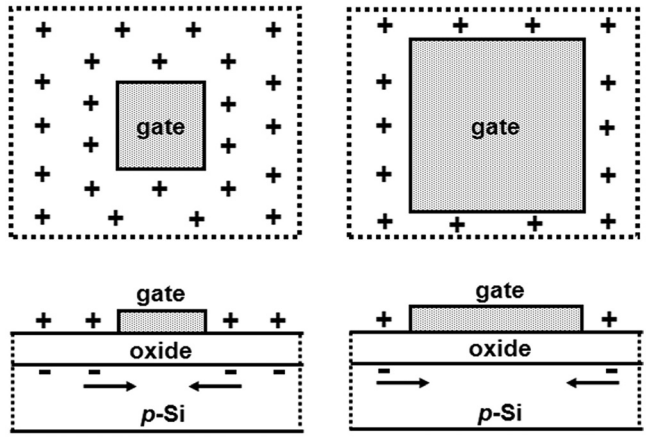

FIG. 3. Schematic to illustrate a possible mechanism for peripheral inversion effects for *p*-type MOS devices. A plan view looking down on the gate area is shown for a smaller device (on the left) and a device where the perimeter-length is doubled (on the right). Beneath these, corresponding cross-sectional schematics illustrate the MOS device structure in each case.

electrode once the oxide/semiconductor interface under the gate electrode is inverted by the applied gate voltage.

Capacitance-voltage measurements performed at multiple frequencies and on varying capacitor areas on both *n*-type and *p*-type devices can be used to determine if such peripheral inversion is responsible for the low frequency behaviour, as the low frequency behaviour provided through peripheral inversion would exhibit specific CV behaviour in the following ways:

(1) For a given device area, the inversion response will reduce with increasing ac measurement frequency.
(2) At a given ac signal frequency, the inversion response will be reduced as the device area increases, due to the increasing diffusion distance from the periphery to the centre of the gate electrode.
(3) The low frequency inversion like behaviour will be observed for either *n* or *p* doped semiconductor substrates, and not for both, as a given oxide charge will only invert the oxide/semiconductor surface for one dopant type.

While the observations described in (1) will be observed for minority carriers supplied either from under the gate area (by generation/recombination or diffusion from the quasi-neutral bulk), or via a peripheral inversion charge, the observations described in (2) and (3) are not consistent with minority carrier supply from the depletion region under the gate electrode. The supply of minority carriers by generation/recombination in the depletion region or by diffusion from the quasi-neutral bulk should not exhibit a dependence on the electrode area and should also be present for both *n* and *p* type semiconductor substrates.

The CV responses in Figures 2(b) and 2(c) are consistent with the presence of a peripheral inversion region, as the low frequency inversion-like behaviour in the region −0.5 V to 4 V is observed to decrease as the area is increased for the 60×60 μm device in Figure 2(b) and the 90×90 μm device in Figure 2(c). We can determine that the charge on the surface or in the bulk of the oxide is positive in this case, which

induces negative charge in the substrate, leading to an inversion response for the *p*-type devices. The results for the same NiSi/MgO gate stack over *n* type Si are shown as insets in Figures 2(a)–2(c). For the *n* type silicon, no inversion behavior is observed, as the positive oxide charge will result in accumulation of the semiconductor surface in this case. This is again consistent with the source of the minority carriers originating from the periphery of the device. This charge was possibly introduced during the reactive ion etch step of the FUSI processing to define the MOS capacitor areas. This etch was used to remove excess Si from outside the MOS capacitor device area, and appears to have left positively charged ions on the surface of the remaining oxide, and/or induced positive charge in the oxide outside the gate area.

The CV response at room temperature (295 K) for NiSi/MgO/*p*-Si devices with varying capacitor dimensions from 30×30 μm to 100×100 μm, is shown in Figures 4(a)–4(c), for fixed ac signal measurement frequencies of 10 kHz, 100 kHz, and 1 MHz, respectively. The corresponding CV responses for *n*-type Si devices are plotted as insets. For the *p*-type devices at low frequency (10 kHz) in Figure 4(a), the peripheral inversion charge has time to respond to the ac signal and contribute to the measured capacitance, even for the largest device area (100×100 μm). However at 100 kHz in Figure 4(b), there is a more rapid drop-off in the peripheral inversion response as the device area increases. This is more pronounced again for the 1 MHz curves plotted in Figure 4(c). It is noted that for the *n*-type devices plotted in the insets to Figures 4(a)–4(c), no low frequency CV behaviour is observed for any ac signal frequency from 2 kHz to 1 MHz for the three device areas.

The CV response as a function of temperature for these devices (ac signal frequency 600 kHz, capacitor dimension 100×100 μm) is plotted in Figure 5, with the corresponding conductance plotted as an inset. It is clear that there is little variation in the CV and GV response at positive gate bias over this wide temperature range, $-50\,^{\circ}$C to $140\,^{\circ}$C. This weak temperature dependence of the CV and GV is further evidence that the observed CV response is due to inversion charge already in place on the periphery of the device. A true minority carrier response due to generation-recombination, or diffusion from the quasi-neutral bulk of the silicon, would exhibit a more significant temperature dependence, as observed by Nicollian and Brews in their analysis of a SiO_2/Si MOS device.[18] In addition, a true minority carrier response would exhibit a change in activation energy (E_A) from half the Si bandgap, $E_G/2$ (0.56 eV) for a generation-recombination regime, to an E_A equal to the Si bandgap, E_G (1.12 eV), at higher temperature for a diffusion regime.[18] An Arrhenius analysis of the inversion conductance (G_I)[18] versus temperature, using the data presented in Figure 5 for these MgO samples, yields an E_A of $\sim$0.14 eV which corresponds to neither regime, and is further evidence that a different mechanism, in this case peripheral inversion, is responsible for the observed inversion response.

While not significant in relation to the peripheral inversion effect which is under investigation in this study, it is also apparent that there is an interface state defect related response observed in the CV characteristics for these *n*-type and *p*-type Si samples with a MgO dielectric layer. It is clearly visible as a frequency dependent distortion in the *p*-type multi-frequency CV responses plotted in Figures 2(a)–2(c), at a gate bias in the range of ~ -1.5 V to -2.5 V, and also for the case of the *n*-type devices in the gate bias range of ~ -0.5 V to 0.5 V in the multi-frequency CVs plotted as insets to Figures 2(a)–2(c), although it's effect on the CV is reduced compared to the *p*-type case. An estimation of the interface state densities (D_{it}) was performed using an approximation to the conductance method.[18] This yields a

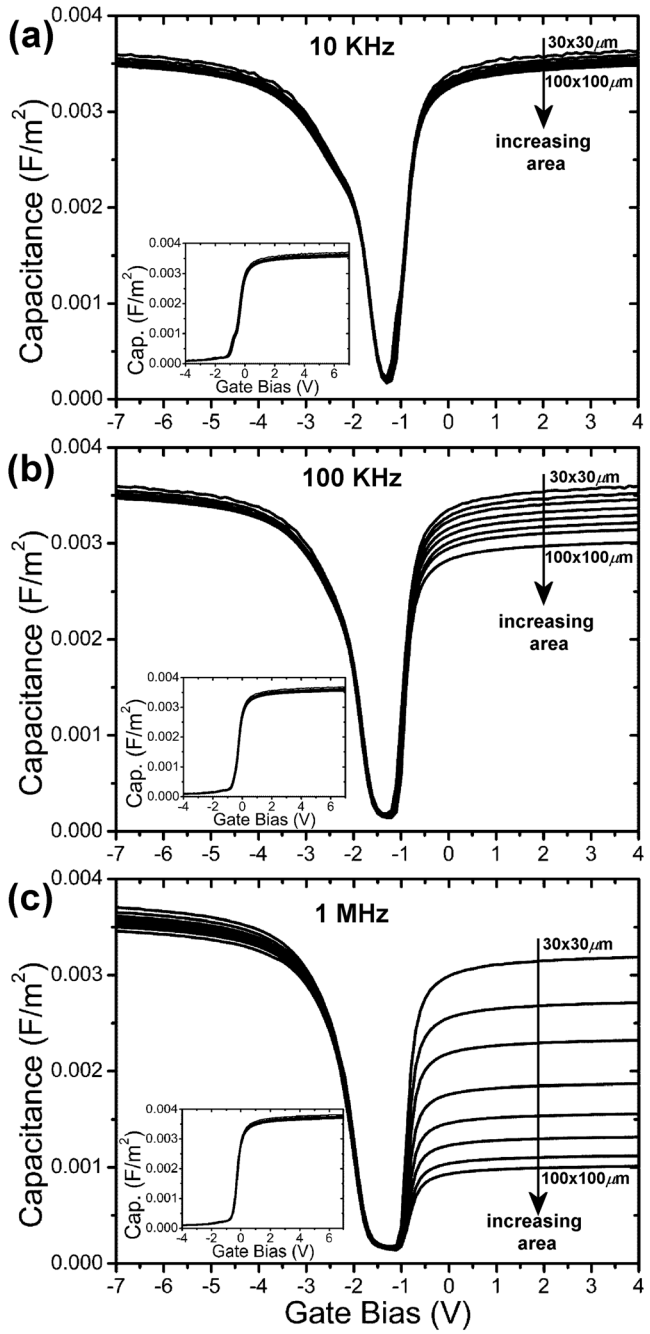

FIG. 4. The CV response at room temperature (295 K) for NiSi/MgO/*p*-Si MOS devices with capacitor squares having varying dimensions from 30×30 μm to 100×100 μm is shown for fixed ac signal measurement frequencies of (a) 10kHz, (b) 100 kHz, and (c) 1 MHz, respectively. The corresponding *n*-type Si device CV responses are plotted as insets. The square MOS capacitors have side lengths of 30, 40, 50, 60, 70, 80, 90, 100 μm.

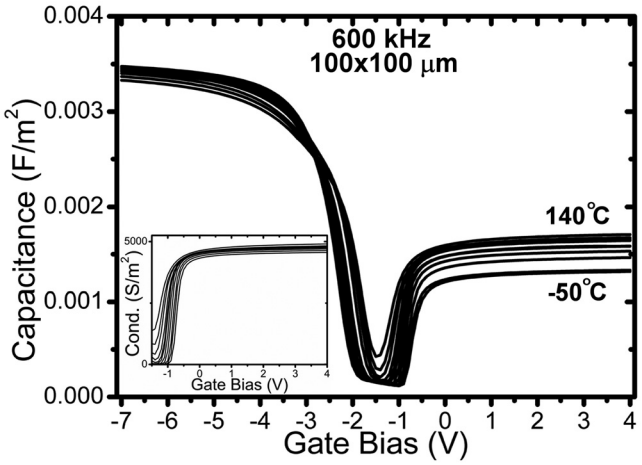

FIG. 5. The CV response as a function of temperature (ac signal frequency 600 kHz, capacitor dimension 100×100 μm), for a *p*-type NiSi/MgO/Si device, with the corresponding conductance plotted as an inset. It is clear that there is little variation in the CV and GV response at positive gate bias over this wide temperature range, $-50\,^{\circ}$C to $140\,^{\circ}$C.

D_{it} distribution across the Si bandgap (not shown), with peak D_{it} values of 1.6×10^{12} cm^{-2} eV^{-1} at $\sim E_v + 0.38$ eV and 6×10^{11} cm^{-2} eV^{-1} at $\sim E_v + 0.8$ eV. The peak energy positions are consistent with those expected for P_b dangling bond defects, as reported extensively in the literature.[14,20–27]

It is important to state that the peripheral inversion effect is not unique to the MgO/Si system or the FUSI processing used for the MgO sample set. To illustrate this, results are now presented showing evidence of peripheral inversion effects for a different oxide/Si MOS system, and where very different processing steps were used in the device fabrication, as described earlier in the experimental section. The CV response at room temperature (295 K) with ac signal frequencies from 2 kHz to 100 kHz for the TiN/$GdSiO_x$/*n*-Si devices is shown in Figures 6(a)–6(c), for circular capacitors with diameters of 100 μm, 200 μm, and 400 μm, respectively. The multi-frequency CV response for the corresponding *p*-type devices is shown as insets to Figures 6(a)–6(c). In analyzing the CV responses in Figures 6(a)–6(c) for the *n*-type devices, it appears that the low frequency CV response is also due to peripheral inversion charge. However, in this case, the peripheral charge on the surface or in the bulk of the oxide is negative, inducing positive charge in the substrate, resulting in a low frequency CV response for *n*-type devices. It is possible that the 900 °C RTA step performed on the exposed $GdSiO_x$ surface resulted in residual negative charge due to moisture reactions on the $GdSiO_x$ surface. Similar behaviour has been reported previously on *n*-type Si with a HfO_2 dielectric which was exposed during MOS device processing,[20,28] and in the case of the study by O'Sullivan *et al.*, the corresponding *p*-type devices did not exhibit any inversion behaviour.[20] Significantly, the inversion response on the TiN/$GdSiO_x$/*n*-Si devices in the present work is gate area dependent, as is expected in the presence of peripheral charge. As the gate area is increased from the 200 μm diameter device in Figure 6(b) to the 400 μm diameter device in Figure 6(c), the magnitude of the capacitance in the inversion region for a given ac signal frequency is

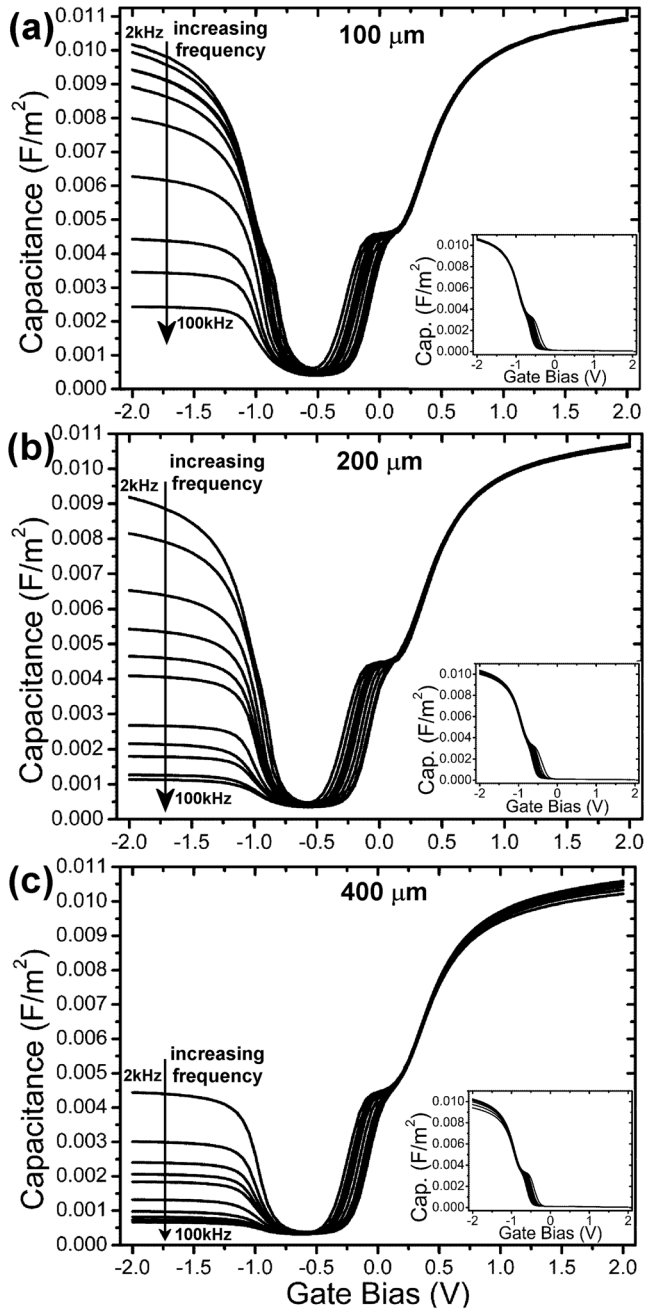

FIG. 6. The CV multi-frequency response at room temperature (295 K) of the TiN/$GdSiO_x$/*n*-Si devices for circular capacitors with diameters of (a) 100×100 μm, (b) 200×200 μm, and (c) 400×400 μm, respectively. The multi-frequency CV responses for the corresponding *p*-type devices are shown as insets. The ac signal frequencies range from 2 kHz to 100 kHz in all cases.

reduced, and the capacitance for gate bias in the range -0.5 V to -2 V drops off at all frequencies. (It should be noted that the smallest device area available for the $GdSiO_x$/Si set was 100 μm in diameter compared to a smallest device of 30×30 μm which was available for the MgO/Si devices.) For the *p*-type devices plotted as insets to Figures 6(a)–6(c), the negative charge on the oxide surface, or within the oxide, results in accumulation of the surface in the region outside the gate electrode, and hence no source of minority carrier is available from the periphery of the device and consequently no low frequency behaviour is recorded.

The CV response at room temperature (295 K) for TiN/$GdSiO_x$/*n*-Si devices with varying capacitor diameter dimensions from 100 μm to 400 μm, is shown in Figure 7 for a fixed ac signal measurement frequency of 10 kHz. The corresponding *p*-type $GdSiO_x$/Si device CV responses are plotted in the inset. As in the case of the MgO sample set plotted previously in Figure 4, there is a more pronounced drop-off in the inversion response as you increase the device area, providing further confirmation that the low frequency CV response is a consequence of peripheral inversion. It is noted that there is no variation in the CV response as you increase the device area for the individual frequencies for the *p*-type devices in the inset to Figure 7.

As in the case of the NiSi/MgO/Si capacitors, there is an interface state defect related response observed in the CV characteristics for these *n*-type and *p*-type Si samples with $GdSiO_x$ dielectric. In the case of the *n*-type NiSi/$GdSiO_x$/*n*-Si sample, it is clearly visible as a frequency dependent distortion in the multi-frequency CV responses plotted in Figures 6(a)–6(c), at a gate bias in the range of ~−0.5 V to 0 V. For the case of the *p*-type NiSi/$GdSiO_x$/*p*-Si sample, the distortion is seen in the gate bias range of ~−0.25 V to −0.75 V, in the multi-frequency CVs plotted as insets to Figures 6(a)–6(c). An estimation of the interface state densities (D_{it}) was performed using an approximation to the conductance method,[18] resulting in peak D_{it} values of 1.8×10^{12} cm^{-2} eV^{-1} at ~$E_v + 0.37$ eV and 2.6×10^{12} cm^{-2} eV^{-1} at ~$E_v + 0.82$ eV. These density values and the peak energy positions are again consistent with those reported for P_b dangling bond defects[14,20–27] and are expected as the samples did not receive a forming gas anneal. It is important to emphasize that the interface states do not contribute to the inversion response discussed in this paper. Once the oxide/silicon surface is inverted, the interface states do not change occupancy with the ac signal variation on the gate and hence cannot play a role in supplying carriers to the inversion region, as discussed by Nicollian and Brews on page 112 in Ref. 18.

The observation of the low-frequency behaviour resulting from a peripheral inversion region is likely to occur for the relatively low doping concentrations which are typically used during oxide/semiconductor process development. Considering the case of doping concentrations of ~1×10^{15} cm^{-3} which were used for the Si samples in this work, the charge density at the on-set of inversion is 1.3×10^{-8} C/cm^2 (or 8×10^{10} cm^{-2}).[29] Hence, a relatively low charge density on the surface, or within the bulk of the oxide, can result in inversion outside the area defined by the gate electrode. The CV behaviour reported in this work will be less likely to be observed as the doping concentration in the semiconductor increases.

Finally, the results presented so far have demonstrated the presence of the peripheral inversion effect for Si MOS devices fabricated using different processes and employing different gate oxides. It is, however, important to state that this phenomenon is not restricted to Si substrates. To illustrate this, results are now presented showing evidence of peripheral inversion effects for an MOS system on a III-V semiconductor, GaAs. The CV response at room temperature (295 K) for Au/Ni/Al_2O_3/*n*-GaAs(111B) devices with varying capacitor dimensions from 30×30 μm to 90×90 μm is shown in Figure 8 for a fixed ac signal measurement frequency of 200 Hz. The corresponding CV responses for *p*-type GaAs(111B) devices are plotted as the inset to Figure 8. Under normal measurement conditions, it should not be possible to observe a minority carrier response on GaAs. As discussed by Passlack *et al.*,[30] low-intensity light illumination is required to generate sufficient minority carriers to observe inversion in C–V measurements on GaAs, as the GaAs energy gap (1.42 eV) results in a reduction of the thermal generation/recombination rate. In this work, the measurements presented in Figure 8 were obtained at room temperature, on-wafer, in a light-tight probe station in a dry air environment. Most importantly, as the measurements were performed in the dark, this rules out any contribution of generation of minority carriers through light illumination. It

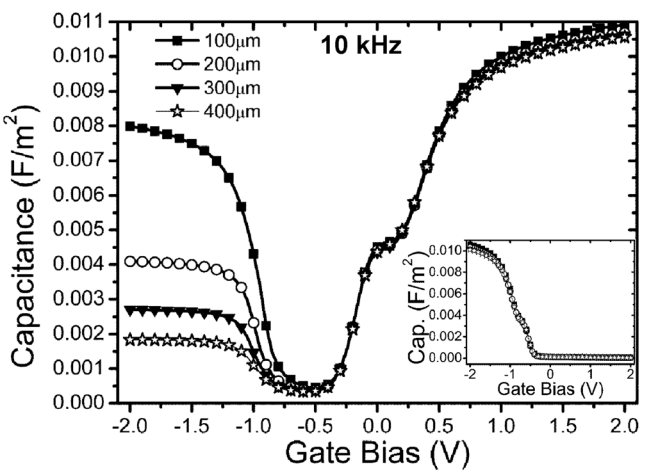

FIG. 7. The CV response at room temperature (295 K) for TiN/$GdSiO_x$/*n*-Si devices with varying capacitor diameters from 100×100 μm to 400×400 μm, is shown for a fixed ac signal measurement frequency of 10 kHz. The corresponding *n*-type Si device CV responses are plotted as an inset. The circular MOS capacitors have diameters of 100, 200, 300, and 400 μm.

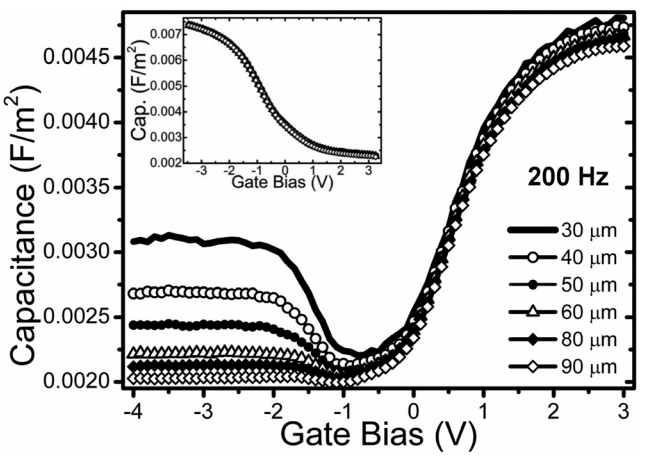

FIG. 8. The CV response at room temperature (295 K) for Au/Ni/Al_2O_3/*n*-GaAs(111B) devices with varying capacitor diameters from 30×30 μm to 90×90 μm, is shown for a fixed ac signal measurement frequency of 200 Hz. The corresponding *p*-type GaAs(111B) device CV responses are plotted as an inset. The square MOS capacitors have side lengths of 30, 40, 50, 60, 80, 90 μm.

is clear that the minority carrier response in Figure 8 is area dependent, and it is only observed on one substrate polarity (see Fig. 8 inset), indicating a peripheral inversion effect is responsible for inducing the minority carrier response. Considering the case of doping concentrations of $\sim 5 \times 10^{17}$ cm^{-3} which were used for the GaAs samples in this work, the charge density at the on-set of inversion is 4.8×10^{-7} C/cm^2 (or 3×10^{12} cm^{-2}).[29] In this case, the low frequency CV response is only observed for *n*-type GaAs devices indicating that the peripheral charge on the surface or in the bulk of the oxide is negative.

CONCLUSION

In conclusion, results were presented which demonstrate the effect of peripheral inversion in MOS capacitors incorporating high-k dielectrics on Si or GaAs. Charge on the oxide surface, or in the oxide, in the region outside the area defined by the gate electrode, can result in inversion of the underlying semiconductor/oxide interface. This provides a source of minority carriers, which can lead to the observation of low frequency CV behaviour. Through the use of identical gate stacks over both *n* and *p* type Si and GaAs substrates, and CV measurements as a function of ac signal frequency and gate area, it is demonstrated that the origin of the low frequency CV response is due to peripheral inversion and not a result of minority carrier generation in the region of the semiconductor under the gate electrode. It has been shown that such behaviour is not unique to a particular device structure or set of processing conditions. This work is also relevant in a wider context to the electrical characterisation of MOSFETs, where multiple processing steps are typically used during device fabrication, and peripheral surface charge could result in misleading electrical characteristics, such as artificially high off-state leakage currents.

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