Silicon Photonic 2.5D Integrated Multi-Chip Module Receiver

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Abstract: We demonstrate the first 2.5D integrated, wavelength division multiplexing, silicon photonic receiver. The multi-chip module utilizes a silicon interposer to integrate the four-channel photonic cascaded microdisk receiver with four electronic transimpedance amplifiers.

1. Introduction

Exponentially increasing bandwidth demands of data centers and high-performance computers [1] presents a need to consider alternative interconnect technologies beyond electrical interconnects. Silicon photonics offers a solution by combining high bandwidth, energy efficiency, low attenuation, parallelization through wavelength division multiplexing (WDM), and the ability to build on the mature CMOS industry [2]. Applying silicon photonics to data center interconnects requires interfacing to electronic systems, as computation originates and terminates in the electrical domain. Additionally, photonics requires driving circuitry to amplify electrical signals for modulators and from photodiodes. The integration of driving electronics with photonics is a crucial design consideration, impacting transceiver bandwidth and energy efficiency. Receiver parasitics reduce swing voltage, introduce noise [3], and lower system bandwidth by influencing the transimpedance amplifier's (TIA) input pole [4].

Various multi-chip module (MCM) integration approaches between electronic integrated circuits (EICs) and photonic integrated circuits (PICs) have been demonstrated: monolithic [5], 2D [6], 3D [4], and 2.5D [7]. Our MCM receiver utilized 2.5D integration, in which the PIC and EIC are flipped side by side on top of an interposer. Our interposer was a thinned silicon substrate to provide a platform for electrical connectivity and through silicon vias (TSVs) to connect the top and back side of the interposer. 2.5D integration presents a compromise between acceptable parasitics and high-density connections with a platform for scalability. The interposer can be fabricated with pad pitches comparable to those of PICs and EICs, allowing for dense microbumps or copper pillars with low parasitics. The interposer supports flip chipping numerous ICs, providing an avenue for scalability. In this paper, we will outline our receiver architecture and report on its performance.

2. Receiver Design

The PIC receiver architecture is composed of four demultiplexing microdisks coupled to a bus waveguide. The microdisks have doped heaters to tune their resonances, which are evenly spaced across the free spectral range. The drop ports of the demuxes are connected to Germanium photodiodes. The photodiode output is connected to the input of a single channel TIA via a pair of stud bumps and a trace on the interposer. Four TIAs are flipped next to the PIC to accommodate the WDM four channels. The output of the TIAs are stud bumped to the interposer and routed to the backside of the interposer through TSVs. Ball grid array (BGA) connections interface the back of the interposer to a PCB, where the signals are routed with microstrip transmission lines to SMAs. The DC signals for the PIC heaters and EIC supply voltages are routed in a similar manner, but terminate in DC connectors on the PCB. The PIC was fabricated through AIM Photonics using the AIM process design kit (PDK). The interposer was fabricated through SUNY CNSE as a custom process. The EICs were commercial bare die Texas Instruments TIAs designed to operate up to 11.3 Gbps. The assembled prototype can be seen in Fig. 1a.

3. Receiver Results

The bandwidths for the four channels can be seen in Fig. 2a. The bandwidth was measured by modulating an external Mach Zehnder modulator with a sine wave source. For each channel, a tunable laser was set to the appropriate microdisk demux's resonance, and the sine wave source was swept from DC to 20 GHz. The output of the TIA was sent to an electrical spectrum analyzer to measure the received tone's power, and were normalized with the bandwidths of the cables and modulator. The measured bandwidths suggest an electrical resonance in the assembled receiver prototype at 7.5 GHz. Additionally, channel 1 is about 20 dB below the other channels, suggesting that there may be a partial connection in one of the stud bumps or BGA bumps. The BERs for channel 3 can be seen in Fig. 2b. The BERs were measured by modulating the external Mach Zehnder with PRBs 2^{15}-1 data

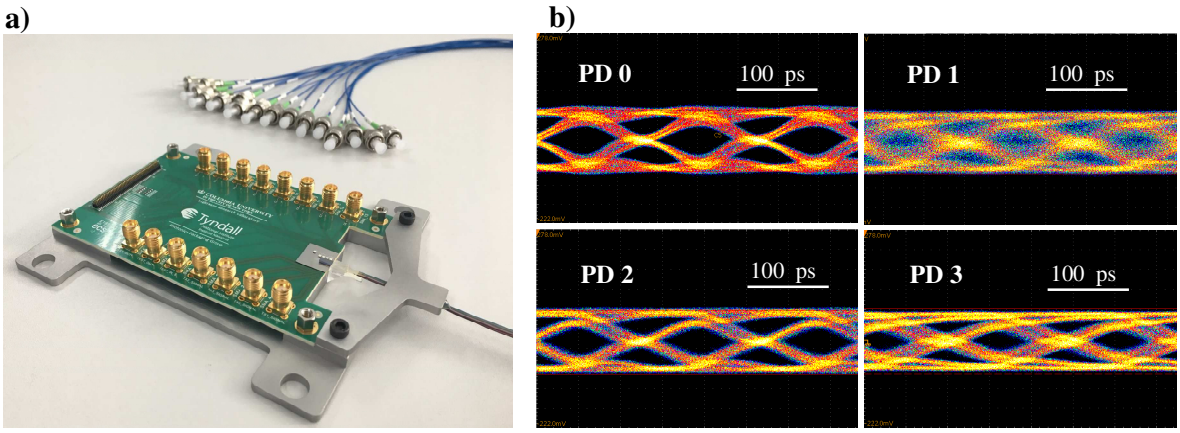

Fig. 1 a) The assembled MCM receiver prototype. b) Eye diagrams for the outputs of the four channels at 7 Gbps

from a pulse pattern generator. The external laser was set to be dropped by the microdisk demux's resonance, and the output of the TIA was sent to a bit error rate tester. The input power into the prototype was varied with an external variable optical attenuator. The optical power into the prototype was measured, and the received power was calculated by subtracting the combined 7.4 dB optical loss from the edge coupler and demux microdisk. Error free performance ($1x10^{-9}$) was achieved at 5 Gbps with -10.5 dBm received power.

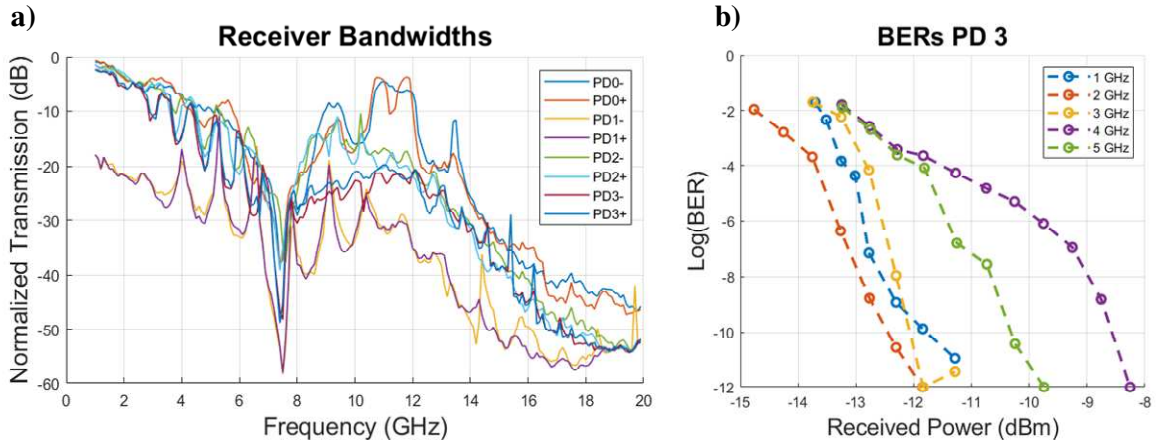

Fig. 2 a) The bandwidths for the both the positive and negative outputs of the four receiver channels. b) The BERs at different data rates for a single channel of the receiver prototype.

4. Conclusions

We demonstrated a multi-chip module silicon photonic receiver, with 2.5D integrated PIC and EICs flipped on top of a thinned silicon interposer. The WDM receiver featured four channels, with microdisks providing the demultiplexing to photodiodes to interface to the single channel bare die TIAs. The receiver design targeted 11.3 Gbps per channel. Error free performance was demonstrated at 5 Gbps with -10.5 dBm received power. This MCM receiver prototype demonstrates a scalable approach for incorporating silicon photonics into datacenters.

5. References

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