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Development of Germanium/Silicon Integration for Near Infrared Detection

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Declaration

This thesis is the candidate's own work and has not been submitted for another degree, either at the University College Cork or elsewhere.

Farzan Gity

Abstract

Silicon (Si) is the base material for electronic technologies and is emerging as a very attractive platform for photonic integrated circuits (PICs). PICs allow optical systems to be made more compact with higher performance than discrete optical components. Applications for PICs are in the area of fibre-optic communication, biomedical devices, photovoltaics and imaging. Germanium (Ge), due to its suitable bandgap for telecommunications and its compatibility with Si technology is preferred over III-V compounds as an integrated on-chip detector at near infrared wavelengths. There are two main approaches for Ge/Si integration: through epitaxial growth and through direct wafer bonding. The lattice mismatch of ~4.2% between Ge and Si is the main problem of the former technique which leads to a high density of dislocations while the bond strength and conductivity of the interface are the main challenges of the latter. Both result in trap states which are expected to play a critical role. Understanding the physics of the interface is a key contribution of this thesis.

This thesis investigates Ge/Si diodes using these two methods. The effects of interface traps on the static and dynamic performance of Ge/Si avalanche photodetectors have been modelled for the first time. The thesis outlines the original process development and characterization of mesa diodes which were fabricated by transferring a ~700 nm thick layer of p-type Ge onto n-type Si using direct wafer bonding and layer exfoliation. The effects of low temperature annealing on the device performance and on the conductivity of the interface have been investigated. It is shown that the diode ideality factor and the series resistance of the device are reduced after annealing. The carrier transport mechanism is shown to be dominated by generation–recombination before annealing and by direct tunnelling in forward bias and band-to-band tunnelling in reverse bias after annealing.

The thesis presents a novel technique to realise photodetectors where one of the substrates is thinned by chemical mechanical polishing (CMP) after bonding the Si-Ge wafers. Based on this technique, Ge/Si detectors with remarkably high responsivities, in excess of 3.5 A/W at 1.55 μm at −2 V, under surface normal illumination have been measured. By performing electrical and optical measurements at various temperatures, the carrier transport through the hetero-interface is analysed by monitoring the Ge band bending from which a detailed band structure of the Ge/Si interface is proposed for the first time. The above unity responsivity of the detectors was explained by light induced potential barrier lowering at the interface. To our knowledge this is the first report of light-gated responsivity for vertically illuminated Ge/Si photodiodes.

The wafer bonding approach followed by layer exfoliation or by CMP is a low temperature wafer scale process. In principle, the technique could be extended to other materials such as Ge on GaAs, or Ge on SOI. The unique results reported here are compatible with surface normal illumination and are capable of being integrated with CMOS electronics and readout units in the form of 2D arrays of detectors. One potential future application is a low-cost Si process-compatible near infrared camera.

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Related patent / publications

Patent: European Patent Application - Number: 1221079.5
Title: Amplified Ge/Si detectors formed by low temperature direct wafer bonding
Inventors: **Farzan Gity**, Brian Corbett, Alan Morrison, and John Hayes

1. **F. Gity**, A. Daly, B. Snyder, F. H. Peters, J. M. Hayes, C. Colinge, A. P. Morrison and B. Corbett, "Ge/Si Heterojunction Photodiodes Fabricated by Low Temperature Wafer Bonding," ***Optics Express***, vol. 21, no. 14, pp. 17309–17314, July **2013**.
2. **F. Gity**, K. Y. Byun, K. -H. Lee, K. Cherkaoui, J. M. Hayes, A. P. Morrison, C. Colinge, and B. Corbett, "Characterization of Germanium/Silicon *p–n* Junction Fabricated by Low Temperature Direct Wafer Bonding and Layer Exfoliation," ***Applied Physics Letters***, vol. 100, Article number: 092102, **2012**.
3. J. M. Hayes, **F. Gity**, B. Corbett, and A. P. Morrison, "Modeling the Effects of Interface Traps on Passive Quenching of a Ge/Si Geiger Mode Avalanche Photodiode," ***Journal of Optical and Quantum Electronics***, vol. 44, pp. 119–124, January **2012**.
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9. J. M. Hayes, **F. Gity**, B. Corbett, and A. P. Morrison, "Modeling the Effects of Interface Traps on Passive Quenching of a Ge/Si Geiger Mode Avalanche Photodiode," *11th International Conference on Numerical Simulation of Optoelectronic Devices (NUSOD)*, Rome, Italy, Sept. **2011**.
10. K. Y. Byun, J. M. Hayes, **F. Gity**, B. Corbett, and C. Colinge, "Wafer Bonded Ge–Si Heterostructure for Avalanche Photodiode Application," *Materials Research Society (MRS)*, San Fransisco, USA, Apr. **2011**.
11. I. Ferain, J. Hayes, R. Yu, K. Y. Byun, **F. Gity**, B. Long, and C. Colinge, "Electrical Conductivity of Directly Bonded Silicon/Germanium Hetero-Structures", *52nd TMS Electronic Materials Conference (EMC)*, p. 117, California, USA, Jun. **2011**.
12. **F. Gity**, J. M. Hayes, B. Corbett, and A. P. Morrison, "Modeling Ge/Si Avalanche Photodiodes," *IEEE European Conference on Integrated Optics (ECIO)*, Cambridge, UK, Apr. **2010**.
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Non-related publications

1. H. Yang, C. L. L. M. Daunt, **F. Gity**, K. –H. Lee, W. Han, B. Corbett, and F. H. Peters, "Zero–Bias High–Speed Edge–Coupled Unitraveling–Carrier InGaAs Photodiode," ***IEEE Photonics Technology Letters***, vol. 22, no. 23, pp. 1747–1749, December **2010**.
2. H. Yang, C. L. L. M. Daunt, **F. Gity**, K. –H. Lee, W. Han, K. Thomas, B. Corbett, and F. H. Peters, "Design and Fabrication of Uni–Traveling–Carrier InGaAs Photodiodes," ***Proc. of SPIE***, vol. 7847, Article Number: 784705, **2010**.
3. H. Yang, C. L. L. M. Daunt, K. –H. Lee, W. Han, **F. Gity**, B. Corbett, and F. H. Peters, "High–Speed and High–Power InGaAs/InP Photodiode," *23rd International Conference on Indium Phosphide and Related Materials (IPRM)*, Berlin, Germany, May **2011**.

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List of acronyms

Acronym	Definition
AML	Applied Microengineering Limited
APD	Avalanche Photodiode
ARC	Anti-Reflection Coating
BCB	Bisbenzocyclobutane
BEOL	Back-End-Of-Line
BER	Bit Error Rate
BOX	Buried Oxide
BW	Bandwidth
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
EPD	Etch Pit Density
GBP	Gain Bandwidth Product
GOI	Germanium-On-Insulator
GR	Guard Ring
LEPE-CVD	Low Energy Plasma Enhanced Chemical Vapour Deposition
MBE	Molecular Beam Epitaxy
MHAH	Multiple Hydrogen Annealing for Heteroepitaxy
MSM	Metal Semiconductor Metal
M/NEMS	Micro/Nano-Electro-Mechanical Systems
NEP	Noise Equivalent Power
NI	Normal Incident
PECVD	Plasma Enhanced Chemical Vapour Deposition
PIC	Photonics Integrated Circuits
RMG	Rapid Melting Growth
RP-CVD	Reduced Pressure Chemical Vapour Deposition
SACM	Separate Absorption Charge Multiplication
SAT	Spray Acid Tool
SC1(2)	Standard Cleaning 1(2) solution

SEG	Selective Epitaxial Growth
SEM	Scanning Electron Microscopy
SIMS	Secondary Ion Mass Spectrometry
SOI	Silicon-On-Insulator
SRP	Spreading Resistance Profile
TDD	Threading Dislocation Density
TEM	Transmission Electron Microscopy
TLM	Transfer Length Method
UHV-CVD	Ultrahigh Vacuum Chemical Vapour Deposition
UID	Un-Intentionally Doped
UPSW	Un-Processed Silicon Wafer
WG	Waveguide
XRD	X-Ray Diffraction

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Chapter 1: Introduction and literature review

1.1. Introduction

In order to achieve high performance and low-cost optical links, it is desirable to integrate optical components such as photodetectors, light sources and modulators with the silicon technology. Silicon is the base material for electronic technologies and is emerging as a very attractive platform for photonic integrated circuits (PICs). As PICs and other optical networks are moving toward the consumer market, developing low-cost and manufacturable optical components integrated on a chip with other electrical components is crucial. Many of these components have been demonstrated by integrating the discrete optical devices in existing silicon integrated circuits. Considerable research has been directed towards this challenge for highly integrated modulators [1], silicon-on-insulator (SOI) waveguide technology [2], and silicon-germanium based photodetectors [3]. One major application of such photodetectors is in optical communication systems. Another application is in infra-red wavelength cameras.

The basic advantages of a silicon-based approach to fabricate photonic devices are the potential to lower cost and easier manufacturing process for mass-production. Most silicon-based optical receivers in the past operated at $\lambda < 1\ \mu m$ (band gap of silicon). In order to extend the operating wavelength to longer wavelengths, i.e., 1.3 μm and 1.55 μm, absorbing materials with smaller band gap, such as germanium, is required to be integrated with silicon.

1.1.1. Germanium for long wavelength detection

Both InGaAs and Ge have high absorption at 1.3 μm which makes them suitable for long wavelength photodiodes. Fig. 1-1 shows the optical absorption coefficient of germanium and silicon as a function of wavelength. The high optical absorption coefficient at 1.3 μm and 1.55 μm makes germanium suitable for photodetection.

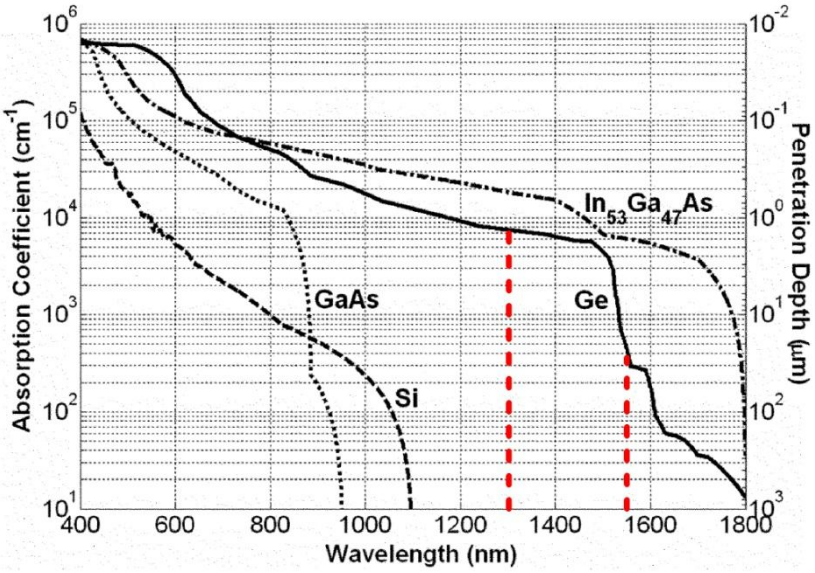


Fig. 1-1. Absorption coefficients of various semiconductors - taken from Dosunmu [4].

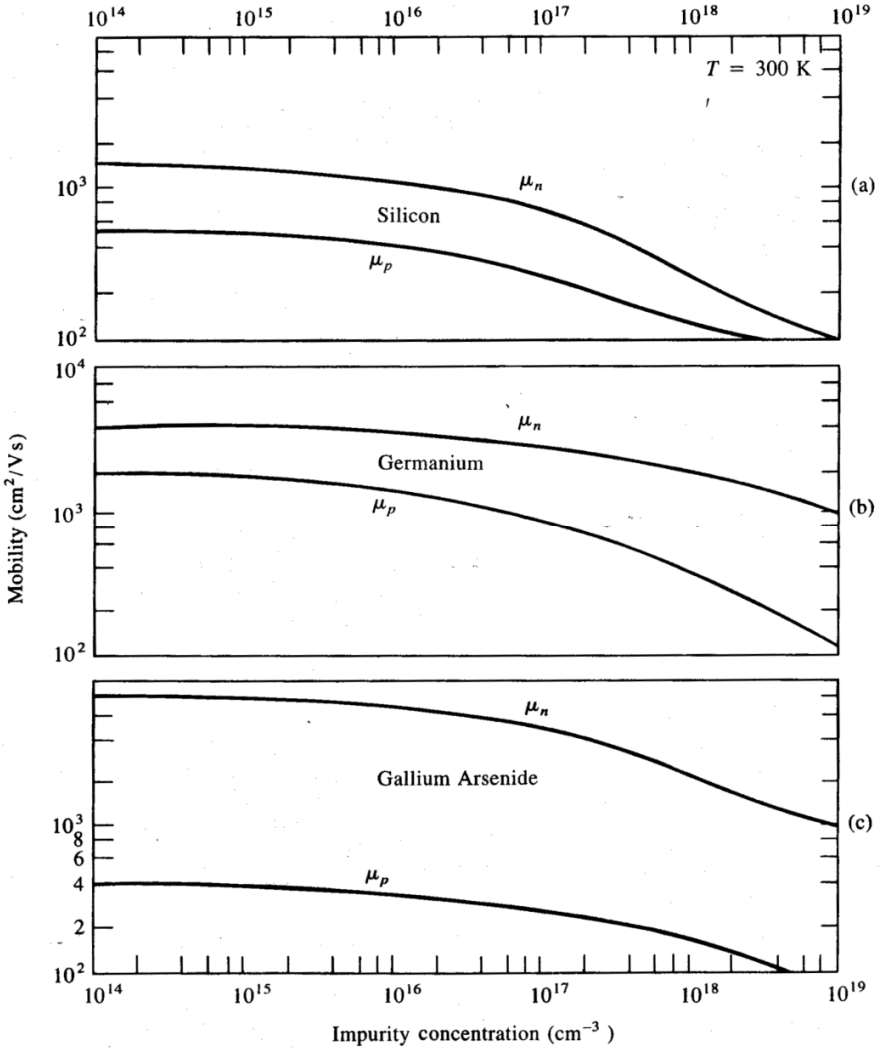


Fig. 1-2. Drift mobility of (a) Si, (b) Ge, and (c) GaAs at 300 K versus impurity concentration - taken from Sze [5].

Although high performance photodetectors are widely available using III-V semiconductors, the use of germanium is advantageous in terms of lower cost of fabrication and compatibility with silicon complementary metal oxide semiconductor (CMOS) process using the existing mature silicon manufacturing infrastructure. Another attractive feature of Ge is its low temperature processing capability. In addition, germanium is promising for other applications such as microwave photonic systems that require high photocurrent [6]. Germanium has also higher carrier mobility than silicon for both electrons (~3x) and holes (~4x). As shown in Fig. 1-2, the hole mobility of germanium is even higher than that of GaAs.

1.1.2. Characteristics of optical receiver

Two of the most important characteristics of optical receivers are their sensitivity and speed; both depend upon the performance of the integrated detectors. A high performance photodiode must provide high quantum efficiency, low leakage current and high speed. The quantum efficiency, η, for a photodetector is a measure of how many electron-hole pairs are collected per incident photon. The quantum efficiency can be expressed as:

$$\eta = (1 - R)\,(1 - e^{-\alpha d}), \tag{1-1}$$

where R is the reflectivity of the material, α is the absorption coefficient of the absorption region, and d is the absorption layer thickness.

The dark current of a photodetector is the current which is generated in the absence of light and depends mostly on the device structure and the material quality. Usually, this current is high for materials with narrow bandgap, and therefore, high intrinsic carrier concentration. For lattice-mismatched materials, the large density of dislocations may be the dominant component of the dark current. In an optical receiver system, the dark current of the photodiode contributes to the noise of the receiver and hence the signal-to-noise ratio of the system.

The speed of a photodetector defines how fast the photodetector responds to a modulated optical input. The speed is determined by both the RC and the transit-time components. For normal-incidence photodiodes there is a trade off between the speed and the quantum efficiency. In order to achieve high quantum efficiency, a thick absorption region is required, which on the other hand, increases the distance that the

photo-generated carriers must travel and hence limits the device speed. This issue can be greatly alleviated if a waveguide configuration is used. In this configuration, light absorption occurs along the propagation axis of an optical mode parallel to the wafer surface, therefore converting the thickness requirement into a waveguide length requirement.

1.2. Ge/Si photonic and electronic integrated circuits

Over the past decades, conventional optical components were typically made of III–V compound materials such as gallium arsenide (GaAs) and indium phosphide (InP) due to their excellent light emission and absorption properties. Unfortunately, compound-semiconductor devices are generally too complicated to process and costly to implement in optical interconnects. In search for a cost-effective solution, Si photonics emerges to hold great promise for its inexpensive material and its compatibility with current CMOS fabrication technology. Recent advancements have also shown that silicon is a viable optical material suitable for high-bandwidth data communication applications. In addition, the feasibility of converging photonic and electronic integrated circuits all on a single chip makes it an extremely attractive option to extend the performance roadmap as driven by Moore's Law.

There is a considerable research work in the field of silicon photonics in particular in the integration of long wavelength germanium photodetectors with silicon. For example, a low-power, short-wavelength eight-channel monolithically integrated photoreceiver array, based on SiGe/Si heterojunction bipolar transistors was demonstrated by Qasaimeh *et al*. from University of Michigan, Ann Arbor in 2000 [7]. The photodiode and transistors are grown by molecular beam epitaxy in a single step. The p-i-n photodiode exhibits a responsivity of 0.3 A/W and a bandwidth of 0.8 GHz at $\lambda = 0.88\ \mu m$.

Design and fabrication of a monolithically integrated evanescent-coupled germanium-on-silicon-on-insulator (SOI) photodetector and CMOS circuits on common SOI platform using an "electronic-first and photonic-last" integration approach are reported in 2010 by Prof. Kwong's group in A*STAR, Singapore [8, 9]. A high-performance detector with an integrated Si waveguide was demonstrated on ~500 nm thick epitaxial germanium absorbing layer which was selectively grown by ultrahigh vacuum chemical vapour deposition (UHV-CVD) technique on an ultrathin SOI

substrate (Fig. 1-3). Performance metrics of photodetector designs featuring vertical and lateral PIN configurations were investigated (Fig. 1-4). High responsivity of ~0.92 A/W was obtained in both detector designs for a wavelength of 1550 nm, which corresponds to a quantum efficiency of ~73%. Eye patterns measurement confirms the achievement of high-speed and low-noise photodetection at a bit rate of 8.5 Gb/s.

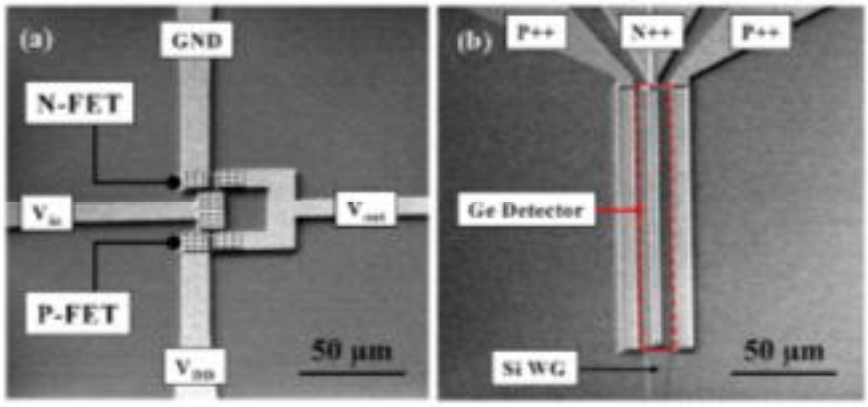


Fig. 1-3. (a) SEM micrograph of a Si CMOS inverter circuit on SOI platform. (b) SEM micrograph of a monolithically integrated Ge p-i-n photodetector with a Si photonic waveguide [8].

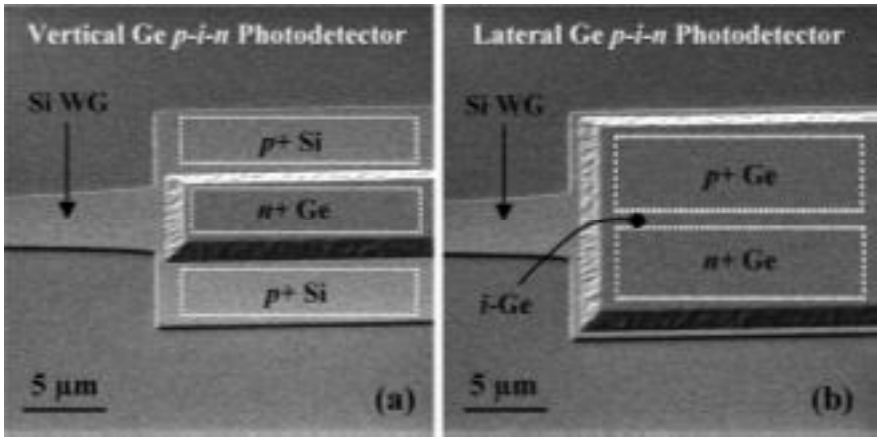


Fig. 1-4. (a) SEM micrograph showing an evanescent coupled Ge photodetector featuring vertical p-i-n configuration. The width *W* and length *L* of the detector is 8 and 100 μm, respectively. (b) Ge photodetector design with a lateral p-i-n configuration. The width *W* and length *L* of this detector is 20 and 100 μm, respectively [8].

Kopp *et al*. from LETI, France in 2011 demonstrated high-density germanium photodiode arrays integrated on top of a dummy CMOS 200-mm silicon wafer by depositing germanium using RP-CVD at temperatures > 700 °C (Fig. 1-5) [10]. Using a conventional available semiconductor fabrication line, the target specifications are reached with a yield exceeding 99% for several thousands of tested photodiodes with respect to bandwidth, responsivity, and dark current. A very low dark current density in the range of 7 mA/cm^2 is obtained. A bandwidth above 9 GHz is reached with a 30-μm diameter photodiode. At a wavelength of 850 nm a responsivity of 0.48 A/W for 350-nm thick Ge layer and 0.56 A/W for 650-nm thick Ge layer is measured.

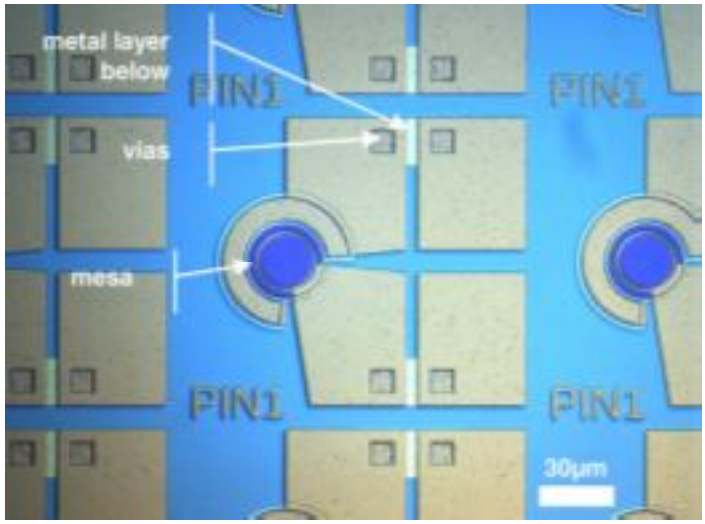


Fig. 1-5. Fabricated 30-μm mesa diameter photodiode array. Vias connect the photodiode pads to the embedded metal layer below from the CMOS-based silicon wafer [10].

Very recently in Dec. 2012, Assefa *et al*. from IBM demonstrated the first sub-100 nm technology that allows the monolithic integration of optical modulators and germanium photodetectors as features into a current 90 nm-base high performance logic technology node [11]. The electrical eye diagram of the receiver, measured with 1.54 μm light modulated at 25 Gbps, shows good performance. To yield deeply scaled nanophotonics features, a high resistivity SOI substrate with 2 μm BOX is utilized as a base for 90 nm CMOS-Integrated Nano-Photonics (CINP) technology (see Fig. 1-6).

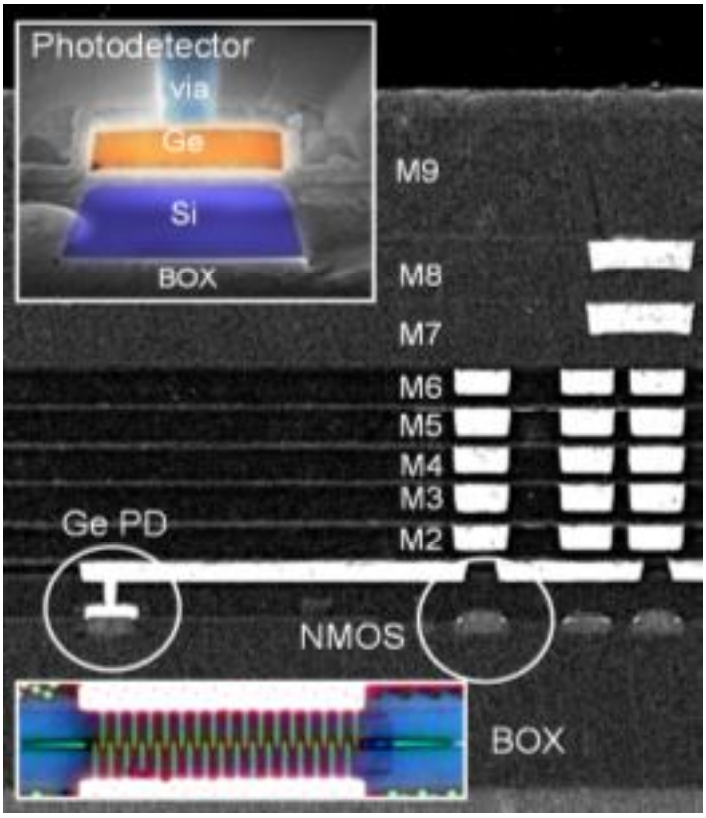


Fig. 1-6. Cross-sectional SEM view of a 90 nm CMOS-Integrated Nano-Photonics (CINP) metal stack with Ge PD embedded into the front-end. Zoomed-in image of a PD is shown on top left. Optical microscope top-down image is shown on the low left [11].

1.3. Ge/Si integration techniques

There are two major techniques to integrate crystalline germanium with silicon. As shown in Fig. 1-7, these methods are epitaxial growth and wafer bonding. Sections 1.3.1 and 1.3.3 review the progress that has been made with regard to each technique. A combination of hetero-epitaxy and wafer bonding has also been investigated for this purpose [10, 12].

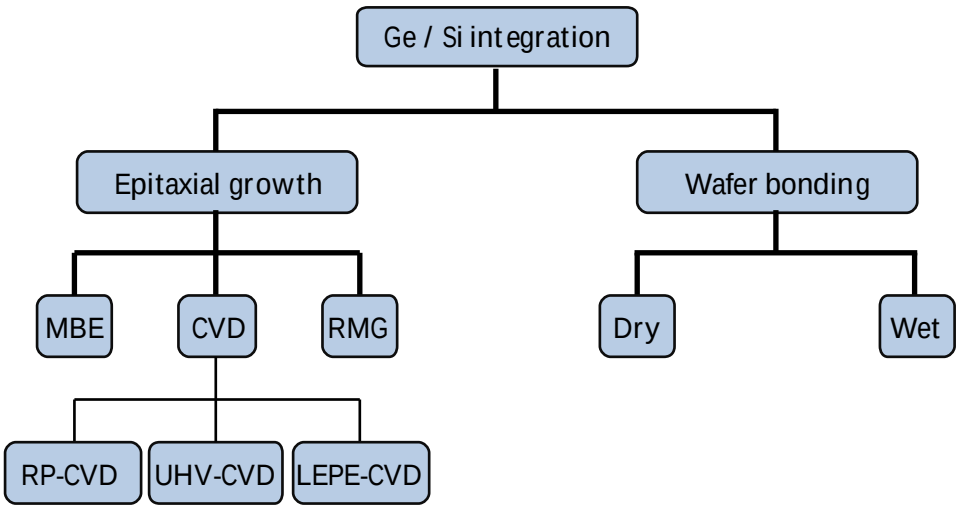


Fig. 1-7. Various techniques that have been used for the integration of germanium with silicon. MBE: Molecular Beam Epitaxy; CVD: Chemical Vapour Deposition; RMG: Rapid Melting Growth; RP-CVD: Reduced Pressure CVD; UHV-CVD: Ultra High Vacuum CVD; LEPE-CVD: Low Energy Plasma Enhanced CVD.

1.3.1. Ge/Si integration by epitaxy

Despite the potential advantages of Ge, the growth techniques and material quality of Ge on Si have limited the device performance and the potential for integration with Si ICs. The greatest challenge for high quality germanium epitaxy on silicon is the 4.2% lattice mismatch between the two materials. The misfit-related strain of the Ge film is relaxed by formation of a micro-rough surface up to a critical thickness of a few monolayers. For thicker Ge films the misfit is relieved by forming dislocation network in the germanium epitaxial layer originated from the Ge/Si interface. The difference between the Si and Ge thermal expansion coefficients (α_{Si} = 3.55 $\times$ 10^{-6} K^{-1} and α_{Ge} = 7.66 $\times$ 10^{-6} K^{-1} [13]) also leads to tensile strain during cooling down from the growth temperature which results in microcracks or residual tensile strain and dislocations which could be an advantage in terms of narrowing the band gap [14].

High density of threading dislocations affects the performance of normal incident germanium devices because of the recombination centres that are introduced along these dislocations. For the purpose of fabricating surface normal Ge photodetectors integrated with Si, the thickness of the Ge absorption layer has to be much larger than the critical thickness. Various techniques have been utilized to achieve low defect

density in the Ge film on Si; such as: (i) graded buffer layers, (ii) selective growth, (iii) two-step Ge growth (low/high temperature), (iv) post-growth cyclic thermal annealing, or combination of some of them.

1.3.1.1. Molecular Beam Epitaxy (MBE)

The first approach to overcome the lattice mismatch and to achieve high-quality Ge epilayer on Si is to use compositionally graded SiGe buffer layer(s). The first successful approach was reported by Luryi *et al*. from AT&T Bell Laboratories in 1984 where a graded SiGe buffer layer grown in a ***MBE*** chamber was used to reduce the threading dislocation density in the Ge layer [15]. The graded buffer layers consist of 10% Ge per 1 μm, which results in a very thick (10 μm) buffer layer for Ge content varying from 0% to 100%. This approach has led to the Ge film with low threading dislocations of $< 2 \times 10^6$ cm^{-2}. In view of the integration with Si CMOS circuits, the thick SiGe buffer layer makes integration difficult.

Compositionally graded Ge_xSi_{1-x} layers on Si at 900 °C with both ***MBE*** and rapid thermal chemical vapour deposition techniques are grown in 1991 by Fitzgerald *et al*. from AT&T Bell Laboratories [16]. Ge_xSi_{1-x} cap layers grown on these graded layers showed low threading-dislocation densities (4×10^5 cm^{-2} and 3×10^6 cm^{-2} for x = 0.23 and x = 0.50, respectively).

Malta *et al*. from North Carolina State University in 1991 reported on a heteroepitaxial Ge on Si grown using ***MBE*** at a temperature of 900 °C [17]. Their results reveal a highly faceted interface, indicating localized Ge melting and subsequent local alloying with Si which leads to extensive threading dislocation confinement near the Ge/Si interface. Etch pit density measurements obtained on Ge heteroepitaxial films showed the density of dislocations to be as low as 10^5 cm^{-2}.

In 2001, Liu *et al*. from UCLA reported high-quality Ge-on-Si using solid-source ***MBE*** [18]. They used a SiGe graded buffer. A relaxed Ge film on a 4-μm-thick graded buffer was grown and shown to have a threading dislocation density of 5.4×10^5 cm^{-2}.

Jutzi *et al*. in 2005 have utilized an ultrathin virtual substrate for the purpose of matching the 4% larger lattice constant of Ge to Si. Matching is obtained by misfit dislocations. A rather high density of threading dislocations in the order of 10^8 cm^{-2} is

generated by the thin ungraded buffer by ***MBE***. In the next growth step at 300 °C, a fully strain relaxed 300 nm intrinsic region is deposited [19].

1.3.1.2. Ultrahigh Vacuum Chemical Vapour Deposition (UHV-CVD)

The heteroepitaxial growth of pure Ge films on (100) Si by ***UHV-CVD*** technique is reported for the first time by Cunningham *et al*. from IBM in 1991 [20]. The growth mode is found to be critically dependent on the substrate temperature during deposition. Two temperature regimes for growth are observed. Between 300 and 375 °C, growth occurs in a two-dimensional, layer-by-layer mode. Above 375 °C, island formation is observed.

In 1998, Currie and Fitzgerald *et al*. from MIT reported high-quality Ge layers grown by ***UHV-CVD*** on optimized relaxed buffers by introducing a chemical mechanical polishing (CMP) step at $Si_{0.5}Ge_{0.5}$ in the graded structure [21]. The Ge graded buffer at 10% Ge μm^{-1} exhibited a final threading dislocation density of 2.1×10^6 cm^{-2} which was an order of magnitude lower than that of a sample with 5% Ge μm^{-1} grade with no CMP step.

Luan and Kimerling *et al*. from MIT in 1999 reported high quality Ge epitaxial layers on Si substrates with low threading-dislocation densities using two-step ***UHV-CVD*** process followed by cyclic thermal annealing [22]. After 30 nm of Ge was deposited on Si, the furnace temperature was raised to 600 °C and 1 μm of Ge was deposited on Si. The wafers were then cyclic annealed between a high annealing temperature and a low annealing temperature. The threading dislocation density was measured to be 2.3×10^7 cm^{-2}.

In 2000, Langdo and Fitzgerald *et al*. from MIT have shown that pure Ge grown selectively on Si substrates using ***UHV-CVD*** is highly perfect at the top surface compared to conventional Ge lattice-mismatched growth on planar Si substrates [23]. Selective growths are usually achieved by using a dielectric mask layer such as SiO_2 or Si_3N_4. Openings are etched through the dielectric layer and reach the surface of the single crystal silicon layer. This “epitaxial necking”, in which threading dislocations are blocked at oxide sidewalls, shows promise for dislocation filtering and the fabrication of low-defect density Ge on Si.

Dehlinger and Koester *et al*. from IBM in 2004 reported on growing a thin Ge seed layer at 350 °C prior to the growth of 400 nm Ge layer at 600 °C by ***UHV-CVD*** [24]. The layer structure then underwent thermal cyclic annealing (780 °C and 900 °C, 10 cycles) to reduce the density of threading dislocations The threading dislocation density after the anneal step was found to be 10^8 cm^{-2}.

Liu and Kimerling *et al*. from MIT in 2005 demonstrated Ge epitaxial layers which were selectively grown directly on Si by ***UHV-CVD*** [25]. A ~60 nm Ge buffer layer was grown at 335 °C followed by a high temperature growth at 700 °C to deposit 2.35 μm of Ge. The Ge epitaxial film was then subjected to a 900 °C anneal to reduce the threading dislocation density from 8×10^8 cm^{-2} to 1.7×10^7 cm^{-2}.

In 2006, Huang and Campbell *et al*. from the University of Texas, Austin have shown that using thin SiGe buffer layers with different Ge compositions leads to low density of threading dislocations [26]. They have grown a 0.18 μm $Si_{0.58}Ge_{0.42}$, and 0.28 μm $Si_{0.42}Ge_{0.58}$ buffer layers in a cold-wall ***UHV-CVD*** system at 500 °C. After growing each buffer layer, the wafer was *in situ* annealed at 750 °C for 15 min to reduce the dislocation density. Following the SiGe buffer layers, a 50 nm thick Ge layer was grown at 350 °C. Finally, the reactor temperature was increased to 600 °C, and a 1.70 μm thick Ge film was grown. The threading dislocation density was over 5×10^8 cm^{-2} in the SiGe layers, and less than 7×10^6 cm^{-2} in the Ge layer.

In 2007, Loh and Kwong *et al*. from A*STAR, Singapore reported a method to grow high quality strain-relaxed Ge on a combination of low-temperature Ge seed layer on low temperature ultrathin $Si_{0.8}Ge_{0.2}$ buffer with thickness of 27.3 nm by ***UHV-CVD*** method without the need to use chemical mechanical polish or high temperature annealing [27]. The etch-pit density on an 8-inch Si wafer was 6×10^6 cm^{-2}.

1.3.1.3. Reduced Pressure Chemical Vapour Deposition (RP-CVD)

In 2006, Morse *et al*. reported on a two-step Ge growth condition in a ***RP-CVD*** [28]. First, 0.1 μm of Ge was deposited at 400 °C, after which the temperature was raised to 670 °C for the rest of the growth (1.2 μm). The 900 °C annealing step serves to reduce the threading dislocation concentration to ~10^7 cm^{-2} which, in turn, leads to a reduction of the device dark current.

1.3.1.4. Low Energy Plasma Enhanced Chemical Vapour Deposition (LEPE-CVD)

Oh and Campbell *et al*. from the University of Texas, Austin in collaboration with Motorola reported on using ***LEPE-CVD*** technique to grow a 1-μm-thick Ge on a Si substrate using a 10-μm-thick graded SiGe buffer layer in 2002 [29]. A growth rate of 45 Å/s ~ 60 Å/s was achieved. The Ge epitaxial layer had a threading dislocation density of 10^5 cm^{-2}.

In 2009, Osmond and Isella *et al*. from Polytechnic University of Milan in collaboration with Epispeed reported on a single step growth of Ge directly on Si at a constant substrate temperature of 500-600 °C by ***LEPE-CVD*** [30]. In order to reduce the threading dislocation density, wafers were annealed in 3 cycles between 600 °C and 780 °C, each time ramping at ~60 °C/min and staying at maximal temperature for 4 min. Annealed samples showed a dislocation density of 2×10^7 cm^{-2} as determined by etch pit counting.

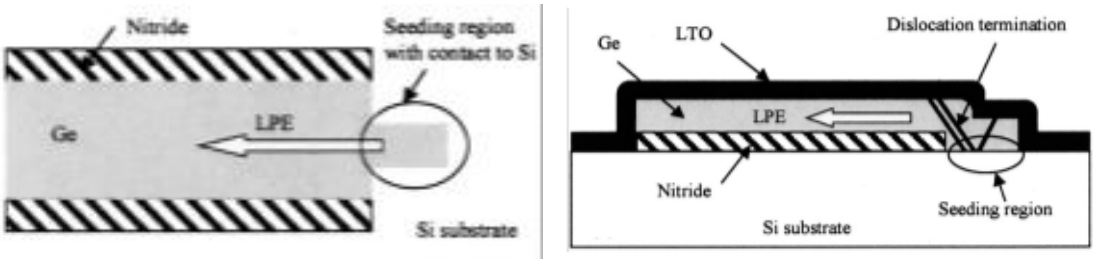
1.3.1.5. Multiple Hydrogen Annealing for Heteroepitaxy (MHAH) CVD

Another direct Ge growth method which is demonstrated by Nyfeh and Saraswat *et al*. from Stanford University in 2004 and 2005 uses ***MHAH-CVD*** at around 825 °C instead of a two-step growth process to confine misfit dislocations near the Ge-Si interface, thus not threading to the surface as expected in this 4.2% lattice-mismatched system [31, 32]. In the first step, a Ge layer was grown at 400 °C at a reduced pressure of 10 torr. This was followed by a H_2 anneal for 1 h at 825 °C and at a pressure of 80 torr, which yielded ~155 nm of Ge with rms surface roughness of 2.9 nm. In the second step, an additional 250 nm of Ge using the above growth conditions was deposited, followed by additional H_2 anneal at 700 °C and 80 torr, which yielded 400 nm of Ge.

1.3.1.6. Rapid Melting Growth (RMG) – Ge on insulator and waveguide structures

In 2004, Liu and Plummer *et al*. from Stanford University developed a method to make GOI based on ***RMG*** on Si substrates and a defect necking technique in which defects are confined to a very short distance [33]. Self-aligned microcrucibles were used to hold the Ge liquid. High-quality single-crystal (100) as well as (111) oriented GOI structures were obtained with a process compatible with Si-based fabrication. No dislocations or stacking faults were found in the RMG Ge films on insulator. The orientation of the Ge

crystals was controlled by the seeding Si substrate. In this technique, as is shown in Fig. 1-8, a silicon nitride layer was first deposited as the insulator layer on top of Si wafers, and then patterned the nitride film by photolithography and etching to make seeding windows through it. Ge was then sputtered non-selectively onto the substrate, covering both nitride and Si exposed by the seeding windows. Next the Ge films were patterned followed by oxide deposition. Rapid thermal annealing was used to heat the wafers up to 940 °C for 2 s. During this anneal, the Ge films melted. The wafers were cooled down naturally taking approximately 10 s to reach 400 °C. While the Ge liquid was cooling down, liquid-phase epitaxy occurred, with the growth front starting from the Si/Ge interface in the seeding windows, and propagating laterally through the Ge liquid on top of the silicon nitride films. This is the technique used by IBM in the fabrication of Ge avalanche photodiodes, which will be discussed in Section 1.3.2.3.



(a) **(b)**

Fig. 1-8. (a) Top view and (b) cross-sectional schematics of the structure used for Ge RMG growth [33]. LTO: Low Temperature Oxide.

In Table 1-1 some features of germanium growth techniques, such as maximum growth temperature, threading dislocation density (TDD) and the additional steps for the purpose of reducing TDD are summarised. By comparing TDD as one of the most crucial features of Ge on Si heteroepitaxy, one can conclude that TDD is in the order of 10^7 cm^{-2} for different growth techniques. It is worth mentioning that the maximum process temperature of epitaxy as an integration approach for almost all of the growth techniques is above the limit of CMOS back-end-of-line (BEOL) fabrication process. One of the goals of this thesis was to analyse the influence of the dislocations and defects at the Ge/Si interface on the performance of Ge/Si detectors. The next goal was to try to make ***normal incident*** Ge on Si avalanche photodiodes having a layer of germanium grown using LEPE-CVD technique [30] on structured silicon wafers. Wafer bonding was also employed in this thesis as another method of integration (see Fig. 1-7) to fabricate CMOS-compatible Ge on Si photodetectors.

Table 1-1. Summary of germanium growth techniques. TDD: Threading Dislocation Density.

Growth technique	Additional steps to reduce TDD				Max. process temp. (°C)	TDD (cm^{-2})	Ref.
	Buffer layer	Selective growth	Two-step growth	Post-growth anneal (°C)			
MBE	✓					$< 2 \times 10^6$	[15]
	✓				900	4×10^5	[16]
					900	10^5	[17]
	✓					5.4×10^5	[18]
	✓				300	10^8	[19]
UHV-CVD			✓		375		[20]
	✓					2.1×10^6	[21]
			✓	900	600	2.3×10^7	[22]
		✓					[23]
			✓	900	600	10^8	[24]
	✓	✓	✓	900	700	1.7×10^7	[25]
	✓			750	600	7×10^6	[26]
	✓					6×10^6	[27]
RP-CVD			✓	900	670	10^7	[28]
LEPE-CVD	✓					10^5	[29]
				780		2×10^7	[30]
MHAH-CVD				825	400	$5\text{-}7 \times 10^7$	[31,32,34]
RMG					940		[33]

1.3.2. Ge/Si photodetector by hetero-epitaxy

Ge/Si photodetectors are mostly designed and fabricated using two structures: normal incident (vertical), or waveguide structures. Due to much lower absorption coefficient of germanium at λ = 1.55 μm (~400 cm^{-2}) compared to λ = 1.3 μm (~8000 cm^{-2}), as is shown in Fig. 1-1, usually the characterization measurements are reported at λ = 1.3 μm.

1.3.2.1. Ge/Si photodetector – vertical structure

In 1984, Luryi *et al*. from AT&T Bell Laboratories demonstrated Ge p-i-n photodiodes on a silicon chip for the first time showing a quantum efficiency of 41% at 1.45 μm, which was measured in a short circuit configuration [15].

In 1998, Colace, Masini and Assanto *et al*. from Terza University of Rome reported metal-germanium-metal photodetectors fabricated on thick relaxed Ge layers [35]. Ge layers were epitaxially grown on silicon substrate using a low-temperature-grown Ge

buffer layer. The detector showed a maximum responsivity of 0.24 A/W at 1.3 μm under a 1 V bias. Later, in 2000, this group in collaboration with Kimerling from MIT demonstrated Ge/Si heterojunction photodetectors with high responsivities of 0.55 A/W at 1.32 μm and 0.25 A/W at 1.55 μm [36]. High quality 1 μm-thick Ge epitaxial layers were grown on Si substrate using a UHV-CVD system followed by cyclic thermal annealing.

In 2002, Oh and Campbell *et al*. from the University of Texas, Austin in collaboration with Motorola reported on an interdigitated p-i-n photodetector fabricated on a 1-μm-thick Ge epitaxial layer grown on a Si substrate using a 10-μm-thick graded SiGe buffer layer using LEPE-CVD technique [29]. The 3-dB bandwidth and the external quantum efficiency were measured on a MSM photodetector having 1-μm finger width and 2-μm spacing with a 25×28 μm^2 active area. At a wavelength of 1.3 μm, the bandwidth was 2.2, 3.5, and 3.8 GHz at bias voltages of −1, −3, and −5 V, respectively. The dark current was 3.2 and 5.0 μA at −3 and −5 V, respectively. This photodetector exhibited an external quantum efficiency of 49% at a wavelength of 1.3 μm.

Jutzi and Berroth *et al*. from University of Stuttgart in 2005 reported on mesa-type vertical-incidence germanium photodiodes (Fig. 1-9) [19]. The 10 μm-diameter device has 3-dB bandwidth of 25.1 GHz at an incident wavelength of 1552 nm and zero external bias. At a reverse bias of 2 V, the bandwidth is 38.9 GHz. The detector exhibits zero bias external quantum efficiencies of 23%, 16%, and 2.8% at 850, 1298, and 1552 nm, respectively.

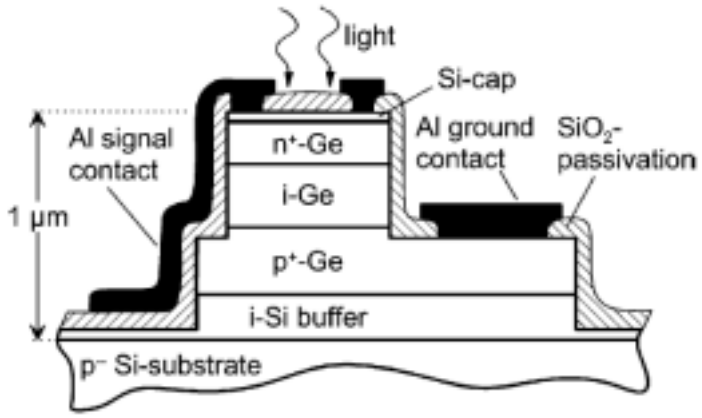


Fig. 1-9. Schematic cross section of the p-i-n photodetector (not to scale) [19].

In 2005, Liu and Kimerling *et al.* from MIT demonstrated a high-performance, tensile-strained Ge p-i-n photodetector on Si platform with an extended detection spectrum of 650-1605 nm and a 3 dB bandwidth of 8.5 GHz measured at λ = 1040 nm [25]. The full bandwidth of the photodetector is achieved at a low reverse bias of 1 V, compatible with the low driving voltage requirements of Si ultra large-scale integrated circuits. Due to the thermal expansion mismatch between the Ge epitaxial layer and the Si substrate, 0.20% in-plane tensile strain was introduced into the Ge layer. As a result, the device covers the entire C band and a large part of the L band in telecommunications. The responsivities of the device at 850, 980, 1310, 1550, and 1605 nm are 0.55, 0.68, 0.87, 0.56, and 0.11 A/W, respectively, without antireflection coating.

In 2006, Okyay and Saraswat *et al.* from Stanford University demonstrated extremely efficient germanium-on-silicon metal-semiconductor-metal photodetectors with responsivities as high as 0.85 A/W at 1.55 μm and 2 V reverse bias (Fig. 1-10) [34]. Ge was directly grown on Si by MHAH-CVD. Photodiodes on such layers exhibit reverse dark currents of 100 mA/cm^2 and external quantum efficiency up to 68%. Later, in 2009 this group reported on normal incidence p-i-n photodiodes on selective-area-grown Ge using MHAH-CVD for the purpose of monolithic integration (Fig. 1-11) [37]. An enhanced efficiency in the near-infrared regime and the absorption edge shifting to longer wavelength is achieved due to 0.14% residual tensile strain in the selective-area-grown Ge. The responsivities at 1.48, 1.525, and 1.55 μm are 0.8, 0.7, and 0.64 A/W, respectively, without an optimal antireflection coating.

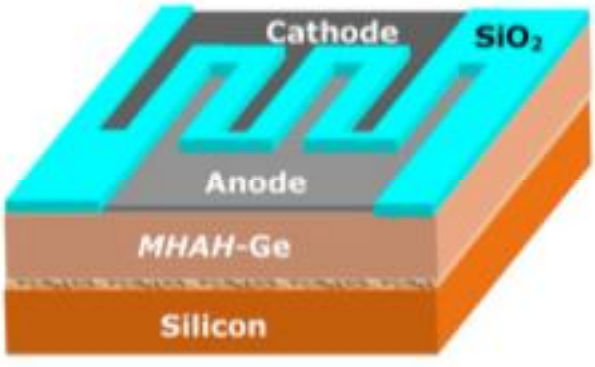


Fig. 1-10. Cross-section of MSM PD fabricated on MHAH-Ge layer grown on Si substrate. SiO2 layer was patterned before the evaporation of the metal electrodes. Defects are concentrated near the Si/Ge interface [34].

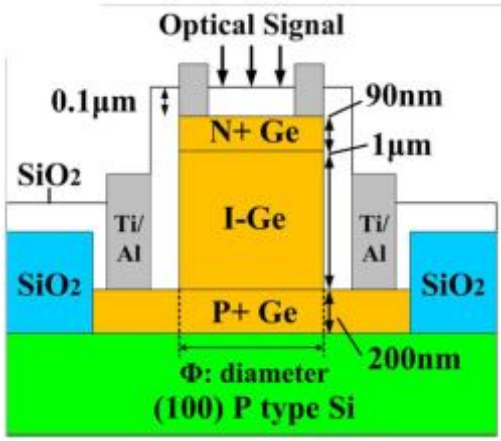


Fig. 1-11. Schematic diagram of the cross section of normal incidence Ge/Si p-i-n photodiode [37].

In 2009, Suh and Kim *et al*. from Electronics and Telecommunications Research Institute, Korea presented high-speed Ge p-i-n photodetectors for vertical incidence with high responsivity, grown by RP-CVD showing the residual tensile strain of 0.16% [38]. A 0.1-μm-thick Ge layer was grown at 400 °C on a (100) silicon wafer. The growth of 1.2- or 1.7-μm-thick Ge layer at 650 °C was followed without additional heat treatment to reduce the defects. The fabricated device exhibits the 3-dB bandwidth of 36 GHz at −3 V, the responsivity of 0.47 A/W at $\lambda \approx 1.55$ μm and at −1 V, and low dark current of 42 nA (which corresponds to dark current density of 18.5 mA/cm^2) at −1 V. The same device also shows the responsivity of 0.7 A/W at $\lambda \approx 1.31$ μm. This group in 2010 presented a high-sensitivity photoreceiver based on a vertical illumination 100% Ge-on-Si photodetector grown by RP-CVD [39]. The fabricated p-i-n photodetector with a 90 μm-diameter mesa shows the −3 dB bandwidth of 7.7 GHz, and the responsivity of 0.9 A/W at $\lambda \sim 1.55$ μm, corresponding to the external quantum efficiency of 72%. A TO-can packaged Ge photoreceiver exhibits the sensitivity of −18.5 dBm for a BER of 10^{-12} at data rate of 10 Gbps.

1.3.2.2. Ge/Si photodetector – waveguide structure

In 2006, Gunn from Luxtera demonstrated the technology to implement CMOS photonics, in particular, Ge photodetectors integrated into CMOS (Fig. 1-12) [40]. The detector showed a bandwidth of 18 GHz and a responsivity of 0.54 A /W at 1554 nm.

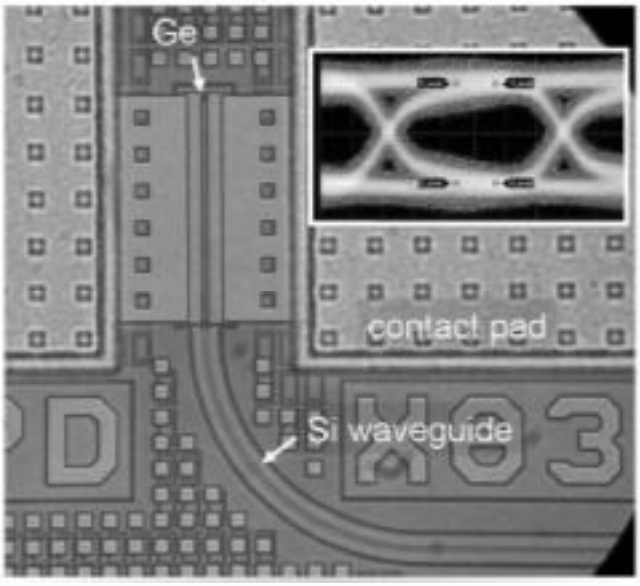


Fig. 1-12. Ge photodetector integrated in CMOS, shown with 10-Gbps eye (inset) [40].

In 2007, Luxtera improved their high-speed optical receiver using germanium waveguide photodetectors monolithically integrated in the CMOS process [41]. Ge was epitaxially grown by reduced pressure chemical vapour deposition (RP-CVD) on patterned 8" SOI wafers using a single step selective process at 350 °C to a thickness of 200 nm. The Ge waveguide photodetector has a homo-junction structure where the anode and cathode are both formed in the Ge layer by means of boron and phosphorous implants, respectively. The germanium waveguide photodetectors show a responsivity of 0.6 A/W at 1554 nm and a 3 dB bandwidth exceeding 20 GHz. The receiver operates at 1550 nm, 10 Gbps with sensitivity better than −14 dBm. Fig. 1-13 shows an optical microscope picture of the detector integrated in the optoelectronic integrated circuit.

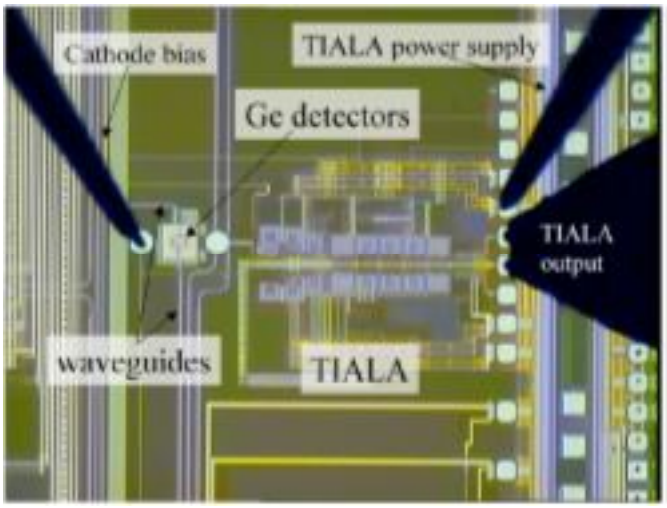


Fig. 1-13. Picture of the optical receiver including germanium waveguide photodetector monolithically integrated in CMOS process by Luxtera [41].

In 2007, Ahn and Kimerling *et al*. from MIT reported a Ge p-i-n photodetector that is monolithically integrated with silicon oxynitride and silicon nitride waveguides forming top-coupled photodetectors (Fig. 1-14) [42]. The waveguide-coupled Ge devices show high efficiency (~90%) over a wide range of wavelengths well beyond the direct band gap of Ge, resulting in a responsivity of 1.08 A/W for 1550 nm light.

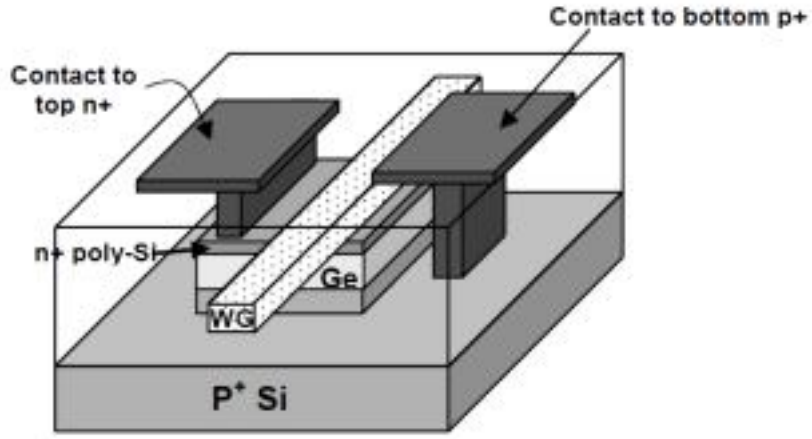


Fig. 1-14. Schematic structure of a waveguide-integrated Ge p-i-n photodetector [42].

Yin *et al.* from Intel reported on evanescently coupled Ge waveguide photodetectors grown on top of Si rib waveguides in 2007 (Fig. 1-15) [43]. A 1.3 μm thick film of Ge was grown by a selective epitaxial process. The growth consisted of a 0.1 μm thick low temperature Ge buffer layer followed by 1.2 μm of Ge grown at 700 °C (a final Ge thickness of 0.8 μm was obtained after CMP). These wafers then underwent a Ge anneal to reduce the threading dislocation density. A Ge waveguide detector with a width of 7.4 μm and length of 50 μm demonstrated an optical bandwidth of 31.3 GHz at −2V for 1550 nm. In addition, a responsivity of 0.89 A/W at 1550 nm and dark current of 169 nA (which corresponds to dark current density of 45.7 mA/cm^2) were measured from this detector at −2V. A higher responsivity of 1.16 A/W was also measured from a longer Ge waveguide detector (4.4 × 100 μm^2), with a corresponding bandwidth of 29.4 GHz at −2V.

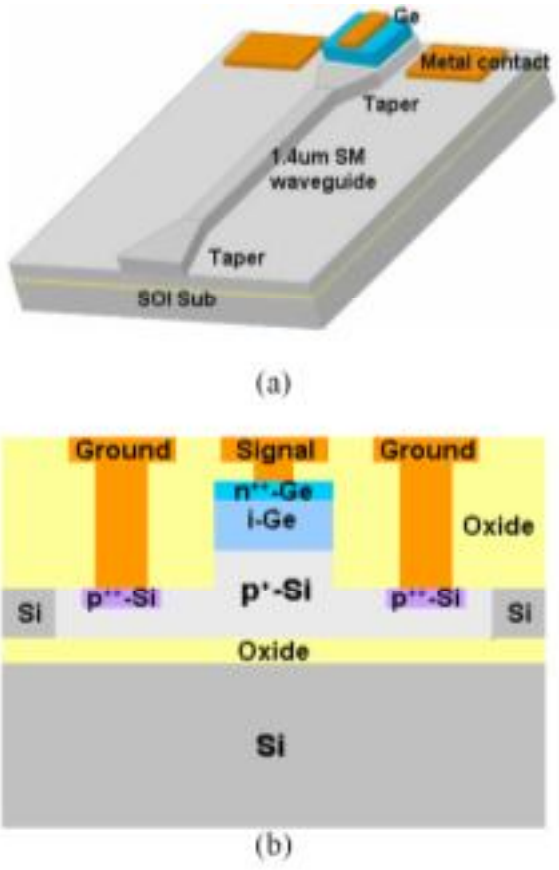


Fig. 1-15. (a) Schematic layout for the Ge detector integrated with a passive waveguide. (b) Cross-section schematic of the Ge n-i-p waveguide photodetector [43].

Feng *et al.* from Kotura Inc. reported a thin-film germanium photodetector integrated on 3 μm thick large core silicon-on-insulator (SOI) waveguides in 2009 [44]. The Ge

layer was selectively grown on top of the Si waveguide with a 100 nm thick Ge buffer layer using low-temperature (400 °C) growth followed by 1.1 μm thick Ge growth at high-temperature (670 °C). The wafers then underwent a post-growth-annealing step to reduce the threading dislocations in the Ge film. The device demonstrates very high external responsivity due to the low fibre coupling loss to the large core waveguides (Fig. 1-16). Even with fibre coupling loss included, the device has demonstrated greater than 0.7 A/W external responsivity at 1550 nm for TM polarization and 0.5 A/W for TE polarization. A low dark current of 0.2 μA at −0.5 V bias is reported, corresponding to dark current density of 28.5 mA/cm^2. 3dB bandwidths of 12 GHz and 8.3 GHz at −2.5V bias are also reported for 100 μm and 200 μm long devices, respectively. The device can cover the communication wavelength spectrum up to 1620 nm with a relatively flat responsivity of > 0.5 A/W.

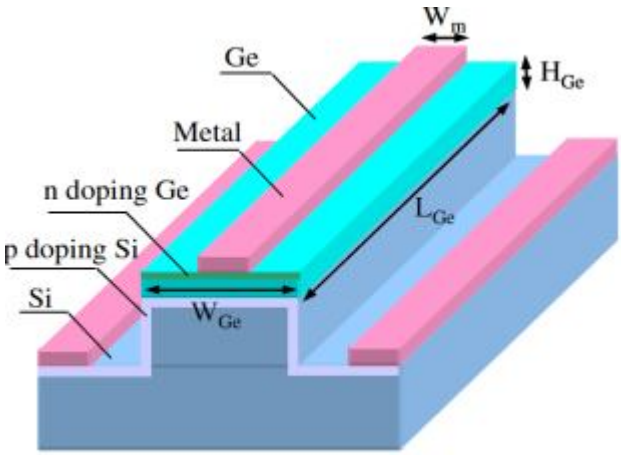


Fig. 1-16. Schematic view of a vertical pin Ge waveguide photodetector integrated on top of an SOI waveguide [44].

Vivien and Osmond *et al*. from University of Paris in collaboration with LETI, demonstrated a compact pin Ge photodetector integrated in submicron SOI rib waveguide selectively grown by RP-CVD in 2009 [45]. The detector length is reduced down to 15 μm using butt coupling configuration (see Fig. 1-17) which is sufficient to totally absorb light at the wavelength of 1.55 μm. A −3 dB bandwidth of 42 GHz has been measured at a 4V reverse bias with a responsivity as high as 1 A/W at the wavelength of 1.55 μm and a low dark current density of 60 mA/cm^2. At a wavelength of 1.52 μm, a responsivity of 1 A/W is obtained under −0.5 V bias.

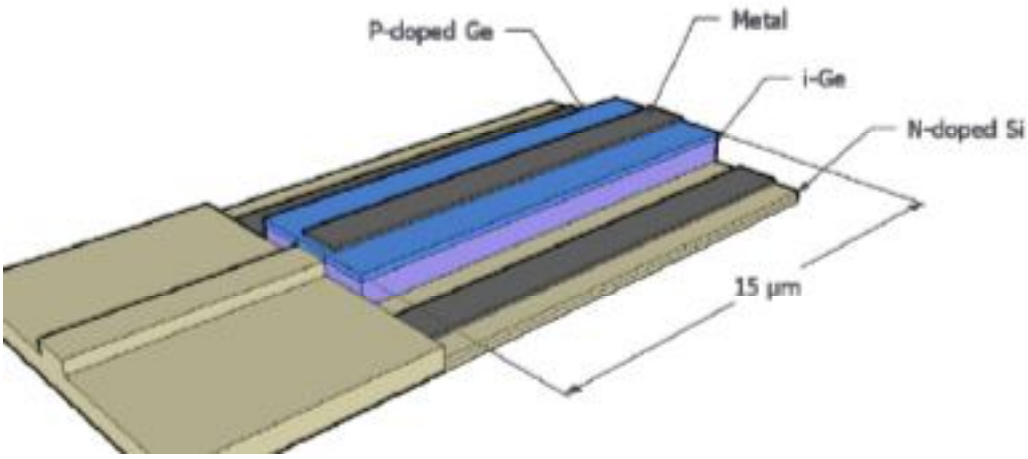


Fig. 1-17. Schematic view of pin germanium photodetector integrated in SOI waveguide. The photodetector length and width are 15 μm and 3 μm, respectively [45].

1.3.2.3. Ge/Si avalanche photodiode

An Avalanche Photodiode (APD) provides higher sensitivity than a conventional PIN photodiode due to its internal gain. It is ideal for extreme low-level light detection and photon counting. The use of APDs instead of PIN photodetectors will result in improved sensitivity. At longer wavelengths Ge can be used as the absorption layer; however, since silicon has lower multiplication noise, usually the APD is designed in such a configuration that multiplication occurs in Si. Due to their performance advantages, typical applications of APDs include low-light level measurement, spectroscopy, data transmission and fibre optic communication, distance measurement, industrial inspection and in various other medical and scientific instrumentation.

In 2009, Wang *et al*. from Nano Photonics, Inc., in collaboration with A*STAR, Singapore demonstrated selectively grown Ge/Si APDs with a bandwidth of 10 GHz at gain of 8 at 1310 nm (Fig. 1-18) [46]. The selective epitaxial Ge growth begins with ~25 nm SiGe graded buffer layer at 350 °C, followed by a 1 μm thick pure Ge layer at 550 °C.

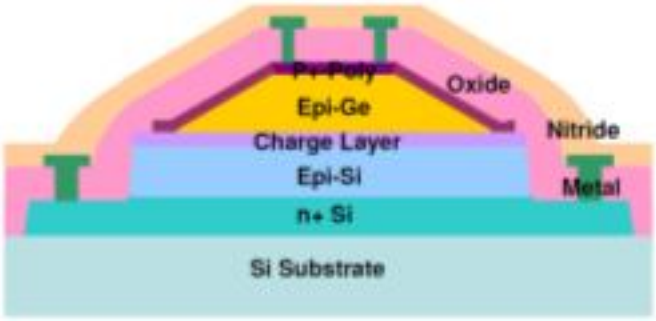


Fig. 1-18. Schematic cross-section of Ge/Si SACM structure [46].

In 2008, Kang, Bowers and Campbell *et al.* from Intel, UCSB and University of Virginia demonstrated monolithically grown germanium on silicon APDs with a 340 GHz gain bandwidth product, having an effective k-value of 0.09 and a sensitivity of -28 dBm at 10 Gb·s^{-1} at 1300 nm (Fig. 1-19) [3]. A two-step germanium epitaxial deposition was used to minimize the misfit dislocation density. A relaxed, germanium seed layer was grown at a lower temperature before the temperature was then increased to complete the growth of the layers. Etch pit studies on films overgrowing this annealed layer have shown a threading dislocation density of ~5×10^6 cm^{-2}, as compared to a pre-annealing concentration larger than 1×10^8 cm^{-2}.

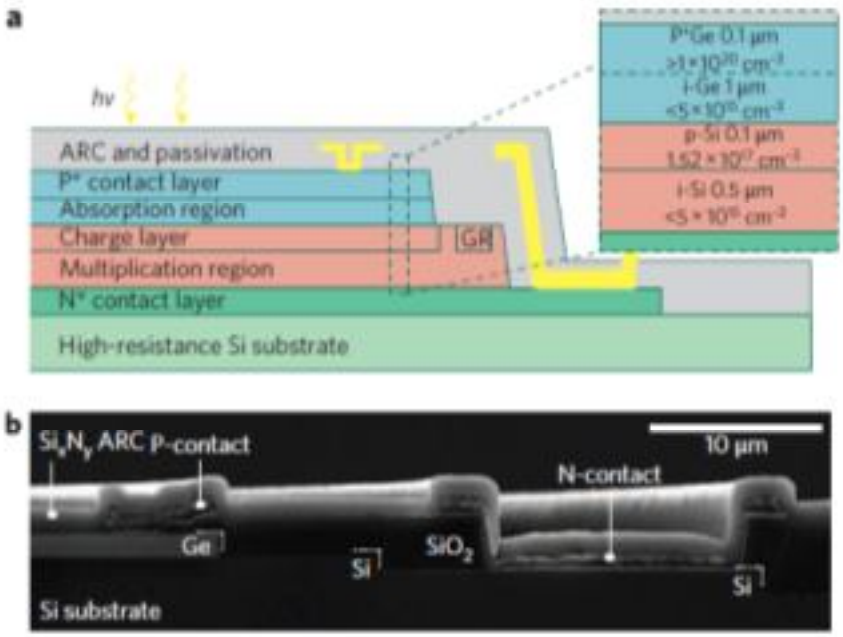


Fig. 1-19. (a) Schematic and (b) SEM cross-sections of a germanium/silicon APD. The floating guard ring (GR in 'a') design was used to prevent premature breakdown along the device perimeter. ARC: anti-reflection coating [3].

In 2010, Assefa *et al*. from IBM reported a waveguide-integrated metal-semiconductor-metal APD fabricated from single-crystal Ge waveguides formed by the rapid melting growth method (Fig. 1-20) [2]. After formation of silicon waveguides a thin SiON layer was deposited on top and a small seeding window down to Si layer was etched. Using rapid thermal chemical vapour deposition, a thin buffer layer of 30% SiGe was grown first, followed by a thick Ge layer. After Ge waveguide patterning and encapsulation the Ge was melted using rapid thermal annealing at around 1000 °C. During fast cooling the crystallization of melted Ge starts from a seeding window and propagates along the Ge waveguide, leaving behind a high-quality single-crystalline SiGe strip 20 μm long with a total Ge concentration of over 90%. By generating strongly non-uniform electric fields, the region of impact ionization in germanium is reduced to just 30 nm. The smallness of the APDs means that a bias voltage of only 1.5 V is required to achieve an avalanche gain of over 10 with operational speeds exceeding 30 GHz. The responsivity of 0.40 A/W and 0.14 A/W has been measured for the 1.3 μm and 1.5 μm wavelengths, respectively, for an APD with 200 nm contact spacing.

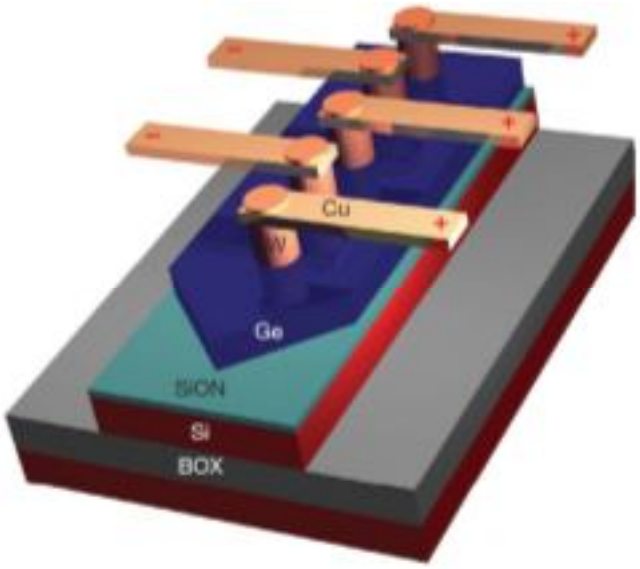


Fig. 1-20. Schematic of the nanophotonics Ge waveguide-integrated APD. The Ge layer is deposited on top of a SiON insulating layer which overlays a Si waveguide. The detector is biased though metallic interdigitated contacts consisting of W plugs and Cu wires [2].

In 2012, Duan *et al*. from A*STAR, Singapore reported a normal incidence Ge/Si avalanche photodiode with separate absorption charge multiplication (SACM) structure by selective epitaxial growth (SEG) [47]. A 1 μm-thick SEG Ge was grown using UHV-CVD epitaxy reactor. The SEG Ge growth started with ~50 nm SiGe graded

buffer layer followed by a Ge seed layer with a thickness of ~50 nm at 350 °C. The temperature was then increased to ~550 °C to complete the Ge growth. By proper design of charge and multiplication layers and by optimizing the electric field distribution in the depletion region to eliminate germanium impact-ionization at high gain, a high responsivity of 12 A/W and a large gain-bandwidth product of 310 GHz have been achieved at 1550 nm.

Table 1-2 summarises the performance of germanium photodetectors fabricated in different structures using different growth conditions.

Table 1-2. Summary of the performance of germanium photodetectors. R: Responsivity; λ: wavelength; η: quantum efficiency; BW: Bandwidth; NI: Normal Incident; WG: Waveguide; NEP: Noise Equivalent Power; MSM: Metal Semiconductor Metal; GBP: Gain Bandwidth Product; SACM APD: Separate Absorption, Charge, and Multiplication Avalanche Photo Diode.

Structure	Growth technique	R (A/W) @ λ (μm) @ Bias (V)	η (%) @ λ (μm) @ Bias (V)	BW (GHz) @ λ (μm) @ Bias (V)	NEP § (pW·Hz$^{-1/2}$)	Ref.
pin NI	MBE		41% @ 1.45 @ 0		38	[15]
MSM NI		0.24 @ 1.3 @ 1			76	[35]
NI	UHV-CVD	0.55 @ 1.32 @ - 0.25 @ 1.55 @ -			73	[36]
pin MSM NI	LEPE-CVD		49 @ 1.3 @ -	2.2 @1.3 @ 1 3.5 @1.3 @ 3 3.8 @1.3 @ 5	35	[29]
nip NI	MBE		23 @ 0.85 @ 0 16 @ 1.298 @ 0 2.8 @ 1.552 @ 0	38.9 @ 1.552 @ 2 25.1 @ 1.552 @ 0	520	[19]
pin NI	UHV-CVD	0.87 @ 1.31 @ - 0.56 @ 1.55 @ -		8.5 @ 1.04 @ 1	32	[25]
MSM NI	MHAH-CVD	0.85 @ 1.55 @ 2	68 @ - @ -		21	[34]
pin NI	MHAH-CVD	0.64 @ 1.55 @ -			28	[37]
pin NI	RP-CVD	0.7 @ 1.31 @ - 0.47 @ 1.55 @ -		36 @ 1.55 @ -	31	[38]
pin NI	RP-CVD	0.9 @ ~1.55 @ -	72 @ ~1.55 @ -	7.7 @ ~1.55 @ -	20	[39]
pin-WG	UHV-CVD	1.08 @ 1.55 @ -	~90 @ - @ -		17	[42]
nip-WG		0.89 @ 1.55 @ 2		31.3 @ 1.55 @ 2	20	[43]
pin-WG	UHV-CVD	0.7 @ 1.55 (TM) @ - 0.5 @ 1.55 (TE) @ -		12 @ - @ 2.5	26 36	[44]
pin-WG	RP-CVD	1 @ 1.55 @ 4		42 @ 1.55 @ 4	18	[45]
pin-QD	MBE	0.1 @ 1.55 @ 2.5			180	[48]

§ NEP is a device parameter which is important for low noise applications. Typical NEP for Si and InGaAs photodiodes is <10 fW·Hz$^{-1/2}$. It is in the same range for Si APDs, and in the range of a few hundred fW·Hz$^{-1/2}$ for InGaAs APDs. This parameter is not quoted in any of the papers in this table and is calculated using the referenced material considering the thermal noise to be dominant compared to the shot noise (dark and total currents are in μA range) and also considering the resistance to be 50 Ω. This parameter is calculated at room temperature and for a bandwidth of 1 Hz.

APD Structure	Growth technique	R (A/W) @ λ (μm) @ Bias (V)	Gain @ λ (μm) @ Bias (V)	GBP (GHz) @ λ (μm) @ Bias (V)	NEP ($pW \cdot Hz^{-1/2}$)	Ref.
SACM APD		0.42 @ 1.31 @ gain = 1	8 @ 1.31 @ 24.5	80 @ 1.31 @ 24.5	Not enough information	[46]
SACM APD	UHV-CVD	0.55 @ 1.31 @ gain = 1 / ~8.5 @ 1.3 @ ~24	~16 @ 1.3 @ ~24	340 @ 1.3 @ ~24	30 (at gain=10; excess noise factor: 2.55)	[3]
MSM-WG	RMG	0.4 @ 1.3 @ ~1 0.14 @ 1.55 @ ~1	10 @ 1.3 @ 1.5	300 @ 1.3 @ 1.5	570 (at gain=4.5; excess noise factor: 2.2)	[2]
SACM APD	UHV-CVD	~0.3 @ 1.55 @ gain = 1 12 @ 1.55 @ 29	~40 @ 1.55 @ 29	310 @ 1.55 @ -	Not enough information	[47]

1.3.3. Ge/Si integration by wafer bonding

As mentioned in the previous section, the primary limitation in hetero-epitaxy is lattice matching of the different materials which limits the applications of this integration method. Wafer bonding technique can eliminate the problems associated with the epitaxial technique. Therefore, direct wafer bonding which is the process of joining flat and clean wafers without any adhesives or intermediate layers can be used to integrate materials that are not suitable for hetero-epitaxy.

The interaction between flat surfaces was first investigated by Rayleigh in 1936 with smooth glass surfaces that interact strongly to form surface bonds [49]. The bonding of surfaces in direct wafer bonding occurs due to the interaction of surface bonds via van der Waals interactions. Surfaces with desired chemical passivation and with minimal surface roughness and number of particles are required to have strong bonds. In principle, all materials, regardless of their structural, crystal orientation, lattice parameters, doping profile / type and wafer thickness should be bonded once contacted as long as they satisfy surface requirements; i.e., surface roughness, flatness, and cleanliness. This flexibility of wafer bonding opens up vast opportunities for advanced electronics, low cost and high throughput packaging of micro-electro-mechanical systems (MEMS) and also for photonics and optoelectronics. Details of wafer bonding steps are mentioned in Appendix A1.

In 1986, IBM presented direct bonding of silicon wafers for the fabrication of silicon-on-insulator (SOI) substrates [50]. Since then, wafer bonding has found many applications in the fabrication of SOI and germanium-on-insulator (GOI) substrates,

and also in micro/nano-electro-mechanical systems (M/NEMS) and 3D integration [51, 52, 53, 54] as well as in III-V compound semiconductor based devices [55, 56], showing wafer bonding as a highly manufacturable and high-yield fabrication process. There are also potential applications in the integration of external light source with silicon due to the intense interest in silicon photonics as a platform for the manipulation and control of light signals near or on CMOS circuitry [57, 58]. Usually, hetero-epitaxy is used as the integration technique. However, as mentioned before, hetero-epitaxial growth leads to large number of misfit and threading dislocations in the deposited film due to lattice mismatch between the epilayer and the substrate. Also high temperature epitaxial growth and/or post growth heat treatment (~700-900 °C) is not compatible with CMOS technology. To circumvent these issues, low temperature direct wafer bonding is highly desirable. Low temperature wafer bonding provides another advantage in integration of dissimilar materials; e.g., germanium or compound semiconductors to silicon, where there is a mismatch in thermal expansion coefficients.

Successful bonding of Ge, GaAs and InP to Si for detectors, lasers and waveguides have been reported [59, 60, 61, 62, 63]. Ge to Si direct wafer bonding has been studied for the fabrication of photodetectors as well as multi-junction solar cells [62, 63, 64].

1.3.3.1. Fabrication challenges using wafer bonding

In most applications it is not desirable to bond two full substrates, but rather to have a thin layer of device material bonded to a thicker substrate. The thinning of the device layer has been achieved by many techniques, including epitaxial layer lift-off [65, 66, 67, 68], transfer defined epitaxial areas (coupons) [57], hydrogen-induced layer exfoliation (or ion-cut process) [69], and back-side etching or wafer thinning [70]. The last two techniques have been used in this thesis.

Hydrogen-induced layer exfoliation, which is studied in this thesis, is an integration technique by direct wafer bonding followed by removal of all but a thin layer of the material to be transferred - Smart Cut™ process [71]. One of the advantages of this process is that it allows reusing the device substrate following exfoliation, and also it guarantees thickness uniformity across the layer. This technique was first used for the fabrication of silicon-on-insulator (SOI) substrates [72]. Since then, it has also been developed for some other semiconductors, such as Ge, to make GOI substrates [73, 74] or as a platform to make the bonded wafers suitable for subsequent epitaxial growth [64].

The greatest challenge in wafer thinning, which has also been used in this study, is that the wafer must be thinned to about 5-10% of its original thickness with a required uniformity of ~1-2 μm. This thinning is especially challenging when using bulk wafers because there is no natural etch stop layer. The final thickness depends on the thinning process control capabilities and is limited by the thickness uniformity specifications of the removal process (that being mechanical grinding and polishing possibly plus wet or dry etching). Successful thinning to a uniform thickness of a few microns has been demonstrated, but typically thicknesses of 20-40 μm are necessary for a robust process.

1.3.4. Ge/Si photodetector by wafer bonding

There are a few groups working on Ge/Si photodetectors by direct wafer bonding in literature due to its complexity. Getting current transport across the interface is the most important challenge in using this method of devices fabrication. In 2007 Kanbe *et al*. from Kochi University of Technology reported on the formation of a wafer-bonded Ge/Si heterojunction using wet wafer bonding followed by annealing at 880 °C for 90 min in a hydrogen atmosphere [75]. A *transition layer* at the heterojunction was reported where an aligned lattice image from Si to Ge together with a disordered lattice image were observed. In the Si layer close to the interface, islandlike modified regions were observed where a large amount of Ge was detected. Oxygen was also detected accumulated at the interface. After the mesa-etching process cracks in the wafers were occasionally observed due to the thermal stress because of high temperature anneal. Later, in 2008, this group reported on Ge/Si heterojunctions formed by wet wafer bonding (Fig. 1-21) and annealing temperatures much lower than their previous experiment (250 or 350 °C) [76]. **Normal incident photodiodes** fabricated using this bonded heterojunctions exhibited photocurrents flowing over the heterojunction with internal quantum efficiency higher than 80% at wavelengths between 1000 and 1550 nm. Dark current density of 51 mA/cm^2 at −20 V is reported for these devices. For these samples a 10 nm-thick transition layer with amorphous-like structure was observed at the metallurgical junction [77].

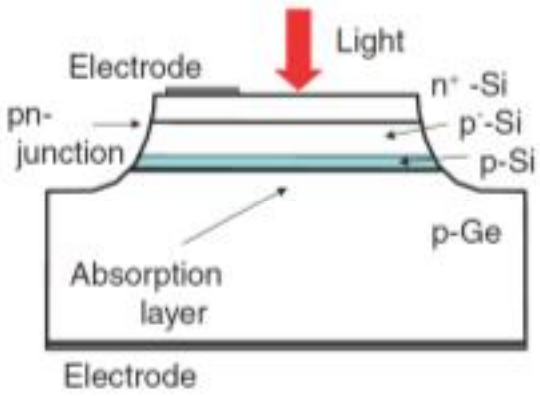


Fig. 1-21. Ge/Si heterojunction photodiode structure fabricated by low temperature wet wafer bonding [76].

In 2011, Jain *et al*. from Stanford University presented a method to fabricate tensile-strained germanium-on-insulator (GOI) substrates using heteroepitaxy and layer transfer techniques [78]. The motivation was to obtain a high-quality wafer-scale GOI platform suitable for silicon-compatible optoelectronic device fabrication. A biaxial tensile strain of 0.16% is verified by XRD. Suitability for device manufacturing is demonstrated through fabrication and characterization of metal-semiconductor-metal photodetectors. In this experiment, approximately 1.57 μm of Ge was epitaxially grown by RP-CVD on Si seed wafer using the MHAH technique. This wafer is then bonded to a Si handle wafer caped with thermal SiO_2 oxide. Bonded wafer pairs were then annealed for 10 hrs at 800 °C. After the post-bond anneal, the Si seed wafer was commercially back-ground, leaving ~50 μm of Si on top of Ge which was then chemically removed. In order to obtain a high-quality, low-defect density GOI film suitable for device fabrication, the defective surface (at Ge/Si epilayer) was removed by chemical-mechanical polishing system. The MSM **normal incident photodetectors** fabricated on this GOI substrate exhibited photoresponse beyond 1.55 μm.

In 2008, Chen and Lipson *et al*. from Cornel University demonstrated metal-semiconductor-metal germanium **waveguide photodetectors** integrated on submicron silicon waveguides fabricated with a low temperature (≤ 400 °C) wafer bonding and ion-cut process (Fig. 1-22) [60]. The devices showed a dark current density of ~400 mA/cm^2, a responsivity of > 0.4 A/W and an estimated quantum efficiency of above 90%.

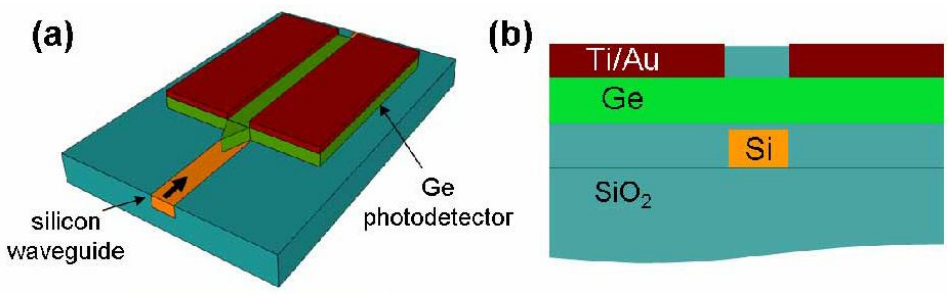


Fig. 1-22. Schematics of (a) the integrated Ge photodetector on a silicon waveguide, and (b) the device cross section [60].

1.4. Organisation of the thesis

An introduction to and a literature review for Ge/Si integration techniques and Ge/Si devices were shown in the previous sections of Chapter 1.

Chapter 2 provides the investigation on the design of Ge/Si separate absorption, charge and multiplication (SACM) avalanche photodiodes (APDs) where germanium is used as the absorption layer and silicon is used as the charge and multiplication layers. The influence of the germanium layer thickness and doping, along with the silicon charge and multiplication layers doping on the detectors' characteristics such as gain, breakdown voltage and gain-bandwidth product are determined. Additionally, the effects of interface donor- and acceptor-type traps on the static and dynamic behaviour of the Ge/Si APDs are presented.

Chapter 3 reports on the investigations on an epitaxial approach to achieve Ge/Si avalanche photodiodes. The structure and the layout of the fabricated detectors as well as different techniques that were used to characterize the germanium and silicon epilayers are presented in this chapter.

Chapter 4 describes the integration of germanium with silicon based on the wafer bonding approach. The fabrication and electrical characterization of current transport across a p-Ge/n-Si diode structure obtained by direct wafer bonding and layer exfoliation is reported. The effects of low temperature anneal on the characteristics of the diode as well as the carrier transport mechanism is also presented in this chapter.

Chapter 5 presents light-gated photoresponse from a p-Ge/n-Si heterojunction photodiode fabricated by low temperature wafer bonding followed by back-side

etching or wafer thinning. Based on the experimental results of the electrical and optical properties of the devices at different temperatures the proposed band alignment at Ge/Si interface as well as the current transport mechanism is described. It has also been shown that the interface traps being filled by photo-generated and thermally-generated carriers play a crucial role in obtaining above unity responsivity.

Chapter 6 concludes the dissertation with a brief summary of the key achievements. A brief discussion about proposed future work is also presented in this chapter.

1.5. Conclusions

As discussed in the preceding sections there have been considerable attempts on the Ge/Si integration using different heteroepitaxial growth techniques. Nevertheless, the main challenge is still the large lattice mismatch between the two materials and therefore the high density of dislocations. The combination of using graded buffer layer(s) and the selective growth technique seem to be the most effective way of reducing the density of dislocations. Based on this challenge, the initial steps of investigating Ge-on-Si layers/devices is mentioned to be the characterization of the Ge film and the Ge/Si interface as well as quantifying the threading dislocation density. This could be performed by taking TEM images of the interface and by counting the etch pits after performing shallow wet etch. From a simulation point of view, it would be important to understand and to be able to predict the behaviour of the dislocations by introducing different defect/trap types and densities at the Ge/Si interface.

The other issue that was discussed in this chapter was related to the high temperature growth and/or post growth cyclic thermal anneal for the purpose of reducing the density of defects in the epi-grown Ge film. Such heat treatment would affect the doping profile of the layers which have been made prior to Ge growth. This could be analysed and optimized by obtaining SRP and/or SIMS profiles of different layers before and after the heat treatment.

Regarding the wafer bonding technique, and as mentioned in the previous section, there are few groups/literatures discussing about the normal incident structures. The main fabrication challenge of this approach is mentioned to be the substrate thinning. Analysing the current transport mechanism through the bonded interface is another important question from the electrical/optical performance point of view.

1.6. References

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Chapter 2: Design and simulation of Ge/Si APDs

2.1. Introduction

In optical fibre communication systems avalanche photodiodes (APDs) can be used to improve the optical detection sensitivity because they have an internal current multiplication mechanism. Since silicon is not responsive at telecommunication wavelengths, another material, such as germanium, must be used as an absorber.

Although providing higher sensitivity, APDs suffer from the avalanche multiplication process causing an internal noise related to the ratio of the electron and hole ionization coefficients [1] which limits the performance of the device. APDs made from silicon have a lower multiplication noise than III-V based devices due to the smaller ratio of ionization coefficients of electrons and holes, typically 0.02 compared to 0.4 for InP [2, 3]. However, Si is not able to absorb light at telecommunication wavelengths, unlike smaller band-gap materials such as Ge and InGaAs. Standard InP-based APDs have high multiplication noise and limited gain-bandwidth product (~100 GHz) making them less attractive than silicon devices [4]. Ge on Si is attractive since it is possible to develop an APD based on a complementary metal oxide semiconductor (CMOS) compatible process [5]. APDs using Ge for absorption and Si for charge and multiplication layers are more promising candidates having shown higher GBP [4]. There are two main approaches to realise Ge/Si APDs, namely Ge epitaxy on Si [4] and Ge/Si wafer bonding [6]. In this section, a generalized structure is modelled to help decide the most appropriate fabrication approach and design of structural parameters depending on the APD requirements.

2.2. Design of Ge/Si APD structure

In a SACM-APD, a *pn* junction is required to build the electric field for impact ionization by applying reverse bias voltage to the junction. As mentioned above, it is desirable to design the device in such a way that the multiplication occurs in silicon. Therefore, the *pn* junction should be made in silicon. However, for detection wavelengths beyond that of silicon ($> 1.1\ \mu m$) a germanium layer is used. A schematic of the generalized Ge/Si

SACM-APD structure is shown in Fig. 2-1. The structure consists of a p-doped Ge absorption layer and an n-doped Si multiplication layer, separated by a p-doped Si charge layer, which is used to control the electric field distribution in the device (the *pn* junction). An additional p-type Si layer is introduced between the charge layer and the physical interface in the Ge/Si SACM-APD structure. This layer reduces the interdiffusion of dopants during epitaxy and also separates the charge layer from the interface between the materials which may attract extra charge and therefore reduce the control of the electric field in the multiplication region. The example device is cylindrical (2D) with a diameter of 30 µm and is simulated using the Silvaco TCAD simulation tool [7] under illumination of –30 dBm (which corresponds to 0.1415 W/cm^2) at wavelength of 1.3 µm.

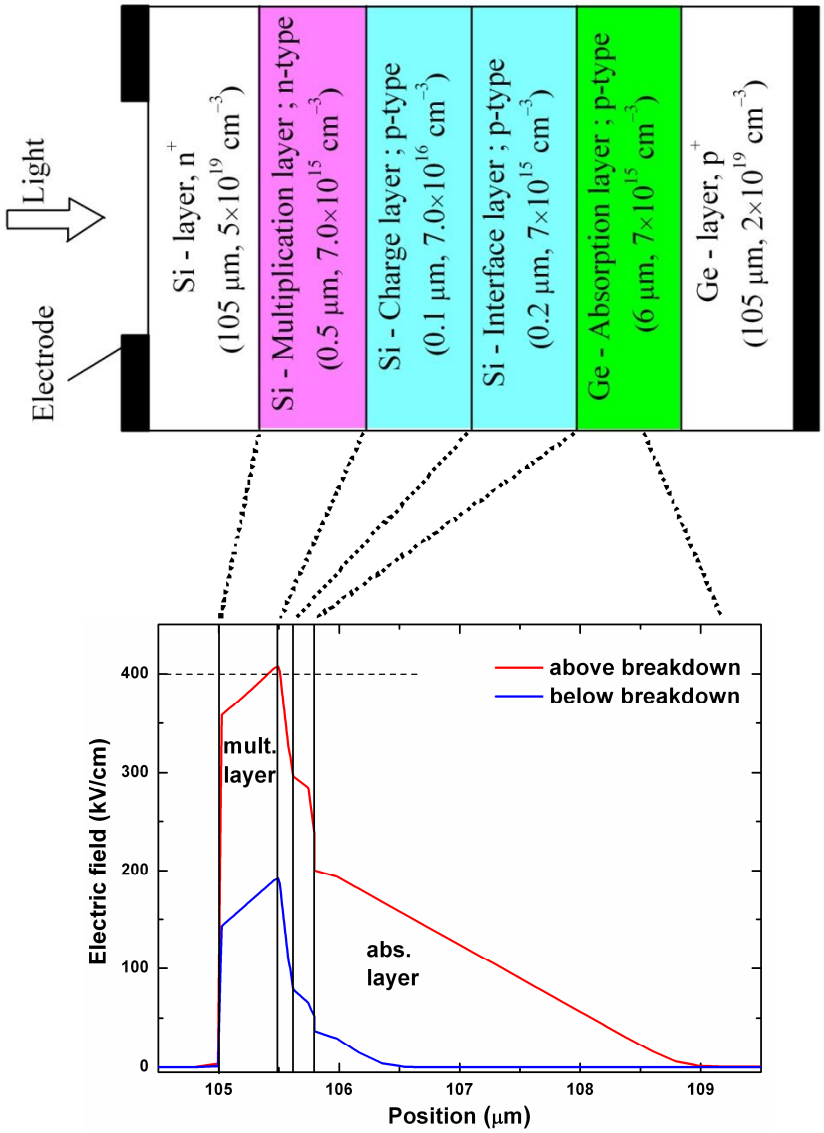


Fig. 2-1. Schematic of the Ge/Si SACM-APD base structure along with the static electric field distribution across the selected regions for two bias voltages.

The static electric field across the APD for two different bias points is shown in Fig. 2-1. For bias voltages below breakdown voltage (blue curve) the electric field in the multiplication region is below the critical value ($E_c \approx 4\times10^5$ V·cm^{-1} in Si [8]) for initialization of impact ionization. By increasing the bias voltage above breakdown (red curve), the electric field distribution over the device is increased particularly in both the multiplication and the absorption regions. As a consequence, impact ionization and avalanching can take place. Higher electric field in the absorption layer will cause the minority carriers to travel toward the electrodes with higher velocity thereby increasing the bandwidth (BW) of the detector.

2.2.1. Gain profile and breakdown voltage

Fig. 2-2 shows the dependence of the gain on applied voltage and on the thickness of the low doped p-type Ge absorption layer. For absorption layer thicknesses less than 6 µm, the breakdown voltage varies significantly (Fig. 2-3), consequently the bias voltage referenced to the breakdown voltage (V_{bd}) of each structure is used ($V_{bias} - V_{bd}$) to allow fair comparison between devices. As shown in Fig. 2-2, by changing the absorption layer thickness, the peak gain and the gain profile change. By increasing the thickness of the Ge absorption layer the voltage drop over this region is increased (see Fig. 2-4), thereby increasing the breakdown voltage. Hence, by optimum design of the absorption layer thickness, the device can show a flat and a more stable gain-voltage profile.

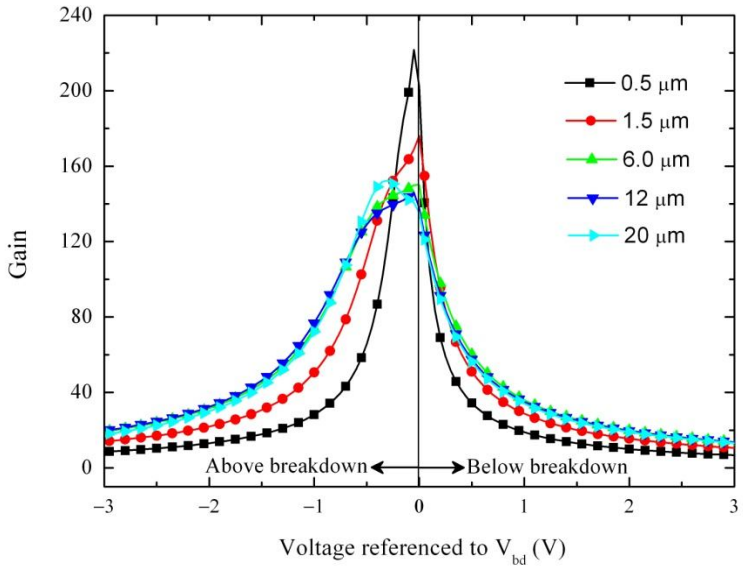


Fig. 2-2. Dependence of the Ge/Si APD gain on the absorption layer thickness.

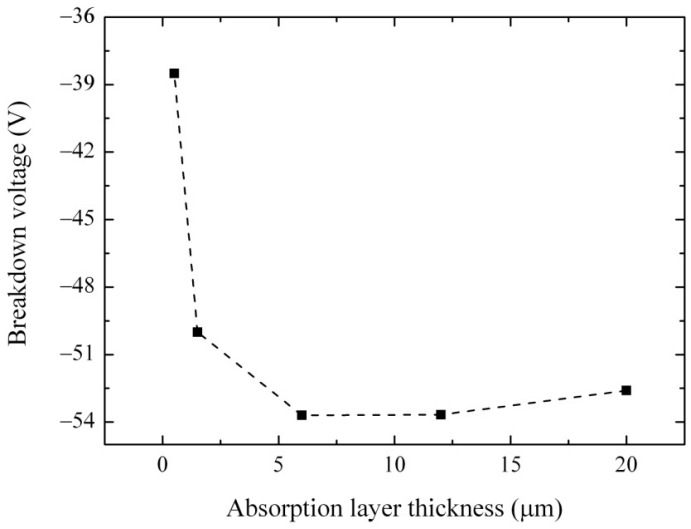


Fig. 2-3. Si / Ge APD breakdown voltage as a function of absorption layer thickness.

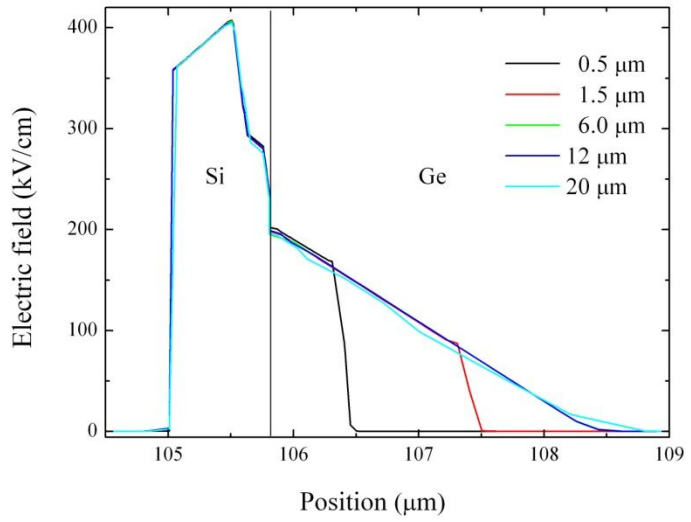


Fig. 2-4. Effects of absorption layer thickness on the electric field across different layers of the Ge/Si APD at V_{bd}.

Fig. 2-5 shows the variation of the APD gain with the p-type doping concentration in a 6 μm thick Ge absorption layer. As shown in Fig. 2-6, for any particular bias voltage a higher-doped absorption layer results in a smaller depletion penetration into this layer. As a result the greatest fraction of the electric field will be inside the multiplication layer. Therefore, the peak of the gain increases (Fig. 2-5) and the breakdown voltage decreases (Fig. 2-7). Because the electric field is concentrated over the multiplication region, any small voltage drop due to high current flow near the breakdown voltage will cause the electric field inside this layer to drop below the critical value for impact

ionization. The electric field reduction in the multiplication region results in a reduction in the gain which in turn will cause the gain-voltage profile to be very narrow. For the case of a lower-doped absorption layer, a portion of the electric field will be distributed across the absorption layer and hence the electric field drop near breakdown will be divided between the absorption and the multiplication layers, thus it will not decrease suddenly in the multiplication region. It is clear from Fig. 2-5 that reducing the doping level of the absorption layer, reduces the dependence of the gain on bias voltage.

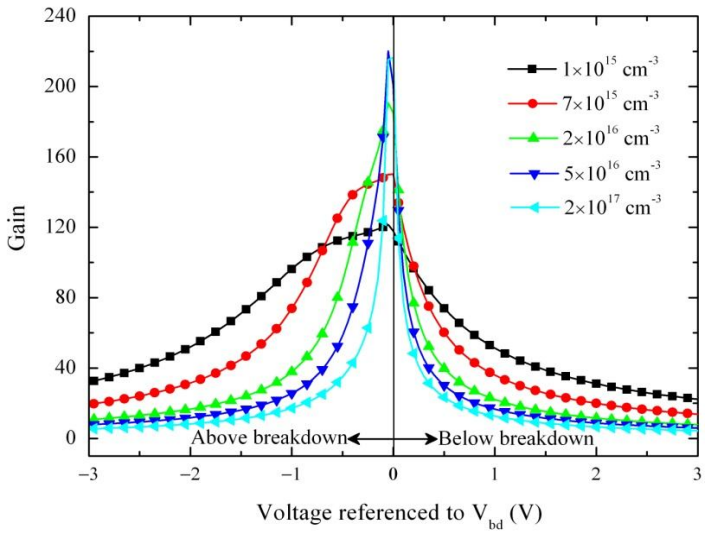


Fig. 2-5. Ge/Si APD gain-voltage profile for different absorption layer doping concentrations. Other structural parameters are the same as Fig. 2-1.

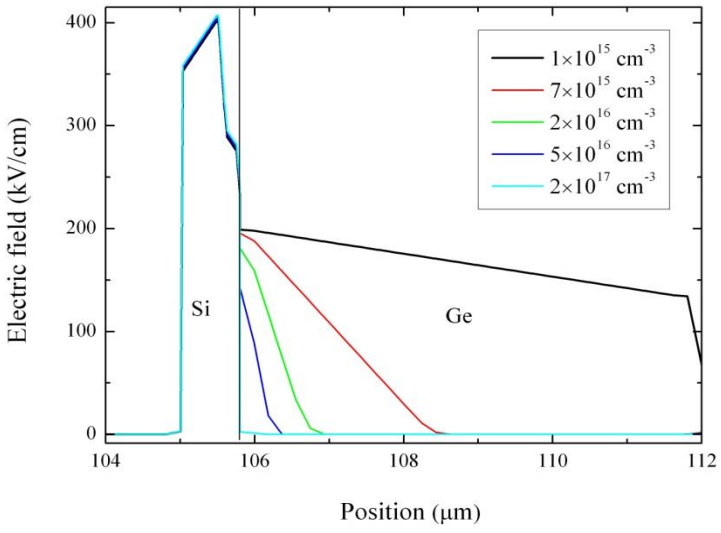


Fig. 2-6. Effects of absorption layer doping concentration on the electric field across different layers of the Ge/Si APD at V_{bd}. Other structural parameters are the same as Fig. 2-1.

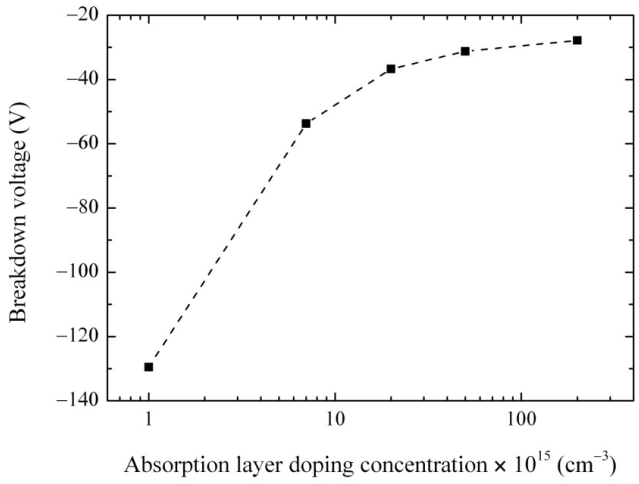


Fig. 2-7. Si/Ge APD breakdown voltage as a function of absorption layer doping concentration. Other structural parameters are the same as Fig. 2-1.

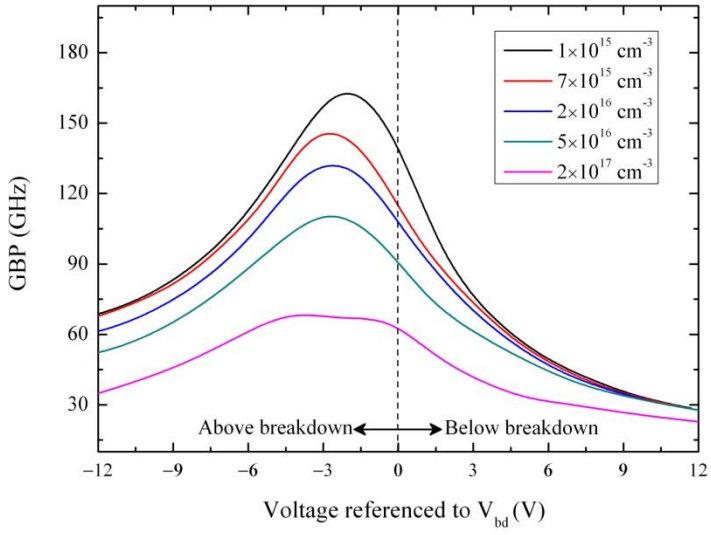
2.2.2. Gain-bandwidth product

The gain-bandwidth product (GBP) of an APD is the product of the APD's bandwidth and its gain. This quantity is commonly specified for APDs, and allows designers to determine the maximum gain that can be extracted from the device for a given frequency (or bandwidth) and vice versa. The frequency response is determined, in the simulator, by changing the frequency of the input ac signal and monitoring the output signal.

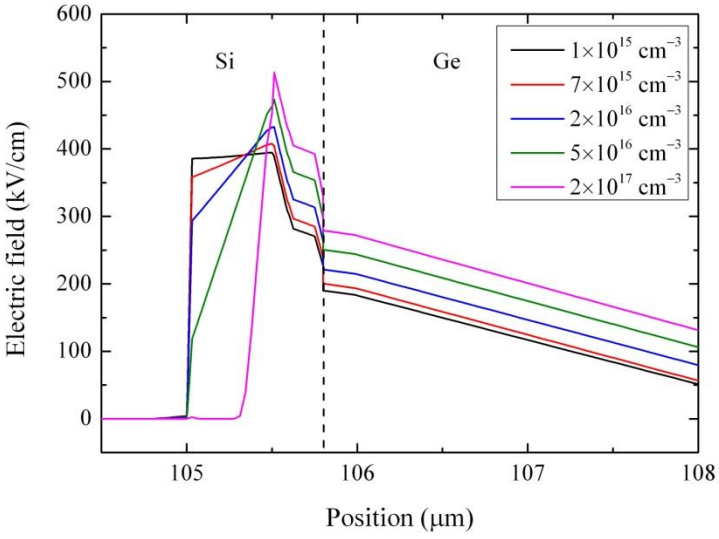
Figs. 2-8(a) and 2-9(a) show the voltage dependence of the GBP versus doping concentration in the multiplication and charge regions, respectively. By increasing the doping level in the multiplication layer the electric field distribution in some parts of this layer decreases dramatically (as indicated in Fig. 2-8(b)). As a result the gain reduces significantly which in turn reduces the avalanche build up time leading to an increase of the bandwidth [9]. However this increase in bandwidth is not enough to prevent the GBP from decreasing.

As illustrated in Fig. 2-9(b), by increasing the charge layer doping concentration the depletion region is kept inside the multiplication layer and the electric field increases. The GBP continues to increase after breakdown up to a point because the decreasing gain causes the bandwidth to increase and compensate the GBP.

Results of this part show how Ge/Si APD's parameters depend on the structural specifications of different layers, and were used to design the structure of the devices which were fabricated and characterized in Chapter 3.

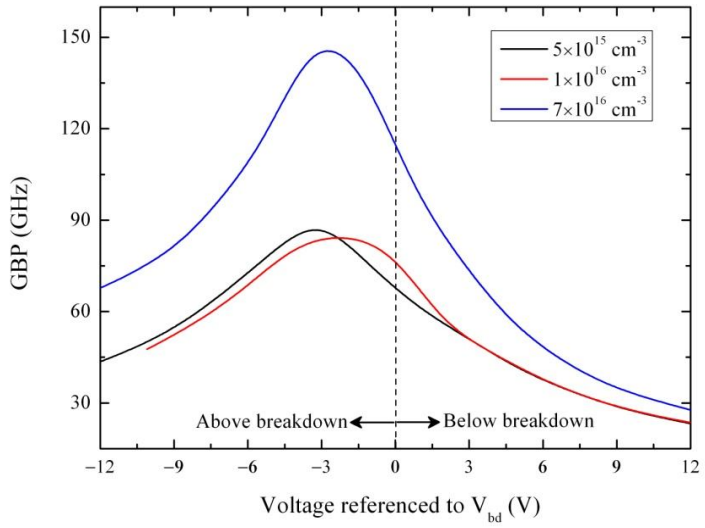


(a)

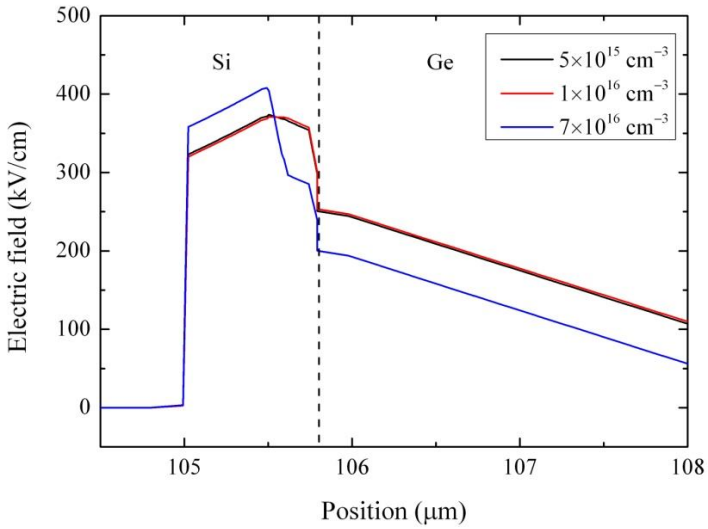


(b)

Fig. 2-8. Dependence of the (a) GBP, and (b) electric field profile of the Si/Ge APD for different multiplication layer doping concentrations. Other structural parameters are the same as Fig. 2-1.



(a)



(b)

Fig. 2-9. Dependence of the (a) GBP, and (b) electric field profile of the Si/Ge APD for different charge layer doping concentrations. Other structural parameters are the same as Fig. 2-1.

2.3. Effects of interface traps

As mentioned before, typically Ge/Si APDs and photodiodes can be fabricated either by epitaxial growth of Ge on Si [10] or by wafer bonding [11]. With epitaxy it is difficult to obtain a high quality Ge layer with sufficient thickness for high absorption because of the 4% mismatch in the lattice constants of Ge and Si [12]. A drawback of wafer bonding can be the formation of a Ge native oxide at the Ge/Si interface [13]. In each

case the electrical and optical characteristics of the APDs are strongly influenced by the heterojunction interface properties, particularly the density of interface traps created by the defects and dislocations caused by relaxation of Ge on Si and/or by the dangling bonds of the Ge native oxide. Experimental and theoretical research reveals that upon exposure of a clean Ge surface to oxygen, a number of defect structures are created, including dangling bonds. It is theoretically predicted and experimentally demonstrated that the dangling bond states are both located in the lower part of the Ge gap centred at energies $E_{acc} = E_v + 0.11$ eV with charge transition neutral/negative (neutral when empty/negatively charged when filled) and $E_{don} = E_v + 0.05$ eV with charge transition positive/neutral (positively charged when empty/neutral when filled) for acceptor and donor interface traps, respectively [14], where E_v is the valence band edge.

The effects of interface traps on the static and dynamic characteristics of Ge/Si APDs based on the one dimensional drift-diffusion model using the Silvaco TCAD tool are presented in this section.

2.3.1. Physics of the model

Based on the simulation results of Section 2.2 the configuration which is schematically illustrated in Fig. 2-10 is considered as the Ge/Si SACM-APD. As mentioned in the previous sections, there is a thin charge layer between the multiplication layer and the absorption layer. This is doped such that one obtains sufficient gain via a high electric field in the multiplication layer while the electric field in the absorber is low enough to ensure carrier drift without multiplication.

Fig. 2-11 shows the acceptor and donor trap centers, whose associated energies lie in the bandgap close to the valence band edge in accordance with published experimental results [15]. Trap centers exchange charge with the conduction and valence bands through the emission and capture of carriers.

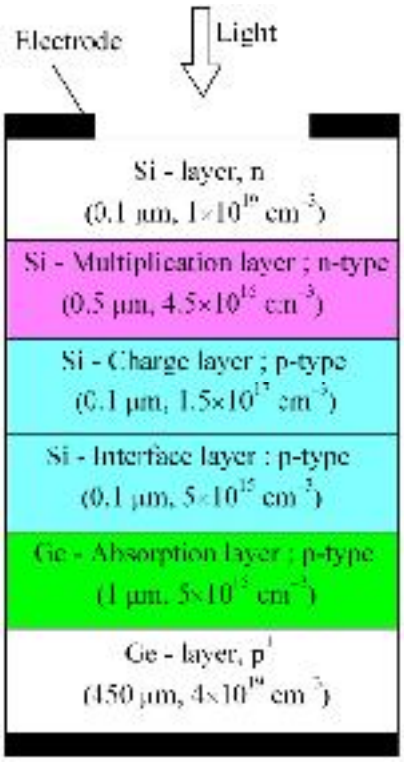


Fig. 2-10. Schematic of the Ge/Si SACM-APD structure modelled in this work.

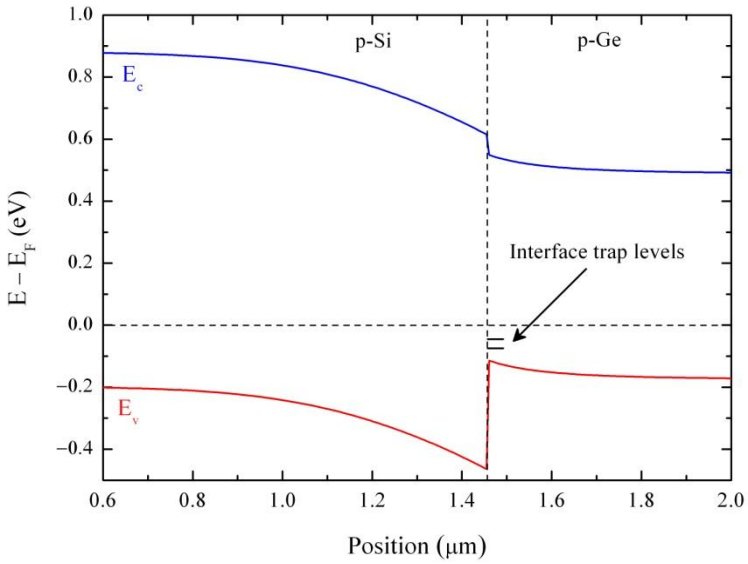


Fig. 2-11. Band diagram and defect levels at p-Si/p-Ge interface at equilibrium (doping concentration is 5×10^{15} cm^{-3} for Si and Ge).

The Ge/Si APD is modeled by solving the Poisson's equation coupled with the charge continuity equations. In this model the total charge, Q_T, caused by the presence of traps is subtracted from the right hand side of the Poisson's equation as follows:

$$\frac{\partial E}{\partial x} = \left(\frac{1}{\varepsilon}\right) \cdot \left[q\left(p - n + N_D^+ - N_A^-\right) - Q_T\right], \tag{2-1}$$

where

$$Q_T = q\left(N_{tD}^+ - N_{tA}^-\right). \tag{2-2}$$

In (2-1), n and p are the electron and hole carrier densities, respectively, which are calculated by solving the carrier continuity equations ((2-3) and (2-4)) coupled with current density equations ((2-5) and (2-6)), self consistently:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\frac{\partial J_n}{\partial x} + G_n - R_n \,, \tag{2-3}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\frac{\partial J_p}{\partial x} + G_p - R_p \,, \tag{2-4}$$

$$J_n = qnv_n(E) + qD_n\frac{\partial n}{\partial x} \,, \tag{2-5}$$

$$J_p = qpv_p(E) - qD_p\frac{\partial p}{\partial x} \,, \tag{2-6}$$

where J_n and J_p are the electron and hole current densities, respectively.

N_{tD}^+ and N_{tA}^- in (2-2) are the densities of ionized donor and acceptor traps that are introduced by the following rate equations:

$$\frac{dN_{tD}^+}{dt} = \left[\frac{1}{\tau_p}p\left(1 - \frac{N_{tD}^+}{N_t}\right) - v_{tp}\sigma_p N_{tD}^+ n_i \exp\left(\frac{E_i - E_t}{kT}\right)\right] - \left[v_{tn}\sigma_n n N_{tD}^+ - \frac{1}{\tau_n}\left(1 - \frac{N_{tD}^+}{N_t}\right)n_i \exp\left(\frac{E_t - E_i}{kT}\right)\right], \tag{2-7}$$

$$\frac{dN_{tA}^-}{dt} = \left[\frac{1}{\tau_n}n\left(1 - \frac{N_{tA}^-}{N_t}\right) - v_{tn}\sigma_n N_{tA}^- n_i \exp\left(\frac{E_t - E_i}{kT}\right)\right] - \left[v_{tp}\sigma_p p N_{tA}^- - \frac{1}{\tau_p}\left(1 - \frac{N_{tA}^-}{N_t}\right)n_i \exp\left(\frac{E_i - E_t}{kT}\right)\right], \tag{2-8}$$

where $\sigma_{n,p}$ are the carrier capture cross sections which have the following relation with the carrier lifetime:

$$\tau_{n,p} = \frac{1}{\sigma_{n,p} v_{tn,p} N_t} \,. \tag{2-9}$$

$G_{n,p}$ and $R_{n,p}$ in (2-3) and (2-4) represent generation and recombination processes, such as photoabsorption and impact ionization as well as trap-assisted (Shockley, Read, Hall) recombination (R^{SRH}).

To describe the impact ionization process the Selberherr model, which shows a strong dependence of the impact ionization coefficients on the electric field, is used [16].

Phonon transitions occur in the presence of a trap (or defect) within the forbidden gap of the semiconductor. Therefore, carrier recombination processes such as SRH, given by (2-10) are also included in the model:

$$R^{SRH} = \frac{np - n_i^2}{\tau_n\left[p + n_i \exp\left(\frac{E_i - E_t}{kT}\right)\right] + \tau_p\left[n + n_i \exp\left(\frac{E_t - E_i}{kT}\right)\right]}. \quad (2\text{-}10)$$

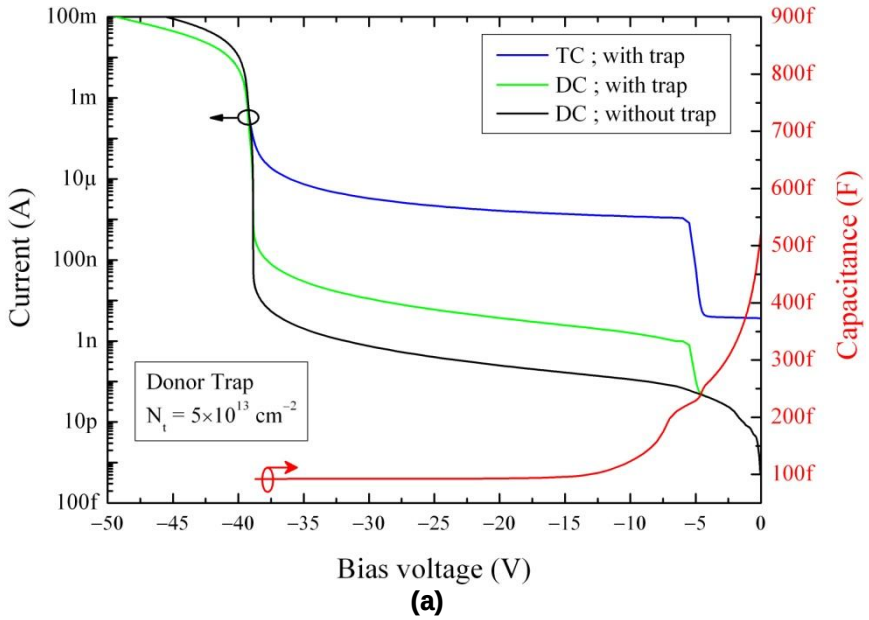
The trap-assisted tunneling process is also considered in the model. However, since this process happens within the region with high electric field (multiplication region) and the fact that the acceptor and donor traps are introduced at the Ge/Si interface, this process does not have any effect on the current-voltage characteristics and the gain of the APD. The Ge/Si band offset (as shown in Fig. 2-11) is also considered in our model. The parameters of the model and their descriptions are listed in Table 2-1.

Table 2-1: Parameters used to model interface traps in Ge/Si APD.

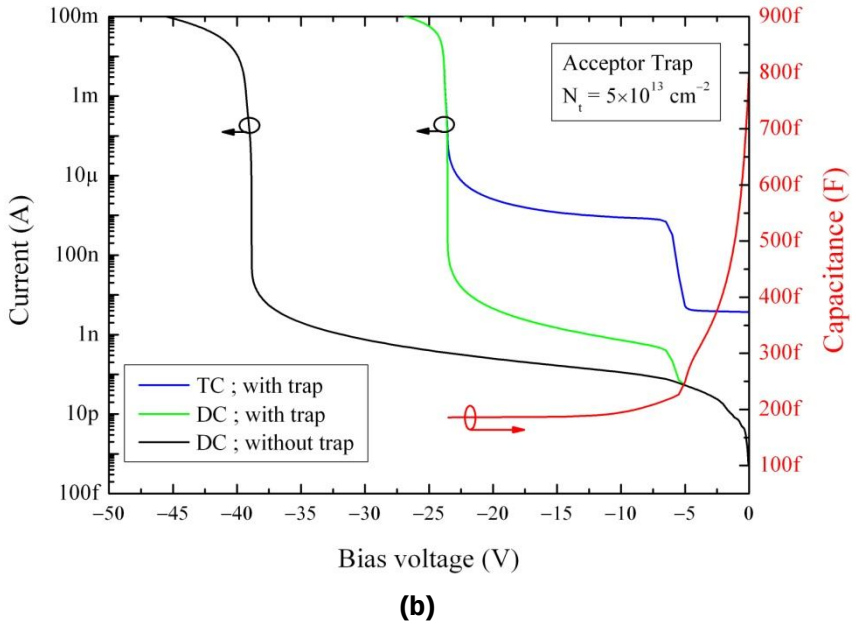
Parameter	Description
E	Electric field
n, p	Electron and hole concentrations
n_i	Intrinsic carrier concentration
N_D^+, N_A^-	Ionized donor and acceptor impurity concentrations
N_{tD}^+, N_{tA}^-	Density of ionized donor and acceptor traps
N_t	Total trap density
Q_T	Total charge caused by traps
τ_n, τ_p	Electron and hole lifetimes
v_{tn}, v_{tp}	Electron and hole thermal velocities
σ_n, σ_p	Electron and hole capture cross sections
v_n, v_n	Electron and hole velocities
D_n, D_p	Electron and hole diffusion constants
E_t	Trap energy level

2.3.2. Electrical characteristics

Fig. 2-12 shows the simulated dark current (DC) and total current (TC) of a circular 30 μm-diameter APD (area: 7.07 × 10^{-6} cm^2) versus bias voltage at room temperature under an input optical power of −30 dBm (which corresponds to 0.1415 W/cm^2) at 1310 nm. As the reverse bias applied to the device increases, the depletion region expands into the Ge region. The density of traps is extracted from ref 14 of this Chapter.



(a)



(b)

Fig. 2-12. *I–V* and *C–V* characteristics of Ge/Si APD with (a) donor traps (N_t = 5×10^{13} cm^{-2}), and (b) acceptor traps (N_t = 5×10^{13} cm^{-2}). Dark current of an ideal APD is also shown.

The APD breakdown voltage (V_{bd}) is defined as the reverse bias voltage at which the dark current is 10 μA [4]. The dark current for the APD device without any traps is 2 nA at a bias equal to 90% of the breakdown voltage (V_{bd} = −38.88 V). For acceptor trap density of 5×10^{13} cm^{-2} the dark current increases to 30 nA at 90% of the breakdown voltage (V_{bd} = −23.55 V). This is due to the generation-recombination current produced by traps at the Ge/Si interface [17].

Comparing Figs. 2-12(a) and 2-12(b) also highlights that it is the acceptor traps that influence the breakdown voltage most. This is explained as follows: both the donor and acceptor trap energies are very close to the valence band below the Fermi level (see Fig. 2-11) and therefore the traps are mostly occupied. A donor trap is neutral when filled (un-ionized) but an acceptor trap is negatively charged when filled (ionized) and a buildup of this interface charge, as described in [14], will influence the electric field resulting in a lower breakdown voltage. Fig. 2-13 illustrates the variation of the APD breakdown voltage with different acceptor trap densities at the interface.

The *C–V* characteristics of the device illustrated in Figs. 2-12(a) and 2-12(b) show that the absorption layer is fully depleted and the device capacitance decreases to a constant value of ~92 fF at 90% of the breakdown voltage for the APD without interface traps. Acceptor interface traps cause the device capacitance to increase to ~186 fF at the same bias voltage, which affects the RC time constant and hence the bandwidth of the APD.

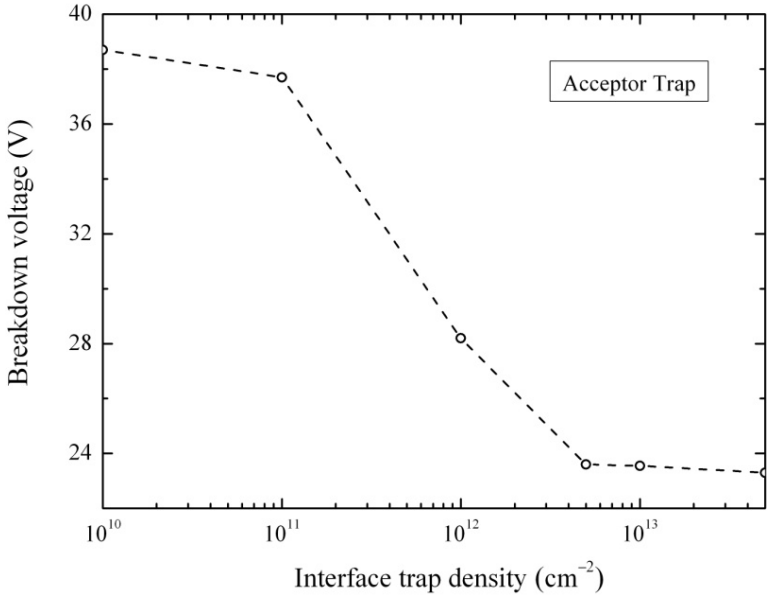


Fig. 2-13. Effects of acceptor trap density on the Ge/Si APD breakdown voltage.

The influence of electron capture cross sections of donor and acceptor traps on the *I–V* characteristics of the Ge/Si APD is shown in Figs. 2-14 and 2-15. According to (2-9), the larger the carrier capture cross section, the smaller the carrier lifetime, and therefore the greater the dark current.

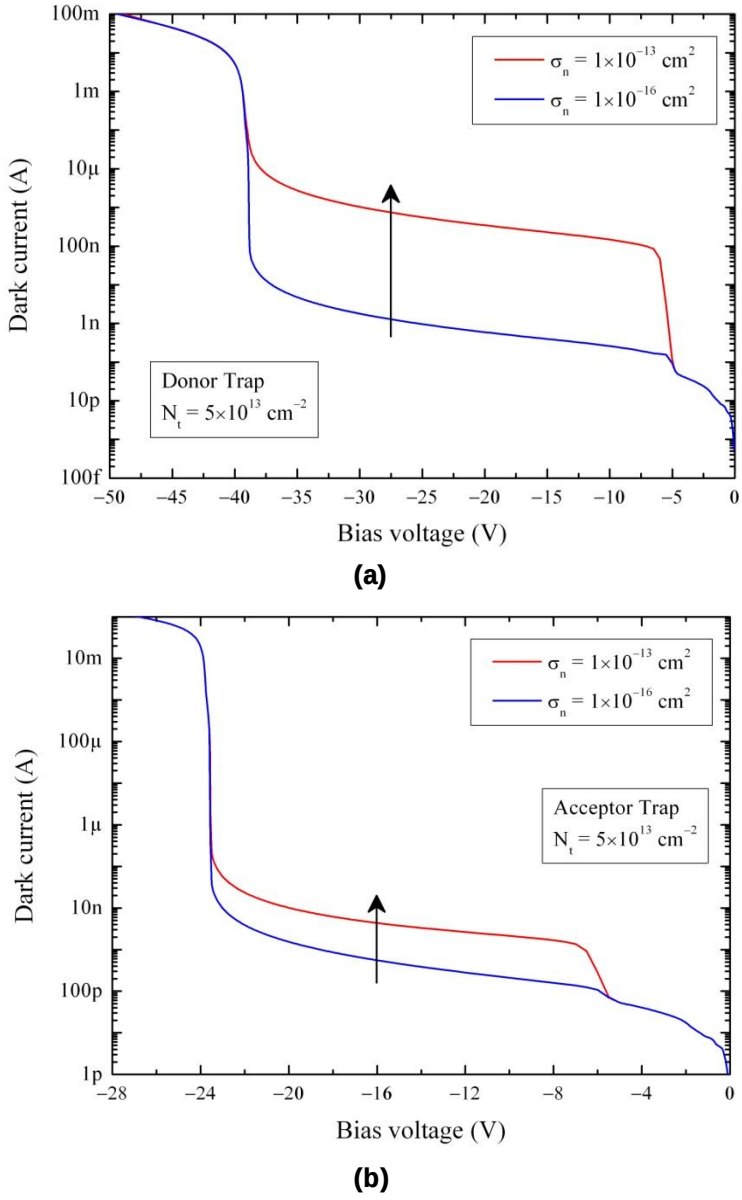
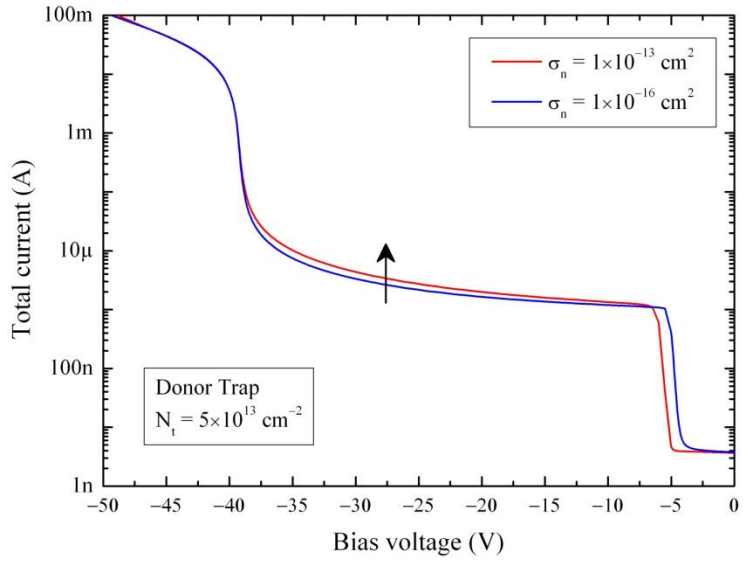
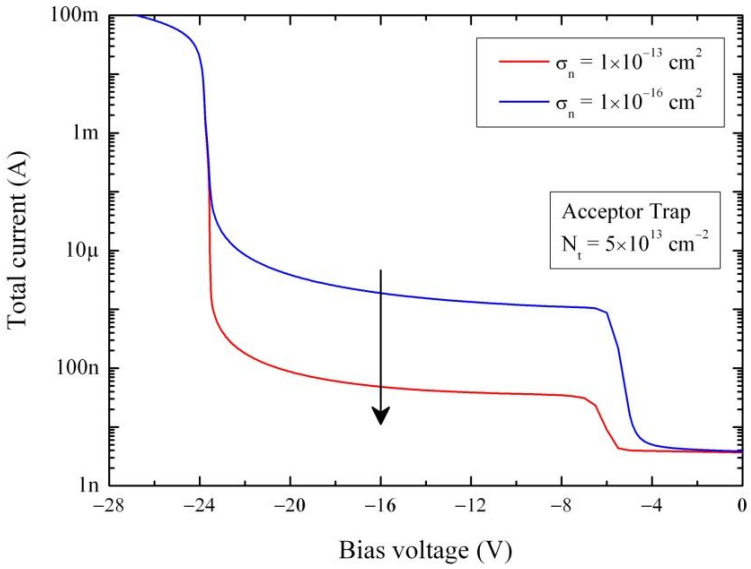


Fig. 2-14. Effects of electron capture cross sections on the dark current for (a) donor type and (b) acceptor type traps. $N_t = 5\times10^{13}$ cm^{-2} for all cases.

Generally, the effects of hole capture cross section of the interface traps on the APD *I–V* characteristics are less since by applying the reverse bias to the device, the photo-generated electrons in the germanium absorption layer move toward the multiplication region through the material interface while the holes move away from the interface towards the anode. Therefore, the hole capture cross section does not affect the *I–V* curves.



(a)



(b)

Fig. 2-15. Effects of electron capture cross sections on the total current for (a) donor type and (b) acceptor type traps. $N_t = 5\times10^{13}$ cm^{-2} for all cases.

The effects of electron capture cross section on the dark current is more considerable for donor type traps compared to acceptor type traps; e.g. the dark current increase from 2 nA to 2.71 µA at 90% of V_{bd} when a donor type trap with $\sigma_n = 1\times10^{-13}$ cm^2 is introduced. Equations (2-9) and (2-10) show that the different trap energies for donors and acceptors combined with different carrier concentrations at the interface result in different recombination rates for the same electron capture cross section.

When the light is switched on, the photo-generated electrons inside the Ge layer pass

the interface where the donor traps are full with electrons (and therefore neutral) and the acceptor traps are ionized. For the donor traps, the trap state acts as a generation center and, as can be seen in Fig. 2-15(a), the total current increases slightly with carrier capture cross section. While for the acceptor case, the trap state acts as a recombination center where the recombination rate increases with electron capture cross section and the total current decreases with electron cross section.

It can also be seen in Figs. 2-14 and 2-15 that the effects of interface traps are observed after the punch through voltage for each device where the depletion region expands into the germanium passing the material interface. This is why a step in the dark current is observed.

2.3.3. Electric field profile and carrier concentration

The electric field distribution across the device is illustrated in Fig. 2-16 for an ideal APD, an APD with donor traps at the interface and for an APD with acceptor traps. The electric field distribution across the device is the same for the ideal APD and the APD with donor traps. Hence, the influence of different acceptor trap densities is considered in this figure.

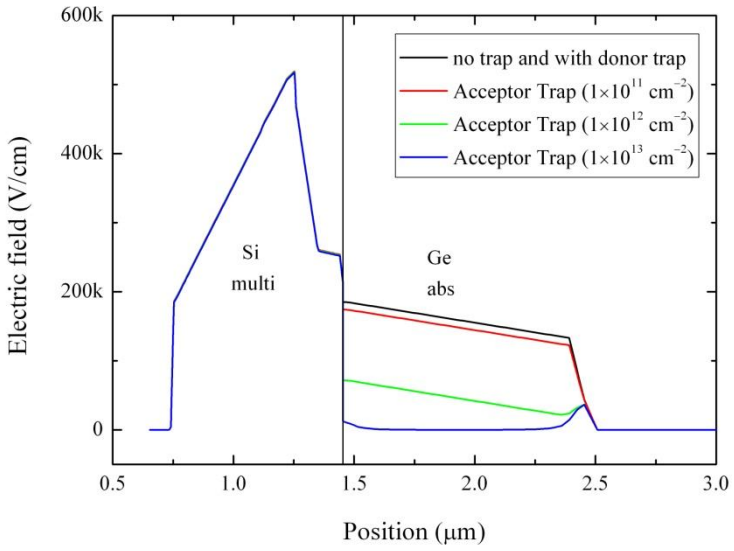
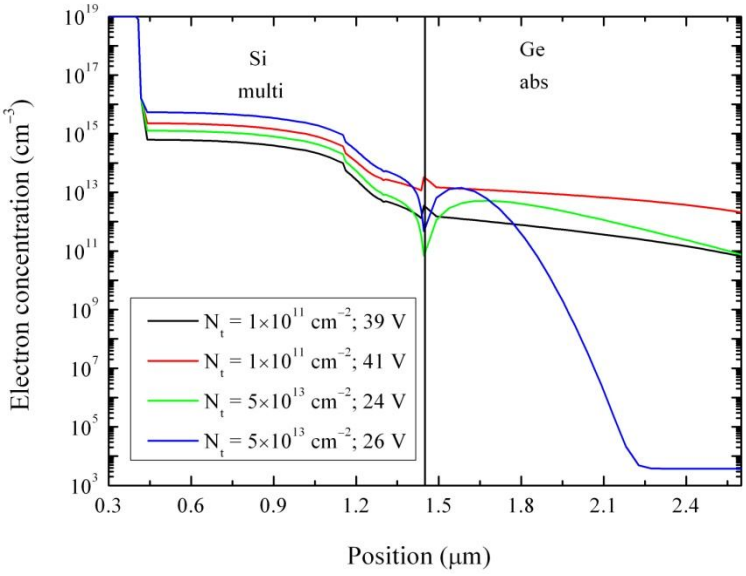
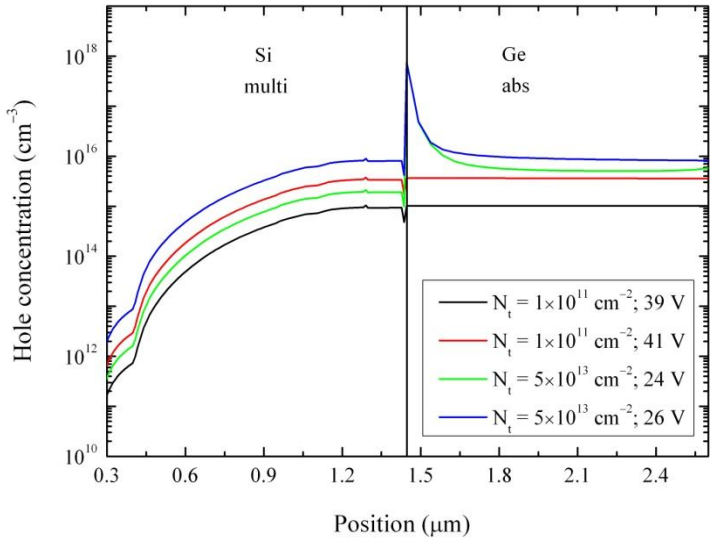


Fig. 2-16. Electric field distribution across the Ge/Si APD at breakdown voltage for no traps and donor traps (N_t = 5×10^{13} cm^{-2}), and for acceptor traps at the interface with different densities. The electric field in the silicon multiplication region is high enough for impact ionization to occur.

The electric field inside the silicon multiplication region must be above the critical value of 4×10^5 V/cm to initiate an avalanche. As can be seen in this figure due to the presence of acceptor traps and by increasing the trap density the electric field level inside the Ge absorption layer reduces to levels even below 100 kV/cm and drops considerably at the material interface. As a result a greater fraction of the electric field will be inside the multiplication layer and, hence, the impact ionization process initiates at smaller bias voltages which in turn shifts the breakdown voltage (see Fig. 2-13).



(a)



(b)

Fig. 2-17. Effects of acceptor trap densities on the (a) electron concentration, and (b) hole concentration across the Ge/Si APD at different bias voltages.

The distribution of electron and hole concentrations across the device is shown in Fig. 2-17 for acceptor traps. Due to the electrons captured by the acceptor traps, Q_T in (2-1) increases and at equilibrium in the steady state condition, where the gradient of the electric field as well as the density of ionized donor and acceptor impurities are constant, this increase in Q_T is compensated by an increase in hole concentration and a decrease in electron concentration. Therefore, as can be seen in Fig. 2-17, the hole concentration increases and the electron concentration decreases in the region where the traps are situated. In the case of the donor traps, they are already filled with electrons and therefore neutral and do not affect the charge in (2-1).

2.3.4. APD gain

The photo-multiplication factor $M_{Ph}(V)$ or APD gain at a particular voltage V is defined as the multiplied photocurrent, I_{MPh}, divided by the photo-current, I_{Ph}, at low voltages where no carrier multiplication takes place [18]:

$$M_{Ph}(V) = \frac{I_{MPh}(V)}{I_{Ph}}. \tag{2-11}$$

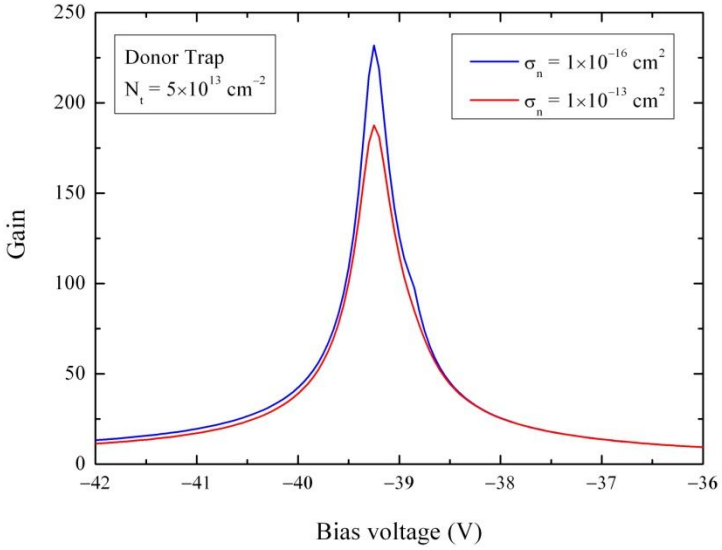
The simulated APD gain can be determined using (2-12) through dividing the calculated photocurrent, i.e. the difference between total current (I_{TC}) and dark current (I_{DC}), by the difference between total current at unity gain ($I_{TC,M=1}$) and dark current at unity gain ($I_{DC,M=1}$) in the device, as follows:

$$gain = \frac{I_{TC} - I_{DC}}{I_{TC,M=1} - I_{DC,M=1}}, \tag{2-12}$$

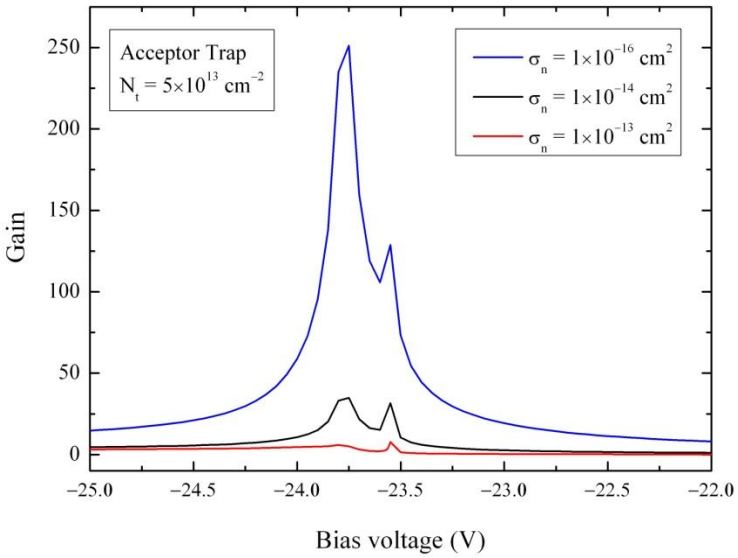
where $I_{TC,M=1} - I_{DC,M=1}$ is defined as the current generated from the photo-absorption in the structure, which takes into account the light reflection at the device surface and layer interfaces, absorption coefficient and absorption layer thickness [8].

Figs. 2-18(a) and 2-18(b) illustrate the gain of the APD showing the influence of interface trap types and electron capture cross sections. According to Fig. 2-18(a), the gain peak reduces by increasing the electron capture cross section; i.e. for $\sigma_n = 1\times10^{-13}$ cm^2 due to the considerable increase in the captured electrons and hence higher dark current (see Figs. 2-14(a) and 2-14(b)), the DC gain of the APD reduces from ~232 for $\sigma_n = 1\times10^{-16}$ cm^2 to ~187 for $\sigma_n = 1\times10^{-13}$ cm^2.

The gain peak reduction is considerable when acceptor traps are included, as illustrated in Fig. 2-18(b). The reason is due to the high recombination rate at the interface due to the presence of acceptor traps. By increasing the electron capture cross section, the recombination rate increases and hence the gain decreases. Since in the Ge/Si SACM APDs electrons initiate the impact ionization process, photo-generated electrons have to pass the material junction and reach the multiplication region and therefore the hole capture cross section has a minor effect on the APD's gain since the holes move away from the interface towards the anode.

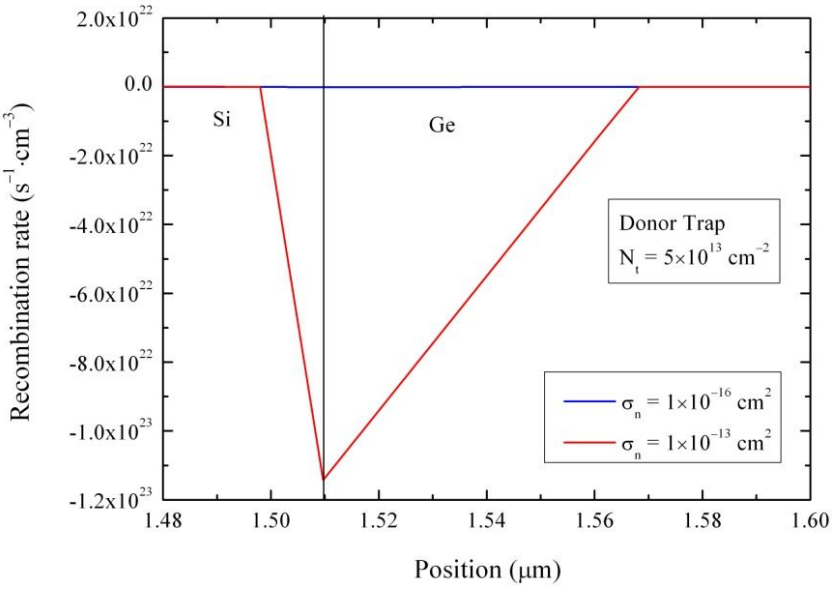


(a)

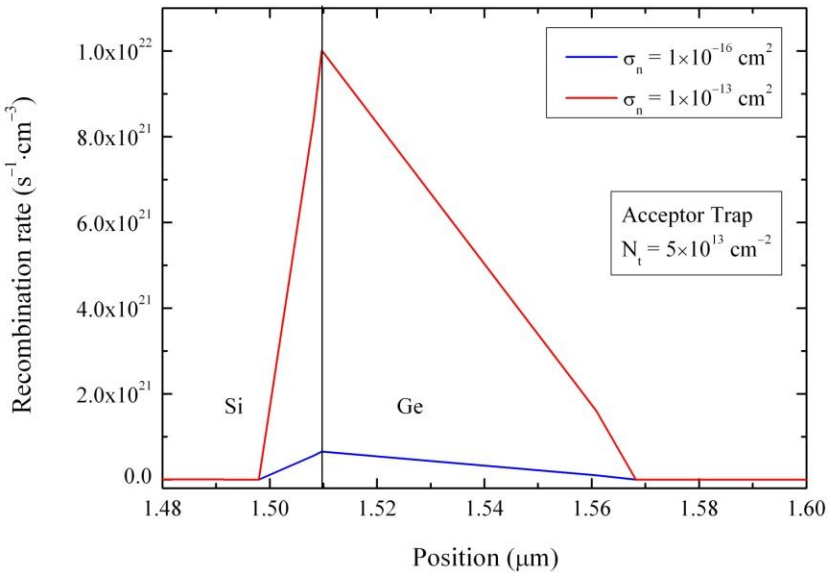


(b)

Fig. 2-18. Gain of Ge/Si APD – comparison between the effects of interface trap types and electron capture cross sections for (a) donor and (b) acceptor traps.



(a)



(b)

Fig. 2-19. Recombination rate profile at the material interface at the bias corresponding to the gain peak for two different trap types: (a) donor traps, and (b) acceptor traps.

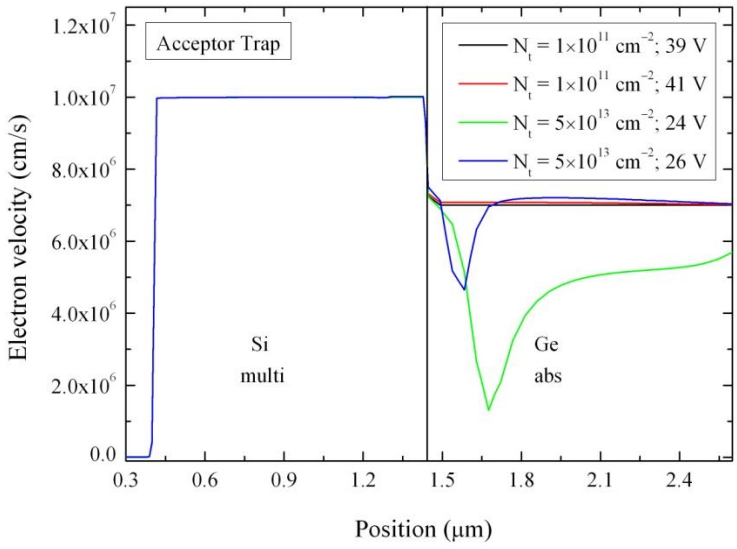
There is an unexpected extra peak in the gain curve which can be explained as follows. From (2-10) we see that R^{SRH} is negative if $n \cdot p < n_i^2$ and is positive if $n \cdot p > n_i^2$. When the APD is reversed biased the depletion region is bereft of carriers. However, the traps

generate a low level of carriers. As the electric field increases multiplication begins to occur and *n* and *p* increase. At some point $n \cdot p > n_i^2$ and R^{SRH} goes positive. The traps now start to act as recombination centers. This reduces the gain until at higher voltages the effect is overcome by the increased multiplication of the photocurrent. This is the cause of the extra peak when comparing Figs. 2-18(a) and 2-18(b). As the voltage is increased beyond this point, the gain increases due to the increasing electric field until the number of carriers in the APD is so high that the gain rolls over due to the inbuilt series resistance of the device and the space charge effect in the multiplication region. This causes a voltage drop between the applied voltage and the junction voltage which is effective for the carrier multiplication [18].

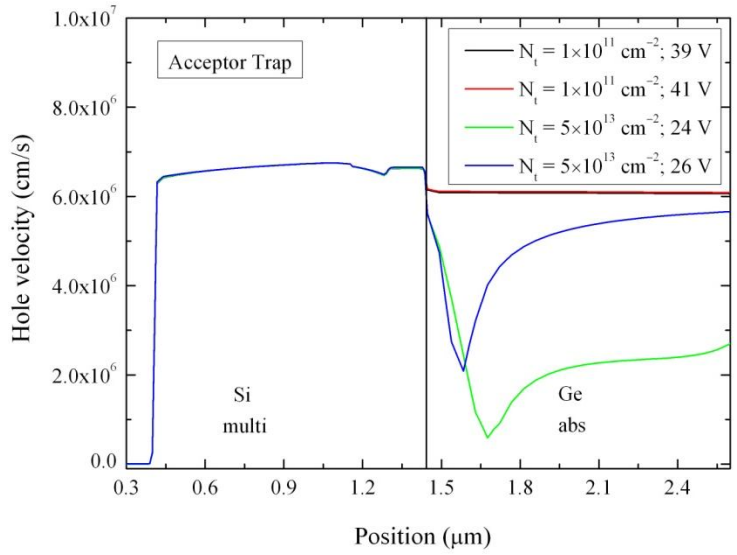
Fig. 2-19 shows the recombination rate for different trap types and electron cross sections at the bias point corresponding to the gain peak. It can be seen that the recombination rate in an APD with acceptor traps for $\sigma_n = 1\times10^{-13}$ cm^2 reaches 1×10^{22} s^{-1}·cm^{-3} while this rate for donor traps considering the same electron capture cross section is -1.2×10^{23} s^{-1}·cm^{-3}. This shows that the donor traps generate carriers while the acceptor traps are doing the opposite at this bias voltage.

2.3.5. Frequency response and gain-bandwidth product

The electron and hole velocities significantly influence the bandwidth of the APD. Therefore, the electron and hole velocities at different bias points across the device for an APD with acceptor interface traps are investigated and shown in Fig. 2-20. It can be seen that for an APD with acceptor trap density of $N_t = 5\times10^{13}$ cm^{-2} the reduction in the electric field (see Fig. 2-16) causes a considerable reduction of the carrier velocities which in turn will increase the transit time of electrons and holes inside the Ge absorption layer and limit the bandwidth of the device. On the other hand, when the acceptor trap density is $N_t = 1\times10^{11}$ cm^{-2} since the electric field inside the Ge layer is higher (see Fig. 2-16), we can see that both the electron and hole velocities have reached their saturation values.



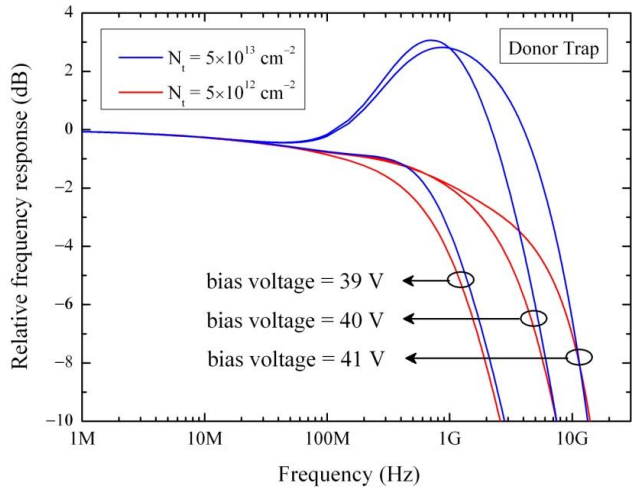
(a)



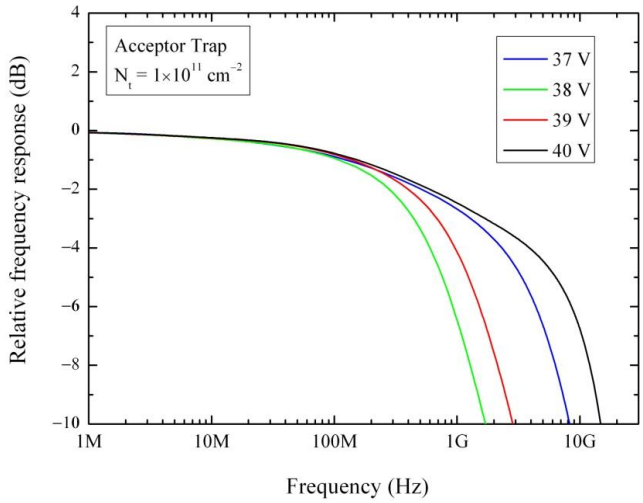
(b)

Fig. 2-20. (a) Electron and (b) hole velocities at different bias voltages considering different acceptor trap densities.

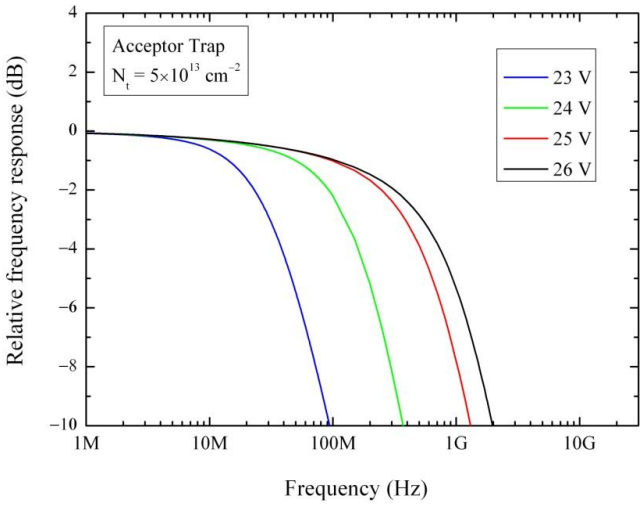
The frequency responses of the Ge/Si APD with different trap types and trap densities are illustrated in Fig. 2-21. Fig. 2-21(a) shows the frequency response of the APD considering two different donor trap densities. The effects of acceptor trap densities of $N_t = 1\times10^{11}$ cm^{-2} and $N_t = 5\times10^{13}$ cm^{-2} at different bias voltages are shown in Figs. 2-21(b) and 2-21(c), respectively. The influences of different donor and acceptor trap densities on the bandwidth of the APD are summarized in Tables 2-2 and 2-3, respectively.



(a)



(b)



(c)

Fig. 2-21. Frequency response at different bias voltages for (a) donor traps, (b) acceptor traps with $N_t = 1\times10^{11}$ cm^{-2}, and (c) acceptor traps with $N_t = 5\times10^{13}$ cm^{-2}. $\sigma_n = 1\times10^{-13}$ cm^2 in all cases.

Table 2-2: Effects of donor trap density on the APD bandwidth.

Density (cm^{-2})	BW (GHz) at bias voltage (V)		
5×10^{12}	0.673 at 39	1.815 at 40	2.721 at 41
5×10^{13}	0.885 at 39	3.467 at 40	6.77 at 41

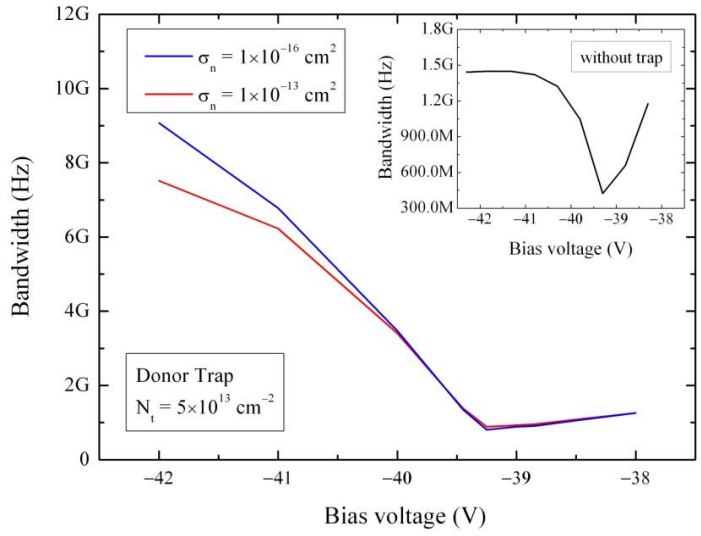
Table 2-3: Effects of acceptor trap density on the APD bandwidth.

Density (cm^{-2})	BW (GHz) at bias voltage (V)			
1×10^{11}	1.29 at 37	0.44 at 38	0.685 at 39	1.7 at 40
5×10^{13}	0.031 at 23	0.125 at 24	0.383 at 25	0.535 at 26

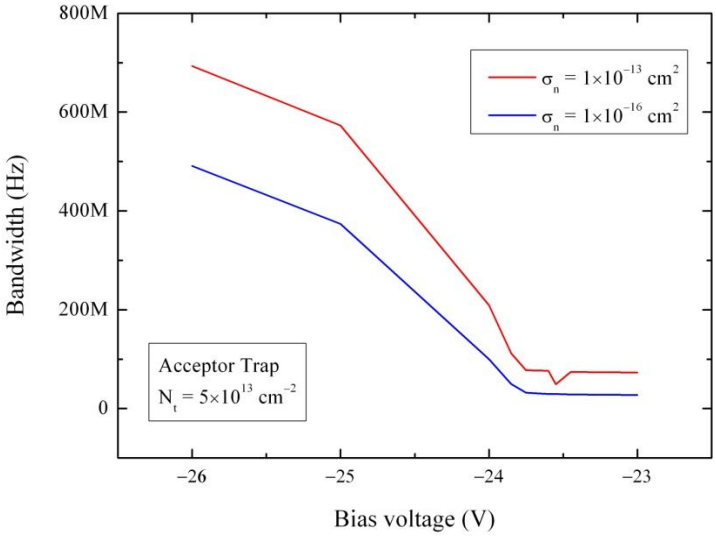
We can see a peaking in the APD bandwidth based on the frequency response shown in Fig. 2-21(a). The reason for this RF peaking is the fact that the donor traps, which are below the Fermi level and very close to the valance band, are full with electrons. These trapped charges change the capacitive and inductive behaviour of the APD particularly at higher frequencies. We believe the interface traps are adding a phase delay and in the case of the donors the phase delay added to the multiplication time and transit time phase delays is sufficient to cause peaking. This requires further investigations. Similar peaking behavior has previously been reported by Dai *et al*. [19], without including the effects of traps.

There are four time constants involved in the response speed of the APD: the depletion layer transit time, the RC time constant, the diffusion time in the un-depleted layer, and the avalanche build-up time. However, traps add capacitance and also alter the carrier lifetimes so it is important to study how this affects the APD bandwidth. Therefore, the effects of electron capture cross section on the bandwidth of the device are investigated and the results are illustrated in Fig. 2-22.

As can be seen in Fig. 2-22, the bandwidth increases after break down due to the reduction in the APD gain and the resulting avalanche build-up time [20]. The inset of Fig. 2-22(a) shows the bandwidth of an ideal APD. The effect of RF peaking for donor traps on the bandwidth is such that the bandwidth increases considerably compared to an ideal APD and reaches above 9 GHz.



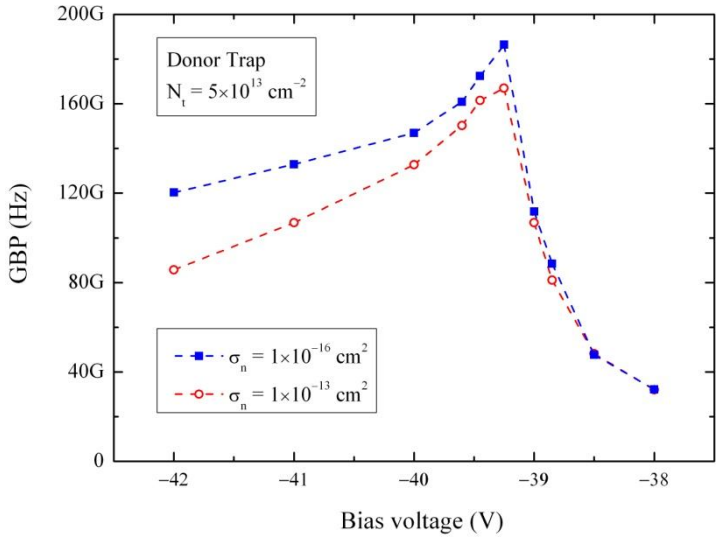
(a)



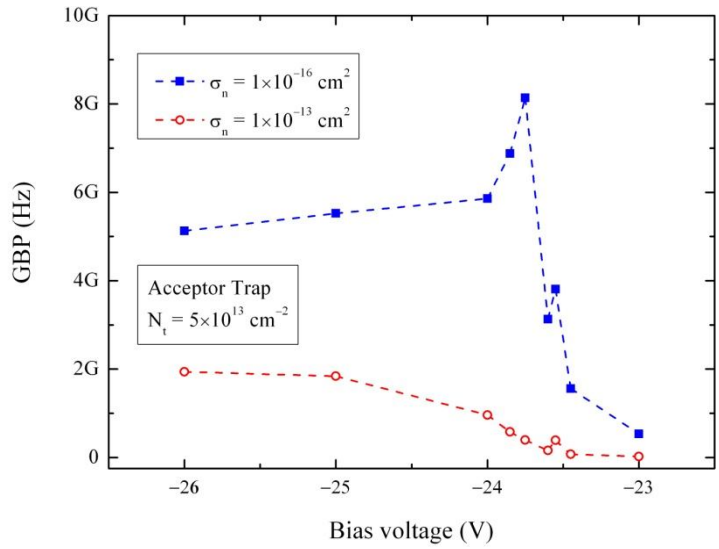
(b)

Fig. 2-22. 3 dB-bandwidth of Ge/Si APD versus bias voltage for different electron capture cross sections for (a) donor traps, and (b) acceptor traps, both with $N_t = 5\times10^{13}$ cm^{-2}. The inset in (a) shows the bandwidth of an ideal APD.

Figs. 2-23(a) and 2-23(b) show the gain-bandwidth product (GBP) of the APDs with donor and acceptor traps, respectively. As illustrated in Figs. 2-18 and 2-22, the APD gain and bandwidth depend on the electron capture cross sections of the traps. Therefore, the effects of electron capture cross sections on the GBP are shown in Fig. 2-23.



(a)



(b)

Fig. 2-23. GBP of Ge/Si APD versus bias voltage for different electron capture cross sections for (a) donor, and (b) acceptor traps.

The GBP increases with gain at low gain values, which shows the nearly constant bandwidth (inset of Fig. 2-22(a)) due to RC and transit time constants. As the gain increases, the bandwidth reduces because of the avalanche build up time. This behaviour is in general due to the trade-off between the gain and the bandwidth [20]. At bias voltages greater than the voltage corresponding to the gain peak, the gain and the multiplication time drop causing a rise in the bandwidth.

2.4. Conclusions

In this chapter the influence of the absorption thickness and doping, along with the charge and multiplication layer doping on the gain-profile, the breakdown voltage and the gain-bandwidth product are determined for the purpose of designing Ge/Si APD. The effects of donor and acceptor traps at the material interface are also modelled for the first time on the SACM Ge/Si APDs characteristics. The influence on the APD breakdown voltage and its *I–V* curve and electric field distribution as well as the gain and GBP is presented.

It is shown that interface traps, particularly acceptor-type traps, have significant effects on the electron and hole concentrations as well as the recombination rate and result in an increase in the dark current. Reduction of electron and hole velocities and increase of the capacitance of the APD due to the presence of interface traps lead to an increase in the RC time constant and hence limits the bandwidth of the APD.

Based on the simulations, the electron capture cross section of the acceptor traps has a greater influence on the APD gain and speed than hole cross sections. It has also been shown that these effects cause a reduction in the APD gain. In contrast, donor traps cause the bandwidth to increase due to the RF peaking at the presence of donor traps.

2.5. References

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Chapter 3: Investigation of photodetectors based on epitaxial Ge on structured Si substrate

3.1. Introduction

There are several types of photodiodes that have been developed for lightwave applications such as photoconductor, metal-semiconductor-metal (MSM), PIN and APD. PIN and APD are the two dominant ones used in the commercially available optical receivers. The PIN photodiode is widely used in optical communication systems due to its low noise, high speed and low dark current. It operates at low bias without internal gain. But for many applications, where very low levels of light are to be detected, photodetectors with high internal gain are desired in order to improve the sensitivity. The high internal gain can be obtained by using APDs. An APD is essentially a reverse-biased PIN photodiode that is operated at voltage close to the breakdown. Photo-generated carriers in the depletion region travel at their saturation velocities, and if they gain enough energy from the electric field during such transit, ionizing collisions with the lattice can occur. The field necessary to produce ionizing collisions is in the range of 10^4 to 10^5 V/cm. Secondary electron-hole pairs are produced in this process. All or some of the primary and secondary carriers may also gain enough energy and produce new carriers. This process is called impact ionization, which leads to carrier multiplication.

Fig. 3-1 shows the schematic drawings of multiplication process for (a) $\alpha \approx \beta$ and (b) $\alpha >> \beta$ where α and β are the impact ionization coefficients of electrons and holes, respectively. The impact ionization coefficients are the reciprocal of the average distance travelled by electrons and holes under the electric field before they impact with the lattice to produce secondary electron-hole pairs. α and β can also be defined as the average number of ionizing evens per unit length. In Fig. 3-1(a), since $\alpha \approx \beta$, the number of secondary electron-hole pairs generated by electrons and holes are roughly equal. In Fig. 3-1(b), since $\alpha >> \beta$, most of impact ionization processes are caused by electrons. α and β are fundamental material parameters but also depend on the electric field through the following formula:

$$\alpha(E) = a_e \cdot \exp\left[-\left(\frac{b_e}{E}\right)^{m_e}\right], \quad (3\text{-}1)$$

$$\beta(E) = a_h \cdot \exp\left[-\left(\frac{b_h}{E}\right)^{m_h}\right], \quad (3\text{-}2)$$

where E is the electric field, a_e, b_e, m_e and a_h, b_h, m_h are materials constants. The electric field required for impact ionization depends on the bandgap energy [1]. Semiconductors with wide bandgaps require high electric fields to initiate the impact ionization process. During the avalanche multiplication process, there are random fluctuations in the actual distance between successive ionizing collisions. These fluctuations give rise to variations in the total number of secondary carriers generated by primary carriers entering into the multiplication region. This leads to noise in the total signal current and the magnitude of the noise depends on the mean avalanche gain.

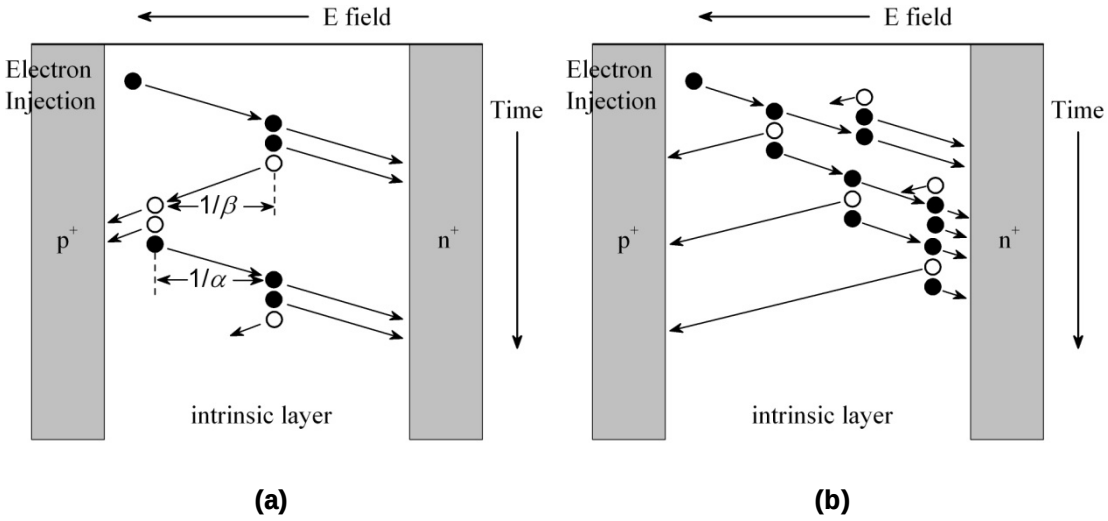


Fig. 3-1: Avalanche multiplication process for (a) $\alpha \approx \beta$, and (b) $\alpha >> \beta$.

The multiplication noise is lower if most of the impact ionization processes are initiated by a single type of carrier with higher impact ionization coefficient. For example, the multiplication noise in Fig. 3-1(b) should be lower than that in Fig. 3-1(a). This is because there is less fluctuation in the ionization process with only one type of carrier participating in the process compared to the case when both electrons and holes are involved.

The avalanche build-up time which affects the bandwidth of the APD depends on the width of the multiplication region and the ratio of the electron and hole ionization coefficients. If $\beta/\alpha \approx 1$, both electrons and holes continuously recycle and persist in the multiplication region which leads to a long response time and low bandwidth. Therefore, an electron-dominant ($\beta/\alpha \approx 0$) or a hole-dominant ($\beta/\alpha \to \infty$) ionization process is desired for a high-bandwidth APD. A thin multiplication region in an APD can also improve the gain-bandwidth-product due to the fact that a narrower multiplication width reduces the effect of carrier feedback for a given gain.

APDs made from silicon have a lower multiplication noise than III-V based devices due to the smaller ratio of ionization coefficients of electrons and holes, typically 0.02 compared to 0.4 for InP [2, 3]. However, the lack of sensitivity of Si to wavelengths beyond 1.1 μm makes this semiconductor unsuitable for photodetection in the 1.3-1.55 μm wavelength range. Presently, full monolithic integration of optoelectronic devices with the Si-based electronics of the optical communications infrastructure has become one of the major focuses of research. Therefore, Si-based optoelectronics and photodetectors in particular, have received considerable attention. Germanium is a viable candidate for integration with Si, given its sensitivity around the 1300-1550 nm wavelength range as well as its compatibility with Si process technologies. A particularly important application is the integration of Ge photodetectors with Si and Si-based electronic devices for the detection of optical signals at wavelengths of 1300 nm and 1550 nm. One option to integrate Ge onto Si is by heteroepitaxy. However, the large lattice mismatch (4%) causes a major problem when Ge is epitaxially grown on Si which is the introduction of a high density of misfit dislocations and threading dislocations in the epilayer. A Ge photodetector with a high threading dislocation density would suffer from large leakage currents, as well as reduced responsivity resulting from carrier recombination at the dislocation defect sites within the Ge layer.

3.2. Layer structure of Ge/Si devices

As discussed in Chapter 2 regarding the effects of different layer properties such as doping concentration and thickness on the APD performance, the layer structure shown in Fig. 3-2 was proposed for our experiments. It was planned to grow the p-type silicon interface layer (see Fig. 2-10) after initial results to reduce the complexity of the physics of the structure and also for the simplicity from a fabrication point of view. The main focus of Chapter 2 was to analyse the issues due to the interface using either

growth or wafer bonding for a general APD device. By growing Si on Ge or Ge on Si, the material interface would not be ideal and defect-free – regardless of which one is grown on the other. Metallurgical junction is also critical in the case of using wafer bonding.

The main difference between Fig. 3-2 and Fig. 2-10 is the substrate. In Fig. 3-2 the substrate is highly-doped n-type Si while in Fig. 2-10 the substrate is p-type Ge. This will not cause any significant difference in the device performance since the electric field drops across the lightly-doped layers (germanium absorption, silicon charge / multiplication layers) and the thickness of highly-doped regions is not critical from a simulation point of view. The main reason for this difference was that our initial goal was to develop the wafer bonding approach and compare the result with epitaxy. And in the wafer bonding technique one of the substrates has to be thinned and based on Tyndall's standard and previously developed recipes for Si dry etching, we simulated the structure based on etching the Si substrate after wafer bonding. As a result in the schematic shown in Fig. 2-10 it is assumed that the Si side of the bonded pair would be etched.

In this structure, the two Si epilayers were grown by the vendor IQE on 4-inch n^+-Si substrates under the following conditions:

- 1st Si epilayer (n-type multiplication layer, phosphorous doped): deposited at 940 °C for 65 s, followed by 60 s stabilization at 940 °C.
- 2nd Si epilayer (p-type charge layer, boron doped): deposited at 940 °C for 13 s.

Both layers are grown at a temperature lower than the standard Si epitaxy due to the following two reasons:

1. the doping gradient from heavily-doped Si substrate to the Si multiplication layer and from the Si multiplication layer to the Si charge layer is significant, and
2. the two layers are thin and the transition region should be very thin as well.

In collaboration with a university in Italy (Politecnico di Milano), the unintentionally doped (UID) epitaxial Ge layer was grown on the HF-dipped structured Si wafers using Low Energy Plasma Enhanced Chemical Vapour Deposition (LEPE-CVD). The advantage of the LEPE-CVD system is its fast growth rate in the range of 4 nm/s to 4.9 nm/s [4, 5]. The growth rates of conventional UHV-CVD or MBE are typically on the

order of a few angstroms per second. The growth rate in our experiment was 4.8 nm/s and the substrate was at the constant temperature of 500 °C. Table 3-1 shows the wafer number corresponding to the thickness of Ge layer. In order to reduce the density of threading dislocations, the wafers were annealed in 6 cycles between 600 °C and 800 °C. The top p^+-Ge layer was deposited at 450 °C with the reduced growth rate of 0.43 nm/s.

Table 3-1: Wafer number and the corresponding Ge layer thickness.

Wafer number	Ge thickness (μm)
8511	1
8515	1.5
8517	4.5
8523	6
8528	8
8536	9

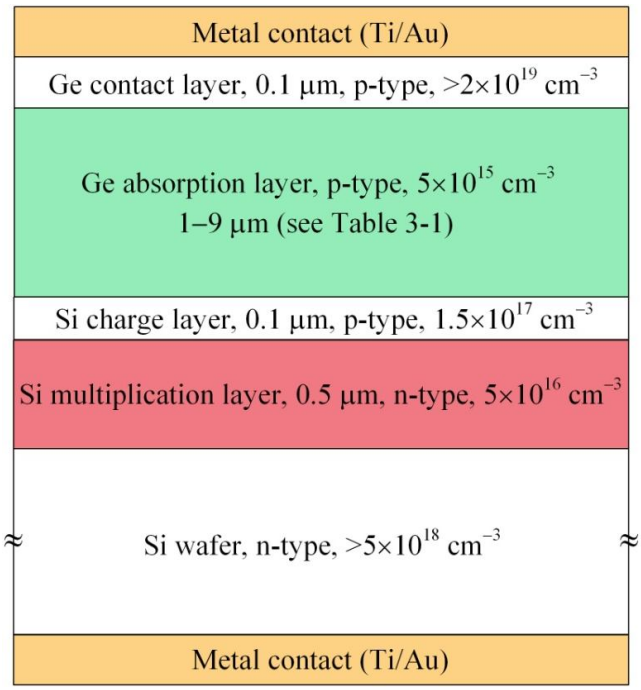


Fig. 3-2. Schematic cross-sectional view of different layers of the epitaxial Ge/Si APDs.

3.3. Material analysis

3.3.1. Ge film characterization

In an epitaxial process the overlayer that is grown on the substrate could have a lattice constant that may differ from that of the substrate (such as Ge/Si epitaxy). One of the requirements for successful epitaxial growth is that the two semiconductors must have nearly identical lattice constants. Since the atoms of the deposited film align themselves to the atoms of the substrate, the presence of any lattice mismatch will create strain in the epitaxial film. As the thickness of the deposited film is increased, the overall strain in the material increases. It is energetically favourable for the material to release the strain by the creation of misfit dislocations when a "critical" thickness is reached [6]. This in turn can also lead to the formation of threading dislocations in the film. The presence of a large number of defects in a semiconductor film would introduce energy states in the material band-gap which can severely degrade device performance by acting as generation/recombination centres.

3.3.2. Quantifying dislocation density

There are three main methods that are most accepted and widely used to determine threading dislocation density: (1) Cross sectional transmission electron microscopy (TEM), (2) defect etching (Etch Pit Density counting), and (3) plan-view TEM. Cross sectional TEM is an excellent way to study the defects in the grown film; however, it is difficult to quantify them due to the small viewing region. In the defect etching method, dislocations are etched at a higher rate than the layer itself, hence the etch pits appear visible using an optical microscope. These etch pits correspond to the dislocations and can be counted to determine threading dislocation density. In the plan-view TEM method, dislocations appear as crystal imperfections in the lattice, and can be counted as well. Threading dislocation density is reported as a density per cm^2. Typical values of threading dislocation density for the germanium on silicon system are in the range of 10^5 to 10^8 cm^{-2} (see Table 1-1). The large range is due to the different methods of growing germanium on silicon and various heat treatments during or after growth. In this study the first two techniques have been used to quantify the density of dislocations in the grown Ge film.

The etchant used for the Etch Pit Density (EPD) counting technique was a mixture of CH_3COOH (67 ml), HNO_3 (20 ml), HF (10 ml), and I_2 (30 mg) [7]. SEM images of the Ge surface after etching were used to count the density of dislocations. Samples with different Ge thickness (wafer number 8511, 8515, 8517, and 8523) showed almost the same threading dislocation density (TDD) of ~1-2×10^7 cm^{-2} which is in agreement with the previously reported TDD using the same growth technique [8]. An SEM image of sample number 8511 (Ge thickness: 1 μm) from wafers grown by LEPE-CVD after shallow etch (10 s) is shown in Fig. 3-3.

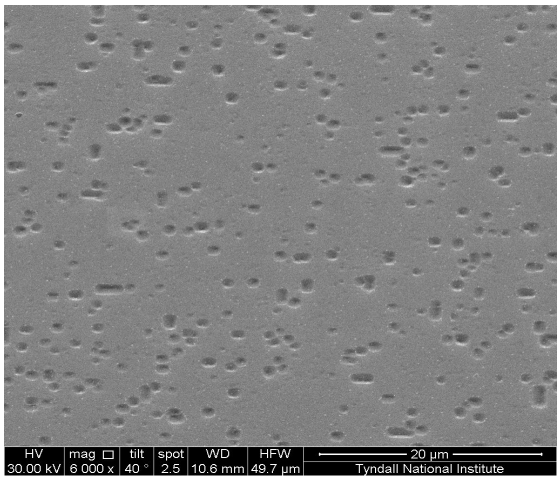


Fig. 3-3. An SEM image of sample number 8511 (Ge thickness: 1 μm) from wafers grown by LEPE-CVD after shallow etch (10 s) for the purpose of EPD counting. The TDD is ~1-2×10^7 cm^{-2}. The scale bar is 20 μm.

To further investigate the quality of the grown Ge film, TEM images were taken from the Ge/Si interface. Fig. 3-4 shows the cross-sectional TEM images at different magnifications. As can be seen, there is no oxide at the interface, however, the effects of stress is quite obvious (periodic gray / black fields at the interface). The spacing between the gray and black fields is not uniform along the interface; however, the length of the black region is ~6 nm and the gray region is ~2.5 nm. The holes at the sidewall (cross section) of the Ge film, shown by red circles in Fig. 3-4, are the dislocations generated at the Ge/Si interface and terminated at the sidewall.

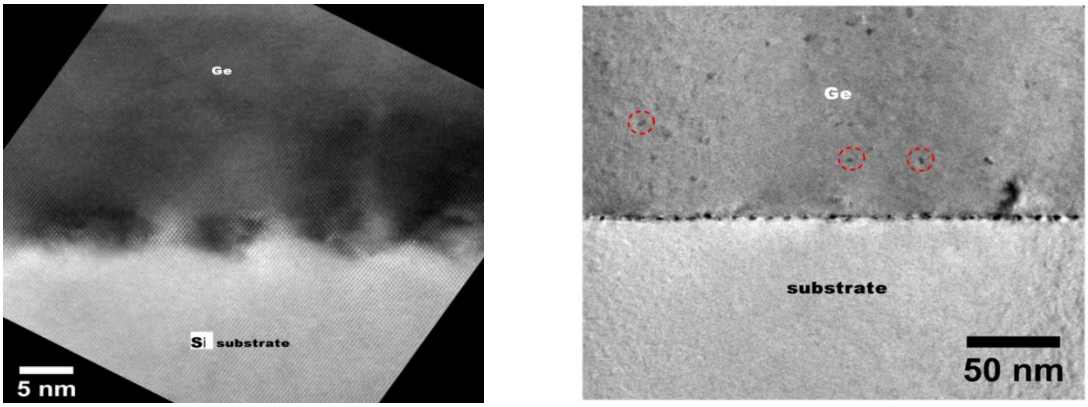


Fig. 3-4. Cross-sectional TEM images of the Ge epitaxial layer directly grown on Si substrate and the Ge/Si interface at different magnifications. Red circles show the dislocations generated at the Ge/Si interface and terminated at the sidewall.

3.4. Doping profile of different layers

3.4.1. Spreading resistance profile

Fig. 3-5 shows the measured carrier profile of wafer number 8511 (Ge thickness: 1 μm) obtained by spreading resistance profiling (SRP) measurement and compares it to the designed profile. A brief explanation of this technique is given in Appendix A2. There is a considerable difference between the actual and desired doping concentration in the charge layer which is probably due to the limitations in Si growth technique. The diffusion of dopant atoms toward the surface of the wafer is also evident which might be due to the Ge growth condition and /or post growth heat treatments.

3.4.2. Secondary-ion mass spectrometry result

Figs. 3-6(a) and 3-6(b) show the concentration of arsenic (As) and boron (B) and the intensity of Si, Ge and Ga in different layers of sample number 8515 (Ge thickness: 1.5 μm), respectively, by Secondary Ion Mass Spectrometry (SIMS). The main difference of the doping concentration shown in Fig. 3-6(a) with reference to the designed level shown in Fig. 3-5 is the doping levels of the *p* and *n* sides of the *pn* junction inside Si (shaded region in Fig. 3-6(a)). The reason for the reduction in the boron doping level in the silicon charge layer might be due to the diffusion of dopant atoms. This is crucial for the device performance, since it greatly affects the electric field profile across the device and therefore changes the device characteristics.

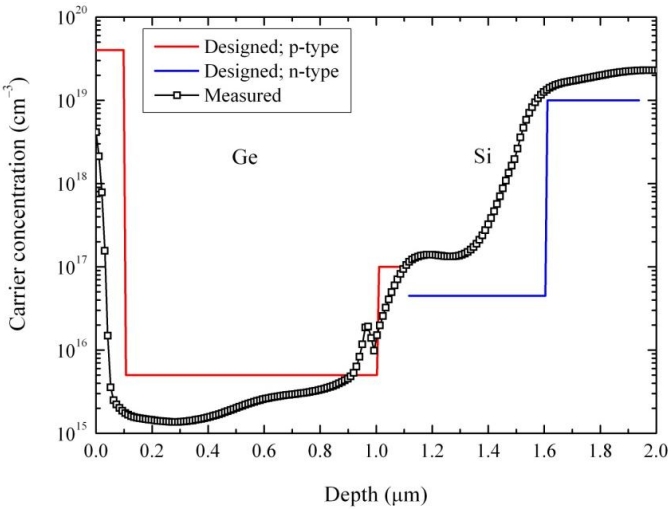
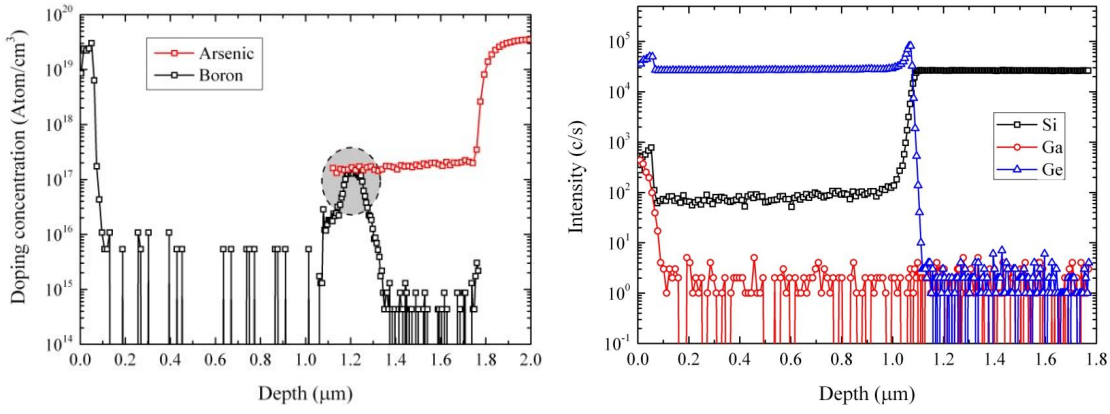


Fig. 3-5. SRP result of wafer number 8511(Ge thickness: 1 μm). Black dots are the measured data; Red line shows the designed doping level in the p-type layers; Blue line shows the designed doping level in the n-type layers.

Fig. 3-6(b) shows the ion intensities of Si, Ga and Ge in different layers of sample number 8515 (Ge thickness: 1.5 μm). An interesting point is that there is an almost constant level of Si in the grown Ge layer (more than two orders of magnitude less than the intensity of Ge), which might be an indication of another approach to compensate the lattice mismatch between Si and Ge for epitaxial technique. As mentioned in Chapter 1, different approaches have been reported to reduce the effects of this mismatch. However, in any of them a constant level of Si is not mentioned.



(a) **(b)**

Fig. 3-6. (a) As and B doping concentrations, and (b) Si, Ge and Ga intensity at different layers of wafer number 8515 (Ge thickness: 1.5 μm). These results are obtained by SIMS measurement. The difference in doping concentration (shaded region in part (a)) with reference to the designed level (Fig. 3-5) is crucial since it greatly affects the electric field profile across the device and therefore changes the device characteristics.

Fig. 3-7 compares the SRP result with the SIMS result of sample number 8515 (Ge thickness: 1.5 μm). The doping level of the p^+-Ge contact layer and the Un-Intentionally Doped (UID) Ge absorption layer is almost in the same level as it had been designed. However, there is a significant difference in the dopant atom concentration and the activated dopant atoms in the Si multiplication and charge layers. This might be due to the low temperature silicon epitaxy process. As mentioned before modified epitaxial process was used for silicon epilayers (charge and multiplication layers) due to their thickness and considerable gradient in doping profile in these two layers. As is shown by dashed circle in Fig. 3-7, the actual thickness of the multiplication region based on the SRP result is ~250 nm, almost half of the designed thickness (see Fig. 3-2).

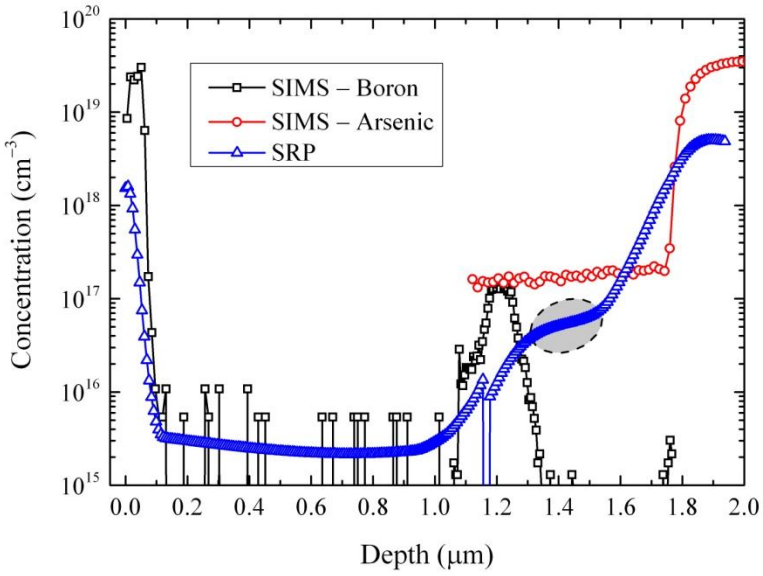


Fig. 3-7. Comparison between the SRP profile (blue triangular symbols) and the SIMS result (black square and red circular symbols for arsenic and boron concentrations) of wafer number 8515 (Ge thickness: 1.5 μm).

In order to eliminate the effects of Ge growth on the diffusion of dopant atoms from Si epilayer(s) into Ge layer (in particular boron of the silicon charge layer), new Si wafers were ordered with modified growth condition. Fig. 3-8 shows the SIMS result of the new Si wafer before Ge growth (un-processed Si wafer; wafer name: UPSW). As can be seen in this figure, the profile of boron is in good agreement with the designed profile (thickness: 100 nm, doping concentration: 1.5×10^{17} cm^{-3}). However, the rise in the profile of arsenic close to the surface does not follow the desired profile. The reason for this is not clear and more growth experiments are required to optimise the silicon epitaxial growth recipe.

In order to determine the effectiveness of the *pn* junction, an SRP measurement was carried out. The results of SRP and SIMS are compared in Fig. 3-9. There is no sign of junction based on the SRP result due to the significant rise in the arsenic concentration at the surface. In order to achieve the designed silicon epilayers in terms of doping level and thickness, a lower growth temperature was used. As a result, the quality of the silicon wafers was poor such that defective regions could easily be noticed on the wafers without even using a microscope. Optical images of the UPSW showing the defects on the surface as well as *I*–*V* characteristics of devices fabricated using this wafer are illustrated in Appendix A3.

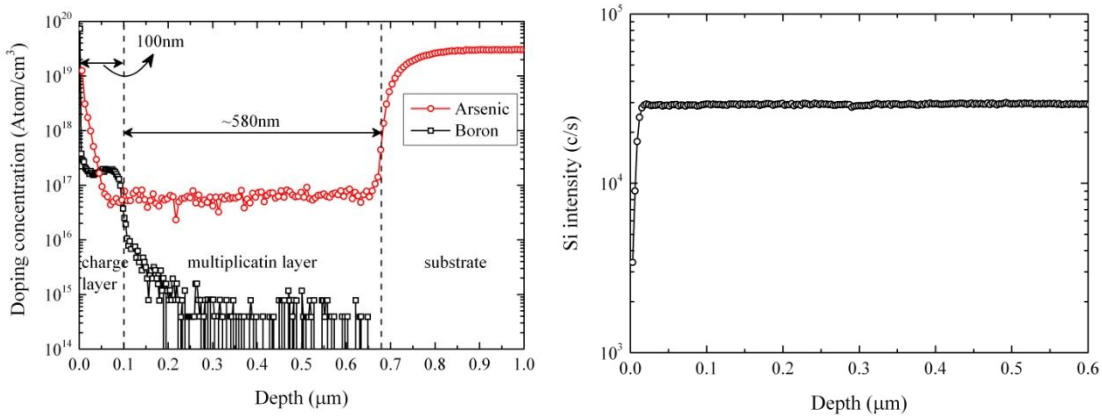


Fig. 3-8. (a) Arsenic and boron doping concentrations, and (b) Si intensity of different layers of UPSW. These results are obtained by SIMS measurement.

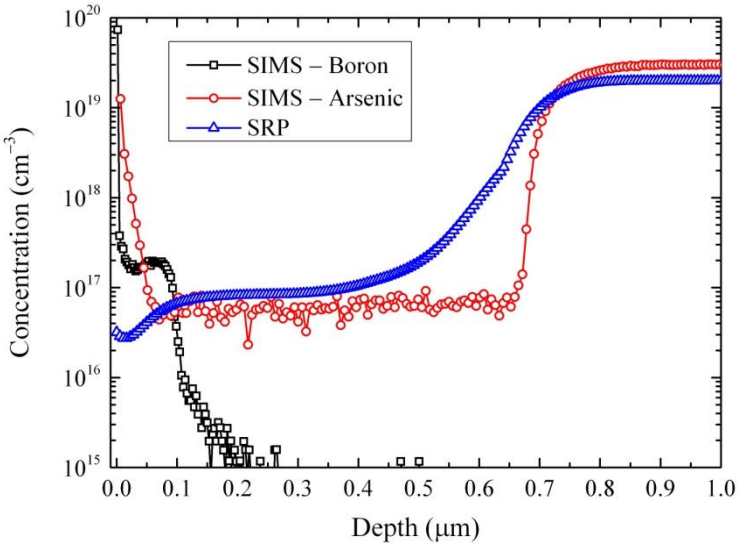


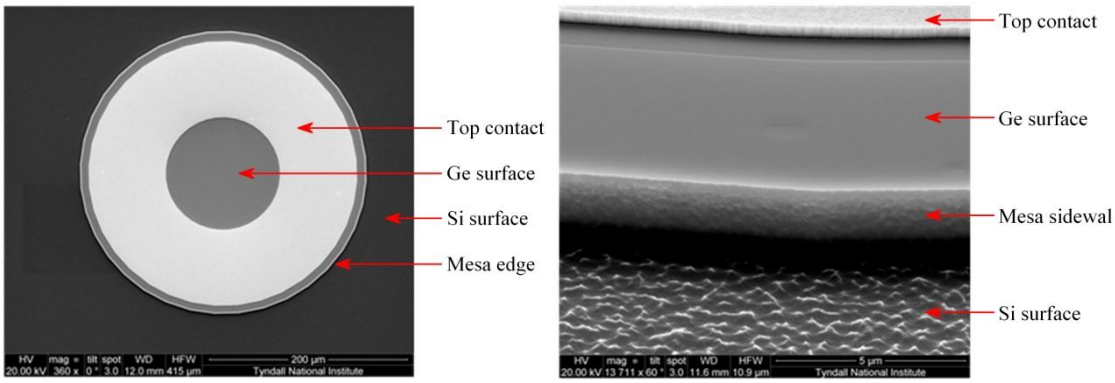
Fig. 3-9. Comparison between the SRP profile (blue triangular symbols) and the SIMS result (black square and red circular symbols for B and As concentrations) of UPSW.

3.5. Mask design

CleWin was used to design the mask for device fabrication. The first level in the mask layout is the top p-metal contact. Different geometries (circular and square) with various diameters (10 μm to 500 μm) and dimensions (100 μm × 100 μm to 500 μm × 500 μm) were considered. The second level is the mesa etch in circular and square geometries. Third level is the pattern to open oxide (which is used for sidewall passivation). The last lithography step is the contact pads.

3.6. Device fabrication

For the purposes of electrical characterization and analyzing the carrier transport, mesa structures with different diameters were fabricated. Ti/Au was used for the p- and n-contacts and deposited by e-beam evaporation and patterned by standard lithography and lift-off process. The mesa structures were then formed by SF_6/C_4F_8 reactive ion etching. Fig. 3-10 shows the top view and side view SEM images of the fabricated Ge/Si device using wafer number 8511 (Ge thickness: 1 μm).



(a) **(b)**

Fig. 3-10. (a) Top view, and (b) side view SEM images of the fabricated Ge/Si devices showing the top contact, mesa edge and sidewall, and Si and Ge surfaces.

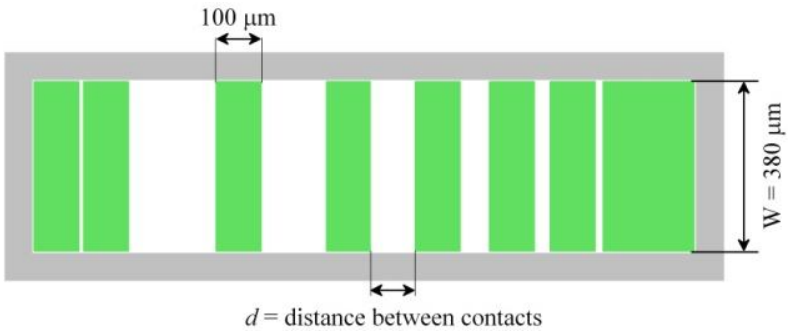
3.7. Electrical characterization

The Transfer Length Method (TLM) is used to obtain the contact resistance. Fig. 3-11(a) shows the TLM pattern and the definitions of contact bar width (W), contact separation distance (d) and the length of the contact stripes. The total resistance (R_T) of wafer number 8511 (Ge thickness: 1 μm) is measured for various contact spacing (d) as shown in Fig. 3-11(b). The following three parameters can be extracted from this measurement [9]:

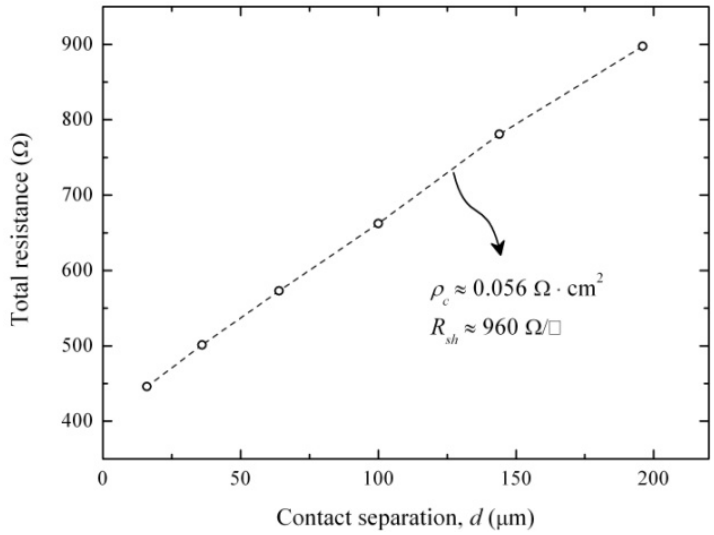
1. The slope $\Delta(R_T)/\Delta(d) = R_{sh}/W$ leads to the sheet resistance with the contact width W independently measured. Hence: $R_{sh} \approx 960\ \Omega/\square$.
2. The intercept at $d = 0$ is $R_T = 2R_c$ giving the contact resistance. Hence: $R_c \approx 400\ \Omega$.
3. The intercept at $R_T = 0$ gives $-d = 2L_T$, which leads to the specific contact resistivity (ρ_c) with R_{sh} known from the slope of the plot. Hence: $L_T \approx 76\ \mu\text{m}$ and $\rho_c = (L_T)^2 \cdot R_{sh} \approx 0.056\ \Omega\cdot\text{cm}^2$.

In summary, we have: $R_T = (R_{sh}/W) \times \text{d} + 2R_c$.

The band diagram of the top Ge and Si layers are illustrated schematically in Fig. 3-12. As is shown in this figure, the exact current path is not clear; i.e. the electrons injected from one of the contacts on top of the sample can either flow just through the first highly doped Ge contact layer, or they can flow to the intrinsic Ge absorption layer beneath the contact layer. In this case the total resistance could be affected by the resistance of this layer. At higher bias voltages, the electrons might also be able to overcome the potential barrier offset between Ge and Si and flow through the lightly-doped Si layer (charge layer). However, due to the *pn* junction in Si (p-type charge and n-type multiplication layers), it is unlikely that the current could flow through the Si multiplication layer. In order to figure out the possible path of current the sheet resistance of the top two germanium layers are calculated based on the resistivity of the layers. The sheet resistance of the top germanium contact layer and the intrinsic absorption layer is ~800 Ω/□ and ~10 kΩ/□, respectively. By comparing these values with the measured data, it can be concluded that the current flows mostly through the top cap layer.



(a)



(b)

Fig. 3-11. (a) A transfer length method test structure showing the definitions of contact metal bar width (*W*), contact separation distance (*d*) and the contact stripe length. (b) Plot of total resistance as a function of contact spacing, *d*, of wafer number 8511 (Ge thickness: 1 μm). The calculated values of sheet resistance and the specific contact resistivity obtained by fitting the curve are also shown in part (b).

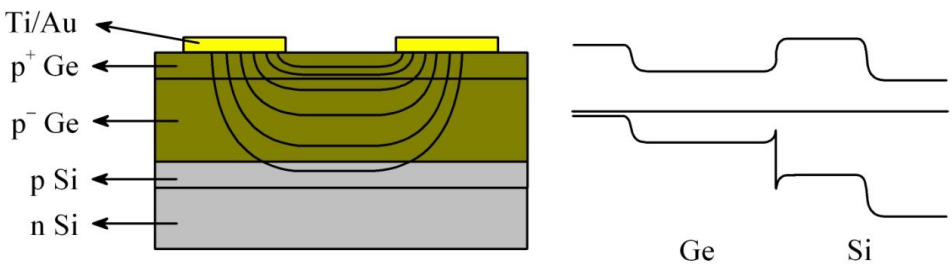
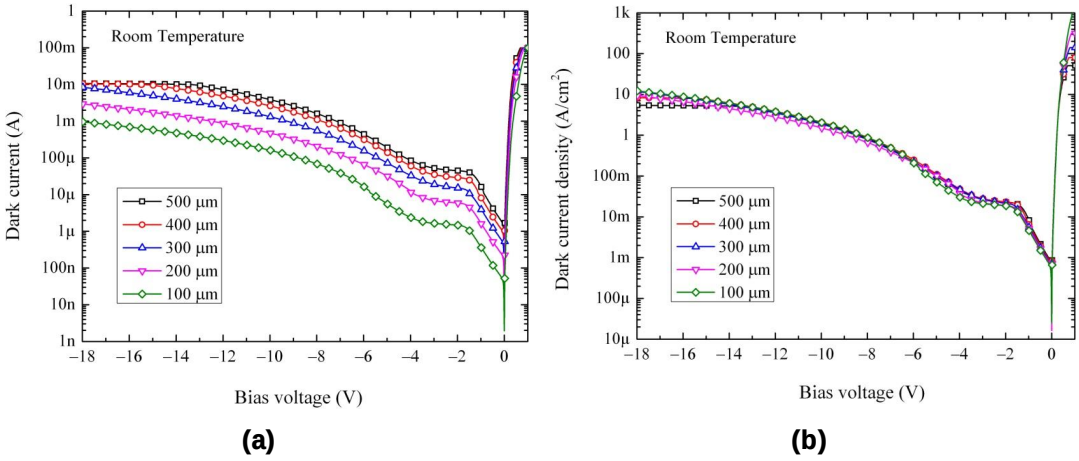


Fig. 3-12. Band diagram of the top Ge and Si layers showing the possible current flow paths.

Fig. 3-13(a) shows the current–voltage (*I–V*) curves of devices with different diameters in semi-log scale. As shown in this figure, the current level even at low bias voltages (–2 < V_{bias} < 0 V) where the electric field is expected to drop in Si multiplication layer is relatively high. Dark current density of the devices is shown in Fig. 3-13(b) where all the curves lie almost on each other. This suggests that the effect of sidewall is not critical at this current level and for such device sizes and that the bulk component is dominant in the leakage current.



(a) **(b)**

Fig. 3-13. (a) Dark current, and (b) dark current density versus bias voltage of Ge/Si devices from wafer number 8515 (Ge thickness: 1.5 µm) with different diameters at room temperature. Bulk component of the current is dominant in the leakage current.

In order to analyze the carrier conduction mechanism, *I–V* measurements were carried out at different temperatures between –50 °C and 20 °C. The results are shown in Fig. 3-14(a). As can be seen in this figure, the reverse current at low reverse bias voltages is temperature dependent while at higher bias voltages it is less temperature dependent. The reverse leakage current at different reverse bias was then fitted to $J = A \cdot \exp(-E_a/kT)$, where J is the diode current density, A is a constant and E_a is the activation energy. E_a was estimated from the slope of the fitted curves. As can be seen in Fig. 3-14(b), the value of E_a at –1 V and –4 V is 0.38 eV and 0.15 eV, respectively. The activation energy decreases with increasing reverse bias voltage. This is consistent with the conclusion that the origin of dark current at low bias voltages is generation through generation / recombination centres, and at higher bias voltages is tunnelling [10].

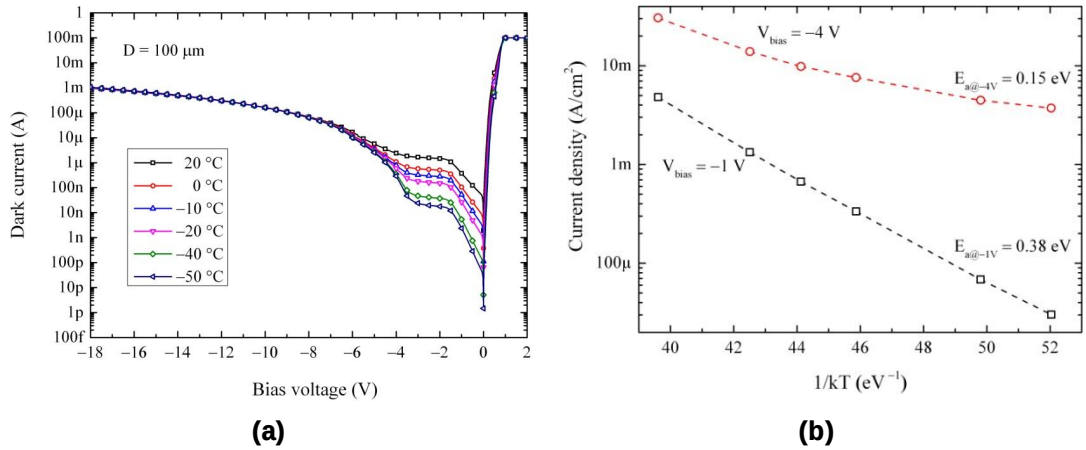


Fig. 3-14. (a) *I–V* characteristics of a 100 µm-diameter Ge/Si device from wafer number 8515 (Ge thickness: 1.5 µm) at different temperatures in dark. (b) Current density versus 1/kT at –1 V and –4 V. The value of E_a at each bias voltage is also shown.

Fig. 3-15(a) shows the effects of temperature on the dark current of the Ge/Si devices with various diameters. The current scales almost linearly with device area which suggests that the bulk leakage is the dominant factor. For smaller devices (e.g. 20 µm or 30 µm) the sidewall leakage should also be considered. The dark current versus device diameter is shown in Fig. 3-15(b) at different temperatures.

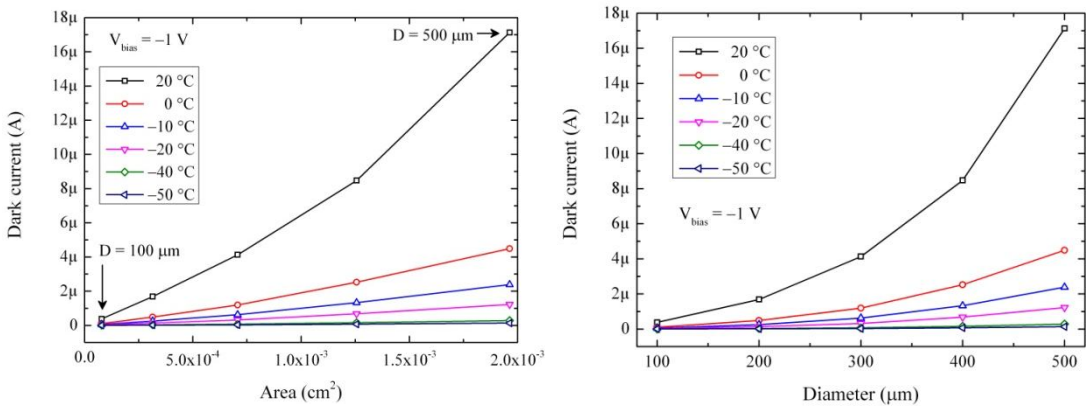


Fig. 3-15. Dark current of the Ge/Si devices versus (a) device area, and (b) device diameter at different temperatures. The Ge/Si devices were made using wafer number 8515 (Ge thickness: 1.5 µm).

Fig. 3-16 illustrates the *I–V* (left axis) and *C–V* (right axis) characteristics of a 300 μm-diameter Ge/Si device made from wafer number 8515 (Ge thickness: 1.5 μm). The reverse bias current of this plot can be divided into the following sections:

1. −1.7 V < *V* < 0 V: The leakage current increases exponentially with reverse bias voltage. On the other hand, the capacitance drops in this voltage range. From Fig. 3-14 where the value of E_a at −1 V is extracted (E_a is almost half of the Ge band gap at this bias point), the current mechanism is suggested to be generation through generation/recombination centres.
2. −3 V < *V* < −1.7 V: The leakage current does not show significant increase in this bias range. The capacitance is almost constant. This means that the electric field has already expanded to its maximum level. The total measured capacitance is ~6 pF which corresponds to the point that the electric field has penetrated into both Ge absorption layer and Si charge and multiplication layers. The corresponding electric filed at −1.7 V and −3 V is 1.2×10^4 V/cm and 2.2×10^4 V/cm, respectively. Both of these values are more than an order of magnitude smaller than the "critical" value for impact ionization ($E_c = 4\times10^5$ V/cm). This leads to the electric field to rise in both silicon and germanium at the same time, similar to PIN structure. Hence, the field reaches E_c in both absorption and multiplication regions. The reason is probably due to the growth condition of Si epilayers and the carrier concentration of each layer, particularly the p-type silicon charge layer. As can be seen in Fig. 3-7, the carrier concentration in Si charge layer is more than one order of magnitude lower than what was designed. As a result, the electric field which had to be controlled by this layer and dropped mostly in Si multiplication layer is now dropped over the whole structure at this very low reverse bias voltage range.
3. −5 V < *V* < −3 V: The leakage current increases with reverse current, however, the capacitance remains constant in this bias range. This could be explained as follows: since the capacitance is almost constant it can be concluded that by increasing the reverse bias voltage the electric field builds up in the lightly-doped layers (Ge absorption, Si charge and Si multiplication layers). And since the current increases in this bias range when E_a decreases from mid Ge bandgap at −1 V to ~0.15 eV at −4 V, one can conclude that the current transport would be trap-assisted tunnelling.
4. *V* < −5 V: the electric field keeps rising in both Ge absorption and Si multiplication regions and at the same time the current increases while the capacitance starts to fluctuate. This could be due to the enhanced trap-assisted

component of the current due to the increase of the electric field. And since Ge has lower bandgap and therefore lower E_c, it is estimated that the impact ionization process occurs in the Ge absorption layer before silicon multiplication layer. This is not what has been designed and I had aimed to achieve. The advantage of integrating Ge with Si is to take advantage of lower impact ionization noise in Si compared to Ge [11]; otherwise, all-Ge avalanche photodiode would be designed [12].

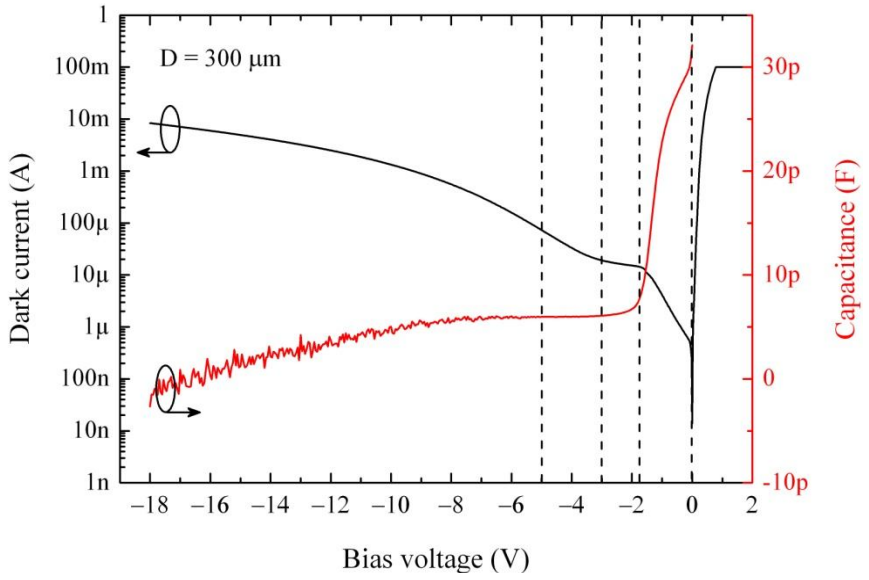


Fig. 3-16. Dark current (left axis) and capacitance (right axis) vs bias voltage of a 300 µm-diameter device at room temperature from wafer number 8515 (Ge thickness: 1.5 µm).

3.8. Low temperature electrical and optical characterization

The dark current (I_{DC}) and total current (I_{TC}) under 1.55 µm laser illumination of a Ge/Si devices made using wafer number 8515 (Ge thickness: 1.5 µm) at 295 K and 125 K are shown in Fig. 3-17. Due to the large distance between the optical fibre and the device in the cryostat chamber, the actual optical power on the device is unknown. As can be seen in this figure, decreasing the measurement temperature down to 125 K reduces the leakage current at low voltages significantly, which shows the considerable contribution of generation/recombination centres in the leakage current at low bias voltages.

The photo-current ($I_{TC} - I_{DC}$) of two devices (400 µm- and 500 µm-diameter) at 125 K is shown in Fig. 3-18. As can be seen in the figure, after ~−4 V the photo-current increases

considerably (more than two orders of magnitude) which suggests that the electric field in the device is high enough to have impact ionization after ~–4V. The photo-current is also noisy at this bias range which could also be related to the impact ionization process. However, the essential problem of the devices is the large amplitude of the dark current. It is worth mentioning that the fluctuation in the photocurrent is not due to the measurement equipments.

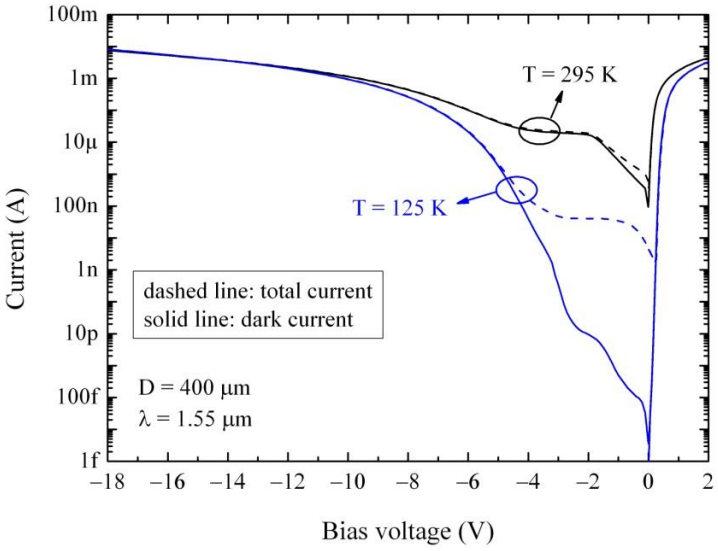


Fig. 3-17. Dark current and total current (under 1.55 µm laser illumination) of a Ge/Si device with the diameter of 400 µm at two different temperatures: 125 K and 295 K. The devices are made using wafer number 8515 (Ge thickness: 1.5 µm).

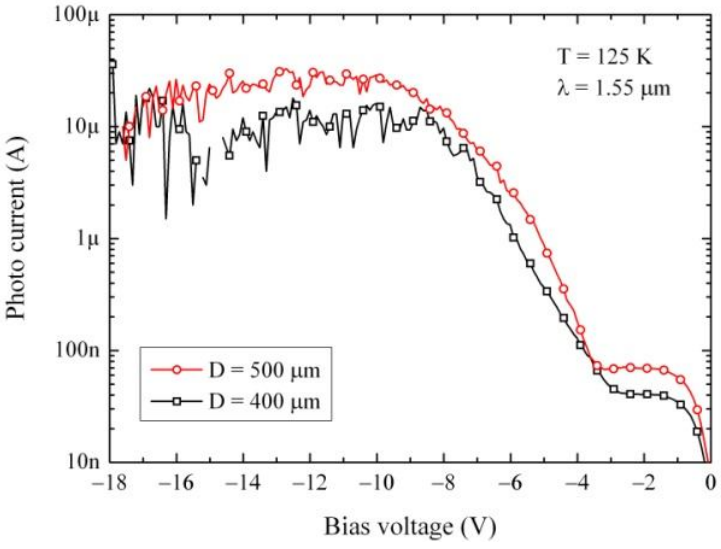


Fig. 3-18. Photo-current ($I_{TC} - I_{DC}$) of a 400 µm- and a 500 µm-diameter device at 125 K. The devices are made using wafer number 8515 (Ge thickness: 1.5 µm).

3.9. Si epilayer characterization

Based on the above results, particularly the high dark current level at low bias voltages (< –2 V) a hypothesis was suggested regarding the poor quality of the Si part of the device. In order to investigate this hypothesis and figure out the reason for the high dark current (considering the acceptable quality of the Ge layer and the Ge/Si interface [8]), the Ge layer of the wafer number 8515 (Ge thickness: 1.5 μm) was removed by wet etching using $NH_4OH:H_2O_2:H_2O$, as schematically shown in Fig. 3-19. The ratio and etch rate is mentioned in Appendix A4.

Using the same mask layout and fabrication process steps as were used to fabricate Ge/Si devices, I made devices on this silicon wafer. Fig. 3-20, compares the dark current–voltage characteristics of the Si and the Ge/Si devices. As can be seen, the dark current of the Si device at low voltages is still very high which could be an indication of the source of high leakage current of the Ge/Si diodes.

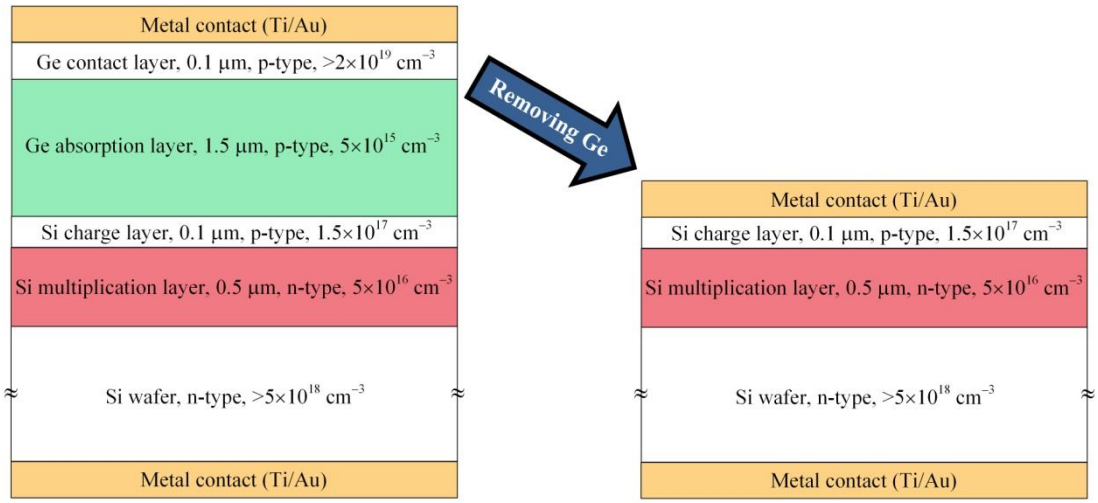


Fig. 3-19. Si devices were made from wafer number 8515 (Ge thickness: 1.5 μm) by removing the germanium layer using wet etching.

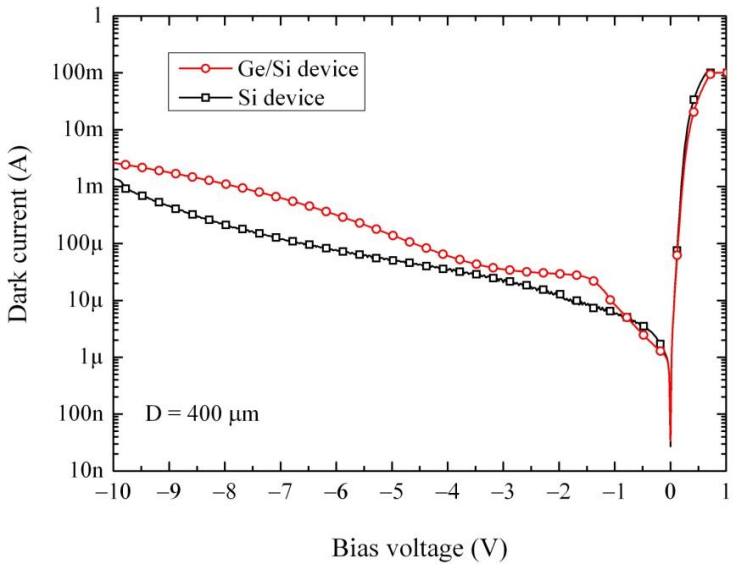
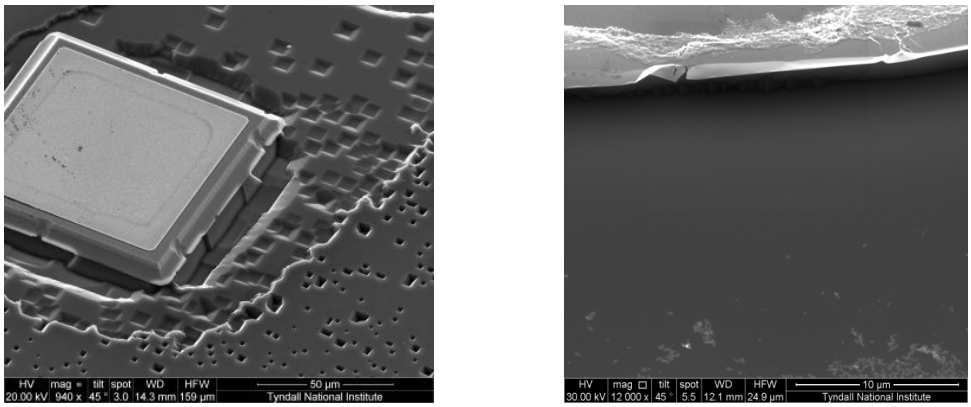


Fig. 3-20. Dark current of the Si device compared to Ge/Si device made from the same wafer (number 8515, Ge thickness: 1.5 µm). It can be concluded that the high reverse current is related to Si epilayer quality.

A Si sample was then etched using KOH solution at 80 °C to perform the etch pit density counting on Si, although it is not a standard technique. The SEM image of the Si surface after KOH etching is shown in Fig. 3-21(a). The holes and pyramids in the silicon are likely due to the defects and dislocations in the Si epilayers and/or the interfaces in Si. As a comparison, the same etching step was performed on a bulk p-type Si wafer and the result is shown in Fig. 3-21(b). No sign of defects can be seen in the p-type bulk sample etched at the same condition as the processed sample was etched.



(a) **(b)**

Fig. 3-21. SEM image of (a) Si sample designed for Ge/Si detector (wafer number 8515, Ge thickness: 1.5 µm), and (b) Si sample (bulk, p-type), both after being etched using KOH.

3.10. Effects of low / high temperature annealing

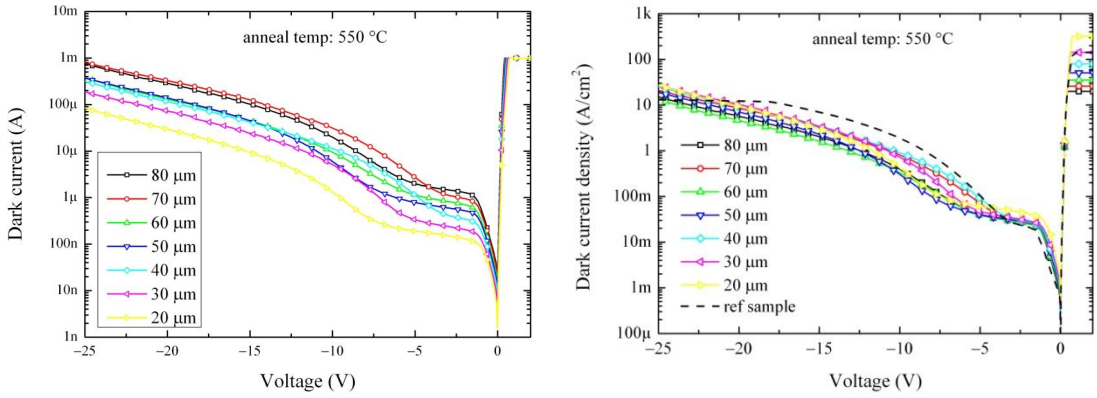
In order to try to improve the quality of Si epilayers and therefore the *I–V* characteristics of the Ge/Si devices, the samples from wafer number 8515 (Ge thickness: 1.5 μm) were annealed under the following two conditions prior to device fabrication:

1. 550 °C for 4 h - sample #1
2. 780 °C for 1 h - sample #2

Fig. 3-22(a) shows the *I–V* curves of sample #1 annealed at 550 °C for 4 h. As can be seen in this figure, the low temperature anneal does not improve the reverse current considerably. The dark current density of a reference sample (not annealed) is shown in Fig. 3-22(b) of the figure for comparison.

The effect of high temperature anneal (sample #2) on the *I–V* characteristic of the Ge/Si devices is presented in Fig. 3-23. Although this high temperature anneal has reduced the leakage current, the dark current density is still high and this figure shows that the effect of high temperature anneal is very non-uniform across the chip. Based on the results of *I–V* measurements at different temperatures the activation energy was measured at different bias voltages which changes from 0.44 eV at −1 V to 0.22 eV at −14 V.

The slope of the *I–V* curve changes at ~−10 V, which is an indication of the change in the punch through voltage and hence the electric field profile. This means that the high temperature anneal has either changed the doping profile of different layers, or improved the defective regions of the sample, or both. Nevertheless, the devices show no sensitivity to light at room temperature. Further investigations are required to define the exact role of the anneal step and its effects, so that the anneal condition can be optimized. Annealing might lead to the “gettering”. Hence smaller devices were fabricated to increase the chance of fabricating devices at higher quality regions after annealing.



(a) (b)

Fig. 3-22. (a) Dark current and (b) dark current density versus voltage of the annealed sample at 550 °C (wafer number: 8515, Ge thickness: 1.5 µm). In part (b), the dark current density of the reference sample (not annealed) is shown for comparison.

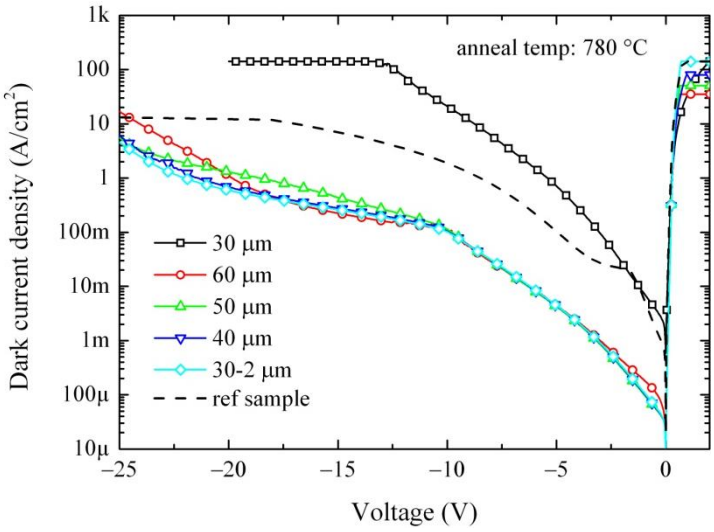


Fig. 3-23. Dark current density of the annealed sample at 780 °C for devices with different diameters (wafer number: 8515, Ge thickness: 1.5 µm). Comparing the results of the two 30 µm-diameter devices shows the non-uniform effect of the high temperature anneal. The characteristic of a reference sample (not annealed) is shown by dashed line.

3.11. Conclusions

In this chapter I reported on my investigations on an epitaxial approach to fabricate Ge/Si avalanche photodiodes (APDs). The structure and the layout of the APDs and different techniques to characterize both the Ge and the Si epilayers were presented.

Threading dislocation density of ~1-2×10^7 cm^{-2} was measured by performing a shallow wet etching. TEM images of the hetero-interface revealed that there was no oxide at the material interface and showed the presence of strain in the Ge film at the interface.

The reason of high leakage current was investigated by analysing the SRP and SIMS profiles of the samples as well as by performing electrical and optical measurements at various temperatures. Such investigations led to the conclusion that the majority of the leakage current is due to the defects in the Si epilayers. High leakage current could also be due to the low Si epitaxial growth temperature which would lead to the presence of in-active dopant atoms.

By removing the germanium film on top of the wafers, silicon devices were fabricated which show high leakage current. Etch pit density counting using KOH was also used. Based on the electrical characterizations of the silicon devices and the observations of the etched sample by KOH we could identify the possible reasons for high leakage current in the Ge/Si devices.

We have also shown that the low temperature anneal does not influence the device characteristics and that the high temperature anneal decreases the leakage current. However, detailed and systematic analyses of the effects of annealing are required to be able to optimize the annealing process. Optimizing the silicon epitaxy process considering the germanium growth condition and the post growth heat treatment could also be another alternative to improve the performance of the Ge/Si APDs.

3.12. References

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Chapter 4: Ge/Si diodes fabricated by layer exfoliation

4.1. Introduction

Germanium (Ge), due to its compatibility with silicon (Si) processing is recognized as the best candidate for expanding the range of functions of CMOS-based devices and circuits [1, 2]. Monolithic integration by the deposition of high-quality single crystalline Ge layer onto Si is impeded by the lattice mismatch of about 4%, leading to a high density of threading dislocations in the Ge epitaxial layer [3]. An alternative approach which avoids the epitaxial relationship is direct wafer bonding followed by removal of all but a thin layer of the material to be transferred. The technique (Smart Cut™ [4]) typically uses hydrogen implantation to form a sub-surface damaged layer which permits the separation (called exfoliation) of the top part of a wafer from its substrate after bonding. This technique does not require controlled wafer thinning as required with bulk wafer bonding and was used in this project to investigate the conductivity of the bonded interface. Understanding the possible current transport mechanisms through the bonded interface is a key in the design of Ge/Si photodiodes.

The exfoliation process requires three steps: (i) implanting a device wafer with a relatively high dose of hydrogen [5], helium [6], or hydrogen-helium co-implants [7] to create the defective region below the surface, (ii) direct bonding of the implanted wafer to the host substrate, and (iii) annealing of the bonded pair, to increase the bonding energy and also to achieve layer splitting by increasing the pressure inside the blisters caused by trapping the implanted molecules in the defects. The higher the annealing temperature, the higher the bond strength; however, the trade off is that when dissimilar materials are used, it is desirable that the splitting temperature is low enough to avoid stress problems associated with the difference in the thermal expansion coefficients and consequently breakage of the wafers. Recently, the feasibility of transferring hydrogen implanted Ge to oxide was demonstrated by Ferain *et al.* [8]. The surface blistering and the heat treatment of B^+/H^+ co-implanted Ge wafer were investigated by Ma *et al.* [9, 10]. In another survey, Chao *et al.* has studied the characteristics of hydrogen in Ge and its effects on the layer splitting process [11]. Splitting kinetics for Si and $Si_{0.8}Ge_{0.2}$ with hydrogen and hydrogen-helium implants was also investigated in [12]. To date, Si on insulator [13], strained Si on insulator [6], Ge on

insulator [7] and SiGe on insulator [14] substrates as well as Si *pn* junctions [5] have been fabricated using this technique. More recently Si/Ge junctions were fabricated by nanomembrane bonding where the junction is dominated by Fowler-Nordheim tunnelling leakage current [15]. In this chapter, I perform a proof of concept of p-Ge/n-Si integration by using wafer bonding and layer exfoliation with low thermal budget (see Table 4-1) for the first time followed by the fabrication, characterization and analysis of the electrical transport across the interfacial oxide.

Table 4-1. Summary of different ion implantation conditions and heat treatments. Abbreviation definitions are as follows – H_2: Hydrogen; He: Helium; SOI: Si On Insulator; GOI: Ge On Insulator; SGOI: SiGe On Insulator; sSOI: strained Si On Insulator; RT: Room Temperature; h: hour; min: minute.

Structure	Implantation		Heat treatment		Ref.
	Element	Energy [keV] / Dose [ions · cm^{-2}]	Bond enhancement	Exfoliation	
n^+ Si/p^- Si diode	H_2	130 / 5×10^{16}	500°C	400°C	[5] §
sSOI	He	- / 7×10^{15}	300°C (5h)+500°C (2h)	850°C (10 min)	[6]
GOI	H_2 & He (co-implant)	H_2: 120 / 3×10^{16} He: 68 / 1×10^{16}	300°C	250-400°C	[7]
SOI	H_2	175 / 5×10^{16}	70°C (2h) + 200°C (3h)	600°C (5 min)	[13]
SGOI	H_2	- / 2.5-5×10^{16}	800-900°C	500-600°C	[14]
SOI	H_2	- / -	>1000°C	400-600°C	[16]
GOI	H_2	200 / 4×10^{16}	250°C (12h)	450°C (30 min)	[17]
p^+ Ge / p^+ Si	H_2	80 / 1×10^{17}	175°C	350 °C	[18] §§
SGOI	H_2	100 / 5×10^{16}	850°C	600°C (3h)	[19]
SGOI	H_2	- / -	250-300°C (20-30h)	400-500°C	[20]
SGOI	H_2	200 / 8×10^{16}	400-500°C (2h)	500-600°C (a few h)	[21]
sSOI	H_2	160 / 5×10^{16}	200°C (12h)	500°C (2h)	[22]
sSOI	H_2	75 / 4×10^{16}	>800°C	500°C	[23]+its ref [10]
SGOI	H_2	100 / 5×10^{16}	850°C (2h)	600°C (3h)	[24]
SOI	H_2 & He (co-implant)	H_2: 120 / 3×10^{16} He: 68 / 1×10^{16}	RT	280-300°C (10-72h)	[25]
p Ge / n^+ Si diode	**H_2**	**180 / 5×10^{16}**	**100°C (1h)+130°C (24h)**	**300°C (5 min)**	**This work**

§ The only diodes that have been fabricated with a similar technique are reported in [5], which is an n^+ Si/p^- Si junction. 1000 °C anneal step for 1 h has been carried out to improve the device performance.

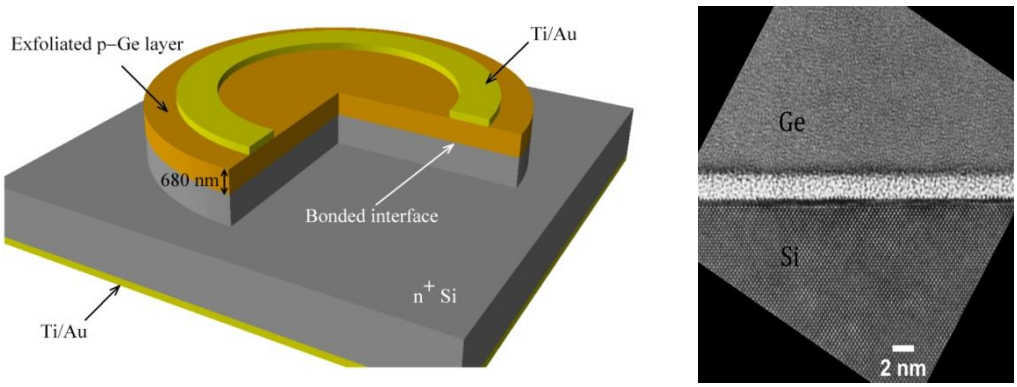
§§ The direct bonding type is hydrophilic for all the structures in this table except for this one which is hydrophobic.

4.2. p-Ge / n^+-Si diode fabrication

A 680 nm p-Ge bonded to an n^+-Si wafer was fabricated using oxygen radical activated bonding combined with layer exfoliation. For the donor Ge substrate, a 100 nm thick

layer of Plasma Enhanced Chemical Vapour Deposition (PECVD) silicon dioxide has been deposited prior to hydrogen implant. The silicon dioxide capping layer protects the Ge surface during the ion implantation. The Ge substrate was then implanted at room temperature with H_2^+ ions at a dose of 5×10^{16} cm^{-2} and energy of 180 keV without active chuck cooling. The oxide layer was then removed in a dilute HF solution. The n^+-Si host wafer and the p-Ge donor wafer were cleaned in a dilute NH_4OH-HF-DI using Standard Cleaning 1 solution with ozone for the Si wafer and without ozone for the hydrogen-implanted Ge wafer [26]. The wafers were then loaded in an Applied Microengineering Limited (AML) AW04 aligner bonder chamber which was pumped down to 10^{-5} mbar and exposed for 10 minutes to oxygen free radicals generated by a remote plasma ring at 100 W. The chamber pressure during remote plasma exposure was 1 mbar. The wafers were then bonded under a force of 1 kN applied for 5 minutes at the chamber pressure of 10^{-5} mbar. The wafers were annealed *in situ* at 100 °C for 1 hour with an applied force of 500 N followed by an *ex situ* annealing at 130 °C for 24 hours in order to enhance the bond strength and induce hydrogen platelet nucleation. The exfoliation was triggered by a short time anneal at 300 °C (5 min at 300 °C). The ramp-up rate was set to 0.5 °C/min in all annealing steps. Since hydrogen can diffuse out from the surface during the bonding process, the low temperature bonding step produces a more concentrated hydrogen profile at the peak implantation region due to the low diffusion coefficient of hydrogen in Ge at low temperatures [27]. After layer exfoliation a thin Ge film, which is 680 nm thick, remained bonded to the Si wafer. It has been shown that there is a "damage-free" region with the thickness of ~150 nm in the transferred Ge film located at the Ge/Si bonded interface [8].

For the purposes of electrical characterization and analyzing the carrier transport across the p-Ge/n^+-Si junction, circular mesa structures with different diameters ranging from 100 µm to 500 µm were fabricated. Ohmic contacts were made using Ti/Au (25/250 nm) deposited by e-beam evaporation and patterned by standard lithography and lift-off process. The circular mesa structures were then formed by SF_6/C_4F_8 reactive ion etching through the junction to a depth of 2.5 µm. No passivation layers were used for the mesa sidewall. After the initial measurements, an annealing step was carried out for 30 min at 400 °C in H_2/N_2 atmosphere in order to improve the performance of the devices. Fig. 4-1(a) illustrates the schematic of the diodes and Fig. 4-1(b) shows a high resolution TEM image of the Ge/Si interface. As can be seem, the interfacial amorphous layer thickness is uniform along the interface and is ~2 nm thick.



(a) **(b)**

Fig. 4-1. (a) Schematic illustration of the Ge/Si diode made by hydrogen implantation and layer transfer technique. (b) High resolution TEM image of the Ge/Si interface. The amorphous interfacial layer is ~2 nm thick and is uniform along the interface.

4.3. Results and discussion

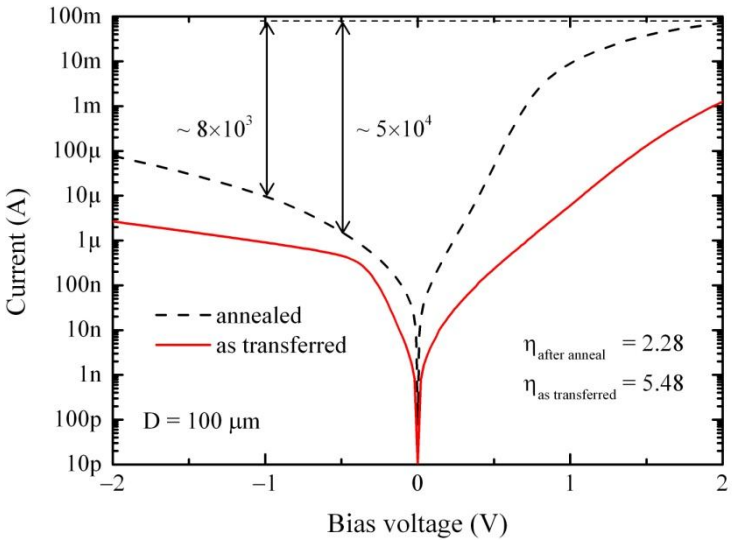
4.3.1. Current–voltage characteristics

Fig. 4-2(a) shows the current–voltage (*I–V*) characteristic (in semi-log scale) of a 100 μm-diameter device and Fig. 4-2(b) shows the characteristic in linear scale. The *I–V* curve exhibits rectifying behaviour before anneal but is limited in the forward current. After the annealing the *I–V* characteristic and the I_{on}/I_{off} current ratio have improved. The annealing step has improved the ideality factor (η) of the diodes from 5.48 to 2.28, as can be seen in Fig. 4-2(a). The forward resistance also shows a reduction from 245 Ω to 15 Ω, both of which are indications of the improvement in the device performance after the low temperature annealing.

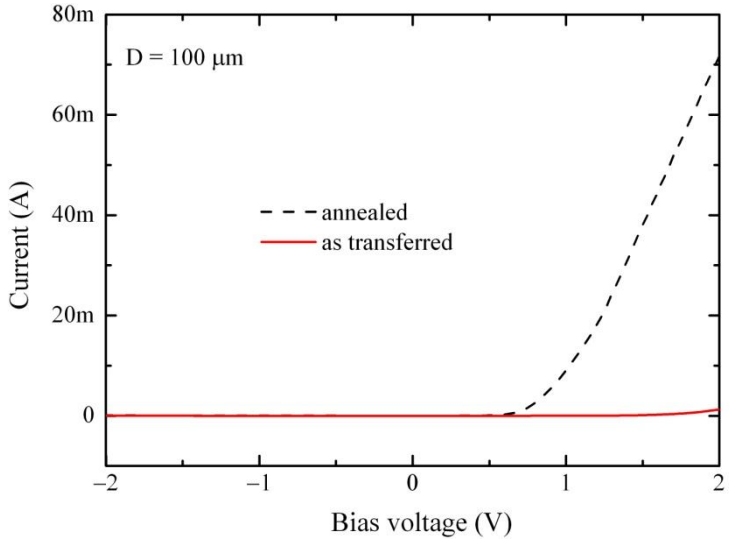
The leakage current can be divided into contributions from a bulk leakage current and a surface leakage current. Fig. 4-3 shows the current versus mesa diameter at 1 V reverse bias before and after annealing. The effects of annealing on the bulk and surface leakage currents are as follows:

	Before anneal	After anneal
J_{bulk} (mA/cm²)	10.5	27.8
$J_{surface}$ (μA/cm)	31.8	9.55

This suggests that the annealing in H_2/N_2 ambient passivates the sidewall dangling bonds and reduces the possible damage due to dry etching. Different surface treatments using dilute HF and HCl were performed after annealing, but did not show any effect on the *I–V* characteristic of the diodes.



(a)



(b)

Fig. 4-2. (a) *I–V* characteristic of a 100 µm-diameter diode before and after annealing in log scale. (b) The *I–V* characteristic in linear scale. As shown in part (a), the ideality factor of the diode is 5.48 before annealing and 2.28 after annealing.

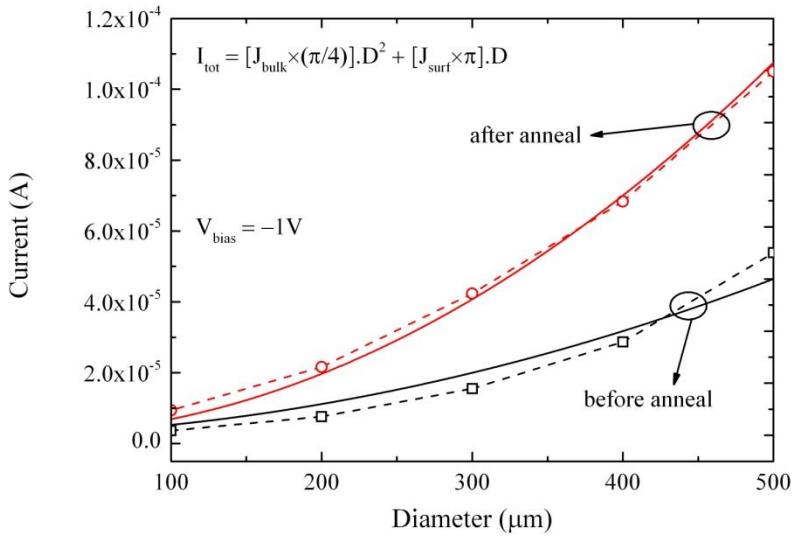
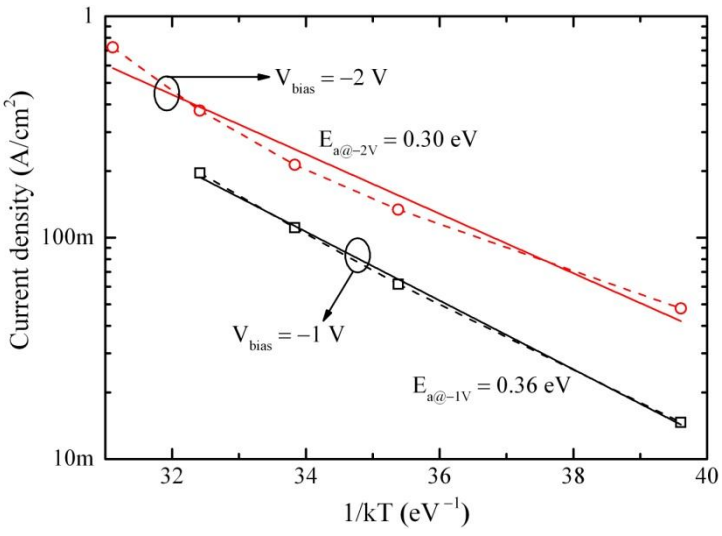


Fig. 4-3. Current versus device diameter at –1 V before and after annealing; Dashed lines: measured data; Solid lines: fit from bulk leakage (per unit area) and surface leakage (per unit diameter).

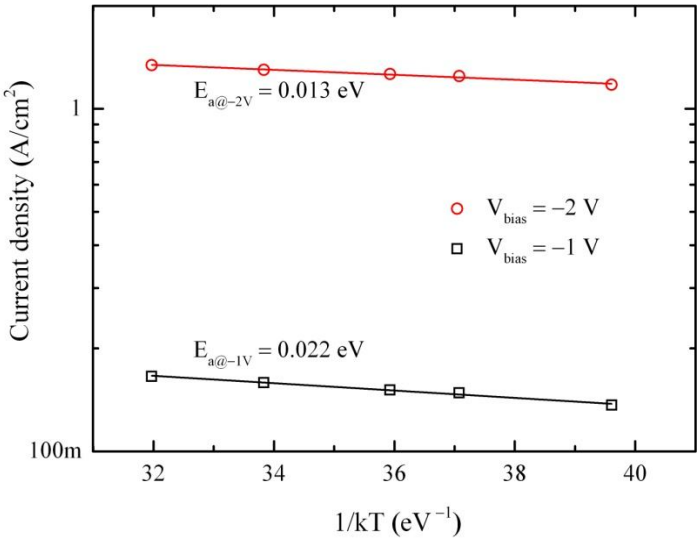
In order to analyze the carrier conduction mechanism, *I–V* measurements were carried out before and after annealing at different temperatures between 20 °C and 100 °C. The reverse leakage current was fitted to the following formula:

$$J = A \cdot \exp(-E_a / kT), \tag{4-1}$$

where J is the diode current density, A is a constant and E_a is the activation energy. Fig. 4-4(a) shows the Arrhenius-fit plots of J versus $1/kT$ (in semi-log scale) for two different reverse bias voltages before annealing. From this figure, E_a is estimated from the slope of the fitted lines. The value of E_a at –1 V and –2 V is 0.36 eV and 0.3 eV, respectively, which corresponds to almost half the Ge bandgap. This suggests that the generation-recombination current in the space charge region is dominant for the devices. Although the depletion region in the reverse bias regime expands mostly in the Ge layer, the origin of the generation-recombination component is not related to the quality of the transferred Ge film since it has been shown that the transferred layer is single crystalline [8]. It could be related to the bonded interface.



(a)



(b)

Fig. 4-4. (a) Current density versus 1/kT at –1 V and –2 V before annealing. (b) Current density versus 1/kT at –1 V and –2 V after annealing. The circular and square symbols are the measured data and the solid lines are the Arrhenius-fit plots. The value of the activation energy at each bias voltage is also shown.

After annealing, the value of E_a at –1 V and –2 V is 0.022 eV and 0.013 eV, respectively, which is much smaller than the Ge bandgap (see Fig. 4-4(b)). Thus, the leakage current density is relatively temperature independent and the conduction mechanism is likely to be direct tunnelling through the interfacial oxide rather than generation-recombination mechanism [15]. This can also be confirmed by the improvement of the diode ideality factor after the heat treatment (see Fig. 4-2(b)).

4.3.2. Proposed band diagram at Ge/Si interface

As shown in Fig. 4-5, the trap energy level is close to the Ge valance band edge and therefore below the Fermi level at equilibrium and hence filled with electrons. If we assume that the traps are donor-type, they would be neutral when filled with electrons, and hence would not affect the electric field. Assuming the traps to be acceptor-type, these traps would be negatively charged when filled with electrons [28] and hence play a significant role in carrier transport by pulling the holes in the Ge substrate toward the Ge/oxide interface which in turn causes Ge band bending upward at low reverse voltages. As a result, electrons directly tunnel through the oxide from Ge valance band to Si conduction band, as shown by arrows in Fig. 4-5. The band bending caused by traps would be less effective by increasing the reverse bias voltage as illustrated in Fig. 4-5 – right.

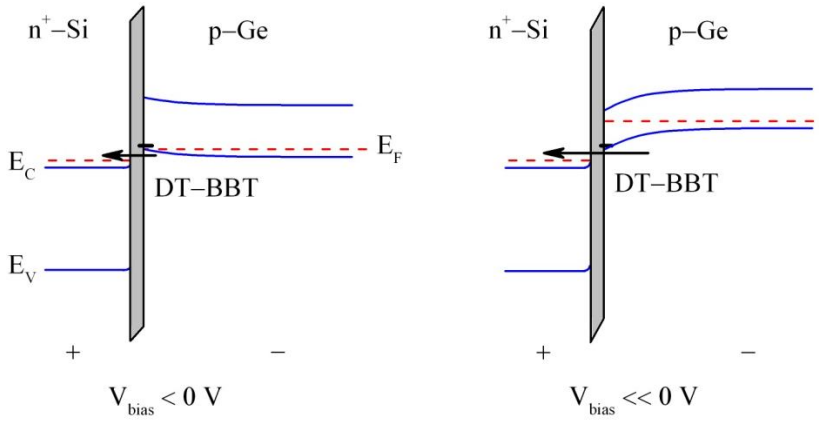


Fig. 4-5. Schematic representation of the Ge/Si band diagram illustrating the carrier transport mechanism in reverse bias.

In the forward bias condition, as shown in Fig. 4-6, carrier transport starts with the electrons tunnelling through the oxide from the Si conduction band to the Ge conduction band. At low forward bias voltages, only the electrons at the tail of the Fermi distribution function of the Si conduction band can travel to the Ge conduction band by tunnelling directly through oxide. By increasing the bias voltage the electrons which are close to the Fermi level contribute to the current. Based on the exponential behaviour of the Fermi distribution function, the current in the forward bias (in log scale) increases linearly with voltage; however, after reaching a high enough bias

voltage (~0.9 V), carriers below the Fermi level can travel to the Ge conduction band (see Fig. 4-6 – right) and the current is limited by the series resistance.

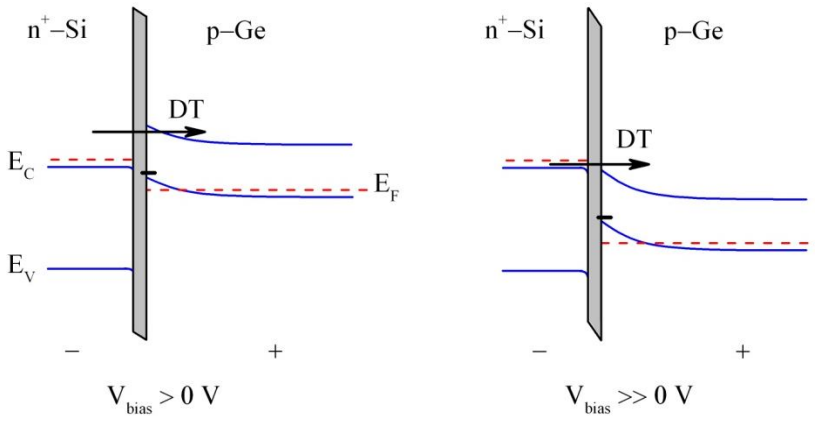


Fig. 4-6. Schematic representation of the Ge/Si band diagram illustrating the carrier transport mechanism in forward bias.

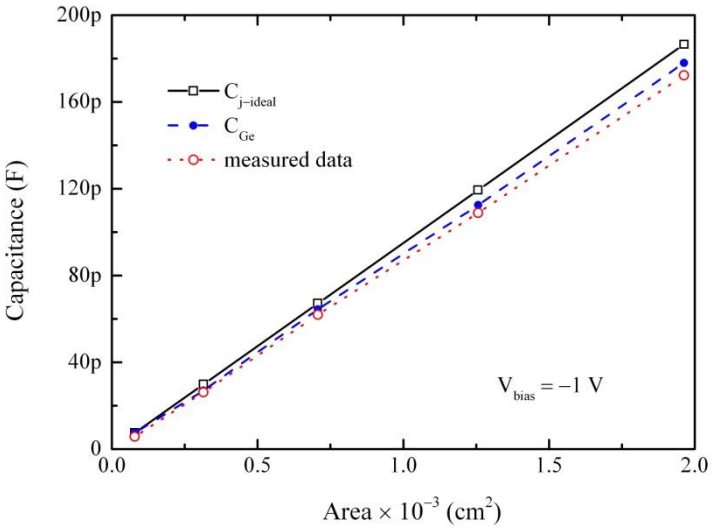
4.3.3. Capacitance–voltage characteristics

The capacitance of the diodes was evaluated by capacitance–voltage (*C–V*) measurements at 100 kHz. Fig. 4-7(a) shows a linear relation of the capacitance with device area at –1 V as expected. Typical *C–V* characteristics are presented in Fig. 4-7(b) for devices with different diameters. Taking into account the doping concentration of Si and Ge, we can assume that the depletion region is mostly in the Ge layer. Therefore, the total capacitance of the diode is the result of two capacitances in series (i.e., C_{ox} and C_{Ge}). Knowing that the interface oxide is ~1.6 nm thick [29], we calculated the capacitance of the depletion region in the Ge film (C_{Ge}). For C_{ox} we have assumed that it consists of 0.8 nm SiO_2 and 0.8 nm GeO_2. The result is also shown in Fig. 4-7(a). We have also calculated the capacitance per unit area of an ideal ($C_{j\text{-}ideal}$) p-Ge/n^+-Si junction (no interfacial oxide), using the following analytical formula [30]:

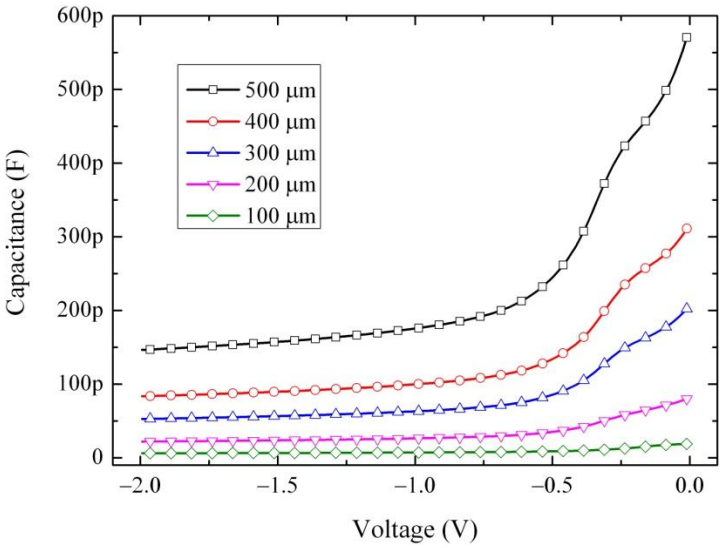
$$C_{j-ideal} = \left[\left(qN_{A,Ge}N_{D,Si}\varepsilon_{Ge}\varepsilon_{Si}\right)/\left(2\left(N_{A,Ge}\varepsilon_{Ge} + N_{D,Si}\varepsilon_{Si}\right)(\Psi_{bi} - V)\right)\right]^{1/2}, \qquad (4\text{-}2)$$

where q, Ψ_{bi} and *V* are the electron charge, built-in potential at equilibrium and applied bias voltage, respectively. $N_{Si(Ge)}$ and $\varepsilon_{Si(Ge)}$ are the doping concentration and the dielectric constant of Si(Ge), respectively. The ideal junction capacitance using the

analytical formula at –1 V is also shown in Fig. 4-7(a). According to the value of C_{Ge}, the depletion width was calculated to be 154 nm at 1 V reverse bias. This means that the space charge region is in the "damage-free" region in the Ge layer [8]. Thus the generation-recombination current measured prior to annealing is not related to the Ge film quality but to the bonded interface which has been improved after the heat treatment.



(a)



(b)

Fig. 4-7. (a) Capacitance versus device area at –1 V. Solid line: junction capacitance calculated using the analytical formula (4-2); Dashed line: capacitance due to the depletion region inside Ge; Dotted line: measured data. (b) *C–V* characteristic of diodes with various diameters.

4.4. Conclusions

In this Chapter the feasibility of fabricating a conductive Ge/Si interface by wafer bonding was investigated. I have shown successful low thermal budget wafer bonding and layer exfoliation of a 680 nm Ge film to bulk Si substrate by fabricating Ge/Si diodes on this bonded pair. Low temperature process (≤ 400 °C) is required for the compatibility with CMOS back-end-of-line (BEOL) processing. This is the first report of the p-Ge/n-Si heterojunction fabricated using layer exfoliation technique. The bond was strong enough to tolerate the fabrication process steps, demonstrating that wafer bonding combined with layer transfer is an effective and reliable technique to join highly lattice mismatched materials that circumvents the serious problems associated with bulk wafer bonding. Improvement in I_{on}/I_{off} ratio is obtained after low temperature annealing with the improvement of diode ideality factor from 5.15 to 2.7. *C–V* measurements have shown that the space charge region is in the "damage-free" region inside the Ge layer and therefore the generation-recombination current measured prior to annealing is not related to the Ge film quality but to the bonded interface. By performing electrical measurements at different temperatures the carrier transport mechanism is shown to be dominated by generation-recombination component before annealing and due to direct tunnelling in forward bias and band-to-band tunnelling in reverse bias after annealing.

Understanding the physics of the bonded interface is crucial in the design of Ge/Si photodiodes. Highly doped materials were used in this part of the project to focus the electric field on the interface to enhance the carrier conduction mechanism. Hence the depletion width was limited to ~150 nm of the Ge layer. As a result, low sensitivity to near infrared wavelengths was assumed. Results of this Chapter were used in the design and fabrication of Ge/Si photodiodes which are presented in Chapter 5.

4.5. References

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Chapter 5: Ge/Si photodetectors fabricated by direct wafer bonding

5.1. Introduction

For the integration of Ge with Si and for the purpose of fabricating integrated on-chip detectors at near infrared wavelengths, a high-quality defect-free, 100% Ge layer is desirable for realising high-performance photodiodes. Low defect density in the Ge layer will lower the dark current by minimizing the leakage mechanisms and noise sources. As mentioned before, integration through epitaxial growth is challenging due to the lattice mismatch between Ge and Si resulting in the formation of a high density of misfit dislocations which increases the leakage current. In order to accommodate this lattice mismatch, different techniques such as deposition of graded SiGe buffer layers [1, 2] and/or high temperature cyclic annealing [2, 3, 4] have been proposed.

Highly effective integration of detectors with silicon waveguides has been achieved through rapid melting growth. However, this requires a high temperature process step (Ge melting point ~940 °C) and is limited to thin Ge layers [5]. A side effect of the high temperature process is Si and Ge interdiffusion [6] resulting in a reduced responsivity at long wavelengths. For the integration of Ge with pre-fabricated Si circuits, the fabrication processes and temperatures have to be compatible with CMOS constraints and, in particular, a limited thermal budget and maximum temperature of 450 °C.

Direct wafer bonding can also be used for the integration of Ge with Si. There, a critical challenge is minimising the thickness of the interfacial layer which forms at the metallurgical junction but also assists in the bonding. Surface activated bonding results in a thinner interfacial layer than wet wafer bonding where the interfacial layer has been reported to be several nanometres thick [7]. The interfacial layer affects the electric field distribution across the junction and hence the carrier transport across the interface. The Ge/Si interface has been studied recently by bonding a p-Ge layer on an n^+-Si substrate using direct wafer bonding and layer exfoliation [8] and also by bonding an n^+-Si nanomembrane to a p^+-Ge substrate [9]. In this chapter, we report on a remarkable responsivity from a p^--Ge/n^+-Si heterojunction photodiode. In addition, detailed analysis regarding the carrier transport across the junction as well as the band

diagram of the interface is presented to explain the increased current flow that has been achieved.

5.2. Device fabrication

An n^+-Si wafer (resistivity ≈ 0.001 Ω.cm, thickness ≈ 535 μm) and a p^--Ge wafer (resistivity ≈ 1 Ω.cm, doping level, N_a ≈ 3.5×10^{15} cm^{-3}, thickness ≈ 510 μm) were chemically cleaned and then bonded at 10^{-5} mbar [8]. The surface activation step was performed by exposing the surface of the wafers to oxygen free radicals generated by a remote plasma ring at 100 W prior to bringing the wafers into direct contact. This step was followed by two 24-hour *ex situ* anneal steps at 200 °C and 300 °C in order to enhance the bond strength. Following the bonding, the Ge side of the bonded pair was thinned by mechanical grinding and polishing leaving a 5.4 μm thick Ge layer. The final thickness depends on the thinning process control capabilities and the bond strength. An iron plate and 9 μm grit Al_2O_3 abrasive were used in a Logitech lapping/polishing machine to thin the wafer (Si or Ge). The plate rotation speed was initially set to 50 rpm (thinning rate ≈ 12 μm/min for Ge and 10 μm/min for Si); however, after reaching the thickness of ~150 μm and in order to reduce the mechanical stress on the bonded pair, the rotation speed was reduced to 30 rpm. The wafer was then polished using a polishing plate and polishing suspension type SF1 at the speed of 50 rpm. No delamination was observed after the grinding and polishing steps.

5.3. Results and discussion - Ge on Si devices

5.3.1. TEM and SEM images of the Ge/Si devices

A high-resolution transmission electron micrograph (HR-TEM) of the Ge/Si heterojunction is shown in Fig. 5-1. The Ge and Si on both sides of the junction are single crystalline without any cracks or dislocations. An amorphous interfacial region is observed to be approximately 2 nm thick. However, there are additional regions at the interface on the Ge side, which are shown in the magnified images. The thick regions could be due to slight changes in the bonding recipe that I used in this experiment to increase the bond strength. The oxygen plasma step was 15 minutes, 5 minutes longer than the previous experiment in Chapter 4, and I think this might cause the additional oxygen atoms to get trapped at the interface and thicker amorphous interfacial regions (see Fig. 4-1).

In order to characterise the electrical and optical properties of the Ge/Si heterojunction I fabricated mesa diodes (Fig. 5-2). Ohmic contacts were made to the p^--Ge and n^+-Si using Ti/Au (25/250 nm) deposited by e–beam evaporation. Circular mesa structures ranging in diameter from 100 µm to 500 µm were formed by SF_6/C_4F_8 inductively coupled plasma etching through the Ge/Si junction to a total depth of 10.2 µm. No anti-reflection coating or sidewall passivation layers were used. After initial measurements, an annealing step was carried out for 30 min at 400 °C in H_2/N_2 (0.05/0.95) atmosphere. We could make Ge on Si and Si on Ge devices. However, our main focus would be on the Ge on Si devices due to the doping levels of the two wafers (lightly p-type Ge and highly n-type Si). For normal incident devices it would be desirable to limit the electric field in the mesa section so that it can expand vertically. The entire fabrication process is done with the temperature ≤ 400 °C and is compatible with the backend processing of CMOS microelectronics.

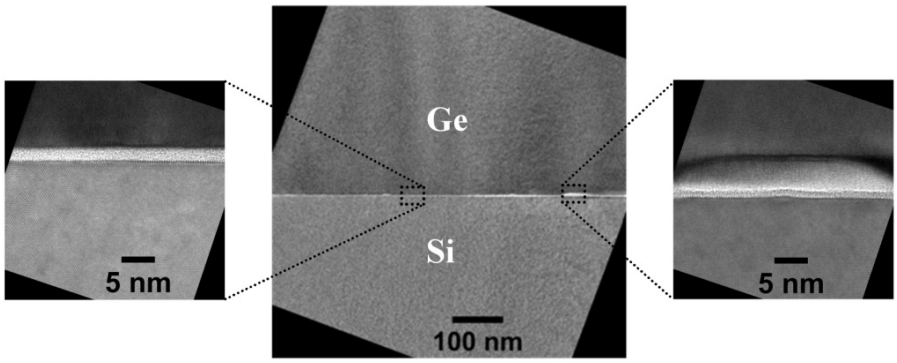


Fig. 5-1. High resolution TEM image of the Ge/Si interface. The two zoomed-in images show the thin (~2 nm thick) interfacial layer (on the left) and the thick region (on the right).

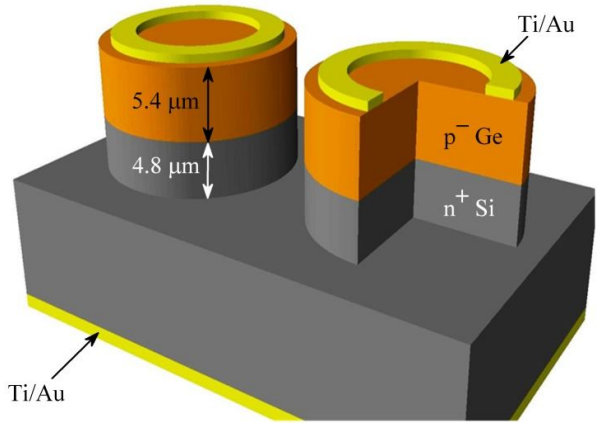
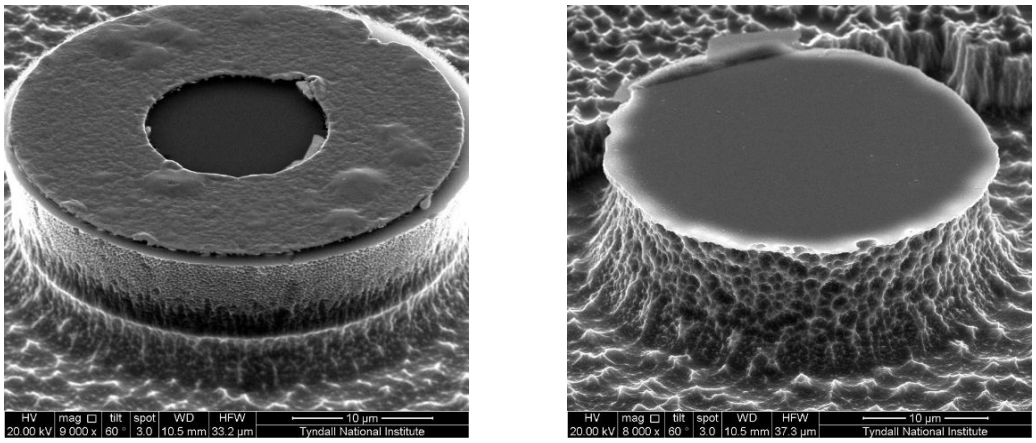


Fig. 5-2. Schematic illustration of the Ge/Si photodetectors made by the wafer bonding technique followed by CMP.

The SEM image in Fig. 5-3(a) illustrates a fabricated Ge/Si photodiode showing the top contact and the mesa sidewall. Fig. 5-3(b) shows a damaged device after chemical mechanical polishing (CMP). The Ge layer is de-bonded from Si substrate due to the mechanical stress during CMP.



(a) **(b)**

Fig. 5-3. SEM image of (a) a fabricated photodiode by direct wafer bonding, and (b) a delaminated bonded pair after CMP.

5.3.2. Electrical characteristics of the Ge/Si diodes

Fig. 5-4 illustrates the dark current density versus voltage (*J*–*V*) of a 500 µm-diameter device at two temperatures (20 °C and −50 °C). This figure clearly shows the rectifying behaviour of the *pn* heterojunction and that the thin interfacial layer does not block carrier transport. The dark currents at 20 °C at −0.5 V, −1 V, and −2 V are 30 µA, 49 µA, and 94 µA, respectively, which correspond to dark current densities of 15 mA/cm^2, 25 mA/cm^2, and 48 mA/cm^2. These values compare very favourably with those reported to date for Ge/Si heterojunction photodetectors [10, 11, 12, 13]. The dark current density of devices with different diameters (Fig. 5-5) shows that the main component of the reverse current is proportional to the area.

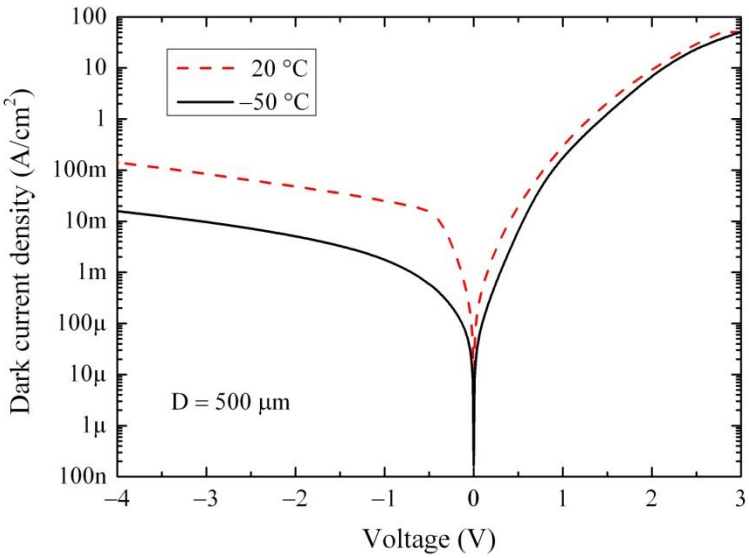


Fig. 5-4. *J–V* characteristics of a 500 µm-diameter device at two different temperatures in the dark. The dashed line is at 20 °C and the solid line is at −50 °C.

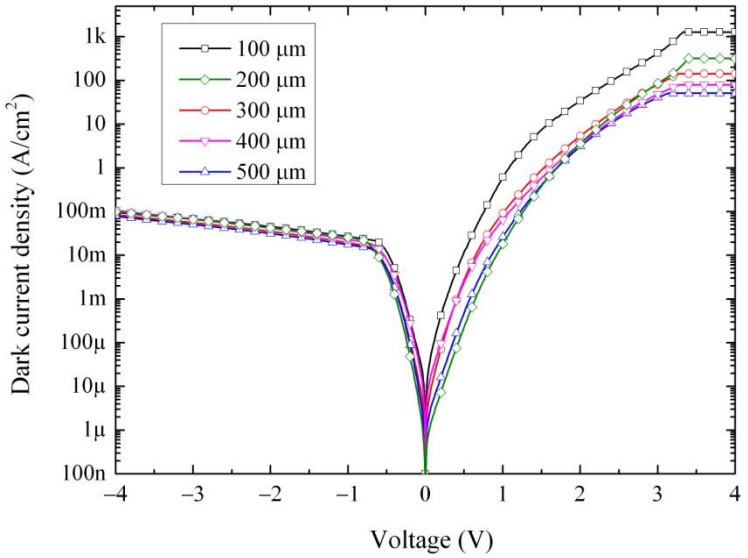


Fig. 5-5. Dark current density of devices with different diameters which shows that the main component of the reverse current is due to the bulk (area).

Capacitance–voltage (*C–V*) measurements were performed at 20 °C and −50 °C and at different frequencies (10 kHz to 1 MHz) in order to understand the variation in depletion width which will occur mainly on the lightly doped Ge side of the junction. Fig. 5-6 shows the *C–V* characteristics at different frequencies. As can be seen in this figure, the *C–V* characteristics are independent of frequency at −50 °C while at 20°C the

capacitance at V > ~−0.5 V increases at lower frequency. The difference in the characteristics is most probably due to the temperature dependence of the emission rates of charge carriers from the interface states. This suggests that interfacial traps are a factor and that these traps are being filled at room temperature.

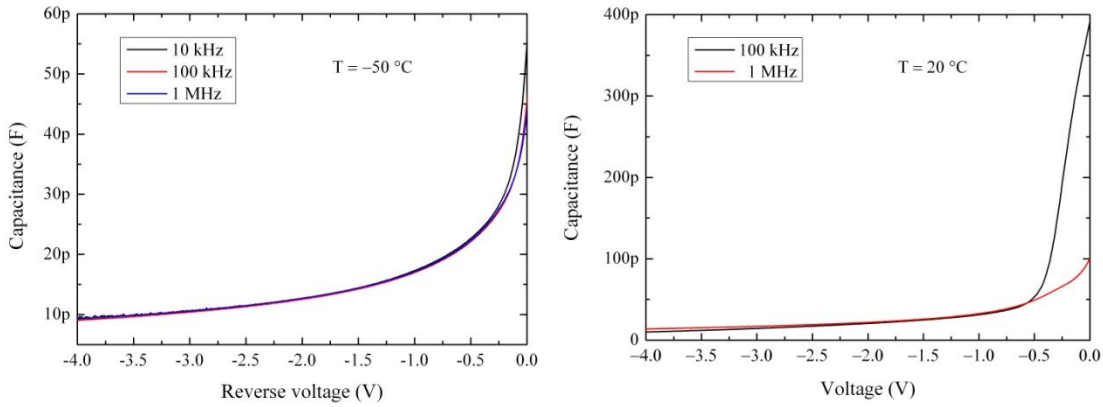


Fig. 5-6. *C–V* characteristics of a Ge/Si photodetector at different frequencies at (a) −50 °C, and (b) 20 °C.

Fig. 5-7 shows the dark current density of a 500 μm-diameter device as a function of reverse bias (left axis) at two different temperatures. Fig. 5-7 also shows how the capacitance depends on the reverse bias voltage at 20 °C and −50 °C (right axis). As can be seen, the reverse current is temperature dependent and the activation energy (E_a) obtained by performing current–voltage (*I–V*) measurements at different temperatures is 0.22 eV at −2 V. Fig. 5-8 shows the variation of reverse current with temperature. As indicated in the figure, E_a decreases slightly at higher reverse bias voltages.

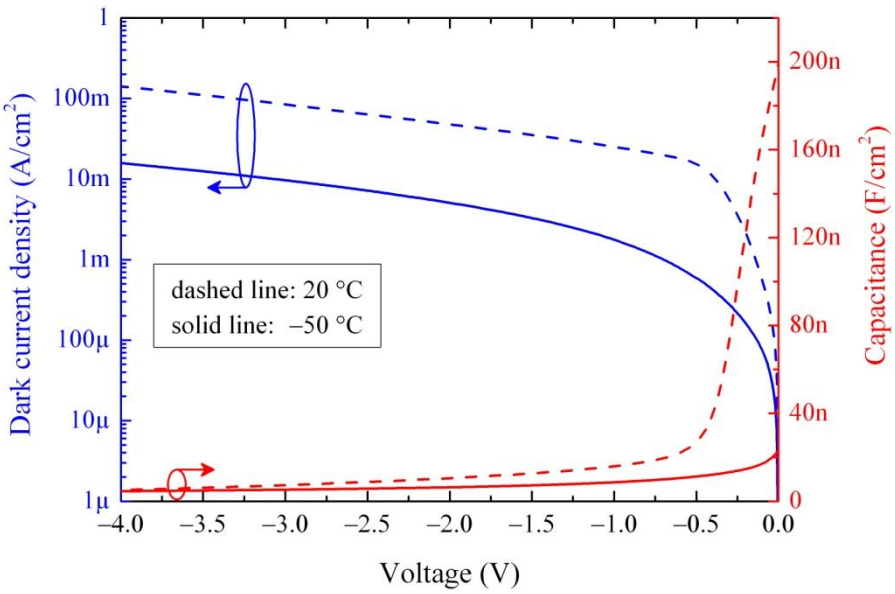


Fig. 5-7. Dark current density versus reverse bias voltage (left axis) and C–V characteristic at 100 kHz (right axis) of the Ge/Si diode. Dashed lines are at 20 °C and solid lines are at −50 °C.

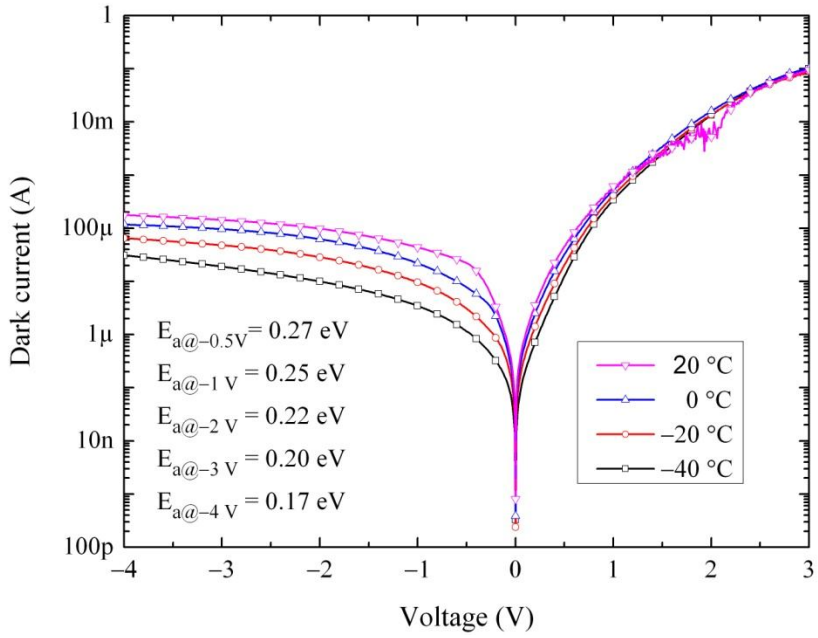


Fig. 5-8. I–V characteristic of a Ge/Si diode at different temperatures. The values of activation energy (E_a) at different reverse bias voltages are indicated in the inset.

Fig. 5-9 shows how $1/C^2$ depends on voltage at -50 °C and 20 °C at 100 kHz in dark and under illumination ($\lambda = 1.62$ μm, $P_{opt} = 10$ μW). As

$$1/C^2 = 2(\Psi_{bi} - V_{bias} - 2kT/q)/(q\varepsilon N_a), \tag{5-1}$$

the extrapolation to 0 V defines the built-in potential (Ψ_{bi}) of Ge at the interface. In (5-1), k, T, q, ε, and N_a are the Boltzmann constant, temperature, electronic charge, permittivity, and free-carrier concentration, respectively. The slope of the $1/C^2$ versus voltage curve gives the free-carrier concentration in Ge which is ~2×10^{15} cm^{-3} and ~6.5×10^{14} cm^{-3} at 20 °C and -50 °C, respectively. Ψ_{bi} is positive at -50 °C which means that the Ge surface at the junction is depleted of holes while the negative value of Ψ_{bi} at 20 °C suggests that the Ge surface at the interface is in the accumulation regime. This accumulation of holes at the Ge/Si interface is an indication of the presence of negative charges at the interface which attract holes from Ge substrate toward the interface. Hence, it can be concluded that the interface traps are acceptor-type traps [14]. Considering the Ge surface potential (Ψ_s) at the interface, the amount of charge at the interface (Q_s) can be calculated using [15]:

$$Q_s = \frac{\sqrt{2}\varepsilon_s kT}{q L_D} F\left(\beta\Psi_s, \frac{n_{po}}{p_{po}}\right), \tag{5-2}$$

where n_{po} and p_{po} are the equilibrium densities of electrons and holes in the bulk of Ge, respectively, L_D is the extrinsic Debye length:

$$L_D = \sqrt{\frac{\varepsilon_s}{q p_{po} \beta}}, \tag{5-3}$$

$$\beta = \frac{q}{kT}, \tag{5-4}$$

and

$$F\left(\beta\Psi_s, \frac{n_{po}}{p_{po}}\right) = \sqrt{[\exp(-\beta\Psi_s) + \beta\Psi_s - 1] + \frac{n_{po}}{p_{po}}[\exp(\beta\Psi_s) - \beta\Psi_s - 1]}. \tag{5-5}$$

Therefore, $Q_{s@20°C} = +1.26\times10^{-8}$ C/cm^2. This leads to the density of occupied traps below E_F to be $N_{s@20°C} = Q_{s@20°C}/q = 7.88\times10^{10}$ cm^{-2}.

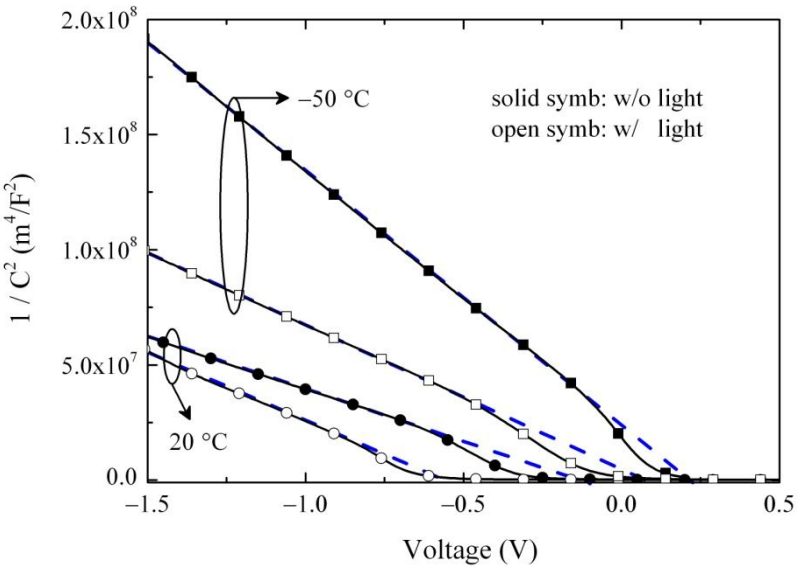


Fig. 5-9. $1/C^2$ versus reverse bias voltage at 20 °C and −50 °C. Solid symbols: in dark; Open symbols: under illumination (λ = 1.62 μm, P_{opt} = 10 μW).

The depletion width (W_D) is shown in Fig. 5-10 as a function of reverse bias voltage at two temperatures (20 °C and −50 °C). At −50 °C and 0 V, the junction is already depleted and the W_D is ~0.5 μm which then expands to 3.08 μm at −4 V. At 20 °C, however, the expansion of the depletion region occurs after ~−0.25 V (shaded area in Fig. 5-10). This is due to the pile up of holes at the interface which should be swept away by the electric field to reach the flat-band condition before depletion starts.

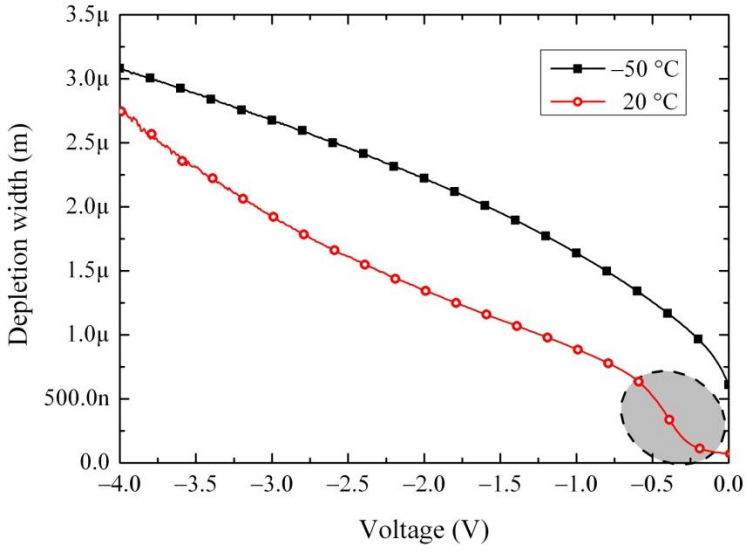


Fig. 5-10. Depletion width as a function of reverse bias voltage at 20 °C and −50 °C. The shaded region illustrates the effect of charges captured by the interface traps at 20 °C.

5.3.3. Proposed band diagram at the Ge/Si interface

Based on the above measurements and discussion, the band diagrams for the Ge/Si bonded interface at equilibrium at −50 °C and 20 °C, are shown in Figs. 5-11(a) and 5-11(b), respectively. The current transport at −50 °C is partially due to electron generation in the Ge depletion zone and tunnelling across the barrier. Trap assisted carrier generation is also likely to be contributing. At 20 °C, the interface traps below E_F are occupied and cause upward band bending of Ge at the interface, thus lowering the potential barrier for carrier transport by thermionic field emission from the Ge to Si conduction band. This temperature-induced potential barrier lowering effect increases the current flow. Regarding the forward bias regime and, as is shown in Fig. 5-4, there is a slow increase in the current both at −50 °C and 20 °C and is attributed to the large band offset between Si and Ge conduction band edges and to the presence of the interfacial layer.

5.3.4. Optical characteristics of the Ge/Si photodiodes

The *I*–*V* characteristics of the 500 μm-diameter mesa which has a 320 μm-diameter open aperture is illustrated in Fig. 5-12. This figure shows the dark current and the photo current at a wavelength of 1.55 μm and different optical powers at −50 °C and 20 °C. The photoresponse of this photodiode at a bias, V_{bias}, of −2 V, and at −50 °C and 20 °C is shown in Fig. 5-13 where the responsivity decreases with increasing power. Light from an Agilent tunable laser is delivered to the detector through a standard cleaved single mode fibre and illuminates a spot much less than the open aperture of the detector. The output power from the fibre at each wavelength is measured using a calibrated Newport optical power meter and the detector current is measured using a Keithley source-meter.

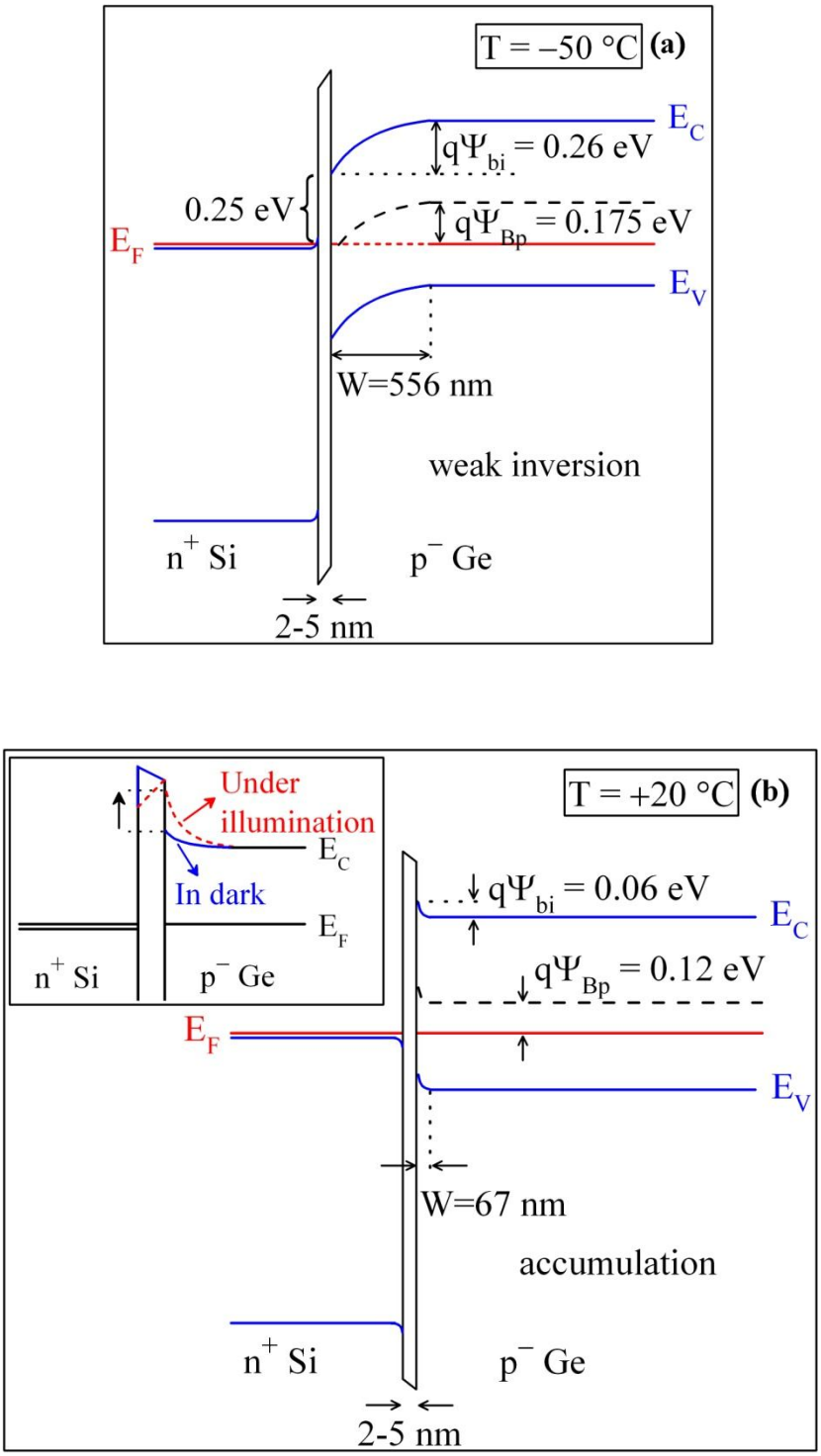


Fig. 5-11. Schematic representation of the Ge/Si band diagram at equilibrium at (a) −50 °C, and (b) 20 °C. Ψ_{bi} and Ψ_{Bp} are the built-in potential and the Fermi potential with respect to the midgap in the bulk of p-Ge, respectively. In part (a), the Ge surface at the interface is in the "weak inversion" mode while in part (b) it is in the "accumulation" mode due to trap filling. The dashed lines in (a) and (b) are the intrinsic Fermi level. The inset of part (b) schematically illustrates the potential barrier lowering due to filling of acceptor traps by either temperature or light.

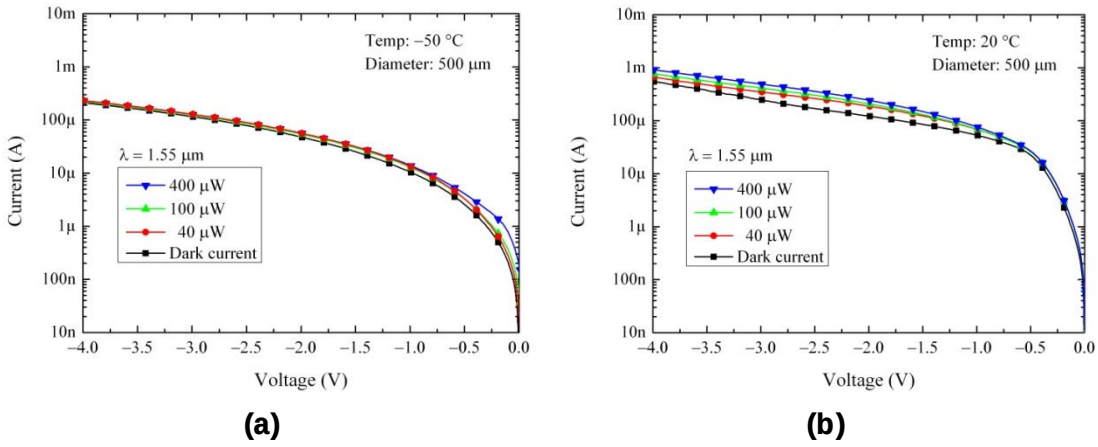


Fig. 5-12. *I–V* characteristics of the 500 μm-diameter Ge/Si photodetector in dark and under illumination (λ = 1.55 μm) at (a) −50 °C, and (b) 20 °C.

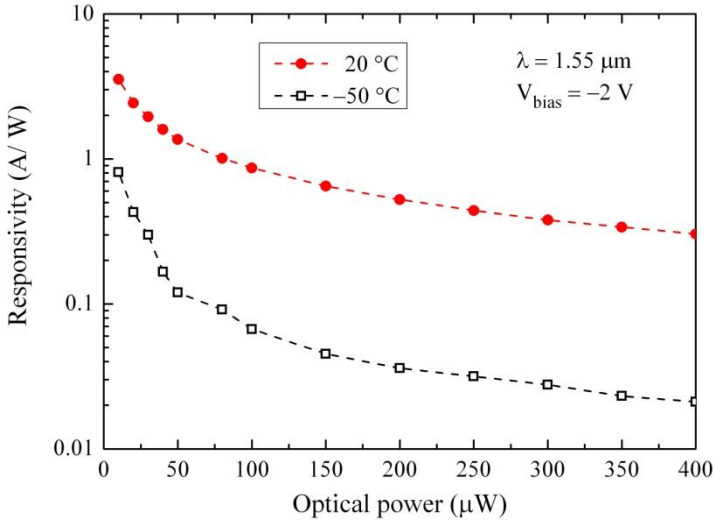


Fig. 5-13. Responsivity of the Ge/Si photodiode versus input optical power at a wavelength of 1.55 μm and *V* = −2 V at two temperatures.

A remarkably high responsivity is measured and is well in excess of one electron per photon even if all photons were absorbed which is not the case. If the absorption coefficient of Ge at 1.55 μm is assumed to be 460 cm^{-1} only 13.5% of the incident light is absorbed in the 5.4 μm thick Ge layer which corresponds to responsivity to be ~0.08 A/W. For an incident power of 10 μW at 1.55 μm, the responsivity is 3.5 A/W at −2 V and a temperature of 20 °C. It is proposed that the interface traps are filled by the photo-excited electrons. This trapped negative charge causes additional band bending leading to increased thermionic field emission by reducing the potential barrier. Similar light-induced barrier lowering has been previously observed in GaN ultraviolet

detectors [16] and in Cu-diffused Au-CdS diodes [17]. To confirm this current transport mechanism, the built-in potential at the Ge interface is measured using *C–V* under illumination (see Fig. 5-9). The Ge built-in potential increases gradually by increasing the incident optical power until it saturates (see inset of Fig. 5-11(b)). A considerable increase from 0.06 V (in dark) to 0.51 V (under illumination at a wavelength of 1.62 μm, 10 μW) at 20 °C demonstrates that the interface is unpinned and suggests that the photo-excited electrons are captured by the empty interface traps above E_F. As a result, the accumulation of holes at the Ge/Si interface increases which leads to a lower potential barrier and therefore higher current levels at a given reverse bias.

The responsivity as a function of wavelength at different temperatures and at two bias voltages is shown in Figs. 5-14(a) and 5-14(b) at two optical powers of 40 μW and 400 μW, respectively. The significant rise of the responsivity at −2 V at 20 °C compared to −1 V is likely to be due to the increase of the electric field at the Ge interface (Ge band bending) which in turn enhances the carrier transport by thermionic field emission (see inset of Fig. 5-11(b)).

Carriers contributing to the current when the device is under illumination are also available under dark condition; however, due to the larger potential barrier when dark, they do not contribute to the current. Although the dark current *density* of the devices compares very favourably with similar structures fabricated by epitaxy, the high responsivity of the 500 μm-diameter device is partially a result of the high dark current of the device. The other point is the non-uniform spatial distribution of free carriers in the presence of incident light; the laser beam is coupled to the device with an optical fibre which makes a spot size much smaller than the opening aperture of the device. This point in addition to the random distribution of the "thicker" region of the amorphous interfacial layer could cause the carriers to flow through the interface at specific locations of the active device region where the incident light beam is focused. In other words, incident light increases the conductivity of the spot through which the background current from across the device area would travel from Ge to Si. As a result, the larger device provides higher background current level than smaller devices and we think this could be the reason for the higher responsivity of larger devices compared to smaller ones. Nevertheless, detailed 2D simulations are required to consider "in-plane" electric field at the interface to be able to confirm this hypothesis.

To our knowledge this is the first report of light-gated responsivity for vertically illuminated Ge/Si photodiodes. Regarding the bandwidth of the devices, since trap filling is involved at the material interface which would affect the lifetime of the

carriers, we do not expect to get high speed performance from such devices; however, further investigations and characterizations are required which could be proposed as future work of this project.

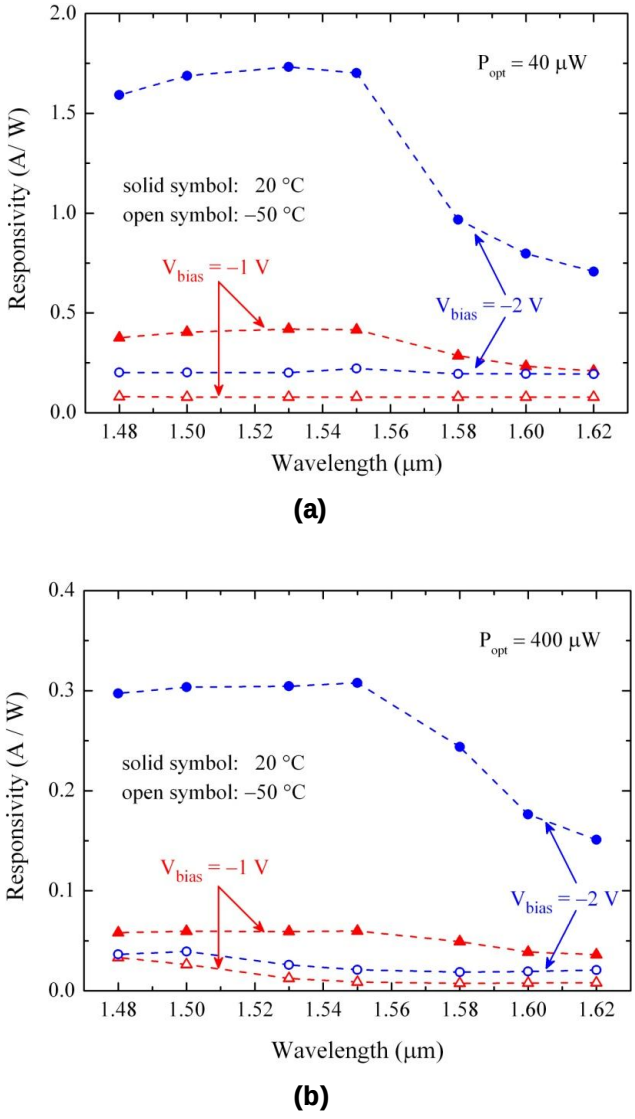
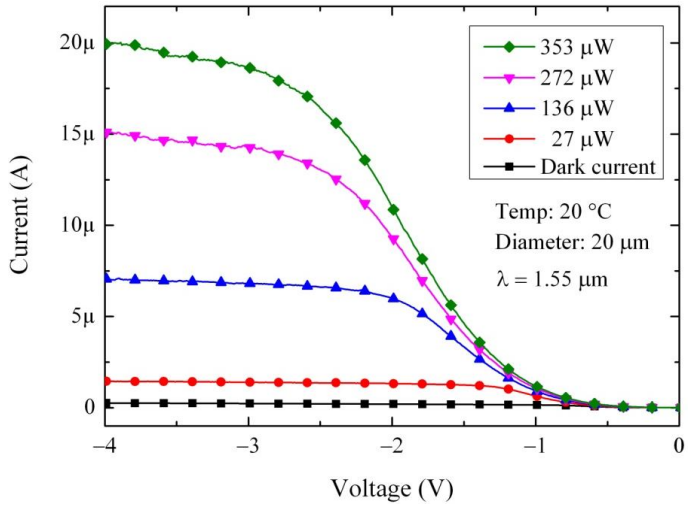


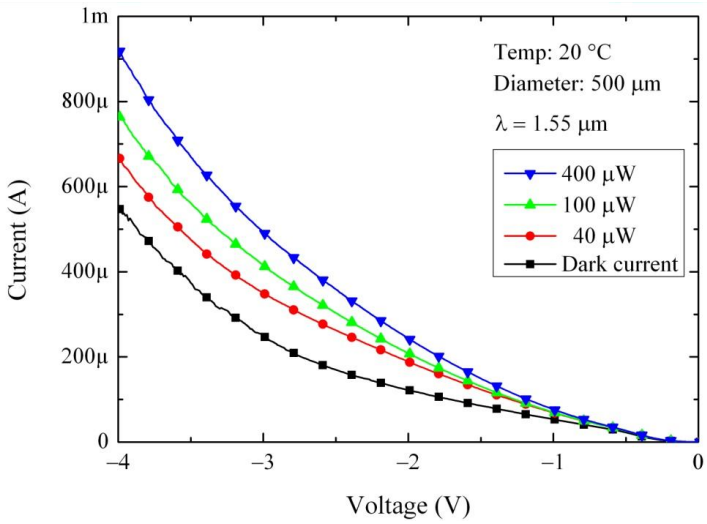
Fig. 5-14. Responsivity as a function of wavelength at different reverse bias voltages and temperatures and at a constant optical power of (a) 40 μW, and (b) 400 μW.

In addition to the large devices, small Ge on Si photodiodes with a diameter range from 20 μm to 80 μm were also fabricated which can be claimed to be the smallest normal incident photodiodes that have ever been fabricated using bulk wafers by the wafer bonding technique. There are two additional steps in the fabrication of small devices: planarization after the mesa etch step (using BCB and silicon nitride) followed by lifting-off contact pads.

Fig. 5-15 shows the *I–V* characteristics of two devices with different diameters (20 µm-diameter device in part (a) and 500 µm-diameter device in part (b)) in linear scale in dark and when the devices are under illumination. As can be seen in this figure, at a bias of −2 V, wavelength of 1.55 µm and optical power of 40 µW the responsivity of 1.6 A/W was measured for the larger device, but with the I_{TC}/I_{DC} ratio of ~1.5. For a 20 µm- and 30 µm-diameter devices a lower responsivity of 0.06 A/W and 0.3 A/W is measured with higher I_{TC}/I_{DC} ratio of 89 and 59, respectively. The reason for low responsivity of the 20 µm-diameter device could be due to the small opening aperture (diameter: 6 µm) compared to the beam spot (diameter: ~20 µm).



(a)



(b)

Fig. 5-15. *I–V* characteristics of the (a) 20 µm-diameter, and (b) 500 µm-diameter Ge on Si photodiodes. I_{TC}/I_{DC} ratio of the smaller device is larger than the large device.

5.4. Results and discussion - Si on Ge devices

In addition to the above mentioned devices, I was able to fabricate Si on Ge devices, as well as devices with diameters as small as 20 µm in diameter (opening aperture diameter: 6 µm) using identical material to that used in the previous section. However, in this experiment the Si wafer was thinned. Fig. 5-16 shows the schematic and the SEM image of the Si on Ge devices fabricated by wafer bonding. The fabrication steps are exactly as mentioned in the previous sections for the Ge on Si devices.

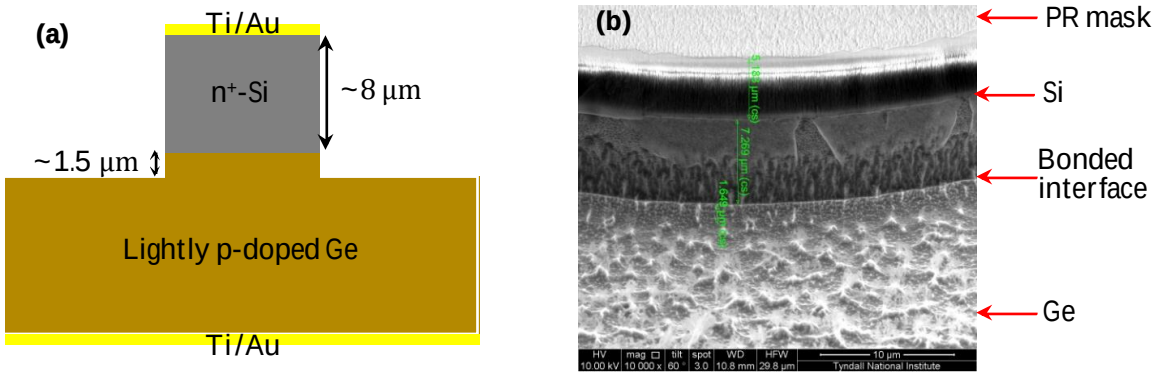


Fig. 5-16. (a) Schematic and (b) SEM image of the *pn* junction fabricated by wafer bonding followed by CMP. The structure is circular mesa.

Fig. 5-17 shows the *I*–*V* curves (dark current and total current, under microscope light) for two different devices at –40 °C. The characteristic clearly shows the rectifying behaviour of the *pn* junction which is an indication of the electric field expansion through the interface into the lightly p-type doped Ge. Since the thickness of the Ge layer in the mesa region is ~1.5 µm, by increasing the reverse bias voltage the electric field will expand laterally when it reaches the end of mesa. As a result the reverse bias voltage could be increased to 40 V without breaking the device/junction.

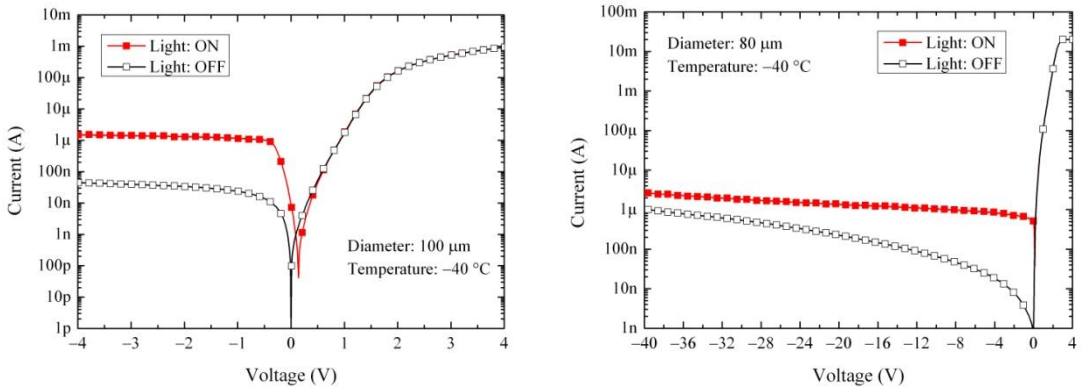


Fig. 5-17. Dark current and total current (under microscope white light illumination) of a 100 µm-diameter device (left) and an 80 µm-diameter device (right) for different bias voltage ranges.

Fig. 5-18 illustrates the *I–V* and *C–V* characteristics for a 100 µm-diameter device at –40 °C. The capacitance at 0 V confirms that the junction is already depleted at equilibrium and the electric field is already expanded and reaches the end of mesa height (the calculated depletion width at 0 V is ~2.17 µm while the Ge mesa height is 1.5 µm). Since by increasing the reverse bias voltage, the electric field expands laterally, the reverse current increases very slowly by applying the reverse bias voltage.

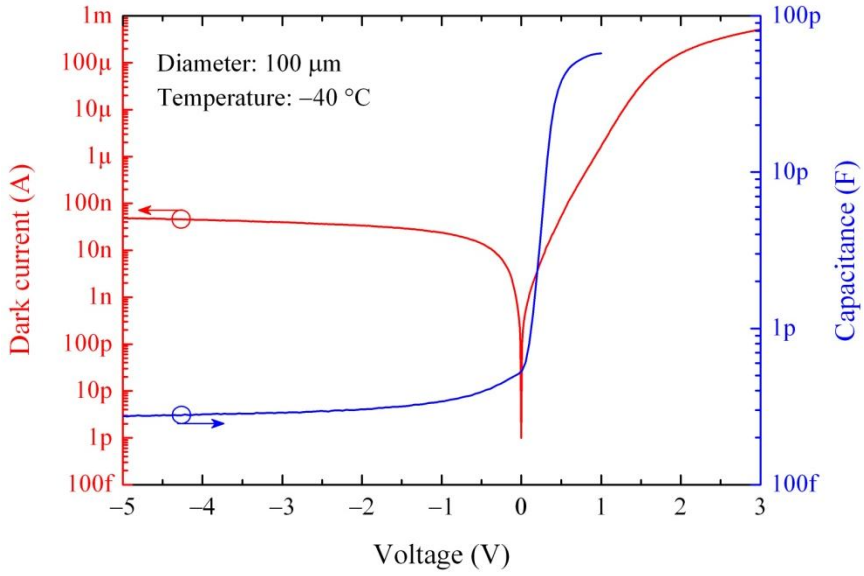


Fig. 5-18. *I–V* (left axis) and *C–V* (right axis) characteristics of a 100 µm-diameter device at –40 °C.

Electrical measurements were performed at different temperatures to analyze the characteristic of the *pn* junction at different temperatures. Fig. 5-19 shows the dependence of the dark current on temperature for a 100 μm-diameter device. As can be seen, the reverse bias current is considerably temperature dependent and the inset shows the average value of the activation energy at 2 V reverse bias.

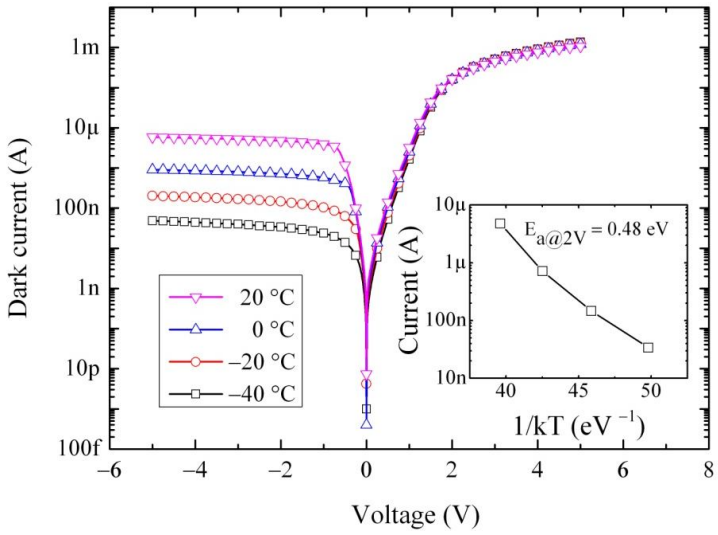


Fig. 5-19. Dark current of the 100 μm-diameter device at various temperatures. The inset shows the dependence of current on temperature and also the activation energy at 2 V.

Fig. 5-20 shows the SEM image of the Si on Ge interface for the 500 μm-diameter device with Ge thickness of ~4.4 μm. Fig. 5-21 shows the *I*–*V* characteristics of this device in dark and under illumination ($\lambda = 1.55$ μm, $P_{opt} = 630$ μW) at room temperature.

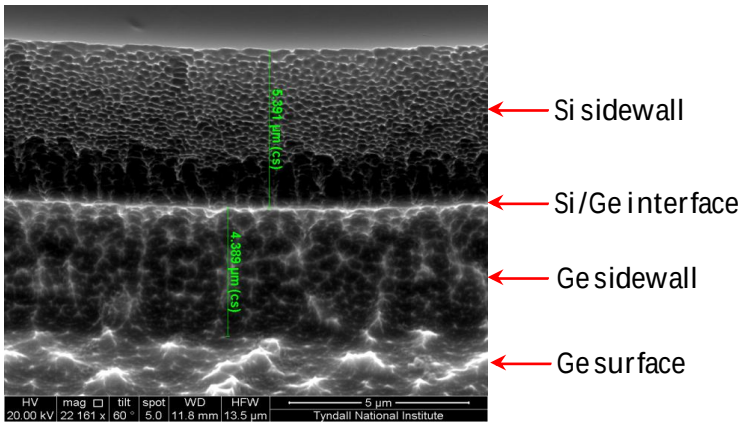


Fig. 5-20. SEM image of the Si on Ge cross section (circular mesa) made by wafer bonding.

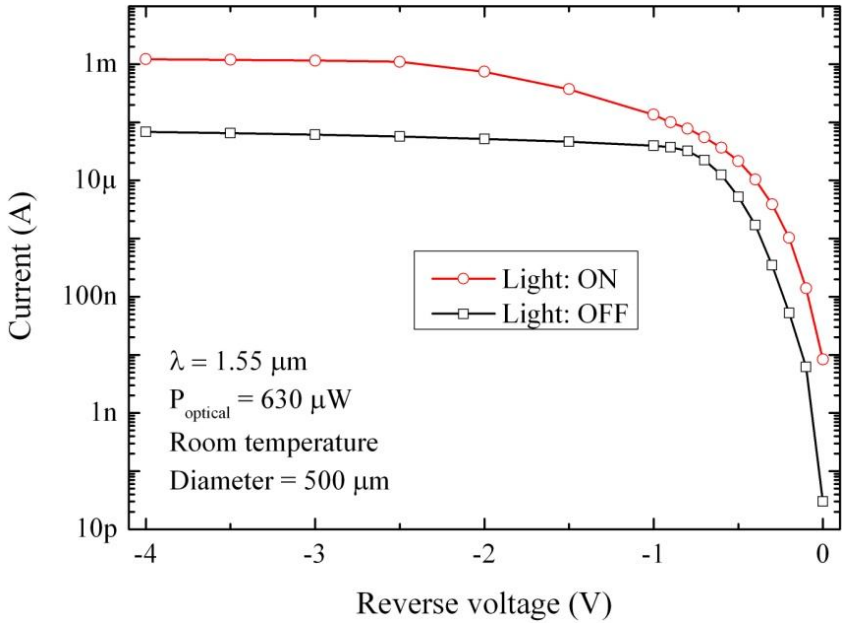


Fig. 5-21. *I–V* characteristics of the 500 µm-diameter Si on Ge photodiode.

The dark current density at 1 V and 4 V reverse bias is 20 mA/cm^2 and 35 mA/cm^2, respectively, which is almost the same as the Ge on Si devices and compares favourably with the devices in literature made by epitaxy. The responsivity of the Si on Ge device at 1 V and 4 V reverse bias and at $\lambda = 1.55$ µm is 0.15 A/W and 1.83 A/W, respectively.

Table 5-1 compares the fabrication parameters and the device characteristics of various vertical illuminated Ge/Si photodetectors manufactured by different groups with the integration technique and the devices fabricated here. As can be seen, the maximum process temperature of wafer bonding technique is 450 °C (CMOS-compatible). The dark current density of the devices compares very favourably with the reported heterojunction photodetectors. The responsivity of the device is much higher than previously reported ones (especially at higher bias voltages; i.e., at −2 V). The values of responsivity at different reverse bias voltages and different temperatures are obtained from Figs. 5-14(a) and 5-14(b) where the input optical power is 40 µW. As shown in Fig. 5-13, higher responsivities are obtained at lower optical powers.

Table 5-1. Performance comparison of different vertical illuminated Ge/Si photodetectors. Abbreviation definitions are as follows – CVD: Chemical Vapour Deposition; RP: Reduced Pressure; UHV: Ultra High Vacuum; LP: Low Pressure; MBE: Molecular Beam Epitaxy; LEPE: Low Energy Plasma Enhanced; MHAH: Multiple Hydrogen Anneal Heteroepitaxy; QD: Quantum Dot; ARC: Anti Reflection Coating; RC: Resonant Cavity.

Fabrication technique	Structure	Ge thickness (μm)	Max. Process Temp. (°C)	Device diameter, D / area, A	Dark current density (mA/cm²)	Responsivity (A/W) @ λ = 1.55 μm	Ref.
RP-CVD	pin-Ge on n-Si	4.11	650	D=90 μm	10.5 § @ −1 V	0.94 (with ARC)	[18]
	nip-Ge on n-Si	1	670	A=4×10⁻⁴ cm²	1-2 @ −1 V	0.15-0.2 @ −1 V	[6]
	pi-Ge on n-Si	1.2	650	D=17 μm	18 § @ −1 V	0.47 @ −1 V	[10]
UHV-CVD	ni-Ge on p-Si RC	0.737	900	D=30 μm	275 § @ −1 V	0.175 § @ −2 V	[19]
	ni-Ge on p-Si	4	900	-	30 @ −1 V	0.5 @ −1 V	[20]+ its [15]
	nip-Ge on p-Si	~1	900	D=30 μm	20 @ −1 V	0.2 @ 0 V	[6]
	pi-Ge on n-Si	1	600	A=50×50 μm²	40 § @ −1 V	0.23 @ −1 V	[12]
	i-Ge on n-Si	1.1 μm SiGe + 2.6 μm Ge	750	D=20 μm	3.6 @ −1 V	0.57 @ −2 V (λ = 1.3 μm)	[2]
	pi-Ge on n-Si	1	800	D=30 μm	16 @ −1 V	0.31 @ −1 V	[21]
LP-CVD	ni-Ge on p-Si	2	800	A=20×20 μm²	8 §@ −1 V	0.3 @ −1 V	[22]
MBE	pin-Ge QD	0.01	550	A=150×300 μm²	0.03 @ −1 V	0.1 § @ −2.5 V	[23]
	nip-Ge on p-Si	0.3 GeSn	850	D=80 μm	10000 @ −1 V	0.1	[24]
LEPE-CVD	pin-Ge on n-Si	3	780	D=3 mm	0.37 @ −1.5 V	0.21 @ −1.5 V	[25]
	pin-Ge on n-Si	3	780	D=3 mm	38 @ −1 V	0.55 § @ −0.5 V	[13]
MHAH	nip-Ge on p-Si	1	800	A=π×10⁴ μm²	~17 § @ −1 V	~0.64 @ −1 V	[26]
Wafer bonding	**p-Ge on n-Si**	**5.4**	**400**	**D=500 μm**	**25 @ −1 V (20 °C) 48 @ −2 V (20 °C) 1.7 @ −1 V (−50 °C) 5 @ −2 V (−50 °C)**	**0.42 @ −1 V (20 °C) 1.7 @ −2V (20 °C) 0.08 @ −1 V (−50 °C) 0.22 @ −2 V (−50 °C)**	**This work**

§ Data calculated using the referenced material.

5.5. Conclusions

In conclusion, we have demonstrated photodetectors with sensitivity to 1.62 μm and with above unity responsivity by low temperature wafer bonding of Ge to Si.

The wafer bonding recipe was developed to increase the Ge-to-Si bond strength which

is critical for substrate thinning steps which were also developed. A longer plasma treatment followed by anneal steps were performed to improve the adhesion. By taking TEM images of the interface no defects or dislocations was observed in neither of the Si nor the Ge side of the bonded pair; however, two types of interfacial regions (thin and thick regions) were recognized.

The devices exhibited well pronounced rectifying behaviour current–voltage characteristics. *I–V* measurements at various temperatures revealed that the reverse current is considerably temperature dependent which is an indication of the presence of interface traps.

A number of experiments were conducted to understand the physics of the interface and the role of interface traps. Performing *C–V* measurements at various temperatures and frequencies revealed that the interface traps are less effective at lower temperatures while at higher temperatures they are thermally active. The interface charge density and the density of occupied traps below Fermi level in dark were found to be 1.26×10^{-8} C/cm^2 and 7.88×10^{10} cm^{-2}, respectively

Although the results of the photodiodes are preliminary, high responsivity was obtained for both Ge-on-Si and Si-on-Ge photodiodes (large devices). However, the high photo-response is due to the presence of high density of interface traps. Trap filling affects the lifetime of the carriers and as a result limits the bandwidth and speed of the devices. Further measurements and investigations are required to obtain the bandwidth of the devices.

The influence of interface charges and the role of interface traps were discovered by monitoring the surface potential of the Ge at different temperatures as well as in dark and under illumination. Based on these observations, a detailed band diagram of the Ge/Si bonded interface was proposed, the band alignment of the Ge and Si was shown to be offset and the Ge bands were shown to shift both with temperature and under illumination due to hole accumulation at the Ge interface resulting in an increase in current providing the high response. This was the first report regarding the light-induced potential barrier lowering of Ge/Si bonded pair.

A hypothesis has been proposed regarding the role of incident light and its influence on the conductivity of the interface “locally” at the beam spot location which requires detailed 2D simulations considering “in-plane” electric field at the interface to be able to confirm this hypothesis.

Owing to the high responsivity and compatibility with CMOS processing, these devices are suitable to be integrated with Si-based read-out circuits for applications such as high-performance near infrared imaging. However, due to the dependency of the current transport mechanism on temperature, temperature should be kept constant.

5.6. References

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Chapter 6: Conclusions and future work

This dissertation addresses the issues related to the integration of germanium as an absorber material in near infrared wavelengths with silicon as a platform to fabricate photodetectors. The primary goal of this thesis was to investigate and develop the use of silicon-germanium as a material system for near infrared photodetection. This includes the challenges of material modelling, heterostructure design, and device design, fabrication and characterization.

In the preceding chapters, the two main integration approaches, i.e., hetero-epitaxy and wafer bonding were explored. Furthermore, the basic processes necessary for the fabrication of Ge/Si long wavelength photodetectors were demonstrated. Also, fundamental physical mechanisms of the carrier transport in the fabricated devices and the electrical/optical properties of the bonded interface were investigated. The following section presents the key conclusions of the previous chapters. Future work necessary to develop the materials integration through both epitaxy and wafer bonding techniques and some of the possible applications are proposed.

6.1. Summary and conclusions

In Chapter 2 Ge/Si separate absorption, charge and multiplication (SACM) avalanche photodiodes (APDs) were investigated. The influence of the absorption thickness and doping, along with the charge and multiplication layer doping on the gain-profile, the breakdown voltage and the gain-bandwidth product were determined.

The influence of interface donor and acceptor traps on the static and dynamic behaviour of Ge/Si SACM APDs was explained in Chapter 2. The effects of different trap types, densities and carrier capture cross sections on the dark current level, breakdown voltage, DC gain, and electric field profile as well as on the frequency response and gain-bandwidth product of the device were also investigated. The results show that the interface traps significantly increase the dark current and reduce the gain. It has also been shown that the acceptor traps reduce the APD bandwidth considerably while the donor traps increase the bandwidth.

In Chapter 3 I reported on my investigations on an epitaxial approach to achieve Ge/Si APDs. The germanium film was grown by the Low Energy Plasma Enhanced Chemical Vapour Deposition (LEPE-CVD)[1] technique. The structure and the layout that were used to fabricate the APDs as well as different techniques to characterize the Ge and Si epilayers are presented in this chapter. The origin of the high dark current was analyzed and discussed. It has also been shown how the possible reasons for leakage current in the devices were located by removing the germanium film and fabricating devices on silicon wafers. We also examined the silicon wafers using KOH, showing a large density of dislocations after etching. The effects of low and high temperature anneal on the device characteristics are also presented in Chapter 3.

In Chapter 4 we reported on the formation and electrical characterization of current transport across a p–Ge to n–Si diode structure obtained by direct wafer bonding and layer exfoliation. It has been shown that a low temperature anneal at 400 °C for 30 minutes improves the forward characteristics of the diode: the ideality factor of the diodes was reduced from 5.48 to 2.28; the forward resistance also showed a reduction from 245 Ω to 15 Ω. The I_{on}/I_{off} ratio ~5×10^4 and ~8×10^3 is obtained at –0.5 V and –1 V, respectively. The carrier transport mechanism was analyzed in this chapter based on the current-voltage and capacitance-voltage measurements and direct tunnelling is suggested as the transport mechanism. It has been demonstrated that although the maximum process temperature was 400 °C the bond strength between the two wafers is high enough to tolerate all the mechanical and thermal stresses of different manufacturing processes. The advantage of this low temperature integration technique is that the devices proposed in the dissertation can be fabricated in a standard silicon foundry without significantly altering the process flow.

Chapter 5 presents the experimental results of a light-gated photoresponse from an asymmetrically doped p^--Ge/n^+-Si heterojunction photodiode fabricated by wafer bonding followed by wafer thinning. Responsivities in excess of 3.5 A/W at 1.55 μm at −2 V were measured with a 5.4 μm thick Ge layer under surface normal illumination. Capacitance-voltage measurements revealed that the interfacial band-structure is temperature dependent, moving from depletion of holes at −50 °C to accumulation at 20 °C. Interface traps filled by photo-generated and thermally-generated carriers are shown to play a crucial role. Based on the experimental results, a detailed description

[1] The germanium heteroepitaxy was done in collaborative work with Dr. G. Isella's group from Polytechnic University of Milan - Pole of Como; L-NESS: Laboratory for Nanostructure Epitaxy and Spintronics on Silicon http://lness.como.polimi.it/giovanniisella.php

of the physics of carrier conduction mechanism and the band diagram at Ge/Si interface has been provided in this chapter. It has been explained that interface trap filling alters the potential barrier height at the interface leading to increased current flow and hence, the above unity responsivity. The results of Chapter 5 are the most significant of this thesis, and yet they are the most preliminary.

6.2. Novel contributions of the work

This section highlights the novel contributions of this PhD project:

- Modelling the effects of Ge/Si interface traps on the performance of Ge/Si APDs
- Fabricating Ge/Si *pn* junction by low temperature wafer bonding and layer transfer or layer exfoliation
- Developing the back-etch process for both Si and Ge materials of a bonded pair
- Fabricating Ge/Si normal incident photodiodes showing remarkably high responsivity by low temperature wafer bonding and back-etch process (grinding and polishing)
- Proposing detailed band-diagram of the Ge/Si interface based on the experimental observations and results

6.3. Recommendations for future work

There is a need for CMOS integrated, low cost and high efficiency optical detectors sensitive to wavelengths beyond that of silicon (1 μm). Applications in measuring and imaging await as do applications in communication receivers. Over the past decades, conventional optical components were typically made of III–V compound materials such as gallium arsenide and indium phosphide due to their excellent light emission and absorption properties. Unfortunately, compound-semiconductor devices are generally complicated to process and costly to implement. More importantly, their fabrication processes are not compatible with CMOS.

In the search for a cost-effective solution, Ge can be used because it is CMOS-compatible. Different approaches for Ge/Si integration have been investigated. Those using high-temperature growth or post-growth heat treatments are not only far beyond the thermal budget of CMOS but lead to inter-diffusion of Si and Ge. The

lowered Ge concentration in the absorption region increases the active region band gap, resulting in a reduced absorption coefficient particularly at longer wavelengths. Epitaxial growth suffers from the number of process steps which need to be done in special systems (e.g. MBE or UHV-CVD) as well as additional ion implantation steps. Deposition of Ge into selected regions with and without re-melting have been more successful but at the expense of high temperature steps and these detectors are only suitable for in-plane waveguide detection when used in a silicon on insulator (SOI) platform. Among other techniques wafer bonding has been proposed for realising waveguide photo-detectors. To date, the conductivity across the interface has not been suitable for high quality photodetectors.

The experiments reported in the final chapter of this thesis explored the feasibility of using low temperature Ge/Si wafer bonding for the purpose of photodetection. These devices with a conductive interface show high responsivity and low dark current density. This paves the way for the manufacturing of CMOS-compatible Ge/Si photodetectors in a two dimensional array configuration connected to on chip electronics as could be used in a high performance camera where high speed performance is not required (due to the presence of traps).

From the modelling perspective, it is crucial to fully understand and predict the physics of the Ge/Si interface by proposing a model which deals with the semiconductor / dielectric / semiconductor structure and demonstrate the vital effects of interface traps and light-induced band bending enhancement in germanium.

Additional theoretical investigations through precise modelling are also crucial to understand the peaking effect in the APD frequency response in the presence of donor traps as demonstrated in Chapter 2. I believe the interface traps are adding a phase delay and in the case of the donors the phase delay added to the multiplication time and transit time phase delays is sufficient to cause peaking. This requires further investigations.

From the perspective of material science, developing the silicon epitaxial process to grow high quality thin layers of charge and multiplication regions (with considerable dopant gradient) is also proposed for the pursuit of the Ge/Si avalanche photodiode fabrication. Other germanium growth techniques, such as growing germanium film selectively on graded SiGe buffer layers is proposed as an alternative in the fabrication of Ge/Si APDs. Wafer bonding could also be employed; however, due to the complexity of the interface, wafers with simpler structures, such as a PIN structure, should be

considered prior to bonding wafers with complex structures and therefore complicated physics, which is under investigation at the moment.

Appendices

A1. Details of wafer bonding

In general, the process of direct wafer bonding can be divided into the following steps:

1) Surface cleaning;
2) Surface activation; and
3) Applying force and heat treatment

Wafer surfaces have to be free from contaminations, such as particles, organic and ionic residues. The presence of particles on the wafer surface results in the creation of voids at the interface. Organic contamination results in weak bonding strength and also interfacial voids. Usually, particulates and organic contaminations can be removed by standard cleaning solutions, such as SC1 wet chemical cleaning process in which the wafers are dipped in $NH_4OH:H_2O_2:H_2O$=1:1:5 followed by a de-ionized (DI) water rinse. SC2 solution ($HCL:H_2O_2:H_2O$=1:1:5) could be used to remove metallic contaminations.

In this thesis a Semitool Spray Acid Tool (SAT) is used to clean the wafers. These cleans include pre-oxidation, hot DI water plus ozone gas and HF final clean for complete oxide removal, if required. The Semitool SAT is a single chamber tool equipped with Ozone, HF and NH_4OH chemistries. This tool utilizes a process known as HydrOzone™ using DI water and ozone gas.

A1-1. Description of cleaning process

The cleaning solution is sprayed across the wafers at an elevated temperature (~75 - 90 °C) as they rotate in the process chamber forming a thin boundary layer on the surface of the wafers. Dry ozone gas is then admitted to the chamber. The ozone diffuses through the thin boundary layer of water and then the water hydrolyzes the C-C and C-H bonds, making them susceptible to attack by the O_3. The hot water maximizes the reaction rate. Reaction by-products are carried away in the boundary

layer. Once the clean step is completed, ozone flow is stopped and a short rinse is initiated.

Where the HydrOzone™ process is highly effective at oxidizing organic material, it fails to address the additional criteria of comprehensive cleans: particle contamination, metallic ion contamination, and removal and regeneration of passivating oxide film. Therefore, HydrOzone™ is combined with HF (FlourOzone™) to address all these issues. The wafer surface is oxidized by the HydrOzone™ (O_3:H_2O). Simultaneously the HF, which is injected into the DI water stream (usually at low injection rates 850:1) removes the oxide layer. This oxidization and strip continues as long as the FlourOzone™ process runs. Particles are removed by three methods: oxidization and removal of organic particles through the presence of H_2O and O_3; lift-off of particles through the build-up and removal of oxide layers; and removal of metallic particles by the dissolution reaction due to HF, assisted by the oxidizer O_3. However, since ozone is a strong oxidizing agent the Ge wafers were cleaned without ozone [1].

Depending on the chemicals that are used for the purpose of surface cleaning, two types of surfaces will be achieved: hydrophilic (water loving) or hydrophobic (water fearing) surfaces. In hydrophilic surface a thin surface oxide with hydrophilic hydroxyl termination groups are created on the surface. The presence of these hydroxyl groups has been shown to increase the bond strength of the bonded structure [2].

Radical activation of the wafers is a key factor for the success of low-temperature bonding [3]. The effects of free radical activation for Si to Si bonding and Ge to Si bonding have been previously reported in the literature [1, 4]. In that study, a comparison of different surface treatments for direct Si to Si wafer bonding was made. Hydrophilic and hydrophobic Si wafers were exposed to a range of pre-treatments, involving oxygen and nitrogen radical activation before bonding the wafers in vacuum. After wafer cleaning and prior to bonding, wafers surfaces were exposed to oxygen radicals in the bonder chamber using a remote *in situ* surface activation tool. During the exposure the chamber pressure was 1 mbar and the power was 100 W. This surface activation step improves the hydrophilicity of the surface (or converts hydrophobic surfaces to hydrophilic ones) by growing a thin layer of highly reactive native oxide, subsequently resulting in a high density of –OH groups (i.e., hydroxyl groups) on the sample surfaces after contacting with H_2O-based solutions.

After bonding the two wafers at room temperature via relatively poor Van der Waals forces or hydrogen bonds, the well-known chemical reactions start forming strong

covalent bonds by means of chemical reactions and rearrangement of atoms at the bonded interface [5]. This process is accelerated by further annealing at an elevated temperature. The different coefficients of thermal expansion between the two materials can lead to thermal stress in the wafers which in turn may cause delamination while/after annealing. Low-temperature bonding eliminates the severe thermal stress that can be induced by high-temperature annealing. The gas by-products of H_2O and H_2 from the chemical reactions can accumulate and cause interfacial voids at the bonding interface. Removing the gas by-products efficiently is therefore a critical step in obtaining high-quality low temperature bonding. This could be done by patterning grooves which has been reported to be led to crack-free interfaces [6] or by further annealing step(s).

A2. Spreading resistance profiling (SRP)

The spreading resistance concept is illustrated in Fig. A2-1 [7].

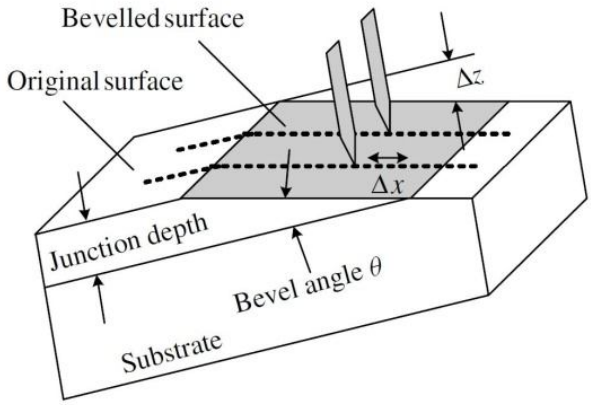


Fig. A2-1. Spreading resistance bevelled sample with probes - the probe path is shown by the dashed line.

The spreading resistance instrument consists of two probes that are stepped along the bevelled semiconductor surface. The resistance between the probes is given by:

$R = 2R_p + 2R_c + 2R_{sp}$

where R_p is the probe resistance, R_c the contact resistance and R_{sp} the spreading resistance. The resistance is measured at each location.

To understand spreading resistance, consider a metallic probe contacting a semiconductor surface as in Fig. A2-2.

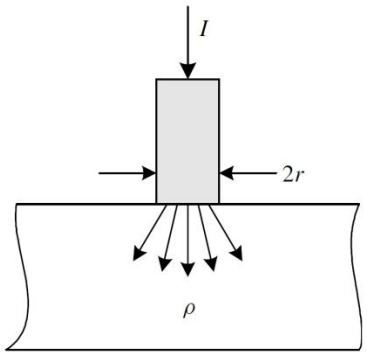


Fig. A2-2. A cylindrical contact of diameter 2*r* to a semiconductor. The arrows represent the current flow.

The current I flows from the probe of diameter $2r$ into a semiconductor of resistivity ρ. The current is concentrated at the probe tip and spreads out radially from the tip. For a cylindrical contact with a planar, circular interface and a highly conductive probe, the spreading resistance is:

$$R_{sp} = \rho / (4r)$$

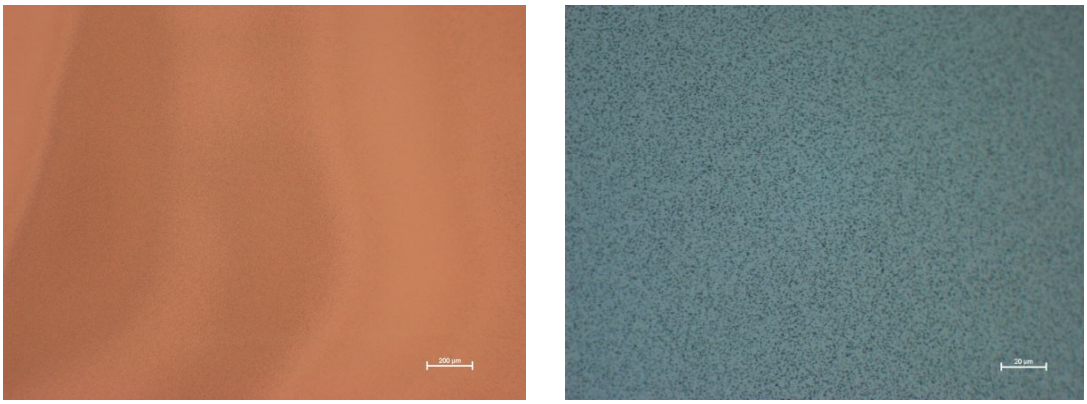
This equation should be verified by comparing spreading resistance with four-point probe measurements and as a result a correction factor (C) that depends on sample resistivity, probe radius, current distribution and probe spacing needs to be applied. Hence,

$$R_{measured} = R_{contact} + \rho / (2r) \times C$$

The contact resistance also depends on wafer resistivity and probe pressure and on the density of surface states.

A3. Defective regions of the UPSW and the *I–V* characteristics

Optical images of the Si wafer surface at two different magnifications are shown in Fig. A3-1.



(a) **(b)**

Fig. A3-1. Optical image of the structured Si wafer designed for Ge/Si detector at two different magnifications. The scale bar in (a) is 200 μm and in (b) is 20 μm.

The designed structure of the wafers is shown in Fig. A3-2. The *pn* junction is at the charge and multiplication layers.

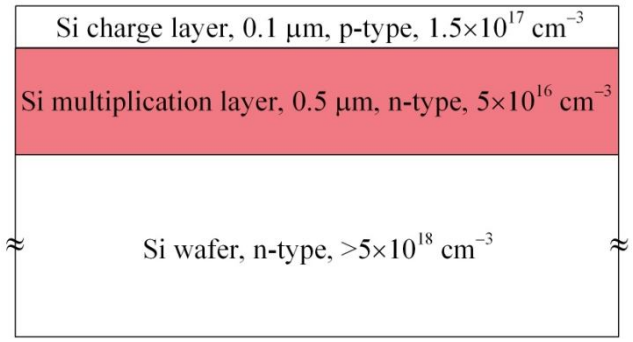


Fig. A3-2. Schematic of the UPSW structure designed for Ge/Si detector.

Fig. A3-3 shows the *I–V* characteristics of the devices made using this set of wafers. It looks more like a resistor than a diode. The very high leakage current is probably due to the defects in the Si wafers.

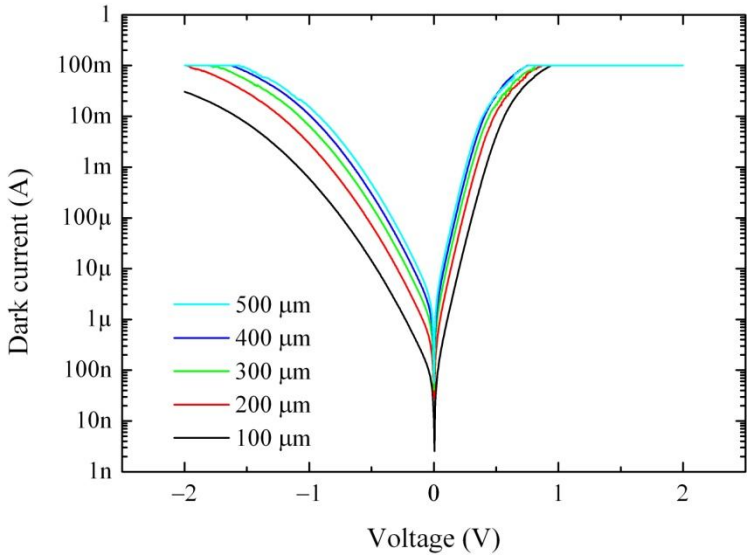


Fig. A3-3. *I–V* characteristics of the devices made using the UPSW.

A4. Germanium and silicon processing parameters

Wet etching: One of the most common solutions for etching germanium is $NH_4OH:H_2O_2:H_2O$. In order to investigate the parameters of this etching solution a number of etch tests were performed and the following results were obtained:

1) The average etch rate for the ratio of 1:7:40 is ~175 nm/min; and
2) The etch rate reduces slightly with time (5 nm/min reduction in the etch rate after ~15 min).

SEM images in Fig. A4-1 show that this is an isotropic etch (the under cut is clearly shown in the figures).

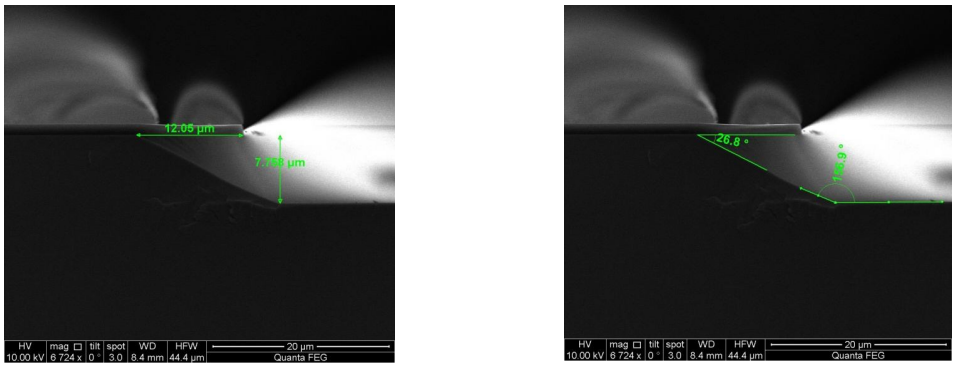


Fig. A4-1. SEM images of the etched Ge sample using $NH_4OH:H_2O_2:H_2O$ after 45 minutes.

Dry etching: Different etch conditions as well as gas combinations were analysed on the etching of germanium. The effect of coil power and Cl_2 gas on the germanium etch rate is considerable, such that by increasing the coil power to 1000 W the etch rate reaches 538 nm/min (Run 5) and by increasing the Cl_2 gas flow the germanium etch rate increases to 516 nm/min (Run 7). The summary of the dry etch experiment is shown in Table A4-1.

Table A4-1. Effects of experimental setup parameters and plasma gases on Ge etch rate. ER: Etch Rate; S: Selectivity.

	BCl_3 (sccm)	Cl_2 (sccm)	Coil power (W)	Platen power (W)	Ge ER (nm/min)	Oxide ER (nm/min)	S
Run 1	30	-	400	75	≈ 100	22.5	≈ 4.4
Run 2	30	-	800	75	The entire mask was etched.		
Run 3	30	-	400	75	85	2.5	34
Run 4	30	-	400	125	105	5	21
Run 5	100	40	1000	100	538	53	≈ 10.2
Run 6	100	40	600	75	275	5	55
Run 7	40	100	600	75	516	20	25.8

SEM images of Run 6 and Run 7 are shown in Figs. A4-2 and A4-3, respectively. By comparing these figures, the germanium surface is smoother for Run 7 than for Run 6.

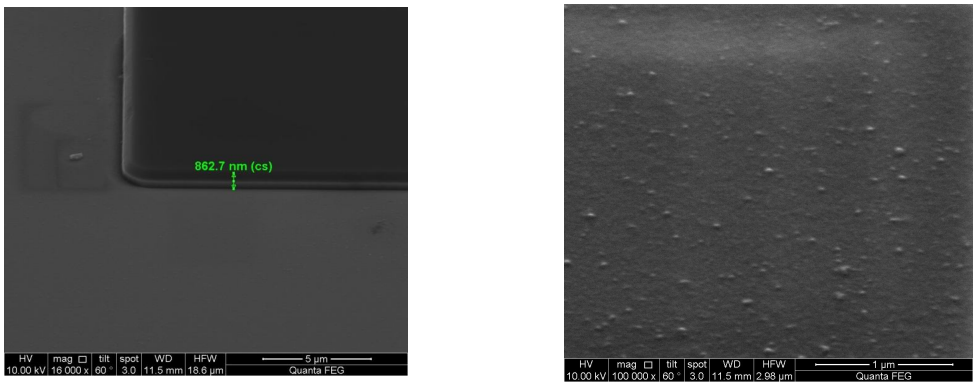


Fig. A4-2. SEM images of the germanium sample after 1 min of Run 6. The image on the right shows the surface of Ge after etching.

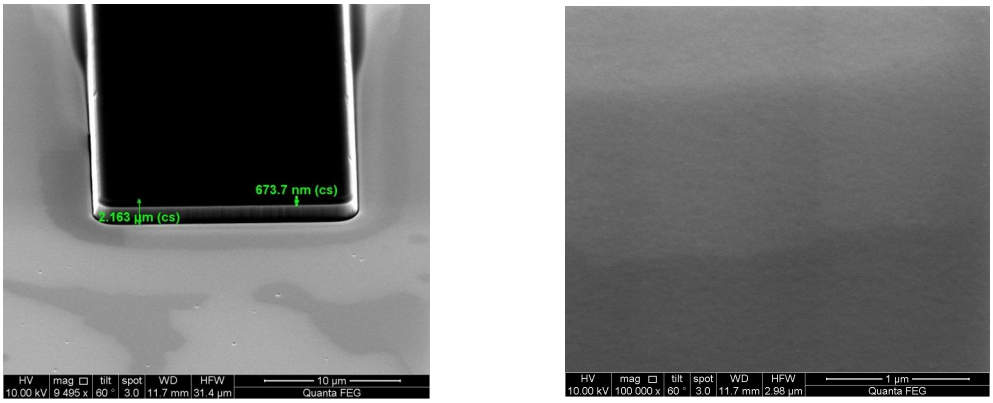


Fig. A4-3. SEM images of the germanium sample after 2 min of Run 7. The image on the right shows the surface of Ge after etching.

In order to create a mesa structure, both germanium and silicon should be etched. Therefore, the etching parameters of SF_6 and C_4F_8 for both silicon and germanium were investigated. In this test the coil and platen powers were set to 600 W and 15 W, respectively. The results are shown in Table A4-2.

Table A4-2: Si and Ge dry etch results using SF_6 and C_4F_8. ER: Etch Rate; S: Selectivity; PR: Photoresist.

	SF_6 (sccm)	C_4F_8 (sccm)	ER (nm/min)	PR ER (nm/min)	S
Silicon	40	90	123	28.5	4.32
Germanium	40	90	143	29.2	4.9

A5. Layer structure of the APD wafers and the device mask layout

Fig. A5-1 shows schematically the layer structures of the wafers that were designed for the Ge/Si APD. Table A5-1 shows the wafer number corresponding to each wafer (different germanium layer thicknesses). As mentioned in Chapter 3, the germanium layers were grown by LEPE-CVD technique.

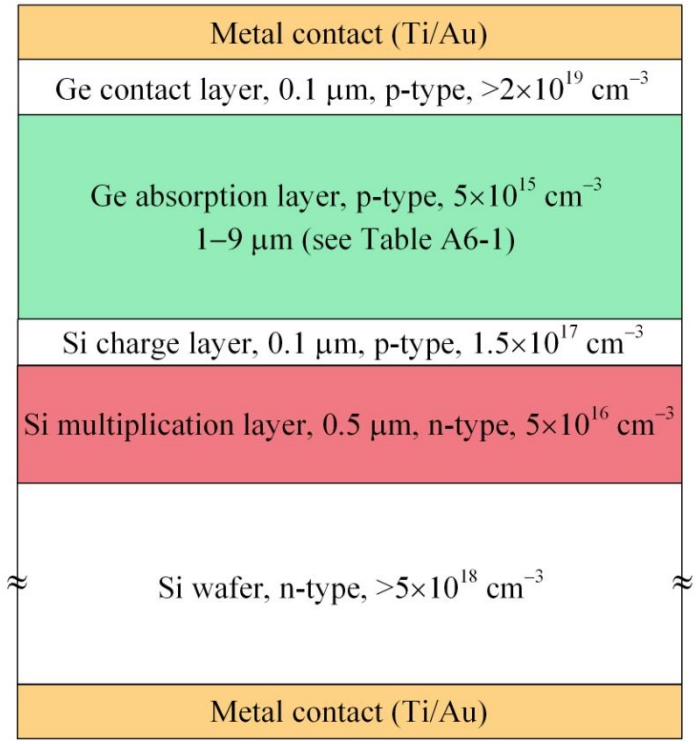
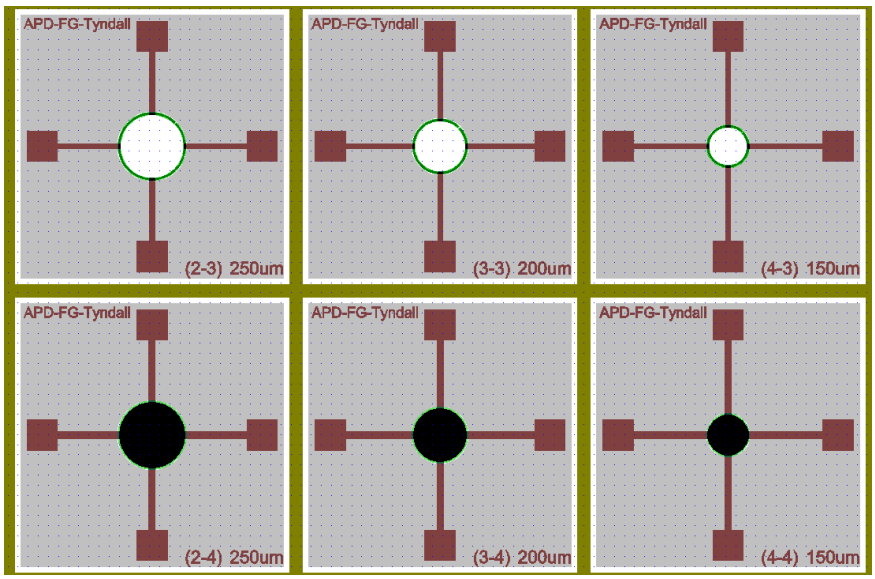


Fig. A5-1. Schematic cross-sectional view of different layers of the epitaxial Ge/Si APDs.

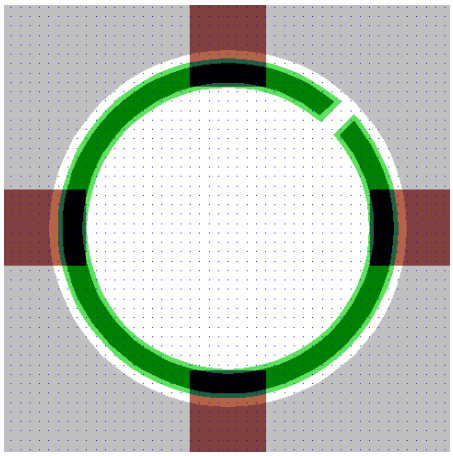
Table A5-1: Wafer number and the corresponding Ge layer thickness.

Wafer number	Ge thickness (μm)
8511	1
8515	1.5
8517	4.5
8523	6
8528	8
8536	9

Fig. A5-2(a) shows part of the mask layout. The first level in the mask layout is the top p-metal contact. This layer is shown as green rings (for devices with a top open aperture) and black circles (for devices without a top open aperture; for the purpose of dark measurement). The second level is the mesa etch in circular and square geometries. The gray region shows this step. The third level is the pattern to open the oxide (dark green region in Fig. A5-2(b)). The last lithography step is the contact pads (red regions).



(a)



(b)

Fig. A5-2. Mask layout of Ge/Si devices at (a) lower magnification, and (b) higher magnification (one device).

A6. References

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