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Hardware Reduction in Digital Delta–Sigma Modulators Via Error Masking—Part I:
MASH DDSM

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Abstract—Two classes of techniques have been developed to whiten the quantization noise in digital delta–sigma modulators (DDSMs): deterministic and stochastic. In this two-part paper, a design methodology for reduced-complexity DDSMs is presented. The design methodology is based on error masking. Rules for selecting the word lengths of the stages in multistage architectures are presented. We show that the hardware requirement can be reduced by up to 20% compared with a conventional design, without sacrificing performance. Simulation and experimental results confirm theoretical predictions. Part I addresses MultistAge noise Shaping (MASH) DDSMs; Part II focuses on single-quantizer DDSMs.

Index Terms—Digital delta-sigma modulators (DDSMs), error masking, MultistAge noise Shaping (MASH).

I. INTRODUCTION

D IGITAL DELTA–SIGMA modulators (DDSMs) are often found in consumer communications and entertainment products including cellular telephones, wireless LANs, modems, and MP3 players. The fundamental operation of the DDSM is to quantize an oversampled discrete-amplitude input signal coarsely within a feedback loop such that the power of the resulting quantization noise is shaped within some frequency band of interest. Popular DDSMs are based on two classes of DSMs called MultistAge Noise Shaping (MASH) DDSMs and single-quantizer (SQ) DDSMs [1]. MASH DDSMs have a feedforward structure and are inherently stable. SQ DDSMs typically incorporate one or more feedback loops and must be designed with care to ensure stability.

Careful DDSM design is also important because modulator imperfections directly affect the purity of the output spectrum of the system in which they are used. One of the most challenging issues is the tonal behavior of the DDSM [2]. Occasionally, the causes of the tonal behavior in a DDSM are the cycles that are particularly likely to occur with slowly varying or dc inputs.

The underlying problem is that the randomization of the outputs by the DDSM is often insufficient and the resulting quantization error forms short and repeating patterns (called cycles); this gives rise to strong unwanted tones in the output spectrum [2].

Two classes of techniques have been developed to whiten the quantization noise: deterministic and stochastic. The deterministic approach to whitening the quantization noise is to guarantee maximum cycle lengths by design. Kozak and Kale [3] and, more recently, Borkowski et al. [4], [5] have shown that the MASH DDSM does not exhibit large spurs when the input is constant and the initial condition of the first stage is odd, due to the inherent whitening of the quantization error spectrum.

The “stochastic” approach to maximizing cycle lengths is to use a “random”1 dither signal to disrupt periodic cycles [6]. Dithering breaks up the cycles and increases the effective cycle length, resulting in smooth noise-shaped spectra. Although the stochastic solution inherently adds noise to the spectrum, it is particularly effective when the word length of the DDSM is short, in which case the deterministic technique cannot guarantee a sufficiently long cycle to whiten the quantization error.

In an earlier work [7], we proposed a reduced-complexity (RC) MASH DDSM which maximizes cycle lengths in a deterministic way without dithering. In this paper, we extend this idea, develop the method theoretically, and show how error masking can be used to reduce the hardware consumption (HC) of MASH DDSMs, using either deterministic or stochastic techniques. In Part II, we will focus on SQ DDSMs [8], [14].

In Section II, we review a typical architecture for a MASH DDSM. In Section III, we explain the design methodology for the DDSM using the deterministic technique. In Section IV, a design example for the DDSM using the deterministic technique is shown. In Section V, the design methodology for MASH DDSMs using the stochastic technique is presented. In Section VI, a design example for the stochastic technique is shown. Finally, we draw some conclusions in Section VII.

II. MASH ARCHITECTURES

Before we explore our design methodology in detail, we first review a conventional MASH DDSM architecture. The structure we consider is based on the digital accumulator model shown in Fig. 1.

1The dither signal is typically produced by a finite state machine. In this case, it is pseudorandom rather than random.
flow operation. The signal $v[n]$ is the sum of the digital words $x[n]$ and $w[n]$. When $v[n]$ is greater than $2^N$, the quantizer overflows, and the output signal $y[n]$ will be 1 (i.e., truncating quantizer). On the other hand, when $v[n]$ is less than $2^N$, the quantizer does not overflow, and $y[n]$ will then be 0. Mathematically, we write

$$y[n] = \begin{cases} 0, & v[n] < 2^N \\ 1, & v[n] \geq 2^N. \end{cases} \quad (1)$$

The function of the digital accumulator is to distribute the power of the quantization error (noise) preferentially toward higher frequencies, thus noise shaping the spectrum.

The effect of the quantizer is usually modeled as an additive quantization noise source $e$. In the Z-domain, we can write the output $Y(z)$ in terms of $X(z)$ and $E(z)$ as follows:

$$Y(z) = X(z) + (1 - z^{-1})E(z). \quad (2)$$

where $X$, $Y$, and $E$ are the $z$ transforms of $x$, $y$, and $e$, respectively.

The output contains not only the input signal but also the quantization error shaped by a filter with transfer function $(1 - z^{-1})$. Ideally, the quantization noise is white and is shaped by the filter so that its power is pushed to the higher frequencies and moved away from the input signal. However, this is not the case for a first-order DDSM. The output signal of the first-order DDSM contains a strong periodic structure, regardless of the output cycle length [9]. A simulation result for a 20-bit first-order DDSM is shown in Fig. 2.

The quantization noise can be whitened and shaped more effectively by a higher order MASH structure. A MASH DDSM uses a cascade of lower order blocks to construct a high-order modulator; it typically comprises first-order modulators or a combination of first- and second-order modulators. The topology of the MASH DDSM is straightforward, and it is stable for all inputs [10]. The simulation result for a 20-bit third-order DDSM is shown in Fig. 3. Note that the power spectrum more closely matches the white-noise approximation in this case and has less tonal behavior. This is because the system has long cycles and the quantization error has been randomized sufficiently.

A. Conventional MASH

The block diagram of an $N$-bit accumulator of the type shown in Fig. 1 is shown schematically in Fig. 4, where the notation $(1, N, N, 1)$ represents a first order, $N$-bit input, $N$-bit quantization error output, and 1-bit carry output, respectively.

Since higher order DSMs are widely used in frequency synthesis applications, we consider, in this paper, the third-order MASH 111 DDSM shown in Fig. 5. This consists of three identical $N$-bit accumulators of the type shown in Fig. 4 and an error cancellation network. MASH 111 indicates that it comprises three first-order accumulators.

The output of the MASH 111 DDSM can be expressed in the Z-domain as

$$Y(z) = STF(z) \cdot X(z) + NTF(z) \cdot E_0(z) \quad (3)$$

Fig. 1. Digital accumulator model.

Fig. 2. Simulated power spectrum of a 20-bit first-order DDSM; the input is 104 857. Note the strong tonal behavior resulting from the inadequate whitening of the quantization noise. The smooth curve shows the ideal behavior of the 20-bit first-order DDSM, assuming that the quantization noise is white.

Fig. 3. Simulated power spectrum of a 20-bit third order DDSM; the input is 104 857. Note the strong tonal behavior resulting from the inadequate whitening of the quantization noise. The smooth curve shows the ideal behavior of the 20-bit third-order DDSM, assuming that the quantization noise is white.

Fig. 4. Block diagram of an $N$-bit accumulator.
where \( X(z) \), \( E_3(z) \), \( STF(z) \), and \( NTF(z) \) are the \( z \)-transforms of the input, the quantizer error of the third stage, and the signal and noise transfer functions of the modulator, respectively. In this example, \( STF(z) = 1 \), and the noise transfer function is given by

\[
NTF(z) = (1 - z^{-1})^3. \tag{4}
\]

Note that the error cancellation network completely removes the quantization errors of the first two stages.

B. RC MASH

In our RC MASH DDSM [7], only the first accumulator has a full-width \( N \)-bit word. By setting the least significant bit (LSB) of the input to “1”, this stage sets the cycle length of the modulator’s quantization error to \( 2^N \)[5].

The error signal of the first stage passes through an \( M \)-bit interstage quantizer \( Q_M \) before being fed forward to the next (\( L \)-bit) stage. The corresponding block diagram of the first accumulator incorporating an interstage quantizer is shown in Fig. 6.\(^2\) The other accumulators use fewer bits to perform the noise shaping. This allows us to reduce the word lengths in the following stages without reducing the cycle length.

The block diagram of our RC MASH 111 DDSM [7], [11] is shown in Fig. 7. The error cancellation network is as in Fig. 5.

\(^2\)The interstage quantization may be realized simply by discarding the \( (N - M) \) LSBs.

In this case, it does not remove the quantization errors completely, as we will show.

A linearized model which illustrates all the quantization error sources is shown in Fig. 8; its output can be expressed in the Z-domain as

\[
Y(z) = STF(z) \cdot X(z) + NTF(z) \cdot E_3(z) + z^{-1}(1 - z^{-1}) \cdot E_{22}(z) + (1 - z^{-1})^2 \cdot E_{23}(z) \tag{5}
\]

where \( STF(z) \) and \( NTF(z) \) are the signal and noise transfer functions, as before. \( E_3(z) \) is the \( z \)-transform of the error introduced by the 1-bit quantizer in the third stage. \( E_{22}(z) \) and \( E_{23}(z) \) are the \( z \)-transforms of the quantizer errors introduced by the \( M \)- and \( L \)-bit interstage quantizers between the first and second and second and third accumulators, respectively.

Note that (5) differs qualitatively from (3) in that it contains two additional shaped noise terms resulting from the errors introduced by the interstage quantizers. By choosing the values of \( M \) and \( L \) appropriately, these contributions can be masked spectrally by the shaped \( E_3 \) term. The guidelines for choosing \( M \) and \( L \) are presented in Section III.
III. DESIGN METHODOLOGY (DITHERLESS CASE)

A. Cycle Length and Tone Location of the DDSM

The guaranteed minimum cycle lengths for MASH DDSMs with identical first-order stages have been found empirically by extensive simulation [4] and proven theoretically [5]. For first-, second- and third-order DSMs, the results are $2^N$, $2^{N-1}$, and $2^{N+1}$, respectively, where $N$ is the word length of the accumulator in the DDSM and the initial condition is odd in the case of the second- and third-order DDSMs [4], [5].

The quantization noise power is spread over a number of tones that is determined by the cycle length, resulting in a tone spacing of $\Delta f = (f_s)/L_n$, where $f_s$ is the sampling frequency and $L_n$ is the cycle length. If $\Delta f$ is less than the resolution bandwidth of the measuring equipment, the resulting discrete spectrum is indistinguishable experimentally from a continuous spectrum [4]. However, when the cycle length of a DDSM output is not sufficiently large, one can observe discrete tones clearly in the power spectrum. The locations of these tones are given by

$$f[k] = k\Delta f, \quad k = 1, 2, \ldots, \frac{L_n}{2}$$

(6)

where $k$ is the index of the tone.

Fig. 9 shows the output power spectrum of a third-order 6-bit DDSM whose output cycle length $L_n$ is $2^7$; this is confirmed by the autocorrelation in Fig. 10, which is periodic with period 128. The discrete power spectrum $P[k]$ of the output $y$ of the DDSM shown in Fig. 9 is defined by

$$P[k] = |Y[k]|^2$$

(7)

where $Y[k]$ is the discrete-time Fourier series [12] of the output of the DDSM with its dc term removed.$^3$

$^3$In this work, we remove the dc component of the output for illustrative purposes as we are concerned primarily with the spectrum of the quantization noise contribution.

Note that the power spectrum of the shaped quantization noise $NTF(z)E_3(z)$ contains $2^7$ discrete tones, as predicted; these are located at $(kf_s)/(2^7)$, with $k = 1, 2, \ldots, 2^7/2$. In particular, the lowest frequency tone appears at $(f_s)/(2^7)$. Note that the $x$ axis is normalized to $f_s/2$ in Fig. 9.

Assuming a cycle of length $L_n$ and additive uniformly distributed white quantization noise, the idealized power spectrum of the shaped noise $NTF(z) \cdot E_3(z)$ is given by

$$S_3(f[k]) = \frac{1}{12L_s} |NTF(z)|^2 \delta_{k\equiv2^n/k_{12}} L_n , \quad k = 1, 2, \ldots, \frac{L_n}{2}$$

(8)

Throughout this paper, we will use the power spectrum $S_3$, which is obtained by assuming that the quantization noise $E_3$ is white, to estimate the power spectrum of the actual shaped quantization noise component $N_3$.

B. Additional Noise Contributions of the Interstage Quantizers

For notational convenience, let us rewrite (5) as follows:

$$Y(z) = STF(z)X(z) + N_3(z) + N_{12}(z) + N_{23}(z)$$

(9)
where \( N_3(z) = NTF(z) \cdot E_3(z) \) is the shaped contribution from the quantizer in the third accumulator, \( N_{12}(z) = z^{-1}(1 - z^{-1})E_{12}(z) \) is the shaped contribution of the first interstage quantizer error, and \( N_{23}(z) = (1 - z^{-1})^2E_{23}(z) \) is the shaped contribution of the second interstage quantizer error.

Assuming that all quantization noise terms can be modeled by independent white sources, we estimate the power spectrum of \( N_3(z) \) as

\[
S_3(f[k]) = \frac{1}{12L_s} \left\{ (1 - z^{-1})^2 \right\}_{\text{white}2\pi/k/L_s}^2
\]

where \( L_s \) is the cycle length.

In the same manner, the spectra obtained by assuming white error sources \( e_{12} \) and \( e_{23} \) are given by

\[
S_{12}(f[k]) = \frac{\Delta_{12}^2}{12L_{12}} \left\{ (1 - z^{-1})^2 \right\}_{\text{white}2\pi/k/L_{12}}^2
\]

\[
S_{23}(f[k]) = \frac{\Delta_{23}^2}{12L_{23}} \left\{ (1 - z^{-1})^2 \right\}_{\text{white}2\pi/k/L_{23}}^2
\]

where \( \Delta_{12} \) and \( \Delta_{23} \) are the quantization steps of the \( M \)- and \( L \)-bit interstage quantizers, which are \((1)/(2^M)\) and \((1)/(2^L)\), respectively. We denote by \( L_{12} \) and \( L_{23} \) the cycle lengths (periods) of the error signals from the interstage quantizers. We will show in the following how these lengths can be determined.

Let us express the dc input \( X \) to the DDSM in binary form, which is \( x_N, x_{N-1}, \ldots, x_1 \), and separate it into its upper and lower pieces as follows:

\[
\{ x_N, x_{N-1}, \ldots, x_1 \} = X_{\text{upper}} + X_{\text{lower}}
\]

\[
\{ x_N, x_{N-1}, \ldots, x_{N-M+1}, 0_{N-M}, \ldots, 0_1 \}
\]

\[
= \{ 0_N, 0_{N-1}, \ldots, 0_{N-M+1}, x_{N-M+1}, x_{N-M+2}, \ldots, x_1 \}.
\]

Since the \((N - M)\) LSBs of \( X_{\text{upper}} \) are 0, they do not contribute to \( N_{12} \). Therefore, \( X_{\text{lower}} \) alone determines \( N_{12} \). Since the \( M \) most significant bits are 0, the error output for \( X_{\text{upper}} \) feeding through the \( N \)-bit accumulator is the same as that feeding through an \((N - M)\)-bit accumulator. Consequently, the cycle length of \( N_{12} \) is the same as the output cycle length of an \((N - M)\)-bit word feeding through an \((N - M)\)-bit accumulator. If we set the LSB of the input to “1,” the cycle length \( L_{12} \) in this case is \( 2^{N-M} \). In the same manner, the cycle length \( L_{23} \) for \( N_{23} \) is \( 2^{N-L} \).

\[
L_3 = 2^N
\]

\[
L_{12} = 2^{N-M}
\]

\[
L_{23} = 2^{N-L}.
\]

The correlation function \( \gamma \), shown in the following equation, can be used to quantify the interdependencies of \( N_{12}, N_{23}, \) and \( N_3 \):

\[
\gamma = \frac{N_{12} \cdot \text{Corr}(x_N, x_{N-M}) \cdot \text{Corr}(x_{N-M}, x_{N-L})}{\sqrt{(N_{12} \cdot \text{Corr}(x_N, x_{N-M})^2), (N_{23} \cdot \text{Corr}(x_{N-M}, x_{N-L})^2)}}
\]

We have performed extensive simulations for different combinations of \( N, M, \) and \( L \), and the correlation results are below 0.02 in each case. Therefore, we conclude empirically that \( N_{12}, N_{23}, \) and \( N_3 \) can be made almost independent of each other.

By assuming independence, the noise power spectrum at the output of the RC MASH DDSM can be approximated by

\[
S(f[k]) = S_3(f[k]) + S_{12}(f[k]) + S_{23}(f[k])
\]

\[
= \frac{1}{12L_s} \left\{ (1 - z^{-1})^2 \right\}_{\text{white}2\pi/k/L_s}^2 + \frac{\Delta_{12}^2}{12L_{12}} \left\{ (1 - z^{-1})^2 \right\}_{\text{white}2\pi/k/L_{12}}^2 + \frac{\Delta_{23}^2}{12L_{23}} \left\{ (1 - z^{-1})^2 \right\}_{\text{white}2\pi/k/L_{23}}^2,
\]

\[
k = 1, 2, \ldots, L_s/2.
\]

C. Error Masking Strategy

The idea of our word-length selection strategy [11] is to mask the contributions of the intermediate quantizers by hiding the noise components \( N_{12} \) and \( N_{23} \) below the \( N_3 \) component.

The idea is shown graphically in Fig. 11. The spectral envelopes \( S_{12} \) and \( S_{23} \) due to the interstage quantizers should lie below the \( S_3 \) envelope. Since all are discrete spectra, the constraints apply at a finite number of points. In particular, we require that

\[
S_{12} < S_3 \cdot f = f_s \cdot k/L_{12}, \quad k = 1, 2, \ldots, L_{12}/2
\]

\[
S_{23} < S_3 \cdot f = f_s \cdot k/L_{23}, \quad k = 1, 2, \ldots, L_{23}/2.
\]

Recall that, for a DDSM with an output cycle length of \( L_s \), the lowest frequency tone is at \( f_s/L_s \). Therefore, since the cycle lengths for \( N_{12} \) and \( N_{23} \) are \( 2^{N-M} \) and \( 2^{N-L} \), the lowest frequency tones in the power spectra of \( N_{12} \) and \( N_{23} \) are at \( f_s/2^{N-M} \) and \( f_s/2^{N-L} \), respectively.

Additionally, at the output of the RC DDSM, since \( S_{12} \) and \( S_{23} \) are first- and second-order shaped, respectively, while \( S_3 \) is third-order shaped, if the levels of the lowest frequency tones in \( N_{12} \) and \( N_{23} \) are below that of \( N_3 \), the overall power of \( N_{12} \) and \( N_{23} \) should always be below the \( S_3 \) envelope. Based on this idea, the constraints can be rewritten as

\[
S_{12} < S_3 \cdot f_s = f_s/2^{N-M}
\]

\[
S_{23} < S_3 \cdot f_s = f_s/2^{N-L}.
\]

Since

\[
|1 - z^{-1}|^2 = |1 - e^{-\pi f/s}|^2
\]

\[
\geq 2 \sin^2(\pi f/s)^2
\]

\[
\sin(\pi f/s) \approx \pi f/s \quad \text{for } f \ll f_s
\]

we can approximate \( S_{12}, S_{23}, \) and \( S_3 \) at low frequencies by

\[
S_{12} \approx \frac{\Delta_{12}^2}{12L_{12}} \cdot 2^M(\pi f/s)^2
\]

\[
S_{23} \approx \frac{\Delta_{23}^2}{12L_{23}} \cdot 2^L(\pi f/s)^4
\]

\[
S_3 \approx \frac{1}{12L_3} \cdot 2^6(\pi f/s)^6
\]

Substituting (23), (24), and (25) into the constraints (19) and (20), we obtain

\[
\frac{1}{2^M} \cdot \frac{1}{12} \cdot 2^{N-M} \cdot 2^2 \cdot \frac{\pi^2}{(2^N)^2} \leq \frac{1}{12} \cdot 2^N \cdot \left( \frac{2}{2^N} \right)^6
\]
which reduce to

\[ 4N - 5M - 4 < 4 \log_2(\pi) \approx 6.6 \]  
\[ 2N - 3L - 2 < 2 \log_2(\pi) \approx 3.3. \] (29)

Based on (28) and (29), in order to design an RC \( N-M-L \) MASH DDSM with the same cycle length and similar power spectrum as a conventional \( N_0 \)-bit MASH DDSM, the design procedure is as follows.

1) Choose \( N = N_0 + 1 \) to ensure that the output cycle length of the RC MASH DDSM is the same as that of the conventional \( N_0 \)-bit MASH DDSM.

2) Choose \( M = \text{ceil}(\frac{4N - 10.6}{5}) \) [from (28)] to ensure that the power of the first tone of \( N_{12} \) is less than \( S_3 \) at the frequency \( f_s/2^{N-M} \), where \( \text{ceil}(x) \) means the smallest integer greater than \( x \).

3) Choose \( L = \text{ceil}(\frac{2N - 5.3}{3}) \) [from (29)] to ensure that the power of the first tone of \( N_{23} \) is less than \( S_3 \) at the frequency \( f_s/2^{N-L} \).

D. Hardware Requirements

Since the accumulators consume most of the hardware in the DDSM and the HC of the accumulators is proportional to their word lengths, we can estimate the relative HC (RHC) of our RC MASH DDSM compared with the conventional MASH DDSM as

\[ \text{RHC} \approx N_0 + \text{ceil} \left( \frac{4N_0 - 6.6}{5} \right) + \text{ceil} \left( \frac{2N_0 - 3.3}{3} \right) 3N_0 \]

\[ \approx \frac{2.47N_0 - 1.42}{3N_0} \times 100\% \] (30)

where the word length of the reference MASH DDSM is \( N_0 \), and we choose \( N, M, \) and \( L \) as in Section III.C. Asymptotically, RHC approaches 82% for large \( N_0 \)’s. When \( N_0 = 19 \), (30) predicts that our RC implementation will require 20% less hardware than a conventional implementation with identical accumulators.

IV. DESIGN EXAMPLE

In order to verify the design methodology in Section III.C, we present a design example for a 19-bit MASH DDSM. The optimum word lengths of the first, second, and third stages of the RC MASH DDSM are 20, 14, and 12, respectively.

First, we simulate the 20–14–12 RC MASH DDSM to show typical contributions \( N_{12}, N_{23}, \) and \( N_3 \). In Fig. 12, the autocorrelation result confirms that the cycle length of \( N_{12} \) is \( 2^{20} \). Fig. 13 shows the power spectrum of \( N_{12} \). The power spectrum \( S_{12} \) based on the white-noise approximation (11) is overlaid as well. As expected, the quantization powers are spread over \( 2^{20-14} \approx 2^6 \) discrete tones, while the location and power of the lowest frequency tone are \( f_s/2^6 \) and approximately -146 dB, respectively. In addition, \( N_{12} \) is shaped by 20 dB/dec, which is the same as for a first-order DDSM.

In Fig. 14, the autocorrelation calculation confirms that the cycle length of \( N_{23} \) is \( 2^{12}(= 256) \). Fig. 15 shows the simulated
output power spectrum \( N_{23} \) with the overlaid white-noise prediction \( S_{23}(12) \), from which we can see that \( N_{23} \) is shaped by 40 dB/dec, as expected. The lowest frequency tone is located at \( f_s/2^{30-12} = f_s/2^8 \), at approximately \(-178 \) dB.

In Fig. 16, the autocorrelation result for \( N_3 \) confirms that the cycle length is \( 2^{20} \) (\( \approx 1048576 \)). Fig. 17 shows the simulated power spectrum for \( N_3 \) and the white-noise estimate \( S_3 \).

A. Simulations

To compare the conventional and RC modulators, we present simulation results. The inputs of the DDSM are selected as the odd numbers that set the normalized input as close as possible to the value 0.1, i.e., \( X = 104857 \) in this case. The simulated output power spectrum of the conventional 19-bit MASH DDSM is shown in Fig. 18. Its cycle length of \( 2^{20} \) is confirmed by Fig. 19.

The output power spectrum for the 20–14–12 RC MASH DDSM is shown in Fig. 20. Note that the \( N_{12} \) and \( N_{23} \) components lie below the spectral envelope of \( N_3 \) and are therefore masked by it, as expected. Consequently, \( N_{12} \) and \( N_{23} \) do not adversely affect the overall performance of the DDSM. On the contrary, the additional quantization error sources serve to whiten the error, resulting in a smoother spectrum overall.

The cycle length of \( 2^{20} \) is confirmed by Fig. 21.

B. Experimental Results

We constructed an experimental demonstration system on a Xilinx Spartan-2E field-programmable-gate-array board clocked at \( f_s = 1.67 \) MHz. The modulator output was converted to continuous time using an Analog Devices AD5445 12-bit DAC with a zeroth-order hold and a low-pass filter with a bandwidth of 10 MHz. Spectral measurements were made using an Agilent E4402B Spectrum Analyzer.

Experimental measurements of the power spectrum of the conventional 19-bit MASH DDSM are shown in Fig. 22. Note that the power spectrum of the conventional 19-bit MASH DDSM is relatively spiky compared to that in the RC modulators.
case, due to the poorer whitening of the quantization noise, as shown in Fig. 19.

Experimental measurements of the power spectrum of the 20–14–12 MASH modulator are shown in Fig. 23. As expected, the noise is shaped at 60 dB/dec. Moreover, the spectrum of the new structure is smoother, as expected, due to the more effective whitening of the quantization noise spectrum, as shown in Fig. 21.

The spectrum of the new structure is smoother and closer to the ideal, even with the same cycle length as the conventional DDSM, due to the more effective whitening of the quantization noise spectrum.

C. HC

The hardware requirements for 1) a conventional 19-bit MASH 111 DDSM and 2) the 20–14–12-bit RC DDSM without dither are summarized in Table I. The HC is reported as the number of flip-flops and the number of four-input lookup tables which represent the synchronous and the asynchronous logic, respectively. The total-equivalent-gate (TEG) count for the design is given as well. These results are based on the map report from the Xilinx ISE program [13]; a full custom implementation could potentially do better.

The 20–14–12 RC MASH DDSM has a marginally better spectral performance than the 19-bit conventional MASH DDSM, with 20% less hardware (TEG); this agrees with our prediction (30).

V. DESIGN METHODOLOGY (WITH DITHER)

A. Additional Noise Contributions of the Interstage Quantizers

In the case of additive input dithering of a MASH system [6], a 1-bit dither pseudorandom signal \( d \) filtered by a shaping filter \( V(z) \) is added to the LSBs of a desired signal \( x \) as shown in Fig. 24.

With dithering, the minimum cycle length of the DDSM is guaranteed to be at least as large as that of the dither generator. This can be significantly larger than the cycle length in a ditherless DDSM. Consequently, the tone spacing is typically
expressed in units at and are, Thus implies that and at low frequencies by , and . Therefore, we apply the following are first- and second-order shaped, respectively, so long that it is hard to find the locations of their constraint at the boundary. In particular, the constraints can be written as

\[
L_{12}(f) = \frac{\Delta_2^2}{12} \left(1 - z^{-1}\right)^2 \left(z^{-1} - z^{-1}\right)^2 \quad (34)
\]

\[
L_{23}(f) = \frac{\Delta_3^2}{12} \left(1 - z^{-1}\right)^2 \left(z^{-1} - z^{-1}\right)^2 \quad (35)
\]

By once again assuming independence, the PSD of the error signal at the output of the dithered RC MASH DDSM can be expressed as

\[
L(f) = L_0(f) + L_{12}(f) + L_{23}(f) + L_{nf}(f) \quad (36)
\]

where \(L_{nf}(f)\) is the contribution due to the dither signal, and we have assumed that \(STF(z) = 1\).

### B. Zeroth-Order Dither

Because of dithering, the cycle lengths of \(e_{12}\) and \(e_{23}\) are so long that it is hard to find the locations of their first tones. Therefore, (19) and (20) cannot be used as constraints to select the DDSM word lengths. Nevertheless, we can still mask the \(N_{12}\) and \(N_{23}\) components below \(N_3\).

It can be shown that, for a DDSM with dithering, the low-frequency noise floor is typically dominated by the dither signal. In the case of a zeroth-order shaped dither, the level of the noise floor is

\[
L_{nf0} = \frac{1}{12 \cdot (2^N)^2}. \quad (37)
\]

In this case, we need to hide the components \(N_{12}\) and \(N_{23}\) below the contributions of \(N_3\) and the noise floor \(L_{nf}\). The largest frequency at which the PSD of the dithering is larger than the contribution from \(e_3\) can be calculated as

\[
\frac{1}{12} \left(2 \sin(\pi f_0/f_s)\right)^6 = \frac{1}{12 \cdot 2^N}. \quad (38)
\]

Assuming

\[
\sin(\pi f_0/f_s) \approx \pi f_0/f_s \quad \text{for } f_0 \ll f_s
\]

as before results in

\[
f_0 = \frac{1}{\pi \cdot 2^{N/3}} \cdot \frac{f_s}{2} \quad (40)
\]

for a sufficiently large \(N\). Therefore, we apply the following constraints: \(L_{12} < L_{nf}\) and \(L_{23} < L_{nf}\) for \(f < f_0\), and \(L_{12} < L_3\) and \(L_{23} < L_3\) for \(f > f_0\).

As \(L_{12}\) and \(L_{23}\) are first- and second-order shaped, respectively, \(L_{12} < L_3\) and \(L_{23} < L_3\) at \(f_0\) implies that \(L_{12} < L_3\) and \(L_{23} < L_3\) for \(f > f_0\). Therefore, we need only to check the constraint at the boundary. In particular, the constraints can be written as

\[
L_{12} < L_3 @ f_0 \quad (41)
\]

\[
L_{23} < L_3 @ f_0 \quad (42)
\]

as shown in Fig. 25.

We approximate \(L_{12}\), \(L_{23}\), and \(L_3\) at low frequencies by

\[
L_{12} \approx \frac{\Delta_2^2}{12} \cdot 2^2(\pi f/f_s)^2 \quad (43)
\]

\[
L_{23} \approx \frac{\Delta_3^2}{12} \cdot 2^4(\pi f/f_s)^4 \quad (44)
\]
\[ L_3 \approx \frac{1}{12} \cdot 2^6 (\pi f/f_s)^6, \]  

(45)

Substituting (43), (44), and (45) into the constraints (41) and (42), we obtain

\[ \frac{1}{2^{2M}} \cdot \frac{1}{12} \cdot \left( \frac{1}{2N/3} \right)^2 < \frac{1}{12} \cdot \left( \frac{1}{2N/3} \right)^6 \]  

(46)

\[ \frac{1}{2^{2L}} \cdot \frac{1}{12} \cdot \left( \frac{1}{2N/3} \right)^4 < \frac{1}{12} \cdot \left( \frac{1}{2N/3} \right)^6 \]  

(47)

which reduce to

\[ M > \frac{2N}{3}, \]  

(48)

\[ L > \frac{N}{3}. \]  

(49)

Based on (48) and (49), if the word length \( N \) of the first stage of the DDSM is determined, the optimum word lengths \( M \) and \( L \) of the second and third stages can be calculated as

\[ M = \text{ceil} \left( \frac{2N}{3} \right) \]  

(50)

\[ L = \text{ceil} \left( \frac{N}{3} \right). \]  

(51)

C. First-Order Dither

If a first-order shaped dither is applied to the input of the DDSM, its noise floor is defined by

\[ L_{n,f1} = \frac{1}{12} \cdot \left( \frac{1}{2N/2} \right)^2 \| (2 \sin(\pi f/f_s)) \|^2. \]  

(52)

The largest frequency at which the PSD of the dither component is larger than that from \( \epsilon_3 \) can be calculated as

\[ \frac{1}{12} \| (2 \sin(\pi f_1/f_s)) \|^4 = \frac{1}{12} \cdot 2^{2N} \]  

(53)

which results in

\[ f_1 \approx \frac{1}{\pi} \cdot \frac{1}{2N/2} \cdot \frac{f_s}{2}. \]  

(54)

Since \( L_{12} \) is first-order shaped, just like the dither, we require that \( L_{12} < L_{n,f1} \), which can be expressed as

\[ \frac{\Delta_2^2}{12} \cdot 2^2 (\pi f/f_s)^2 \leq \frac{1}{12} \cdot \left( \frac{1}{2N/2} \right)^6 \cdot 2^2 (\pi f/f_s)^2 \]  

(55)

which reduces to

\[ M \geq N. \]  

(55)

Therefore, \( M \geq N \). Since our objective is to reduce the overall hardware requirement, we choose \( M = N \). Next, \( L_{23} \) needs to be masked by \( L_3 \), as shown schematically in Fig. 26.

Thus, the word-length selection strategy for the third accumulator requires that

\[ L_{23} < L_{3 \oplus f_1}. \]  

(57)

This can be expanded as

\[ \frac{1}{2^{2L}} \cdot \frac{1}{12} \cdot \left( \frac{1}{2N/2} \right)^4 < \frac{1}{12} \cdot \left( \frac{1}{2N/2} \right)^6 \]  

(58)

which gives

\[ L > \frac{N}{2}. \]  

(59)

If we want to ensure that \( L_{23} \) is further below \( L_3 \), we can impose a guard band of 3 dB, for example. In this way, we force \( L_{12} \) to be half of \( L_3 \) at \( f_1 \), and the constraint becomes

\[ L > \frac{N}{2}. \]  

(60)
D. Hardware Requirements

The RHC of our \textit{RC} MASH DDSM designed with the zero-order dither technique compared with the conventional DDSM is

\[ RHC_0 \approx \frac{N + \text{cei}(0.67N) + \text{cei}(0.33N)}{3N} \times 100\%, \quad (61) \]

\( RHC_0 \) approaches 67% for large \( N \)'s. However, due to the fact that dithering consumes some additional hardware, the percentage hardware saving of the DDSM plus dither generator is less.

In the same manner, the \( RHC \) of our \textit{RC} MASH DDSM designed with first-order dither and a 3-dB guard band compared with the conventional DDSM is

\[ RHC_1 \approx \frac{N + \text{cei}(0.5N + 0.5)}{3N} \times 100\%. \quad (62) \]

Asymptotically, \( RHC_1 \) approaches 83% for large \( N \)'s. For the 14-bit case, (62) predicts that our \textit{RC} implementation will require 15% less hardware.

VI. DESIGN EXAMPLE (WITH DITHER)

A design example for a zeroth-order dithered 20-bit MASH DDSM is discussed in this section. Applying design equations (50) and (51), the appropriate word lengths of the second and third stages of the \textit{RC} DDSM are 14 and 7, respectively. A 20–14–7 \textit{RC} DDSM is simulated to show typical contributions \( N_{12}, N_{23}, \) and \( N_3 \) (see Figs. 27–29). The dither cycle length is \( 2^{24} \).

A. Simulations

The simulated PSD for a conventional zeroth-order dithered 20-bit MASH DDSM is shown in Fig. 30. The PSD of the \textit{RC} 20–14–7-bit equivalent is shown in Fig. 31. Note that the \( N_{12} \) and \( N_{23} \) components lie below the
Fig. 31. Simulated PSD at the output of a zeroth-order dithered RC 20–14–7-bit MASH 111 DDSM; the input is 104,857 (Compare with Fig. 30).

Fig. 32. Simulated PSD at the output of a conventional first-order dithered 14-bit MASH 111 DDSM; the input is 1639. The dc term has been removed. The solid curves are $L_3$ and $L_\ldots f_1$.

The simulated PSD for a conventional 14-bit MASH 111 DDSM with first-order dither is shown in Fig. 32. Applying the design (60), the word length of the third stage of the RC DDSM is eight. The simulated PSD for the RC 14–14–8 MASH 111 DDSM is shown in Fig. 33. As expected, the RC DDSM achieves an almost identical PSD compared to the conventional 14-bit DDSM.

**B. RHC**

The hardware requirements for: 1) a conventional 20-bit MASH 111 DDSM with zeroth-order dither; 2) an RC 20–14–7 DDSM with zeroth-order dither; 3) a conventional 14-bit MASH 111 DDSM with first-order dither; and 4) an RC 14–14–8 MASH DDSM with first-order dither are summarized in Table II.

<table>
<thead>
<tr>
<th>MASH DDSM with dither</th>
<th>Hardware Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) 20 bit with zeroth-order dither</td>
<td>139</td>
</tr>
<tr>
<td>(b) 20-14-7 bit with zeroth-order dither</td>
<td>101</td>
</tr>
<tr>
<td>(c) 14 bit with first-order dither</td>
<td>109</td>
</tr>
<tr>
<td>(d) 14-14-8 bit with first-order dither</td>
<td>97</td>
</tr>
</tbody>
</table>

The 20–14–7 RC MASH DDSM with zeroth-order dither achieves an almost identical PSD to the 20-bit conventional DDSM with dithering, but with 29% less hardware. If we subtract the HC for the dither block for both MASH DDSMs, which is 266 TEG, our RC MASH DDSM has an RHC of 67%, as predicted by (61). For the first-order dither case, our 14–14–7 DDSM consumes 89% hardware compared with the conventional 14-bit RC DDSM. In the same manner, if we exclude the consumption of the dither block, the RHC for our RC DDSM is 86% of the conventional DDSM, as predicted by (62).

**VII. CONCLUSION**

In this paper, we have presented a design methodology for MASH DDSMs based on error masking. We have shown that, starting with a conventional DDSM, it is possible to find an optimized word length for each stage of the DDSM, which allows a reduction in the HC by up to 20%, without degrading the spectral performance. Our simulation and experimental results confirm our analytical predictions. In the second part of this paper, we will extend our methodology to SQ DDSMs [14].

**REFERENCES**


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