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Paper Title: Post-Breakdown Conduction in Metal Gate/MgO/InP Structures

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# ABSTRACT:

The electrical behavior of broken down thin films of magnesium oxide (MgO) grown on indium phosphide (InP) substrates was investigated. To our knowledge, this is the first report that identifies the soft breakdown (SBD) conduction mode in a metal gate/high- $\kappa$ /III-V semiconductor structure. It is shown that the leakage current associated with this failure mode follows the power-law model I= $aV^b$  for both injection polarities in a voltage range that largely exceeds the one reported for SiO<sub>2</sub>. We also show that the hard breakdown (HBD) current is remarkably high, involving significant thermal effects that are believed to be at the origin of the switching behavior exhibited by the I-V characteristics.

CATEGORIES: Novel Gate Stack/Dielectrics and FEOL Reliability and Failure Mechanisms

Novel Device Reliability and Failure Mechanisms

# Post-Breakdown Conduction in Metal Gate/MgO/InP Structures

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Abstract-The electrical behavior of broken down thin films of magnesium oxide (MgO) grown on indium phosphide (InP) substrates was investigated. To our knowledge, this is the first report that identifies the soft breakdown (SBD) conduction mode in a metal gate/high- $\kappa$ /III-V semiconductor structure. It is shown that the leakage current associated with this failure mode follows the power-law model I= $aV^b$  for both injection polarities in a voltage range that largely exceeds the one reported for SiO<sub>2</sub>. We also show that the hard breakdown (HBD) current is remarkably high, involving significant thermal effects that are believed to be at the origin of the switching behavior exhibited by the I-V characteristics.

### I. INTRODUCTION

Even though every gate dielectric stack degrades and eventually breaks down when subjected to a sufficiently high or prolonged electrical stress, the magnitude and particular features of the leakage current vary from system to system. In order to identify the post-breakdown (BD) conduction modes as well as their dynamical aspects, a vast terminology (digital/analog SBD, linear/nonlinear HBD, progressive BD) has been introduced [1] but these terms are rather vague with respect to the magnitude of the current or the voltage range in which they become observable. Additionally, it has been demonstrated that the detection criterion of an oxide BD event in terms of the leakage current excess has a profound impact on the reliability assessment of MOS devices [2]. That is the reason why studies about the post-BD conduction modes in emerging MOS technologies such as those based on metal gate/high-κ/III-V semiconductors are strongly required. In this work, we have focused the attention on the electrical behavior of broken down NiSi gate/MgO/InP stacks. We have chosen this system, first, because MgO is considered a good alternative to replace SiO<sub>2</sub> as gate dielectric both for low [3] and high power applications [4]. MgO has a large band gap (from 7.3 [3]- 7.8eV [5]), what ensures sufficiently large band offsets with the semiconductor substrate, medium to high dielectric permittivity  $\kappa$  (from 6.7 [6] to 10 [5]) depending on the growth process and annealing conditions, high thermal conductivity [4] suitable for applications involving large power dissipation, high breakdown field (12 MV/cm) compared to SiO<sub>2</sub> [4] and notably, MgO is a chemically inert material, which has the benefit of minimising the formation of interfacial layers when in contact with semiconductor substrates [3]. Second, InP is a compound semiconductor that has been successfully integrated into high-speed MOSFETs [7], mainly for its high electron mobility and thermal conductivity [8]. In addition, InP seems to be a more forgiving material with respect to the Fermi-level pinning problem [9]. It has also been reported that the interface of MgO films grown on p-type InP is very smooth at the atomic scale with no evidence of interfacial reaction [10]. The potential of thin MgO films as alternative gate dielectrics has been examined not only in combination with Si [3,6] but also with a number of other semiconductor substrates such as GaN [11] and GaAs [12].

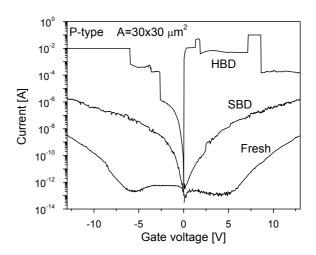


Fig. 1. Typical I-V characteristics measured after the dielectric breakdown of the MgO layer. SBD and HBD correspond to soft and hard breakdown modes, respectively.

# II. SAMPLE PREPARATION

MgO films of nominal thickness 20 nm were deposited by electron beam evaporation from 99.9% MgO pellets at a rate of 0.2Å/s, at 180 °C on n- and p-type InP substrates (S doped

concentration  $3 \times 10^{18}$  cm<sup>-3</sup> and Zn doped concentration  $3\text{-}5 \times 10^{18}$  cm<sup>-3</sup>, respectively). The samples were capped *in-situ* with 100 nm of amorphous silicon ( $\alpha$ -Si) using a second e-beam source. For the NiSi gate process, nickel was deposited by e-beam evaporation ( $\sim$ 80 nm) through a patterned resist mask followed by a lift-off process. The RTA is a one step process at 500 °C for 30 s in N<sub>2</sub>. The areas of the devices tested are  $9.0 \times 10^{-6}$ ,  $1.6 \times 10^{-5}$ , and  $4.9 \times 10^{-5}$  cm<sup>2</sup>. The permittivity of the MgO film from capacitance-voltage analysis is 8.1.

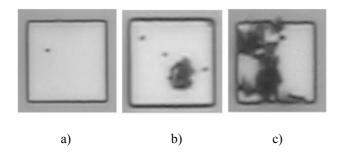


Fig. 2. Effects of the dielectric BD on the gate electrode (different samples). a) single SBD spot, b) multiple SBD spots and HBD, c) HBD with thermal destruction.

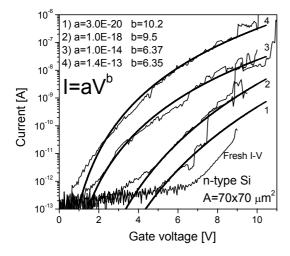


Fig. 3. Experimental (thin lines) and model (thick lines) SBD I-V characteristics

# III. EXPERIMENTAL RESULTS AND ANALYSIS

Figure 1 shows typical I-V characteristics measured before and after the dielectric BD of the MgO layer. The curves were obtained by ramped voltage stresses in a p-type InP sample. Similar results are obtained for the n-type samples. Notice that the SBD curves extend up to  $\pm 13$ V, nearly a factor X3 the maximum voltage range reported for the observation of SBD in SiO<sub>2</sub> [1]. If the same sample is further stressed, the leakage current increases reaching soon the compliance limit of the

measurement setup. If this limit is increased further, the HBD I-V characteristic frequently exhibits a switching behavior (see for instance the positive bias region in Fig. 1). In connection with this modification of the leakage current, the photographs in Fig. 2 show three cases of particular interest: Fig. 2.a corresponds to the appearance of a single leakage spot while Fig. 2.b corresponds to multiple SBD spots and one HBD event. Finally, Fig. 2.c reveals the lateral propagation of the HBD failure mode across the FUSI gate. The switchings in the I-V characteristic are only observable after this extensive damage. We surmise that they might be related to the variation of the contact resistance between the measurement probe and the gate electrode caused by the important thermal effects that take place during the voltage sweep. However, it is worth pointing out that this kind of resistive switching can also be linked to atomic rearrangements within the BD path since similar behavior has been reported for a wide variety of metal oxides [13] as well as for SiO<sub>2</sub> [14]. Notice also that the HBD current is very high, what can be mainly attributed to the high doping level of the InP substrates used in this study.

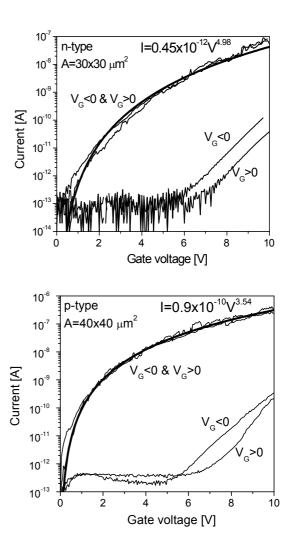


Fig. 4. Experimental (thin lines) and model (thick line) SBD I-V characteristics

Figure 3 shows the evolution of the SBD current in a single sample using progressive voltage stress (end voltage is increased after each sweep). The curves correspond to an increasing number of SBD spots. Notice also that the power *b* decreases with the current magnitude as previously reported for SiO<sub>2</sub> [15]. As shown in Fig. 4, contrary to what happens to the fresh I-V characteristics, the SBD current in MgO is symmetrical with respect to the sign of the applied voltage both for the n- and p-type samples. This is consistent with the idea that the oxide barrier plays no role after SBD and that as long as there is sufficient charge available for conduction, the particular features of the injecting electrode are irrelevant in the description of the phenomenon [1].

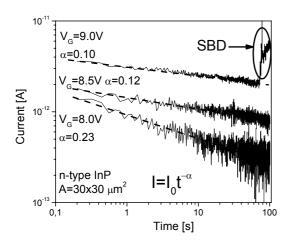


Fig. 5. Experimental (solid lines) and fitting results (dashed lines) using a power-law dependence

We have also explored the degradation mechanism that leads to the post-BD state using constant electrical stress. Fig. 5 shows the effects of applying a constant voltage to the gate on the leakage current. Notice that the current decreases following a power-law model  $I(t)=I_0t^{-\alpha}$ , with  $I_0$  and  $\alpha$  constants and t the stress time. This particular dependence has been observed in different gate dielectrics and has been attributed to negative charge trapping. As shown in Fig. 5, in our samples,  $\alpha$  decreases with the stress voltage. This is at variance with what has been reported for HfO<sub>2</sub> [16] but consistent with the experimental data for thick SiO<sub>2</sub> [17] and thin HfAlO [18] films with poly-Si and TiN gate, respectively. The reason for this different trend is unknown for the moment. Even though the leakage current in our samples exhibits a noisy behavior during degradation, the seeming increase of the current fluctuations is only an artifact due to the use of a log-log scale. In fact, the analysis of the fluctuations reveals that the occurrence of the SBD event is not preceded by any anomalous behavior of the trapping characteristics (see the upper curve in Fig. 6).

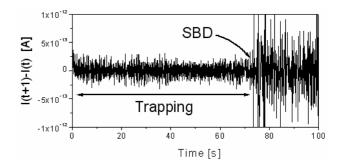


Fig. 6. Fluctuating behavior of the leakage current before and after the SBD event calculated from the upper curve shown in Fig. 5.

## IV. CONCLUSIONS

post-breakdown conduction modes gate/MgO/InP structures were investigated. The soft-BD I-V characteristics in MgO exhibit virtually all the same features that were reported in the past for SiO<sub>2</sub> with the only exception being the voltage range in which this failure mode becomes observable. Once again, this seems to stress the fact that this mode is associated with a conduction mechanism governed by the laws of confined electron transport in which the relevance of the material and the injecting electrode properties are not essential. This is confirmed by the symmetry of the conduction characteristics with the applied voltage. However, a big difference has been observed in the case of HBD. The hard-BD spots in MgO are much more conductive than those in SiO<sub>2</sub>. We believe that this is caused by the high doping level of the InP substrates considered in this study. Additionally, the large leakage current after HBD can be attributed to a larger extension of the damaged area. The connection between the thermal effects occurring during stress and the switching behavior of the I-V is also an issue that requires further investigation. Finally, the charge trapping dynamics was explored and it was found to follow the same trend reported before for other high-κ dielectrics.

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### REFERENCES

- [1] E. Miranda and J. Suñé, "Electron transport through broken down ultra-thin SiO<sub>2</sub> layers in MOS devices," *Mic. Rel.*, vol. 44, 2004, 1.
- [2] J. Suñé, E. Wu, and S. Tous, "A physics-based deconstruction of the percolation model of oxide breakdown," *Mic. Eng.*, vol. 84, 2007, 1917.
- [3] L. Yan, C. Lopez, R. Shrestha, E. Irene, A. Suvorova, and M. Saunders, "Magnesium oxide as a candidate high-κ gate dielectric," *Appl. Phys. Lett.*, vol. 88, 2006, 142901.
- [4] A. Posadas, F. Walker, C. Ahn, T. Goodrich, Z. Cai, and K. Ziemer, "Epitaxial MgO as an alternative gate dielectric for SiC transistor applications," *Appl. Phys. Lett.*, vol. 92, 2008, 233511.
- [5] In *II-VI and I-VII Compounds; Semimagnetic Compounds*, Landolt-Börnstein, New Series, Group III, Vol. 41B, edited by O. Madelung *et al.*, Springer, Heidelberg, 1999.
- [6] B. Brennan, S. Mc Donnell, and G. Hughes, "Photoemission studies of the interface formation of ultrathin MgO dielectric layers on the oxidized Si(111) surface," *J. of Phys.: Conf. Ser.*, vol. 100, 2008, 042047.
- [7] H. Zhao, D. Shahrjerdi, F. Zhu, M. Zhang, H. Kim, I. Ok, J. Yum, S. Park, S. Banerjee, and J. Lee, "Gate-first inversion-type InP metal-oxide-semiconductor field-effect transistors with atomic-layer-deposited Al<sub>2</sub>O<sub>3</sub> gate dielectric," *Appl. Phys. Lett.*, vol. 92, 2008, 233508.
- [8] R. Sumathi, N. Dharmarasu, S. Arulkumaran, P. Jayavel, and J. Kumar, "Improved electrical properties on the anodic oxide/InP interface for MOS structures," *J. Elect. Mat.*, vol. 27, 1998, 1358.
- [9] Y. Wu, Y. Xuan, T. Shen, P. Ye, Z. Cheng, and A. Lochtefeld, "Enhancement-mode InP n-channel metal-oxide-semiconductor field-effect transistors with atomic-layer-deposited Al<sub>2</sub>O<sub>3</sub> dielectrics," *Appl. Phys. Lett.*, vol. 91, 2007, 022108.
- [10] T. Kim and Y. You, "Microstructural and electrical properties of MgOthin films grown on p-InP (100) substrates at low temperatures," *Appl. Surf. Sci.*, vol. 180, 2001, 162.
- [11] H. Cho, K. Lee, B. Gila, C. Abernathy, S. Pearton, and F. Ren, "Effects of oxide thickness and gate length on DC performance of submicrometer MgO/GaN MOSFETs," *Elect. Sol. St. Lett.*, vol. 6, 2003, G119.
- [12] S. Chromik, M. Spankova, I. Vavra, J. Liday, P. Vogrincic, and P. Lobotka, "Preparation and structural properties of MgO films grown on GaAs substrate," *Appl. Sur. Sci.*, vol. 254, 2008, 3635.
- [13] A. Sawa, "Resistive switching in transition metal oxides," *Materials Today*, vol. 11, 2008, 28.
- [14] E. Miranda, J. Suñé, R. Rodríguez, M. Nafría, and X. Aymerich, "Breakdown and anti-breakdown events in high-field stressed ultrathin gate oxides," *Sol. St. Elect.*, vol. 45, 2001, 1327.
- [15] E. Miranda, J. Suñé, R. Rodríguez, M. Nafría, and X. Aymerich, "A function-fit model for the soft breakdown

- failure mode," IEEE Electron Dev. Lett., vol. 20, 1999, 265.
- [16] S. Zafar, A. Callegari, E. Gusev, and M. Fischetti, "Charge trapping related threshold voltage instabilities in high permittivity gate dielectric stacks", *J. Appl. Phys.*, vol. 93, 2003, 2998.
- [17] E. Runnion, S. Gladstone, R. Scott, D. Dumin, L. Lie, and J. Mitros, "Thickness dependence of stress-induced leakage currents in silicon oxide," *IEEE Trans. Elec. Dev.*, vol. 44, 1997, 993.
- [18] W. Loh, B. Cho, M. Joo, M. Li, D. Chan, S. Mathew, and D. Kwong, "Charge trapping and breakdown mechanism in HfAlO/TaN gate stack analyzed using carrier separation," *IEEE Trans. Dev. Mat. Rel.*, vol. 4, 2004, 696.