Reduced Complexity MASH Delta–Sigma Modulator

Zhipeng Ye, *Student Member, IEEE*, and Michael Peter Kennedy, *Fellow, IEEE*

***Abstract*—A reduced complexity digital multi-stage noise shaping (MASH) delta–sigma modulator for fractional-*N* frequency synthesizer applications is proposed. A long word is used for the first modulator in a MASH structure; the sequence length is maximized by setting the least significant bit of the input to "1;" shorter words are used in subsequent stages. Experimental results confirm simulations.**

***Index Terms*—Complexity, delta–sigma modulator, multi-stage noise shaping (MASH), noise shaping, sequence length.**

I. Introduction

FREQUENCY synthesizers based on phase-locked loops (PLLs) are widely used in wireless communication systems. A number of methods are known to realize the fractional-*N* division function that are based upon the concept of integer-*N* frequency synthesis [1]–[3]; these include pulse swallowing, phase interpolation, Wheatly random jittering and delta–sigma modulation to control the multi-modulus frequency dividers. A delta–sigma modulator (DSM) realization of a fractional-*N* frequency synthesizer can achieve low phase noise, fast settling time, fine channel resolution, and wide tuning bandwidth [2].

Careful modulator design is very important, because all modulator spectrum imperfections will directly affect the purity of the synthesizer spectrum. One of the most challenging issues is the tonal behavior of the delta–sigma modulator [4]. Often cited causes of the tonal behavior in a DSM are the cycles that are especially likely to occur with slowly-varying or dc inputs. In other words, the randomization of the inputs by the DSM is often insufficient and the quantization error forms short and repeating patterns. This gives rise to strong unwanted tones in the output spectrum [4].

First-order DSMs are seldom used in frequency synthesis applications due to the fact that the output sequence contains periodic structure, regardless of the choice of the initial condition, [5]. On the other hand, higher order modulators can benefit from more randomization of the quantizer error [5]. High-order delta–sigma modulators can be realized with interpolative and MASH architectures [2], [6]. The MASH structure uses a cascade of lower order blocks to construct a high-order modulator; it typically comprises a cascade of first-order modulators or a combination of first- and second-order modulators and can produce long cycles.

Manuscript received November 2, 2006; revised January 15, 2007. This work is supported in part by Science Foundation Ireland under Grant 02/IN.1/I45. This paper was recommended by Associate Editor: G. Manganaro.

The authors are with the Department of Microelectronic Engineering and Tyndall National Institute, University College Cork, Cork, Ireland (e-mail: zhipeng.ye@ue.ucc.ie; peter.kennedy@ucc.ie).

Digital Object Identifier 10.1109/TCSII.2007.896940

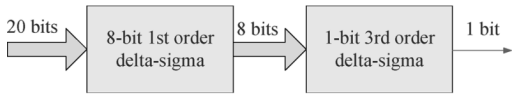

Fig. 1. Block diagram of the DSM from [9].

Dithering can be used to break the periodicity of cycles and thereby reduce or remove spurs but this requires additional hardware and inherently adds noise, albeit small and shaped. Kozak and Kale [5], and more recently Borkowski *et al.* [7], have shown that the MASH 111 DSM does not exhibit large spurs when the initial condition of the first stage is odd, due to the inherent whitening of the quantization error spectrum. Furthermore, Borkowski and Kostamovaara [8] have shown that guaranteeing maximum sequence lengths by setting the initial conditions in higher order modulators can be as effective as dithering in eliminating spurs.

In this brief, we address the issue of obtaining maximum length sequences without considering possible additional dithering. We note that the sequence length in a conventional MASH structure comprising first-order stages is determined primarily by that of the first stage in the cascade when the LSB of the input is set to "1" [7].

In [9], a first-order DSM is added as the input block of a third-order modulator, as shown in Fig. 1; it reduces the number of effective input bits from 20 to 8, while maintaining the accuracy of the input. This leads to sequence lengths that are comparable to a 20-bit modulator, but with less hardware than a comparable 19-bit third-order modulator.

In this brief, we extend this idea and apply it to the MASH architecture so that the hardware complexity can be reduced further.

In Section II, delta–sigma modulation for fractional-*N* frequency synthesis is reviewed and the conventional MASH DSM is discussed. In Section III, we describe our reduced complexity MASH DSM. Simulation and experimental results are presented in Sections IV and V and compared with the conventional structure. Finally, we draw some conclusions in Section VI.

II. DSM for Fractional-*N* Frequency Synthesis

Digital DSMs (DDSMs) are well known in the field of communication and have been used extensively in D/A conversion applications [10]. The fundamental operation of these modulators relies on the fact that a small amount of quantization noise power remains within the useful signal band, with the rest pushed to higher frequencies.

In fractional-*N* frequency synthesis applications, the same principles can also be exploited by pushing the phase error towards higher frequencies so that the phase noise in the vicinity of the desired carrier frequency is small [2]. Since the loop filter has a low-pass characteristic, the high-frequency phase error is suppressed.

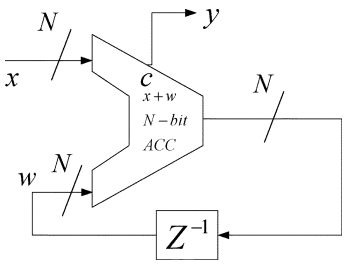

Fig. 2. Digital accumulator.

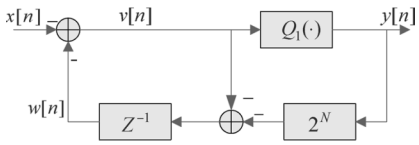

Fig. 3. Accumulator model.

Periodic behavior is inherently present in DDSMs because they are finite state machines [4]. This results in tonal behavior due to finite output sequence lengths. When the modulator generates a periodic output sequence with length L_s, the power of the quantization noise is spread among L_s tones. If the quantization noise is sufficiently randomized and L_s is large enough, the noise power does not concentrate into a few dominant spurious tones [7].

The guaranteed minimum sequence lengths for MASH DDSMs with identical first-order stages have been found by extensive simulation [7] and proven theoretically [11]. For first-, second- and third-order DSMs, the results are 2^N, 2^{N-1}, and 2^{N+1}, respectively, where N is the wordlength of the accumulator in the delta–sigma modulator, provided that the input is odd in the first-order DDSM and the initial condition is odd in the case of second and third-order DDSMs [7], [11].

The accumulator shown in Fig. 2 is used in the implementation of high-order MASH DSMs; its model is shown in Fig. 3.

The nonlinear difference equations governing the structure shown in Fig. 3 can be summarized as

$$v[n] = x[n] + w[n] \tag{1}$$

$$y[n] = Q_1(v[n]) = \begin{cases} 1, & v[n] \geq 2^N \\ 0, & v[n] < 2^N \end{cases} \tag{2}$$

$$w[n] = v[n-1] - 2^N \cdot y[n-1] \tag{3}$$

where 0 and 1 denote the output levels of the single-bit (or binary) quantizer, and $Q_1(\cdot)$ is the quantization function.

The block diagram of the *N*-bit accumulator is shown schematically in Fig. 4, where (1, *N*, *N*, 1) means first order, *N*-bit input, *N*-bit quantization error output, and 1-bit carry output, respectively. Since higher order delta–sigma modulators are widely used in frequency synthesis applications, the third-order MASH 111 DDSM shown in Fig. 5 is considered in this brief. It typically consists of three *identical N*-bit accumulators.

The output of the MASH 111 DDSM can be expressed in the *Z*-domain as

$$Y(z) = \mathrm{STF}(z) \cdot X(z) + \mathrm{NTF}(z) \cdot N_3(z) \tag{4}$$

Fig. 4. Block diagram of an *N*-bit accumulator.

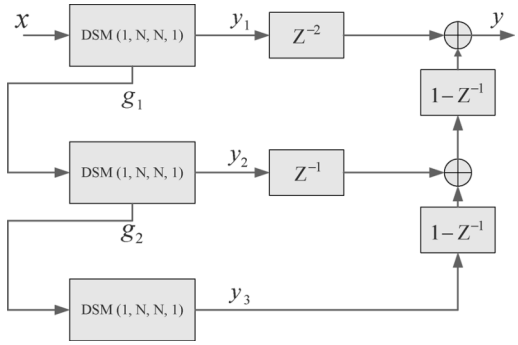

Fig. 5. Block diagram of a MASH 111 DDSM.

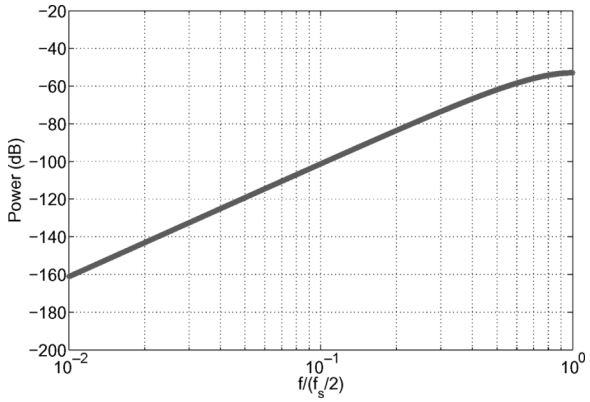

Fig. 6. Power predicted by the white noise model (6) assuming $L_s = 2^{20}$.

where $X(z)$, $N_3(z)$, $\mathrm{STF}(z)$, and $\mathrm{NTF}(z)$ are the z-transforms of the input, the quantizer error of the third stage, and the signal and noise transfer functions of the modulator, respectively. $\mathrm{STF}(z) = z^{-2}$ and the noise transfer function is given by

$$\mathrm{NTF}(z) = (1 - z^{-1})^3. \tag{5}$$

The idealized power spectrum of the shaped noise $\mathrm{NTF}(z) \cdot N_3(z)$, assuming a cycle of length L_s and white quantization noise, is given by

$$N(f[k]) = \frac{1}{12L_s} \left|\mathrm{NTF}(z)\right|^2_{z=e^{j2\pi k/L_s}}, \quad k = 0, 1, 2, \ldots, \frac{L_s}{2} - 1 \tag{6}$$

where $f[k] = (kf_s/L_s)$ and f_s is the clock frequency.

The predicted discrete power spectrum when $L_s = 2^{20}$ is shown in Fig. 6. For low frequencies, the slope of the curve is 60 dB/decade.

A. 19-Bit MASH 111 DDSM

The simulations in this brief were performed using a Verilog-HDL description of the digital hardware. In order to make a fair

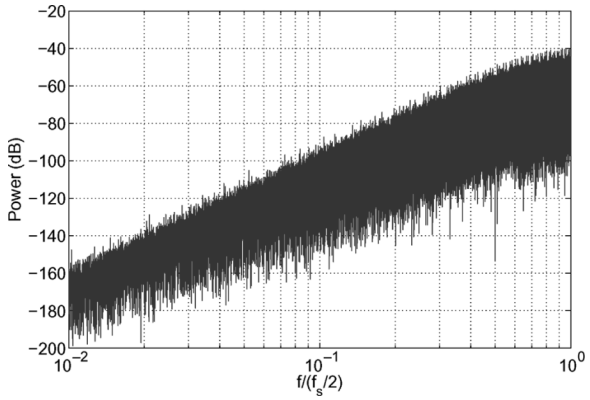

Fig. 7. Simulated power for conventional 19-bit MASH 111 DDSM; input is 52429.

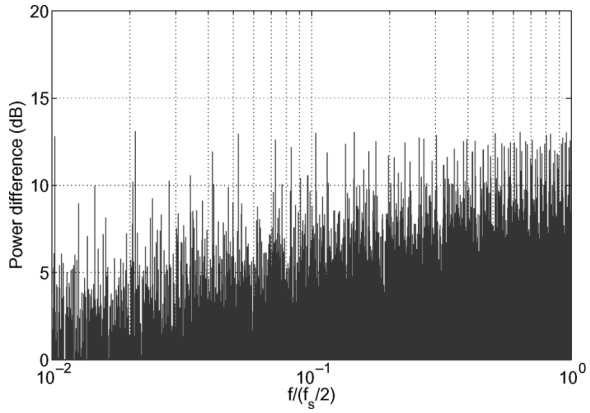

Fig. 8. Deviation of the power from the white noise model for a conventional 19-bit DDSM; input is 52429.

comparison, the inputs of the DSMs are chosen throughout the brief as the odd binary fractions closest to 0.1.

The output discrete power spectrum $P[k]$ of the DDSM is defined by (7), where $Y[k]$ is the discrete-time Fourier series (DTFS) [12] of the output of the DDSM with its dc term removed

$$P[k] = |Y[k]|^2 . \tag{7}$$

The power spectrum of a conventional 19-bit MASH 111 DDSM is shown in Fig. 7, where the slope of 60 dB/decade is observable. Although the power spectrum in Fig. 7 has the characteristic 60 dB/decade shape of the white noise model in Fig. 6, it differs qualitatively in two fundamental ways: 1) the curve is not smooth but contains a large number of discrete frequency components (giving rise to the spiky nature); 2) these tones are above the levels predicted by the white noise model (6).

The decibel difference between the actual power spectrum and the white noise model in Fig. 6 is shown in Fig. 8. Note that it exceeds the ideal in the worst case by 13 dB.

The output sequence length of the DDSM can be found in a number of ways. We consider the autocorrelation function, as suggested in [7]. From Fig. 9, we find that the output sequence length is $2^{(19+1)} = 1048576$, as expected [7], [11].

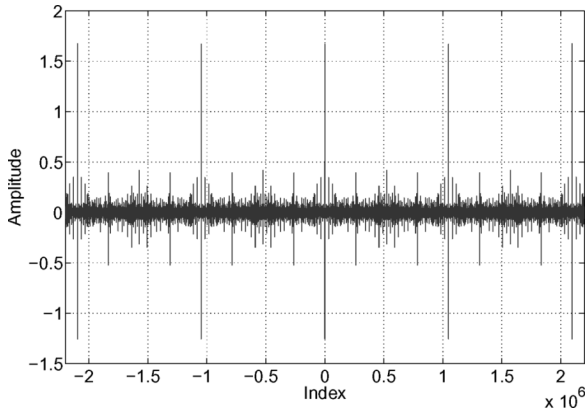

Fig. 9. Autocorrelation result for a conventional 19-bit MASH 111 DDSM; input is 52429.

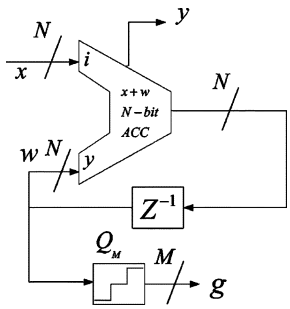

Fig. 10. *N*-bit digital accumulator with an *M*-bit quantizer.

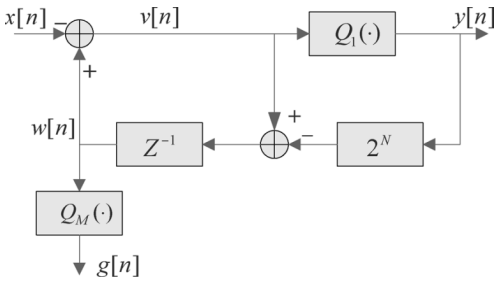

Fig. 11. Model of the *N*-bit accumulator with an *M*-bit quantizer.

III. Reduced Complexity MASH DDSM

The closeness of the power spectrum to the white noise approximation shown in Fig. 6 is influenced by the sequence length and the effective number of bits in the modulator. In our reduced complexity MASH DDSM, only the first accumulator has a long word (*N*-bit); by setting the LSB of the input to "1," this stage sets the sequence length to 2^N [11]. The error signal is quantized by an *M*-bit quantizer Q_M before being fed forward to the next stage. This is shown in Fig. 10, while the corresponding model and block diagram are shown in Figs. 11 and 12, respectively. The other accumulators use fewer bits to do the shaping. This allows us to reduce the word lengths in the following stages without reducing the sequence length.

The corresponding difference equations for this structure are (1)–(3) and (8), in which $Q_M(\cdot)$ models the *M*-bit quantizer

$$g[n] = Q_M\left(w[n]\right). \tag{8}$$

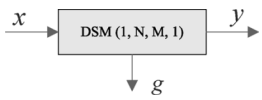

Fig. 12. Block diagram of the n-bit accumulator with an *M*-bit quantizer.

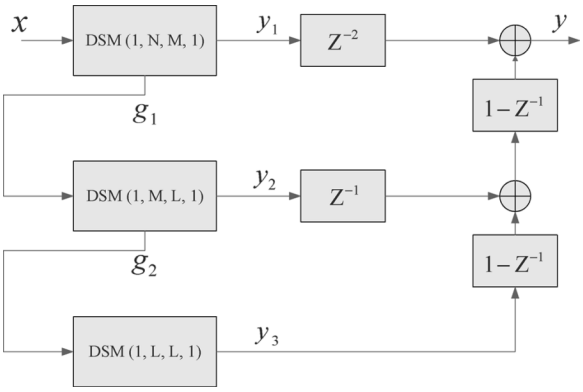

Fig. 13. MASH 111 DDSM: randomization is incorporated in the modulator.

The block diagram of our reduced complexity MASH 111 DDSM [13] is shown in Fig. 13. Its output can be expressed in the *Z*-domain as

$$Y(z) = \mathrm{STF}(z) \cdot X(z) + \mathrm{NTF}(z) \cdot N_3(z) + z^{-1}(1 - z^{-1}) \cdot N_{12}(z) + (1 - z^{-1})^2 \cdot N_{23}(z) \quad (9)$$

where $N_{12}(z)$ and $N_{23}(z)$ are the z-transforms of the quantizer errors introduced by the *M*-bit and *L*-bit quantizers between the first and second and second and third accumulators, respectively.

M and *L* should be chosen much larger than 1, so that the quantization errors from the *M*- and *L*-bit quantizers are much less than N_3. Although the contributions from N_{12} and N_{23} are only first- and second-order noise shaped, respectively, they are significantly below the N_3 contribution at high frequencies, where the DDSM has the greatest influence on the performance of a fractional-*N* frequency synthesizer.

IV. Simulation Results

In order to compare the performance of the new topology with the conventional one, simulation results for the new MASH 111 DSM are presented. Since the guaranteed output sequence length for the first-order DDSM is 2^N when the input is odd [7], [11], we use a 20-bit accumulator to guarantee that our structure always achieves the maximum possible sequence length 2^{20}, the same as the conventional 19-bit DSM discussed in Section II. Therefore, we set the LSB of our input to "1" and use only the 19 MSBs for the input x. A 12-bit accumulator and a 8-bit accumulator are used after the 20-bit accumulator to perform the higher order noise shaping. Thus, *N, M, L* are 20, 12, and 8 in this case.

The simulated output power spectrum is shown in Fig. 14. The expected 60 dB/decade slope is observed. The peak deviation from the white noise model of less than 8 dB in Fig. 15 is 5 dB less than in the case of the 19-bit conventional modulator discussed in the last section.

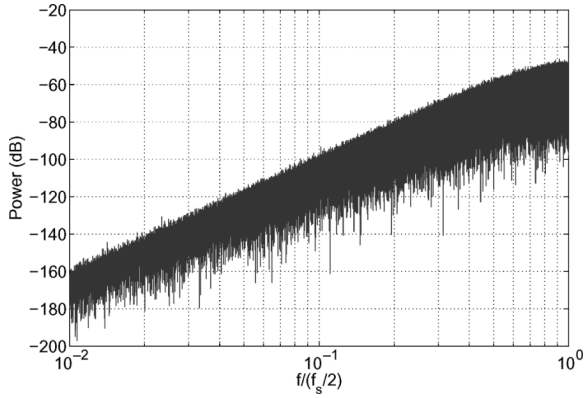

Fig. 14. Simulated power for the new 20-12-8-bit MASH 111 DSM; input is 104857.

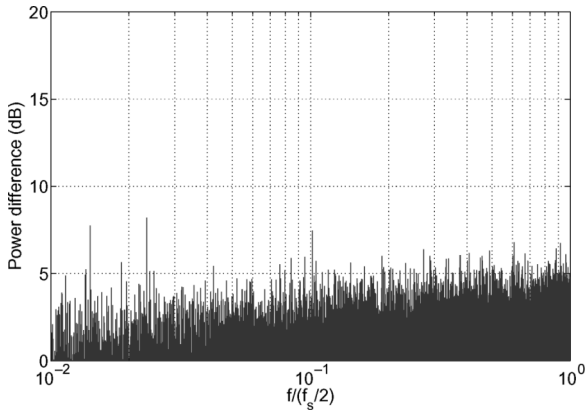

Fig. 15. Deviation of the power from the white noise model for the new 20-12-8-bit MASH 111 DSM; input is 104857.

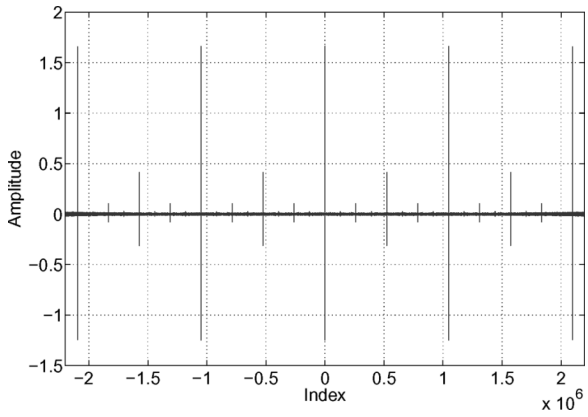

Fig. 16. Autocorrelation result for the new 20-12-8-bit MASH 111 DDSM; input is 104857.

The autocorrelation result shown in Fig. 16 confirms that the sequence length is 2^{20}, as expected. Note that the autocorrelation function in Fig. 16 is closer to white than that in Fig. 9. This superior whitening of the quantization noise manifests itself in the frequency domain as a smoother spectrum (Fig. 14 versus Fig. 7).

V. Experimental Results

We constructed an experimental demonstration system on a Xilinx Spartan-2E FPGA board clocked at $f_s = 2.5$ MHz. The

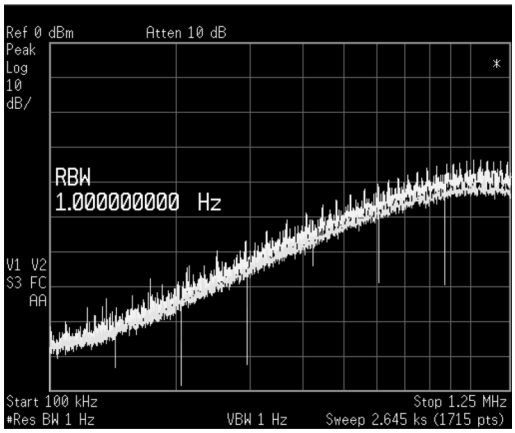

Fig. 17. Experiment results for the conventional 19-bit (upper, spiky curve; input is 52429) and the new 20-12-8 (lower, smooth curve; input is 104857) MASH 111 DDSM.

TABLE I
HARDWARE CONSUMPTION OF THE CONVENTIONAL 19-bit MASH 111 DDSM AND THE NEW 20-12-8 MASH 111 DDSM

DSM		19–bit	20–12–8 bit	(20-12-8/19-19-19)%
Hardware Consumption	FFs	105	71	68%
	LUTs	69	52	75%
	TEGs	1523	1033	68%

modulator output was converted to continuous time using an Analog Devices AD5445 12-bit DAC. Spectral measurements were made using an Agilent E4402B Spectrum Analyzer. Experimental measurements of the power spectrum of the conventional 19-bit MASH DDSM and the new 20-12-8 MASH modulator are shown in Fig. 17. The spectrum of the new structure is smoother, as expected, due to the more effective whitening of the quantization noise spectrum.

The hardware requirements for a conventional 19-bit and our new 20-12-8 bit DDSM are summarized in Table I. The hardware consumption is reported as the number of flip-flops (FFs) and the number of 4-input look-up tables (LUTs) which represent the synchronous logic and the asynchronous logic, respectively. Total equivalent gate (TEG) count for the design is given as well. They are based on the map report from the Xilinx ISE program [14].

From Table I, we see that the new 20-12-8 MASH 111 DDSM consumes 68% FFs and 75% LUTs of the conventional 19-bit MASH 111 DDSM. The total equivalent gate count in the new 20-12-8 DDSM is 68% of the conventional 19-bit DDSM. In addition, the new DDSM achieves a more smooth and lower level power spectrum. Thus, for a given spectral performance, the hardware requirements for this topology are significantly lower than for a conventional DDSM with identical stages.

VI. CONCLUSION

In this brief, a reduced complexity MASH DDSM has been presented. A long word is used for the first modulator in a MASH structure to maximize the sequence length; shorter words are then used in subsequent stages. A sequence length of 2^N is guaranteed by setting the LSB of the input to the delta–sigma modulator to "1." The performance of the architecture has been verified via Verilog HDL simulations and by experiment using a Xilinx Spartan-2E FPGA and Analog Devices AD5445 12-bit DAC. Our simulation and experimental results show that it performs better than the conventional MASH structure, but with less hardware. The same idea can be applied to higher order DDSMs, where the benefits of reduced complexity will be even greater.

We are currently developing an optimum strategy for selecting the resolutions of the inter-stage quantizers; we will report on this in a future publication.

ACKNOWLEDGMENT

The authors thank Analog Devices for providing the EVAL-AD5445EB DAC evaluation board in this project; C. McCarthy for building the experimental hardware; and K. Hosseini, Dr. O. De Feo, and the reviewers for constructive feedback.

REFERENCES

[1] V. Reinhardt, K. Gould, K. McNab, and M. Bustamante, "A short survey of frequency synthesizer techniques," in *Proc. 40th Ann. Freq. Contr. Symp.*, May 1986, pp. 355–365.
[2] T. A. Riley, M. Copeland, and T. Kwasniewski, "Delta–sigma modulation in fractional-*N* frequency synthesis," *IEEE J. Solid-State Circuits*, vol. 28, no. 5, pp. 553–559, May 1993.
[3] S. E. Meninger and M. H. Perrott, "A fractional-*N* frequency synthesizer architecture utilizing a mismatch compensated PFD/DAC structure for reduced quantization-induced phase noise," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 11, pp. 839–849, Nov. 2003.
[4] V. Friedman, "The structure of the limit cycles in sigma delta modulation," *IEEE Trans. Commun.*, vol. 35, pp. 784–796, Jul. 1989.
[5] M. Kozak and I. Kale, "Rigorous analysis of delta–sigma modulator for fractional-*N* PLL frequency synthesis," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 6, pp. 1148–1162, Jun. 2004.
[6] B. Miller and R. J. Conley, "A multiple modulator fractional divider," *IEEE Trans. Instrum. Meas.*, vol. 40, no. 3, pp. 576–583, Jun. 1991.
[7] M. J. Borkowski, T. A. D. Riley, J. Hakkinen, and J. Kostamovaara, "A practical $\Delta\Sigma$ modulator design method based on periodical behavior analysis," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 10, pp. 626–630, Oct. 2005.
[8] M. J. Borkowski and J. Kostamovaara, "On randomization of digital delta–sigma modulators with dc inputs," in *Proc. ISCAS 2006*, Kos, Greece, May 2006, pp. 3770–3773.
[9] B. Bornoosh, A. Afzali-Kusha, R. Dehghani, M. Mehrara, S. M. Atarodi, and M. Nourani, "Reduced complexity 1-bit high-order digital delta–sigma modulator for low-voltage fractional-*N* frequency synthesis applications," *Proc. IEE Circuits Devices Syst.*, vol. 152, no. 5, pp. 471–476, Oct. 2005.
[10] G. Temes, "delta–sigma D/A converters," in *Proc. IEEE Int. Symp. Circuits Syst. Tutorials*, 1994, pp. 225–234.
[11] K. Hosseini and M. P. Kennedy, "Mathematical analysis of digital MASH delta–sigma modulator for fractional-*N* frequency synthesizers," in *Proc. PRIME 2006.*, Otranto, Italy, Jun. 2006, pp. 309–312.
[12] S. Haykin and B. D. Van Veen, *Signals and Systems*, 2nd ed. New York: Wiley, 2003.
[13] M. P. Kennedy and Z. Ye, "A delta–sigma modulator," Irish Patent Appl. # 2006/0763, Oct. 17, 2006.
[14] *"SE Quick Start Tutorial"* 2005 [Online]. Available: http://toolbox.xilinx.com\\/docsan/xilinx7/books/docs/qst/qst.pdf