Effect of Solder Volume on joint shape with variable chip-to-board contact pad ratio.

Pio Jesudoss[1)], Alan Mathewson[1)], William Wright[2)], Brendan O' Flynn[1)] and Frank Stam[1)]

[1)] Microelectronics Applications Integration
Tyndall National Institute, Lee Maltings, Prospect Row, Cork, Irland
[2)] Department of Electrical and Electronic Engineering, University College Cork, Cork, Ireland

***Abstract**: The objective of this paper is to investigate the effect of the pad size ratio between the chip and board end of a solder joint on the shape of that solder joint in combination with the solder volume available. The shape of the solder joint is correlated to its reliability and thus of importance. For low density chip bond pad applications Flip Chip (FC) manufacturing costs can be kept down by using larger size board pads suitable for solder application. By using "Surface Evolver" software package the solder joint shapes associated with different size/shape solder preforms and chip/board pad ratios are predicted. In this case a so called Flip-Chip Over Hole (FCOH) assembly format has been used. Assembly trials involved the deposition of lead-free 99.3Sn0.7Cu solder on the board side, followed by reflow, an underfill process and back die encapsulation. During the assembly work pad off-sets occurred that have been taken into account for the Surface Evolver solder joint shape prediction and accurately matched the real assembly. Overall, good correlation was found between the simulated solder joint shape and the actual fabricated solder joint shapes. Solder preforms were found to exhibit better control over the solder volume. Reflow simulation of commercially available solder preform volumes suggests that for a fixed stand-off height and chip-board pad ratio, the solder volume value and the surface tension determines the shape of the joint.*

1. INTRODUCTION

Flip-Chip interconnection involves attaching chip's bond pads face down on to a substrate directly. This technology developed by IBM in the 1960's under the name of C4 (controlled collapse method) has been used increasingly and has a projected growth rate of 30-40% in the next decade [1], [2].

The demand for bare die packaging to have high reliability at reduced cost makes flip chip (FC) technology a preferable choice compared to the more conventional wire bonding technologies[3], [4].

For low density chip bond pad applications FC manufacturing costs can be kept down by using larger size board pads suitable for solder application. Larger board pad geometries could reduce the direct cost of the board, but also the cost of the FC assembly since the application of interconnect material can be achieved at lower cost

In a Flip Chip Over Hole (FCOH) process the solder joint connections between a flexible substrate and a direct attached chip is of particular interest, because it defines the electrical reliability of the connection. Figure 1 illustrates the requirement of the solder joint shape when the substrate is exposed to bending,

In an earlier study [5], assemblies of chip-to-board interconnection with variable aspect ratio contact pad areas were compared to the equilibrium shapes of solder joint predicted by Surface Evolver [6]. This study showed that, when offset is taken into account, there is a good correlation between Surface Evolver shape prediction and the observed experimental shape, as shown in figure.2.

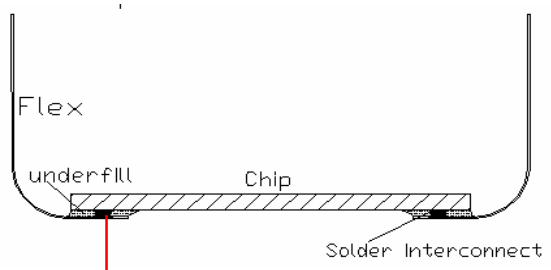


Fig. 1. Schematic of FCOH

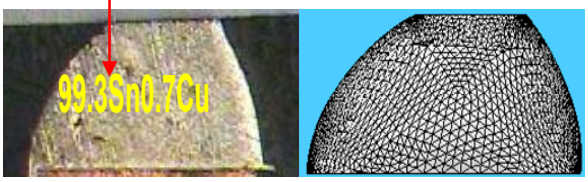


Fig. 2. Cross-section of ratio $chip_{pad}/sub_{pad}$ 0.6 and its corresponding Surface Evolver predicted shape.

In all FC applications rigorous control of dispensed solder volume is essential in obtaining the repeatability of the standoff height and the shape of the joint. Solder volume is one of the essential parameters in determining the stress in the joints [7], [8], [9]. There is a wide range of solder application techniques that can be used to control the solder volume, this includes evaporation, electroplating, stencil printing, electroless plating and solder jet printing techniques. Since cost effectiveness is an issue in most applications, stencil printing is the most commonly used technique [10] to control solder volume where the volume control is a major issue [8], [11]. Even though Screen printing is favoured for small bond pads, the assembly considered in this work has variable aspect ratio with large bond pads on the substrate side. Therefore, the control of volume is obtained by the use of solder preforms.

In typical IC and system assembly applications, similar chip-to-board bond pad aspect ratios are used to achieve a reliable interconnection [12]. Yeung et al [13] have used the Surface Evolver to predict solder joint shape and have also shown that a 50% increase in pad size resulted in the reduction of the standoff height for parallel chip-to-board pads. However, no studies have been reported on the impact of commercially available solder preform volumes on the joint shape with a variable chip-to-board pad contact ratio.

The preliminary work presented here describes the effect of commercially available solder preform volumes on the joint shape depending on chip-to-board contact pad ratio and how Surface Evolver could be used as a tool for solder preform selection.

In the next section, a detailed review of the solder preforms, chip, substrate, and the FCOH packaging will be presented. This is followed by results, a discussion and conclusions.

2. EXPERIMENTAL METHODOLOGY

In order to verify the objective of the paper, "surface evolver" has been used to simulate the effect of solder preform volume on the shape of the joint. To corroborate the simulated results the following assembly approach was considered.

2.1. Solder Preforms

Solder preforms are custom made solder pellets that are commercially available. They consist of predetermined quantities of solder alloy, and come in different shapes ands sizes, with tight volume tolerances.

2.2. The Test Chip

The chip developed for this research has a low bond pad count of 5 and measures 6 x 6 mm. Three different size chip bond pads have been used: 100µm, 300µm, and 500µm square.

2.3. Substrate

A thin Flex board of thickness 0.025mm was fabricated for this research. The board pad metallization scheme consist of 15µm Cu, 5µm Ni and 0.05µm of electroplated flash gold. A square window of 4.4mm was cut from the centre of the board to expose the chip to external conditions.

2.4. Assembly Process

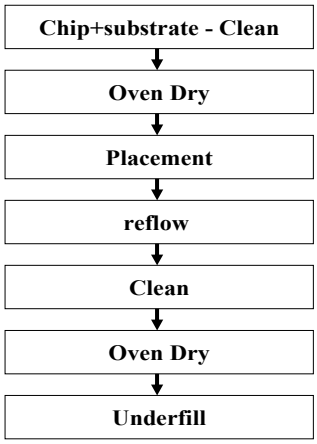


Fig. 3. Process flow for flip chip assembly

3. SURFACE EVOLVER

The Surface Evolver is an interactive program [6], which models surfaces shaped by different constraints and energies. An initial surface can be defined in a data file and it becomes possible to visualise the evolution of the surface towards its minimal energy by a gradient descent method in the Surface Evolver programme. The energy in the Evolver can be a combination of surface tension, gravitational energy, squared mean curvature or user-defined surface integrals.

In the data file that is presented to the simulator, the basic geometric elements used to represent a surface are vertices, edges, facets, and bodies. Vertices are points, edges are straight line segments joining pairs of vertices, and facets are flat triangles bounded by three edges. A surface is a union of facets and a body is defined by its bounding facets. The term "surface" refers to all of the geometric elements plus supplementary data such as constraints, boundaries, and forces. A surface has a total energy which arises from surface tension, gravitational energy, and possibly other sources and the lowest level of this combination of energies is determined in the simulation

In the case of modelling liquid solder, the energies that are taken into account are surface tension, the gravitational energy and the external energy due to the applied loads such as the weight of the package [15]. As opposed to most Ball Grid Array (BGA) packages, the bare die with small weight [16] is considered in this technology and therefore the external pressure from the weight of the chip could be excluded from equation 1 given below.

$$E = \int_V \rho g z dV + \int_S T dS \qquad (1)$$

Where ρ, g are the corresponding solder density, gravity and z the height between the $chip_{pad}$ and $substrate_{pad}$. V represents the volume of solder, T the surface tension and S the solder surface. E is the potential energy that governs the solder joint geometry.

4. RESULTS AND DISCUSSION

4.1. Critical solder volume

For a variable aspect ratio chip-to-board contact pad geometry, the critical volume (V_c) from where a small increase or decrease in volume leads to either a convex or a concave shaped joint was calculated using the following trapezoid volume (figure 4) equation 2.

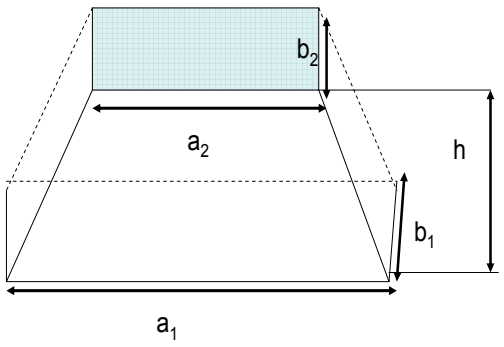


Fig.4. Schematic of trapezoid where a_1, a2 are the lengths, b_1 and b_2 widths and h the height. In the trapezoid, a2xb2 represents the chip pad while a1xb1 represents board pad and h is stand-off height

$$V_c = \left[a_1 * b_1 + a_2 * b_2 + \left(a_1 * b_2 + a_2 * b_1\right)/2 \right] * \frac{h}{3} \qquad (2)$$

This critical solder volume was calculated for different chip-to-board pad ratio's and is presented in Table 1.

Ratio $chip_{pad}/sub_{pad}$	V_c (mm^3)
0.2	0.015
0.6	0.024
1	0.037

Table. 1. Critical solder volume for different chip-to-pad ratios.

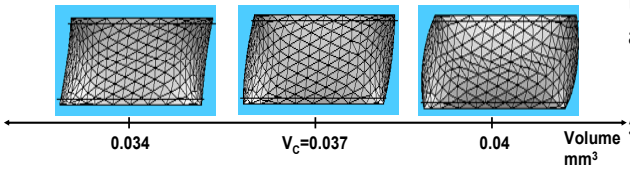


Fig. 5. Variations of the shape of the joint with the increase or decrease of 8.1 percent solder volume.

The results for simulated joints with a pad ratio 1, are shown in figure 5. In this particular case, an increase or decrease in solder volume by 8.1 percent will respectively result in either a convex or concave joint.

4.2. Surface Evolver as a tool in selecting solder preforms and volume effect

Commercially available solder preform volumes are used in simulating the joints for variable contact pad ratio as shown in figure 6.

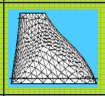
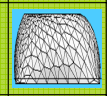
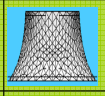
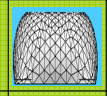
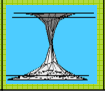
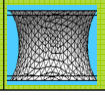
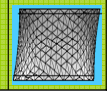
Ratio $chip_{pad}/sub_{pad}$	H (mm)	Vol (mm^3) $3.277*10^{-3}$	Vol (mm^3) $1.6387*!0^{-2}$	Vol (mm^3) $3.277*10^{-2}$	Offset In y direction (µm)
0.2	0.15				150 −y direction
0.6	0.15				60 +y direction
1	0.15				40 +y direction

Fig.6. Equilibrium shapes of solder joints predicted by Surface Evolver for commercially available solder preforms

The simulated results show that for a certain chip-to-substrate pad ratio and constant standoff height, volume is an important parameter in determining the shape of the joint. These simulated results help to choose the appropriate solder preforms to obtain the required solder shape to lower the stress in the joints. For example it shows that the joint formed with the volume of 0.003mm^3 simulated for ratio $chip_{pad}/sub_{pad}$ 1 and a standoff height of 0.15mm would have robustness, while volume of 0.016mm^3 and 0.03mm^3 could provide a stable joint. This shows that Surface Evolver could be used in the process as a selection tool in choosing solder preforms for the chosen application.

5. CONCLUSION

This preliminary work shows that Surface Evolver can accurately predict the joint shape formed by variable chip-to-substrate contact pad area ratio's for a given volume. It also provides an insight in the importance of solder volume control in shaping the joint. Finally it shows that Surface Evolver could be used as a selection tool in choosing more suitable solder preforms for the required application.

The use of concave shaped joints in an assembly could improve the joint fatigue life [17], [18]. From a mechanical point of view, a convex shaped joint would accumulate stress at the solder-pad interface whereas the concave shaped joint would absorb the stress. The convex shaped joints are most likely to fail at the solder-pad interface while the concave shaped joints at the neck of the joint. This is in accordance with the observation by Xingheng Liu et al. However, R.S. Cheng et al [19] and I. K. Hui et al [20] state that the convex shaped joints would have longer fatigue life. Future work on this subject will incorporate the simulated joint shapes in ANSYS or Coventor to study the stress in the joints as a function of thermal and mechanical excursions and assist choosing the optimum shape joint for this application.

ACKNOWLEDGEMENT

The author would like to acknowledge Enterprise Ireland for providing the opportunity to carry out the work presented in this paper

The author of this paper would like to thank Prof. Brakke for making this software freely available and for helping him resolve certain code problems. Prof. Brakke was not directly involved in the project, so the

author takes the sole responsibility for any errors or omissions.

REFERENCES

[1] Satoru Zama, Daniel F. Baldwin, Toshiya Hikami, and Hideaki Murata, "Flip Chip Interconnect Systems Using Copper Wire Stud Bump and Lead Free Solder", *IEEE Transaction on Electronics Packaging Manufacturing*, Vol. 24, No. 4, October 2001, pp. 261-268.

[2] Zhaowei Zhong, "Assembly and reliability of flip chip on boards using ACAs or eutectic solder with underfill", *Microelectronics International*, Vol. 16, No. 3, 1999, pp. 6-14.

[3] John Lau and Ray Chen, "Cost Analysis: Solder Bumped Flip Chip verses Wire Bonding", *IEEECPMT Int'l Electronics Manufacturing Technology Synopsium,* 1998, pp. 464-472.

[4] Frank E. Sauser, Chunyan Li, Richard G. AzizKhan, Chong H. Ahn, and Ian Papautsky, "Pressure Pressure Microsensing Catheters for Neonatal Care ", *IEEE,* 2001, pp. 1476-1479.

[5] Pio Jesudoss, Alan Mathewson, William Wright, and Frank Stam, "Evaluation of chip-to-board interconnection using variable aspect ratio contact pad areas", *Proc. 26th International Conference On Microelectronics (MIEL 2008)*, Vol. 2, Niš, Serbia, may 2008, pp. 565-568.

[6] K.A. Brakke, "Surface Evolver version 2.30c", *Susquehanna University*, 2008. Available for free download fromhttp://www.susqu.edu/brakke/evolver/evolver.html. The windows version has been used for this paper.

[7] Jean-Paul Clech, "Flip-Chip / CSP assembly Reliability and Solder Volume effects", *SMI*, 1998, pp. 1-10.

[8] Peter M. Martino, Gary M. Freedman, Livia M. Raczm Julian Szekely, "Prediction Solder Joint Shape by Computer Modeling ", *IEEE*, 1994, pp. 1071-1078.

[9] Bingzhi Su, Saeed Hareb, Y. C. Lee, Mirng-Ji Lii and Mark E Thurston, "Solder Joint Reliability Modeling for a 540-I/O Plastic Ball-Grid-Array Assembly", *IEEE International Conference on Multichip Modules and High Density Packaging*, 1998, pp. 422-428.

[10] David A. Hutt, Daniel G. Rhodes, Paul P. Conway, Samjid H. Mannan, "Investigation of a Low Cost Solder Bumping Technique for Flip-Chip Interconnection", *IEEE/CPMT Int'l Electronics Manufacturing Technology Symposium*, 1999, pp. 334-342.

[11] Changaing Liu, M. W. Hendriksen, David A. Hutt, Paul P. Conway, and David C Whalley, "Materials and Processes Issues in Fine Pitch Eutectic Solder Flip Chip Interconnection", *IEEE Transaction on Components and Packaging Technologies*, Vol. 29, No. 4, December 2006, pp. 869-876.

[12] Peter Wölflick, Klaus Feldman, " Lead-Free Low-Cost Flip-Chip Process chain: Layout, Process, Reliability", *IEEE/SEMI Technology Symposium:International Electronics Manufacturing Technology (IEMT) Symposium*, 2002, pp. 27-34.

[13] Betty H. Yeung and Tien-Yu Tom Lee. "Evaluation and Optimization of Package Processing and Design Through Solder Joint Profile Prediction", *IEEE Transactions on Electronics Packaging Manufacturing*, January 2003, Vol. 26, No. 1,pp. 68-74.

[14] Mike Fenner, "Solder Preforms: Constant Solder Volumes For consistent Assembly", *OnBoard Technology*, February 2005, pp. 46-47.

[15] Sidharth, Richard Blish and Devendra Natekar, "Solder Joint Shape and Standoff Height Prediction and Integration with FEA_Based Methodology for Reliability Evaluation", *IEEE Electronic Components and Technology Conference*, 2002, pp. 1739-1744.

[16] Lewis S. Goldmann, "A Heuristic Force-Height Equation for Molten Axisymmetric solder joints", *IEEE*, 1993, pp. 1120-1124.

[17] Xingsheng Liu and Guo-Quan Lu, "Effects of Solder Shape and Heights on Thermal Fatigue Lifetime", *IEEE Transaction on Components and Packaging Technologies*, Vol. 26, No. 2, June 2003, pp. 455-465.

[18] T. H. Juand Y. C. Lee, "Effects of Ceramic Ball-Grid-Arrray Package's Manufacturing Variations on Solder Joint Reliability", *MCM Proceedings,1994*, pp. 514-519.

[19] R. S. Chen, S. C. Tseng and C. S. Wan, "Effect of Solder Joint Structure and Shape on Thermal Reliability of Plastic Ball Grid Array Package", *Int J Adv MAnuf Technol*, 2006, pp. 677-687

[20] I. K. Hui and B Ralph, "A Study of the Strength and Shape of Surface mount Technology Leadless Chip Solder Joints ", *Proc Instn Mech Engrs*, Vol. 211, Part B, 1995, pp. 29-41.

.

.