On the Robustness of R-$2R$ Ladder DAC's

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***Abstract*—A model of the linear R-$2R$ ladder digital-to-analog converter (DAC) is developed in terms of the ratios of the effective resistances at the nodes of the ladder. This formulation demonstrates clearly why an infinite number of different sets of resistors can produce the same linearity error and shows how this error can be reduced by trimming. The relationship between the weights of the bits and the resistor ratios suggests appropriate trimming, design, and test strategies.**

***Index Terms*—Data converters, digital-to-analog conversion, mixed-signal circuits, resistive ladders.**

I. Introduction

MUCH theoretical work in recent years has been devoted to the problem of testing analog and mixed-signal integrated circuits [1]–[8]. In particular, the element-value solvability problem[8] is concerned with determining whether or not it it possible to find the values of (possibly faulty) parameters of a circuit from a set of measurements. This is related to the problem of selecting a limited number of testpoints to perform a test efficiently using a minimum number of measurements [8].

The majority of the circuit theoretic studies of fault location and element solvability assume that a test engineer has access to a sufficiently large number of nodes in the circuit under test. While this may be a valid assumption for board-level work, it does not hold for many integrated circuits, where a limited number of variables may be accessible. An extreme case is a data converter where a single input or output is available. Here, a nonunique relationship between element values and linearity error can produce robustness of the functionality against variations in internal parameter values.

It is well known that the linearity error of an R-$2R$ ladder DAC may be reduced by trimming the resistors appropriately. What may appear surprising is that a given trimming procedure can improve the linearity of the device by moving the resistors away from their nominal values. This property results from the structural robustness of the ladder.

In this work, we derive a simplified model, in terms of resistance ratios, of a digital-to-analog converter (DAC) based on a resistive ladder [9] which consists of linear resistors and ideal open/short switches. We study the connection between the weights of the bits and the resistance ratios in order to gain insight into the robustness of the resistive ladder architecture.

In particular, we show that given access to all digital inputs of the DAC, and to only one output node, it is impossible to determine the values of the resistors in the ladder. Only resistor ratios are important in determining the transfer characteristic of the DAC, and these ratios can be determined in principle from a limited set of measurements. This observation can be exploited in defining model-based trim, design, and test strategies [10] for R-$2R$ ladder DAC's.

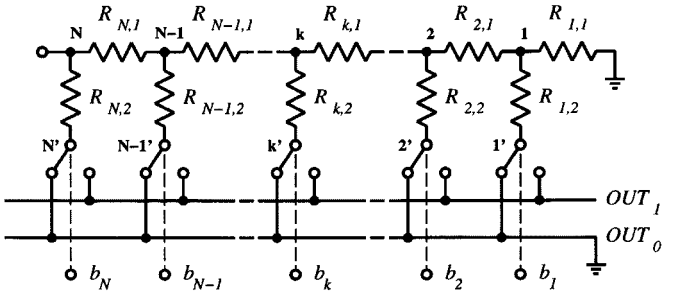

Fig. 1. R-$2R$ ladder consisting of linear resistors and open/short switches controlled by bits b_k, $k = 1, 2, \cdots, N$.

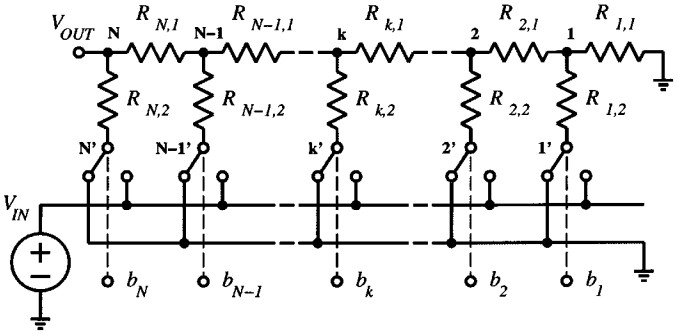

Fig. 2. Voltage-mode R-$2R$ ladder.

II. The Model

Throughout this work, we consider the N-bit R-$2R$ ladder shown in Fig. 1. We extend our analysis in Section V to include also a segmented resistive ladder architecture.

Associated with each node k of the ladder is a pair of linear resistors, $R_{k,1}$ and $R_{k,2}$, which connect it to nodes $k-1$ and k', respectively. An ideal open/short switch connects node k' to the OUT_0 or OUT_1 node, depending on whether the corresponding input bit b_k is 0 or 1.

For notational convenience, we denote by $R_{k,3}$ the effective resistance at node k seen looking into the left-hand end of $R_{k,1}$. In addition, we define the ratios

$$r_k = \frac{R_{k,3}}{R_{k,2}}, \qquad k = 1, 2, \cdots. \tag{1}$$

The R-$2R$ ladder is typically used in one of two ways to construct a DAC. Current mode exploits current division along the ladder while voltage mode is based on voltage division [11]. In this work, we treat only voltage-mode operation.

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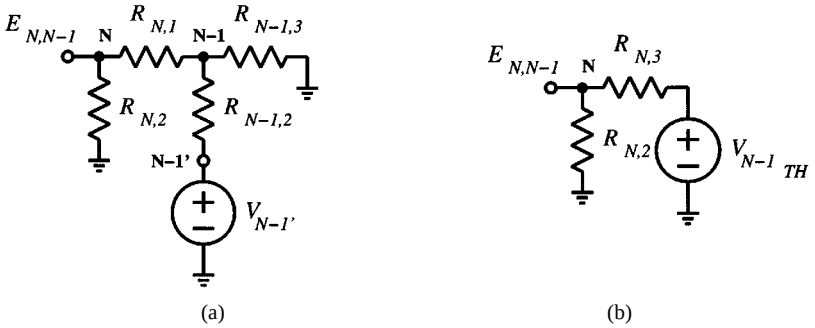

Fig. 3. (a) Equivalent circuit for calculating the contribution $E_{N,\,N-1}$ of $V_{N-1'}$ to $V_{\rm OUT}$. (b) Its simplified Thévenin equivalent.

TABLE I
VOLTAGE-MODE R-$2R$ LADDER DAC. $R_{k,1}$ AND $R_{k,2}$ DENOTE THE RESISTORS IN FIG. 2 AND r_k, $k = 1, \cdots, 8$ ARE THE CORRESPONDING RATIOS DEFINED BY (1). w_k IS THE WEIGHT ASSOCIATED WITH BIT k AS DETERMINED FROM MEASUREMENTS OF $V_{\rm OUT}$; $\hat{r}_k$ IS THE CORRESPONDING ESTIMATE OF r_k

k	$R_{k,1}(\Omega)$	$R_{k,2}(\Omega)$	r_k	w_k	$\hat{r}_k$
1	20020	20000	1.0010000000	0.0039085941	1.0010000000
2	9990	20000	0.9997498751	0.0078113293	0.9997498751
3	10010	20000	1.0004374609	0.0156314480	1.0004374609
4	9990	20000	0.9996093413	0.0312438503	0.9996093413
5	10010	20000	1.0004023162	0.0625250558	1.0004023162
6	9990	20000	0.9996005588	0.1249750268	0.9996005588
7	10010	20000	1.0004001198	0.2501000237	1.0004001198
8	9990	20000	0.9996000099	0.4998999825	0.9996000099

TABLE II
VOLTAGE-MODE R-$2R$ LADDER DAC. $R_{k,1}$ AND $R_{k,2}$ DENOTE THE RESISTORS IN FIG. 2 AND r_k, $k = 1, \cdots, 8$ ARE THE CORRESPONDING RESISTANCE RATIOS DEFINED BY (1). w_k IS THE WEIGHT ASSOCIATED WITH BIT k AND $\hat{r}_k$ IS THE ESTIMATE OF r_k

k	$R_{k,1}(\Omega)$	$R_{k,2}(\Omega)$	r_k	w_k	$\hat{r}_k$
1	40040.000	40000	1.0010000000	0.0039085941	1.0010000000
2	19980.000	40000	0.9997498751	0.0078113293	0.9997498751
3	20020.000	40000	1.0004374609	0.0156314480	1.0004374609
4	19980.000	40000	0.9996093413	0.0312438503	0.9996093413
5	20020.000	40000	1.0004023162	0.0625250558	1.0004023162
6	19980.000	40000	0.9996005588	0.1249750268	0.9996005588
7	20060.016	40040	1.0004001198	0.2501000237	1.0004001198
8	19959.996	40000	0.9996000099	0.4998999825	0.9996000099

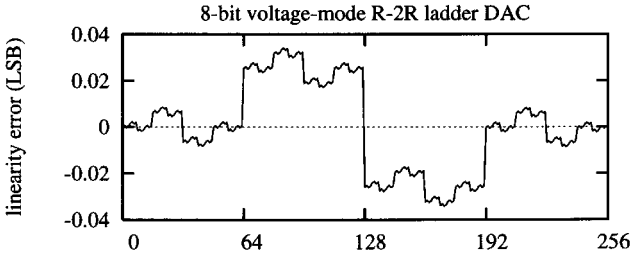

Fig. 4. Linearity error associated with the ladders detailed in Tables I and II.

III. VOLTAGE-MODE OPERATION

A DAC exploiting an R-$2R$ ladder in voltage mode is shown in Fig. 2. In this case, bit b_k of the input word causes node k' to be connected to ground or to $V_{\rm IN}$ if b_k = 0 or 1, respectively.

Since the R-$2R$ ladder we consider is linear, the superposition theorem [12] applies, and the voltage at the output node N may be determined by summing the contributions from each of the inputs $V_{k'}$ with all other sources zeroed. Thus

$$V_{\rm OUT} = \sum_{k=1}^{N} E_N, k$$

where $E_N k$ is the contribution to the voltage at node N due to voltage $V_{k'}$ applied at node k'.

Consider first the contribution due to $V_{N'}$ with all other sources zeroed. In this case, node N is connected to $V_{N'}$ via $R_{N,\,2}$ and to ground via the equivalent resistance $R_{N,\,3}$. By voltage division

$$E_N, N = \frac{R_{N,3}}{R_{N,\,2} + R_{N,3}}\, V_{N'} = \frac{r_N}{1 + r_N}\, V_{N'}$$

where r_N is as defined in (1).

At node $N-1$, the equivalent circuit for calculating the contribution to $V_{\rm OUT}$ of $V_{N-1'}$ acting alone is shown in Fig. 3(a). $R_{N-1,\,3}$ denotes the total resistance seen by node $N-1$ looking into $R_{N-1,\,1}$.

The contribution due to $V_{N-1'}$ acting alone is

$$\begin{aligned} E_{N,\,N-1} &= \frac{R_{N,\,2}}{R_{N,\,2} + R_{N,\,3}}\, V_{N-1_{TH}} \\ &= \left(\frac{r_N - 1}{1 + r_N - 1}\right) \frac{1}{1 + r_N}\, V_{N-1'}. \end{aligned}$$

Repeating this process along the ladder, it can be shown in general that $E_N, k = w_k V_{k'}$ for $k = 1, 2, \cdots, N$, where

$$w_k = \begin{cases} \dfrac{r_N}{1 + r_N}, & \text{if } k = N \\ \left(\dfrac{r_k}{1 + r_k}\right) \displaystyle\prod_{j=k+1}^{N} \left(\frac{1}{1 + r_j}\right), & \text{if } k < N. \end{cases} \tag{2}$$

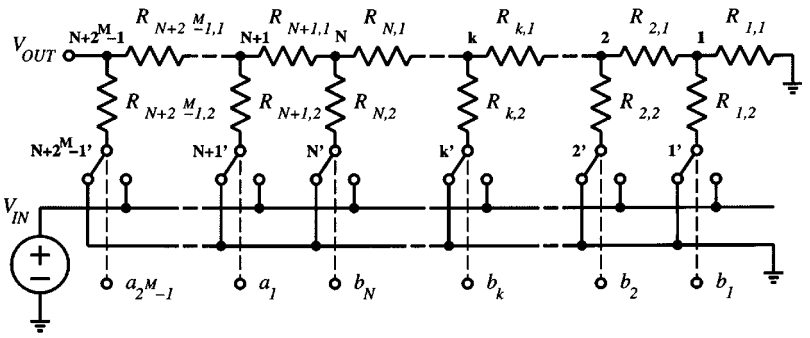

Fig. 5. Segmented voltage-mode resistive ladder DAC. In the nominal ladder, $R_{k,2} = 2R$ for all k, $R_{1,1} = 2R$, $R_{k,1} = R$ for $k = 2, 3, \cdots, N+1$, and $R_{k,1} = 0$ for $k = N+2, \cdots, N+2^M-1$.

The voltage applied at node k' is 0 or $V_{\rm IN}$, depending on whether $b_k = 0$ or 1. Thus, $V_{k'} = b_k V_{\rm IN}$. The total output voltage is given by

$$\begin{aligned} V_{\rm OUT} &= \sum_{k=1}^{N} E_N, k \\ &= \sum_{k=1}^{N} b_k w_k V_{\rm IN} \\ &= [\,b_1 \quad b_2 \quad \cdots \quad b_k \quad \cdots \quad b_{N-1} \quad b_N\,] \begin{bmatrix} w_1 \\ w_2 \\ \vdots \\ w_k \\ \vdots \\ w_{N-1} \\ w_N \end{bmatrix} V_{\rm IN}. \end{aligned}$$

A. Operation of the Ideal R-$2R$ Ladder

In an ideal R-$2R$ ladder, $R_{k,3} = R_{k,2}$ for $k = 1, 2, \cdots, N$. Hence, $r_k = 1$ for $k = 1, 2, \cdots, N$ and $w_k = 1/2^{N-k+1}$. Therefore

$$\begin{aligned} V_{\rm OUT} &= \sum_{j=1}^{N} \frac{b_j}{2^{N-k+1}} V_{\rm IN} \\ &= \frac{U}{2^N} V_{\rm IN} \end{aligned}$$

where $b_N b_{N-1} \cdots b_2 b_1$ is the binary expansion of the input word U.

B. Determination of Resistance Ratios

We ask the question: can one determine the ratios r_k, $k = 1, 2, \cdots, N$ in an R-$2R$ ladder DAC simply by measuring the output voltage $V_{\rm OUT}$?

Let $V_{\rm OUT}(U)$ be the measured output corresponding to input word U, as before. In the voltage-mode case, a judiciously chosen subset of N measurements (out of a possible 2^N) is sufficient to determine the weights w_k. In particular, we have that

$$\begin{bmatrix} V_{\rm OUT}(1) \\ V_{\rm OUT}(2) \\ V_{\rm OUT}(4) \\ \vdots \\ V_{\rm OUT}(2^{N-2}) \\ V_{\rm OUT}(2^{N-1}) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & \cdots & 0 & 0 \\ 0 & 1 & 0 & \cdots & 0 & 0 \\ 0 & 0 & 1 & \cdots & 0 & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & 1 & 0 \\ 0 & 0 & 0 & \cdots & 0 & 1 \end{bmatrix} \begin{bmatrix} w_1 \\ w_2 \\ w_3 \\ \vdots \\ w_{N-1} \\ w_N \end{bmatrix} V_{\rm IN} = \begin{bmatrix} w_1 \\ w_2 \\ \vdots \\ w_{N-1} \\ w_N \end{bmatrix} V_{\rm IN} \tag{3}$$

where $V_{\rm OUT}$ is measured at $U = 1, 2, 4, 8, \cdots, 2^N$.

Thus, the weights w_k of a voltage-mode DAC can in principle be determined with just N measurements, provided that $V_{\rm IN}$ is known. From these weights w_k, the ratios r_k may be estimated by setting

$$\hat{r}_N = \frac{w_N}{1 - w_N}$$

and evaluating

$$\hat{r}_k = \frac{\rho_k}{1 - \rho_k}$$

for $k = (N-1)$ to 1 in turn, where

$$\rho_k = w_k \prod_{j=k+1}^{N} (1 + \hat{r}_j).$$

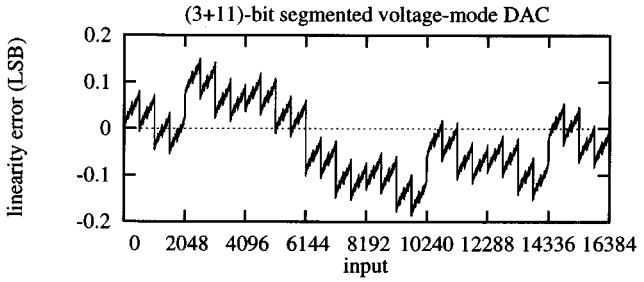

Fig. 6. Endpoint-corrected linearity error associated with the (3 +11)-bit segmented voltage-mode DAC in Table III. The linearity error is given by $(16383/V_{\rm OUT}(16383))V_{\rm OUT}(U) - U$, $U = 0, 1, 2, \cdots, 16383$.

Now $\hat{r}_k$ provides an estimate of r_k. In a process monitoring role, these estimates could potentially be used to quantify the deviation of production parts from their nominal design values. From a test engineering perspective, the extracted weights w_k can be exploited in linear error mechanism modeling [8], [10].

C. Example

Consider the two voltage-mode R-$2R$ ladder DAC's whose resistor values are given in Tables I and II, respectively. Here, the ladders are mismatched in a similar way but the normalized resistances of the ladders are different (10 and 20 kΩ, respectively). Output measurements are simulated for $V_{\mathrm{IN}} = 5$ V in both cases. While the values of the resistors in the 20 kΩ ladder are not quite double those in the 10 kΩ ladder, they have been chosen so that the ratios r_k and weights w_k are identical.[1] Therefore, the normalized error plots for these devices, shown in Fig. 4, are also identical; equivalently, both devices belong to the same ambiguity group [7], [8].

In both of these examples, the estimates $\hat{r}_k$, $k = 1, 2, \cdots, 8$ of the resistance ratios determined from simulations of the two ladders are identical to ten decimal places.

IV. Relationship Between Weights w_k and Ratios r_k

It is interesting to note the form of the weights in the eight-bit case

$$
\begin{aligned}
w_1 &= \left(\frac{r_1}{1+r_1}\right)\left(\frac{1}{1+r_2}\right)\left(\frac{1}{1+r_3}\right)\\
&\quad\cdot\left(\frac{1}{1+r_4}\right)\left(\frac{1}{1+r_5}\right)\left(\frac{1}{1+r_6}\right)\\
&\quad\cdot\left(\frac{1}{1+r_7}\right)\left(\frac{1}{1+r_8}\right)\\
w_2 &= \left(\frac{r_2}{1+r_2}\right)\left(\frac{1}{1+r_3}\right)\left(\frac{1}{1+r_4}\right)\left(\frac{1}{1+r_5}\right)\\
&\quad\cdot\left(\frac{1}{1+r_6}\right)\left(\frac{1}{1+r_7}\right)\left(\frac{1}{1+r_8}\right)\\
w_3 &= \left(\frac{r_3}{1+r_3}\right)\left(\frac{1}{1+r_4}\right)\left(\frac{1}{1+r_5}\right)\\
&\quad\cdot\left(\frac{1}{1+r_6}\right)\left(\frac{1}{1+r_7}\right)\left(\frac{1}{1+r_8}\right)\\
w_4 &= \left(\frac{r_4}{1+r_4}\right)\left(\frac{1}{1+r_5}\right)\left(\frac{1}{1+r_6}\right)\\
&\quad\cdot\left(\frac{1}{1+r_7}\right)\left(\frac{1}{1+r_8}\right)\\
w_5 &= \left(\frac{r_5}{1+r_5}\right)\left(\frac{1}{1+r_6}\right)\left(\frac{1}{1+r_7}\right)\left(\frac{1}{1+r_8}\right)\\
w_6 &= \left(\frac{r_6}{1+r_6}\right)\left(\frac{1}{1+r_7}\right)\left(\frac{1}{1+r_8}\right)\\
w_7 &= \left(\frac{r_7}{1+r_7}\right)\left(\frac{1}{1+r_8}\right)\\
w_8 &= \left(\frac{r_8}{1+r_8}\right).
\end{aligned}
$$

[1] $R_{7,1}$ and $R_{8,1}$ in Table II have been "trimmed" to compensate for the error in $R_{7,2}$.

TABLE III
(3 + 11)-BIT SEGMENTED VOLTAGE-MODE DAC. $R_{k,1}$ AND $R_{k,2}$ DENOTE THE RESISTORS IN FIG. 2 AND r_k, $k = 1, \cdots, 8$ ARE THE CORRESPONDING RESISTANCE RATIOS DEFINED BY (1). w_k IS THE WEIGHT ASSOCIATED WITH BIT k AS DETERMINED FROM MEASUREMENTS OF V_{OUT}; $\hat{r}_k$ IS THE CORRESPONDING ESTIMATE OF r_k

k	$R_{k,1}(\Omega)$	$R_{k,2}(\Omega)$	r_k	w_k	$\hat{r}_k$
1	20000	20012	0.99940036	0.00006108	0.99940036
2	10000	20011	0.99960017	0.00012216	0.99960017
3	10000	20010	0.99967513	0.00024428	0.99967513
4	10000	20009	0.99971886	0.00048851	0.99971886
5	10000	20008	0.99975477	0.00097692	0.99975477
6	10000	20007	0.99978873	0.00195366	0.99978873
7	10000	20006	0.99982221	0.00390704	0.99982221
8	10000	20005	0.99985557	0.00781364	0.99985557
9	10000	20004	0.99988890	0.01562667	0.99988890
10	10000	20005	0.99982226	0.03124951	0.99982226
11	10000	20004	0.99988057	0.06249712	0.99988057
12	10000	20001	1.00002013	0.12500422	1.00002013
13	0	20002	0.49998004	0.12499797	0.49998004
14	0	20003	0.33330780	0.12499172	0.33330780
15	0	20002	0.24999813	0.12499797	0.24999813
16	0	20001	0.20000880	0.12500422	0.20000880
17	0	20002	0.16666445	0.12499797	0.16666445
18	0	20001	0.14286266	0.12500422	0.14286266

A. Implications for Trimming

In an ideal binary-weighted DAC, we require that $w_{k+1} = 2w_k$ for all k. This can be achieved by ensuring that

$$r_{k+1} = \frac{2r_k}{1+r_k}. \tag{4}$$

In a nominal R-$2R$ ladder, $r_k = 1$ for all k. If, due to production variations, $r_k \neq 1$ for some k, the constraint (4) can still be met, and the linearity error minimized, by adjusting r_j for $j = k+1, k+2, \cdots, N$. Each r_j can be set by trimming $R_{j,1}$ and/or $R_{j,2}$. Note that, during the trimming process, it may be necessary to move resistors away from their nominal values.

If the ladder is trimmed from the right end by adjusting the ratios r_1, r_2, r_3, etc., in turn, it is clear that the absolute value of each weight w_k will be affected by an adjustment of r_j for all $j > k$. However, the ratio of any pair of weights ($w_k/w_i\ i < k$) is unaffected by trimming further up the ladder. Therefore, the trimming algorithm should try to fix the ratios of weights with the *current* value of the LSB rather than its *final* value.

B. Implications for Design

From the designer's perspective, the goal is to ensure that $w_{k+1} = 2w_k$ in order to produce a binary-weighted DAC. Clearly, this objective can be achieved with any number of different sets of ratios r_k. In particular, it is not necessary to choose $r_k = 1$, nor is it necessary to define the absolute value of w_1.

Consider the case of an ideal R-$2R$ ladder where we want $r_k = 1$ for all k. When switch resistances are taken into ac-

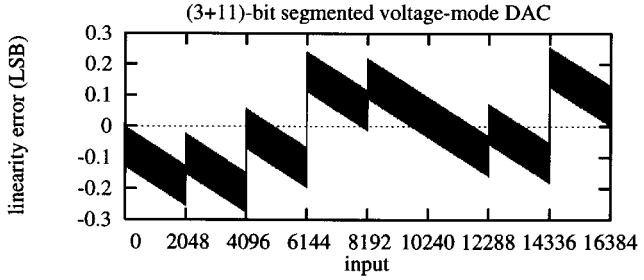

Fig. 7. Endpoint-corrected linearity error associated with the (3 +11)-bit segmented voltage-mode DAC in Table IV. The linearity error is given by $(16383/V_{\rm OUT}(16383))V_{\rm OUT}(U) - U$, $U = 0, 1, 2, \cdots, 16383$.

count, a dummy switch can be inserted in series with $R_{1,1}$ to compensate for the switch in series with $R_{1,2}$ and guarantee $r_1 = 1$. Alternatively, an appropriate choice of "mismatch" at the right end of the ladder when sizing the switches in series with $R_{1,1}$ and $R_{1,2}$ can yield ratios $r_k \neq 1$ but still guarantee binary weighting. The total switch area resulting from this strategy may be less than by choosing $r_k \equiv 1$ for all k.

C. Implications for Production Monitoring

Finally, from the production monitoring viewpoint, we note that although w_k, $k = 1, 2, \cdots, N$, can in principle be determined with just N measurements using (3), a better estimate of the w_k's may be obtained in the case of limited measurement resolution by solving a larger subset of the overdetermined system of equations

$$\begin{bmatrix} V_{\rm OUT}(0) \\ V_{\rm OUT}(1) \\ V_{\rm OUT}(2) \\ V_{\rm OUT}(3) \\ \vdots \\ V_{\rm OUT}(2^N-2) \\ V_{\rm OUT}(2^N-1) \end{bmatrix} = \begin{bmatrix} 0 & 0 & \cdots & 0 & 0 \\ 1 & 0 & \cdots & 0 & 0 \\ 0 & 1 & \cdots & 0 & 0 \\ 1 & 1 & \cdots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 1 & \cdots & 1 & 1 \\ 1 & 1 & \cdots & 1 & 1 \end{bmatrix} \begin{bmatrix} w_1 \\ w_2 \\ w_3 \\ \vdots \\ w_{N-1} \\ w_N \end{bmatrix} V_{\rm IN}.$$

V. Voltage-Mode Operation: Segmented Architecture

In an R-$2R$ ladder, it is necessary to have tight matching between each bit and the sum of all lesser bits in order to ensure monotonic operation [13]. Segmented architectures allow this requirement to be relaxed and permit the construction of high-resolution converters.

An $(M + N)$-bit segmented design provides a coarse/fine structure. The most significant M bits define 2^M segments which are further subdivided by an N-bit R-$2R$ ladder. Provided that the N-bit ladder is monotonic and that its full-scale output is less than that of the next segment, monotonicity is guaranteed. This is called the next-segment approach.

A. Operation of the Voltage-Mode Segmented $(M + N)$-Bit DAC

A commonly-used next-segment DAC architecture is shown in Fig. 5. The coarse DAC consists of $2^M - 1$ identical resistors ($R_{N+1,2}, \cdots, R_{N+2^M-1,2}$) which are selected by a thermometer code. The fine DAC is an N-bit R-$2R$ ladder.

TABLE IV
(3 + 11)-Bit Segmented Voltage-Mode DAC. $R_{k,1}$ and $R_{k,2}$ Denote the Resistors in Fig. 2 and r_k, $k = 1, \cdots, 8$ Are the Corresponding Ratios Defined by (1). w_k Is the Weight Associated with Bit k as Determined From Measurements of $V_{\rm OUT}$; $\hat{r}_k$ Is the Corresponding Estimate of r_k

k	$R_{k,1}(\Omega)$	$R_{k,2}(\Omega)$	r_k	w_k	$\hat{r}_k$
1	20000	24096	0.83001328	0.00005733	0.83001328
2	10000	22048	0.94924177	0.00011998	0.94924177
3	10000	21024	0.98634585	0.00024302	0.98634585
4	10000	20512	0.99647721	0.00048768	0.99647721
5	10000	20256	0.99910660	0.00097621	0.99910660
6	10000	20128	0.99977513	0.00195284	0.99977513
7	10000	20064	0.99994360	0.00390591	0.99994360
8	10000	20032	0.99998588	0.00781193	0.99998588
9	10000	20016	0.99999647	0.01562391	0.99999647
10	10000	20008	0.99999912	0.03124784	0.99999912
11	10000	20004	0.99999978	0.06249570	0.99999978
12	10000	20001	1.00004994	0.12499766	1.00004994
13	0	20000	0.50003749	0.12500391	0.50003749
14	0	19999	0.33336666	0.12501016	0.33336666
15	0	20001	0.24999375	0.12499766	0.24999375
16	0	20002	0.19998600	0.12499141	0.19998600
17	0	20001	0.16666528	0.12499766	0.16666528
18	0	19999	0.14287041	0.12501016	0.14287041

The least significant bits are applied directly to the switches in the R-$2R$ ladder. Bit b_k, $k = 1, 2, \cdots, N$ of the input word causes node k' to be connected to ground or to $V_{\rm IN}$ if $b_k = 0$ or 1, respectively. The most significant M bits are decoded to produce $a_1, a_2, \cdots, a_{2^M-1}$ which select the segments. Bit a_k, $k = 1, 2, \cdots, 2^M - 1$ causes node $N + k'$ to be connected to ground or to $V_{\rm IN}$ if $a_k = 0$ or 1, respectively.

Since this network is linear, the superposition theorem [12] applies, and the voltage at the output node $N + 2^M - 1$ may be determined by summing the contributions from each of the inputs $V_{k'}$ with all other sources zeroed. Thus

$$V_{\rm OUT} = \sum_{k=1}^{N+2^M-1} E_{N+2^M-1,\,k}$$

where $E_{N+2^M-1,\,k}$ is the contribution to the voltage at node $N + 2^M - 1$ due to voltage $V_{k'}$ applied at node k'.

Consider first the contribution due to $V_{N+2^M-1'}$ with all other sources zeroed. In this case, node $N + 2^M - 1$ is connected to $V_{N+2^M-1'}$ via $R_{N+2^M-1,\,2}$ and to ground via the equivalent resistance $R_{N+2^M-1,\,3}$.

By voltage division

$$E_{N+2-1,\,N+2^M-1} = \frac{R_{N+2^M-1,3}}{R_{N+2^M-1,2} + R_{N+2^M-1,3}} V_{N+2^M-1'} = \frac{r_{N+2^M-1}}{1 + r_{N+2^M-1}} V_{N+2^M-1'}$$

where r_{N+2^M-1} is as defined in (1).

The contributions to $V_{\rm OUT}$ due to the other inputs may be calculated by determining the Thévenin equivalent to the right of each node in turn, as in the case of the voltage-mode ladder without segmentation. The contribution due to the input $V_{k'}$ at node k' is given by

$$E_{N+2^M-1,\,k} = w_k V_{k'}$$

where w_k is defined by

$$w_k = \begin{cases} \dfrac{r_{N+2^M-1}}{1+r_{N+2^M-1}}, & \text{if } k = N+2^M-1 \\ \left(\dfrac{r_k}{1+r_k}\right)\displaystyle\prod_{j=k+1}^{N+2^M-1}\left(\dfrac{1}{1+r_j}\right), & \text{if } k < N+2^M-1. \end{cases} \tag{5}$$

The total output voltage is given by (5a) at the bottom of this page.

B. Operation of the Ideal Segmented DAC

In the N-bit DAC, $R_{k,\,3} = R_{k,\,2} = 2R$ for $k = 1, 2, \cdots, N$, giving $r_k = 1$ for $k = 1, 2, \cdots, N$.

The output resistance of the ladder is increased to $2R$ by setting $R_{N+1,\,2} = R$. The segment resistors have nominal value $2R$ and are interconnected by short-circuits. Hence, $R_{k,\,2} = 2R$ for $k = N+1, N+2, \cdots, N+2^M-1$ and $R_{k,\,1} = 0$ for $k = N+2, N+3, \cdots, N+2^M-1$. This gives $R_{N+k,\,3} = 2R/k$ for $k = 1, 2, \cdots, 2^M-1$. Hence

$$r_{N+k} = \frac{1}{k}, \qquad k = 1, 2, \cdots, 2^M-1.$$

Substituting for each r_k yields

$$\begin{bmatrix} w_1 \\ w_2 \\ \vdots \\ w_{N-1} \\ w_N \\ \hline w_{N+1} \\ w_{N+2} \\ \vdots \\ w_{N+2^M-1} \end{bmatrix} = \begin{bmatrix} \dfrac{1}{2^{M+N}} \\ \dfrac{1}{2^{M+N-1}} \\ \vdots \\ \dfrac{1}{2^{M+2}} \\ \dfrac{1}{2^{M+1}} \\ \hline \dfrac{1}{2^M} \\ \dfrac{1}{2^M} \\ \vdots \\ \dfrac{1}{2^M} \end{bmatrix}.$$

Therefore

$$V_{\rm OUT} = \left(\sum_{k=1}^{N}\frac{b_k}{2^{N-k+1}} + \sum_{k=1}^{2^M-1} a_k\right)\frac{V_{\rm IN}}{2^M}$$

where $b_N b_{N-1} \cdots b_2 b_1$ are the LSB's of the input word U and the upper M bits are decoded to give the a_ks.

C. Diagnosability of the Segmented Voltage-Mode DAC

Is it possible to determine the ratios r_k, $k = 1, 2, \cdots, N+2^M-1$ in a segmented voltage-mode DAC simply by measuring the output voltage $V_{\rm OUT}$?

Let $V_{\rm OUT}(U)$ be the measured output corresponding to input word U, as before. In this case, the weights w_k may be determined by making just $N+M$ (out of a possible 2^{N+M}) measurements of $V_{\rm OUT}$. In particular, $N+M$ measurements of $V_{\rm OUT}$ with $U = 1, 2, 4, 8, \cdots, 2^N, \cdots, 2^{N+M}$, yield (6) at the bottom of the next page.

$$V_{\rm OUT} = \sum_{k=1}^{N+2^M-1} E_{N,\,k} = \left(\sum_{k=1}^{N} b_k w_k + \sum_{k=1}^{2^M-1} a_k w_{N+k}\right) V_{\rm IN}$$

$$= \begin{bmatrix} b_1 & b_2 & \cdots & b_k & \cdots & b_{N-1} & b_N \end{bmatrix} \begin{bmatrix} a_1 & a_2 & \cdots & a_{2^M-1} \end{bmatrix} \begin{bmatrix} w_1 \\ w_2 \\ \vdots \\ w_k \\ \vdots \\ w_{N-1} \\ w_N \\ \hline w_{N+1} \\ w_{N+2} \\ \vdots \\ w_{N+2^M-1} \end{bmatrix} V_{\rm IN}. \tag{5a}$$

Assuming that V_{IN} is known, (6) may be rewritten to give the weights w_k explicitly in terms of the $N+M$ measured outputs shown at the bottom of this page.

From these weights w_k, the ratios r_k may be estimated by setting

$$\hat{r}_{N+2^M-1} = \frac{w_{N+2^M-1}}{1 - w_{N+2^M-1}}$$

and evaluating

$$\hat{r}_k = \frac{\rho_k}{1-\rho_k}$$

for $k = N + 2^M - 1$ to 1 in turn, where

$$\rho_k = w_k \prod_{j=k+1}^{N+2^M-1} (1+\hat{r}_j).$$

As before, $\hat{r}_k$ provides an estimate of r_k.

D. Example

Consider the 14-bit segmented voltage-mode DAC whose resistor values are given in Table III. The DAC consists of an 11-bit R-$2R$ ladder and three decoded bits driving seven segment resistors. This linear network was simulated using a reference input $V_{\text{IN}} = 5$ V. The endpoint-corrected linearity error is shown in Fig. 6. Note that the estimates $\hat{r}_k$ of the resistor ratios

$$\left[\begin{array}{c} V_{\text{OUT}}(1) \\ V_{\text{OUT}}(2) \\ V_{\text{OUT}}(4) \\ \vdots \\ V_{\text{OUT}}(2^{N-2}) \\ V_{\text{OUT}}(2^{N-1}) \\ \hline V_{\text{OUT}}(2^N) \\ V_{\text{OUT}}(2^{N+1}) \\ \vdots \\ V_{\text{OUT}}(2^{N+M-1}) \end{array}\right] = \left[\begin{array}{cccccc|ccc} 1 & 0 & 0 & \cdots & 0 & 0 & 0 & 0 & \cdots & 0 \\ 0 & 1 & 0 & \cdots & 0 & 0 & 0 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 & 0 & 0 & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 1 & 0 & 0 & 0 & \cdots & 0 \\ 0 & 0 & 0 & \cdots & 0 & 1 & 0 & 0 & \cdots & 0 \\ \hline 0 & 0 & 0 & \cdots & 0 & 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 0 & \cdots & 0 & 0 & 1 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 0 & 0 & 1 & 1 & \cdots & 1 \end{array}\right] \left[\begin{array}{c} w_1 \\ w_2 \\ w_3 \\ \vdots \\ w_{N-1} \\ w_N \\ \hline w_{N+1} \\ w_{N+2} \\ \vdots \\ w_{N+2^M-1} \end{array}\right] V_{\text{IN}}$$

$$= \left[\begin{array}{c} w_1 \\ w_2 \\ w_3 \\ \vdots \\ w_{N-1} \\ w_N \\ \hline w_{N+1} \\ w_{N+1} + w_{N+2} \\ \vdots \\ w_{N+1} + w_{N+2} + \cdots + w_{N+2^M-1} \end{array}\right] V_{\text{IN}}. \tag{6}$$

$$\left[\begin{array}{c} w_1 \\ w_2 \\ w_3 \\ \vdots \\ w_{N-1} \\ w_N \\ \hline w_{N+1} \\ w_{N+2} \\ \vdots \\ w_{N+2^M-1} \end{array}\right] = \frac{1}{V_{\text{IN}}} \left[\begin{array}{c} V_{\text{OUT}}(1) \\ V_{\text{OUT}}(2) \\ V_{\text{OUT}}(4) \\ \vdots \\ V_{\text{OUT}}(2^{N-2}) \\ V_{\text{OUT}}(2^{N-1}) \\ \hline V_{\text{OUT}}(2^N) \\ V_{\text{OUT}}(2^{N+1}) - V_{\text{OUT}}(2^N) \\ \vdots \\ V_{\text{OUT}}(2^{N+M-1}) - \cdots - V_{\text{OUT}}(2^{N+1}) - V_{\text{OUT}}(2^N) \end{array}\right].$$

at the node of the network extracted from the simulated data are correct to eight significant figures.

Note also that mismatch errors at the right end of the ladder are less significant than those at the left end or in the segment resistors.

Fig. 7, shows the linearity error of the $(3+11)$-bit DAC summarized in Table IV.

In this case, gross errors (of up to 20%) have been introduced into the resistors at the LSB end of the ladder in order to exaggerate the relative effects of mismatches at different bit positions. Here, the large errors in the LSB resistors (and the corresponding weights) contribute proportionately less to the overall error than do the much smaller errors in the segment resistors.

Qualitatively, this is because the full-scale error due to a fractional error in an LSB is smaller than for the same fractional error in a more significant bit. Furthermore, errors in the LSB resistor ratios r_k are divided down by a factor of approximately four at each node up the ladder so that the ratios for the MSB's are relatively insensitive to errors further to the right along the ladder.

In terms of trimming a segmented voltage-mode DAC, more effort should be devoted to matching the segment resistors and the MSB's of the ladder than the LSB's since the former are more likely to determine the final accuracy than the latter.

VI. Concluding Remarks

In this work, we have developed a model of the linear R-$2R$ ladder DAC which is parameterized by the ratios of effective resistances at the nodes of the ladder. This formulation provides insight into the operation of the ladder. It explains why the ladder is insensitive to the absolute values of the constituent resistors, and suggests appropriate trimming, design, and test stategies. We have not considered the case of code-dependent resistors in the ladder [14]; this is the focus of on-going work.

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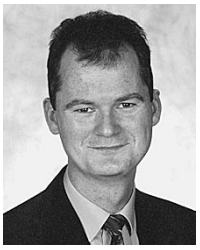

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