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Development of Inversion-Mode and Junctionless Indium-Gallium-Arsenide MOSFETs

Vladimir Djara

Thesis Submitted for the degree of Doctor of Philosophy

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December 2013
Declaration

I declare that the entire content of this thesis is my own work, unless otherwise stated, and that this thesis has not been submitted for another degree, either at University College Cork or elsewhere.

Vladimir Djara
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5.12 DC $I_d-V_g$ characteristics measured over a range of temperature ($T$) going from 4 K to 292 K on a 10-µm-channel-length device at a drain-to-source voltage ($V_{ds}$) of 50 mV. A zero-temperature coefficient (ZTC) point is observed. Inset: Source and drain series resistance ($R_{SD}$) as a function of temperature ($T$).

5.13 Effective mobility ($\mu_{\text{eff}}$) vs inversion charge ($N_{\text{inv}}$) extracted using ICP at a frequency ($f$) of 1 MHz and a duty cycle ($D$) ranging from 50% to 5% and multi-frequency ICP. Excellent agreement is obtained between the $\mu_{\text{eff}}$ extracted from Split C-V ($f = 1 \text{ MHz}, T = 292 \text{ K}$) and that extracted by ICP ($f = 1 \text{ MHz}, D = 50\%$). The experimental $\mu_{\text{eff}}$ values (symbols) were fitted with the empirical model reported in [37].

5.14 Effective mobility ($\mu_{\text{eff}}$) vs inversion charge ($N_{\text{inv}}$) extracted using split C-V at a frequency ($f$) of 1 MHz for a range of temperature ($T$) going ranging from 292 K to 35 K. The experimental $\mu_{eff}$ values (symbols) were fitted with the empirical model reported in [37].

5.15 Scattering components obtained from the fitting of the effective mobility ($\mu_{\text{eff}}$) vs inversion charge ($N_{\text{inv}}$) curves extracted from ICP ($f = 1 \text{ MHz}, D = 50\%$) and multi-frequency (M-F) ICP. The phonon scattering mobility, the surface roughness scattering mobility, the Coulomb scattering mobility and the total mobility are noted $\mu_{\text{ph}}$, $\mu_{\text{sr}}$, $\mu_{\text{C}}$, and $\mu_{\text{tot}}$, respectively. While the same $\mu_{\text{ph}}$ and $\mu_{\text{sr}}$ were used to fit both curves, $\mu_{\text{C}}$ was adjusted to account for the removal of the border trap contribution to the total pumped-charged density ($N_{CP}$).
5.16 AFM topography data of (a) the unpassivated p-In$_{0.53}$Ga$_{0.47}$As surface and (b) the p-In$_{0.53}$Ga$_{0.47}$As surface after 10% (NH$_4$)$_2$S passivation for 20 min, 10 nm Al$_2$O$_3$ deposition by ALD, implant activation at 600°C for 15 s and finally Al$_2$O$_3$ etch using dilute HF. Both measurements were taken over a 1 µm × 1 µm area. The AFM measurements were performed by M. Burke (Tyndall).

6.1 In$_{0.53}$Ga$_{0.47}$As channel thickness ($t_{\text{InGaAs}}$) vs In$_{0.53}$Ga$_{0.47}$As channel doping ($N_d$). The calculated maximum depletion width ($W_{d\text{max}}$) yields the boundary between the fully depleted and non-fully depleted device structure. The 20 nm $t_{\text{InGaAs}}$ limit, where severe effective electron mobility ($\mu_{eff}$) degradation is reported [10], and the set of $t_{\text{InGaAs}}$ (32, 24, 20, 16 and 12 nm) vs $N_d$ ($9 \times 10^{17}$/cm$^3$) parameters corresponding to the fabricated devices are also indicated.

6.2 Quasi-static capacitance-voltage (C-V) characteristics obtained for Pd/Al$_2$O$_3$/n-In$_{0.53}$Ga$_{0.47}$As/p-In$_{0.52}$Al$_{0.48}$As/p-InP structures using a self-consistent Poisson-Schrödinger solver. The structures featured In$_{0.53}$Ga$_{0.47}$As channel thicknesses ($t_{\text{InGaAs}}$) of 32, 24 and 16 nm and an In$_{0.53}$Ga$_{0.47}$As channel doping ($N_d$) of $9 \times 10^{17}$/cm$^3$. A flat-band capacitance ($C_{fb}$) of 0.52 µF/cm$^2$ and flat-band voltage ($V_{fb}$) of 0.2 V were obtained. It is noted that the dotted line inversion response of the quasi-static C-V curves will not be typically observed experimentally in a multi-frequency C-V.

6.3 Conduction band diagrams of Pd/Al$_2$O$_3$/n-In$_{0.53}$Ga$_{0.47}$As/p-In$_{0.52}$Al$_{0.48}$As/p-InP structures obtained from self-consistent Poisson-Schrödinger calculations. Diagrams of a 32-nm-thick In$_{0.53}$Ga$_{0.47}$As channel device showing (a) the flat-band and (b) the fully depleted conditions. The Fermi level needs to move 0.07 eV above the conduction band edge ($E_C$) to reach flat-band and 0.54 eV below $E_C$ to reach full depletion. Diagrams of a 24-nm-thick In$_{0.53}$Ga$_{0.47}$As channel device showing (c) the flat-band and (d) the fully depleted conditions. The Fermi level needs to move 0.07 eV above $E_C$ to reach flat-band and 0.31 eV below $E_C$ to reach full depletion.

6.4 (a) Energy range required to move from flat-band to full depletion as a function of In$_{0.53}$Ga$_{0.47}$As channel thickness ($t_{\text{InGaAs}}$). The values were obtained from self-consistent Poisson-Schrödinger calculations. (b) Comparison of the $D_{it}$ values reported for Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOS structures [15-26].

6.5 Diagram and cross-section transmission electron microscopy (TEM) image of the MOVPE grown n-In$_{0.53}$Ga$_{0.47}$As (32 nm)/p-In$_{0.52}$Al$_{0.48}$As (500 nm)/p$^+$-InP wafer structure used for the digital etch (DE) process characterization and for the device fabrication.
6.6 In$_{0.53}$Ga$_{0.47}$As channel thinning using a $\text{H}_2\text{O}_2$/HCl digital etch (DE) process [27]. Excellent agreement between spectroscopic ellipsometry (SE) and TEM (Figure 6.5) measurements was obtained prior to DE. An etch rate of 0.8 nm/cycle was extracted from the linear fit. The $R^2 = 0.999$ of the linear fit confirms the excellent control of the In$_{0.53}$Ga$_{0.47}$As etch rate. ............................... 126

6.7 Atomic force microscopy (AFM) topography data of n-In$_{0.53}$Ga$_{0.47}$As (a) before digital etch (DE) and after (b) a 10-cycle, (c) a 15-cycle and (d) a 20-cycle DE. The measurements were taken over $1 \mu m \times 1 \mu m$ scan areas. The AFM measurements were performed by M. Burke (Tyndall). ........................................ 127

6.8 Fabrication process flow of planar Gate-enclosed Junctionless In$_{0.53}$Ga$_{0.47}$As MOSFETs including (a) 10% (NH$_4$)$_2$S for 30 min passivation [16, 21] prior to ALD $\text{Al}_2\text{O}_3$ (8.5 nm), (b) Pd (200 nm) gate lift-off, (c) $\text{Al}_2\text{O}_3$ etch in dilute HF for S/D contact opening and (d) 10% NH$_4$OH for 20 sec surface treatment followed by Au (14 nm)/Ge (14 nm)/Au (14 nm)/Ni (11 nm)/Au (200 nm) [29] S/D contact lift-off. (e) Cross-section diagram of a gate-enclosed junctionless MOSFET architecture. The drain radius ($r_d$), gate inner radius ($r_{in}^g$), gate outer radius ($r_{out}^g$) and source radius ($r_s$) are 35, 45, 105 and 135 $\mu m$, respectively. ......................... 129

6.9 $I_d$-$V_{ds}$ output characteristics of a planar gate-enclosed junctionless In$_{0.53}$Ga$_{0.47}$As MOSFET featuring a 24-nm-thick In$_{0.53}$Ga$_{0.47}$As channel. A $(W/L)_{eff}$ of 7.41 was used for the $W/L$ normalization of $I_d$. ................................................ 130

6.10 $I_d$-$V_g$ transfer characteristics measured at $V_{ds} = 50$ mV on planar gate-enclosed junctionless In$_{0.53}$Ga$_{0.47}$As MOSFETs with $t_{\text{InGaAs}} = 32, 24, 20, 16$ and 12 nm. A $(W/L)_{eff}$ of 7.41 was used for the $W/L$ normalization of $I_d$. ................................................ 131

6.11 (a) $I_{ON}/I_{OFF}$ vs $t_{\text{InGaAs}}$. The best $I_{ON}/I_{OFF}$ value of $1.5 \times 10^5$ was obtained with $t_{\text{InGaAs}} = 20$ nm. For $t_{\text{InGaAs}} > 20$ nm, $I_{ON}/I_{OFF}$ is degraded due to an increase in $I_{OFF}$. For $t_{\text{InGaAs}} < 20$ nm, the $I_{ON}/I_{OFF}$ is degraded due to a decrease in $I_{ON}$. (b) Subthreshold swing (SS) vs $t_{\text{InGaAs}}$. SS scaling with $t_{\text{InGaAs}}$ observed for $t_{\text{InGaAs}}$ reducing from 24 nm to 16 nm. The lowest SS (115 mV/dec.) was obtained with $t_{\text{InGaAs}} = 16$ nm. ......................... 132

6.12 $I$-$V$ characteristic of a n-In$_{0.53}$Ga$_{0.47}$As/p-In$_{0.52}$Al$_{0.48}$As heterojunction diode fabricated on the wafer structure shown in Figure 6.5. More than 7 orders of magnitude between the forward and reverse current is observed, indicating excellent junction isolation. ....................................... 133
6.13 (a) $C_{gc}$-$V_g$ characteristics measured at a frequency of 1 MHz on planar gate-enclosed junctionless In$_{0.53}$Ga$_{0.47}$As MOSFETs with $t_{InGaAs} = 32$ nm. Inset: Calculated minimum capacitance ($C_{min}$) vs In$_{0.53}$Ga$_{0.47}$As doping ($N_d$). A measured $C_{min}$ of $\sim 0.2 \mu F/cm^2$ at $V_g = -2$ V suggests a $N_d < 1.1 \times 10^{18}/cm^3$. (b) Fermi level position at the Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As interface in an ideal and in the fabricated devices. In the fabricated device, the Fermi level is pinned above $E_F - E_C = -0.54$ eV [Figure 6.3(b)], preventing the full depletion of the 32-nm-thick In$_{0.53}$Ga$_{0.47}$As channel.

6.14 (a) Multi-frequency $C_{gc}$-$V_g$ characteristic of a 24-nm-thick In$_{0.53}$Ga$_{0.47}$As channel device showing low frequency dispersion near accumulation. The low $C_{min}$ of $\sim 40$ nF/cm$^2$ suggests full depletion at $V_g < -1$ V. Inset: Evolution of the conductance peak normalized to angular frequency ($G/\omega$). (b) Comparison of the conductance and high-low methods for the extraction of the density of interface traps ($D_{it}$). Inset: Fermi level position at the Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As interface in an ideal and in the fabricated devices. In the fabricated device, the Fermi level reaches $E_F$-$E_C = -0.3$ eV at $V_g = -1$ V, demonstrating the full depletion of the 24-nm-thick In$_{0.53}$Ga$_{0.47}$As channel.

6.15 (a) 100-kHz $C_{gc}$-$V_g$ characteristics measured on 24, 20 and 16-nm-thick In$_{0.53}$Ga$_{0.47}$As-channel devices. The theoretical flat-band capacitance ($C_{fb}$) obtained from calculations is reported on the curves to extract a flat-band voltage ($V_{fb}$) of 0 V. (b) Plot of the surface carrier density ($N_s$) at flat-band vs $t_{InGaAs}$. The total charge density ($N_{tot}$) was obtained by integrating $C_{gc}$. $N_s$ was obtained by correcting $N_{tot}$ for the density of interface trap ($D_{it}$) integrated across the energy range of operation of the corresponding device. The $N_s$ at flat-band vs $t_{InGaAs}$ curves were calculated for ideal devices with $N_d = 1.1 \times 10^{18}$, $9 \times 10^{17}$ and $7 \times 10^{17}/cm^3$. The x-intercepts obtained by extrapolation of the curves yielded the total dark space thickness values (accounting for the top and bottom interfaces). The case of a SiO$_2$/Si-on-isulator (SOI) structure with a channel $N_d$ of $9 \times 10^{17}/cm^3$ is shown for comparison.
6.16 (a) Circuit equivalent model of the device. $R_{c,D}$ and $R_{c,S}$ are the resistances of the contacts to the drain and source areas, respectively. $R_D$, $R_S$, $R_{D-to-G}$ and $R_{G-to-S}$ are the resistances associated with the sheet resistance of the drain, source, drain-to-source and gate-to-source areas, respectively. $R_{ch}$ is the resistance of the channel. (b) Simplified circuit equivalent model assuming a specific contact resistance ($\rho_c$) of $5 \times 10^{-6} \, \Omega \cdot \text{cm}^2$, a transfer length ($L_t$) of 0.5 $\mu$m and a mobility in the $n$-In$_{0.53}$Ga$_{0.47}$As ($N_d = 9 \times 10^{17} / \text{cm}^3$) layer of 2000 $\text{cm}^2/V \cdot \text{s}$. (c) Comparison of the series resistance ($R_{\text{series}}$) vs $I_{\text{InGaAs}}$ extracted from the $I_d$-$V_g$ curves shown in Figure 6.10 and calculated from the simplified equivalent circuit model shown in (b) with estimated and/or extracted surface carrier density [noted $n.t$ in Equation 6.4] and carrier mobility ($\mu$) parameters.

6.17 Effective electron mobility ($\mu_{\text{eff}}$) vs $N_s$. Values of $\mu_{\text{eff}}$ at flat-band of 2130, 1975 and 310 $\text{cm}^2/V \cdot \text{s}$ were obtained for planar gate-enclosed junctionless In$_{0.53}$Ga$_{0.47}$As MOSFETs featuring $t_{\text{InGaAs}}$ of 24, 20 and 16 nm, respectively. The abrupt drop in $\mu_{\text{eff}}$ observed for $t_{\text{InGaAs}} = 16$ nm is consistent with [10]. The $\mu_{\text{eff}}$ of an inversion-mode Pd/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOSFET with implanted S/D measured at a temperature ($T$) of 35 K (see [5]) is shown for comparison. The $\mu_{\text{eff}}$ data of the junctionless devices are corrected for $R_{\text{series}}$ and $D_{it}$. The $\mu_{\text{eff}}$ data of the inversion-mode device is only corrected for $R_{\text{series}}$ but the reduced $T$ acts as a $D_{it}$ correction [35].
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<td>3-D</td>
<td>3-dimension</td>
</tr>
<tr>
<td>ac</td>
<td>alternative current</td>
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<tr>
<td>AFM</td>
<td>atomic force microscopy</td>
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<td>ALD</td>
<td>atomic layer deposition</td>
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<td>ANOVA</td>
<td>analysis of variance</td>
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<tr>
<td>C-V</td>
<td>capacitance-voltage</td>
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<tr>
<td>CMOS</td>
<td>complementary metal-oxide-semiconductor</td>
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<td>CP</td>
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<td>DIBL</td>
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<td>DOE</td>
<td>design of experiment</td>
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<tr>
<td>EOT</td>
<td>equivalent oxide thickness</td>
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<tr>
<td>FDSOI</td>
<td>fully-depleted silicon on insulator</td>
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<tr>
<td>FET</td>
<td>field effect transistor</td>
</tr>
<tr>
<td>FGA</td>
<td>forming gas (H&lt;sub&gt;2&lt;/sub&gt;/N&lt;sub&gt;2&lt;/sub&gt;) anneal</td>
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<tr>
<td>G-V</td>
<td>conductance-voltage</td>
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<tr>
<td>GAA</td>
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<td>GGO</td>
<td>gallium gadolinium oxide</td>
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<td>metal-organic vapor phase epitaxy</td>
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<tr>
<td>SP</td>
<td>standard power</td>
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<tr>
<td>SRH</td>
<td>Shockley-Read-Hall</td>
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<td>SRIM</td>
<td>stopping and range of ions in matter</td>
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<td>subthreshold swing</td>
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<td>transmission electron microscopy</td>
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<tr>
<td>TLM</td>
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<td>TMA</td>
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<td>zero-temperature coefficient</td>
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<td>total charge density ($N_{CV}$) obtained from split C-V</td>
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<td>channel resistance</td>
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<td>resistance associated to the sheet resistance of the drain</td>
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<td>gate outer radius</td>
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<td>resistance of a ring</td>
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<td>resistance associated to the sheet resistance of the source</td>
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<td>source radius</td>
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<td>source and drain series resistance</td>
<td>$[\Omega], [\Omega/\text{m}]$</td>
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<td>$R_{series}$</td>
<td>series resistance</td>
<td>$[\Omega], [\Omega/\text{m}]$</td>
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<td>total resistance</td>
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Abstract

This PhD covers the design, fabrication and characterization of planar inversion-mode and junctionless $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ metal-oxide-semiconductor field-effect transistors (MOSFETs). The objectives of this work were to (1) use the fabricated devices as test vehicles for further studies of the defects present in the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ gate stack through the development of alternative electrical characterization techniques, (2) identify and understand the impact of the MOSFET fabrication process steps on the gate stack defects and (3) explore defect passivation techniques and alternative device architectures to reduce gate stack defects.

An implant activation anneal process was first developed for the formation of the source and drain (S/D) terminals of the inversion-mode device. Test structures based on the transfer length method (TLM) were fabricated and used as part of a Doehlert design of experiment (DOE) to investigate a process window covering annealing temperatures of 625°C to 725°C and annealing times of 15 s to 45 s. The optimized process was 715°C for 32 s, leading to a minimum sheet resistance ($R_{\text{sheet}}$) of $(195.6 \pm 3.4) \Omega/\square$. Non-alloyed Au/Ge/Au/Ni/Au contacts, on the sample annealed at 675°C for 30 s (centre point of the experimental domain), exhibited a low specific contact resistance ($\rho_\text{C}$) of $(7 \times 4.5) \times 10^{-7} \Omega \cdot \text{cm}^2$.

The sample annealed at 675°C for 30 s was further investigated using secondary ion mass spectrometry (SIMS) and cross-sectional transmission electron microscopy (TEM) analyses. SIMS revealed that Si ions did not diffuse with annealing, while TEM showed the formation of characteristic loop defects potentially responsible for the $R_{\text{sheet}}$ and $\rho_\text{C}$ degradation. The impact of the activation anneal on the performance of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ metal-oxide-semiconductor (MOS) gate stack was also studied. Large density of interface traps ($D_{\text{it}}$) values of 2.0, 2.3 and $2.7 \times 10^{13} /\text{cm}^2 \cdot \text{eV}$ were estimated using the conductance method on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ metal-oxide-semiconductor capacitors (MOSCAPs) annealed at 675°C, 700°C and 725°C, respectively. The results indicated that, in the 675°C to 725°C range, an increase of 25°C increased $D_{\text{it}}$ by $\sim 16\%$.

Fabricated inversion-mode $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFETs were used to investigate the impact of a 300°C for 30 min forming gas (H$_2$/N$_2$) anneal (FGA) process on their electrical performance. The FGA was found to effectively remove or passivate the fixed positive oxide charge...
present in the Al$_2$O$_3$ gate dielectric, as a reduction in [oxide charge ($N^+$) from $6.3 \times 10^{12}$ cm$^{-2}$ to $1.3 \times 10^{12}$ cm$^{-2}$ was observed following FGA. The reduction in $N^+$ yielded an increase in ON-state-to-OFF-state current ratio ($I_{\text{ON}}/I_{\text{OFF}}$) of three orders of magnitude due to the removal of an inversion layer, located at the periphery of the devices, responsible for a large OFF-state current ($I_{\text{OFF}}$). Moreover, the FGA significantly improved the source or drain-to-substrate junction isolation, with a reduction of two orders of magnitude in the reverse bias leakage exhibited by the Si-implanted In$_{0.53}$Ga$_{0.47}$As $n^+/p$ junctions, consistent with a passivation of mid-gap defects in the implanted In$_{0.53}$Ga$_{0.47}$As areas. Following FGA, the devices exhibited a subthreshold swing (SS) of 150 mV/decade, an $I_{\text{ON}}/I_{\text{OFF}}$ of $\sim 10^4$ and the transconductance, drive current and peak effective mobility increased by 29% [to 1.1 mS/mm for a gate length ($L$) of 20 µm and a drain-to-source voltage ($V_{ds}$) of 50 mV], 25% [to 19 mV/mm for a $L$ of 20 µm, a $V_{ds}$ of 1.5 V and a gate overdrive of 2 V] and 15% (to 750 cm$^2$/V.s), respectively.

An alternative technique, based on the fitting of the measured full-gate capacitance ($C_g$) vs gate voltage ($V_g$) and corresponding Maserjian Y-function using a self-consistent Poisson-Schrödinger solver, was developed to further investigate gate stack defects. The proposed techniques provides more information than the conventional Terman, high-low and conductance methods. Indeed, this technique can yield (1) the band bending efficiency of the gate stack, (2) the surface-equivalent density of interface and border trap ($D_{\text{trap}}$) vs energy ($E$) profile across the full In$_{0.53}$Ga$_{0.47}$As bandgap and extending in the In$_{0.53}$Ga$_{0.47}$As conduction band and (3) the donor and acceptor nature of the traps. The obtained $D_{\text{trap}}(E)$ featured a peak of donor-like interface traps with a density of $1.5 \times 10^{13}$ cm$^{-2}$.eV located at $\sim 0.36$ eV above the In$_{0.53}$Ga$_{0.47}$As valence band edge ($E_{\text{V}}$) and a high density of donor-like traps increasing towards $E_{\text{V}}$. The analysis also indicated acceptor-like traps located in the In$_{0.53}$Ga$_{0.47}$As conduction band, with a density of $\sim 2.5 \times 10^{13}$ cm$^{-2}$.eV at 0.3 eV above the In$_{0.53}$Ga$_{0.47}$As conduction band edge ($E_{\text{C}}$).

The inversion-charge pumping (ICP) method was investigated for the extraction of the inversion-charge density ($N_{\text{inv}}$) and effective mobility ($\mu_{\text{eff}}$). The initial method was modified to minimize the overestimation of $N_{\text{inv}}$ due to charge trapping mechanisms involving traps located at energy levels lying in the In$_{0.53}$Ga$_{0.47}$As bandgap and In$_{0.53}$Ga$_{0.47}$As conduction band. The method was further developed and a multi-frequency (M-F) ICP approach was proposed to (1) study the traps located at energy levels aligned with the In$_{0.53}$Ga$_{0.47}$As conduction band and (2) effectively separate the charge trapping contribution from $N_{\text{inv}}$. A discrete trap capture cross section ($\sigma$) of $\sim 4.5 \times 10^{-21}$ cm$^2$ was obtained, suggesting a very narrow spatial distribution of border traps located at a distance of $\sim 1.5$ Å from the interface. The analysis also revealed a $\mu_{\text{eff}}$ peaking at $\sim 2850$ cm$^2$/V.s at a low $N_{\text{inv}}$ of $7 \times 10^{11}$ cm$^2$/V.s and rapidly decreasing to $\sim 600$ cm$^2$/V.s at $N_{\text{inv}} = 1 \times 10^{13}$ cm$^2$. Gate-to-channel capacitance ($C_{gc}$) split capacitance-voltage (C-V) measurements performed over a range of temperature going from 292 K to 35 K.
indicated that surface roughness scattering was the main factor limiting the mobility. Atomic force microscopy (AFM) measurements confirmed a large surface roughness of 1.95 ± 0.28 nm on the In$_{0.53}$Ga$_{0.47}$As channel caused by the S/D implant activation anneal process.

In order to circumvent the issue relative to the S/D implant activation, a planar junctionless MOSFET based on an Al$_2$O$_3$/n-In$_{0.53}$Ga$_{0.47}$As/p-In$_{0.52}$Al$_{0.48}$As structure was designed and fabricated. One significant advantage of this device architecture is that the thermal budget is set by the Al$_2$O$_3$ deposition process by atomic layer deposition (ALD). A digital etch (DE) process was used to thin the In$_{0.53}$Ga$_{0.47}$As channel in order to investigate the impact of the In$_{0.53}$Ga$_{0.47}$As channel thickness ($t_{\text{InGaAs}}$) on the device operation and performance. The DE process characterization using spectroscopic ellipsometry (SE) and AFM revealed an etch rate of 0.8 nm/cycle and a root mean square (RMS) surface roughness of 0.28 nm (after 20 cycles), respectively. Values of $D_{il}$ near the conduction band in the low-$10^{12}$ /cm$^2$.eV were also extracted, suggesting that the DE process did not significantly degrade the Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As interface properties. The reduction of $t_{\text{InGaAs}}$ offers the advantage of reducing the energy range swept by the Fermi level when switching the device from ON-state to OFF-state. This was used to maintain the device operation within the upper part of the In$_{0.53}$Ga$_{0.47}$As bandgap, where $D_{il}$ is the lowest, in order to achieve lower SS. Scaling of the SS with $t_{\text{InGaAs}}$ was successfully demonstrated for $t_{\text{InGaAs}}$ going from 24 to 16 nm, with a minimum SS of 113 mV/dec. for $t_{\text{InGaAs}} = 16$ nm. Flat-band $\mu_{\text{ef}}$ values of 2130 and 1975 cm$^2$/V.s were also extracted on devices with $t_{\text{InGaAs}}$ values of 24 and 20 nm, respectively.
Acknowledgments

After five years of excitement, ups and downs and also hard work, it is a great pleasure to look back, remember and thank everyone who helped me along the way.

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xxx
Chapter 1

Introduction

1.1 Extending Moore’s Law

1.1.1 Classic Scaling Rules

In 1965, Gordon Moore predicted that the density of transistors on a chip would double approximately every 18 months [1]. Even though this empirical prediction was only based on data collected over a 6-year period (1959 - 1965), the so-called Moore’s law has held remarkably well over the past 48 years, due to the continuous efforts from the semiconductor industry to push the limits of technology. While it is clear that increasing the density of transistors enables to add more circuit functionalities to a chip of a given size, many other advantages arise from reducing the size of the transistors.

In 1974, Dennard and co-workers first introduced the principles of transistor scaling (Figure 1.1), where the dimensions of a transistor are reduced by a scaling factor $\alpha$ to produce a smaller transistor with enhanced performance [2, 3]. As the dimensions and voltages are reduced by $\alpha$ and the doping is increased by $\alpha$, the electric field configuration in the smaller transistor remains the same as that in the original one. As a result, the switching speed of the smaller transistor increases by $\alpha$ and the power dissipation reduces by $\alpha^2$.

Table 1.1 shows the scaling rules of the main physical parameters. It is worth noting that these scaling rules imply that the threshold voltage ($V_T$) should also reduce by $\alpha$ [1]. This cannot be achieved in a conventional metal-oxide-semiconductor field-effect transistor (MOSFET) due to the impossibility to scale the subthreshold swing (SS) below the 60 mV/dec. limit [at a temperature ($T$) of 292 K], which is known as the Boltzmann limit [5, 6].

The “classic” Dennard’s scaling rules were followed by the semiconductor industry until 2001 (130-nm node) [7], when geometrical scaling was still sufficient to deliver performance improvement. In all subsequent technology nodes (i.e.: < 100 nm), “short-channel effects”, arising from the very small distance separating the source from the drain, involved performance degradation.
1.1. Extending Moore’s Law

Figure 1.1: Schematic illustration of the transistor scaling, where $\alpha$ is the scaling parameter [2].

<table>
<thead>
<tr>
<th>Physical Parameter</th>
<th>Scaling Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Length and Width</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>Wiring Width</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>Gate Oxide Thickness</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>Electric Field in Device</td>
<td>1</td>
</tr>
<tr>
<td>Voltage</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>On-current per Device</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>Doping</td>
<td>$\alpha$</td>
</tr>
<tr>
<td>Area</td>
<td>$1/\alpha^2$</td>
</tr>
<tr>
<td>Capacitance</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>Gate Delay</td>
<td>$1/\alpha$</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>$1/\alpha^2$</td>
</tr>
<tr>
<td>Power Density</td>
<td>1</td>
</tr>
</tbody>
</table>
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Figure 1.2: Cross-section TEM images of strained silicon transistors (90-nm node) including (a) n-MOSFET with tensile strain induced by Si$_3$N$_4$ cap film and (b) p-MOSFET with compressive strain induced by SiGe S/D heteroepitaxial regrowth. The gate lengths of the n-MOSFET and p-MOSFET are 45 nm and 50 nm, respectively [11, 12].

Indeed, as the channel length reduces, drain-induced electrostatic effects lower the energy barrier between the source and the drain, which degrades the $V_T$ roll-off, drain-induced barrier lowering (DIBL) and $SS$ [8]. Various techniques including the use of ultra-thin gate dielectrics, shallow source/drain junctions and high channel doping can be used to reduce short-channel effects and improve devices performance [9]. However, most of these approaches directly conflict with the goal of obtaining high carrier mobility, low $SS$, low source and drain series resistance ($R_{SD}$) and therefore large ON-state current ($I_{ON}$) and low OFF-state current ($I_{OFF}$) at low supply voltage.

1.1.2 Technology Boosters

So far, to delay the end of Moore’s law, imaginative “technology boosters” have been progressively introduced [7]. Since 2003 (90-nm node), tensile and compressive local strain across the Si channel have been used for the mobility enhancement of holes and electrons, respectively. Tensile strain on the channel of n-MOSFETs is induced by a Si$_3$N$_4$ cap film deposited above the gate stack [Figure 1.2(a)], while compressive strain on the channel of p-MOSFETs is implemented by SiGe heteroepitaxial regrowth of the source and drain (S/D) [Figure 1.2(b)] [10]. Unfortunately, the scaling of the transistor dimensions decreases the volume/quantity of the stressor materials for both n and p-MOSFETs thus decreasing mobility and drive current. As a result, performance was gained in the following technology nodes owing to the integration of even more challenging processes.

From 2003 to 2007 (90-nm and 65-nm nodes), the scaling of the SiO$_2$ gate dielectric slowed as
1.1. Extending Moore’s Law

Figure 1.3: TEM images of p-MOSFETs of the (a) 65-nm node featuring a SiO$_2$/poly-Si gate stack and (b) 45-nm node featuring a high-$k$/metal gate stack. The gate lengths of the devices in (a) and (b) are 35 nm [12, 13].

...a result of the power limitations arising from an increase in gate leakage. Indeed, as the thickness of the SiO$_2$ gate dielectric reduced to < 2 nm [Figure 1.3(a)], the gate leakage current due to direct tunneling of electrons through the SiO$_2$ increased to unacceptable levels [14]. In order to overcome this issue, the “high-$k$/metal gate” stack, [Figure 1.3(b)], was introduced in 2008 (45 nm node) [15]. The high dielectric constant (high-$k$) oxide enabled a gate leakage reduction by a factor $> 25$ while scaling the equivalent oxide thickness (EOT) by a factor $0.7$ [13]. The metal gate also replaced the doped polysilicon gate in order to resolve issues of drive current degradation due to polysilicon depletion [16] and $V_T$ variations due to Fermi level pinning at the high-$k$/polysilicon interface [17].

In 2011 (22-nm node), a non-planar 3-dimension (3-D) device architecture was introduced in order to further reduce short-channel effects (Figure 1.4). In this device architecture, the gate is wrapped around the top and the sidewalls of a Si fin, creating a tri-gate with an improved electrostatic control over the channel [18]. However, the tri-gate device architecture brings further process complexity when compared to the conventional planar device architecture. For instance, obtaining a uniform S/D doping of the fin surfaces using implantation has been found difficult due to the shadowing effect of adjacent fins [19], suggesting that an alternative technique, such as plasma doping may be required to achieve sidewall “conformal” doping [20]. Furthermore, significant challenges remain to maintain a high level of mobility enhancement from stress in fin structures with numerous free surfaces [7]. Maintaining the scaling roadmap will, therefore, require further improvement in channel mobility.

The monolithic integration of high-mobility III-V (and Ge) materials on a Si platform represents a potential long-term option for future sub-22-nm technology nodes [28]. Although III-V
Table 1.2: Performance of state-of-the-art III-V, SOI and bulk Si n-MOSFETs.

<table>
<thead>
<tr>
<th>Device</th>
<th>Dimensions</th>
<th>Performance</th>
<th>[Ref.]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>length ($L$)</td>
<td>$W_{fin}$</td>
<td>$I_{ON}$ ($\mu$A/µm)</td>
</tr>
<tr>
<td>InAs-OI</td>
<td>55</td>
<td>-</td>
<td>278</td>
</tr>
<tr>
<td>Planar FET</td>
<td></td>
<td></td>
<td>$V_{ds} = 0.5$ V</td>
</tr>
<tr>
<td>6 nm Al$_2$O$_3$</td>
<td></td>
<td></td>
<td>$V_{g}$-$V_{T} = 0.5$ V</td>
</tr>
<tr>
<td>In$<em>{0.62}$Ga$</em>{0.35}$As</td>
<td>80</td>
<td>20</td>
<td>$\sim$510</td>
</tr>
<tr>
<td>GAA FET</td>
<td></td>
<td></td>
<td>$V_{ds} = 0.5$ V</td>
</tr>
<tr>
<td>4 nm LaAlO$_3$/</td>
<td></td>
<td></td>
<td>$V_{g}$-$V_{T} = 0.5$ V</td>
</tr>
<tr>
<td>0.5 nm Al$_2$O$_3$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>140</td>
<td>-</td>
<td>$\sim$200</td>
</tr>
<tr>
<td>Planar FET</td>
<td></td>
<td></td>
<td>$V_{ds} = 0.5$ V</td>
</tr>
<tr>
<td>6.5 nm HfO$_2$/</td>
<td></td>
<td></td>
<td>$V_{g}$-$V_{T} = 0.5$ V</td>
</tr>
<tr>
<td>0.5 nm Al$_2$O$_3$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>140</td>
<td>40</td>
<td>$\sim$200</td>
</tr>
<tr>
<td>GAA FET</td>
<td></td>
<td></td>
<td>$V_{ds} = 0.5$ V</td>
</tr>
<tr>
<td>7 nm Al$_2$O$_3$/</td>
<td></td>
<td></td>
<td>$V_{g}$-$V_{T} = 0.5$ V</td>
</tr>
<tr>
<td>1 nm InP</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>60</td>
<td>40</td>
<td>$\sim$500</td>
</tr>
<tr>
<td>Tri-gate FET</td>
<td></td>
<td></td>
<td>$V_{ds} = 0.5$ V</td>
</tr>
<tr>
<td>high-k</td>
<td></td>
<td></td>
<td>$V_{g}$-$V_{T} = 0.5$ V</td>
</tr>
<tr>
<td>FDSOI</td>
<td>24</td>
<td>-</td>
<td>1070</td>
</tr>
<tr>
<td>Planar FET</td>
<td></td>
<td></td>
<td>$V_{ds} = 1$ V</td>
</tr>
<tr>
<td>SOI</td>
<td>13</td>
<td>22</td>
<td>455</td>
</tr>
<tr>
<td>Junctionless FET</td>
<td></td>
<td></td>
<td>$V_{ds} = 0.9$ V</td>
</tr>
<tr>
<td>HfSiON</td>
<td></td>
<td></td>
<td>$V_{g}$-$V_{T} = 0.65$ V</td>
</tr>
<tr>
<td>Bulk Si</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Tri-gate FET</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(LP)</td>
<td>34</td>
<td>-</td>
<td>410</td>
</tr>
<tr>
<td>(SP)</td>
<td>34</td>
<td>-</td>
<td>710</td>
</tr>
<tr>
<td>(HP)</td>
<td>30</td>
<td>-</td>
<td>1080</td>
</tr>
</tbody>
</table>

5
1.2 Challenges for High-\textit{k}/III-V MOSFETs

1.2.1 Low Defect Densities in High-\textit{k}/III-V Gate Stacks

Achieving low defect densities in high-\textit{k}/III-V gate stacks represents a considerable challenge as, unlike their Si counterpart, III-V semiconductors do not have a high quality native oxide. As a result, a high density of electrically active defects is observed not only at the high-\textit{k}/III-V interface but also within the high-\textit{k} dielectric.

The terminology used to define these defects is in line with the standardized terminology developed for the SiO\textsubscript{2}/Si system by the Deal committee in 1979 [29] and updated by Fleetwood in 1992 [30]. The high-\textit{k}/III-V defect terminology is presented using the case of the Al\textsubscript{2}O\textsubscript{3}/In\textsubscript{0.53}Ga\textsubscript{0.53}As system, which is the most widely studied high-\textit{k}/III-V system.

The Al\textsubscript{2}O\textsubscript{3} and In\textsubscript{0.53}Ga\textsubscript{0.53}As materials combine interesting electrical properties with good
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growth process control, making the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.53}\text{As}$ system highly attractive for metal-oxide-semiconductor (MOS) studies. $\text{Al}_2\text{O}_3$ offers a high bandgap ($\sim 9$ eV), a high breakdown electric field (5 - 30 MV/cm), a reasonably high dielectric constant (8.6 - 10) along with a high thermal stability ($> 1000^\circ\text{C}$) [31], while $\text{In}_{0.53}\text{Ga}_{0.53}\text{As}$ features a high Hall electron mobility of 4000 - 5000 cm$^2$/V.s [32], a sufficiently large bandgap of 0.74 eV [33] to avoid leakage current due to band-to-band tunneling [34] and a large intervalley separation of 0.5 eV that prevents population of the low mobility L and X valleys [35]. Moreover, from a processing point of view, the deposition of highly uniform $\text{Al}_2\text{O}_3$ films by atomic layer deposition (ALD) using trimethylaluminum ($\text{Al(CH}_3)_3$) (TMA) and $\text{H}_2\text{O}$ precursors is very well controlled [36] and high quality $\text{In}_{0.53}\text{Ga}_{0.53}\text{As}$ films are routinely grown lattice matched to epi-ready InP substrates by molecular beam epitaxy (MBE) and metal-organic vapor phase epitaxy (MOVPE) [37].

Defects such as interface traps, near-interface oxide traps (referred to here as border traps$^1$) and fixed oxide charges are depicted separately in Figure 1.5 (a), (b) and (c), respectively. Interface traps can exchange charges with the $\text{In}_{0.53}\text{Ga}_{0.53}\text{As}$ channel through a thermally activated Shockley-Read-Hall (SRH) process [45] and the trap occupancy is set by the Fermi-Dirac statistics [46]. In the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.53}\text{As}$ MOS system, the interface traps located at energy levels lying within the bandgap are donors (+/0), while the interface traps located within the conduction band are acceptors (0/-) [Figure 1.5(a)] [38, 39].

Recent studies have also indicated the presence of border traps located within a few nanometers from the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.53}\text{As}$ interface [41, 42] and at energy levels aligned with the $\text{In}_{0.53}\text{Ga}_{0.53}\text{As}$ conduction band [43] [Figure 1.5(b)]. Border traps are charged and discharged through a temperature-independent tunneling process [43] within timescales depending on their distances from the interface [38, 48].

Fixed oxide charges are oxide traps that do not “communicate” with the underlying channel as their energy position is either too high or too low to be reached by the Fermi level, making them always empty or always full [41] [Figure 1.5(c)]. The sign of their charge then depends on their nature (donor or acceptor) and on their energy position. As a result, a fixed positive charge is an always-empty donor (+/0) oxide trap, while a fixed negative charge is an always-full acceptor (0/-) oxide trap.

The interface traps located within the $\text{In}_{0.53}\text{Ga}_{0.53}\text{As}$ bandgap are responsible for the degradation of the switching performance (high $SS$). In the case of excessively large density of interface traps ($D_{it}$), the Fermi level can remain pinned within the $\text{In}_{0.53}\text{Ga}_{0.53}\text{As}$ bandgap, preventing the device from turning off. The interface traps located within the $\text{In}_{0.53}\text{Ga}_{0.53}\text{As}$ conduction band have been reported to pin the Fermi level within the conduction band [47], limiting the

$^1$The term border trap originates from an analogy with the term border state, which was used in the context of the American Civil War (1861-1865) [30].

$^2$Fleetwood defined border traps as oxide traps located within $\sim 3$ nm from the interface [39]. In recent MOS gate stack technologies, the oxides are so thin that all oxide traps can be considered to be border traps.
Figure 1.5: (a) Interface traps [38,40], (b) border traps [41,43] and (c) fixed oxide charges [44] in an Al₂O₃/In₀.₅₃Ga₀.₄₇As MOS device.
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Figure 1.6: Multi-frequency (M-F) capacitance-voltage (C-V) characteristics obtained on Al$_2$O$_3$/n-In$_{0.53}$Ga$_{0.47}$As MOSCAPs without (a) and with (b) the optimized (NH$_4$)$_2$S surface passivation reported in [49]. The M-F C-V characteristics were measured by Éamon O’Connor. (c) Impact of the same surface passivation on the effective mobility ($\mu_{\text{eff}}$) vs carrier density ($N_s$) extracted on flatband-mode MOSFETs [50]. The surface passivation was performed at the Tyndall National Institute and the design, fabrication and characterization of the flatband-mode Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOSFETs were performed at the University of Glasgow.

Electron mobility and drive current. Since the interface traps located within the In$_{0.53}$Ga$_{0.47}$As conduction band are acceptors, they also have the potential to result in mobility degradation due to Coulomb scattering. The border traps are responsible for the hysteresis generally observed in the current-voltage (I-V) and capacitance-voltage (C-V) characteristics of transistors, leading to $V_T$ instabilities. Fixed oxide charges are responsible for the $V_T$ shift and for the mobility degradation due to Coulomb scattering.

Continuous efforts to improve defect passivation and dielectric deposition processes have resulted in significant reductions in the densities of interface traps, border traps and fixed oxide charges present in high-$k$/III-V gate stacks. The use of metal-oxide-semiconductor capacitors (MOSCAPs) has been particularly relevant to the optimization of high-$k$/III-V gate stacks. Indeed, when compared to MOSFETS MOSCAPs offer the process simplicity needed for testing alternative passivation and deposition processes in the absence of the subsequent transistor process steps (i.e.: implantation, anneal, plasma etch), which can also affect the gate stack quality. Once optimized using a MOSCAP, the gate stack process can be integrated in a MOSFET process
1.2. Challenges for High-\textit{k}/III-V MOSFETs

Figure 1.7: $D_{it}$ values reported in the literature since 2008 for In$_{0.53}$Ga$_{0.53}$As MOS structures with LaAlO$_3$ \cite{53}, ZrO$_2$ \cite{54}, HfO$_2$ \cite{53-60}, Al$_2$O$_3$ \cite{12,49,60-69}, Si$_3$N$_4$ \cite{70} and SiO$_2$ \cite{71} gate oxides. The $k$-values of these gate oxides are reported in \cite{14}.

flow. As an example, Figure 1.6(a) and (b) show the significant reduction in frequency dispersion near the accumulation region in the multi-frequency (M-F) C-V characteristics of Al$_2$O$_3$/n-In$_{0.53}$Ga$_{0.53}$As MOSCAPs following the optimized (NH$_4$)$_2$S surface passivation process reported in \cite{49}. The integration of this process in an implant-free flatband-mode Al$_2$O$_3$/In$_{0.53}$Ga$_{0.53}$As MOSFET process flow \cite{51} yielded a significant increase in effective mobility ($\mu_{eff}$) at low carrier density ($N_s$) [Figure 1.6(c)] \cite{50}, consistent with a reduction in Coulomb scattering \cite{52} due to a reduction in $D_{it}$ near the In$_{0.53}$Ga$_{0.53}$As conduction band.

The main results reported on the passivation and electrical characterization of interface traps, border traps and fixed oxide charges are discussed in further detail in sub-sections 1.2.1.1, 1.2.1.2 and 1.2.1.3 respectively.

1.2.1.1 Interface Trap Passivation and Characterization

The passivation and characterization of interface traps, located at energy levels lying within the In$_{0.53}$Ga$_{0.53}$As bandgap, have been the focus of intense research in recent years. Figure 1.7 compares $D_{it}$ values reported in the literature since 2008 for In$_{0.53}$Ga$_{0.53}$As MOSCAPs with LaAlO$_3$ \cite{53}, ZrO$_2$ \cite{54}, HfO$_2$ \cite{53-60}, Al$_2$O$_3$ \cite{12,49,60-69}, Si$_3$N$_4$ \cite{70} and SiO$_2$ \cite{71} gate oxides. The short-dash red lines, representing the minimum and maximum $D_{it}$ values, show a discrepancy of more than 2 orders of magnitude, with reported $D_{it}$ values ranging from low-10$^{11}$ /cm$^2$.eV to exceeding 10$^{14}$ /cm$^2$.eV.

Part of this discrepancy can be attributed to the variability in surface passivation and oxide...
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Figure 1.8: Comparison of the \( D_{it} \) values reported for (a) HfO\(_2\)/In\(_{0.53}\)Ga\(_{0.47}\)As MOS structures \([55-60]\) and (b) Al\(_2\)O\(_3\)/In\(_{0.53}\)Ga\(_{0.47}\)As MOS structures \([42, 49, 60-69]\).

deposition processes. Various passivation methods, including treatment in \((\text{NH}_4)_2\text{S} \) \([49]\), \textit{in-situ} \(\text{H}_2\text{S} \) exposure subsequent to MOVPE \([72]\), \textit{in-situ} hydrogen \([73]\) and nitrogen \([59]\) plasmas prior to ALD, deposition of thin Si \([74, 75]\), and Ge interlayers \([76]\) and forming gas \(\text{H}_2/\text{N}_2 \) annealing \([77, 78]\) have shown improvements over unpassivated interfaces. Moreover, chemical vapor deposition (CVD) \([70]\), physical vapor deposition (PVD) \([71]\), molecular atomic deposition (MAD) \([65]\) and molecular beam deposition (MBD) \([79]\) have been reported for the deposition of various gate dielectrics on In\(_{0.53}\)Ga\(_{0.47}\)As, but the ALD \([86, 80]\) has now become mainstream, especially since the observation of the ALD “self-cleaning” effect on GaAs \([81-83]\) and on InGaAs \([84]\).

Part of this discrepancy can also be attributed to the high-\(k\) In\(_{0.53}\)Ga\(_{0.47}\)As interface control dependence on the composition of the gate dielectric. Figure 1.8 suggests that Al\(_2\)O\(_3\) can offer significantly better interface properties than HfO\(_2\), especially in the upper part of the In\(_{0.53}\)Ga\(_{0.47}\)As bandgap, which is of particular interest for \(n\)-channel MOSFETs. A number of groups have taken advantage of the good interface properties of the Al\(_2\)O\(_3\)/InGaAs system to form bi-layer oxide stacks, where the Al\(_2\)O\(_3\) is sandwiched between the InGaAs and an oxide of high-\(k\) value such as HfO\(_2\) \([59, 60, 85, 86]\), ZrO\(_2\) \([54]\) and LaAlO\(_3\) \([22]\).

The discrepancy in the reported \( D_{it} \) values extracted on high-\(k\) In\(_{0.53}\)Ga\(_{0.53}\)As MOSCAPs can also arise from the differences in \( D_{it} \) extraction methods \([87]\). This issue is illustrated in Figure 1.9, where a discrepancy of \(\sim 2\) orders of magnitude is observed between reported mid-gap \( D_{it} \) values extracted on similar ALD Al\(_2\)O\(_3\) films deposited \textit{ex-situ} on sulphur passivated
1.2. Challenges for High-$k$/III-V MOSFETs

In$_{0.53}$Ga$_{0.53}$As surfaces using the conductance method [49, 57, 61, 63, 64, 66], a method based on the fitting of a measured quasi-static (Q-S) C-V [62], the high-low frequency capacitance method [49] and the charge pumping method [42].

In$_{0.53}$Ga$_{0.53}$As surfaces using the conductance method [49, 57, 61, 63, 64, 66], a method based on the fitting of a measured quasi-static (Q-S) C-V [62], the high-low frequency capacitance method [49] and the charge pumping method [42].

The most commonly used methods, such as the conductance method [88], the low-frequency (Berglund) method [89], the high-frequency (Terman) method [90] and the combined high-low frequency capacitance (Castagné-Vapaille) method [91], were initially established to evaluate interface trap densities in the SiO$_2$/Si system. Unfortunately, these methods require various assumptions/approximations to be made in order to obtain parameters such as the oxide capacitance, the doping concentration or the capture cross sections. While these assumptions/approximations enable correct $D_{it}$ extraction in the SiO$_2$/Si system, blindly applying them to high-$k$/InGaAs systems can lead to erroneous $D_{it}$ values [92, 93]. This is mainly due to the fact that InGaAs features a lower conduction band density of state and smaller bandgap than Si and that the $D_{it}$ in high-$k$/InGaAs systems is significantly higher than that in the SiO$_2$/Si MOS system. Although some guidelines [92] have been reported to improve on the accuracy of the $D_{it}$ extraction in the high-$k$/InGaAs MOSCAPs, several issues still remain.

The conductance method, which is the most reliable and widely used $D_{it}$ extraction method [93], is only valid when applied in depletion [88]. This represents a significant limitation for extracting the $D_{it}$ profile across the full InGaAs bandgap, which is generally circumvented through the measurement of both n-type and p-type MOS structures [49] under the assumption that the

![Graph](image.png)

Figure 1.9: $D_{it}$ values extracted on similar ex-situ deposited ALD Al$_2$O$_3$ films on sulfur passivated In$_{0.53}$Ga$_{0.53}$As using the conductance method [49, 57, 61, 63, 64, 66], a method based on the fitting of a measured quasi-static (Q-S) C-V [62], the high-low frequency capacitance method [49] and the charge pumping method [42].
Si (n-type) and Zn (p-type) dopants, and differences in InGaAs growth conditions, have similar or no impact on the quality of the high-$k$/InGaAs interface.

The availability of high-$k$/III-V MOSFETs has enabled the development of alternative $D_{it}$ extraction methods to address the limitation of the conductance method. Martens et al. developed a “full conductance” method to extract the $D_{it}$ across the full semiconductor bandgap [93, 94], Ali et al. modeled the M-F gate-to-channel split C-V and conductance-voltage (G-V) characteristics to extract the $D_{it}$ near the In$_{0.53}$Ga$_{0.53}$As conduction band [53] and complement the conventional conductance method [88]. The charge pumping technique [95] was also used to profile the $D_{it}$ across the InGaAs bandgap [12, 67, 96, 97], and yielded $D_{it}$ profiles in reasonable agreement with those obtained from the other methods. Hall measurements were recently performed on high-$k$/III-V gated Hall bars as part of mobility studies [47, 98]. Contrary to the conventional gate-to-channel split C-V technique, which only enables to extract the total charge density (sum of inversion charge and trapped charge densities), the Hall measurement technique yields the mobile (inversion) charge density. In the work reported by Taoka et al. in [47], the total charge density obtained from gate-to-channel split C-V measurements was compared to the mobile charge density extracted from Hall measurements in order to extract the trap density located at energy levels aligned with the conduction band. This study revealed that large trap densities $>10^{12} \text{ cm}^{-2}\text{eV}$ were responsible for the Fermi level pinning inside the InGaAs conduction band, leading to a significant $I_{ON}$ degradation. Although this issue was initially attributed to the presence of interface traps located at energy levels aligned with the InGaAs conduction band [47], it is noted that border traps could also contribute to the pinning of the Fermi level inside the InGaAs conduction band.

1.2.1.2 Border Trap Passivation and Characterization

The presence of border traps located at energy levels aligned with the InGaAs conduction band and their effective passivation using a forming gas (H$_2$/N$_2$) anneal (FGA) process was demonstrated in [43] through the analysis of the frequency dispersion in the accumulation region of the M-F C-V characteristics of Al$_2$O$_3$/n-In$_{0.53}$Ga$_{0.53}$As MOSCAPs measured over a range of $T$ before and after FGA. No significant change in frequency dispersion in accumulation was observed when varying $T$ during measurements, suggesting the presence of a tunneling process involving border traps located at energy levels aligned with the In$_{0.53}$Ga$_{0.53}$As conduction band. Moreover, a marked reduction in frequency dispersion was observed following FGA, indicating a passivation of border traps with FGA. Admittance models accounting for the spatial distribution of border traps were then developed to explain the frequency dispersion in the accumulation region of the M-F C-V characteristics of Al$_2$O$_3$/n-In$_{0.53}$Ga$_{0.53}$As MOSCAPs [38, 48]. Following these studies, a more direct method based on the charge pumping technique [95] was applied.
to Al₂O₃/n-In₀.₅₃Ga₀.₅₃As MOSFETs in order to obtain the spatial distribution of border traps across the Al₂O₃ film thickness [42]. However, as the charge pumping method requires the use of a body contact, which is not always available in III-V MOSFETs, an alternative method based on high-frequency transconductance measurements was proposed by Johansson et al. in order to circumvent this problem [41]. This alternative method, demonstrated on planar surface-channel and vertical nanowire III-V MOSFETs featuring a 6.5-nm-thick HfO₂ gate dielectric on a 0.5-nm-thick Al₂O₃ interface control layer, yielded border trap densities of \( \sim 10^{21} \) /cm³.eV near the interface (depth < 0.5 nm) and of \( \sim 10^{19} \) /cm³.eV deeper in the oxide (depth > 0.5 nm) [41]. These border trap density values are consistent with the values extracted from C-V [38, 43, 48] and charge pumping [42] measurements.

### 1.2.1.3 Fixed Oxide Charge Passivation and Characterization

The nature and density of fixed oxide charges can be extracted using a set of MOSCAPs featuring different oxide thicknesses \( t_{\text{ox}} \). This method was applied in [99] to characterize the fixed oxide charges present in the Al₂O₃/In₀.₅₃Ga₀.₅₃As system. C-V characteristics, recorded at a frequency \( f \) of 1 MHz and a \( T \) of -50°C to minimize the contribution of interface and border traps to the measured capacitance [Figure 1.10(a)], were used to extract the flat-band voltage \( V_{\text{fb}} \) associated with each \( t_{\text{ox}} \). As the presence of positive (negative) fixed charges manifests itself as a negative (positive) shift of the \( V_{\text{fb}} \) relative to the theoretical flat-band voltage, the negative slope and positive intercept of the linear relationship observed on the \( V_{\text{fb}} \) vs \( t_{\text{ox}} \) curve revealed a negative interface fixed charge density \( N_{\text{int}} \) of \( 10^{13} \) /cm² at the Al₂O₃/n-In₀.₅₃Ga₀.₅₃As interface along with a positive bulk fixed charge density \( N_{\text{bulk}} \) of \( 2 \times 10^{19} \) /cm³ distributed throughout the bulk of the Al₂O₃ film [inset Figure 1.10(a)].

The effect of FGA on the fixed oxide charges present in the Al₂O₃/In₀.₅₃Ga₀.₅₃As system has been studied in [44, 99, 101]. Comparing the pre-FGA [Figure 1.10(a)] and post-FGA [Figure 1.10(b)] C-V characteristics reported in [99], clearly shows that FGA is an efficient technique to passivate fixed charges. Indeed, after FGA the C-V characteristics are aligned at \( V_{\text{theo}} \) (within the error on the estimation of the metal work function) [Figure 1.10(b)] and the \( V_{\text{fb}} \) shift with \( t_{\text{ox}} \) has become negligible [inset Figure 1.10(b)]. A detailed analysis of the \( V_{\text{fb}} \) vs \( t_{\text{ox}} \) data following FGA revealed a negative fixed charge density of \( 7.4 \times 10^{11} \) /cm² at the interface along with a positive fixed charge density of \( 5 \times 10^{18} \) /cm³ distributed throughout the bulk of the Al₂O₃ film, representing a reduction in interface fixed charge density and bulk fixed charge density of 92% and 75%, respectively.
Figure 1.10: Normalized C-V characteristics measured on Al$_2$O$_3$/n-In$_{0.53}$Ga$_{0.53}$As MOSCAPs at a frequency ($f$) of 1 MHz and a temperature ($T$) of -50°C (a) before and (b) after FGA [99]. The oxide thickness ($t_{ox}$) ranges from 11.5 nm to 20 nm. The insets show the evolution of the flat-band voltage ($V_{fb}$) as a function of $t_{ox}$. $N_{bulk}$ and $N_{int}$ represent the bulk and the interface fixed charge densities, respectively. The beige shaded area indicates the uncertainty on the theoretical flat-band voltage ($V_{fb}^{theo}$).
1.2. Challenges for High-\textit{k}/\textit{III-V} MOSFETs

Figure 1.11: Transfer length ($L_t$) vs specific contact resistivity ($\rho_C$) curve calculated for \textit{n}-In$_{0.53}$Ga$_{0.53}$As epitaxially doped to $\sim 3.5 \times 10^{19}$ /cm$^3$ featuring a sheet resistance ($R_{\text{sheet}}$) of 17 $\Omega$/sq. $^{103}$. In this configuration, the contact length ($L_C$) of 7 nm targeted for the 12-nm node is much lower than $L_t$.

1.2.2 Low Resistance Source and Drain Contacts

Aggressive scaling of the S/D is also urgently needed for potential insertion of \textit{III-V} MOSFETs into production by 2020 (12-nm node). At this stage and according to the \textit{international technology roadmap for semiconductor (ITRS)} the MOSFETs should feature a drain current in saturation ($I_{D,\text{sat}}$) of 2733 $\mu$A/\mu$m$ at a supply voltage ($V_{DD}$) of 0.68 V with a S/D contact length ($L_C$) of 7 nm and a $R_{SD}$ of 120 $\Omega$/\mu$m $^{102}$.

In order to put these values in the perspective of a future \textit{III-V MOSFET} we can assume an In$_{0.53}$Ga$_{0.53}$As device meeting the 12-nm node performance/scaling targets $^{102}$ and featuring S/D made of an \textit{n}-In$_{0.53}$Ga$_{0.53}$As material epitaxially doped to its saturation limit ($\sim 3.5 \times 10^{19}$ /cm$^3$). The successful MBE growth of such a material was reported in $^{103}$, where the \textit{presented transfer length method (TLM)} $^{104}$ analysis was used to extract an \textit{n}-In$_{0.53}$Ga$_{0.53}$As sheet resistance ($R_{\text{sheet}}$) of $\sim 17$ $\Omega$/sq. The transfer length ($L_t$), which is the distance over which most (1/e) of the current flows from the semiconductor to the metal (or vice versa), can then be calculated as a function of specific contact resistance ($\rho_C$) for a given $R_{\text{sheet}}$ (Figure 1.11) using:

$$L_t = \frac{\rho_C}{\sqrt{R_{\text{sheet}}}}$$ \hfill (1.1)

In such a device configuration, it is clear that the $L_C$ of 7 nm targeted for the 12-nm node would be much lower than $L_t$, leading to significant current crowding and an exponential increase in $\rho_C$. 

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Figure 1.12: Percentage loss in drain current in saturation ($I_{D,sat}$) vs specific contact resistivity ($\rho_C$) curve calculated for a 12-nm node device using the method reported in [106].

[105] Assuming a $R_{SD}$ dominated by contact resistances, it is possible to estimate the impact of $\rho_C$ on $I_{D,sat}$ using the method reported in [106]. From Figure 1.12 it is clear that the 12-nm node will require an ultralow $\rho_C$ of $< 5 \times 10^{-9} \, \Omega \cdot \text{cm}^2$, in close agreement with [105].

In the case of experimental InGaAs MOSFETs used as test vehicles for gate stack engineering and characterization, the S/D areas are generally formed by Si implantation [39, 42, 77, 101, 107–109]. So far, maximum doping concentrations in the range of $\sim 4 \times 10^{18}$ /cm$^3$ have been achieved using this technique [110]. Such doping levels appear to be insufficient to achieve the $\rho_C < 5 \times 10^{-9} \, \Omega \cdot \text{cm}^2$ target. Alternatives to implantation are currently under investigation. Values of $\rho_C < 10^{-8} \, \Omega \cdot \text{cm}^2$ have been successfully obtained on n-InGaAs surfaces epitaxially doped to $\sim 3.5 \times 10^{19}$ /cm$^3$ and treated with HN$_4$OH prior to metal contact deposition [103]. To improve on the reproducibility, contacts deposited in-situ by MBE on highly doped (> $10^{19}$ /cm$^3$) n-InAs and n-InGaAs surfaces were investigated and revealed ultralow $\rho_C$ values in the range of $5.0 \times 10^{-9}$ to $1.5 \times 10^{-8} \, \Omega \cdot \text{cm}^2$ [111, 112].

However, since this technique adds significant process complexity, a different approach to form low Schottky barrier height (SBH) contacts using a “nikelide” Ni-In$_x$Ga$_{1-x}$As metallic phase is now attracting significant attention [113, 114]. In [115], contacts formed by alloying a thin ex-situ deposited Ni film with In$_x$Ga$_{1-x}$As, were reported to offer a low SBH of 0.13 eV for Ni-In$_{0.53}$Ga$_{0.57}$As/In$_{0.53}$Ga$_{0.57}$As and almost 0 eV for Ni-In$_x$Ga$_{1-x}$As/In$_x$Ga$_{1-x}$As (x > 0.7). This technique, which also offers the advantage of being fully complementary metal-oxide-semiconductor (CMOS) compatible [116], was adopted by a number of groups for the S/D contact.
1.3 Objectives and Organization of the Thesis

formation of III-V MOSFETs [21, 116, 117]. Very recently, this technique was applied to undoped InAs to form a Ni-InAs phase, which yielded a record low $\rho_C$ value of $2.7 \times 10^{-9} \Omega\text{cm}^2$ [118]. This important result not only confirms the trend reported in [115] for SBH reduction with In concentration, but also gives strong evidence that the 12-nm node ITRS target for $\rho_C$ is achievable with InAs.

1.2.3 Integration of III-V Channel Materials on a Si Platform

Finally, the insertion of III-V MOSFETs into production will require the integration of III-V materials on large Si platforms. While various techniques including the use of III-V composite buffers [119, 120], shallow trenches in Si for aspect ratio trapping [121, 122] and wafer bonding [123, 124] have already been demonstrated, further improvements are still required in order to meet industry requirements. While it is clear that addressing this issue is of critical importance to the future of the III-V MOSFET technology, this research topic goes beyond the objectives of this thesis.

1.3 Objectives and Organization of the Thesis

This thesis covers the development and analysis of two Al$_2$O$_3$/In$_{0.53}$Ga$_{0.53}$As MOSFET device architectures. The fabricated devices were used to investigate the fixed oxide charge [107], interface traps [39] and border traps in the Al$_2$O$_3$/In$_{0.53}$Ga$_{0.53}$As gate stack along with the factors which limit carrier mobility in the In$_{0.53}$Ga$_{0.53}$As channel [108, 125]. The first Al$_2$O$_3$/In$_{0.53}$Ga$_{0.53}$As MOSFET developed was a conventional inversion-mode device, with a surface channel and Si-implanted S/D regions [120]. The second Al$_2$O$_3$/In$_{0.53}$Ga$_{0.53}$As MOSFET architecture was based on the junctionless device concept, first reported by Prof. J. P. Colinge on SOI in 2010 [127]. The fabricated junctionless Al$_2$O$_3$/In$_{0.53}$Ga$_{0.53}$As MOSFET featured a fully-depleted In$_{0.53}$Ga$_{0.53}$As channel isolated by a wide bandgap In$_{0.52}$Al$_{0.48}$As buffer [120].

Figure 1.13 shows a logic flow chart of the research work presented in this thesis. The work started with a preliminary study of the Si implant activation in p-In$_{0.53}$Ga$_{0.53}$As [78], to form the S/D regions of the inversion-mode MOSFET. Test structures based on the TLM [104] were used in a Doehlert design of experiment [128] to optimize the activation anneal process, while MOSCAPs were used to investigate the impact of the activation anneal process on the MOS gate stack performance [129] (Chapter 2). A FGA process was used to improve the performance of the fabricated inversion-mode MOSFETs [117] and extend on the study of fixed oxide charge passivation by FGA reported by Long et al. in [99] (Chapter 3). The devices were also used as test vehicles for the investigation of electrically active defects present in the Al$_2$O$_3$/In$_{0.53}$Ga$_{0.53}$As gate stack [39, 130]. An alternative technique based on a combination of full-gate capacitance
Figure 1.13: Logic flow chart of research work presented in this thesis.
1.3. Objectives and Organization of the Thesis

measurements [131] and self-consistent Poisson-Schrödinger calculations [132, 133] was developed for this purpose (Chapter 4). The electron mobility in the $\text{In}_{0.53}\text{Ga}_{0.53}\text{As}$ channel was also investigated (Chapter 5). The application of the inversion-charge pumping (ICP) method, first proposed by Kerber et al. in [95, 134] for the mobility extraction of high-$k$ SiO$_2$/Si MOSFETs, was demonstrated on $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.53}\text{As}$ MOSFETs [125] and further developed for the characterization of border traps. The obtained mobility results were also compared to low-temperature split C-V results. These detailed investigations allowed to identify a major issue arising from the S/D formation of the inversion-mode device architecture. In order to circumvent this issue, an $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.53}\text{As}$ junctionless MOSFET was developed [126]. The impact of channel thickness on the performance of the fabricated junctionless devices was also studied (Chapter 6). In the last chapter (Chapter 7), a summary of the main results obtained in this work is presented along with some suggestions for further research.
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Chapter 2

Source/Drain Activation and Impact on Gate Stack

2.1 Introduction

As mentioned in section 1.2.1 (page 6), a significant amount of research has already been dedicated to the integration of high-$k$ gate oxides on In$_{0.53}$Ga$_{0.47}$As substrates through the use of metal-oxide-semiconductor capacitors (MOSCAPs). However, the additional process steps required to form the source and drain (S/D) of an In$_{0.53}$Ga$_{0.47}$As MOSFET can significantly increase the complexity of the device fabrication process flow. As a result, the In$_{0.53}$Ga$_{0.47}$As MOSFET fabrication process flow must be carefully engineered so that the formation of the S/D does not excessively degrade the electrical properties of the gate stack.

Two types of process flows are generally reported for S/D-implanted III-V metal-oxide-semiconductor field-effect transistors (MOSFETs): the gate-first process [13] and the gate-last process [35]. The gate-first process offers the advantage of being a self-aligned process. However, since the high-$k$ metal-gate stack is formed before the S/D implant and anneal steps, the metal, the high-$k$ and the high-$k$/In$_{0.53}$Ga$_{0.47}$As interface have to withstand the activation anneal process, which generally leads to performance degradation of the gate stack. In the gate-last process, which is non self-aligned, the high-$k$ metal-gate stack is deposited after the S/D implant and anneal steps. This adds further process complexity as a sacrificial oxide layer needs to be deposited before the S/D implant and removed after the S/D activation anneal. Although it was demonstrated in [3] that the gate-last process offers better gate stack electrical properties than the gate-first process, we speculate that the gate-last process may suffer from repeatability issues as the In$_{0.53}$Ga$_{0.47}$As surface is exposed to additional processing before the high-$k$ oxide deposition.

The “high-$k$/first + metal-gate last” process represents an intermediate approach between the...
gate-first and gate-last processes, where the high-$k$ oxide is deposited before the S/D implant and S/D activation anneal but the metal-gate is formed after the S/D activation anneal. This approach enables to minimize the In$_{0.53}$Ga$_{0.47}$As native oxide formation due to air exposure and the In$_{0.53}$Ga$_{0.47}$As surface degradation/contamination due to additional wet chemical treatments. It also avoids the annealing of the metal-gate during the S/D activation process. Removing these sources of gate stack degradation allows the study of the impact of the S/D activation anneal on the high-$k$ oxide insulating properties and on the high-$k$/In$_{0.53}$Ga$_{0.47}$As interface.

In this work, we first optimized the S/D activation anneal process using test structures based on the transfer length method (TLM) as part of a Doehlert design of experiment (DOE). We also investigated the impact of the S/D activation anneal process on the gate stack performance of “pre-metal annealed” In$_{0.53}$Ga$_{0.47}$As MOSCAPs and fabricated “high-$k$ first + metal-gate-last” In$_{0.53}$Ga$_{0.47}$As n-MOSFETs.

### 2.2 Samples Preparation

TLM structures, pre-metal annealed MOSCAPs (MOSCAPs exposed to S/D activation anneal prior to gate metal deposition) and “high-$k$ first + metal-gate last” n-channel MOSFETs were fabricated on p-In$_{0.53}$Ga$_{0.47}$As (80 nm, $5 \times 10^{16}$ /cm$^3$)/p-InP buffer (80 nm, $5 \times 10^{16}$ /cm$^3$)/Semi-Insulating (SI)-InP wafers grown by metal-organic vapor phase epitaxy (MOVPE). The growth was performed at low pressure (80 mbar) in a commercial horizontal MOVPE reactor using standard metalorganic precursors: trimethylindium (TMIn), trimethylgallium (TMGa), and Diethylzinc (DEZn), purified hydride precursors: arsine (AsH$_3$) and phosphine (PH$_3$) in purified N$_2$ carrier gas. The growth temperature was 760°C (thermocouple) and the growth rate was 1 µm/h throughout. The V/III ratio during the In$_{0.53}$Ga$_{0.47}$As layer growth was 140. Low temperature photoluminescence (10 K) linewidths below 1 meV (unpublished data) were system-
2.3 Doehlert Design of Experiment

Doehlert [DOEs] are second-order uniform-shell designs [7], which offer significant advantages over second-order counterparts such as central composite and Box-Behnken designs. They need fewer experimental runs per number of model coefficients and are, therefore, more efficient [20]. The methods of implementation, statistical analysis and process optimization used in this study are presented in Appendix A (page 152). Further details can be obtained in reference [21]. Briefly, 

1The Au/Ge/Au stack forms an eutectic that melts at 360°C. The Ge diffuses in the In$_{0.53}$Ga$_{0.47}$As and acts as a n-type dopant. The Ni enhances the Ge diffusion process and also prevents the contact from “balling-up”. The 200-nm-thick Au overcoat is used to reduce the sheet resistance of the metal stack [10].
Chapter 2. Source/Drain Activation and Impact on Gate Stack

Figure 2.1: (a) Time vs temperature anneal process window showing the seven activation anneal conditions of the DOE along with activation anneal conditions reported in the literature [12-13]. The lowest thermal budget limit, where InP etch pitting starts, is also indicated [19]. (b) Optical image of a fabricated TLM structure. The width \( W \) of the Si-implanted TLM bar is 30 µm and the metal contact separations \( d \) are 5, 10, 15, 25, 40 and 60 µm.

A two-factor Doehlert DOE relies on the following mathematical model:

\[
\hat{Y} = \beta_0 + \beta_1 X_1 + \beta_2 X_2 + \beta_{11} X_1^2 + \beta_{22} X_2^2 + \beta_{12} X_1 X_2
\]  

(2.1)

where \( \hat{Y} \) is the estimated response, \( X_1 \) and \( X_2 \) are the normalized variables representing the two factors, \( \beta_0 \) is the offset coefficient, \( \beta_1 \) and \( \beta_2 \) are the first-order coefficients, \( \beta_{11} \) and \( \beta_{22} \) are the second-order coefficients and \( \beta_{12} \) is the interaction coefficient. Seven experimental runs are required to obtain the six coefficients of the model. The statistical significance of the coefficients is assessed with a Student’s \( t \)-test and the statistical significance of the model is checked with an analysis of variance (ANOVA). The process optimization is performed using the Lagrange criterion.

2.4 Results and Discussion

2.4.1 Analysis of Doehlert Design of Experiment

The current-voltage (I-V) characteristics obtained on all the TLM samples showed ohmic behavior [Figure 2.2(a)]. The measured resistances of the seven samples plotted against their corresponding measured contact separation are shown in Figure 2.2(b). The contact separations were measured using a calibrated optical microscope. The results obtained for each run were
2.4. Results and Discussion

Figure 2.2: (a) Current-voltage (I-V) measurements of the sample annealed in run 2, where 5 to 60 indicate the contacts separations \(d\) in \(\mu m\). (b) Resistances \(R\) vs \(d\), where 1 to 7 are the run numbers. Inset: Linear extrapolation of \(R\) vs \(d\) (run 5). The slope is \(R_{\text{sheet}}/W\), the \(y\)-intercept is \(R = 2 \times R_C\) and the \(x\)-intercept is \(d = -2 \times L_t\).

fitted with a linear model in order to extract the sheet resistance \(R_{\text{sheet}}\) values. The correlation coefficient \(R\) of each individual fit was found to be greater than 0.99991, indicating excellent fitting of the linear models to the experimental data. Values of contact resistance \(R_C\) and transfer length \(L_t\) were obtained by extrapolating the linear fits [inset of Figure 2.2(b)] and their corresponding specific contact resistance \(\rho_C\) values were calculated from \(\rho_C = R_{\text{sheet}} \times L_t\). Table 2.2 shows the obtained \(R_{\text{sheet}}\), \(R_C\), \(L_t\) and \(\rho_C\) values. The \(R_{\text{sheet}}\) values were used as part of the Doehlert DOE to obtain the following model:

\[
\hat{Y} = 265.0 - 167.6 \times X_1 - 35.8 \times X_2 + 102.9 \times X_1^2 + 47.9 \times X_2^2 + 25.9 \times X_1X_2
\]

where \(\hat{Y}\) is the estimated \(R_{\text{sheet}}\), \(X_1\) is the normalized anneal temperature and \(X_2\) is the normalized anneal time. The Student’s \(t\)-test \([P\text{-value } (P) < 0.05]\) showed that all the coefficients are statistically significant (Table 2.3). The effect of the anneal temperature on \(R_{\text{sheet}}\) is more important than the effect of anneal time since \(\beta_1 > \beta_2\) and \(\beta_{11} > \beta_{22}\). The ANOVA \([P < 0.05]\) revealed that the model is statistically significant (Table 2.4). A determinant coefficient \(R^2\) of 0.99972 was obtained, indicating that less than 0.1% of the experimental response is not explained by the model. Moreover, the corresponding \(R\) of 0.99986 indicates an excellent fit of the model to the experimental response. Figure 2.3 shows the evolution of \(R_{\text{sheet}}\) within the experimental domain. \(R_{\text{sheet}}\) reduces dramatically with anneal temperature and an anneal time slightly above 30 s gives the lowest \(R_{\text{sheet}}\) achievable with any given anneal temperature of the experimental domain. The Lagrange criterion applied to the model revealed an optimized
Table 2.2: Experimental $R_{\text{sheet}}$, $R_C$, $L_t$ and $\rho_C$ obtained for each run of the Doehlert DOE. $F_1$ and $F_2$ are the anneal temperature factor and the anneal time factor, respectively.

<table>
<thead>
<tr>
<th>Run</th>
<th>$F_1$ ($^\circ\text{C}$)</th>
<th>$F_2$ (s)</th>
<th>$R_{\text{sheet}}$ ($\Omega/\square$)</th>
<th>$R_C$ ($\Omega$)</th>
<th>$L_t$ (nm)</th>
<th>$\rho_C$ ($\Omega\cdot\text{cm}^2$)</th>
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<td>1 (mean)</td>
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<td>30</td>
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<td>5.0</td>
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<td>725</td>
<td>30</td>
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<td>$5.2 \times 10^2$</td>
<td>$5.5 \times 10^{-7}$</td>
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<td>45</td>
<td>224.2</td>
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<td>30</td>
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<td>$6.3 \times 10^{-6}$</td>
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<td>15</td>
<td>263.9</td>
<td>5.7</td>
<td>$6.1 \times 10^2$</td>
<td>$9.8 \times 10^{-7}$</td>
</tr>
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</table>

a Mean of: $1.1 \times 10^{-6}$, $5.1 \times 10^{-8}$, $6.6 \times 10^{-7}$, $6.8 \times 10^{-7}$, $1.2 \times 10^{-6}$.

Table 2.3: Student’s $t$-test applied to each coefficient of the $R_{\text{sheet}}$ model.

<table>
<thead>
<tr>
<th>Term</th>
<th>Coefficient</th>
<th>Estimate</th>
<th>Standard error</th>
<th>$t$-value</th>
<th>$P$-value</th>
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<tbody>
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<td>87.1</td>
<td>$3.8 \times 10^{-9}$ a</td>
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<td>-95.5</td>
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</tr>
<tr>
<td>Time</td>
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<td>1.8</td>
<td>-20.4</td>
<td>$5.1 \times 10^{-6}$ a</td>
</tr>
<tr>
<td>Temperature $\times$ Time</td>
<td>$\beta_{12}$</td>
<td>25.9</td>
<td>3.5</td>
<td>7.4</td>
<td>$7.3 \times 10^{-4}$ a</td>
</tr>
<tr>
<td>Temperature $\times$ Temperature</td>
<td>$\beta_{11}$</td>
<td>102.9</td>
<td>3.7</td>
<td>27.6</td>
<td>$1.2 \times 10^{-6}$ a</td>
</tr>
<tr>
<td>Time $\times$ Time</td>
<td>$\beta_{22}$</td>
<td>47.9</td>
<td>3.7</td>
<td>12.9</td>
<td>$5.2 \times 10^{-5}$ a</td>
</tr>
</tbody>
</table>

a Significant at a 5% level ($P < 0.05$).

process condition of 715°C for 32 s, leading to a minimum $R_{\text{sheet}}$ of $(195.6 \pm 3.4)$ $\Omega/\square$.

Since the range of values obtained for $\rho_C$ in run 1 was comparable to the range of $\rho_C$ values of the entire study (Table 2.2), we could not obtain a reliable Doehlert model for $\rho_C$ and no definite conclusions could be drawn in relation to the variation of $\rho_C$ with activation anneal temperature and time. This can be explained by the fact that the $R_C$ values are much lower than the $R_{\text{sheet}}$ values, making the extraction of the $\rho_C$ values very sensitive to errors in the measurements of the TLM resistances and dimensions. In this case, the approach used in [22], where TLM structures with a range of sub-micron spacing between the contacts are used, should provide a significantly lower error in the extracted $\rho_C$ values and yield a statistically significant $\rho_C$ model. A $\rho_C$ value of $(7.4 \pm 4.5) \times 10^{-7}$ $\Omega\cdot\text{cm}^2$ was obtained by applying the error analysis reported in [23] to the set of $\rho_C$ values of run 1. Although this value, obtained with a non-alloyed Au/Ge/Au/Ni/Au contact and no surface preparation, is comparable to the $\rho_C = 4.3 \times 10^{-7} \Omega\cdot\text{cm}^2$ reported in [24] for annealed Pd/Si-based contacts on a $1 \times 10^{19}$ $\text{cm}^{-3}$ Si-doped In$_{0.5}$Ga$_{0.5}$As epitaxial layer, a significant $\rho_C$ improvement is still required for S/D-implanted III-V MOSFETs to be considered as a viable alternative to standard Si MOSFETs. Considering the international technology roadmap for semiconductor (ITRS) timescales for potential III-V
Table 2.4: ANOVA applied to the entire model.

<table>
<thead>
<tr>
<th>Source of variation</th>
<th>Sum of squares</th>
<th>Degree of freedom</th>
<th>Mean square</th>
<th>F-value</th>
<th>P-value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model</td>
<td>106447.1</td>
<td>5</td>
<td>21289.4</td>
<td>2314.1</td>
<td>2.1 × 10^{-8} a</td>
</tr>
<tr>
<td>Residuals</td>
<td>46.0</td>
<td>5</td>
<td>9.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lack of fit</td>
<td>8.6</td>
<td>1</td>
<td>8.6</td>
<td>0.9</td>
<td>0.4</td>
</tr>
<tr>
<td>Pure error</td>
<td>37.4</td>
<td>4</td>
<td>9.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td>106476.8</td>
<td>10</td>
<td>10647.7</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

$R^2 = 0.99972$, $R = 0.99986$. a Significant at a 5% level ($P < 0.05$).

Figure 2.3: $R_{\text{sheet}}$ response surface and contour plot as a function of annealing temperature and time. The correlation coefficient $R$ of the model is $0.99986$. The Lagrange criterion applied to the model revealed an optimized process condition of $715 {}^\circ \text{C}$ for 32 s, leading to a minimum $R_{\text{sheet}}$ of $(195.6 \pm 3.4) \Omega/\square$. 
Chapter 2. Source/Drain Activation and Impact on Gate Stack

MOSFETs insertion into production, \( \rho_C \) values below \( 5 \times 10^{-9} \, \Omega \cdot \text{cm}^2 \) will have to be achieved [25]. Although our results suggest that such low \( \rho_C \) values might not be achievable with ion implantation, the issue of S/D formation might not represent a showstopper for III-V MOSFETs as a \( \rho_C \) of \( 2.7 \times 10^{-9} \, \Omega \cdot \text{cm}^2 \) was recently achieved with an alternative technique to form a metallic Ni-InAs contact on InAs [22] (see also section 1.2.2 page 16).

We performed secondary ion mass spectrometry (SIMS) measurements and cross-sectional transmission electron microscopy (TEM) analysis on the sample annealed in run 1 (at 675°C for 30 s) as it represents the centre point of the experimental domain used for the DOE. The comparison of the SIMS Si ion profiles before and after activation annealing shown in Figure 2.4(a) clearly indicates that the Si ions did not diffuse during activation annealing, in agreement with [26] and ruling out the degradation of \( R_{sheet} \) and \( \rho_C \) due to a loss of Si ions. The SIMS profiles show reasonably good agreement with the stopping and range of ions in matter (SRIM) simulation [27]. It is noted that a HfO\(_2\) thickness of \((10.1 \pm 0.1)\) nm across a 2-in wafer was measured by SE [inset of Figure 2.4(a)] and used in the simulation. The SIMS and simulated profiles show a high Si ion concentration (\( > 2 \times 10^{19} \, /\text{cm}^3 \)) within the first 40 nm of the \( p-\text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) along with a \( \sim 100 \, \text{nm/dec.} \) tail roll-off. Figure 2.4(b) reveals that the location of the ion implantation defects follows the trend of the Si ion concentration of the SIMS profile. Extended defects are observed in the \( p-\text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) to a depth of \( \sim 75 \, \text{nm} \), while coarser agglomerates can be seen to a depth of \( \sim 40 \, \text{nm} \), where the Si ion concentration in the SIMS profile is highest [Figure 2.5(a)]. Figure 2.4(c) shows that the 675°C for 30 s anneal process did not eliminate the implantation defects, consistent with [26], while Figure 2.5(b) indicates that the anneal leads to the formation of characteristic loop defects that have a peak depth of \( \sim 50 \, \text{nm} \). We speculate that these defects could be responsible for the degradation of \( R_{sheet} \) and \( \rho_C \).

2.4.2 Impact of Activation Anneal on Gate Stack Performance

Pre-metal annealed MOSCAPs featuring bi-layer oxide films, composed of 2 nm of Al\(_2\)O\(_3\) and 8 nm of HfO\(_2\), were characterized in terms of leakage and capacitance to study the impact of the S/D activation anneal process on the gate stack performance. Low leakage current densities below \( 2.1 \times 10^{-8} \, \text{A/cm}^2 \) at electrical fields below \( \sim 3 \, \text{MV/cm} \) were obtained. Although the Al\(_2\)O\(_3\)/HfO\(_2\) films were deposited on a \( p \)-doped \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) material, the capacitance-voltage (C-V) characteristics revealed \( n \)-type behaviour [Figure 2.6(a) and (b)]. This is an unexpected result, which could indicate possible diffusion effects of unintentional \( n \)-type dopants arising from the substrate/epitaxial interface during the MOVPE growth and/or the activation anneal process, consistent with a recent report from Ostinelli et al. [28]. Increasing the anneal temperature from 675°C [Figure 2.6(a)] to 725°C range [Figure 2.6(b)], did not increase the dispersion of capacitance per decade of frequency in accumulation, which remained at a low value.
2.4. Results and Discussion

Figure 2.4: (a) SRIM simulation and SIMS measurements (before and after 675°C for 30 s annealing) of the two-stage Si implantation (1 × 10^{14} /cm² at 80 keV and 1 × 10^{14} /cm² at 30 keV) into the HfO₂ (10 nm)/p-In₀.₅₃Ga₀.₄₇As (160 nm)/p-InP (80 nm)/SI-InP structure. Inset: Contour plot of the HfO₂ film thickness measured by SE across a 2-in wafer. TEM images of (b) a non-annealed sample and (c) a 675°C for 30 s annealed sample. The SIMS measurements were conducted at INTEL Ireland and the TEM analysis was performed by S. B. Newcomb (Glebe Scientific).
Figure 2.5: TEM images of the Si-implanted ($1 \times 10^{14}$/cm$^2$ at 80 keV and $1 \times 10^{14}$/cm$^2$ at 30 keV) HfO$_2$ (10 nm)/$p$-In$_{0.53}$Ga$_{0.47}$As (160 nm)/$p$-InP (80 nm)/Si-InP structure (a) before and (b) after 675$^\circ$C for 30 s annealing. The TEM analysis was performed by S. B. Newcomb (Glebe Scientific).

of 1.7%, suggesting that the annealing did not involve the creation of a significant amount of oxide traps. However, a significantly larger distortion of the C-V characteristics was observed on the sample annealed at 725$^\circ$C. This is consistent with an increase in the density of interface traps ($D_{it}$) in the In$_{0.53}$Ga$_{0.47}$As bandgap with anneal temperature. Figure 2.6(c) shows the 100 kHz conductance-voltage (G-V) and C-V characteristics of samples annealed at 675$^\circ$C, 700$^\circ$C and 725$^\circ$C. The impact of the increasing conductance peak with temperature is clearly visible on the C-V characteristics, where it manifests as an increase in stretch out. $D_{it}$ estimates for each anneal temperature were obtained using the conductance method [29]. Although $D_{it}$ calculations using the 100-kHz conductance peaks underestimate the actual $D_{it}$ values, it is interesting to consider the $D_{it}$ trend with anneal temperature. Large $D_{it}$ values of 2.0, 2.3 and $2.7 \times 10^{13}$/cm$^2$.eV were obtained for the samples annealed at 675$^\circ$C, 700$^\circ$C and 725$^\circ$C, respectively. This indicates that, in the 675$^\circ$C to 725$^\circ$C range, an increase of 25$^\circ$C increases $D_{it}$ by $\sim$ 16%. Considering the following relationship between the MOSFET subthreshold swing (SS) and $D_{it}$ [30, 31]:

$$SS \approx \left( \frac{k_B T \ln(10)}{q} \right) \left( 1 + \frac{q D_{it}}{C_{ox}} \right)$$

(2.3)
where $k_B$ is the Boltzmann constant, $T$ is the temperature and $C_{ox}$ is the oxide capacitance, it is clear that this issue is of critical importance for the fabrication of future high-performance In$_{0.53}$Ga$_{0.47}$As MOSFETs.

### 2.4.3 Issues With First Fabricated MOSFETs

Figure 2.7(a) shows a picture of an In$_{0.53}$Ga$_{0.47}$As MOSFET fabricated with the "high-$k$ first + metal-gate last" process. The S/D activation anneal was performed at 650°C for 30 sec in N$_2$. We used a lower activation anneal temperature than that of the optimum point predicted by the DOE in order to maintain reasonable $D_{it}$ in the In$_{0.53}$Ga$_{0.47}$As bandgap. Figure 2.7(b) shows the drain current ($I_d$) vs drain-to-source voltage ($V_{ds}$) characteristics of a 5-μm-gate-length device featuring a 10-nm-thick HfO$_2$ gate oxide. Although a maximum $I_d$ of 180 mA/mm was achieved at a gate voltage ($V_g$) of 2 V and a $V_{ds}$ of 2.5 V, a large OFF-state current ($I_{OFF}$) was observed, even at a $V_g$ of -2 V. This large $I_{OFF}$ is consistent with the unexpected n-type behaviour of the C-V characteristics. Indeed, since the devices are not isolated, any n-In$_{0.53}$Ga$_{0.47}$As linking the source and drain terminals outside of the gate area could potentially contribute to the $I_{OFF}$. Another possibility that should not be ruled out is that the Fermi level could be pinned inside the In$_{0.53}$Ga$_{0.47}$As bandgap due to the presence of a large $D_{it}$ arising from the high temperature activation anneal process.

### 2.5 Conclusion

We studied the effect of the implant activation anneal process on the S/D sheet resistance and gate oxide capacitance as part of the development of a “high-$k$ first + metal-gate last” In$_{0.53}$Ga$_{0.47}$As MOSFET TLM structures were fabricated as part of a Doehler DOE to investigate an experimental domain of 625°C to 725°C and 15 s to 45 s. While the $R_{sheet}$ model presented a minimum at 715°C for 32 s leading to a minimum $R_{sheet}$ value of (195.6 ± 3.4) Ω/□, the $ρ_{C}$ model was not found to be statistically significant due to a large error in the $ρ_{C}$ extraction. It is noted that TLM structures with a range of sub-micron spacing between the contacts would significantly reduce the error in the $ρ_{C}$ extraction and could yield a statistically significant $ρ_{C}$ model.

Physical analysis was also performed on the sample annealed at 675°C for 30 s (centre point of the experimental domain). The SIMS analysis showed that the activation anneal process did not involve Si ion diffusion within the p-In$_{0.53}$Ga$_{0.47}$As, while the TEM revealed the formation of characteristic loop defects that have a peak depth of approximately 50 nm. We speculate that these defects could have a significant effect on $R_{sheet}$ and $ρ_{C}$. Further investigations to correlate loop defect densities with the $R_{sheet}$ and $ρ_{C}$ degradation are required.
Figure 2.6: Capacitance-voltage (C-V) characteristics of the Pd/HfO$_2$ (8 nm)/Al$_2$O$_3$ (2 nm)/$p$-In$_{0.53}$Ga$_{0.47}$As/$p$-InP/SI-InP structures annealed for 30 s in N$_2$ at (a) 675°C and (b) 725°C. The unexpected $n$-type C-V behavior could result from a possible diffusion of unintentional $n$-type dopants from the substrate/epitaxial interface, in agreement with [28]. (c) Conductance-voltage (G-V) and C-V characteristics measured at a frequency of 100 kHz on Pd/HfO$_2$ (8 nm)/Al$_2$O$_3$ (2 nm)/$p$-In$_{0.53}$Ga$_{0.47}$As/$p$-InP/SI-InP structures annealed at 675°C, 700°C and 725°C for 30 s in N$_2$. 

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Figure 2.7: (a) Picture of a fabricated In$_{0.53}$Ga$_{0.47}$As MOSFET obtained with the “high-k first + metal-gate last” process. G, S, D, and B indicate the gate, source, drain, and body contacts, respectively. (b) Drain current ($I_d$) vs drain-source voltage ($V_{ds}$) for a 5-µm gate length Pd/HfO$_2$/In$_{0.53}$Ga$_{0.47}$As MOSFET for a gate voltage ($V_g$) varied from -2 V to 2 V with a step of 0.5 V.

The Pd/HfO$_2$/Al$_2$O$_3$/p-In$_{0.53}$Ga$_{0.47}$As/p-InP/SI-InP MOSCAPs subjected to activation annealing of 675°C to 725°C for 30 s presented reasonable leakage currents below $2.1 \times 10^{-8}$ A/cm$^2$ for electric fields of ~3 MV/cm. However, the C-V measurements (performed on p-type MOSCAPs) revealed an unexpected n-type C-V behavior, suggesting a possible diffusion of unintentional n-type dopants arising from the substrate/epitaxial interface. The dispersion of capacitance per decade of frequency in accumulation remained at a low value of 1.7% over the same temperature range, indicating that annealing did not involve the creation of a significant amount of oxide traps. However, the degradation of the C-V characteristics with increasing anneal temperature revealed a ~16% increase in $D_{it}$ for every 25°C increase within the studied temperature range of 675°C to 725°C.

A “high-k first + metal-gate last” In$_{0.53}$Ga$_{0.47}$As MOSFET was demonstrated. Although the 5-µm-channel-length device featured a reasonable maximum $I_d$ of 180 mA/mm at a $V_g$ of 2 V and a $V_{ds}$ of 2.5 V, a large $I_{OFF}$ was observed. This large $I_{OFF}$ could originate from (1) the possible diffusion of unintentional n-type dopants in the In$_{0.53}$Ga$_{0.47}$As/InP epitaxial layers during the MOVPE growth and/or during the S/D activation anneal process, leading to leakage paths between the source and drain terminals or (2) a high $D_{it}$ caused by the S/D activation anneal process and responsible for the pinning of the Fermi level inside the In$_{0.53}$Ga$_{0.47}$As bandgap, preventing the device from switching off.
Chapter 2. Source/Drain Activation and Impact on Gate Stack

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Chapter 2. Source/Drain Activation and Impact on Gate Stack


Chapter 3

Impact of Forming Gas Annealing on MOSFET Performance

3.1 Introduction

A major obstacle to the development of surface-channel In\(_{0.53}\)Ga\(_{0.47}\)As metal-oxide-semiconductor field-effect transistors (MOSFETs) is the integration of high-\(k\) gate oxides on the In\(_{0.53}\)Ga\(_{0.47}\)As surface with a sufficiently low density of interface traps, border traps and fixed oxide charges, as seen in section 1.2.1 (page 6). Various methods such as \((NH_4)_2S\) passivation [14], silicon inter-layer [5, 6], interface control layer [7, 8] and InP capping [9], have been explored to reduce defects in high-\(k\)/In\(_{0.53}\)Ga\(_{0.47}\)As structures. The use of a forming gas (H\(_2/N_2\)) anneal (FGA) which is well known for passivating \(Pb\)-like defects in SiO\(_2\)/Si and high-\(k\)/SiO\(_x\)/Si systems [10, 11], represents an alternative or complimentary approach for reducing defects in high-\(k\)/In\(_{0.53}\)Ga\(_{0.47}\)As structures subsequent to the gate oxide deposition.

Recent studies using metal-oxide-semiconductor capacitors (MOSCAPs) have shown that a FGA can reduce the fixed charge density in Al\(_2\)O\(_3\)/In\(_{0.53}\)Ga\(_{0.47}\)As systems [12, 13] and reduce the density of interface traps \((D_{it})\) near the In\(_{0.53}\)Ga\(_{47}\)As conduction band in HfO\(_2\)/n-In\(_{0.53}\)Ga\(_{47}\)As MOSCAPs [14]. However, results reported to date do not indicate any significant influence of FGA on the prominent donor-like defects near mid-gap [1].

In this chapter, we extend on the work reported to date on the effect of FGA on In\(_{0.53}\)Ga\(_{47}\)As MOSCAPs [12, 13] to investigate the impact of FGA on the performance of surface-channel In\(_{0.53}\)Ga\(_{47}\)As MOSFETs.

Since our preliminary In\(_{0.53}\)Ga\(_{47}\)As MOSFET indicated a large OFF-state current \((I_{OFF})\) (section 2.4, page 41) resulting from a possible diffusion of unintentional \(n\)-type dopants from the SI-InP substrate to the In\(_{0.53}\)Ga\(_{47}\)As channel during the metal-organic vapor phase epitaxy (MOVPE) growth and/or during the source and drain (S/D) activation anneal, we modified our
3.2 Samples preparation

Surface-channel MOSFETs (Figure 3.1) and MOSCAP were fabricated on a 2-μm-thick Zn-doped (4 × 10^{17} /cm^3) p-In_{0.53}Ga_{0.47}As layer grown on a 2-inch p+ InP wafer by MOVPE. A dedicated lithography mask set was designed for the fabrication of the devices (Appendix B). The In_{0.53}Ga_{0.47}As surface passivation prior to gate oxide deposition was an immersion in 10% (NH_4)_2S at room temperature for 20 min, which was found to be an optimum in terms of interface state reduction and for the suppression of native oxide formation [1, 2]. The transfer time to the atomic layer deposition (ALD) reactor after surface passivation was 3 to 5 min. A 10-nm-thick Al_2O_3 gate oxide film was formed by ALD using alternating pulses of trimethyl-aluminum [Al(CH_3)_3] (TMA) and H_2O precursors at 250°C. The S/D regions were selectively implanted device wafer structure and fabrication process flow in order to mitigate this issue. We used a much thicker (2 μm) In_{0.53}Ga_{0.47}As layer, replaced the SI-InP substrate by a p+ InP substrate and further reduced the thermal budget of the S/D activation anneal process.

Figure 3.1: Schematic cross-sectional diagram of a surface-channel In_{0.53}Ga_{0.47}As MOSFET with a 10-nm-thick ALD Al_2O_3 dielectric and a Pd gate. The nominal gate (L) is 1, 2, 3, 5, 10, 20 or 40 μm and the width (W) is 50 μm. The overlap of the Pd gate over the Si-implanted n^+ regions is 1.5 μm and the separation between the Pd gate contact and the source (S) or drain (D) contact is 4 μm.

\[ L = 1, 2, 3, 5, 10, 20, 40 \mu m / W = 50 \mu m \]
Chapter 3. Impact of Forming Gas Annealing on MOSFET Performance

Figure 3.2: TEM images (a) through the gate stack region of the MOSFET confirming the 10-nm Al₂O₃ gate oxide thickness and (b) through the gate overlap region, showing the implant defects in the Si-implanted n⁺ region. The TEM analysis was performed by M. Schmidt. (Tyndall National Institute)

with a Si dose of 1 × 10¹⁴ /cm² at 80 keV and 1 × 10¹⁴ /cm² at 30 keV. Based on the results obtained in Chapter 2, a rapid thermal anneal (RTA) process of 600°C for 15 s in a N₂ atmosphere was selected for the activation of the implant. A 140-nm-thick SiO₂ field oxide was formed by electron beam evaporation and liftoff to minimize the gate pad capacitance. Non-self-aligned ohmic contacts were defined by lithography, selective wet etching of the Al₂O₃ in dilute HF and electron beam evaporation of a Au (14 nm)/Ge (14 nm)/Au (14 nm)/Ni (11 nm)/Au (200 nm) metal stack. A 200-nm-thick Pd gate was defined by electron beam evaporation and liftoff. Tests confirmed the absence of delamination of the Pd metal following FGA. A 300°C for 30 min FGA was carried out in an open tube furnace.

The finished devices had a nominal gate length (L) of 1, 2, 3, 5, 10, 20, 40 µm with a 1.5 µm gate metal overlap over the Si-implanted S/D regions, 4-µm gate contact to source or drain contact separation and a 50-µm gate width (Figure 3.1). Relatively long channel length devices were intentionally selected for the study to allow the effect of the FGA process on the electrical properties of the In₀.₅₃Ga₄₇As MOSFETs to be examined in the absence of short channel effects.

3.3 Results and Discussion

3.3.1 Transmission Electron Microscopy Analysis of Gate Stack and Implanted Regions

Cross-sectional transmission electron microscopy (TEM) images through the gate oxide region and through the implanted area at the end of device fabrication are shown in Figure 3.2(a) and (b), respectively. Figure 3.2(a) confirms the 10 nm Al₂O₃ film thickness, which corresponds to
3.3 Results and Discussion

Figure 3.3: $I_d-V_{gs}$ obtained on 20-µm-gate-length and 50-µm-gate-width MOSFETs at $V_{ds} = 50$ mV before and after FGA. The MOSFETs feature a $V_T$ of -0.63 and 0.43 V before and after FGA, respectively. (b) Q-S C-V simulation of the Pd/Al2O3/p-In0.53Ga0.47As gate stack obtained using a Poisson-Schrödinger simulator [21]. The ideal $V_T$ of 0.7 V was obtained based on a Pd work function of 4.7 eV [21], a 10-nm-thick Al2O3 film with a $k$-value of 8.6, and a $p$-In0.53Ga0.47As doping level of $4 \times 10^{17}$ /cm$^3$.

the nominal value from the ALD process and a growth rate per cycle of 1 Å/cycle. There is no evidence of an interface oxide between the In0.53Ga0.47As surface and the Al2O3 layer, consistent with previous reports for the optimised (NH4)$_2$S process and subsequent ALD Al2O3 formation [1], and with the reported “self-cleaning” effect of ALD on GaAs [16-18] and on InGaAs [19] surfaces. Figure 3.2(b) shows the remaining implant defects in the gate overlap region after activation anneal and FGA, indicating that these two anneals are not sufficient to fully remove the defects caused by the Si implantation process.

3.3.2 Fixed Oxide Charge Passivation, Threshold Voltage Shift and OFF-State Leakage Reduction

Figure 3.3(a) shows the drain current ($I_d$) vs gate-to-source voltage ($V_{gs}$) characteristics at a drain-to-source voltage ($V_{ds}$) = 50 mV obtained on a 20-µm-gate-length and 50-µm-gate-width device before and after FGA. The threshold voltage ($V_T$) shifts from -0.63 V before FGA to 0.43 V after FGA. The negative $V_T$ before FGA indicates the presence of fixed positive charges within the Al2O3. Figure 3.3(b) shows a quasi-static (Q-S) capacitance-voltage (C-V) of the Pd/Al2O3/p-In0.53Ga0.47As gate stack obtained using a self consistent Poisson-Schrödinger

\[V_T\] is extracted using the linear extrapolation method.
The asymmetric shape of the simulated $Q-S-C-V$ response, due to the very low density of states of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ conduction band, is not experimentally observed. This absence of asymmetry has been attributed to the presence of additional traps located at energy levels aligned with the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ conduction band [22]. In the simulation, the metal work function ($W_f$) of Pd on $\text{Al}_2\text{O}_3$, the $\text{Al}_2\text{O}_3$ oxide thickness ($t_{ox}$) and $C_v$-value and the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ $p$-type dopant density ($N_d$) were set to 4.7 eV [21], 10 nm, 8.6 [23] and $4 \times 10^{17}$ /cm$^3$, respectively. Considering an ideal $V_T$ of 0.7 V [Figure 3.3 b] and an oxide capacitance ($C_{ox}$) of $7.6 \times 10^{-7}$ F/cm$^2$, we calculated an equivalent density of fixed positive oxide charge at the $\text{Al}_2\text{O}_3/p-\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface before and after FGA of $6.3 \times 10^{12}$ /cm$^2$ and $1.3 \times 10^{12}$ /cm$^2$, respectively. Recent studies of $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSCAPs over $n$- and $p$-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ prior to FGA reported fixed positive oxide charge densities of $\sim 1 \times 10^{19}$ /cm$^3$ distributed throughout the $\text{Al}_2\text{O}_3$ layer [12]. A density of $\sim 1 \times 10^{19}$ /cm$^3$ throughout a 10-nm-thick $\text{Al}_2\text{O}_3$ film corresponds to an equivalent surface density at the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface of $\sim 1 \times 10^{13}$ /cm$^2$, which is consistent with our pre-FGA value of $6.3 \times 10^{12}$ /cm$^2$.

The origin of the fixed positive charge has been assigned to $\text{Al}$ dangling bonds based on theoretical modelling [13], and its reduction following the FGA process is consistent with hydrogen passivation of the dangling bond sites in the $\text{Al}_2\text{O}_3$.

The fixed charge within the $\text{Al}_2\text{O}_3$ gate oxide can have a significant impact on the MOSFET behaviour. We calculated that, for an $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ $N_d$ of $4 \times 10^{17}$ /cm$^3$, fixed positive charge densities in excess of $2 \times 10^{12}$ /cm$^2$ are sufficient to create an inversion layer at the $\text{Al}_2\text{O}_3/p-\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface. This indicates that the fixed positive oxide charge density of $6.3 \times 10^{12}$ /cm$^2$ before FGA is sufficient to invert the $p$-$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface, while the fixed positive oxide charge density of $1.3 \times 10^{12}$ /cm$^2$ after FGA is not. The strong inversion layer before FGA can be modulated in the region under the Pd gate. However, this inversion charge is also present in the region outside the area defined by the gate, and is subsequently referred to as the “peripheral inversion region”. We suggest that the high $I_{OFF}$ and poor subthreshold swing (SS) of the MOSFET before FGA [Figure 3.4 a] are due to the presence of a peripheral inversion region that cannot be controlled by the gate voltage. The log $I_{OFF}/V_{gs}$ characteristics measured at 20°C and -50°C before FGA [Figure 3.4 a] reveals that the $I_{OFF}$ ($I_{gs}$ at $V_{gs}>0$) is only weakly temperature dependent, which further indicates that the $I_{OFF}$ before FGA is due to the

1. Though the $8.6$ for $\text{Al}_2\text{O}_3$ was obtained from the slope of the capacitance equivalent thickness in accumulation vs $t_{ox}$ for $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ metal-oxide-semiconductor (MOS) structures with $t_{ox}$ ranging from 5 to 20 nm. These measurements were performed by Y. Y. Gomeniuk (Lashkaryov Institute of Semiconductor Physics, Kiev, Ukraine).

2. For an $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ $N_d$ of $4 \times 10^{17}$ /cm$^3$, the maximum depletion width is 50 nm (where the intrinsic carrier density ($n_i$) for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ is taken as $6.3 \times 10^{11}$ /cm$^3$ [23]). Hence, the total density of charge resulting from the ionized acceptor at the onset of inversion is $2 \times 10^{12}$ /cm$^2$. Positive oxide charge densities in $\text{Al}_2\text{O}_3$ in excess of $2 \times 10^{12}$ /cm$^2$ will result in inversion of the $p$-$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface.
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Figure 3.4: Comparison of the 20°C and -50°C log \( I_d-V_{gs} \) measured at \( V_{ds} = 50 \text{ mV} \) on 20-\( \mu \text{m-gate-length} \) and 50-\( \mu \text{m-gate-width} \) MOSFETs (a) before and (b) after FGA. The log \( I_d-V_{gs} \) values are shown with matched gate overdrive (\( V_{gs}-V_T \)).

peripheral inversion region. It is noted that the formation of a peripheral inversion depends on the substrate doping concentration, the oxide capacitance, and the density and sign of the fixed oxide charge. Moreover, a high leakage current due to a peripheral inversion region will not be observed on a “ring-gate” MOSFET where the gate encircles the drain and obviates the need for isolation [25]. Figure 3.4(b) shows a \( I_{OFF} \) reduction of three orders of magnitude (ON-state-to-OFF-state current ratio (\( I_{ON}/I_{OFF} \)) \( \sim 10^4 \)) due to the removal of the peripheral inversion region following the FGA process. The temperature dependence of the \( I_{OFF} \) after FGA is evident and the \( I_{ON}/I_{OFF} \) at -50°C is \( \sim 10^6 \).

Following the FGA process, we obtained a SS of 150 mV/dec. This SS yielded a \( D_{it} \) value in the upper part of the In\(_{0.53}\)Ga\(_{47}\)As bandgap of \( \sim 5.8 \times 10^{12} \text{ cm}^2 \text{eV} \), in line with the literature values reported for the Al\(_2\)O\(_3\)/In\(_{0.53}\)Ga\(_{47}\)As system [Figure 1.8(b), page 11]. It is noted that for the pre-FGA case, the SS is dominated by the peripheral leakage current and cannot be used for interface state density determination.

3.3.3 MOSCAPs Behaviour and Density of Interface Traps

Figure 3.5(a) and (b) show the multi-frequency (M-F) C-V characteristics of Pd/Al\(_2\)O\(_3\)/p-In\(_{0.53}\)Ga\(_{47}\)As MOSCAPs before and after the FGA. These MOSCAPs are adjacent to the MOS-
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Figure 3.5: Multi-frequency (M-F) capacitance-voltage (C-V) characteristics of Pd/Al$_2$O$_3$/p-In$_{0.53}$Ga$_{0.47}$As MOSCAPs measured from 100 Hz to 100 kHz (a) before and (b) after FGA. The $V_T$ of the corresponding MOSFETs is highlighted on the C-V characteristics.

MOSFETs on the same wafer. The passivation of fixed positive charges within the Al$_2$O$_3$ after FGA results in a C-V shift consistent with the shift observed on the $I_d$-$V_{gs}$ characteristics shown in Figure 3.3(a). The $V_T$ of the corresponding MOSFETs is highlighted in Figure 3.5(a) and (b). The comparison of the 100-Hz C-V responses at the on-set of inversion shows a steeper slope after FGA indicating a reduction in $D_{it}$ near the p-In$_{0.53}$Ga$_{0.47}$As conduction band, consistent with [14].

There has been debate over the expected M-F C-V response of In$_{0.53}$Ga$_{0.47}$As MOSCAPs in inversion and the method to identify genuine surface inversion [26]. The availability of the MOSCAPs and adjacent MOSFETs on the same wafer allows the $V_T$ obtained from the MOSFETs to be identified on the M-F C-V response of the Pd/Al$_2$O$_3$/p-In$_{0.53}$Ga$_{0.47}$As MOSCAPs. In addition, the M-F C-V response for gate voltage ($V_g$) $> V_T$ illustrates the behaviour of a Pd/Al$_2$O$_3$/p-In$_{0.53}$Ga$_{0.47}$As MOSCAP beyond inversion. Figure 3.3(a) and (b) show that, beyond inversion, the capacitance as a function of applied voltage increases and then acquires an approximately constant value. The value of the capacitance in inversion increases with decreasing frequency up to a maximum value set by the oxide capacitance. This frequency dependent C-V behaviour has also been obtained following an optimized (NH$_4$)$_2$S treatment of n- and p-In$_{0.53}$Ga$_{0.47}$As prior to ALD Al$_2$O$_3$ deposition [3].

Figure 3.6 shows the parallel conductance ($G_p$) normalized to angular frequency ($\omega$) plotted as a function of frequency ($f$) for a selected $V_g$. A clear $G_p$ peak was observed for $V_g = -1.9$ V before FGA and $V_g = -0.8$ V after FGA. Considering the $V_T$ shift induced by the FGA and
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Figure 3.6: Normalized parallel conductance ($G_p/\omega$) vs frequency ($f$) obtained with the conductance method [27, 28] for a 10-nm-thick Al$_2$O$_3$ film with a $k$-value of 8.6. The $D_{it}$ extraction at $V_g = -1.9$ V before FGA and at $V_g = -0.8$ V after FGA yielded the same value of $\sim 4.0 \times 10^{12}$ /cm$^2$·eV.
that both $V_g$ values corresponded to the same $V_g - V_T$ of $\sim 1.25$ V, we assumed that the Fermi level in both cases was at the same energy position. The values of $D_{it}$ and trap capture time constant ($\tau$) were obtained using the conductance method [27, 28]. The FGA did not reduce the $D_{it}$ as values of $\sim 4.0 \times 10^{12} \text{ /cm}^2\text{eV}$ were extracted before and after FGA. These $D_{it}$ values are in reasonable agreement with the $D_{it}$ of $\sim 5.8 \times 10^{12} \text{ /cm}^2\text{eV}$ extracted from the SS of the MOSFETs post FGA. The FGA did not have a significant impact on $\tau$ as values of $\sim 48.5 \mu\text{s}$ and $\sim 43.8 \mu\text{s}$ were obtained before and after FGA, respectively.

### 3.3.4 Transconductance, Drive Current and Effective Mobility Improvement

Figure 3.7(a) compares the transconductance ($g_m$) vs gate overdrive ($V_{gs} - V_T$) obtained on 20-µm-gate-length and 50-µm-gate-width MOSFETs before and after FGA. Whereas the peak $g_m$ increases by 29% after FGA, the higher field values of $g_m$ only slightly improve with FGA. Figure 3.7(b) shows the drain current versus drain voltage ($I_d - V_{ds}$) output characteristics obtained for an In$_{0.53}$Ga$_{47}$As MOSFET with a gate length of 20 µm and a gate width of 50 µm before and after FGA. The device exhibits well behaved output characteristics with drain current saturation for $V_{ds} > V_{gs} - V_T$. The drive current at a 2-V gate overdrive was 14.8 mA/mm before FGA and 18.5 mA/mm after FGA, representing a 25% improvement with FGA. These drive current values are comparable to, or slightly higher, than other published values for surface channel In$_{0.53}$Ga$_{47}$As MOSFETs [31, 29], assuming drive current scaling with $1/L$. 63
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Figure 3.8: Effective mobility ($\mu_{eff}$) versus inversion charge density ($N_{inv}$) before and after FGA. The peak $\mu_{eff}$ increases by 15% after FGA. (Inset) 2-MHz gate-to-channel $C_{gc}$ split C-V characteristics before and after FGA.

Figure 6.17 shows the effective mobility ($\mu_{eff}$) as a function of the inversion-charge density ($N_{inv}$) extracted using the $I_d - V_{gs}$ characteristics (Figure 3.3(a)) and the 2-MHz gate-to-channel split C-V characteristics (inset Figure 6.17). The parasitic overlap capacitances were removed from the measured gate-to-channel capacitance ($C_{gc}$) using the method reported in [30]. Devices with $L$ ranging from 1 $\mu$m to 40 $\mu$m were used to extract the source and drain series resistance ($R_{SD}$) values used in the $\mu_{eff}$. $R_{SD}$ values were evaluated at $V_{ds} = 50$ mV to ensure devices operation in the linear region. The devices featured a $R_{SD}$ of 235 $\Omega$ and 103 $\Omega$ before and after FGA, respectively. The peak $\mu_{eff}$ increased from 650 cm$^2$/V.s to 750 cm$^2$/V.s with FGA. This 15% improvement in the peak $\mu_{eff}$ after FGA is consistent with a reduction in the positive oxide charge, which reduces the Coulomb scattering component. A reduction in the $D_{it}$ near the In$_{0.53}$Ga$_{47}$As conduction band, as suggested by the C-V characteristics before and after FGA (Figure 3.5(a) and (b)) and consistent with [14], could also contribute to the increase in peak $\mu_{eff}$.

Figure 3.9 shows that the extracted peak $\mu_{eff}$ after FGA is comparable to other published values for surface-channel In$_{0.53}$Ga$_{47}$As MOSFETs [29, 31-34]. It is noted that the In$_{0.53}$Ga$_{47}$As channel $N_d$ of $4 \times 10^{17}$ /cm$^3$ used in this study is four to twenty times higher than the values used in the comparative publications. The published experimental values for the peak $\mu_{eff}$ in surface-channel In$_{0.53}$Ga$_{47}$As MOSFETs remain well below the theoretical values expected for reasonable values of fixed oxide charge, interface traps and surface roughness, where peak values of $\sim$4000 cm$^2$/V.s are calculated [35]. This discrepancy could relate to the approach typically
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Figure 3.9: Extracted peak effective mobility ($\mu_{\text{eff}}$) vs $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel doping ($N_a$) compared to literature values obtained in [5, 29, 31-34]. GGO stands for gallium gadolinium oxide.

employed to determine $\mu_{\text{eff}}$. Indeed, for the calculation of $N_{\text{inv}}$ on the $x$-axis of Figure 6.17, it is assumed that the integral of $C_{gc}$ for $V_g > V_T$ yields $N_{\text{inv}}$ and is unaffected by trapped charges in interface and oxide traps. However, a number of recent publications have reported the presence of interface traps [22, 36, 37] and oxide traps [37-40] located at energy levels aligned with the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ conduction band. In this case, the integral of $C_{gc}$ will contain contributions from both free charge and trapped charge, which will result in an overestimation of $N_{\text{inv}}$ and a corresponding underestimation of $\mu_{\text{eff}}$. No corrections for the effect of bulk oxide charge trapping have been applied in this work in order to allow a fair comparison with the $\mu_{\text{eff}}$ values reported in [31, 29, 31]. However, a detailed study of this issue will be presented in Chapter 4 and Chapter 5.

3.3.5 Junction Leakage Reduction

The FGA also improves the current-voltage behaviour of the source or drain-to-substrate $n^+/p$ junctions. Figure 3.10(a) shows the current-voltage (I-V) characteristics for the $n^+/p$ junctions before and after FGA. The saturation current in reverse bias is reduced by more than two orders of magnitude as a result of the FGA. The measurement temperature (223 K to 293 K) and applied bias (0.1 V to 0.5 V) dependence of the $n^+/p$ junction characteristics before and after the FGA is shown in Figure 3.10(b). The activation energy ($E_a$) extrapolated to zero bias from Figure 3.10(b) yields values of 0.37 eV and 0.40 eV before and after the FGA, respectively. The
3.4 Conclusion

We demonstrated that a 300°C, 30 min FGA dramatically improved the performance of surface-channel In$_{0.53}$Ga$_{0.47}$As MOSFETs with Al$_2$O$_3$ as gate dielectric. The FGA process reduced the density of fixed positive charges in the Al$_2$O$_3$, which removed a parasitic peripheral inversion region, and resulted in an increase in $I_{ON}/I_{OFF}$ by three orders of magnitude. The FGA improved the $g_m$, drive current and peak $I_{eff}$ by 29%, 25% and 15%, respectively. C-V measurements of MOSCAPs revealed that the FGA reduced $D_d$ near the In$_{0.53}$Ga$_{0.47}$As conduction band but did not reduce the mid-gap $D_d$. A reduction of two orders of magnitude was also observed in the reverse bias leakage current density in the Si-implanted In$_{0.53}$Ga$_{0.47}$As $n^+/p$ junctions in the S/D regions of the MOSFETs, consistent with the passivation of mid-gap states in the In$_{0.53}$Ga$_{0.47}$As by the FGA.
The fabricated devices featured sufficient electrical performance to be used as text vehicles for the development of alternative electrical characterization techniques, which will be presented in Chapter 4 and Chapter 5.
Bibliography


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Chapter 4

Analysis of MOS Gate Stack Defects

4.1 Introduction

Although InGaAs metal-oxide-semiconductor field-effect transistors (MOSFETs) with performance approaching that of state-of-the-art Si devices have already been demonstrated (see Table 1.2, page 5), further performance improvements are still required for potential introduction of InGaAs devices into production. Considering the case of the high-$k$ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ metal-oxide-semiconductor (MOS) system, the density of interface traps ($D_{it}$) located in the middle of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ bandgap, is typically reported to be in the range of low-10$^{11}$ to mid-10$^{13}$/cm$^2$eV (see Figure 1.7, page 10). Moreover, recent reports have also indicated the presence of both interface traps [13] and border traps [1, 4, 5] aligned with the conduction band.

A better understanding and control of interface and border traps could enable to significantly improve device performance. The study of the traps located throughout the full energy range swept by the Fermi level during device operation, might enable to achieve this goal. Moreover, knowledge of the energy distribution of interface and border traps is important as any specific features of the extracted surface-equivalent density of interface and border trap ($D_{\text{trap}}$) vs energy ($E$) profile can be compared to theoretical models of defect energies in order to identify the physical origin of the traps [6].

One approach to obtain the $D_{\text{trap}}(E)$ profile of a high-$k$ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ system is to compare the quasi-static (Q-S) capacitance-voltage (C-V) response measured on a metal-oxide-semiconductor capacitor (MOSCAP) to a theoretical Q-S C-V response [2]. An alternative approach is to use $n$ and $p$-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSCAPs to examine the $D_{\text{trap}}$ profile in the upper and lower portions of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ bandgap, respectively [7].

The availability of surface-channel high-$k$ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFETs opens up new possibilities for investigating interface and border traps when compared to high-$k$ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSCAPs. Martens et al. developed a “full conductance” method for surface-channel III-V
Figure 4.1: Full gate capacitance ($C_g$) vs gate voltage ($V_g$) measurement setup, where the gate contact (G) of the MOSFET is connected to the “high” of the impedance meter and the source (S), drain (D) and substrate contacts are shorted together and connected to the “low”.

First, we will compare a measured full-gate capacitance ($C_g$) vs gate voltage ($V_g$) characteristic to a theoretical (ideal) high-frequency (H-F) C-V characteristic calculated with a self-consistent Poisson-Schrödinger solver [13] in order to extract a surface-equivalent density of fixed positive oxide charge ($N^+$) along with a $D_{trap}[E]$ integrated across the In$_{0.53}$Ga$_{0.47}$As bandgap. Then, we will demonstrate an alternative $D_{trap}[E]$ extraction method based on the fitting of the measured $C_g[V_g]$ characteristic and its corresponding Maserjian Y-function [14, 15] by introducing a $D_{trap}[E]$ into the self-consistent Poisson-Schrödinger calculations.
4.2 Full Gate Capacitance Measurement

The $C_g V_g$ characteristic of the Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOSFET was obtained using a measurement configuration where the gate contact is connected to the “high” of the impedance meter and the source, drain and substrate contacts are shorted together and connected to the “low” (Figure 4.1). The advantage of this measurement, when compared to the $C-V$ measurement of a MOSCAP, is that for the condition of strong inversion the source and drain areas supply the inversion charge at the Al$_2$O$_3$/p-In$_{0.53}$Ga$_{0.47}$As interface, allowing a full $C_g V_g$ response to be obtained.

A frequency ($f$) of 1 MHz and a temperature ($T$) of -50°C were selected in order to minimize the capacitance response associated with the presence of interface traps and border traps and obtain the approximation of the true H-F $C_g V_g$ response required for the fitting. Values of $f$ higher than 1 MHz were avoided to prevent distortion of the inversion part of the $C_g V_g$ characteristic due to parasitic channel resistance effects [10]. A $T$ of -50°C was selected as it represented the lowest $T$ available on the probe station.

The experimental $C_g V_g$ characteristic was corrected for the parasitic capacitances associated with the gate overlap (Figure 3.1) and gate pad using the method reported in [17].

4.3 Maserjian Y-Function

The Maserjian Y-function applied to a $C_g V_g$ characteristic is expressed as follows [14]:

$$Y = \frac{1}{C_g^3} \frac{dC_g}{dV_g}$$  \hspace{1cm} (4.1)

Figure 4.2a) and (b) show a theoretical (ideal) p-type $C_g V_g$ characteristic and its corresponding Maserjian Y-function, respectively. The Maserjian Y-function is generally used to extract key MOS parameters such as the threshold voltage ($V_T$), the p-type dopant density ($N_a$) and the flat-band voltage ($V_{fb}$) without prior knowledge of the oxide capacitance ($C_{ox}$) [14, 15]. This is particularly useful in the analysis of high-$k$ III-V MOS systems as the low density of states in the conduction band [18] together with issues of traps with energies aligned with the conduction band [19], make the extraction of $C_{ox}$ particularly difficult.

First, the Maserjian Y-function features a sharp peak at $V_T$ [Figure 4.2b)]. Then, the $Y_{min}$ plateau observed in depletion can be used to extract $N_a$ and $V_{fb}$ using Equations 4.2 and 4.3, respectively:

$1$The same process is involved in a conventional gate-to-channel capacitance ($C_{gc}$) split $C-V$ measurement [16].

$2$It is noted that lower temperature measurements at 77 K or below may be required to obtain the true H-F $C_g V_g$ response.
Figure 4.2: Example of theoretical (ideal) p-type $C_g$-$V_g$ characteristic (a) and corresponding Maserjian Y-function (b). The threshold voltage ($V_T$) and flat-band voltage ($V_{fb}$) are obtained from the peak of the Maserjian Y-function and Equation 4.3 respectively. $V_T$ and $V_{fb}$ delimitate the accumulation (acc.), depletion and inversion (inv.) regions. Knowing $V_{fb}$ allows to extract the flat-band capacitance ($C_{fb}$). The grey shaded areas represent the In$_{0.53}$Ga$_{0.47}$As bandgap.
4.4 Results and Discussion

4.4.1 Integrated Fixed Oxide Charge and Integrated Interface Trap Density

The $C_g V_g$ characteristic measured at $f = 1$ MHz and $T = -50^\circ$C is shown in Figure 4.3. Considering the Shockley-Read-Hall (SRH) statistics [19] and assuming an interface trap capture cross section ($\sigma$) of $\sim 1 \times 10^{-15}$ cm$^2$ [20], the $T$ of $-50^\circ$C and $f$ of 1 MHz should remove the interface defect capacitance response over an energy range relative to the In$_{0.53}$Ga$_{0.47}$As valence band edge ($E_V$) going from $E - E_V = 0.17$ eV to 0.63 eV. Also plotted in Figure 4.3 is the theoretical (ideal) H-F $C_g V_g$ response for the case of no interface/border traps, or fixed oxide charges. The theoretical $C_g V_g$ response was obtained by solving the Poisson equation in depletion [21] and by...
self-consistently solving the Poisson-Schrödinger equations in inversion, including quantization in all valleys [22]. In the theoretical calculations, the metal work function ($W_f$) for Pd on Al2O3, the Al2O3 film thickness and $E_g$ value, and the p-In0.53Ga0.47As doping were set to 4.7 eV [23], 10 nm (see cross-sectional transmission electron microscopy (TEM) image shown in Figure 3.2(a), page 57), 8.6 [24] and $3.3 \times 10^{17}/\text{cm}^3$ (obtained from measured minimum capacitance), respectively. The measured $C_g V_g$ can then be compared to the theoretical (ideal) $C_g V_g$ to highlight the impact of fixed oxide charges and interface/border traps.

Firstly, it is clear from Figure 4.3 that the experimental threshold voltage ($V_{T\text{exp}}$) is shifted in the negative direction relative to the theoretical threshold voltage ($V_{T\text{theo}}$), indicating the presence of positive fixed charge in the Al2O3. The magnitude of the difference between the $V_{T\text{theo}}$ and $V_{T\text{exp}}$ ($\Delta V_T$) yields a $N^+$ which is given by:

$$N^+ = C_{ox} \times \frac{\Delta V_T}{q} \quad (4.4)$$

where, $\Delta V_T = V_{T\text{theo}} - V_{T\text{exp}}$. Based on the $\Delta V_T$ obtained from Figure 4.3, a $N^+$ of $1.2 \times 10^{12}/\text{cm}^2$ is obtained, in close agreement with the results presented in Sub-section 3.3.2 (page 58) and consistent with previous reports [25, 26]. As already mentioned in Sub-section 1.2.1.3 (page 14), the Al2O3/In0.53Ga0.47As system features a negative fixed charge located at the Al2O3/In0.53Ga0.47As interface along with a positive fixed charge distributed throughout the thickness of the Al2O3 film. It is therefore important to point out that the $N^+$ calculated in Equation 4.4 is a surface-equivalent density of fixed oxide charge in units $/\text{cm}^2$ as it represents the net fixed charge integrated across the interface and oxide thickness.

Secondly, the experimental characteristic is stretched out from $V_{T\text{exp}}$ towards the experimental flat-band voltage ($V_{fb\text{exp}}$) in comparison to the theoretical response [Figure 4.3]. This stretch out is attributed to the presence of interface traps (and possibly border traps) located within the In0.53Ga0.47As bandgap. The experimental and theoretical values of $V_T$ and $V_{fb}$ as identified in Figure 4.3 can be used to estimate the integrated $D_{\text{trap}}$ across the In0.53Ga0.47As bandgap in units $/\text{cm}^2$. For In0.53Ga0.47As with a bandgap ($E_g$) of $\sim 0.75$ eV and a $N_a$ of $3.3 \times 10^{17}/\text{cm}^3$, the conditions of flat band and inversion correspond to Fermi energy ($E_f$) positions at the Al2O3/In0.53Ga0.47As interface of $E_f - E_V = 0.04$ eV and $E_f - E_V = 0.71$ eV, respectively. This indicates that the majority of the In0.53Ga0.47As bandgap is swept as $V_g$ goes from $V_{T\text{exp}}$ to $V_{fb\text{exp}}$. The approach presented here expands on the method reported in [26], where the experimental flat band conditions in n- and p-doped Al2O3/In0.53Ga0.47As MOS structures were used to evaluate the integrated $D_{\text{trap}}$ across the In0.53Ga0.47As bandgap. The availability of a four terminal transistor allows the evaluation of the integrated $D_{\text{trap}}$ value with a single device structure. The additional gate voltage required to sweep from $V_{T\text{exp}}$ to $V_{fb\text{exp}}$ in the experimental curve compared to the theoretical curve is directly related to the integrated $D_{\text{trap}}$ across the
In\textsubscript{0.53}Ga\textsubscript{0.47}As bandgap, as:

\[ D_{\text{trap}} = C_{ox} \times \frac{(V_{fb}^{\text{exp}} - V_{fb}^{\text{theo}}) - (V_{T}^{\text{exp}} - V_{T}^{\text{theo}})}{q} \]  

(4.5)

where \( V_{fb}^{\text{theo}} \) is the theoretical flat-band voltage. From Figure 4.3, this yields a value of \( D_{\text{trap}} = 1.2 \times 10^{13} \) /cm\(^2\), which represents the integrated \( D_{\text{trap}}(E) \) from the flat band condition \((E_{F}-E_{V}) = 0.04 \) eV) to the onset of inversion \((E_{F}-E_{V}) = 0.71 \) eV).

### 4.4.2 Band Bending and Trap Density Profile

Our approach to obtaining the \( D_{\text{trap}}(E) \) is based on the fitting of the experimental \( C_{g}V_{g} \) characteristic using a self-consistent Poisson-Schrödinger solver accounting for fixed oxide charge and interface/border traps. To assist with the fitting process, we used the Maserjian Y-function. Figure 4.4 illustrates the four steps required to obtain a good fit.

Starting with a theoretical (ideal) H-F \( C_{g}V_{g} \) characteristic [Figure 4.4(a)] and corresponding Maserjian Y-function [Figure 4.4(b)], the \( N^+ \) of \( 1.2 \times 10^{12} \) /cm\(^2\) obtained in Section 4.4.1 is introduced in the H-F model in order to align the \( V_{fb}^{\text{theo}} \) to the \( V_{T}^{\text{exp}} \) [Figure 4.4(c) and (d)]. It is clear from Figure 4.4(c) that the experimental \( C_{g}V_{g} \) characteristic is significantly stretched out over the 0.5 V to -3.5 V gate bias range compared to the calculated \( C_{g}V_{g} \) characteristic.

This stretch out is attributed to the effect of traps located in the In\textsubscript{0.53}Ga\textsubscript{0.47}As bandgap. In Figures 4.4(e) and (f), a \( D_{\text{trap}}(E) \) is introduced in the H-F model in order to account for the stretch out of the experimental \( C_{g}V_{g} \) characteristic. It is noted that the Maserjian Y-function was found very useful at this stage to match the stretched out over the 0.5 V to -3.5 V gate bias range [inset Figure 4.4(f)] and fine tune the \( D_{\text{trap}}(E) \) across the In\textsubscript{0.53}Ga\textsubscript{0.47}As bandgap. Figure 4.4(e) shows that the the experimental capacitance in inversion exceeds the theoretical maximum value. This observation is consistent with the presence of interface traps [H3] and/or border traps [H4] at energy levels aligned with the In\textsubscript{0.53}Ga\textsubscript{0.47}As conduction band, providing an additional capacitance in parallel with the inversion capacitance. The \( C_{g}V_{g} \) characteristics shown in Figure 4.5 indicate that very little dispersion in capacitance in inversion is observed over a range of \( f \) going from 1 kHz to 1 MHz at \( T = 292 \) K and for \( f \) going from 292 K to 78 K at \( f = 1 \) MHz. This suggests that it is not possible to “freeze-out” the effect of traps at a \( f = 1 \) MHz and \( T = -50^\circ \) C in the inversion region of the \( C_{g}V_{g} \) characteristic. This result is consistent with the inversion capacitance exceeding the theoretical maximum value and indicates that the inversion region of the \( C_{g}V_{g} \) characteristic cannot not be fitted with the H-F model.

\(^{3}\)In the H-F model, the introduction of a \( D_{\text{trap}}(E) \) induces a stretch out of the \( C_{g}V_{g} \) characteristic along the x-axis but no stretch out along the y-axis (no trap capacitance is added).

\(^{4}\)These measurements were performed on devices obtained with the same fabrication process flow but from a different batch. Although the devices featured slightly different electrical performance, the point made relative to the lack of dispersion in capacitance in strong inversion with \( f \) and \( T \) remains valid.
Figure 4.4: Illustrating the four steps in the fitting of the experimental $C_g-V_g$ (a, c, e, g) and corresponding Maserjian Y-function (b, d, f, h). (a-b) theoretical (ideal) high-frequency (H-F) model, (c-d) H-F model with fixed oxide charge ($N^+$), (e-f) H-F model with $N^+$ and trap energy profile [$D_{trap}(E)$], and (g-h) spliced H-F model in depletion with quasi-static (Q-S) model in inversion, including $N^+$ and $D_{trap}(E)$. $V_{fb}$ and $V_T$ indicate the experimental flat-band and threshold voltages, respectively. The fitting was performed by T. P. O'Regan (Tyndall).
4.4. Results and Discussion

Figure 4.5: Gate-to-channel capacitance ($C_{gc}$) vs gate voltage ($V_g$) measured over a range of frequency ($f$) going 1 kHz to 1 MHz for a fixed temperature ($T$) of 292 K and at a $f$ of 1 MHz and a $T$ of 78 K. Low capacitance dispersion with $f$ and $T$ is observed in inversion ($V_g > 0.5$ V).

even with the introduction of a $D_{trap}[E]$ extending into the In$_{0.53}$Ga$_{0.47}$As conduction band. As a consequence, the inversion part of the curve is fitted with the Q-S self-consistent Poisson-Schrödinger model including a $D_{trap}[E]$ profile extending into the In$_{0.53}$Ga$_{0.47}$As conduction band. The resulting experimental and theoretical $C_{gc}$-$V_g$ responses and the corresponding Maserjian Y-functions are shown in Figure 4.4(g) and (h), respectively.

Figure 4.6(a) shows the extracted experimental band bending $E-E_V$ vs $V_g$ profile along with the profile of a theoretical (ideal) device. A marked degradation of the band bending efficiency is observed in the lower part of the In$_{0.53}$Ga$_{0.47}$As bandgap as well as in the In$_{0.53}$Ga$_{0.47}$As conduction band. The corresponding $D_{trap}[E]$ profile presents three main features [Figure 4.6(b)]:

1. A large density of donor (+/0) traps extending from the In$_{0.53}$Ga$_{0.47}$As valence band into the lower part of the In$_{0.53}$Ga$_{0.47}$As bandgap is observed. While our method can reveal the electrical nature of the traps (i.e.: donor or acceptor), further analysis is required to state about the physical nature of the traps (i.e.: interface traps or border traps).

2. A distribution of donor (+/0) traps peaking at $1.5 \times 10^{13} / \text{cm}^2 \cdot \text{eV}$ and centred at 0.36 eV above the In$_{0.53}$Ga$_{0.47}$As valence band edge (mid-gap) is also observed. This peak, associated with the presence of interface traps in [2, 10], is not always reported. Indeed, the $D_{trap}[E]$ profiles reported in [2, 24] show a monotonic increase from the In$_{0.53}$Ga$_{0.47}$As conduction band towards the valence band edge. It is possible that, in these works, a broader
Figure 4.6: (a) Comparison of the band bending $E-E_V$ vs $V_g$ profile obtained with the fitting of the $C_g-V_g$ characteristic and Maserjian $Y$-function to the profile obtained for a theoretical (ideal) device. (b) Trap density vs energy profile obtained from the fitting of the Maserjian $Y$-function and $C_g-V_g$ characteristic. The blue solid line and the red short dash line represent donor-type (+/0) and acceptor-type (0/-) trap density profiles, respectively. The donor-type trap density profile suggests the presence of two components, which are highlighted as two Gaussian distributions (blue short dot lines). The grey shaded areas represent the In$_{0.53}$Ga$_{0.47}$As bandgap.
feature extending from the valence band into the bandgap could prevent the observation of a clear peak around the mid-gap.

3. A broad feature extending into the In$_{0.53}$Ga$_{0.47}$As conduction band, acquiring a density of $\sim 2.5 \times 10^{13} \text{ cm}^{-2} \text{ eV}$ at 0.3 eV above the In$_{0.53}$Ga$_{0.47}$As conduction band edge ($E_C$).

This density value is in very close agreement with Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOS structures reported in [2], and the case of the Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOS with an (NH$_4$)$_2$S surface preparation reported in [3].

4.4.3 Comparison with Conventional Methods

In this subsection, the data obtained using the fitting of the $C_g-V_g$ characteristic and Maserjian Y-function (Figure 4.6) is compared to the results obtained with conventional methods such as the Berghlund integral [28], the Terman method [29], the high-low method [30], and the full conductance method [8]. It is important to note here that these methods were only applied after the data extraction based on the fitting the $C_g-V_g$ and Maserjian Y-function was performed, indicating that the extraction process was not biased by any preliminary analysis.

Figure 4.7(a) compares the band bending vs $V_g$ obtained using the fitting of the $C_g-V_g$ and Maserjian Y-function, the Terman method [29] and the Berghlund integral [28]. While the data used with the Terman method is the same as that used for the fitting (i.e.: $C_g-V_g$ measured at $f = 1 \text{ MHz and } T = -50^\circ\text{C}$), the data used in the calculation of the Berghlund integral is a $C_g-V_g$ characteristic measured at $f = 200 \text{ Hz and } T = 25^\circ\text{C}$ (not shown). Excellent agreement is obtained between the fitting method and the Terman method. However, a significant discrepancy between the Berghlund integral and the other methods is observed. For $V_g$ going from 0.4 V to -0.4 V, the Berghlund integral indicates a less efficient band bending than the other methods. This could be attributed to the fact that the $D_{trap}$ response near the band edges could not be “frozen out” at $f = 1 \text{ MHz and } T = -50^\circ\text{C}$, leading to an overestimation of the band bending efficiency near the band edges with the methods relying on an estimate of the H-F $C_g-V_g$ response (i.e.: fitting method and Terman method), consistent with [31]. For $V_g > -0.4$ V, the Berghlund integral severely overestimates the band bending efficiency, suggesting that the $f$ of 200 Hz is not sufficiently low to obtain a full response of the interface traps located near the middle of the In$_{0.53}$Ga$_{0.47}$As bandgap. This is in agreement with [7], where the use of a $f$ as low as 40 Hz is recommended to maximize the $D_{trap}$ response.

Figure 4.7(b) compares the $D_{trap}(E)$ profile obtained with the fitting method to the profiles extracted with the Terman, high-low and full conductance methods. The excellent agreement

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5The $C_g-V_g$ characteristic is corrected for parasitic capacitance using the method reported in [17]. This method requires the measurement of a device with a long gate length and a device with a short gate length. The small gate area of the short gate-length device, the lowest $f$ giving acceptable noise level was 200 Hz.
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Figure 4.7: (a) Comparison of the band bending $E-E_V$ vs $V_g$ profile obtained with the fitting of the $C_g-V_g$ characteristic and Maserjian Y-function to the profile obtained with the Terman method [29] and Berglund integral [28]. (b) Comparison of the trap density vs energy profile obtained with the fitting method to the profiles extracted from the Terman (the short dash curve shows the interpolation of the Terman data), high-low [30] and full conductance [8] methods. $C_{ox}/q$ is indicated to highlight the limitation of the full conductance method. The grey shaded areas represent the In$_{0.53}$Ga$_{0.47}$As bandgap.
4.5. Conclusion

between the fitting method and the Terman method is consistent with the analysis of the band bending shown in Figure 4.7(a). For $E_{\text{F}} - E_{\text{V}}$ going from 0.5 eV to 0.73 eV, it is clear that the fitting method and the Terman method underestimate $D_{\text{trap}}$. The high-low and the conductance methods, however, show reasonable agreement in this energy range, where $D_{\text{trap}}$ decreases from $5.8 \times 10^{12}$ /cm$^2$.eV to $4.2 \times 10^{12}$ /cm$^2$.eV. For $E_{\text{F}} - E_{\text{V}} < 0.5$ eV, the high-low method underestimates $D_{\text{trap}}$ as it suffers from the same limitation as that observed in the analysis of the Berglund integral [Figure 4.7(a)]. The conductance method also underestimates $D_{\text{trap}}$ in this energy range. This underestimation is consistent with recent works [8, 31] reporting $D_{\text{it}}$ underestimation with the conductance method in the case of $D_{\text{it}}$ values exceeding $C_{\text{ox}}/q$. This is the case in our devices since $C_{\text{ox}}/q = 4.75 \times 10^{12}$ /cm$^2$.eV and the fitting method indicates a mid-gap $D_{\text{it}}$ feature peaking at $1.5 \times 10^{13}$ /cm$^2$.eV.

4.5 Conclusion

The fixed oxide charges and interface/border traps present in the Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOS-FETs presented in Chapter 3 were examined through the study of the full gate capacitance $C_{g} - V_{g}$ characteristic. The $C_{g} - V_{g}$ characteristic was measured at a $f$ of 1 MHz and a $T$ of -50$^\circ$C in order to approximate a true H-F response. The comparison of the measured $C_{g} - V_{g}$ characteristic with a theoretical (ideal) H-F characteristic yielded a $N^+$ of $1.2 \times 10^{12}$ /cm$^2$ along with an integrated $D_{\text{trap}}$ across the In$_{0.53}$Ga$_{0.47}$As bandgap of $1.2 \times 10^{13}$ /cm$^2$.

The fitting of the $C_{g} - V_{g}$ characteristic and corresponding Maserjian Y-function yielded a $D_{\text{trap}}(E)$ across the In$_{0.53}$Ga$_{0.47}$As energy gap and extending into the In$_{0.53}$Ga$_{0.47}$As conduction band. This analysis revealed donor-like (+/0) traps within the In$_{0.53}$Ga$_{0.47}$As bandgap, with a peak density of $1.5 \times 10^{13}$ /cm$^2$.eV and centered at 0.36 eV above the In$_{0.53}$Ga$_{0.47}$As $E_{\text{V}}$. A sharp increase in donor-like (+/0) trap density in the energy range of 0.1 eV to 0.2 eV above the In$_{0.53}$Ga$_{0.47}$As $E_{\text{V}}$ was also observed. The analysis also indicated acceptor-like (0/-) traps located at energy levels aligned with the In$_{0.53}$Ga$_{0.47}$As conduction band, with a density of $2.5 \times 10^{13}$ /cm$^2$.eV at 0.3 eV above the In$_{0.53}$Ga$_{0.47}$As $E_{\text{C}}$. Although the fitting could reveal whether the observed traps were donors or acceptors, this method could not to discern whether these traps were interface traps, border traps, or a combination of both.

Finally, excellent agreement with the conventional Terman method was obtained. However, the comparison with the high-low and conductance methods highlighted a $D_{\text{trap}}$ underestimation near the In$_{0.53}$Ga$_{0.47}$As band edges. This issue may be addressed through the measurement and fitting of a $C_{g} - V_{g}$ characteristic obtained at a $T$ of 77 K or lower.
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Chapter 4. Analysis of MOS Gate Stack Defects


Chapter 5

Investigation of Border Traps and Mobility

5.1 Introduction

InGaAs and related compound semiconductors have become serious candidates for replacing strained Si in future complementary metal-oxide-semiconductor (CMOS) device applications due to their remarkable electron mobility [1]. The “standard” method for extracting the effective mobility ($\mu_{\text{eff}}$) in a metal-oxide-semiconductor field-effect transistor (MOSFET) relies on a gate-to-channel split capacitance-voltage (C-V) measurement combined with a measurement of the drain current ($I_d$) vs gate voltage ($V_g$) characteristic in direct current (DC) [2]. While this method enables highly accurate $\mu_{\text{eff}}$ extraction on SiO$_2$/Si MOSFETs, its accuracy when applied to emerging high-$k$ InGaAs devices, with relatively high density of interface traps ($D_{it}$) and density of border traps ($D_{bt}$), becomes questionable. In an attempt to address this issue, we investigated the use of an alternative method based on the inversion-charge pumping (ICP) and pulsed $I_d$-$V_g$ measurements, first proposed by Kerber et al. for Si based MOSFETs in [3], for the $\mu_{\text{eff}}$ extraction of surface-channel Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOSFETs.

5.2 Experimental Details

5.2.1 Surface-channel Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOSFETs

The In$_{0.53}$Ga$_{0.47}$As MOSFETs used in this study were fabricated using the fabrication process flow presented in Chapter 3. Briefly, the devices featured a $p$-In$_{0.53}$Ga$_{0.47}$As channel nominally doped to $4 \times 10^{17}$ /cm$^3$. An optimized (NH$_4$)$_2$S surface passivation [4, 5] was performed before the formation of a 10-nm-thick Al$_2$O$_3$ gate dielectric by atomic layer deposition (ALD). The
source and drain (S/D) areas were implanted with Si ions and subsequently activated at 600°C for 30 sec in N₂. The Pd gate and the Au/Ge/Au/Ni/Au S/D metal contacts were formed by electron-beam evaporation and lift-off. It is noted that, although the fabrication process remained the same, the devices examined in this Chapter were processed approximately a year after those presented in Chapter 3 and, consequently, exhibited slightly different DC performance at room temperature. Indeed, while the subthreshold swing (SS) remained at \( \sim 150 \text{ mV/dec.} \), a threshold voltage \( V_T \) of 0.2 V was obtained, indicating the presence of a higher fixed positive charge in the Al₂O₃ compared to the devices presented in Chapter 3.

5.2.2 Inversion-Charge Pumping Method

The ICP measurement setup shown in Figure 5.1 is similar to that of an amplitude sweep charge pumping (CP) method \[6, 7\]. The S/D contacts are shorted and connected to the ground, a square pulse train of variable amplitude going from base voltage \( V_{\text{base}} \approx \text{flat-band voltage} \) \( V_{\text{fb}} \) to peak voltage \( V_{\text{peak}} \) is applied to the gate contact and the total pumped charge density \( N_{\text{CP}} \) is measured on the substrate contact. The geometrical and trapped charge components of \( N_{\text{CP}} \) are respectively expressed as the first and second terms in the brackets of equation 5.1 \[6, 8\]:

\[
N_{\text{CP}} = \alpha C_{\text{ox}} \frac{(V_g - V_T)}{q} + (D_{\text{it}} + D_{\text{bt}} t_{\text{bt}}) \Delta E
\]

(5.1)

where \( \alpha \) is the fraction of inversion-charge density \( N_{\text{inv}} \) recombining in the substrate, \( C_{\text{ox}} \) is the gate oxide capacitance, \( q \) is the charge of an electron, \( t_{\text{bt}} \) is the oxide thickness over which the border traps are probed and \( \Delta E \) is the energy interval swept by the Fermi level going from \( V_g = V_{\text{base}} \) to \( V_{\text{peak}} \). The ICP method applied to devices featuring low \( D_{\text{it}} \) and \( D_{\text{bt}} \) such as SiO₂/Si MOSFETs enables direct extraction of \( N_{\text{inv}} \) by simply maximizing the geometrical component, \[9\], through the use of devices with channel length \( L \) > 20 \( \mu \text{m} \) in combination with fast (10 ns) pulse rise time \( (t_r) \) and fall time \( (t_f) \) \[3, 7\]. Under such conditions, most of \( N_{\text{inv}} \) is forced to recombine in the substrate and contributes to \( N_{\text{CP}} \). A correction for the fraction \( (1- \alpha) \) of \( N_{\text{inv}} \) lost by diffusion to the S/D representing the sum of the density of charge lost to the source \( N_S \) and the density of charge lost to the drain \( N_D \) is applied through the measurements of \( N_{\text{CP-S}} \) [Figure 5.1(b)] and \( N_{\text{CP-D}} \) [Figure 5.1(c)]\[1\]. Following the measurements of \( N_{\text{CP-SD}}, N_{\text{CP-S}} \) and \( N_{\text{CP-D}} \), \( N_{\text{inv}} \) can be extracted using the relationship:

\[
N_{\text{inv}} = N_{\text{CP-S}} + N_{\text{CP-D}} - N_{\text{CP-SD}}
\]

(5.2)

\[1\] Kerber et al. in \[3\] assumed device symmetry and used \( N_{\text{inv}} = 2 \times N_{\text{CP-S}} - N_{\text{CP}} \). As we observed a slight difference between the measured \( N_{\text{CP-S}} \) and \( N_{\text{CP-D}} \), which was attributed to our non self-aligned device fabrication process, we measured \( N_{\text{CP-S}} \) and \( N_{\text{CP-D}} \) and applied Equation 5.2 in order to obtain accurate \( N_{\text{inv}} \).
Figure 5.1: Schematics of the Inversion-Charge Pumping (ICP) setup used to extract the inversion charge density ($N_{\text{inv}}$) in long channel ($L > 20 \mu m$) Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOSFETs through the measurements of (a) $N_{\text{CP SD}}$, (b) $N_{\text{CP S}}$ and (c) $N_{\text{CP D}}$. $V_{\text{base}}$, $V_{\text{peak}}$, $N_S$ and $N_D$ represent the base voltage, peak voltage, loss to the source and loss to the drain, respectively. $N_{\text{inv}}$ is obtained using the relationship: $N_{\text{inv}} = N_{\text{CP S}} + N_{\text{CP D}} - N_{\text{CP SD}}$. 
In the case of devices featuring relatively high $D_{it}$ and $D_{bt}$ such as high-$k$ InGaAs MOSFETs, the ICP measurement parameters need to be carefully selected in order to, not only maximize the geometrical component, but also minimize the trapped charge component.

5.3 Results and Discussion

5.3.1 Inversion-Charge Pumping Measurements

5.3.1.1 Reduction of the Interface Trap Contribution

5.3.1.1.1 Interface Trap Density Profile

Figure 5.2 shows the $D_{it}$ vs $V_g$ profile obtained on the Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOSFETs using the high (1 MHz) - low (2 kHz) frequency method, [10], measured at a temperature ($T$) of 292 K along with the full-conductance method, [11], performed over a range of $T$ going from 292 K to 78 K. An agreement was obtained between the two methods at 292 K. It is noted that the $D_{it}$ is intentionally plotted against $V_g$ (not against energy) in order to identify the different $D_{it}$ contribution for varying $V_{base}$. The $D_{it}$ vs $V_g$ profile presents relatively high $D_{it}$ levels ($D_{it} > C_{ox}/q = 4.75 \times 10^{12} /\text{cm}^2\text{.eV}$) going towards the middle of the In$_{0.53}$Ga$_{0.47}$As bandgap for $V_g < -1$ V. $D_{it}$ values of $\sim 2 \times 10^{12}$ to $\sim 5 \times 10^{12} /\text{cm}^2\text{.eV}$ are observed near the In$_{0.53}$Ga$_{0.47}$As conduction band for $V_g$ ranging from $V_T$ to $V_T - 0.5$ V (i.e.: $V_g = -0.3$ V). These results are consistent with the analysis presented in Chapter 4 [(Figure 4.7(b), page 85)] and with the literature review shown for the Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As system in Chapter 1 [Figure 1.8(b), page 11].

5.3.1.1.2 Impact of Base Voltage and Comparison with Split C-V at Low Temperature

We found that the ICP measurement configuration where $V_{base} \approx V_{fb}$ [Figure 5.3(a)], initially developed by Kerber et al. [2] for the for the SiO$_2$/Si interface, featuring typical $D_{it}$ values of $< 10^{11} /\text{cm}^2\text{.eV}$ [11, 13], was not suitable for the Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOSFETs due to the large $D_{it}$ level observed towards the middle of the In$_{0.53}$Ga$_{0.47}$As bandgap (Figure 5.2 and Chapter 4). Indeed, in this configuration, any interface trap located within the semiconductor bandgap can contribute to $N_{CP}$ and, therefore, lead to an overestimation of $N_{inv}$. In this work, our approach was to raise $V_{base}$ as depicted in Figure 5.3(b), in order to increase the amount of interface traps constantly occupied during the ICP measurement and, therefore, reduce the $D_{it}$ contribution to $N_{CP}$. This is demonstrated in Figure 5.4(a) with $N_{CP}$ measurements obtained for a range of $V_{base}$ going from -0.9 V to -0.3 V and corrected for the loss to the S/D (1-$\alpha$) using Equation 5.2. Indeed, as $V_{base}$ was gradually raised to -0.3 V, which corresponds to the region of the $D_{it}$ vs $V_g$ profile where the $D_{it}$ is the lowest [Figure 5.2, the $N_{CP}$ vs $V_{peak}$ curves are progressively
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Figure 5.2: Density of interface traps ($D_{it}$) vs gate voltage ($V_g$) profile obtained using the high-low and full-conductance methods. The high-low was performed at a temperature ($T$) of 292 K while that of the full-conductance method was varied from 292 K to 78 K in order to access interface traps located in different parts of the In$_{0.53}$Ga$_{0.47}$As bandgap [12]. The relatively large $D_{it}$ values (greater than $C_{ox}/q$) obtained with the high-low method for $V_g < -0.75$ V preclude the use of a conductance-based method in that $V_g$ range [13]. The threshold voltage ($V_T$) of 0.2 V, obtained at $T = 292$ K, is used to locate the In$_{0.53}$Ga$_{0.47}$As conduction band edge.
Figure 5.3: Energy band diagrams of a \( p \)-type metal-oxide-semiconductor (MOS) structure showing (a) the SiO\(_2\)/Si interface case, where the density of interface trap (\( D_{it} \)) distributed across the semiconductor bandgap is negligible (< 10\(^{10}\) /cm\(^2\)eV), allowing to perform the ICP measurement with \( V_{\text{base}} = V_{\text{FB}} \), and (b) the high-\( k \)/In\(_{0.53}\)Ga\(_{0.47}\)As interface case, where the \( D_{it} \) is large, requiring \( V_{\text{fb}} \ll V_{\text{base}} < V_T \) in order to maintain constant occupancy of most of the interface traps during the ICP measurement. It is noted that as \( V_{\text{base}} \) is raised from \( V_{\text{fb}} \) towards \( V_T \), the structure is moved from a flat-band condition to a depletion condition, which involves the formation of a space charge region (SCR) energy barrier impeding the recombination of the inversion charge during the ICP measurement. In the diagrams, \( E_{\text{fm}} \) is the metal Fermi level while \( E_C \), \( E_V \) and \( E_{fp} \) are the semiconductor conduction band edge, valence band edge and Fermi level, respectively.
Figure 5.4: (a) Total pumped charge density ($N_{CP}$) vs peak voltage ($V_{peak}$) obtained for a base voltage ($V_{base}$) ranging from -0.3 V to -0.9 V. The ICP measurements were performed on a 40-μm-channel-length device with a frequency ($f$) of 1 MHz, a duty cycle ($D$) of 50 % and pulse rise time ($t_r$) and fall time ($t_f$) of 10 ns. The $D_{it}$ contribution to $N_{CP}$ reduces as $V_{base}$ is raised from -0.9 V to -0.3 V. The experimental curves are non-linear and their slopes deviate from the theoretical $C_{inv} (V_g - V_T)/q$ curve, where $C_{inv}$ is the capacitance in inversion measured by split C-V at a temperature ($T$) of 35 K and $q$ is the charge of an electron. (b) Total charge density ($N_{CV}$) vs $V_g$ obtained by split C-V at $f = 1$ MHz over a range of $T$ going from 440 K to 35 K. The $D_{it}$ contribution to $N_{CV}$ reduces as $T$ is reduced.
5.3. Results and Discussion

Figure 5.5: Loss to S/D (1-\(\alpha\)) vs peak voltage (\(V_{\text{peak}}\)) obtained for a base voltage (\(V_{\text{base}}\)) ranging from -0.3 V to -0.9 V. The space charge region (SCR) barrier height increases as \(V_{\text{base}}\) is raised from -0.9 V to -0.3 V.

shifted downwards in \(N_{\text{CP}}\) magnitude until a point where \(N_{\text{CP}}\) only starts rising at \(V_{\text{peak}} \sim V_T\), suggesting that the response of the majority of the interface trap located within the In\(_{0.53}\)Ga\(_{0.47}\)As bandgap is removed.

A similar approach was used in [16], where split C-V measurements were performed at a low \(T\) of 77 K in order to “freeze” the response of the interface traps located near the In\(_{0.53}\)Ga\(_{0.47}\)As conduction band and extract a more accurate \(N_{\text{inv}}\). We performed split C-V measurements over a wide range of \(T\) going from 440 K to 35 K Figure 5.4(b) in order to verify this concept and demonstrate that varying \(V_{\text{base}}\) in an ICP measurement performed at \(T = 292\) K had the same impact as varying \(T\) in split C-V measurement. From Figure 5.4(b), where the \(N_{\text{CV}}\) which is defined here as \(N_{\text{CV}} = N_{\text{inv}} + (D_0 + D_t) V_b \Delta E\), is plotted against \(V_g\) it is clear that the \(N_{\text{CV}}-V_g\) curves exhibit a progressive reduction in \(N_{\text{CV}}\) magnitude as \(T\) reduces from 440 K to 35 K. The similarity between the two trends observed in Figure 5.4(a) and (b) provides evidence to support the idea that raising \(V_{\text{base}}\) reduces the contribution of interface states, located in the upper part of the In\(_{0.53}\)Ga\(_{0.47}\)As bandgap, to \(N_{\text{CP}}\).

Having demonstrated the advantage of raising \(V_{\text{base}}\), we now need to consider the issue associated with a higher \(V_{\text{base}}\). Indeed, as \(V_{\text{base}}\) is raised towards \(V_T\), the fraction (1-\(\alpha\)) of \(N_{\text{inv}}\) lost to
the S/D increases significantly (Figure 5.5) and the correction applied to \(N_{CP}\) using Equation 5.2 becomes larger. This is explained by the fact that as \(V_{base}\) increases, the barrier height of the space charge region (SCR) increases [Figure 5.3(b)], impeding the recombination of the inversion charge in the substrate but favoring its diffusion to the S/D, consistent with [9].

Referring back to Figure 5.4(a) and considering an inversion capacitance of \(5.5 \times 10^{-7} \text{ F/cm}^2\) extracted from the split C-V measurement at frequency \((f) = 1 \text{ MHz and } T = 35 \text{ K}[\text{Figure 5.4(b)}]\), we can compare the measured \(N_{CP}V_{\text{peak}}\) \((V_{base} = -0.3 \text{ V})\) curve to a theoretical \(C_{\text{inv}}V_{g}\) curve. It is evident that the \(N_{CP}V_{\text{peak}}\) curve "curls up" and significantly deviates from \(C_{\text{inv}}V_{g}\) as \(V_{\text{peak}}\) increases. If the only contribution to \(N_{CP}\) above \(V_{T}\) is \(N_{\text{inv}}\), this relationship should be linear. We suggest that this deviation from linearity for \(V_{g} > V_{T}\) is a consequence of a \(D_{bt}\) contribution. Moreover, the same \(D_{bt}\) affects the ICP and the split C-V measurement differently. This can be explained using the energy band diagram of a metal-oxide-semiconductor (MOS) structure assuming a simplified \(D_{bt}\) uniformly distributed across energy. In the case of the ICP measurement, the \(\Delta E\) swept by the Fermi level going from \(V_{base}\) to \(V_{\text{peak}}\) increases with \(V_{\text{peak}}\) [Figure 5.6(a)]. As a result, the integrated border trap contribution \(D_{bt}I_{bt}\Delta E\) to \(N_{CP}\) (Equation 5.1) also increases with \(V_{\text{peak}}\) leading to the non-linearity observed on the \(N_{CP}V_{\text{peak}}\) curves [Figure 5.4(a)]. In the case of a split C-V measurement, however, where the response to a small alternative current (ac) signal superposed to a slowly varying \(V_{g}\) is measured [Figure 5.6(b)], \(\Delta E\) and, therefore, \(D_{bt}I_{bt}\Delta E\) only depend on the amplitude of the ac signal (typically 25 mV) but remain independent of \(V_{g}\). In the presence of a non-uniformly distributed \(D_{bt}\) across energy, \(D_{bt}I_{bt}\Delta E\) will vary with \(V_{g}\). However, this effect will not be as strong as in the case of the ICP.

5.3.1.2 Reduction of the Border Trap Contribution

5.3.1.2.1 Evidence of Border Trap Contribution

Recent studies have indicated the presence of border traps in high-k InGaAs MOS structures using C-V [17, 18], charge pumping [19] and high-frequency transconductance [20] measurements. Evidence of the presence of border traps can also be observed in the \(I_{d}V_{g}\) characteristic, where it is manifest as a hysteresis [21, 22]. Single pulse and DC \(I_{d}V_{g}\) hysteresis, performed on a 1-\(\mu\)m channel-length \((L)\) device at a drain-to-source voltage \((V_{ds})\) of 50 mV, are shown in Figure 5.7. Going from a “slow” DC measurement to a “fast” single pulse measurement, the hysteresis increased from 70 mV to 195 mV, while the drain current at \(V_{g} = 2.5 \text{ V}\) increased from 14.5 mA/mm to 16 mA/mm. This strongly suggests the presence of a charge trapping process involving border traps.
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Figure 5.6: Example of energy band diagrams of a p-type metal-oxide-semiconductor (MOS) structure with a density of border traps ($D_{bt}$) assumed to be uniformly distributed across energy. (a) Case of an ICP measurement where the base voltage ($V_{base}$) is set to -0.3 V and the peak voltage ($V_{peak}$) is set to a value above the threshold voltage ($V_T$), respectively. (b) Case of a split C-V measurement where the gate voltage ($V_g$) > $V_T$. In an ICP measurement, the energy range ($\Delta E$) swept by the Fermi level increases with $V_{peak}$, while in a split C-V measurement, $\Delta E$ depends on the amplitude of the AC signal (typically set to 25 mV) and not on $V_g$. Consequently, the $D_{bt} \cdot t_{ox} \cdot \Delta E$ contribution in an ICP measurement at large $V_{peak}$ is much higher than that of a split C-V measurement performed at a $V_g$ matching $V_{peak}$. In the diagrams, $E_C$, and $E_{fp}$ are the semiconductor conduction band edge, and Fermi level, respectively.
5.3.1.2.2 Impact of Duty Cycle

To minimize the $D_{bt}$ contribution to $N_{CP}$, we propose to keep $f$ constant but reduce the duty cycle ($D$) in order to reduce the transient charging time ($t_{charge} = D/f$) of the border traps. This approach is based on the premise that, since border traps capture charges from the inversion layer, the time to charge the border traps must be larger than the time required to form the inversion layer. The impact of $D$ ($t_{charge}$) on $N_{CP}$ is presented in Figure 5.8, where $D$ ($t_{charge}$) is gradually reduced from 50% (500 ns) to 5% (50 ns) for $f = 1$ MHz. The “curling up” of the $N_{CP}$-$V_{peak}$ curve, which was attributed to a $D_{bt}$ contribution, gradually reduces as $D$ reduces. At $D = 5\%$, the $N_{CP}$-$V_{peak}$ curve nearly matches $C_{inv}(V_gV_T)/q$ and the “curling up” almost disappears, suggesting a significant reduction in the $D_{bt}$ contribution.

5.3.1.2.3 Multi-frequency Inversion-charge Pumping

In order to study the impact of $f$ on the $D_{bt}$ response, we performed ICP measurements over a range of $f$ going from 10 kHz to 2 MHz for a fixed $D$ of 50% and a $V_{peak}$ going from 0 V to 2 V. In Figure 5.9, $N_{CP}$ is plotted against $f$ on the top x-axis and against $t_{charge}$ on
5.3. Results and Discussion

Figure 5.8: (a) Impact of duty cycle ($D$) on total pumped charge density ($N_{CP}$) obtained from ICP performed at a frequency ($f$) of 1 MHz and a rise time ($t_r$) and fall time ($t_f$) of 10 ns. The curve obtained at $D = 5\%$ nearly matches the theoretical $C_{inv} (V_g - V_T)/q$ curve, consistent with a reduction of the $D_{bt}$ contribution to $N_{CP}$ at low $D$. 

$N_{CP} (10^{12}/\text{cm}^2)$

$V_{peak} (\text{V})$
Figure 5.9: Total pumped charge density ($N_{CP}$) plotted against frequency ($f$) on the top $x$-axis and against charging time ($t_{charge}$), which is equal to $1/(2.f)$, on the bottom $x$-axis. The symbols show the experimental data obtained from the measurements performed on a 40-µm-channel-length device with the pulse rise time ($t_r$) and fall time ($t_f$) set to 10 ns, a base voltage ($V_{base}$) of -0.3 V and a duty cycle ($D$) of 50%. The peak voltage ($V_{peak}$) was varied from 0 V to 2 V. The lines represent the fitting of the data with the proposed charge trapping model.
Table 5.1: Model parameters fitted for a range of peak voltage ($V_{\text{peak}}$) values going from 0 V to 2 V. $N^0_{\text{bt}}$ is the border trap density in the Al$_2$O$_3$ integrated across energy and thickness, $\tau$ is the capture time constant, $\beta$ is the distribution factor of capture time constant and $N_{\text{inv}}$ is the inversion-charge density.

<table>
<thead>
<tr>
<th>$V_{\text{peak}}$ (V)</th>
<th>0</th>
<th>0.5</th>
<th>1</th>
<th>1.5</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\tau$ ($\mu$s)</td>
<td>1.7</td>
<td>1.2</td>
<td>1.2</td>
<td>1.1</td>
<td>1.0</td>
</tr>
<tr>
<td>$\beta$</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
<td>1.0</td>
</tr>
<tr>
<td>$N^0_{\text{bt}}$ ($10^{12}$ /cm$^2$)</td>
<td>1.4</td>
<td>2.9</td>
<td>4.6</td>
<td>6.3</td>
<td>7.8</td>
</tr>
<tr>
<td>$N_{\text{inv}}$ ($10^{12}$ /cm$^2$)</td>
<td>0.09</td>
<td>0.7</td>
<td>1.9</td>
<td>3.5</td>
<td>5.7</td>
</tr>
<tr>
<td>Adjusted R$^2$</td>
<td>0.997</td>
<td>0.991</td>
<td>0.984</td>
<td>0.964</td>
<td>0.991</td>
</tr>
</tbody>
</table>

the bottom x-axis [as $D = 50\%$, $t_{\text{charge}} = 0.5/f$]. $N_{\text{CP}}$ increases as $f$ reduces and a clear $N_{\text{CP}}$ saturation is reached for $f < \sim 100$ kHz ($t_{\text{charge}} > \sim 5$ $\mu$s), suggesting a full $D_{\text{bt}}$ response in that $f$ range. In the high $f$ region, however, no $N_{\text{CP}}$ saturation is observed. This suggests that some border traps still respond at $f > 2$ MHz. This is in line with the work reported in [20], where evidence of “fast” border traps responding to $f > 1$ GHz is demonstrated. Unfortunately, the GHz frequency range is not accessible in our case. Indeed, considering the following equation for the recombination of the electrons of the inversion layer with the holes of the $p$-type substrate:

$$N_{\text{inv}}(t) = N_{\text{inv}}(0). \exp(-t/\tau_e)$$ (5.3)

and an electron lifetime ($\tau_e$) of 30 ns for $p$-In$_{0.53}$Ga$_{0.47}$As doped to $4 \times 10^{17}$ /cm$^3$ [23], we calculated that a channel with $N_{\text{inv}} = 10^{11}$ /cm$^2$, $10^{12}$ /cm$^2$ and $10^{13}$ /cm$^2$ would be effectively depleted ($N_{\text{inv}} < 10^9$ /cm$^2$) in approximately 130 ns, 210 ns and 270 ns, respectively. This indicates that it is not possible to perform ICP measurements at $f > 2$ MHz and $D = 50\%$ as the transient discharge time [$t_{\text{discharge}} = (1-D)/f$] becomes too short to allow the full $N_{\text{inv}}$ recombination, leading to an underestimation of $N_{\text{inv}}$. We propose to circumvent this issue by fitting the measured “multi-frequency ICP” data shown in Figure 5.9 using a charge trapping model, similar to that reported in [24]-[26], but including $N_{\text{inv}}$ and assuming a negligible $D_{\text{it}}$ contribution to $N_{\text{CP}} (\text{as } V_{\text{base}} = -0.3 \text{ V}):$

$$N_{\text{CP}} = N^0_{\text{bt}}[1 - \exp(-(t_{\text{charge}}/\tau)^\beta)] + N_{\text{inv}}$$ (5.4)

where $\tau$ is the capture time constant, $\beta$ is the distribution factor of the capture cross section ($\sigma$) and $N^0_{\text{bt}}$ is the surface-equivalent density of border trap integrated across the energy range swept as $V_g$ goes from $V_{\text{base}}$ to $V_{\text{peak}}$. The $\tau$, $\beta$, $N^0_{\text{bt}}$ and $N_{\text{inv}}$ values obtained from the fitting of the multi-frequency $N_{\text{CP}}$ data for $V_{\text{peak}}$ ranging from 0 V to 2 V (Figure 5.9) are summarized in Table 5.1. Adjusted R$^2$ ranging from 0.964 to 0.997 were obtained, indicating a good fit of the
model to the experimental data.

As $V_{\text{peak}}$ increased from 0 V to 2 V, a decrease in $\tau$ from 1.6 $\mu$s to 1.0 $\mu$s was observed. These $\tau$ values are consistent with the values reported in [24] for traps located at energy levels aligned with the In$_{0.53}$Ga$_{0.47}$As conduction band. In the charge trapping model, the distribution factor $\beta$, which represents a measure of the width of the $\sigma$ distribution of the traps, can range between a value of 1.0 and 0. A $\beta$ value of 1.0 corresponds to a discrete $\sigma$, while values approaching 0 indicate very wide distributions of $\sigma$. The fact that our experimental data was best fitted with $\beta = 1.0$ indicates a discrete $\sigma$ and suggests that the border traps could originate from a single type of physical defect. It is possible to estimate $\sigma$ using:

$$\tau = (N.\sigma.v_{th})^{-1}$$  \hspace{1cm} (5.5)$$

where $N$ is the volume inversion density and $v_{th}$ is the electron thermal velocity. Considering $\tau \approx 1 \mu$s, $v_{th} = 5.5 \times 10^7$ cm/s [28] and $N = 4.1 \times 10^{18}$ /cm$^3$ [27] we estimated that $\sigma$ was $\sim 4.5 \times 10^{21}$ cm$^2$. This rather small $\sigma$ value is consistent with that of border traps [29], as $\sigma$ values in the $10^{-13}$ to $10^{-17}$ range are generally considered for interface traps [12, 19, 30]. The distance ($x$) of the border traps from the semiconductor interface can be estimated using the relationship [31]:

$$x = \lambda \ln(t_{t}/\tau)$$  \hspace{1cm} (5.6)$$

where $t_t$ is the tunnelling time and $\lambda$ is the attenuation coefficient. Considering that $N_{CP}$ saturation is reached at $t \sim 5$ $\mu$s (Figure 5.9) and $\lambda = 1.1 \times 10^{-8}$ cm [20], we calculated a distance $x$ of $\sim 1.5$ Å from the interface, consistent with the value reported in [20] for a HfO$_2$/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As system. The increase in $N_{bt}^0$ with $V_{\text{peak}}$ is consistent with the presence of border traps located at energy levels aligned with the In$_{0.53}$Ga$_{0.47}$As conduction band [17]. Moreover, assuming a $\sim 2$-Å-wide border trap distribution [20], consistent with a discrete $\sigma$, and considering that an energy range of 0.77 eV is swept when $V_g$ goes from $V_{\text{base}} = -0.3$ V to $V_{\text{peak}} = 2$ V [obtained from the analysis of Chapter 4], a $N_{bt}^0$ of $7.8 \times 10^{12}$ /cm$^2$ would equate to a $D_{bt}$ of $5.1 \times 10^{20}$ /cm$^3$.eV, which is in reasonable agreement with the peak $D_{bt}$ values of $1.05 \times 10^{21}$ /cm$^3$.eV and $1.6 \times 10^{21}$ /cm$^3$.eV reported in [19] and [20], respectively. This analysis suggests the presence of border traps featuring a very small capture cross section and being located very close to the Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As interface in a very narrow spatial distribution. We speculate that the presence of these border traps could be due to an ultra-thin interlayer of native oxide at the Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As interface. This speculation warrants further investigation. It is noted that the fast trapping of electrons, in border-trap distributions presenting very similar

\footnote{Self-consistent Poisson Schrödinger calculations revealed an inversion layer thickness of 14 nm at $N_{inv} = 5.7 \times 10^{12}$ /cm$^2$, yielding $N = 4.1 \times 10^{18}$ /cm$^3$.}
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Figure 5.10: Comparison of the total pumped-charged density \(N_{CP}\) obtained from inversion-charge pumping (ICP) at a frequency \(f\) of 1 MHz and duty cycle \(D\) of 5\%, and multi-frequency ICP. In both measurements the base voltage \(V_{base}\) was -0.3 V and the rise time \(t_r\) and fall time \(t_f\) were 10 ns.

The negligible \(N_{inv}\) value at \(V_{peak} = 0\) V (Table 5.1) is consistent with a \(V_T\) of 0.2 V. As \(V_{peak}\) increases from 0.5 V to 2 V, \(N_{inv}\) increases from \(7.0 \times 10^{11}\) to \(5.7 \times 10^{12}/\text{cm}^2\). Figure 5.10 compares the \(N_{CP}\) obtained from multi-frequency ICP to that obtained from ICP \((f = 1\text{MHz}\) and \(D = 5\%))\). The Multi-frequency ICP gives slightly lower \(N_{CP}\) values, confirming that some border traps can respond in less than 50 ns, consistent with [20].

Although the separation of the \(D_{bt}\) component of \(N_{CP}\) was successfully demonstrated through the fitting of the multi-frequency ICP data, it is important to note that a potential \(D_{bt}\) component associated with interface traps located at energy levels aligned with the In\(_{0.53}\)Ga\(_{0.47}\)As conduction, [33], may still lead to an overestimation of \(N_{inv}\). However, the integration of the total trap density vs energy profile obtained in Chapter 4 [Figure 4.6(b), page 83], across a \(\Delta E\) corresponding to a \(V_g\) sweep going from 0.5 to 2 V, yielded a trap density of \(\sim 4.4 \times 10^{12}/\text{cm}^2\). This value is in close agreement with the value of \(4.9 \times 10^{12}/\text{cm}^2\) obtained by subtracting the...
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$N_{bt}^0$ values obtained using the multi-frequency method for $V_{\text{peak}} = 2$ V and 0.5 V (Table 5.1). This provides strong evidence that most of the traps located at energy levels aligned with the In$_{0.53}$Ga$_{0.47}$As conduction could be border traps in these devices. It also suggests that the $N_{\text{inv}}$ extracted by multi-frequency ICP represents a good estimate of the true $N_{\text{inv}}$.

The multi-frequency ICP technique was demonstrated to be an effective approach for the characterization of border traps and the extraction of $N_{\text{inv}}$. However, this approach suffers from one limitation: the very large number of measurements required to obtain a full $N_{\text{inv}}$ vs $V_g$ curve. For instance, obtaining the data shown in Figure 5.9 required the measurement of $N_{\text{CP}_-SD}$, $N_{\text{CP}_-S}$ and $N_{\text{CP}_-D}$ (Figure 5.1) at 13 different $f$, representing a total of 39 measurements. Such a large number of measurements makes this approach difficult to implement without stressing the devices, especially when low $f$ are required to investigate the full $D_{bt}$ response.

5.3.2 $I_d-V_g$ Measurements

5.3.2.1 Pulse $I_d-V_g$ Measurements and Series Resistance Extraction

Figure 5.11 compares the pulsed and DC $I_d-V_g$ measurements performed at a drain-to-source voltage ($V_{ds}$) of 50 mV on a device featuring a channel length ($L$) of 1 µm and a channel width ($W$) of 50 µm. The rise time ($t_r$) and fall time ($t_f$) of the pulsed $I_d-V_g$ measurement were set to 10 ns. It is noted that the pulsed measurement resulted in a $\sim 10\%$ increase in the maximum drain current, consistent with a charge trapping process within the Al$_2$O$_3$ gate oxide. As the presence of “fast” border traps was demonstrated, we speculate that higher $f$ or lower $D$ may reveal an even higher maximum drain current. Unfortunately, our pulsed $I-V$ setup does not allow such measurement conditions. Additional pulsed and DC $I_d-V_g$ measurements were performed on devices with channel lengths of 2, 3, 5, 10 and 20 µm in order to extract S/D resistance ($R_{SD}$) values of 49 Ω and 59 Ω, respectively (inset Figure 5.11).

5.3.2.2 Low Temperature DC $I_d-V_g$ Measurements and Series Resistance Extraction

The effect of reducing $T$ in DC $I_d-V_g$ measurements is illustrated in Figure 5.12. The $V_T$ shifts towards more positive values as $T$ reduces, consistent with Figure 5.4(b). A zero-temperature coefficient (ZTC) point at $V_g = 2.15$ V is observed. The inset of Figure 5.12 shows that $R_{SD}$ increases when $T$ is reduced. This is consistent with an incomplete ionization of the S/D dopant increasing as $T$ reduces [34].
5.3. Results and Discussion

Figure 5.11: Comparison of the pulse and DC $I_d-V_g$ characteristics performed on a 1-$\mu$m-channel-length device at a drain-to-source voltage ($V_{ds}$) of 50 mV. The rise time ($t_r$) and fall time ($t_f$) of the pulse measurement were set to 10 ns. Inset: $R_{total}$ ($= V_{ds}/I_d$) vs channel length ($L$) at a gate voltage ($V_g$) of 2.5 V. The intercept on the $y$-axis yields the source and drain series resistance ($R_{SD}$).

Figure 5.12: DC $I_d-V_g$ characteristics measured over a range of temperature ($T$) going from 4 K to 292 K on a 10-$\mu$m-channel-length device at a drain-to-source voltage ($V_{ds}$) of 50 mV. A zero-temperature coefficient (ZTC) point is observed. Inset: Source and drain series resistance ($R_{SD}$) as a function of temperature ($T$).
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Figure 5.13: Effective mobility ($\mu_{\text{eff}}$) vs inversion charge ($N_{\text{inv}}$) extracted using ICP at a frequency ($f$) of 1 MHz and a duty cycle ($D$) ranging from 50% to 5% and multi-frequency ICP. Excellent agreement is obtained between the $\mu_{\text{eff}}$ extracted from Split C-V ($f = 1$ MHz, $T = 292$ K) and that extracted by ICP ($f = 1$ MHz, $D = 50\%$). The experimental $\mu_{\text{eff}}$ values (symbols) were fitted with the empirical model reported in [37].

5.3.3 Comparison of the Effective Mobility Extracted from the Inversion-Charge Pumping, Multi-frequency Inversion-Charge Pumping and Low Temperature Split C-V Methods

Figure 5.13 compares the $\mu_{\text{eff}}$ extracted from ICP ($f = 1$ MHz, varied $D$), multi-frequency ICP and Split C-V ($f = 1$ MHz, $T = 292$ K). Excellent agreement between the ICP at $D = 50\%$ and split C-V was obtained. As the $D_{\text{bt}}$ contribution to $N_{\text{CP}}$ is reduced due to a reduction in $D$, $\mu_{\text{eff}}$ at low $N_{\text{inv}}$ increases significantly. A peak $\mu_{\text{eff}}$ of 2850 cm$^2$/V.s at a low $N_{\text{inv}}$ of $7 \times 10^{11}$ cm$^2$/V.s was obtained from multi-frequency ICP. However, a strong $N_{\text{inv}}$ dependence is also observed as $\mu_{\text{eff}}$ rapidly drops down to $\sim 600$ cm$^2$/V.s at $N_{\text{inv}} = 1 \times 10^{13}$ /cm$^2$. This strong $N_{\text{inv}}$ dependence is consistent with a $\mu_{\text{eff}}$ dominated by surface roughness at high $N_{\text{inv}}$, in agreement with [16,35,36].

As the $\mu_{\text{eff}}$ degradation mechanism due to surface roughness is typically independent of $T$, we extracted $\mu_{\text{eff}}$ from Split C-V ($f = 1$ MHz) measurements performed over a range of $T$ going from 292 K to 35 K. While an increase in $\mu_{\text{eff}}$ is observed for $N_{\text{inv}} < 4 \times 10^{12}$/cm$^2$ as $T$ reduces, consistent with the reduction of the $D_{\text{bt}}$ contribution to $N_{\text{inv}}$ at lower $T$ discussed in paragraph 5.3.1.1.2 and also reported in [16], it is very clear that $\mu_{\text{eff}}$ remains independent of $T$ for $N_{\text{inv}} > 4 \times 10^{12}$/cm$^2$. This temperature independence and strong $N_{\text{inv}}$ dependence
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Figure 5.14: Effective mobility ($\mu_{eff}$) vs inversion charge ($N_{inv}$) extracted using split C-V at a frequency ($f$) of 1 MHz for a range of temperature ($T$) going ranging from 292 K to 35 K. The experimental $\mu_{eff}$ values (symbols) were fitted with the empirical model reported in [37].

represent a strong evidence that $\mu_{eff}$ is dominated by surface roughness at high $N_{inv}$. However, the $\mu_{eff}$ extracted from split C-V at $T = 35$ K still remained lower than that extracted with the ICP (D = 5%) and multi-frequency ICP methods.

5.3.4 Modeling of Effective Mobility

In order to gain further insight in the mechanisms involved in the $\mu_{eff}$ degradation, we fitted the extracted $\mu_{eff}$ using the empirical model reported in [37], where the phonon scattering mobility ($\mu_{ph}$), the surface roughness scattering mobility ($\mu_{sr}$), the Coulomb scattering mobility ($\mu_{C}$) and the total mobility ($\mu_{tot}$) are expressed in Equations 5.7, 5.8, 5.9, and 5.10, respectively:

$$\mu_{ph} = A.N_{inv}^{-0.3}T^{-1.75}$$  \hspace{1cm} (5.7)

$$\mu_{sr} = B.N_{inv}^{\beta}$$  \hspace{1cm} (5.8)

$$\mu_{C} = C.N_{inv}^{\gamma}$$  \hspace{1cm} (5.9)

$$1/\mu_{tot} = 1/\mu_{ph} + 1/\mu_{sr} + 1/\mu_{C}$$  \hspace{1cm} (5.10)

The parameters $A$, $B$, $\beta$, $C$ and $\gamma$ were adjusted to fit the experimental $\mu_{eff}$ extracted from ICP ($f = 1$ MHz, varied $D$), multi-frequency ICP and split C-V ($f = 1$ MHz, varied $T$). As indicated by the $T^{-1.75}$ dependence of $\mu_{ph}$, phonon scattering becomes negligible at low $T$. 

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Therefore, we first fitted the high $N_{inv}$ part of the $\mu_{eff}$ curve extracted from split $C$-$V$ at $T = 35$ K in order to obtain the coefficients $B = 6.5 \times 10^{15}$ and $\beta = -1$ that define $\mu_{sr}$. It is noted that, although surface roughness generally shows a $N_{inv}^{-2}$ dependence, a $N_{inv}^{-0.7}$ dependence was reported in [36] for Al$_2$O$_3$/In$_x$Ga$_{1-x}$As MOSFETs. We then obtained a $\gamma$ of 1.3 for $\mu_C$ by fitting the low $N_{inv}$ part of the curve. We then fitted $\mu_{eff}$ over a range of $T$ going from 35 K to 292 K to obtain a coefficient $A$ of $\sim 4 \times 10^{12}$ for $\mu_{ph}$, which was found to be higher than $10^4$ cm$^2$/V.s and have no significant impact on $\mu_{eff}$, consistent with [35, 36]. The coefficient $C$ of for $\mu_C$ was adjusted in order to account for the reduction of the $D_{it}$ contribution to $N_{CV}$ at lower $T$. The same model was also used to fit the ICP ($f = 1$ MHz, varied $D$) and multi-frequency ICP data, as shown in Figure 5.13. A simple adjustment of $\mu_C$ was found to be sufficient to obtain good fittings (Figure 5.15).

The approach presented in Chapter 4 was used in a parallel study to remove the contribution of traps aligned with the In$_{0.53}$Ga$_{0.47}$As conduction band to a $N_{CV}$ measured by split $C$-$V$ [35]. This enabled to extract $N_{inv}$ and $\mu_{eff}$ and perform first-principles theoretical calculations [the calculations were performed by T. P. O'Regan (Tyndall)] in order to investigate the scattering mechanisms responsible for the $\mu_{eff}$ degradation. This analysis yielded results comparable to the results obtained with the multi-frequency ICP approach. Moreover, the theoretical calculations predicted a surface root mean square (RMS) roughness of 1.95 nm on the In$_{0.53}$Ga$_{0.47}$As channel.

### 5.3.5 Analysis of the Surface Roughness of the Channel

RMS surface roughness measurements were obtained by atomic force microscopy (AFM) on a set of different samples in order to confirm the results obtained from the fitting of the electrical data and to identify the process step responsible for the high roughness of the In$_{0.53}$Ga$_{0.47}$As surface. As listed in Table 5.2, the unpassivated sample [Figure 5.16(a)], the (NH$_4$)$_2$S surface-passivated sample and the dilute-HF-dipped p-In$_{0.53}$Ga$_{0.47}$As samples revealed low RMS surface roughness values of $0.21 \pm 0.07$ nm, $0.23 \pm 0.04$ nm and $0.21 \pm 0.07$ nm, respectively. However, a significantly high RMS surface roughness ($1.95 \pm 0.28$ nm) was observed on the device sample, exposed to surface passivation, ALD of Al$_2$O$_3$, activation anneal at 600$^\circ$C for 15 sec and Al$_2$O$_3$ removal using dilute HF [Figure 5.16(b)]. This confirms the result obtained from the fitting of the $\mu_{eff}$ vs $N_{inv}$ curves (Figure 5.13 and Figure 5.14) and suggests an RMS surface roughness increase following activation anneal at 600$^\circ$C for 15 sec. We speculate that the As atoms desorbed from surface during the S/D activation anneal, leading to the formation of Ga aggregates [Figure 5.16]. The aggregates formation is very significant and the formation mechanisms warrant further investigation.
5.3. Results and Discussion

Figure 5.15: Scattering components obtained from the fitting of the effective mobility ($\mu_{\text{eff}}$) vs inversion charge ($N_{\text{inv}}$) curves extracted from ICP ($f = 1$ MHz, $D = 50\%$) and multi-frequency (M-F) ICP. The phonon scattering mobility, the surface roughness scattering mobility, the Coulomb scattering mobility and the total mobility are noted $\mu_{\text{ph}}$, $\mu_{\text{sr}}$, $\mu_{\text{C}}$, and $\mu_{\text{tot}}$, respectively. While the same $\mu_{\text{ph}}$ and $\mu_{\text{sr}}$ were used to fit both curves, $\mu_{\text{C}}$ was adjusted to account for the removal of the border trap contribution to the total pumped-charged density ($N_{\text{CP}}$).
Table 5.2: RMS surface roughness extracted from AFM measurements. The quoted value represents the mean from at least three measurements at separate locations (each on a 1 µm × 1 µm scan area) and the uncertainty is given by the standard deviation.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Treatment</th>
<th>RMS (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Unpassivated</td>
<td>0.21 ± 0.07</td>
</tr>
<tr>
<td>2</td>
<td>10% (NH₄)₂S (20 min)</td>
<td>0.23 ± 0.04</td>
</tr>
<tr>
<td>3</td>
<td>dilute HF (20 s)</td>
<td>0.21 ± 0.05</td>
</tr>
<tr>
<td>4</td>
<td>10% (NH₄)₂S (20 min)/ALD Al₂O₃/RTA (600°C, 15 s)/dilute HF (20 s)</td>
<td>1.95 ± 0.28</td>
</tr>
</tbody>
</table>

Figure 5.16: AFM topography data of (a) the unpassivated $p$-In$_{0.53}$Ga$_{0.47}$As surface and (b) the $p$-In$_{0.53}$Ga$_{0.47}$As surface after 10% (NH₄)$_₂$S pasivation for 20 min, 10 nm Al₂O₃ deposition by ALD, implant activation at 600°C for 15 s and finally Al₂O₃ etch using dilute HF. Both measurements were taken over a 1 µm × 1 µm area. The AFM measurements were performed by M. Burke (Tyndall).
5.4 Conclusion

We applied the ICP method to extract the $\mu_{\text{eff}}$ of surface-channel Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOS-FETs. We adjusted the ICP measurement parameters in order to minimize the impact of $D_{it}$ and $D_{bt}$ on the measured $N_{\text{inv}}$. The $V_{\text{base}}$ minimized the $D_{it}$ response, while the duty cycle ($D$) was used to reduce the $D_{bt}$ response. We proposed a multi-frequency ICP technique to investigate the $D_{bt}$ response. The investigations suggested a discrete $\sigma$ value of $\sim 4.5 \times 10^{-21}$ cm$^2$, consistent with a very narrow spatial distribution of border traps located very close ($\sim 1.5$ Å) to the Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As interface. Although a peak $\mu_{\text{eff}}$ of $\sim 2850$ cm$^2$/V.s was extracted at a low $N_{\text{inv}}$ of $7 \times 10^{11}$ /cm$^2$ using the multi-frequency ICP technique, a sharp drop in $\mu_{\text{eff}}$ was observed at higher $N_{\text{inv}}$ due to a dominant surface roughness scattering mechanism. This was confirmed by the lack of $T$ dependence observed in the $\mu_{\text{eff}}$ at $N_{\text{inv}} > 4 \times 10^{12}$ /cm$^2$ obtained by split C-V measurements performed over a range of $T$ going from 292 K to 35 K along with the high RMS surface roughness of 1.95 ± 0.28 nm measured by AFM on the In$_{0.53}$Ga$_{0.47}$As surface. Finally, the AFM measurements identify the S/D activation anneal process ($600^\circ$C for 15 s) as being the cause of high In$_{0.53}$Ga$_{0.47}$As surface roughness.
Chapter 5. Investigation of Border Traps and Mobility

Bibliography


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Chapter 6

Impact of Channel Thickness on Junctionless MOSFET Performance

6.1 Introduction

The junctionless device concept for silicon on insulator (SOI) metal-oxide-semiconductor field-effect transistors (MOSFETs) first introduced by Colinge et al. in 2010 [1], has demonstrated considerable gains in terms of process simplicity when compared to conventional inversion-mode MOSFETs. While the original devices featured near-ideal subthreshold slope and extremely low OFF-state current, further work demonstrated an increase in ON-current through the use of strain-induced mobility enhancement techniques [2]. To extend on this work, we propose to apply the junctionless device concept to a III-V structure. The following reasons suggest that the junctionless device concept could be particularly well suited to III-V structures:

1. The high donor doping concentration ($N_d$) required in the channel of a junctionless MOSFET is less problematic for In$_{0.53}$Ga$_{0.47}$As than it is for Si. Indeed, the bulk electron mobility in Si is $100 \text{ cm}^2/\text{V.s}$ at $N_d = 1 \times 10^{19} \text{/cm}^3$ [3], while that in In$_{0.53}$Ga$_{0.47}$As is $\sim 4000 \text{ cm}^2/\text{V.s}$ at a similar $N_d$ level [4].

2. The junctionless architecture circumvents the difficulties associated with the implantation [5, 6] or regrowth [7, 8] techniques generally used to form the source and drain (S/D) regions of III-V inversion-mode MOSFETs.

The objective of this work is to implement the junctionless device concept in a planar III-V structure, where the SiO$_2$ of the SOI in [1] is replaced by a wide bandgap $p$-In$_{0.52}$Al$_{0.48}$As barrier layer with a low acceptor doping concentration ($N_a$), in order to study the impact of the In$_{0.53}$Ga$_{0.47}$As channel thickness ($t_{\text{InGaAs}}$) on the device performance.
Figure 6.1: In$_{0.53}$Ga$_{0.47}$As channel thickness ($t_{\text{InGaAs}}$) vs In$_{0.53}$Ga$_{0.47}$As channel doping ($N_d$). The calculated maximum depletion width ($W_d^{\text{max}}$) yields the boundary between the fully depleted and non-fully depleted device structure. The 20 nm $t_{\text{InGaAs}}$ limit, where severe effective electron mobility ($\mu_{\text{eff}}$) degradation is reported [10], and the set of $t_{\text{InGaAs}}$ (32, 24, 20, 16 and 12 nm) vs $N_d$ ($9 \times 10^{17}$ /cm$^3$) parameters corresponding to the fabricated devices are also indicated.

To obtain a planar junctionless In$_{0.53}$Ga$_{0.47}$As MOSFET featuring a high ON-current ($I_{\text{ON}}$) and a low OFF-current ($I_{\text{OFF}}$), the In$_{0.53}$Ga$_{0.47}$As channel $N_d$ and $t_{\text{InGaAs}}$ need to be carefully selected. Indeed, a high $N_d$ is required to obtain a high $I_{\text{ON}}$ and a good source and drain (S/D) contact resistance [9]. However, since the channel has to be fully depleted of carriers for the device to be switched off, a low $I_{\text{OFF}}$ will only be achieved if the channel thickness is thinner than the maximum depletion width ($W_d^{\text{max}}$) which given by:

$$W_d^{\text{max}} = 2\sqrt{\frac{\epsilon_s k_B T \ln(N_d/n_i)}{q^2 N_d}}$$

(6.1)

where $\epsilon_s$ is the semiconductor dielectric constant, $k_B$ is the Boltzmann constant, $T$ is the temperature, $n_i$ is the intrinsic carrier concentration and $q$ is the charge of an electron. The $W_d^{\text{max}}$ boundary between the fully depleted and non-fully depleted structures is shown in Figure 6.1. One additional parameter to take into account when designing planar junctionless III-V
6.1. Introduction

Figure 6.2: Quasi-static capacitance-voltage (C-V) characteristics obtained for Pd/Al$_2$O$_3$/n-In$_{0.53}$Ga$_{0.47}$As/p-In$_{0.52}$Al$_{0.48}$As/p-InP structures using a self-consistent Poisson-Schrödinger solver. The structures featured In$_{0.53}$Ga$_{0.47}$As channel thicknesses ($t_{\text{InGaAs}}$) of 32, 24 and 16 nm and an In$_{0.53}$Ga$_{0.47}$As channel doping ($N_d$) of $9 \times 10^{17}$/cm$^3$. A flat-band capacitance ($C_{fb}$) of 0.52 µF/cm$^2$ and flat-band voltage ($V_{fb}$) of 0.2 V were obtained. It is noted that the dotted line inversion response of the quasi-static C-V curves will not be typically observed experimentally in a multi-frequency C-V.

MOSFETs is the severe effective electron mobility ($\mu_{\text{eff}}$) degradation observed in devices with sub-20 nm In$_{0.53}$Ga$_{0.47}$As channel thickness [10]. With this in mind, we varied $t_{\text{InGaAs}}$ for a fixed $N_d$ value in order to investigate the behavior of fully depleted devices.

To assist in the device analysis, self-consistent Poisson-Schrödinger calculations [11] were performed for ideal Pd/Al$_2$O$_3$/n-In$_{0.53}$Ga$_{0.47}$As/p-In$_{0.52}$Al$_{0.48}$As/p$^+$-InP device structures. In the calculations, the work function ($W_f$) of Pd on Al$_2$O$_3$, the Al$_2$O$_3$ film thickness ($t_{\text{ox}}$) and the Al$_2$O$_3$ $k$-value were set to 4.7 eV [12], 8.5 nm (see section 6.3) and 8.6 [6, 13, 14], respectively. The only parameter that was manually adjusted was the $N_d$ in the In$_{0.53}$Ga$_{0.47}$As channel. The adjustment procedure, which yielded a $N_d$ value of $9 \times 10^{17}$/cm$^3$ ($W_d^{\text{max}} \sim 34.5$ nm), will be presented in sub-section 6.4.3. It is noted that we could not extract $N_d$ from the minimum capacitance ($C_{\text{min}}$) of the high-frequency capacitance-voltage (C-V) characteristic of the device metal-oxide-semiconductor (MOS) gate stack since $t_{\text{InGaAs}} < W_d^{\text{max}}$.

Figure 6.2 compares the quasi-static (Q-S) C-V characteristics calculated for $t_{\text{InGaAs}}$ values of 100, 32 and 24 nm. The calculations revealed a flat-band capacitance ($C_{fb}$) of 0.52 µF/cm$^2$ along with a flat-band voltage ($V_{fb}$) of 0.2 V. For $t_{\text{InGaAs}} = 100$ nm ($< W_d^{\text{max}}$) the quasi-static C-V characteristic presents the expected shape of an n-type MOS structure: a decreasing capacitance
Figure 6.3: Conduction band diagrams of Pd/Al₂O₃/n-In₀.₅₃Ga₀.₄₇As/p-In₀.₅₂Al₀.₄₈As/p-InP structures obtained from self-consistent Poisson-Schrödinger calculations. Diagrams of a 32-nm-thick In₀.₅₃Ga₀.₄₇As channel device showing (a) the flat-band and (b) the fully depleted conditions. The Fermi level needs to move 0.07 eV above the conduction band edge ($E_C$) to reach flat-band and 0.54 eV below $E_C$ to reach full depletion. Diagrams of a 24-nm-thick In₀.₅₃Ga₀.₄₇As channel device showing (c) the flat-band and (d) the fully depleted conditions. The Fermi level needs to move 0.07 eV above $E_C$ to reach flat-band and 0.31 eV below $E_C$ to reach full depletion.
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Figure 6.4: (a) Energy range required to move from flat-band to full depletion as a function of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel thickness ($t_{\text{InGaAs}}$). The values were obtained from self-consistent Poisson-Schrödinger calculations. (b) Comparison of the $D_{it}$ values reported for $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS structures [15-20].
going from accumulation \((V_g > V_{fb})\) to depletion \((V_T < V_g < V_{fb})\), a \(C_{min}\) set by \(N_d\) and a sharp increase in capacitance going from depletion to inversion \((V_g < V_T)\). However, for \(t_{InGaAs} = 32\) and \(24\) nm \((< W_{max})\), the curves feature a \(C_{min}\) falling down to a negligible value of \(\sim 30\) nF/cm\(^2\), consistent with fully depleted structures. This comparison also highlights the fact that a thinner In\(_{0.53}\)Ga\(_{0.47}\)As channel requires a smaller \(V_g\) sweep to move from flat-band (ON-state) to fully depleted (OFF-state) and \textit{vice versa}, which is highly desirable for low power device applications. A second advantage arising from the scaling of \(t_{InGaAs}\) can be observed on the band diagrams of the 32 and 24-nm-thick In\(_{0.53}\)Ga\(_{0.47}\)As channel devices shown in Figure 6.3.

At flat-band [Figure 6.3(a) and (c)], the Fermi levels in both devices are located 0.07 eV above the conduction band. However, to reach full depletion in the 32-nm-thick In\(_{0.53}\)Ga\(_{0.47}\)As channel device, the Fermi level has to move to 0.54 eV below the conduction band edge \((E_C)\) [Figure 6.3(b)] while it only has to move 0.31 eV below \(E_C\) in the 24-nm-thick In\(_{0.53}\)Ga\(_{0.47}\)As channel device [Figure 6.3(d)]. From Figure 6.4(a), it is clear that the range of energy required to move from flat-band to fully depleted scales with \(t_{InGaAs}\). The review of the \(D_{it}\) energy profile reported for Al\(_2\)O\(_3\)/In\(_{0.53}\)Ga\(_{0.47}\)As MOS structures [1526] [Figure 6.4(b)] shows that this trend is particularly advantageous to Al\(_2\)O\(_3\)/In\(_{0.53}\)Ga\(_{0.47}\)As MOS devices. Indeed, while \(D_{it}\) values in the low-10\(^{11}\) to mid-10\(^{12}\) \(\text{cm}^{-2}\) eV range are generally reported for the upper part of the In\(_{0.53}\)Ga\(_{0.47}\)As bandgap, much higher \(D_{it}\) values in the 10\(^{13}\) \(\text{cm}^{-2}\) eV range are observed in the lower part of the In\(_{0.53}\)Ga\(_{0.47}\)As bandgap.

Consequently, we propose to scale \(t_{InGaAs}\) in order to avoid device operation in the lower part of the In\(_{0.53}\)Ga\(_{0.47}\)As bandgap and, therefore, achieve better switching performance.

### 6.2 Channel Thinning by Digital Etching

Figure 6.5 shows a diagram and a transmission electron microscopy (TEM) cross-section image of the n-In\(_{0.53}\)Ga\(_{0.47}\)As (32 nm)/p-In\(_{0.52}\)Al\(_{0.48}\)As (500 nm) device structure grown by metal-organic vapor phase epitaxy (MOVPE) on p\(^+\)-InP substrates. The nominal doping was \(2 \times 10^{18}\) /cm\(^3\) in the n-In\(_{0.53}\)Ga\(_{0.47}\)As and \(8 \times 10^{15}\) /cm\(^3\) in the p-In\(_{0.52}\)Al\(_{0.48}\)As. We used a 10\% H\(_2\)O\(_2\) / 10\% HCl digital etch (DE) process [27] for the thinning of the n-In\(_{0.53}\)Ga\(_{0.47}\)As channel. The DE was characterized in terms of etch rate and surface roughness directly on the device structure.

Spectroscopic ellipsometry (SE) measurements were performed to monitor the In\(_{0.53}\)Ga\(_{0.47}\)As etch rate and thickness (Figure 6.6). SE enables direct extraction of film thicknesses of multilayer structures through the fitting of the amplitude ratio and phase shift components measured upon reflection over a wide range of wavelength going from 245 nm to 1690 nm. The excellent agreement obtained between the TEM (Figure 6.5) and SE measurements performed before DE (Figure 6.6) validates the SE measurement technique. A DE rate of 0.8 nm/cycle was extracted.
6.2. Channel Thinning by Digital Etching

Figure 6.5: Diagram and cross-section transmission electron microscopy (TEM) image of the MOVPE grown $n$-In$_{0.53}$Ga$_{0.47}$As (32 nm)/$p$-In$_{0.52}$Al$_{0.48}$As (500 nm)/$p^+$-InP wafer structure used for the digital etch (DE) process characterization and for the device fabrication.

Figure 6.6: In$_{0.53}$Ga$_{0.47}$As channel thinning using a H$_2$O$_2$/HCl digital etch (DE) process [27]. Excellent agreement between spectroscopic ellipsometry (SE) and TEM (Figure 6.5) measurements was obtained prior to DE. An etch rate of 0.8 nm/cycle was extracted from the linear fit. The $R^2 = 0.999$ of the linear fit confirms the excellent control of the In$_{0.53}$Ga$_{0.47}$As etch rate.
Figure 6.7: Atomic force microscopy (AFM) topography data of $n$-In$_{0.53}$Ga$_{0.47}$As (a) before digital etch (DE) and after (b) a 10-cycle, (c) a 15-cycle and (d) a 20-cycle DE. The measurements were taken over 1 µm × 1 µm scan areas. The AFM measurements were performed by M. Burke (Tyndall).

Table 6.1: Root mean square (RMS) surface roughness data from AFM measurements taken on $n$-In$_{0.53}$Ga$_{0.47}$As before digital etch (DE) and after a 10-cycle, 15-cycle and 20-cycle (DE) (Figure 6.7). The quoted values represent the mean, maximum and minimum from four measurements at separate locations (each on a 1 µm × 1 µm scan area). The uncertainties on the mean values are given by the standard deviation.

<table>
<thead>
<tr>
<th>RMS</th>
<th>No Etch</th>
<th>DE Cycles</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>10</td>
<td>15</td>
</tr>
<tr>
<td>Mean (nm)</td>
<td>0.20 ± 0.01</td>
<td>0.21 ± 0.01</td>
</tr>
<tr>
<td>Max. (nm)</td>
<td>0.20</td>
<td>0.23</td>
</tr>
<tr>
<td>Min. (nm)</td>
<td>0.19</td>
<td>0.20</td>
</tr>
</tbody>
</table>
6.3. Fabrication of Planar Gate-enclosed Junctionless MOSFETs

from the linear fit of the SE measurements vs number of etch cycles. The $R^2$ of 0.999 confirms the excellent control of the In$_{0.53}$Ga$_{0.47}$As etch rate. It is noted that SE provides a more direct and more accurate alternative to the procedure reported in [28] for a similar process characterization. Atomic force microscopy (AFM) topography data were acquired before DE [Figure 6.7(a)] and after 10-cycle [Figure 6.7(b)], 15-cycle [Figure 6.7(c)] and 20-cycle [Figure 6.7(d)] DE in order to investigate the impact of DE on the In$_{0.53}$Ga$_{0.47}$As surface roughness. The corresponding root mean square (RMS) surface roughness values are listed in Table 6.1 in terms of mean, maximum and minimum values, obtained from four measurements at separate locations. The mean RMS surface roughness gradually increases from 0.20 ± 0.01 nm before DE to 0.28 ± 0.01 nm after a 20-cycle DE in line with [28].

6.3 Fabrication of Planar Gate-enclosed Junctionless MOSFETs

Five samples consisting of a 32-nm-thick $n$-In$_{0.53}$Ga$_{0.47}$As on a 500-nm-thick $p$-In$_{0.52}$Al$_{0.48}$As ($N_d = 8 \times 10^{15} \, /cm^3$) barrier grown by MOVPE on $p'$-InP substrates (Figure 6.5) were dedicated to the study of the impact of $t_{InGaAs}$ on the performance of junctionless In$_{0.53}$Ga$_{0.47}$As MOSFETs. Although a $N_d$ of $2 \times 10^{18} \, /cm^3$ was targeted for the In$_{0.53}$Ga$_{0.47}$As channel, our analysis revealed a $N_d$ of $9 \times 10^{17} \, /cm^3$ (see sub-section 6.4.3). As already mentioned in section 6.1 (122), the $N_d$ could not be measured experimentally. Moreover, no dopant calibration run was performed prior to the growth of the structure. While devices were fabricated directly on the first sample ($t_{InGaAs} = 32$ nm), additional DEs were performed on the 4 remaining samples to thin down the top In$_{0.53}$Ga$_{0.47}$As layers prior to device fabrication. The numbers of etch cycles were adjusted in order to obtain $t_{InGaAs} = 24, 20, 16$ and 12 nm. A non-self-aligned gate-enclosed layout was employed to simplify the fabrication process flow of the planar junctionless MOSFETs. A surface passivation in 10% (NH$_4$)$_2$S for 30 min [16, 21] was performed before atomic layer deposition (ALD) of an 8.5-nm-thick Al$_2$O$_3$ gate oxide film [Figure 6.8(a)]. It is noted that the $t_{ox}$ of 8.5 nm was measured directly on the device samples by SE. A 200-nm-thick Pd gate was formed by e-beam evaporation and lift-off [Figure 6.8(b)]. The Al$_2$O$_3$ on the S/D contact areas was etched in dilute HF [Figure 6.8(c)]. A 20 sec surface treatment in 10% NH$_4$OH was performed prior to S/D contact formation by e-beam evaporation of a Au (14 nm)/Ge (14 nm)/Au (14 nm)/Ni (11 nm)/Au (200 nm) stack [29] and lift-off [Figure 6.8(d)].

The fabricated gate-enclosed junctionless In$_{0.53}$Ga$_{0.47}$As MOSFETs featured a drain radius ($r_d$), a gate inner radius ($r_{in}^g$), a gate outer radius ($r_{out}^g$) and source radius ($r_s$) are 35, 45, 105 and 135 µm, respectively [Figure 6.8(e)].
Figure 6.8: Fabrication process flow of planar Gate-enclosed Junctionless In$_{0.53}$Ga$_{0.47}$As MOSFETs including (a) 10% (NH$_4$)$_2$S for 30 min passivation [16, 21] prior to ALD Al$_2$O$_3$, (8.5 nm), (b) Pd (200 nm) gate lift-off, (c) Al$_2$O$_3$ etch in dilute HF for S/D contact opening and (d) 10% NH$_4$OH for 20 sec surface treatment followed by Au (14 nm)/Ge (14 nm)/Au (14 nm)/Ni (11 nm)/Au (200 nm) [29] S/D contact lift-off. (e) Cross-section diagram of a gate-enclosed junctionless MOSFET architecture. The drain radius ($r_D$), gate inner radius ($r_{g}^{in}$), gate outer radius ($r_{g}^{out}$) and source radius ($r_S$) are 35, 45, 105 and 135 µm, respectively.
6.4 Analysis of Planar Gate-enclosed Junctionless MOSFETs

6.4.1 Impact of Channel Thickness on Device Performance

Figure 6.9 shows a well behaved $I_d-V_{ds}$ output characteristic obtained for a planar gate-enclosed junctionless $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSFET featuring a 24-nm-thick $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel. The output characteristic is normalized to $W/L = 1$ using [30]:

$$
(W/L)_{\text{eff}} = 2\pi \left[\ln\left(\frac{r_{\text{out}}}{r_{\text{in}}}\right)\right]^{-1}
$$

(6.2)

A $(W/L)_{\text{eff}}$ of 7.41 was obtained based on the device dimensions shown in Figure 6.8(e). The normalized (measured) drive current at $V_g = 0.5$ V and $V_{ds} = 1$ V is 260 $\mu$A/µm (1.93 mA).

Figure 6.10 compares the $I_d-V_g$ characteristics measured at a $V_{ds} = 50$ mV on devices featuring a $t_{\text{InGaAs}}$ of 32, 24, 20, 16 and 12 nm. The $I_d-V_g$ transfer characteristics are plotted in log scale to highlight the $I_{ON}/I_{OFF}$ and subthreshold swing (SS) of each device. The 20-nm-thick channel device exhibits the highest $I_{ON}/I_{OFF}$ ($1.5 \times 10^5$) [Figure 6.11]. It is interesting to note that for $t_{\text{InGaAs}} < 20$ nm the $I_{ON}/I_{OFF}$ reduces due to a degradation of the $I_{ON}$, while for $t_{\text{InGaAs}} > 20$ nm the $I_{ON}/I_{OFF}$ reduces due to an increase in $I_{OFF}$. Moreover, scaling $t_{\text{InGaAs}}$ from 24 nm

$^2$I$_{\text{ON}}$/I$_{\text{OFF}}$ is defined here as the ratio between the maximum and minimum drain currents, irrespective of the gate voltage swing.
Figure 6.10: $I_d$-$V_g$ transfer characteristics measured at $V_{ds} = 50$ mV on planar gate-enclosed junctionless In$_{0.53}$Ga$_{0.47}$As MOSFETs with $t_{InGaAs} = 32$, 24, 20, 16 and 12 nm. A $(W/L)_{eff}$ of 7.41 was used for the $W/L$ normalization of $I_d$.

To 16 nm reduces the SS from 178 mV/dec. to 115 mV/dec. [Figure 6.11]. We suggest that the severe degradation of the $I_{ON}$ in the 12-nm-thick In$_{0.53}$Ga$_{0.47}$As channel device is responsible for the change of trend of SS going from a $t_{InGaAs}$ value of 16 nm to a value of 12 nm. It is noted that the SS of the 32-nm-thick In$_{0.53}$Ga$_{0.47}$As channel device could not be extracted due to an excessive $I_{OFF}$.

The $I$-$V$ characteristic of the $n$-In$_{0.53}$Ga$_{0.47}$As/$p$-In$_{0.52}$Al$_{0.48}$As heterojunction diode presented in Figure 6.12 indicates a forward to reverse bias current ratio of $4 \times 10^7$. This suggests excellent junction isolation and, therefore, rules out the substrate leakage as the cause of high $I_{OFF}$ in the 32-nm-thick In$_{0.53}$Ga$_{0.47}$As channel device.

Figure 6.13(a) shows the $C_{gc}$-$V_g$ characteristic of a 32-nm-thick In$_{0.53}$Ga$_{0.47}$As-channel device measured at a frequency of 1 MHz. The measured capacitance of $\sim 0.2$ $\mu$F/cm$^2$ at $V_g = -2$ V indicates that the device is not fully depleted. We compared this capacitance value to the calculated theoretical $C_{min}$ for a range of $N_d$ values [inset Figure 6.13(a)]. The calculations revealed that a capacitance of 0.2 $\mu$F/cm$^2$ can only be achieved for $N_d < 1.1 \times 10^{18}$ /cm$^3$.

This represents an important finding that gives further confidence in the $N_d$ extraction that will be presented in sub-section 6.4.3. Figure 6.13(b) compares the evolution of the experimental $C_{gc}$-$V_g$ characteristic with the results of the simulation.

\[\text{The } C_{gc}-V_g \text{ characteristic was obtained using a measurement configuration where the source and drain terminals are shorted and connected to the high of the impedance meter, the gate terminal is connected to the low and the substrate is left floating.}\]
6.4. Analysis of Planar Gate-enclosed Junctionless MOSFETs

Figure 6.11: (a) $I_{ON}/I_{OFF}$ vs $t_{InGaAs}$. The best $I_{ON}/I_{OFF}$ value of $1.5 \times 10^5$ was obtained with $t_{InGaAs} = 20$ nm. For $t_{InGaAs} > 20$ nm, $I_{ON}/I_{OFF}$ is degraded due to an increase in $I_{OFF}$. For $t_{InGaAs} < 20$ nm, the $I_{ON}/I_{OFF}$ is degraded due to a decrease in $I_{ON}$. (b) Subthreshold swing ($SS$) vs $t_{InGaAs}$. $SS$ scaling with $t_{InGaAs}$ observed for $t_{InGaAs}$ reducing from 24 nm to 16 nm. The lowest $SS$ (115 mV/dec.) was obtained with $t_{InGaAs} = 16$ nm.
Chapter 6. Impact of Channel Thickness on Junctionless MOSFET Performance

Figure 6.12: $I-V$ characteristic of a $n$-$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/p$-$\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ heterojunction diode fabricated on the wafer structure shown in Figure 6.5. More than 7 orders of magnitude between the forward and reverse current is observed, indicating excellent junction isolation and ideal $E_F-E_C$ vs $V_g$ curves, which suggest that the Fermi level is pinned $\sim 0.45$ eV below $E_C$. This is consistent with high $D_{it}$ levels towards the lower part of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ bandgap [Figure 6.4(b)]. This Fermi level pinning prevents the 32-nm-thick $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$-channel device from reaching full depletion, in agreement with the high $I_{OFF}$ observed in the device $I_d-V_g$ characteristic shown in Figure 6.10.

6.4.2 Density of Interface Traps

Figure 6.14(a) shows a multi-frequency $C_{gc}-V_g$ characteristic of a device featuring a 24-nm-thick $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel. The sharp drop of capacitance down to a $C_{min}$ of $\sim 40$ nF/cm$^2$ confirms that the device is fully depleted at $V_g < -0.8$ V. In the $V_g$ range going from -0.5 V to 0 V (towards accumulation), a very low frequency dispersion is observed, suggesting a low $D_{it}$ in the upper part of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ bandgap. A $D_{it}$ profile [Figure 6.14(b)] was obtained from the conductance method [31] applied to the capacitance and conductance data shown in Figure 6.14(a) and for an oxide capacitance $C_{ox}$ of 0.895 µF/cm$^2$. The inset of Figure 6.14(a) shows the evolution of the peak of conductance normalized to the angular frequency ($G/\omega$) across the $V_g$ range where the conductance method is applicable. As the frequency increases from 400 Hz to 100 kHz, the $G/\omega$ peak reduces and moves from -1.4 V to -0.8 V, consistent with a reducing $D_{it}$ going from the middle of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ bandgap towards conduction band edge. This trend was confirmed by the $D_{it}$ profile obtained from the high-low method applied to the 100 kHz (high $\omega$) and 100 kHz (low $\omega$). It is noted that a $C_{gc}-V_g$ trace measured at a frequency of 1 MHz would have provided a better approximation of the true high-frequency response. Due to the large series resistance ($R_{series}$) arising from the use of a very thin
6.4. Analysis of Planar Gate-enclosed Junctionless MOSFETs

Figure 6.13: (a) $C_{gc}$-$V_g$ characteristics measured at a frequency of 1 MHz on planar gate-enclosed junctionless In$_{0.53}$Ga$_{0.47}$As MOSFETs with $t_{InGaAs} = 32$ nm. Inset: Calculated minimum capacitance ($C_{min}$) vs In$_{0.53}$Ga$_{0.47}$As doping ($N_d$). A measured $C_{min}$ of $\sim 0.2 \mu$F/cm$^2$ at $V_g = -2$ V suggests a $N_d < 1.1 \times 10^{18}$ /cm$^3$. (b) Fermi level position at the Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As interface in an ideal and in the fabricated devices. In the fabricated device, the Fermi level is pinned above $E_F - E_C = -0.54$ eV [Figure 6.3(b)], preventing the full depletion of the 32-nm-thick In$_{0.53}$Ga$_{0.47}$As channel.
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Figure 6.14: (a) Multi-frequency $C_{gc}-V_g$ characteristic of a 24-nm-thick In$_{0.53}$Ga$_{0.47}$As channel device showing low frequency dispersion near accumulation. The low $C_{min}$ of $\sim$ 40 nF/cm$^2$ suggests full depletion at $V_g < -1$ V. Inset: Evolution of the conductance peak normalized to angular frequency ($G/\omega$). (b) Comparison of the conductance and high-low methods for the extraction of the density of interface traps ($D_{it}$). Inset: Fermi level position at the Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As interface in an ideal and in the fabricated devices. In the fabricated device, the Fermi level reaches $E_F-E_C = -0.3$ eV at $V_g = -1$ V, demonstrating the full depletion of the 24-nm-thick In$_{0.53}$Ga$_{0.47}$As channel.
Hz (low) capacitance traces shown in Figure 6.14(a). It is noted that the presence of a peak at $\sim -1.4$ V in the 100 Hz capacitance response suggests a $D_{it}$ response rather than a minority carrier response, providing more confidence in the $D_{it}$ extraction using the high-low method [16]. The inset of Figure 6.14(b) shows the Fermi level position at the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface as a function of $V_g$ in an ideal and in the fabricated 24-nm-thick $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel device. In contrast to the case of the 32-nm-thick $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel device, the Fermi level in the 24-nm-thick $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel device can be moved below the energy level required to reach full depletion (i.e.: $E_F-E_C = -0.31$ eV [Figure 6.3(d)]), in agreement with the good $I_{ON}/I_{OFF}$ of $3.3 \times 10^4$ obtained with $t_{\text{InGaAs}} = 24$ nm [Figure 6.11(a)]. The reasonably low $D_{it}$ values of $1.3 \times 10^{12}$ to $5.2 \times 10^{12} \text{cm}^{-2}\text{eV}^{-1}$ obtained within the 0.3 eV energy range below $E_C$ suggest that the $\text{DE}$ process does not significantly degrade the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface.

### 6.4.3 Surface Carrier Concentration, Substrate Doping and Dark Space

Figure 6.15(a) compares the 100-kHz $C_{gc}-V_g$ characteristics measured on the 24, 20 and 16-nm-thick $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel devices. The theoretical $C_{fb}$ obtained from the calculation was used in conjunction with the experimental $C_{gc}-V_g$ characteristics in order to extract a flat-band voltage of 0 V. The total surface charge density at flat-band ($N_{tot}$), including the surface carrier density at flat-band ($N_s$) along with a $D_{it}$ contribution, was obtained by integrating the experimental $C_{gc}$ curve across a $V_g$ range where the device goes from full depletion to flat-band [Figure 6.15(b)]. Following the calculation of $N_{tot}$, we extracted the free charge density in the conduction band ($N_s$) by subtracting to the integrated $D_{it}$ integrated across the energy range of operation of the device from $N_{tot}$. This procedure was performed for $t_{\text{InGaAs}} = 24$, 20 and 16 nm [Figure 6.15(b)]. We also calculated the theoretical $N_s$ at flat-band for a range of $t_{\text{InGaAs}}$ and $N_d$ [Figure 6.15(b)]. An excellent match was obtained between the experimental $N_s$ and the theoretical $N_s$ for $N_d = 9 \times 10^{17} \text{cm}^{-3}$.

We extrapolated the curves obtained from the calculations in order to show the $x$-intercepts, which represent the amount of surface depletion (dark space) arising from quantum-mechanical effects pushing the carriers away from the top and bottom interfaces. This effect is more significant in an $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ structure than in a $\text{SiO}_2/\text{SOI}$ structure. Indeed, a total dark space thickness accounting for the top and bottom interfaces ($t_{dark}$) of 7.5 nm is extracted for the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ structure with a channel $N_d$ of $9 \times 10^{17} \text{cm}^{-3}$, while a $t_{dark}$ of only 1.8 nm is obtained for the $\text{SiO}_2/\text{SOI}$ structure at the same channel $N_d$. We suggest that this issue could partly explain the severe $I_{ON}$ degradation observed for $t_{\text{InGaAs}} = 16$ and 12 nm [Figure 6.10]. The calculations also indicate that $t_{dark}$ could be reduced by increasing $N_d$, in agreement with the trend reported for high-$k$/Ge MOSFETs in [32].

(24 nm) $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel, our measurements were limited to a maximum frequency of 100 kHz.
Figure 6.15: (a) 100-kHz $C_{gc}$-$V_g$ characteristics measured on 24, 20 and 16-nm-thick In$_{0.53}$Ga$_{0.47}$As-channel devices. The theoretical flat-band capacitance ($C_{fb}$) obtained from calculations is reported on the curves to extract a flat-band voltage ($V_{fb}$) of 0 V. (b) Plot of the surface carrier density ($N_s$) at flat-band vs $t_{InGaAs}$. The total charge density ($N_{tot}$) was obtained by integrating $C_{gc}$. $N_s$ was obtained by correcting $N_{tot}$ for the density of interface trap ($D_{it}$) integrated across the energy range of operation of the corresponding device. The $N_s$ at flat-band vs $t_{InGaAs}$ curves were calculated for ideal devices with $N_d = 1.1 \times 10^{18}$, $9 \times 10^{17}$ and $7 \times 10^{17}$ /cm$^3$. The $x$-intercepts obtained by extrapolation of the curves yielded the total dark space thickness values (accounting for the top and bottom interfaces). The case of a SiO$_2$/Si-on-isulator (SOI) structure with a channel $N_d$ of $9 \times 10^{17}$ /cm$^3$ is shown for comparison.
6.4.4 Series Resistance

Figure 6.16(a) represents the circuit equivalent model of a gate-enclosed junctionless device, where \( R_{c,D} \) and \( R_{c,S} \) are the contact resistances to the drain and source, respectively; \( R_D, R_S, R_{D\rightarrow G} \) and \( R_{G\rightarrow S} \) are the series resistances associated with the sheet resistance of the drain area, source area, non-gated drain-to-gate area and non-gated gate-to-source area, respectively; and \( R_{ch} \) is the channel resistance, which is controlled by the gate. In order to estimate the contribution of \( R_D, R_S, R_{D\rightarrow G}, \) and \( R_{G\rightarrow S} \), we start with the expression of the resistance associated with the sheet resistance of a linear bar of semiconductor:

\[
R = R_{\text{sheet}} \cdot (W/L)^{-1} = [q \cdot \mu \cdot n \cdot t_{\text{bar}} \cdot (W/L)]^{-1}
\]  \hspace{1cm} (6.3)

where \( R_{\text{sheet}} \) is the sheet resistance of the semiconductor material, \( q \) is the charge of an electron, \( \mu \) is the carrier mobility, \( n \) is the carrier density, and \( t_{\text{bar}} \), \( W \) and \( L \) are the thickness, length and width of the bar, respectively. To obtain the resistance of a ring structure with \( r_{\text{in}} \) and \( r_{\text{out}} \) as inner and outer radii, the \( (W/L) \) ratio in Equation 6.3 is replaced by the \( (W/L)_{\text{eff}} \) of Equation 6.2, yielding:

\[
R_{\text{ring}} = [q \cdot \mu \cdot n \cdot t \cdot (W/L)_{\text{eff}}]^{-1} = \ln[(r_{\text{out}}/r_{\text{in}}) [2\pi q \cdot \mu \cdot n \cdot t]^{-1}]
\]  \hspace{1cm} (6.4)

Considering the dimensions of the planar gate-enclosed junctionless In\(_{0.53}\)Ga\(_{0.47}\)As MOSFETs shown in Figure 6.8(e), and assuming conservative values of \( 5 \times 10^{-6} \) \( \Omega \cdot \text{cm}^2 \) for the specific contact resistance, 0.5 \( \mu \text{m} \) for the transfer length and 2000 \( \text{cm}^2/\text{V.s} \) for the carrier mobility in n-In\(_{0.53}\)Ga\(_{0.47}\)As along with the extracted In\(_{0.53}\)Ga\(_{0.47}\)As \( N_d \) of \( 9 \times 10^{17} \) \( /\text{cm}^3 \), we calculated each contribution to the total series resistance \( (R_{\text{series}}) \). The calculations revealed that the series resistance contribution associated with the sheet resistances of the non-gated areas \( (R_{D\rightarrow G} \) and \( R_{G\rightarrow S}) \), represented at least 91% of \( R_{\text{series}} \) (depending on \( t_{\text{InGaAs}} \), suggesting that \( R_{\text{series}} \approx (R_{D\rightarrow G} + R_{G\rightarrow S}) \). As a result, the sheet resistances of the drain \( (R_D) \) and source \( (R_S) \) areas and contact resistances to the drain \( (R_{c,D}) \) and source \( (R_{c,S}) \) areas can be neglected and the circuit equivalent model for the series resistance shown in Figure 6.16(a) can be simplified to that shown in Figure 6.16(b). The total resistance \( (R_{\text{tot}}) \) is obtained from a device \( I_d-V_g \) characteristic:

\[
R_{\text{tot}} = V_{ds}/I_d = R_{ch} + R_{\text{series}}
\]  \hspace{1cm} (6.5)

It is noted that the \( R_{\text{sheet}} \) of the semiconductor underneath the gate is controlled by \( V_g \). In an ideal device, the \( R_{\text{sheet}} \) of the channel area is the same as that of the non-gated area when \( V_g \) is set to the flat-band voltage \( (V_{fb}) \). The presence of a fixed charge \( (Q_{\text{fixed}}) \) in the Al\(_2\)O\(_3\)/In\(_{0.53}\)Ga\(_{0.47}\)As system was reported in [33, 34]. \( Q_{\text{fixed}} \) has two components: a fixed negative charge at the Al\(_2\)O\(_3\)/In\(_{0.53}\)Ga\(_{0.47}\)As interface and a fixed positive charge distributed
Figure 6.16: (a) Circuit equivalent model of the device. $R_{c,D}$ and $R_{c,S}$ are the resistances of the contacts to the drain and source areas, respectively. $R_D$, $R_S$, $R_{D-to-G}$ and $R_{G-to-S}$ are the resistances associated with the sheet resistance of the drain, source, drain-to-source and gate-to-source areas, respectively. $R_{ch}$ is the resistance of the channel. (b) Simplified circuit equivalent model assuming a specific contact resistance ($\rho_c$) of $5 \times 10^{-6} \ \Omega \text{cm}^2$, a transfer length ($L_t$) of 0.5 $\mu$m and a mobility in the n-In$_{0.53}$Ga$_{0.47}$As ($N_d = 9 \times 10^{17} \ /\text{cm}^3$) layer of 2000 cm$^2$/V.s. (c) Comparison of the series resistance ($R_{series}$) vs $t_{\text{InGaAs}}$ extracted from the $I_d-V_g$ curves shown in Figure 6.10 and calculated from the simplified equivalent circuit model shown in (b) with estimated and/or extracted surface carrier density [noted $n,t$ in Equation 6.4] and carrier mobility ($\mu$) parameters.
throughout the bulk of the Al\textsubscript{2}O\textsubscript{3} film. It is noted that \(Q_{\text{fixed}}\) plays an important role in the
device operation, as it not only degrades \(\mu_{\text{eff}}\) due to Coulomb scattering, but it also impacts
\(R_{\text{series}}\) through \(R_{D\rightarrow G}\) and \(R_{G\rightarrow S}\). Indeed, a negative (positive) fixed charge will deplete
(accumulate) the non-gated \textit{n}-type semiconductor, increasing (decreasing) the contribution of
\(R_{D\rightarrow G}\) and \(R_{G\rightarrow S}\) to \(R_{\text{series}}\).

A value of -0.2 V, corresponding to the flat-band voltage shift \((\Delta V_{fb})\) induced by \(Q_{\text{fixed}}\), was obtained by comparing the experimen-
tal \(V_{fb}\) of 0 V (Figure 6.15a) to the theoretical \(V_{fb}\) of 0.2 V (Figure 6.2). The negative \(\Delta V_{fb}\) indicates a net positive surface-equivalent fixed charge in the Al\textsubscript{2}O\textsubscript{3}, consistent with [34] for \(t_{ox} = 8.5\) nm, suggesting that the non-gated areas are in
slight accumulation. Therefore, applying \(V_{g} = (V_{fb} - \Delta V_{fb})\) to the gate terminal enables to set
the channel at the same accumulation level as that of the non-gated areas, leading to a uniform
\(R_{\text{sheet}}\) between the source and drain terminals. Under this particular condition, the channel and
non-gated areas can be considered as a single disk of uniform \(R_{\text{sheet}}\), allowing the calculation of
\(R_{\text{tot}}\) using Equation 6.5 and the extraction of \(R_{D\rightarrow G}\), \(R_{G\rightarrow S}\) and \(R_{\text{series}}\) with Equation 6.4.

Figure 6.16(c) shows the \(R_{\text{series}}\) extracted for the 32, 24, 20, 16 and 12-nm-thick In\textsubscript{0.53}Ga\textsubscript{0.47}As
channel devices. A dramatic increase in \(R_{\text{series}}\) is observed for \(t_{\text{InGaAs}} < 20\) nm. The calculated
\(R_{\text{series}}\) curves, obtained using the simplified equivalent circuit model shown in Figure 6.16(b),
Equation 6.4 and the estimated and/or extracted surface carrier density [noted \(n.t\) in Equation 6.4]
and carrier mobility \((\mu)\) parameters, indicate that the dramatic increase in \(R_{\text{series}}\) is
observed for \(t_{\text{InGaAs}} < 20\) nm cannot be entirely explained by the reduction in surface carrier
density arising from the scaling of \(t_{\text{InGaAs}}\) and the dark space phenomenon. This suggests that
a \(\mu\) degradation for \(t_{\text{InGaAs}} < 20\) nm, consistent with [10].

6.4.5 Effective Mobility

The effect of \(t_{\text{InGaAs}}\) on the \(\mu_{\text{eff}}\) of planar gate-enclosed junctionless In\textsubscript{0.53}Ga\textsubscript{0.47}As MOSFETs
is shown in Figure 6.17. It is noted that the \(\mu_{\text{eff}}\) values are corrected for \(R_{\text{series}}\) and \(D_{it}\). The
24 and 20-nm-thick In\textsubscript{0.53}Ga\textsubscript{0.47}As channel devices feature a peak \(\mu_{\text{eff}}\) at flat-band of 2130 and
1975 cm\textsuperscript{2}/V.s, respectively. A marked drop in \(\mu_{\text{eff}}\) is observed on the 16-nm-thick In\textsubscript{0.53}Ga\textsubscript{0.47}As
channel device. This agrees with [10] and is also consistent with the lower \(I_{\text{ON}}\) and higher
\(R_{\text{series}}\) obtained in Sub-sections 6.4.1 and 6.4.4, respectively. We calculated the \(R_{\text{series}}\) using the
simplified equivalent circuit model with the extracted \(N_{s}\) and \(\mu_{\text{eff}}\) at flat-band (Figure 6.16).
Excellent agreement was obtained with the \(R_{\text{series}}\) extracted from the \(I_{d}-V_{g}\) curves, confirming
that the sharp increase in \(R_{\text{series}}\) for \(t_{\text{InGaAs}} < 16\) nm is mainly due to a \(\mu_{\text{eff}}\) degradation.

The \(\mu_{\text{eff}}\) of an inversion-mode Pd/Al\textsubscript{2}O\textsubscript{3}/In\textsubscript{0.53}Ga\textsubscript{0.47}As MOSFET measured at a temperature \((T)\) of 35 K is also shown for comparison. Since the \(\mu_{\text{eff}}\) values of the junctionless device
Figure 6.17: Effective electron mobility ($\mu_{\text{eff}}$) vs $N_s$. Values of $\mu_{\text{eff}}$ at flat-band of 2130, 1975 and 310 cm$^2$/V.s were obtained for planar gate-enclosed junctionless In$_{0.53}$Ga$_{0.47}$As MOSFETs featuring $t_{\text{InGaAs}}$ of 24, 20 and 16 nm, respectively. The abrupt drop in $\mu_{\text{eff}}$ observed for $t_{\text{InGaAs}} = 16$ nm is consistent with [10]. The $\mu_{\text{eff}}$ of an inversion-mode Pd/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOSFET with implanted S/D measured at a temperature ($T$) of 35 K (see [5]) is shown for comparison. The $\mu_{\text{eff}}$ data of the junctionless devices are corrected for $R_{\text{series}}$ and $D_{\text{it}}$. The $\mu_{\text{eff}}$ data of the inversion-mode device is only corrected for $R_{\text{series}}$ but the reduced $T$ acts as a $D_{\text{it}}$ correction [35].
are corrected for $D_{it}$, we selected a $T$ of 35 K for the $\mu_{\text{eff}}$ of the inversion-mode device in order to obtain a fair comparison between the two devices. Indeed, as reported in [35], low temperature measurements can be used to "freeze" the contribution of the $D_{it}$ located near the conduction band and obtain a $D_{it}$ correction. Moreover, we showed in Chapter 5 that the $\mu_{\text{eff}}$ of the inversion-mode device was dominated by surface roughness scattering and that phonon scattering had no significant impact at $T = 292$ K, indicating that the $\mu_{\text{eff}}$ at 35 K represents a good estimate of the $\mu_{\text{eff}}$ at 292 K corrected for $D_{it}$. The severe $\mu_{\text{eff}}$ degradation due to surface roughness scattering in the inversion-mode device arises from the use of a 600°C for 30 sec implant activation anneal process, which is required to form the S/D terminals of the device. The junctionless device concept obviates the need for such high temperature anneal processes. Moreover, since the AFM measurements taken on the In$_{0.53}$Ga$_{0.47}$As channel after 10, 15 and 20 DE cycles only revealed a small increase in surface roughness with DE, we suggest that surface roughness scattering may not be responsible for the significant $\mu_{\text{eff}}$ degradation of the junctionless device at $t_{\text{InGaAs}} = 16$ nm. We speculate that the lower $\mu_{\text{eff}}$ at $t_{\text{InGaAs}} = 16$ nm could be due to quantum confinement effects. Rigorous calculations would be required to verify this point.

6.5 Conclusion

We applied the junctionless MOSFET concept to an Al$_2$O$_3$/n-In$_{0.53}$Ga$_{0.47}$As/p-In$_{0.52}$Al$_{0.48}$As structure. The n-In$_{0.53}$Ga$_{0.47}$As/p-In$_{0.52}$Al$_{0.48}$As heterojunction offered excellent device isolation. Moreover, we showed that thinning the In$_{0.53}$Ga$_{0.47}$As channel using a DE process did not significantly degrade the Al$_2$O$_3$/n-In$_{0.53}$Ga$_{0.47}$As interface properties in terms of $D_{it}$ and surface roughness. Although a detailed analysis of the device operation and performance was presented, further investigations of the $\mu_{\text{eff}}$ degradation mechanisms involved in devices with sub-20-nm In$_{0.53}$Ga$_{0.47}$As channel thickness are required.
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Chapter 7

Conclusions and Suggestions for Further Research

7.1 Conclusions

The primary aim of this PhD was to develop In$_{0.53}$Ga$_{0.47}$As metal-oxide-semiconductor field-effect transistors (MOSFETs) building on the knowledge of the high-$k$ In$_{0.53}$Ga$_{0.47}$As metal-oxide-semiconductor (MOS) system developed at Tyndall since 2006. This involved both a conventional surface channel In$_{0.53}$Ga$_{0.47}$As MOSFETs with Si implanted source and drain (S/D) regions and the development of the junctionless MOSFET concept with an In$_{0.53}$Ga$_{0.47}$As channel. The main results are summarized below:

- The activation of Si implant in $p$-type In$_{0.53}$Ga$_{0.47}$As was first investigated for the formation of the source and drain terminals of an inversion-mode In$_{0.53}$Ga$_{0.47}$As MOSFET. While a number of groups had already demonstrated the use of Si implantation and activation in the process flow of inversion-mode III-V MOSFETs, we could not find a systematic study of the impact of activation anneal temperature and anneal time on the sheet resistance ($R_{\text{sheet}}$) of the S/D areas. We, therefore, prepared implanted In$_{0.53}$Ga$_{0.47}$As test structures based on the transfer length method (TLM) as part of a Doehlert design of experiment (DOE) to investigate a wide process window going from 625°C to 725°C for 15 s to 45 s. The analysis of the Doehlert DOE revealed an optimized process point at 715°C for 32 sec giving a low $R_{\text{sheet}}$ of 195.6 ± 3.4 Ω/□. The impact of the activation anneal on the gate stack was then investigated through the use of pre-metal annealed metal-oxide-semiconductor capacitors (MOSCAPs). The analysis of the capacitance-voltage (C-V) and conductance-voltage (G-V) measurements performed on the MOSCAPs indicated a degradation of the high-$k$ In$_{0.53}$Ga$_{0.47}$As interface with increasing anneal temperature. The density of interface traps ($D_{it}$) was found to increase by ~16% for every 25°C increase
within the studied temperature range of 675°C to 725°C. While the results obtained for the S/D implantation suggest that the $10^{19}$-$10^{20}$/cm$^3$ doping levels required to achieve ultralow resistance ohmic contacts for logic devices, these results may still be relevant to other applications with less stringent requirements.

- A reduced thermal budget of 600°C for 30 s was, therefore, selected for the S/D activation of the inversion-mode Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOSFETs. The obtained devices were used as test vehicles to investigate the impact of a 300°C for 30 min forming gas (H$_2$/N$_2$) anneal (FGA) process on the gate stack. The FGA process was found to be efficient at removing or passivating fixed positive charges in the Al$_2$O$_3$, resulting in a shift of the threshold voltage from -0.63 V to 0.43 V and in an increase in the ON-state-to-OFF-state current ratio ($I_{ON}/I_{OFF}$) of three orders of magnitude. Following FGA, the devices exhibited a subthreshold swing (SS) of 150 mV/decade, and the transconductance, drive current and peak effective mobility ($\mu_{eff}$) increased by 29%, 25% and 15%, respectively. The FGA significantly improved the source or drain-to-substrate junction isolation, with a reduction of two orders of magnitude in the reverse bias leakage exhibited by the Si-implanted In$_{0.53}$Ga$_{0.47}$As n$^+/p$ junctions, which is consistent with a passivation of mid-gap defects in the In$_{0.53}$Ga$_{0.47}$As by the FGA process. After FGA, the devices featured sufficient performance to be used as test structures to perform detailed analysis of the gate stack defects and channel electron mobility.

- A “full-gate capacitance” method involving the fitting of the measured full-gate capacitance ($C_g$) vs gate voltage ($V_g$) characteristic and corresponding Maserjian Y-function using a self-consistent Poisson-Schrödinger solver was then developed to obtain the energy distribution of traps [$D_{trap}(E)$] across the In$_{0.53}$Ga$_{0.47}$As bandgap and extending into the In$_{0.53}$Ga$_{0.47}$As conduction band. The obtained $D_{trap}(E)$ featured a peak of donor-like interface traps with a density of $1.5 \times 10^{13}$/cm$^2$.eV located at ~0.36 eV above the In$_{0.53}$Ga$_{0.47}$As valence band edge ($E_V$) and a high density of donor-like traps increasing towards $E_V$. The analysis also indicated acceptor-like traps located in the In$_{0.53}$Ga$_{0.47}$As conduction band, with a density of ~2.5 $\times$ $10^{13}$/cm$^2$.eV at 0.3 eV above the In$_{0.53}$Ga$_{0.47}$As conduction band edge ($E_C$). The proposed method provides a more complete information than the conventional methods (i.e.: High-Low, Terman and conductance). Moreover, the information obtained from this method can be combined with theoretical calculation models to gain further insight into the atomic origin of the traps observed in the high-k/In$_{0.53}$Ga$_{0.47}$As MOS system.

- A “multi-frequency” inversion-charge pumping (ICP) technique was developed to separate the contribution of traps aligned with the In$_{0.53}$Ga$_{0.47}$As conduction band from the inversion-charge density ($N_{inv}$). The analysis yielded (1) a very narrow spatial distribution of traps
7.2 Suggestions for Further Research

A range of fabrication process modules, characterization techniques and device architectures were developed and explored as part of this PhD. The list below gives one suggestion for further work in each of these areas:

- This work highlighted the difficulties associated with the formation of the $S/D$ terminals of inversion-mode In$_{0.53}$Ga$_{0.47}$As MOSFETS using implantation and activation. It was shown that the high thermal budget required to obtain maximum activation and low series...
resistance \((R_{\text{series}})\) was responsible for the severe degradation of the high-k \(\text{In}_{0.53}\text{Ga}_{0.47}\text{As}\) interface in terms of interface traps and surface roughness. It would be interesting to try to improve the protection of the \(\text{In}_{0.53}\text{Ga}_{0.47}\text{As}\) surface for the activation anneal. Varying capping materials and capping film thicknesses could have an impact on the \(\text{In}_{0.53}\text{Ga}_{0.47}\text{As}\) \text{RMS} surface roughness for a given thermal budget. It could also be interesting to try to activate the implant in a \text{metal-organic vapor phase epitaxy (MOVPE)} system under arsine ambient.

- An alternative method to extract the energy distribution of traps across the \(\text{In}_{0.53}\text{Ga}_{0.47}\text{As}\) bandgap and extending into the \(\text{In}_{0.53}\text{Ga}_{0.47}\text{As}\) conduction band was proposed. The method is based on the fitting of the measured \(C_{\text{g}}V_{\text{g}}\) characteristic (and Maserjian Y-function) measured at a frequency \((f)\) of 1 MHz and a \(T\) of -50°C. The method relied on the assumption that the measured characteristic was a good approximation of the true high-frequency (H-F) characteristic. It would be interesting to repeat this analysis using a better approximation of the H-F \(C_{\text{g}}V_{\text{g}}\) characteristic obtained at a \(T\) of 77 K or lower.

- The study of the impact of \(\text{InGaAs}\) on the performance of planar junctionless \(\text{In}_{0.53}\text{Ga}_{0.47}\text{As}\) MOSFETs was presented. The study indicated a dramatic increase in \(R_{\text{series}}\) as \(\text{InGaAs}\) reduced. It would be interesting to fabricate and characterize devices with \(\text{InGaAs} < 16\) nm with raised \(S/D\) terminals. This could be achieved by selectively etching the channel without etching the \(S/D\) area. This would only require a slight alteration of the fabrication process flow but no modification of the lithography mask. The fabrication process flow is given in Appendix C.
Appendix A

Doehlert Design of Experiment

A.1 Implementation

The Doehlert design of experiment (DOE) relies on the following second-order equation [1, 2]:

\[ y = \beta_0 + \beta_1 x_1 + \beta_2 x_2 + \beta_{11} x_1^2 + \beta_{22} x_2^2 + \beta_{12} x_1 x_2 + e \]  

(A.1)

where \( y \) is the experimental response, \( x_1 \) and \( x_2 \) are the two distinct variables and \( e \) is the residual error. The obtained seven-equation system with six unknown \( \beta \) coefficients can be expressed by the matrix representations (A.2) and (A.3):

\[
\begin{pmatrix}
y_1 \\
y_2 \\
y_3 \\
y_4 \\
y_5 \\
y_6 \\
y_7
\end{pmatrix} = \begin{pmatrix}
1 & x_{1,1} & x_{1,2} & x_{1,1} \times x_{1,2} & x_{1,1}^2 & x_{1,2}^2 \\
1 & x_{2,1} & x_{2,2} & x_{2,1} \times x_{2,2} & x_{2,1}^2 & x_{2,2}^2 \\
1 & x_{3,1} & x_{3,2} & x_{3,1} \times x_{3,2} & x_{3,1}^2 & x_{3,2}^2 \\
1 & x_{4,1} & x_{4,2} & x_{4,1} \times x_{4,2} & x_{4,1}^2 & x_{4,2}^2 \\
1 & x_{5,1} & x_{5,2} & x_{5,1} \times x_{5,2} & x_{5,1}^2 & x_{5,2}^2 \\
1 & x_{6,1} & x_{6,2} & x_{6,1} \times x_{6,2} & x_{6,1}^2 & x_{6,2}^2 \\
1 & x_{7,1} & x_{7,2} & x_{7,1} \times x_{7,2} & x_{7,1}^2 & x_{7,2}^2
\end{pmatrix} \begin{pmatrix}
\beta_0 \\
\beta_1 \\
\beta_2 \\
\beta_{11} \\
\beta_{22} \\
\beta_{12}
\end{pmatrix} + \begin{pmatrix}
e_1 \\
e_2 \\
e_3 \\
e_4 \\
e_5 \\
e_6 \\
e_7
\end{pmatrix}
\]

(A.2)

\[ Y = X.B + E \]  

(A.3)

where \( Y \), \( X \), \( B \) and \( E \) are the experimental-response vector, the Doehlert matrix [A.4], the coefficient vector and the residual-error vector, respectively.
\[ X = \begin{pmatrix} 
1 & 0 & 0 & 0 & 0 & 0 \\
1 & 1 & 0 & 0 & 1 & 0 \\
1 & 1/2 & \sqrt{3}/2 & \sqrt{3}/4 & 1/4 & 3/4 \\
1 & -1/2 & \sqrt{3}/2 & -\sqrt{3}/4 & 1/4 & 3/4 \\
1 & -1 & 0 & 0 & 1 & 0 \\
1 & 1/2 & -\sqrt{3}/2 & \sqrt{3}/4 & 1/4 & 3/4 \\
1 & -1/2 & -\sqrt{3}/2 & -\sqrt{3}/4 & 1/4 & 3/4 \\
\end{pmatrix} \quad (A.4) \]

The Doehlert matrix \((A.4)\) is based on a set of dimensionless normalized values \(x_{i,j}\) attributed to the two variables of the model. The normalization allows comparison of experimental factors \(F_1\) and \(F_1\) having different dimensions (e.g.: temperature and time). The transformation of normalized values \(x_{i,j}\) (where \(i\) is the run number and \(j\) the factor/variable number) into real factor levels \(l_{i,j}\) is obtained according to the following relationship:

\[ l_{i,j} = (x_{i,j} \times \delta l_j) + l_{1,j} \quad (A.5) \]

where \(l_{1,j}\) is a level of factor \(F_j\) at the center of the experimental domain and \(\delta l_j\) is the step variation between consecutive levels of \(F_j\). The regression coefficients are obtained using the method of least squares, which enables to fit the experimental response with the lowest residual error possible. As a result, equation \(A.3\) can be simplified into:

\[ \hat{Y} = X.\hat{B} \quad (A.6) \]

where \(\hat{Y}\) is the estimated-response vector and \(\hat{B}\) is the regression-coefficient vector. Equation \(A.6\) is rearranged and applied to the experimental-response vector \(Y\) in order to obtain vector \(\hat{B}\):

\[ \hat{B} = (X^T.X)^{-1}.X^T.Y \quad (A.7) \]

The center point of the Doehlert DOE (run 1) is repeated \(i\) times to allow estimation of the response standard error \(\hat{\sigma}_e^2\).

\[ \hat{\sigma}_e^2 = \frac{1}{i-1} \sum_i (y_i - y_{1,i})^2 \quad (A.8) \]

The estimates of the standard error of each regression coefficient are:

\[ \hat{\sigma}(\hat{B}_j) = \sqrt{C_{j,j} \times \hat{\sigma}_e^2} \quad (A.9) \]

where \(C_{j,j}\) are diagonal elements of matrix \((X^T.X)^{-1}\).
A.2 Statistical Analysis

The statistical significance of each coefficient of the model is checked using a Student’s t-test [3]. A coefficient is considered to be significant when its $P$-value is below $\alpha$ (here $\alpha = 0.05$). The test of the overall significance of the model is achieved by analysis of variance (ANOVA) (F-test) [2]. The model is considered to be significant when the $P$-value of the regression is below $\alpha$ and the $P$-value of the lack-of-fit above $\alpha$. The determinant coefficient $R^2$ and the correlation coefficient $R$ are used to assess the quality of the fit. The closer the $R^2$ and the $R$ to 1, the better the fit.

A.3 Process Optimization

The process optimization is performed using the Lagrange criterion, which is based on the calculation of the Hessian determinant $H$ of $\hat{Y}$ [4]:

$$H = \begin{vmatrix} \frac{\partial^2 \hat{Y}}{\partial X_1^2} & \frac{\partial^2 \hat{Y}}{\partial X_1 \partial X_2} \\ \frac{\partial^2 \hat{Y}}{\partial X_2 \partial X_1} & \frac{\partial^2 \hat{Y}}{\partial X_2^2} \end{vmatrix} = \left( \frac{\partial^2 \hat{Y}}{\partial X_1^2} \right) \left( \frac{\partial^2 \hat{Y}}{\partial X_2^2} \right) - \left( \frac{\partial^2 \hat{Y}}{\partial X_1 \partial X_2} \right) \left( \frac{\partial^2 \hat{Y}}{\partial X_2 \partial X_1} \right)$$ (A.10)

The following four possible situations enable to determine the nature of the critical point of the response function:

- $H > 0$ and $\frac{\partial^2 \hat{Y}}{\partial X_1^2} < 0$: the critical point is a maximum
- $H > 0$ and $\frac{\partial^2 \hat{Y}}{\partial X_1^2} > 0$: the critical point is a minimum
- $H < 0$: the critical point is a saddle point
- $H = 0$: no information

The coordinate of the critical point are obtained by solving the following system of two equations:

$$\frac{\partial \hat{Y}}{\partial X_1} = 0 \text{ and } \frac{\partial \hat{Y}}{\partial X_2} = 0$$ (A.11)
Bibliography


Appendix B

Masks

• Linear TLM structures
  Mask name: FORME1-TLM
  - Layer 1: etch of alignment marks
  - Layer 2: implantation
  - Layer 3: mesa etch
  - Layer 4: metal contacts lift-off

• Inversion-mode MOSFETs and circular TLM structures
  Mask name: FORME3 Mask1
  - Layer 1: etch of alignment marks / isolation
  - Layer 2: S/D implantation
  - Layer 3: oxide etch for opening for S/D and body contacts
  - Layer 4: oxide lift-off for gate pad

  Mask name: FORME3 Mask2
  - Layer 5: S/D contacts lift-off
  - Layer 6: gate pad + body contact lift-off
  - Layer 7: gate metal lift-off
  - Layer 8: metal lift-off for circular TLM structures
Appendix C

Process Flow for Junctionless MOSFETs with Raised Source and Drain

Use mask: JLESS-INGAAS1(PO No 404-96284)

1. Litho level 0: ALIGN ETCH
   - Standard S1813 process for wet etch
   - Wet etch alignment marks InGaAs/InP (target depth ~200-300 nm) with H$_2$SO$_4$:H$_2$O$_2$:DI (1:1:8) for ~20 s
   - PR removal with hot 1165 only (no plasmod)

2. Litho level1: GATE LIFTOFF (Note: This is for an etch)
   - Standard S1813 process for wet etch
   - Digital wet etch of the InGaAs channel (16 - 20 nm deep) with cycles of dips in HCl:DI 1:10 (10 s) and dilute H$_2$O$_2$:DI 1:10 (10 s). Target: for 16 nm etch depth - 20 cycles, for 20 nm etch depth - 25 cycles. Ellipsometry model: “In53Ga47As on InP Vladimir”.
   - PR removal with hot 1165 only (no plasmod)

3. Optimized surface passivation in 10% (NH$_4$)$_2$S for 30 min immediately followed by 8 nm ALD Al$_2$O$_3$

4. Litho level1: GATE LIFTOFF
• Standard LOR3A/S1805 process for liftoff
• 200 nm Pd evap, pre-evap heat to 100°C for 30 min. Evap at 80°C, evap rate: 0.5 Å/s for first 50 nm then 1 Å/s.

5. Litho level 2: OXIDE ETCH

• Standard S1813 process for wet etch
• BOE/DI (1/10) etch for 25 s to remove Al₂O₃
• PR removal with hot 1165 only (no plasmod)


• Standard LOR3A/S1805 process for liftoff
• Pre-load heat 90°C.
• Pre-deposition dip in ammonia/DI (1:10) for 20 s before loading
• Deposit N-metal Au/Ge/Au/Ni/Au (14/14/14/11/200 nm)

**Standard litho processes:**

• S1813 for etch: HMDS 4000 rpm for 60 s, S1813 4000 rpm for 60 s, bake 115°C for 2 min, expose 7.5 s, develop MF319 for 45 s, oven bake 90°C for 30 min

• LOR3A/S1805 for liftoff: HMDS 3000 rpm for 50 s, LOR3A 3000 rpm for 50 s, bake 150°C for 3 min, HMDS 3000 rpm for 50 s, S1805 3000 rpm for 50 s, bake 115°C for 2 min, expose 4.5 s, develop MF319 for 1 min 15 s, oven bake 90°C for 30 min
Appendix D

List of Achievements

• Filed Patent Application


• Accepted Publications


5. P. K. Hurley, É. O’Connor, V. Djara, S. Monaghan, I. M. Povey, R. D. Long, B. Sheehan, J. Lin, P. C. McIntyre, B. Brennan, R. M. Wallace, M. E. Pemble, and


• Oral Presentations at International Conferences


Appendix D. List of Achievements

Pd/Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOSFETs,” IEEE Semiconductor Interface Specialists Conference (SISC), Arlington - United States, 2011.


- Poster Presentations at International Conferences

1. V. Djara, K. Cherkaoui, T. Lopez, É. O’Connor, I. M. Povey, K. K. Thomas, and P. K. Hurley, “Junctionless InGaAs MOSFETs with InAlAs Barrier Isolation and Channel Thinning by Digital Wet Etching,” IEEE Device Research Conference (DRC), Notre Dame - United States, 2013.


- Award

1. BOC Gases Ireland Postgraduate Bursary Award 2012 (runner up) for research accomplishments in the field of high-\(k\)/III-V metal-oxide-semiconductor field-effect transistors (MOSFETs)

- Publications in Preparation


2. V. Djara, K. Cherkaoui, T. Lopez, M. Burke, É. O’Connor, I. M. Povey, K. K. Thomas, and P. K. Hurley, “Impact of Channel Thickness in Junctionless Al$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As MOSFETs MOSFETs,” IEEE Trans. Electron Devices.
Accepted Publications (Not Related to the PhD)


Appendix D. List of Achievements

