

Title	Atomic layer deposition of interface control layers for the fabrication of III/V MOS devices
Authors	Mullins, John A.
Publication date	2014
Original Citation	Mullins, J. A. 2014. Atomic layer deposition of interface control layers for the fabrication of III/V MOS devices. PhD Thesis, University College Cork.
Type of publication	Doctoral thesis
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Download date	2024-04-25 02:14:16
Item downloaded from	https://hdl.handle.net/10468/2009

Ollscoil na hÉireann, Corcaigh

NATIONAL UNIVERSITY OF IRELAND, CORK



**Atomic layer deposition of interface control layers for the
fabrication of III/V MOS devices**

A Thesis Presented to
The National University of Ireland, Cork
For the Degree of Doctor of Philosophy
by

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March 2014

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DECLARATION

All work outlined in this thesis is the original work of the author and has not been submitted for any other degree or qualification.

Signature of the author:

Date _____

ACKNOWLEDGEMENTS

Firstly, I would like to extend my sincerest gratitude to my supervisors, Professor Martyn Pemble for giving me the opportunity to conduct research at the Tyndall National Institute and special thanks to Dr. Ian Povey for his constant advice and instruction during all aspects of this PhD.

Thanks to all the members of the Advanced Materials and Surfaces Group, both past and present including Dr Dirk Hagen Dr. Shane O'Brien, Dr. Richard Winfield, Dr. Aileen O'Mahony, Dr. Mark Nolan, Dr. Jeff Hamilton, John Kinsella, Conor Moynihan, Igor Kazadojev, Dr. Brendan Sheehan, Adrian Walsh, Barry Hutchinson and Mary-Claire O'Regan who have all made my time spent at Tyndall very enjoyable.

I would like to thank Dr. Paul Hurley for his advice and other members of his group for their assistance, Dr. Karim Cherkaoui, Dr. Scott Monaghan, and Dr. Éamon O'Connor. Thanks to Dr. Patrick Carolyn for the microscopy work. Thanks to Dr. Dan O'Connell for device fabrication and Dr. Vladimir Djara for ellipsometry training and thanks to those who collaborated on this work Agnes Kurek, Dr. Simon B. Newcomb and James Connolly.

Finally, thanks to my Ma and Da for all their support, to Eileen for her patience and help maintaining my sanity and to my friends in both Clonmel and Cork for providing much needed company at the weekend.

ABSTRACT

The continued advancement of metal oxide semiconductor field effect transistor (MOSFET) technology has shifted the focus from Si/SiO₂ transistors towards high- κ /III-V transistors for high performance, faster devices. This has been necessary due to the limitations associated with the scaling of the SiO₂ thickness below ~ 1 nm and the associated increased leakage current due to direct electron tunnelling through the gate oxide. The use of these materials exhibiting lower effective charge carrier mass in conjunction with the use of a high- κ gate oxide allows for the continuation of device scaling and increases in the associated MOSFET device performance. The high- κ /III-V interface is a critical challenge to the integration of high- κ dielectrics on III-V channels. The interfacial chemistry of the high- κ /III-V system is more complex than Si, due to the nature of the multitude of potential native oxide chemistries at the surface with the resultant interfacial layer showing poor electrical insulating properties when high- κ dielectrics are deposited directly on these oxides. It is necessary to ensure that a good quality interface is formed in order to reduce leakage and interface state defect density to maximise channel mobility and reduce variability and power dissipation.

In this work, the ALD growth of aluminium oxide (Al₂O₃) and hafnium oxide (HfO₂) after various surface pre-treatments was carried out, with the aim of improving the high- κ /III-V interface by reducing the D_{it} – the density of interface defects caused by imperfections such as dangling bonds, dimers and other unsatisfied bonds at the interfaces of materials.

A brief investigation was performed into the structural and electrical properties of Al_2O_3 films deposited on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ at 200 and 300°C via a novel amidinate precursor. Samples were determined to experience a severe nucleation delay when deposited directly on native oxides, leading to diminished functionality as a gate insulator due to largely reduced growth per cycle.

Aluminium oxide MOS capacitors were prepared by ALD and the electrical characteristics of GaAs, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and InP capacitors which had been exposed to pre-pulse treatments from triethyl gallium and trimethyl indium were examined, to determine if self-cleaning reactions similar to those of trimethyl aluminium occur for other alkyl precursors. An improved C-V characteristic was observed for GaAs devices indicating an improved interface possibly indicating an improvement of the surface upon pre-pulsing with TEG, conversely degraded electrical characteristics observed for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and InP MOS devices after pre-treatment with triethyl gallium and trimethyl indium respectively.

The electrical characteristics of $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors after in-situ H_2/Ar plasma treatment or in-situ ammonium sulphide passivation were investigated and estimates of interface D_{it} calculated. The use of plasma reduced the amount of interface defects as evidenced in the improved C-V characteristics. Samples treated with ammonium sulphide in the ALD chamber were found to display no significant improvement of the high- κ /III-V interface.

HfO_2 MOS capacitors were fabricated using two different precursors comparing the industry standard hafnium chloride process with deposition from amide precursors incorporating a ~1nm interface control layer of aluminium oxide and the structural and electrical properties

investigated. Capacitors furnished from the chloride process exhibited lower hysteresis and improved C-V characteristics as compared to that of hafnium dioxide grown from an amide precursor, an indication that no etching of the film takes place using the chloride precursor in conjunction with a 1nm interlayer. Optimisation of the amide process was carried out and scaled samples electrically characterised in order to determine if reduced bilayer structures display improved electrical characteristics. Samples were determined to exhibit good electrical characteristics with a low midgap D_{it} indicative of an unpinned Fermi level.

THESIS OVERVIEW

Chapter 1 – In Chapter 1, an overview of the necessity of high- κ oxides and the challenges and progression associated with their integration on III-V channel materials for application in complementary metal oxide semiconductor technology, is provided.

Chapter 2 – This chapter addresses the topic of atomic layer deposition (ALD) – providing an overview of the development of ALD, the key characteristics of ALD as a deposition technique. The characteristics of metal oxide semiconductor devices are discussed in detail together with the impact of defects in the system on the electrical characteristics and the passivation of these defects. Additionally, a theoretical explanation of the MOS fabrication and analysis techniques used in this work is presented.

Chapter 3 – In this chapter a growth study is described using a new acetamidinate precursor on Si substrates. The structural and electrical characteristics of capacitors fabricated using this precursor on III-V materials are described.

Chapter 4 – In chapter 4 the electrical characteristics of samples pre-treated with metal precursors are discussed. The treatment of GaAs with triethyl gallium (TEG), $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ with TEG and InP with trimethyl indium (TMI) on both *n*- and *p*- type substrates is explored to determine if self-cleaning reactions analogous to that of the well documented TMA native oxide clean-up take place.

Chapter 5 – In Chapter 5, the electrical characteristics of metal oxide semiconductor capacitors which have received surface pre-treatments are investigated and compared to the previously investigated ammonium sulphide passivation. Initial investigations use both *n* and *p* In_{0.53}Ga_{0.47}As with a H₂/Ar in-situ plasma treatment to remove native oxides and electrical characteristics are used to investigate the efficacy of the plasma treatment. A second comparison is made between the optimised ex-situ ammonium sulphide etch and exposure to ammonium sulphide vapour in an ALD chamber to determine if the removal of native oxides is possible using vapour phase ammonium sulphide.

Chapter 6 – The differences in the electrical characteristics of HfO₂ films deposited from two precursors is investigated. A thin (nominal ~1 nm) interface control layer (ICL) of a wide bandgap material (Al₂O₃), was deposited on a sulfur passivated In_{0.53}Ga_{0.47}As surface prior to deposition of a ~5 nm HfO₂ layer, by ALD from either tetrakis dimethylaminohafnium (TDMAH) or HfCl₄. The aim of the ICL is to modify and improve the bilayer oxide structures, by increasing the barrier height to tunnelling and potentially promoting self-cleaning of the III-V native oxides whilst allowing for continued device scaling. The resulting devices are characterised structurally and electrically.

Chapter 7 – Chapter 7 presents conclusions arising from the research work outlined in this thesis and suggestions for future experimental work.

Chapter 1: Introduction to CMOS technology.

1.1 Motivation – Moore’s Law

In recent decades an enormous boom in the use of microelectronic devices has occurred with advanced electronics such as CPU’s with very high processing power being needed for everyday activities such as video streaming. Transistors are central to these microelectronic devices with the Si/SiO₂ based system the semiconductor of choice, due to the ease of production of high quality Si substrates and the primary advantage of the system being the high quality interface between Si and SiO₂ gate dielectric, which may be obtained from thermal oxidation of Si. A postulation made in 1965 by Gordon Moore states that the density of transistors on an integrated circuit would double every two years¹. While this postulation is now referred to as Moore’s law it is not strictly a law but it has guided the progress of the semiconductor industry serving as a challenge for the industry in terms of being able to remain in-line with this prediction, as illustrated in figure 1.1

Currently, scaling is necessary to decrease the cost per fabricated device allowing electronic devices to remain cost effective and also to improve device drive current to allow for high speed operation of transistors² and reduce power consumption. To improve device drive current, The simple concept of scaling for MOS transistors is to reduce all of the physical dimensions by the same amount, while increasing the body doping and reducing the applied voltage to cause the depletion regions within the devices to scale as much as the other dimensions, this necessarily allows for the increase in transistor density on the chip.

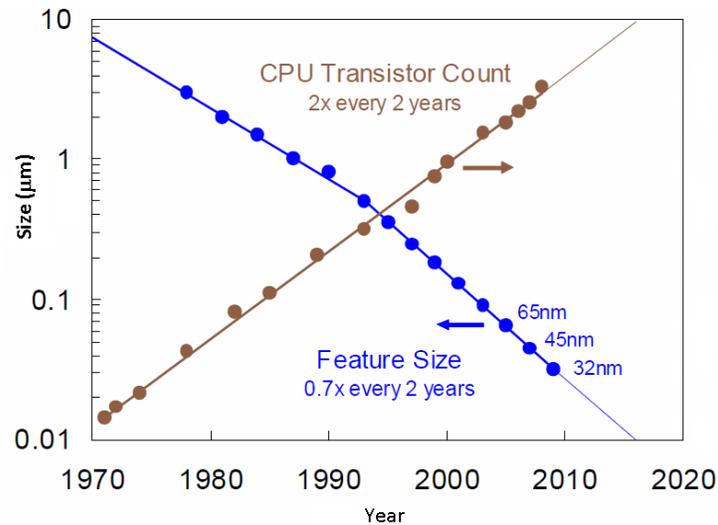


Fig. 1.1 The scaling trend of Moore's Law showing the increasing density of transistors on an integrated circuit against time and the reduction in channel length against time³.

With aggressive scaling taking place between successive generations of Si/SiO₂ technology – essentially the same since the fabrication of the first microprocessor in 1971 – the technology has approached its limit with the reduction in thickness of the gate dielectric to a few atomic layers⁴. Below a physical thickness of 15Å the leakage current of the Si/SiO₂ system drastically increases above 1A/cm² at an operating voltage of 1V due to the tunnelling through the gate oxide layer. In order to maintain scaling for future generations of transistors a new technology was introduced to commercial manufacturing in 2007⁵ with the advent of the first HfO₂/Si based gate dielectric yielding greatly improved device performance, the scaling of previous technology nodes until 2010 is illustrated below in figure 1.2.

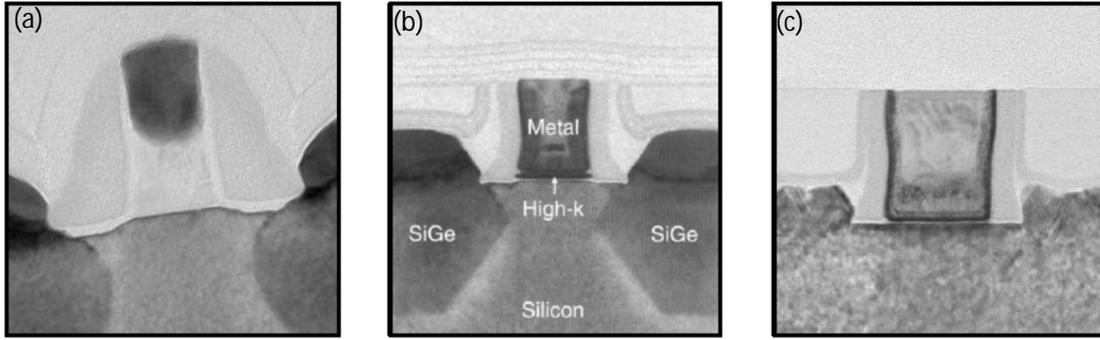


Fig. 1.2 TEM micrographs of Intel's a) 65nm node, b) 45nm node with high- κ dielectric and c) 32nm node planar node⁶.

1.1.2 High- κ on Si

Higher dielectric constant (κ) materials were sought to maintain a high gate capacitance while retaining an oxide thickness large enough to inhibit gate leakage via quantum mechanical tunnelling through the gate oxide. The gate oxide capacitance is described by:

$$C_{ox} = \frac{A\epsilon_0\kappa}{T_{ox}} \quad \text{Equation 1.1}^7$$

Where C_{ox} is the oxide capacitance (F/m), κ is the relative permittivity, ϵ_0 is the permittivity of free space (8.854×10^{-12} F/m²), T_{ox} is the oxide thickness (m) and A is the capacitor area (m²).

The thickness of these new, higher permittivity oxides is referenced back to that of the original SiO₂ oxide by the Equivalent Oxide Thickness (EOT) as given by:

$$T_{ox} = EOT = \left(\frac{3.9}{\kappa_{high-k}} \right) t_{high-k} \quad \text{Equation 1.2}^7$$

This EOT relates the thickness of SiO₂ that would be needed to reach the same capacitance as the high-κ oxide layer, where t_{high-k} is the thickness of the high-κ dielectric layer and κ_{high-k} is the dielectric constant of the high-κ layer. If more than one high-κ oxide is used for example in a bilayer structure then the equation is simply modified to account for the thickness and dielectric constant of both films (equation 1.3).

$$EOT = \left(\frac{3.9}{\kappa_{1high-k}} \right) t_{1high-k} + \left(\frac{3.9}{\kappa_{2high-k}} \right) t_{2high-k} \quad \text{Equation 1.3}$$

As well as having a larger dielectric constant a successful candidate material to replace the SiO₂ gate dielectric on Si must also have some other useful characteristics in addition to a high-κ value (25-30) to allow for iterative generations of reasonable scaling such as:

i) Thermodynamic stability with respect to Si, to prevent the formation of a metal silicate interlayer when in contact with the semiconductor thus lowering the κ value. Some materials may be slightly reactive with Si such as was found with ZrO₂, forming the silicide, ZrSi₂⁸ the formation of such an interlayer results in diminished functionality of the gate oxide. HfO₂ has exhibited both a high κ value as well as minimal chemical reactivity towards Si.

ii) Have large band offsets to maintain functionality as an insulator. This requires that the potential barrier at the valence and conduction bands must inhibit conduction by the Schottky emission of electrons or holes from the semiconductor into the oxide bands during device operation^{9,10}. The use of some high-κ oxides such as SrTiO₃ previously used in DRAM¹¹ is limited for MOS devices as there is a correlation between the κ value of the oxide and the band gap of the oxide. Oxides with high-κ values tend to have lower band gaps as is illustrated in figure 1.3 below.

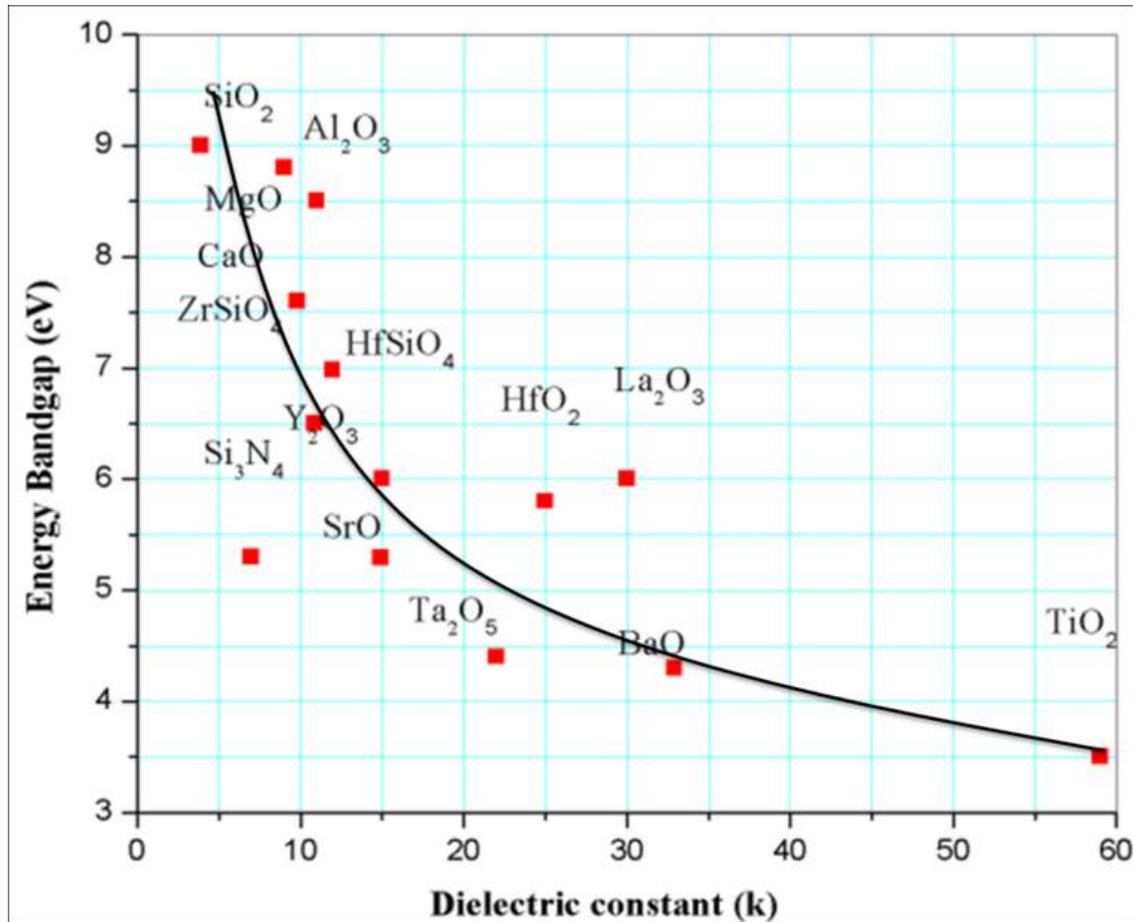


Fig. 1.3 Static dielectric constant versus band gap for candidate gate oxides¹²

iii) Possess a low density of interfacial defect states when deposited on the semiconductor. Many early experiments with high- κ oxides yielded an interface state density of ca. $10^{11-13} \text{cm}^{-2} \text{eV}^{-1}$ ^{7,13}. Such a poor interface quality may result in reduced performance and reliability of the transistor. Typical Si/SiO₂ devices have an interface state density of not more than $10^{10} \text{cm}^{-2} \text{eV}^{-1}$ to ensure proper device operation¹⁴.

iv) Low electrical leakage current densities ca. 10^{-8}Acm^{-2} to identify the oxide as having excellent insulator properties¹⁵. This ensures efficient function of electrical devices and less consumption of power when the device is turned off.

High- κ oxides were first introduced at full scale production of field effect transistors for the 45-nm node by Intel with the use of HfO_2 as the gate dielectric¹⁶, seen as an innovation for semiconductor design. Current state of the art has been scaled to the 22nm node and incorporates a tri gate configuration with the gate oxide covering three sides of the transistor enabling greater control of the channel and reduced contributions from the substrate as illustrated below in figure 1.4.

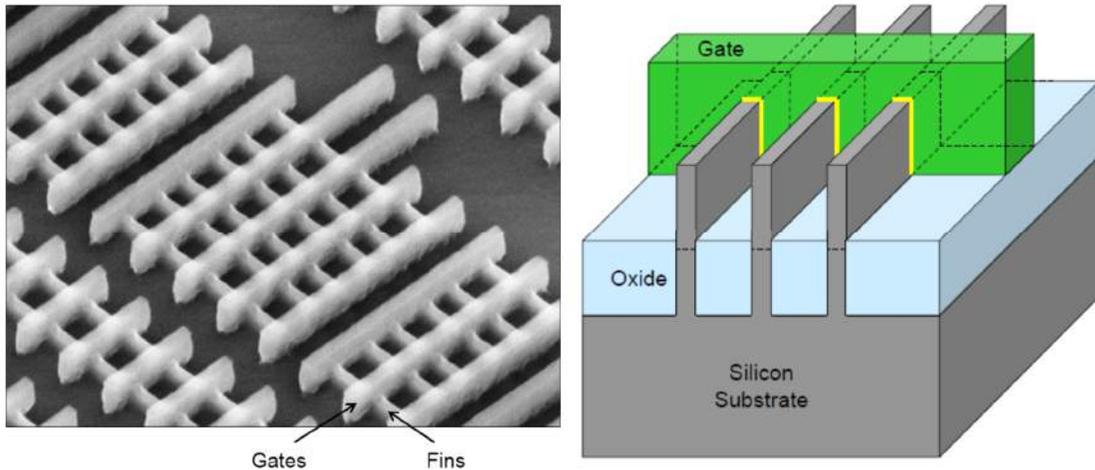


Fig 1.4. TEM micrograph of a current state of the art Intel 22nm finFET, presented alongside an illustration of the structure¹⁶.

Though HfO_2 has been chosen as the gate dielectric of choice initial investigations considered several high- κ candidates with ZrO_2 , Al_2O_3 , Y_2O_3 , La_2O_3 and Ta_2O_5 ^{7,17-21} as possible candidates for replacing the SiO_2 gate oxide, however disadvantages were found with all of the candidates. Of the most researched candidates Al_2O_3 has too low a κ value to offer generations of scaling and tends to diffuse into Si substrates at high processing temperature²². ZrO_2 was found to be unstable with respect to Si^{23} while Hf analogues of Zr compounds are more stable at the same temperatures²⁴. La_2O_3 films tend to be hygroscopic and have large negative flat band shifts due to the incorporation of positive fixed charge²⁵ affecting operating

voltage of prospective devices; also this moisture sensitive nature renders La_2O_3 unsuitable for very large scale integration (VLSI) processes as these involve frequent exposure to atmosphere. HfO_2 exhibits the greatest thermodynamic stability with Si under processing conditions, such as the 1000°C anneal required to activate source and drain dopants, this is important as diffusion of Hf and Zr from the gate oxide into the semiconductor creates trap levels in the semiconductor band gap²⁶

HfO_2 was chosen as a high- κ candidate due to its good mix of relatively large band gap, $\sim 5.7\text{eV}$ and dielectric constant of ~ 25 which compare favourably to the SiO_2 values of 8.9eV and 3.9 respectively²⁷.

1.1.3 High- κ metal gate implementation

With the advent of a new gate oxide a change in the gate material was also necessary. Previous transistors could use heavily doped polysilicon ($\sim 10^{20}$ atoms/ cm^3) as a gate material to modulate the Fermi level in the MOS device, however there are several problems associated with the use of a poly-Si gate oxide. Device geometries of such small proportions predicted for scaling trends would cause the poly-silicon gate to have a detrimental effect on device characteristics where the use of thin oxides no longer allows the depletion width of a poly-doped gate to be ignored. This adds an additional capacitance to the system and effectively increases t_{ox} leading to a reduced device performance by reducing the inversion charge in the device channel.

Furthermore the instability of high- κ oxides with respect to Si at high processing temperatures makes a poly-Si gate undesirable due to the formation of metal silicates. This thermal instability leads to the creation of defects at the high- κ /poly Si gate which cause Fermi level pinning in transistors²⁸. The transistor channel mobility – how quickly charge

carriers can travel through the semiconductor inversion channel – may also be impacted at by the high- κ /poly-Si gate interface with phonon scattering occurring due to various modes of lattice vibration²⁹⁻³¹. This occurs as the high- κ dielectric has polarizable metal-oxygen bonds, the oscillating dipoles which interact with the channel carriers when the gate plasma and the high- κ oscillations are in resonance. This resonance condition leads to a significant decrease in carrier mobility and an increase in effective mass. Coulomb scattering may occur due to the collision of minority carriers with the charges impurities including fixed oxide charge³². A model of coulomb scattering developed for SiC transistors shows that the scattering rate is directly proportional to the density of occupied interface traps and the fixed charge density at the interface³².

These disadvantages can be alleviated by the incorporation of a metal gate; the large density of electrons in a metal gate can effectively screen the phonon vibrations in the gate oxide. The use of metal gates calls for the use of two different metals, one for *n*-type and one for *p*-type MOS. Each metal used has a different workfunction; the intent of using metals with different work functions is to modulate the Fermi level of the system towards the appropriate band edge close to inversion for the semiconductor and device type, the advantage of using two different metals for MOS devices is clarified below in figure 1.5 for silicon devices.

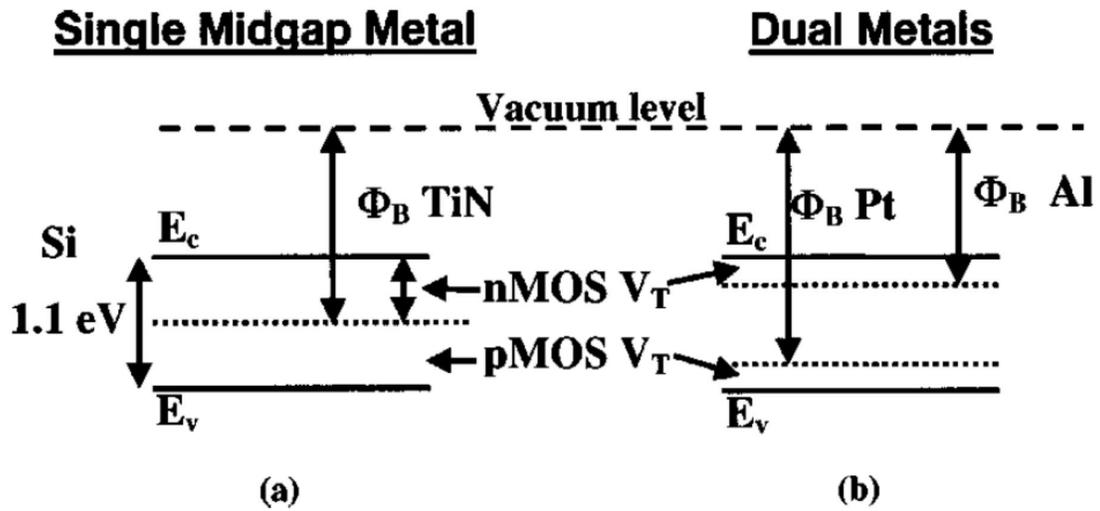


Fig. 1.5: An illustration of band edge modulation by dual metal gates for use in n - and p -MOS³³

1.1.4 III-V semiconductor properties

III-V semiconductor materials are composed of elements from groups III (Al, Ga, In) and V (P, As, Sb) and have the possibility to be alloyed to form binary, tertiary and quaternary semiconductor compounds with a variety of bandgaps and lattice constants. The structure of many III-V semiconductors is that of the zinc-blende structure with each group III atom bound to 4 group V atoms in a tetrahedral arrangement and vice versa as represented in figure 1.6.

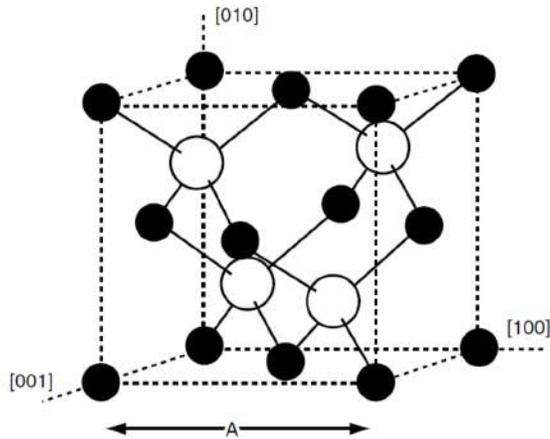


Fig 1.6: The zinc-blende structure of III-V semiconductors³⁴

Many III-V semiconductors generally possess direct bandgaps, meaning that the conduction band minimum and valence band maximum occur at the same point in crystal momentum. This allows for either the electronic or photonic creation of electron-hole pairs. In contrast an indirect semiconductor such as Si which has minima and maxima at different crystal momentum requires the absorption of a phonon to maintain crystal momentum and create electron-hole pairs as shown in figure 1.7.

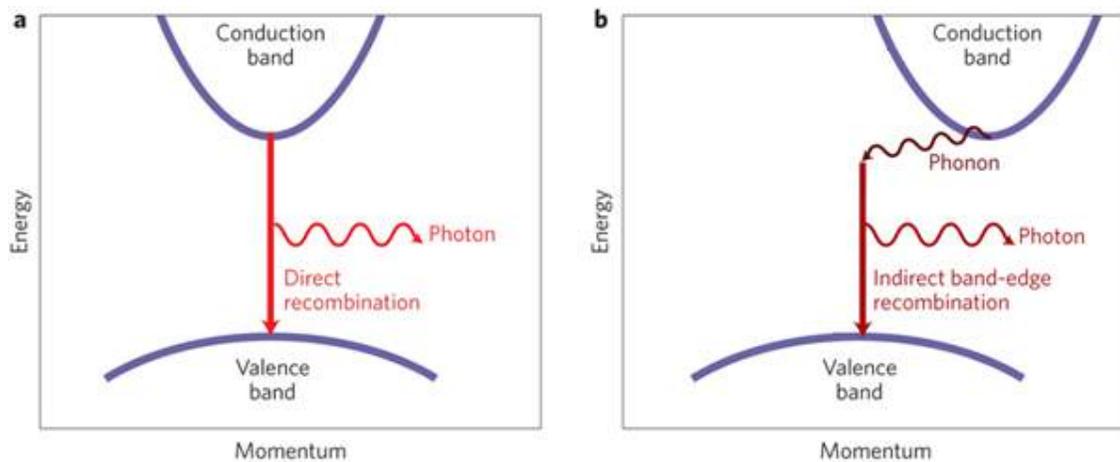


Fig 1.7: a) An illustration of a direct bandgap semiconductor such as GaAs. b) An indirect-bandgap semiconductor, such as silicon³⁵.

Chief among the desirable properties of III-V compounds is improved carrier mobility (table 1.1). Mobility enhancement in III-V semiconductors comes from their lower effective electron mass than that of silicon. The lower effective mass translates into a higher average velocity of carriers in the channel thereby providing higher drive current in MOSFET devices. The higher drive current results in a greater switching speed and also allow the scaling of power supply voltage to reduce the power consumption of a device. The trade-off for this mobility enhancement is that III-V's tend to have smaller bandgaps³⁶ and larger dielectric constants³⁶ than the silicon system, these smaller bandgaps may pose a problem for the integration of III-V semiconductors into devices as the small bandgaps allow for direct tunnelling of carriers to happen. Most research for *n*- channel MOS currently investigates the In_{0.53}Ga_{0.47}As since its properties are somewhere in the middle of III-V compounds having a combination of good carrier mobility with a reasonable bandgap which may be tuned by varying the indium content³⁷ and may be easily grown on InP substrates³⁸ which are readily available at the time of writing as 3" substrates, with Ge channels seen as the most promising candidate for high performance *p* MOS to realise a fully functioning CMOS devices.

	Si	GaAs	In _{0.53} Ga _{0.47} As	InP	Ge
Electron mobility (cm ² V ⁻¹ s ⁻¹)	400	9200	14000	5400	3900
Hole mobility (cm ² V ⁻¹ s ⁻¹)	160	400	300	200	1900

Table 1.1: The electron and hole mobility of relevant III-V semiconductors³⁹

1.1.5 Fermi Level Pinning

The Fermi energy, E_f , is the energy of the highest level completely occupied by electrons in a material at 0K, and is also known generally as the Fermi level. In intrinsic semiconductor materials, the Fermi level is usually very close to the middle of the band gap when the number of electrons in the conduction band is the same as the number of holes in the valence band. When two materials, e.g., a semiconductor and a metal which in general have two different work-functions, make a contact, charge is redistributed between the two, to reach thermal equilibrium and equalize the Fermi level in the system. An ideal system is illustrated in figure 1.8 below. This equalisation of the Fermi level in the real case is accompanied by the flow of charge i.e. electrons and an accompanying band bending in the semiconductor. Fermi level pinning takes place when a large number of surface states are present at this interface, which have energy states in the band gap. This results in the modification of the band structure to incorporate localized energy levels associated with these defective states, which may lie anywhere in the band gap, from the valence band to the conduction band.

The surface and bulk of III-V semiconductors have many possible defects associated with them such as dangling bonds, vacancies, dimers and atom substitutions. This leads to the creation of many acceptor (which accept an electron) and donor (which donate an electron) states in the system, unlike the Si/SiO₂ system which has the ability to relax bonding configuration to reconstruct and remove defects^{40,41} the difficulty bond rearrangement of III-V materials makes it difficult to compensate for any intrinsic defects.

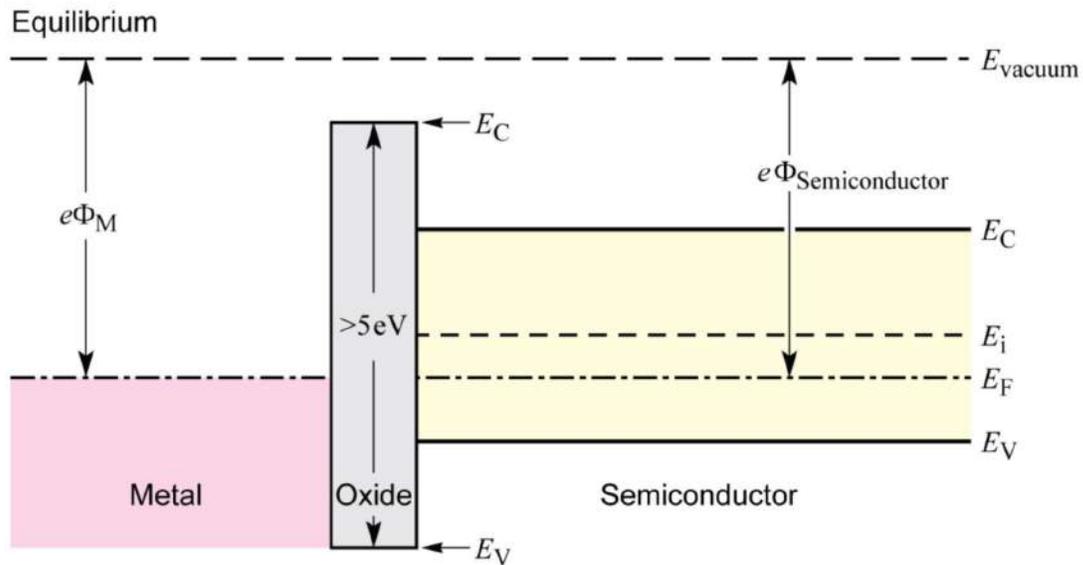


Fig. 1.8: An ideal MOS capacitor where the Fermi level is equalised throughout the structure⁴².

The density of surface states can be very large (e.g., 1 state per surface atom). The crystallographic density of surface atoms is in the range of 10^{14}cm^{-2} . A high density of these surface states and their associated energy levels provides the charge required to equalise the Fermi level in the total system (since they will be neutral or charged depending on the position of the Fermi level in the system initially) and restricts the band bending that would otherwise take place hence leading to a very small displacement of the Fermi level known as “Fermi level pinning”. The free modulation of the Fermi level and the accompanying band bending is essential for fully functioning transistors as to turn on transistors the Fermi level must be moved into the valence or conduction band. It should be noted that pinning does not happen on every semiconductor as the surface states may not always have energies inside the band gap, e.g. the non-polar (110) surface of III-V materials.

1.1.6 III-V MOSFET developments

III-V transistors are potential alternatives to the high- κ /Si MOSFET system currently in use, as III-V devices offer enhanced electron transport. In contrast to the rapid development of Si/SiO₂ based MOSFETs based on simply scaling transistor design, considerably less progress has been made in the performance of the III-V transistor, since the inception of the original III-V devices based on SiO₂/GaAs fabricated by Becke and White in 1967⁴³. Early work focused on the use of the GaAs native oxides as the dielectric layer analogous to the Si/SiO₂ system. However, the use of these leaky, unstable native oxides as the gate dielectric which exhibit low electric breakdown strengths were not a feasible option. Although the progress of realizing a suitable gate-oxide on GaAs was hindered for a long time, the high electron mobility transistor (HEMT), first developed by Mimura⁴⁴ became the first commercialised III-V transistor technology. Passlack and Hong at Bell Labs reported MOS structures with a low interface state density in 1995. The devices were fabricated using molecular-beam-epitaxy (MBE) of Ga₂O₃/ (Gd₂O₃) dielectric film on GaAs⁴⁵.

The first device to show improved performance over silicon analogues was a *p*-channel GaAs enhancement-mode MOSFET i.e. a normally off device, was reported in 2002⁴⁶ However, a viable demonstration of the *n*-channel complement remained elusive until recently; 2003 for the depletion mode MOSFET⁴⁷ i.e. a normally on device, and 2005 for the enhancement mode MOSFET⁴⁸ i.e. normally off device. Later, following on from the work of Passlack and Hong, the same Ga₂O₃/ (Gd₂O₃) dielectric was used to realize enhancement-mode MOSFETs with an In_{0.53}Ga_{0.47}As channel⁴⁹. A dual layer stack of Ga-rich Ga₂O₃/ (Gd₂O₃) and Al₂O₃ on InGaAs has also been shown to have a free-moving Fermi level which could be moved between the conduction and valence band edges⁵⁰. With the first tentative steps towards realising a common gate stack for In_{0.53}Ga_{0.47}As and Ge channels provided by Lin *et al.* in

2010⁵¹. High performance inversion mode III-V MOSFETs with InGaAs channel have also been demonstrated using atomic layer deposition (ALD) of several high- κ dielectrics such as Al_2O_3 ⁵², HfO_2 ⁵², HfAlO ⁵³ and ZrO_2 ⁵⁴.

The issues with developing a III-V MOS device as mentioned previously are due to the properties of native oxides present at the surface of the semiconductor. III-V surfaces readily react with atmospheric gases to form thick layers of native oxides. Surface layer oxides for the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ system generally exist in stable oxidation states of +5, +3 and +1 and small amounts of metallic As-As⁵⁵ with stable $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ oxides thought to include As_2O_3 , As_2O_5 , Ga_2O_3 , Ga_2O , In_2O_3 , GaAsO_4 and InAsO_4 ⁵⁵. Arsenic oxides have been determined to be the least stable oxides in the system and Ga oxides the most stable⁵⁶. GaAs systems have similar native oxides present, lacking the contribution from indium compounds and dimers and mainly consisting of As_2O_3 , As_2O_5 , Ga_2O_3 , and Ga_2O in addition to a small amount of elemental As⁵⁷. The native oxide of InP has largely been shown to consist of InPO_4 and In_2O_3 with In, P, P_2O_3 , P_2O_5 ⁵⁸ also possible. The presence of these native oxides at the interface with a high- κ oxide has led to Fermi level pinning as explained in the previous section, being observed in many III-V electrical devices and is associated with the poor electrical quality of the mixed native oxide layer.

To remove these native oxides and improve the interface many methods have been investigated. The surface pre-treatment of $\text{In}_x\text{Ga}_{1-x}\text{As}$ requires the removal of the In, Ga and As oxides and suppression of native oxide regrowth, the study of which is less established for $\text{In}_x\text{Ga}_{1-x}\text{As}$ systems than for the GaAs surface pre-treatment. Improvements in the electrical characteristics of III-V MOS capacitor devices can be achieved by reduction or removal of the III-V native oxides layers using various techniques such as chemical pre-treatments with

HF⁻⁵⁹, NH₄(OH)⁶⁰, or surface passivation methods (e.g. H₂S, (NH₄)₂S)^{61,62} deposition of interface passivation/control layers at the high- κ /III-V interface⁶³⁻⁶⁸, thermal treatment methods^{69,70}, ALD pre-pulsing of precursors⁷¹⁻⁷³, plasma treatment^{74,75}, atomic hydrogen exposure⁷⁰ and annealing^{76,77}. The removal of native oxides by ALD and surface passivation are dealt with in more detail in chapter 2.

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Chapter 2: Introduction to ALD and MOS analysis

2.1 Atomic Layer Deposition

Atomic layer deposition is a method related to Chemical Vapour Deposition (CVD). Atomic layer deposition is used to deposit conformal layers of films with thicknesses achievable down to sub monolayer¹ levels. In contrast to a CVD process where both precursors enter the reactor and react on the heated substrate surface simultaneously resulting in rapid deposition of a layer, ALD requires the sequential pulsing of these precursors. The use of sequential self-terminating gas-solid reactions is unique to the ALD technique. These reactions provide a self-limiting character to the process, making ALD a perfect process for use in coating and infiltrating materials where strict control of deposition thickness is necessary. However this strength of the ALD process is also the largest inherent problem readily apparent as growth rates for ALD processes are slow rendering it unsuitable for the growth of thick films.

Development of the Atomic Layer Deposition technique appears under two guises in earlier literature. In the 1960's ALD was theoretically discussed as molecular layering by soviet scientists². Their initial discussion makes mention of the deposition of titanium dioxide and germanium dioxide (TiO_2 and GeO_2). The more conventionally acknowledged origin of ALD is in the development of a technique called "Atomic Layer Epitaxy" by T. Suntola and J. Anston in Finland in the late 1970's and evidenced in the aforementioned authors patent

application³, which makes note of the use of sequential gas phase precursors ZnCl₂ and H₂S to grow a film monolayer by monolayer in conjunction with the use of vacuum to achieve this. The patent makes mention of the deposition of ZnS, SnO₂ and GaP, with the motivation to create thin film electroluminescent displays. Today ALD is used for a wide number of applications, such as: waveguides⁴, anti—reflective coatings⁵, solar cell technology⁶, magnetic read write heads⁷ and diffusion coatings⁸.

2.1.1 Principles of Atomic Layer Deposition

Atomic layer deposition as mentioned in the introduction is characterised by the use of self-terminating, sequential, gas-solid reactions. These reactions are self-limiting due to the finite amount of reactive sites that are available on a substrate combined with steric hindrance from precursor ligands. The technique for the growth of binary compounds can be summarised in 4 distinct steps illustrated in figure 2.1.

- 1.) Introduction of the first gas phase precursor in isolation into the vacuum deposition chamber and the chemisorption and subsequent reaction of this precursor on the surface of the substrate.
- 2.) A purge cycle, to remove any unreacted gas phase precursor, any gas phase by-products from the reaction and remove any weakly adsorbed species.
- 3.) Introduction of the second gas phase precursor and its subsequent reaction with chemisorbed species to produce the desired compound.
- 4.) A second purge to remove any unreacted species and products.

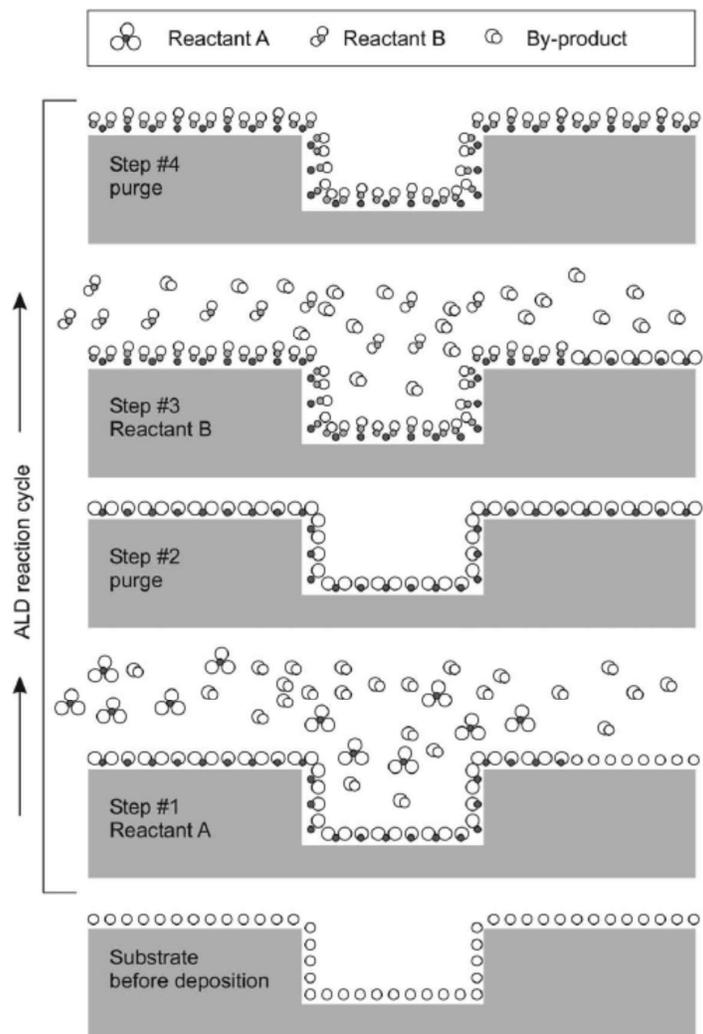


Fig. 2.1: A representation of the atomic layer deposition reaction cycle⁹

This process results in the growth of a “monolayer” of the desired film, defined as “the amount of adsorbate which is needed to occupy all absorption sites as defined by the structure of the surface and the chemical nature of the adsorbant”¹⁰ and each iteration of steps 1-4 is known as a “cycle” with the application of each reactant known as a “half cycle”. The process is repeated as many times as desired in this sequential fashion to build up a film of known thickness. Growth is generally described in terms of growth per cycle or GPC, this is

due to the tendency of most ALD processes not to grow complete monolayers but rather fractions of monolayers.

The adsorption of precursor molecules can be divided into two general classes on the basis of the strength of interaction between the adsorbing molecule and the solid surface; (i) physisorption – the physical adsorption of a molecule which is always reversible adsorption and (ii) chemisorption – the chemical absorption of a molecule which may or may not be a reversible reaction. It is important to note that only precursor molecules which are chemisorbed onto the substrate surface will be available to react, elevated reactor temperatures cause weakly bound physisorbed molecules to re-evaporate without reacting. It is important that sufficient purge times are left between the introduction of the second precursor to avoid any mixing of the precursor pulses (figure 2.2) leading to a CVD type growth.

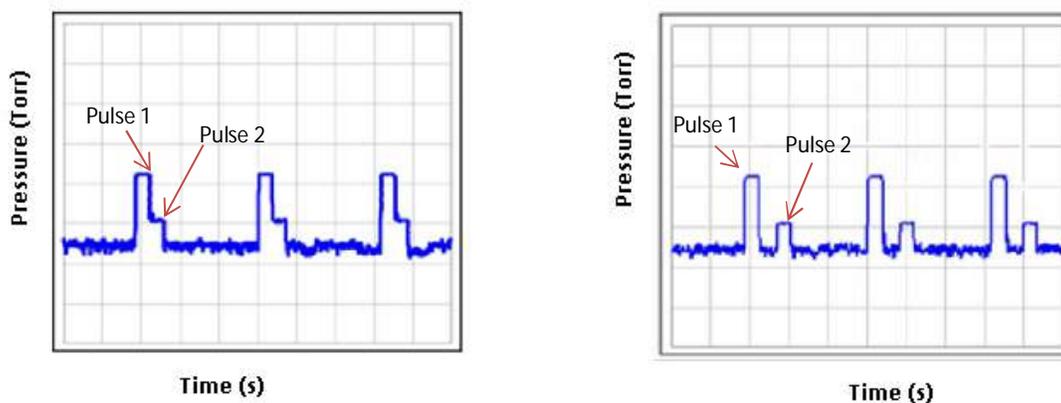
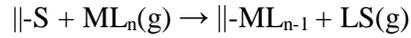


Fig. 2.2: An illustration of pulse overlap as a result of improper purge times which may result in CVD type growth compared to precursor pulses which are separated by a sufficient purge time to present distinct peaks.

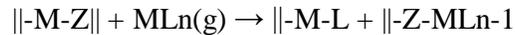
Chemisorption can occur as part of the ALD deposition mechanism in one of three ways; (i) ligand exchange, (ii) dissociation or (iii) association¹¹

(i) Ligand exchange mechanism: A reactant molecule (ML_n) is adsorbed onto the surface ($\parallel-S$) in the ligand exchange reaction



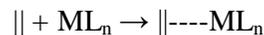
The precursor chemisorbs on the surface of the substrate and a metal ligand combines with a surface group to form a volatile product which may re-evaporate. Ligand exchange is the most common chemisorption method during ALD.

(ii) Dissociative mechanism: The precursor molecule is divided between two or more reactive sites on the substrate surface ($\parallel-M-Z\parallel$)



This method produces no gaseous by-products during this step but rather results in two species coordinated to the substrate surface.

(iii) Associative mechanism: in the associative method, the precursor molecule chemisorbs to an active site on the surface of the substrate without the release of ligands.



Secondly once the precursor has reacted in one of these ways to chemisorb to the substrate the amount of material which remains after these gas-solid reactions on the substrate may

vary due to desorption leading to different types of adsorption which may occur as illustrated below in figure 2.22.

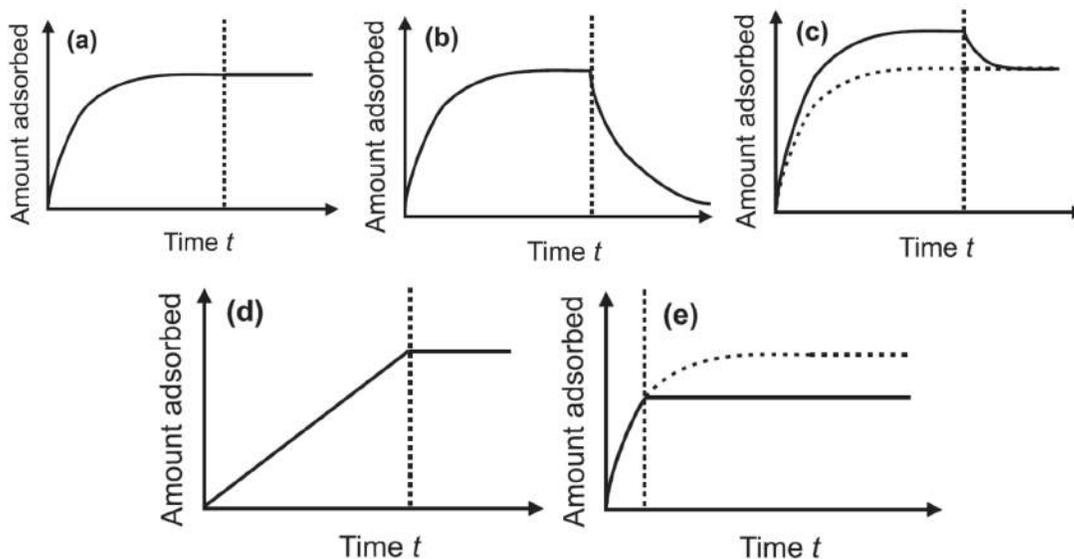


Fig. 2.3: Schematic illustration of different types of adsorption: (a) irreversible saturating adsorption (as required for ALD), (b) reversible saturating adsorption, (c) combined irreversible and reversible saturating adsorption, (d) irreversible non-saturating adsorption (i.e., deposition), and (e) irreversible saturating adsorption not allowed to saturate⁹.

Both irreversible and reversible adsorption can be fully saturating reactions as shown in Figure 2.3a and 2.3b respectively. For the adsorption to be self-terminating, the adsorbed material should not desorb from the surface during the purge. This implies that in ALD, the type of adsorption must be irreversible adsorption i.e. irreversible during the experiment.

2.1.2 Growth per cycle (GPC)

The growth per cycle of an ALD process is generally given in nanometres or angstroms, this growth rate is affected by several factors such as: partial pressure of reactants, number of reactive sites, duration of reactant pulse, surface functionalization of the substrate and

perhaps most importantly steric hindrance of ligands. Due to this it is necessary to undertake growth studies for different precursors to determine the growth per cycle and the optimum growth parameters. However a number of models have been proposed to theoretically estimate the maximum achievable growth per cycle possible for a precursor related to ligand composition.

The first model, developed by Ritala makes use of the size of ML_n reactant to estimate the GPC from steric hindrance¹². The size of the ML_n reactant is calculated from the density of the liquid reactant and the area covered by the reactant when it is assumed to be in a close packed monolayer. This was tested by comparing the deposition of titanium isopropoxide and titanium tetrachloride at 350°C achieving a growth per cycle of 0.30Å and 0.56Å per cycle respectively. Clearly, the less sterically hindered precursor yields a larger growth per cycle as it blocks fewer reactive sites present on the substrate. The second model, developed by Ylilammi *et al.*¹³ expands on this and calculates the maximum GPC from the size of the adsorbed ML_z species. To achieve this, the bond lengths of the metal and ligands must be either known or assumed. The third model developed by Simon, Aarik¹⁴ and Puurunen¹⁵ independently which calculates the maximum possible coverage based on the number and size of ligands bound to the metal.

Initial nucleation on substrates may be enhanced or retarded depending on the process and the initial functionalization of the deposition substrate. A nucleation delay where reactants do not react initially with the substrate, or only nucleate at certain areas may lead to island growth. This has been reported to have some dependence on the surface chemistry, with nucleation delays observed during the growth of zirconium oxide and aluminium oxide on hydrogen terminated silicon (100) substrates from $ZrCl_4$, TMA and H_2O at 300°C¹⁶. A study

by Frank et al¹⁷. further demonstrated that on H-terminated surfaces, an incubation period is necessary for deposition of Al₂O₃ and that the growth was initiated by a prolonged TMA pulse rather than a water pulse. On hydroxylated surfaces a linear dependence of the GPC of Al₂O₃ on –OH group concentration has been reported with GPC seen to decrease with increasing temperature, related to the desorption of hydroxyl groups from the surface¹⁸.

An ideal ALD process should exhibit a linear GPC. In practice some variation in growth rate may be observed before a linear growth rate is obtained, a small substrate enhancement may be evidenced. The converse is also true, with substrate inhibition occurring before the GPC stabilises to linear growth. As such each ALD process has a temperature window where “the reactions are saturating and the reactant neither physisorbs nor decomposes on the surface¹¹”.

For most thermal ALD processes this takes place between 200°- 400°. Temperatures outside of this “window” may cause incomplete reaction due to a lack of thermal energy to complete the reaction, precursor condensation on the deposition substrate which may lead to a higher growth per cycle or CVD like behaviour, re-evaporation of the chemisorbed precursor or decomposition of the precursor as illustrated in figure 2.4. Growth should be independent of the precursor pulse duration, provided pulses of sufficient duration to fully saturate the surface are used. To establish the ALD characteristics of a particular deposition process three growth studies must be performed: (i) determination of the effect of the number of deposition cycles on the film thickness i.e.: GPC, (ii) analysis of the variation of thickness/GPC with increasing/decreasing deposition temperature to determine the ALD temperature window and (iii) analysis of the effect of increasing/decreasing precursor pulse length on the thickness/GPC to establish fully saturating behaviour.

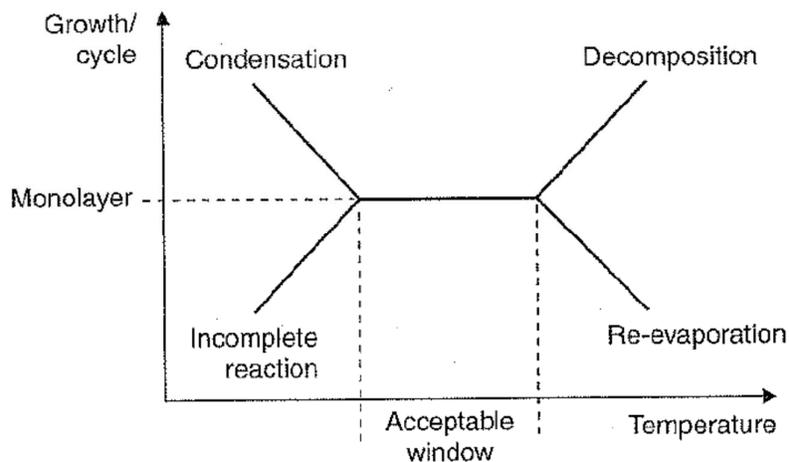


Fig 2.4: The temperature window and the effects of temperature on ALD precursors¹⁹

2.1.3 ALD Precursors

Since its inception many different classes of materials have been exploited as ALD precursors. There are several key features of a good precursor including sufficient volatility at a low temperature to ensure a high vapour pressure to allow transport to the chamber. A precursor must be thermally stable at the deposition temperature to prevent decomposition, discourage self-reaction to preserve the self-limiting nature of the deposition and have the ability to easily adsorb onto reactive surface sites. A good precursor should neither etch the growing film nor be incorporated into the film ensuring a pure film is grown. Precursors may be solids, liquids or gases but liquid and gaseous precursors are favoured due to the much larger vapour pressure of these precursors. Further precursor characteristics such as non-toxicity and low cost are desirable but not requirements. Precursors can generally be divided into two groups; organometallic reagents (which contain a metal carbon bond) and non-organometallic reagents. Some precursors commonly used in ALD are illustrated below in figure 2.5. High volatility precursors such as gases and highly volatile liquids may be fed directly into the reactor by rapid pulsing of valves. In contrast lower volatility liquids and

solids require the use of heated bubblers and transport lines to introduce them to the reactor vessel.

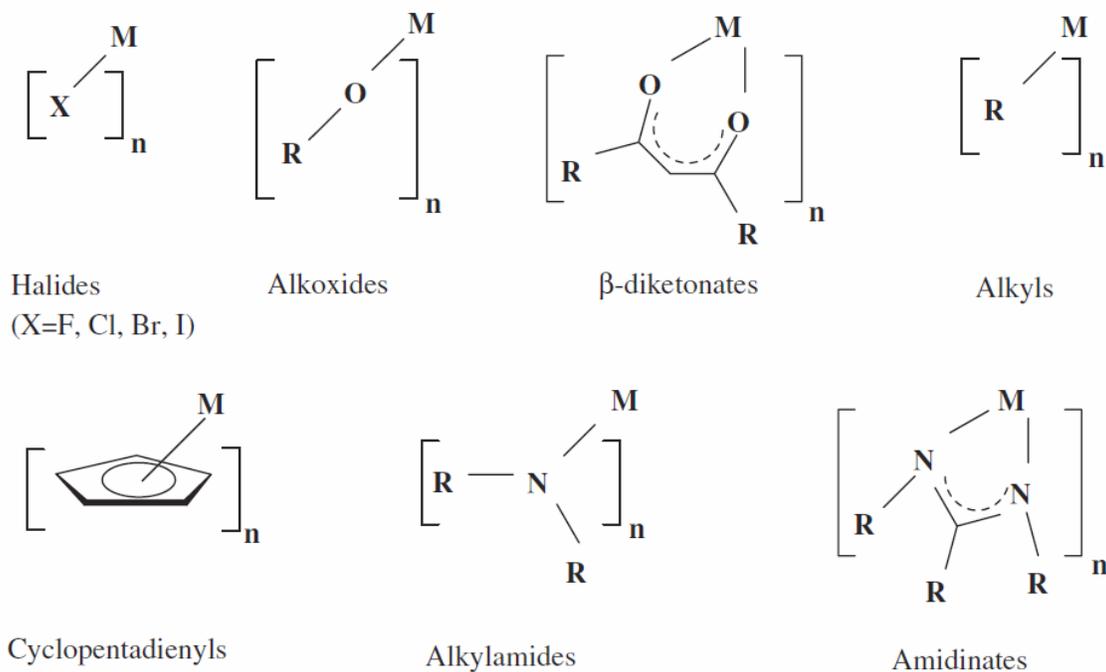


Fig. 2.5: Typical precursor ligands commonly used in atomic layer deposition.

A suitable co-reagent is necessary for film growth; in general gases such as O_2 are not suitable as elemental sources for thermal ALD as they are not reactive enough, though O_2 has been used as a co-reagent for the deposition of noble metal oxide films which catalyse the dissociation of oxygen on their surface²⁰. The most commonly used oxygen containing co reagent is water with ozone used in a significant minority of growth studies. Less commonly used oxygen containing compounds are N_2O , H_2O_2 , alcohols and oxygen radicals²¹.

2.1.3.1 Halides

Halides were implemented as precursor molecules in the first descriptions of ALD. Halides are generally available with high vapour pressures, have high thermal stability, are available for many metals and are highly reactive due to the halide ligand. Typically halides are solid but there are liquid examples like that of stannous chloride (SnCl_4). The high thermal stability allows surface exchange reactions to predominate allowing for excellent surface coverage of the deposition substrate. Halide complexes are small molecules. One advantage of this is a reduction in the steric hindrance while growing the film, yielding a larger GPC. Contamination of films via incorporation of halides can be a problem. Using halide precursors at lower temperatures, this can result in the creation of large numbers of rechargeable oxide traps present in the film^{22,23} furthermore the reaction by-products from halides are quite frequently strong acids e.g.: HCl, HF etc... which may etch the resultant film.

2.1.3.2 Alkyls

Alkyl precursors are true organometallic compounds, having a carbon-metal bond. This type of precursor was originally used in CVD and later adapted for use in an ALD process. Besides generally higher reactivity alkyl precursors make use of methyl or ethyl groups where possible to limit steric hindrance. Reaction products from these precursors are generally saturated hydrocarbons that are easily removed from the ALD system. Trimethyl aluminium (TMA) is a model example of an alkyl precursor and the TMA/water reaction is often cited as an example of “ideal” ALD exhibiting linear GPC, and a large temperature window.

2.1.3.3 Alkylamides

Alkylamides are ligands which contain one or more alkyl groups (such as ethyl or methyl groups) bonded to a nitrogen atom as an amine group. This type of precursor is noted to have high surface mobility, lending itself perfectly to conformal surface growth and exhibits high reactivity with surface hydroxyl groups. Examples of commonly used alkylamide precursors include tetrakisdimethylamino-hafnium (TDMAH; $\text{Hf}[\text{N}(\text{CH}_3)_2]_4$), tetrakisdialkylamino-hafnium (TDEAH; $(\text{Hf}[\text{N}(\text{C}_2\text{H}_5)_2]_4)$, and tetrakisethylmethylamino-hafnium (TEMAH; $\text{Hf}[\text{N}(\text{CH}_3)(\text{C}_2\text{H}_5)]_4$). Alkylamides are reactive towards water, O_2 plasma, and ammonia (NH_3) and are used for deposition of metal oxides such as HfO_2 , ZrO_2 and TiO_2 .

2.1.3.4 Amidinates

Acetamidinates are a newer branch of ALD precursors, whose use has been developed over the last decade and are promising candidates since they would appear to be available for most metals. Initial descriptions exist for precursors containing Co, La, Ni, Fe, Ag, Au, Mn and Ru²⁴⁻²⁶. Acetamidinates have also been investigated for the potential deposition of copper metal^{27,28} including the growth of Cu on Zn and SiO_2 substrates and extensive study into the mechanism of reaction of the precursor^{29,30}.

2.1.4 ALD Hardware designs

Typical ALD reactors in use for research purposes may be custom built or bought from commercial manufacturers. Regardless ALD kits consist of several components common to all systems: a vacuum deposition chamber, a vacuum pump, an exhaust trap, a high purity precursor carrier gas commonly N_2 or Ar to ensure a low rate of impurities, a heated precursor manifold, heated precursor delivery lines and a series of mass flow controllers (to

control gas flow) and swagelock ALD valves which are capable of opening or closing in the order of tens of milliseconds³¹. Reactors for ALD generally adapt to one of two common designs. Reactors may be flow tube reactors similar to a CVD reactor which operate from 1-10 Torr or resemble a molecular beam epitaxy (MBE) reactor, designed to operate at very low pressures and be adapted to incorporate plasma sources and various analytical tools such as the low pressure may be maintained throughout the system. In a reactor there are different mechanisms by which the gaseous flow of precursor can arrive at the substrate. Introduction of the precursor may take place either from above the centre of the substrate (“showerhead” configuration) or from the side of the substrate flowing across it (“cross-flow” configuration).

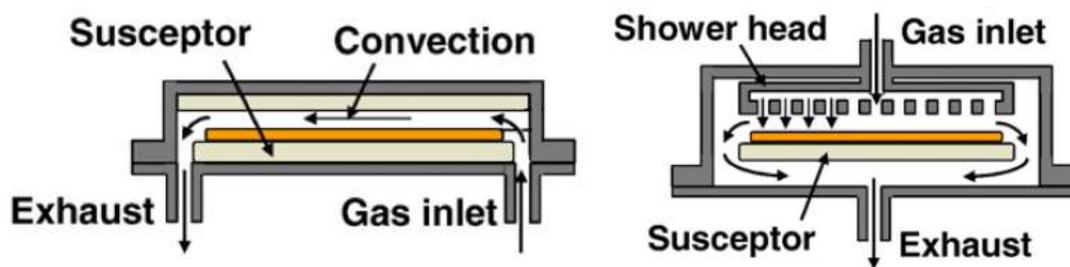


Fig 2.6: A comparison of an ALD cross flow reactor and an ALD showerhead reactor³²

Generally cross flow reactors require careful purging of the reactor to prevent a CVD process occurring at the leading edge of film growth, affecting the overall cross sample reproducibility of a process. A plasma source may be included either in the vacuum reactor or located remotely to form a plasma-enhanced ALD apparatus. A plasma source will usually operate at ~100-500 torr and does not use an inert carrier gas in the plasma half of the reaction cycle, but a carrier gas may be used during the alternating ALD half cycle. Another class of ALD reactor which is far more relevant to commercial concerns is the batch reactor,

which facilitates deposition of many substrates at the same time, reducing operating costs. At the time of writing, a number of companies supply commercial ALD kits such as ASM³³, Oxford Instrument³⁴, Beneq Oy³⁵, CambridgeNanotech/Ultratech³⁶, Applied Materials³⁷, Tokyo electron limited³⁸ and Picosun Oy³⁹

2.1.4.1 Thermal ALD systems

A thermal ALD process entails several deposition steps. Firstly a precursor is heated and evaporated to generate vapour pressure in a sealed bubbler. A valve is opened and the precursor is pulled under vacuum along heated delivery lines through to the vacuum deposition chamber. Heating of the lines is essential to prevent the condensation of precursor during transport. The two types of ALD chamber used for vacuum deposition are hot wall and cold wall reactors. A hot wall reactor utilises a heating jacket or jackets to surround the reactor tightly and maintains the reactor walls at or near the deposition temperature for the duration of the run. The advantage of hot wall reactors is that any deposition on the reactor walls from physisorbed precursor is a quality ALD film and should not disturb the flow of precursor in the chamber. Hot wall reactors also tend to allow for the quick purging of the reaction space due the higher precursor desorption flux from the heated walls. This coupled with a minimised internal surface area of a reactor allows for fast cycle times.

In contrast, cold wall reactors only heat the substrate to the deposition temperature while other reactor components are kept at a lower temperature. This allows delivery of precursors that may decompose at the deposition temperatures typical for hot wall reactors, but generally such reactors have longer purge times to ensure efficient removal of excess precursor or reaction by products and therefore may exhibit a greater CVD component due to the reduced rate of desorption of precursors from the cold wall surfaces causing crossover of pulses of precursors.

2.1.4.2 Plasma enhanced ALD systems (PEALD)

Plasma ALD is very similar in concept to thermal ALD and makes use of a plasma as the second reactant in the binary deposition process. A plasma is a collection of free charged particles created by applied electrical fields. A RF plasma source is used to disassociate precursor molecules into the desired plasma species which consists of reactive radicals, ions and photons. The advantage associated with PEALD is the energy supplied by the plasma as a co-reagent allows for the completion of chemical reactions which would normally lie outside the thermal ALD process window. It may also be considered an advantage the use of a plasma as a co-reagent due to the large sticking co-efficient of water which may lead to reduced cycle times for plasma processes compared to thermal processes which use water as a co-reagent. Typical plasmas used to grow thin oxides, metals and nitrides include O₂, N₂, NH₃, O₃ and H₂.

There are two common plasma sources possible in an ALD system; plasma exposure may be direct or indirect. In direct plasma the plasma is generated between the reactor showerhead and the substrate with the precursors exposed to all components of the plasma. This direct method imparts a large amount of energy to the precursor chemisorbed on the substrate which may increase the surface mobility of the precursor, increasing the film conformality, however direct plasma has drawbacks associated with it including possible surface damage of the substrate via roughening induced from the plasma. The second configuration possible is remote plasma; remote plasma ALD generates the plasma outside the reactor and only the generated radicals are introduced to the deposition chamber. The benefit of the remote plasma method is a noticeable reduction in damage to the substrate surface from particle impacts however this plasma is potentially less reactive than a direct plasma method.

2.1.5 Self-cleaning by ALD

The deposition of Al₂O₃ and HfO₂ layers on several III-V substrates has been reported to yield an improved semiconductor/III-V interface through the removal of native oxides. The reduction or complete removal of native oxides has been reported for multiple precursors on multiple III-V substrates. Self-cleaning reactions have been reported for TMA, TDMAH, TEMAH, TDMAT precursors⁴⁰⁻⁴³ and GaAs, InGaAs, InSb, GaSb and InAs^{40,43-47} substrates.

The initial report of self-cleaning by ALD was by Ye *et al.*⁴⁰ on GaAs substrates, displaying a thinning of native oxides on the GaAs surface to a layer 0.6 nanometres thick, removal of excess elemental arsenic atoms at the surface and realisation of low D_{it} values $\sim 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. Frank *et al.*¹⁷ subsequently demonstrated the reduction of GaAs native oxides from 2.5nm to 1nm upon deposition of 4nm of Al₂O₃. Brennan *et al.*, Lee *et al.* and Milojevic *et al.*⁴⁸⁻⁵⁰ (see fig. 2.7) all reported that both on GaAs and InGaAs substrates the initial metal precursor pulse is responsible for the majority of arsenic oxide removal with subsequent metal precursor pulses required to minimise the presence of gallium oxides. More detailed XPS investigations by Hinkle *et al.* shown in figure 2.8 confirmed that the initial metal precursor pulse removes native oxides with no re-oxidation of the semiconductor surface with subsequent oxygen containing precursor pulses. It was revealed from this XPS study that the initial pulse of TMA provided a reduction in the +3 surface states whereas the HfO₂ precursor provided a reduction in +5 native oxides present. This observation led to the postulation that clean-up reactions are precursor oxidation state dependant.

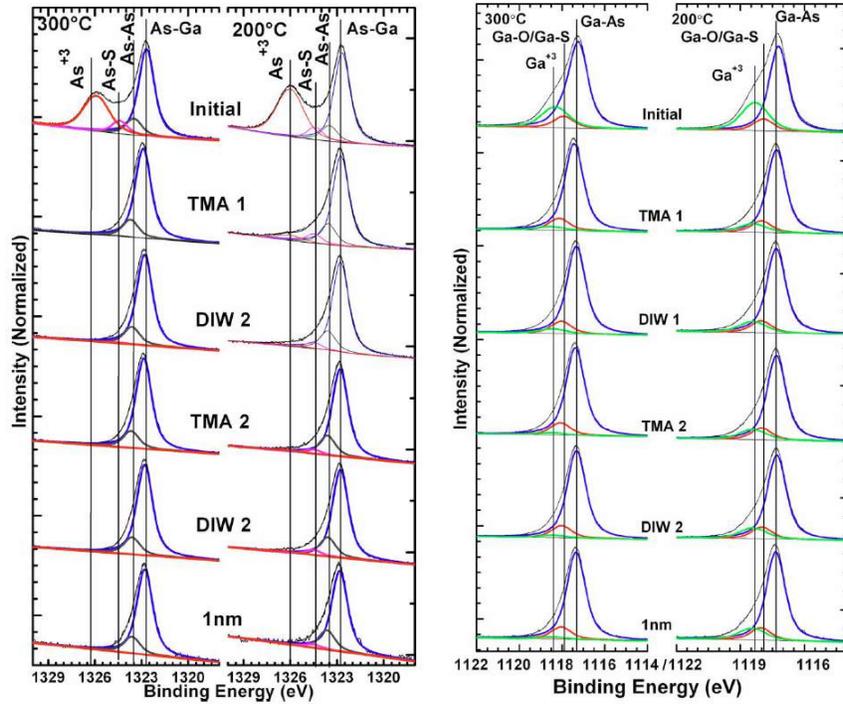


Fig. 2.7: XPS spectra detailing the reported initial clean-up of arsenic and gallium oxides following pulsing of TMA for 1 pulse, 2 pulse and 10 cycles of ALD with concurrent reduction in +3 oxidation states by Milojevic *et al.*⁵⁰

The self-cleaning mechanism during the use of TMA is believed to take place via a ligand exchange reaction whereby the Al^{3+} in the $\text{Al}(\text{CH}_3)_3$ precursor preferentially replaces arsenic and gallium oxides in the 3+ oxidation state, resulting in AlO_x formation and presumably $\text{As}(\text{CH}_3)_3$ and $\text{Ga}(\text{CH}_3)_3$ as volatile reaction products. This process has also been modelled for the TMA precursor by Klejna *et al.*⁵¹ Ligand exchange is proposed to explain the removal of As-O bonds with the accompanying production of elemental arsenic (As_4) which would evaporate at standard deposition temperatures. The same study predicts that organic ligands desorb primarily as C_2H_6 . Experiments to support ligand exchange theories with detailed XPS measurements have been carried out by Brennan *et al.*⁵² by pulsing TMA without an oxygen containing co-reagent with a subsequent growth of Al_2O_3 observed accompanying a decrease in the native oxides. More recently investigations of precursor dose

and Al₂O₃ interface formation suggests that self-cleaning and interface formation occurs during the first two cycles of Al₂O₃ deposition with bulk film growth initiated after this⁵³.

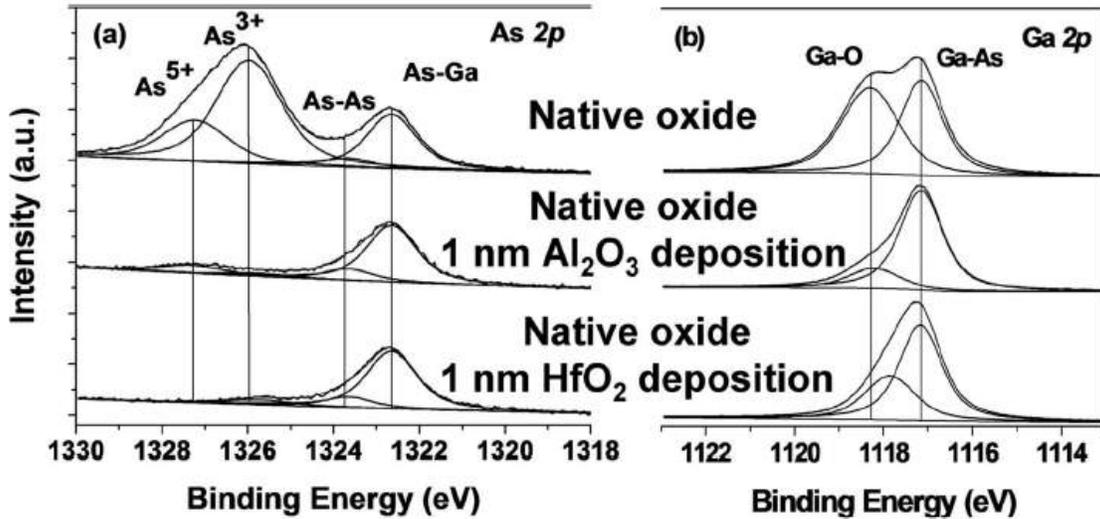


Fig. 2.8: (a) As $2p$ $3/2$ and (b) Ga $2p$ $3/2$ spectra, showing reduction of native oxides on GaAs. Oxide reduction is specific to the precursor with the removal of +3 oxides from 1 nm of Al₂O₃ and +5 oxidation states from 1 nm of HfO₂⁵⁴

Similar properties have also been observed by Suzuki et al, indicating that an interface control layer 0.2nm thick may provide the same benefit as thicker depositions when seeking to improve the high- κ /III-V interface⁵⁵.

The self-cleaning mechanism for HfO₂ precursors is currently unknown as the Hf precursor is in the +4 oxidation state and no direct ligand exchange is favourable with either +3 or +5 oxides indicating that the prevalent clean-up reaction must take place by another mechanism. To compound this, the use of TDMAH has resulted in some conflicting reports in relation to the temperature at which self-cleaning properties are observed, Shahrjerdi et al.⁵⁶ first reported that no self-cleaning takes places on GaAs at 200°C. Later Hackley et al.⁵⁷ reported interfacial oxide clean-up taking place at 275°C. Suri et al.⁵⁸ reported that TDMAH requires

a deposition of at least 300°C or higher to achieve an interface almost completely free from oxides. It has been reported that Hf loses one out of four Hf–N linkages in a TDMAH molecule at 275°C and two Hf–N linkages at 355°C an indication that clean-up reactions at ALD deposition temperatures may be facilitated by a TDMAH species with only 3 metal-precursor bonds⁵⁹. Most recently McDonnell et al.⁶⁰ have reported the same cleaning effects with TDMAH at lower temperatures of 200°C after a NH₄OH pre-treatment etch and attributed the discrepancies in reported cleaning action of the precursor as a result of ex-situ analysis allowing for re-oxidation of samples. Further work on determining the dominant mechanism is necessary to fully understand the clean-up reactions associated with hafnium alkylamide precursors.

2.2 ALD of metal oxides

2.2.1 ALD of Aluminium Oxide

Aluminium oxide (Al₂O₃) has been exhaustively described in literature as an “ideal” ALD process due to its thermal stability, its conformal and uniform deposition, and due to the fact that it can be deposited over a wide temperature range from room temperature (~25°C) to ~300 °C⁶¹ and is the most studied and used material in ALD at the time of writing. Although Al₂O₃ may be deposited using many diverse precursors e.g. AlCl₃⁶², AlMe₃⁶³, Al(NEt₂)₃⁶⁴ with many typical co-reactants e.g. water, oxygen⁶², ozone⁶⁴ and alcohols⁶³. The most common and facile ALD process makes use of TMA with water as the co-reagent via thermal ALD. Deposition of Al₂O₃ from TMA and water typically furnishes a GPC of ~1.0 Å/cycle, however, this is observed to decrease with increasing deposition temperature, related to dehydroxylation of the substrate surface⁶⁵. The reactions of the TMA/substrate surface and TMA/water, are self-limiting as TMA is highly reactive. The CH₄ by-product of the TMA/water process is inert and easily removed by pumping this is illustrated in figure 2.9.

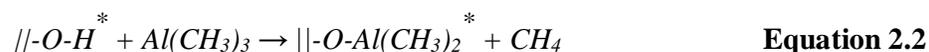
Al₂O₃ has been incorporated with current semiconductor research as its characteristic high κ -value ($k \sim 8.6$)⁶⁶ compared to SiO₂ ($k=3.9$) with low residual impurities and reproducible character are ideal for the fabrication of test devices. Research on III-V devices has also revealed the property of native oxide removal during the deposition of Al₂O₃ from TMA as discussed above. In this work Al₂O₃ was deposited from TMA and water. The deposition of Al₂O₃ using TMA and water, occurs via two half reactions, which together yield the overall reaction described in equation 2.1.

Overall reaction



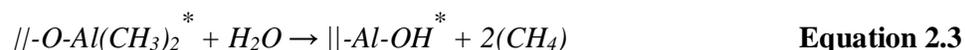
In the first half reaction (Equation 2.1), the TMA reacts with the surface O-H group, forming a Al-O bond and resulting in the loss of gas-phase CH₄.

First half reaction: Reaction of gaseous Al(CH₃)₃ with O-H terminated substrate surface:



In the second reaction, the water reacts with the $\| -O-Al(CH_3)_2$ surface, resulting in the formation of a new Al-O bond and the release of gaseous CH₄. The asterisk indicates a surface adsorbed species. (Equation 2.2).

Second half-reaction: Reaction of gaseous water with reactive surface:



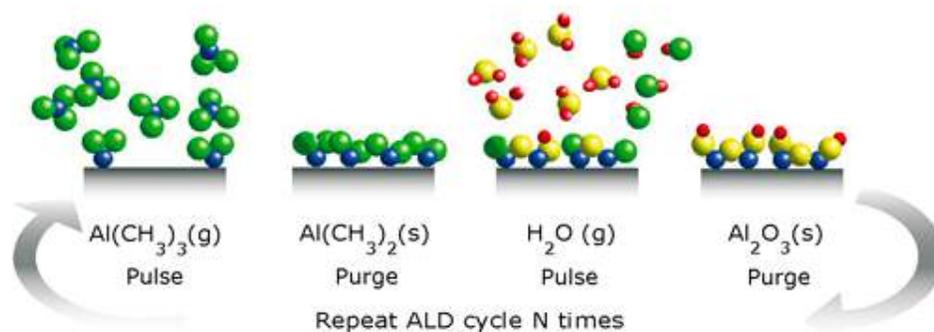


Fig. 2.9: Schematic representation of Al_2O_3 ALD process using TMA and water showing initial reaction of TMA with substrate surface (chemisorption), reaction of the surface with water, and formation of an Al_2O_3 layer following multiple cycles.⁶⁷

2.2.2 ALD of Hafnium Oxide

HfO_2 has emerged as a key area of interest in the deposition of high- κ oxides for CMOS and beyond CMOS applications. It has a κ -value of ~ 16 - 25 ⁶⁸ more than four times that of Si ($\kappa=3.9$) and displays high thermal stability which is a vital characteristic for CMOS applications. Initial studies of HfO_2 growth by vapour deposition primarily used HfCl_4 and water as precursors⁶⁹. It has been reported that HfO_2 films deposited by ALD display smooth growth with the roughness equivalent to the original surface on which it is deposited at low temperature⁷⁰. Deposition of HfO_2 using HfCl_4 and water below 300°C results in predominantly monoclinic phase HfO_2 ⁷¹. However, the use of films deposited from HfCl_4 for research electrical devices is not ideal as chlorine from the precursor may be incorporated into the film leading to an increase in threshold voltage and introduce extra interface states in devices⁷². Previous devices exhibited an increased leakage current attributed to the incorporation of chlorine atoms in deposited films when using HfCl_4 for deposition of HfO_2 ⁷³. The production of HCl as a by-product of the HfCl_4 /water deposition also further

raises concerns of the deposited film and the internal surface of the reactor being etched by reaction by-products as deposition occurs⁷⁴. Increasingly alkyl amides precursors are used for HfO₂ deposition due to their greater volatility and lack of halide atoms to contaminate films, with the hafnium alkylamide precursors TDMAH; Hf[N(CH₃)₂]₄, TDEAH; Hf[N(C₂H₅)₂]₄ and TEMAH; Hf[N(C₂H₅)(CH₃)]₄ recently being the most common precursors for the deposition of HfO₂ due to their increased volatility and high growth rates of typically ~0.93 Å/cycle⁷⁵. Of late focus has been in particular on TDMAH as it has a higher vapour pressure than TDEAH and TEMAH equivalents. Deposition of HfO₂ from TDMAH and water results in amorphous films when deposition is performed at less than 100 °C and entirely monoclinic films are formed at a deposition temperature of 300 °C and above⁷⁵. The reported GPC of TDMAH is 0.9Å/cycle with a reported ALD window of 200-300°C. Above 300°C a higher GPC has been reported of 1.1Å/cycle, possibly an indication of some precursor decomposition at higher temperatures⁷⁶.

In this work, HfO₂ deposition is undertaken using TDMAH and water. The deposition of the HfO₂ using these precursors is believed to proceed via a reaction mechanism which is influenced by bond-energy considerations and acid-base theory similar to that modelled for Hf[N(C₂H₅)(CH₃)]₄⁷⁷

The deposition of HfO₂ from TDMAH and water proceeds via two half reactions which together constitute the full reaction. The first half-reaction involves the reaction of the gaseous TDMAH with the active substrate surface (in this case, an O-H terminated surface) and the second reaction involves the incoming water molecule reacting with the Hf-surface species as described by the following reactions.

Overall reaction equation:



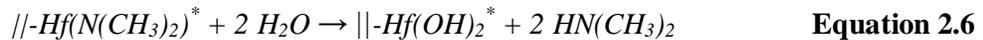
In the first half reaction (Equation 2.4), the TDMAH reacts with the surface O-H group, forming a Hf-O bond and resulting in the loss of gas-phase $\text{HN}(\text{CH}_3)_2$.

First half reaction: Reaction of $\text{Hf}[\text{N}(\text{CH}_3)_2]_4$ with O-H terminated substrate:



In the second reaction, the water reacts with the $\text{Hf}[\text{N}(\text{CH}_3)_2]$ on the surface, resulting in the formation of a new Hf-O bond and the release of gaseous $\text{HN}(\text{CH}_3)_2$ (Equation 2.6).

Second half reaction: Reaction of gaseous water with the reactive surface:



2.3 The ideal MOS Capacitor

The metal oxide semiconductor (MOS) structure is a planar structure which can be treated as a parallel plate capacitor since it consists of two conductors separated by an insulator. A much simpler analogue of the MOSFET, it consists of a semiconductor substrate, with a layer of insulating dielectric and finally a metal layer on top of which is a contact as illustrated in figure 2.10 below. In an ideal MOS capacitor charge will flow between the semiconductor and metal until a Fermi level equilibrium is reached in the system where the Fermi level is constant throughout. The capacitor has three distinct behaviours when the metal gate is

biased at various gate voltages. These bias regimes for a p -type device are i) accumulation where the bias applied is less than the flatband voltage, ii) depletion which takes place between the flatband voltage and the threshold voltage and iii) inversion where the bias applied is larger than the threshold voltage. All examples discussed in the following are for p -doped Si substrates with SiO_2 gate oxide.

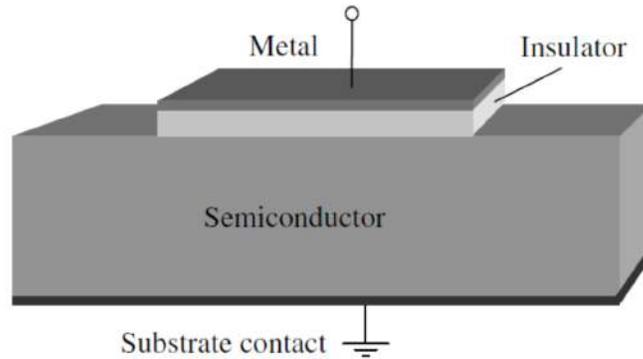


Fig. 2.10: A cross section of a generic MOS capacitor⁷⁸

The application of a negative voltage ($V_g < 0$) will draw majority carriers (holes in the instance of p -doped semiconductors) towards the semiconductor/oxide interface, leading to the formation of an accumulation layer of majority carriers at the semiconductor-metal interface as illustrated in figure 2.11.

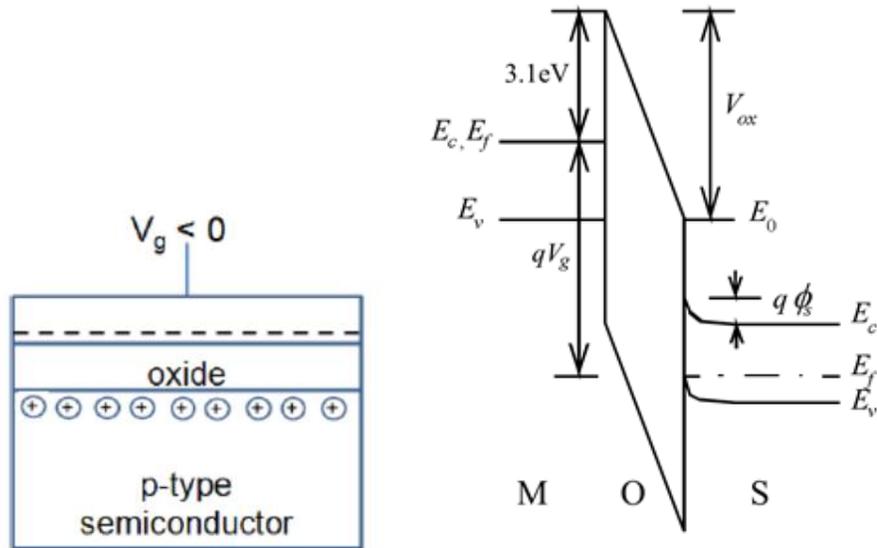


Fig. 2.11: Accumulation regime in p -substrate device showing accumulation of majority carriers (holes) at semiconductor/oxide interface when negative gate bias applied and the accompanying band structure. Adapted from ^{79,80}

In practical terms the flatband voltage is the voltage required to move bands to the same level as they would be in the ideal MOS capacitor situation i.e. the work function of both the metal and semiconductor are equal. This is not the general case as metals and semiconductors have different work functions and charge must flow between them. In the case of a silicon p^+ substrate the flatband voltage will be negative ($V_g < 0$). The application of a small positive voltage ($V_g > 0$) will cause holes to leave the semiconductor-oxide interface and move into the body of the device. This forms a depletion region free of holes as illustrated in figure 2.12 with the depletion zone signified by dashes. The depletion region still has charge associated with it as mobile holes are removed and ionized atoms remain in the lattice.

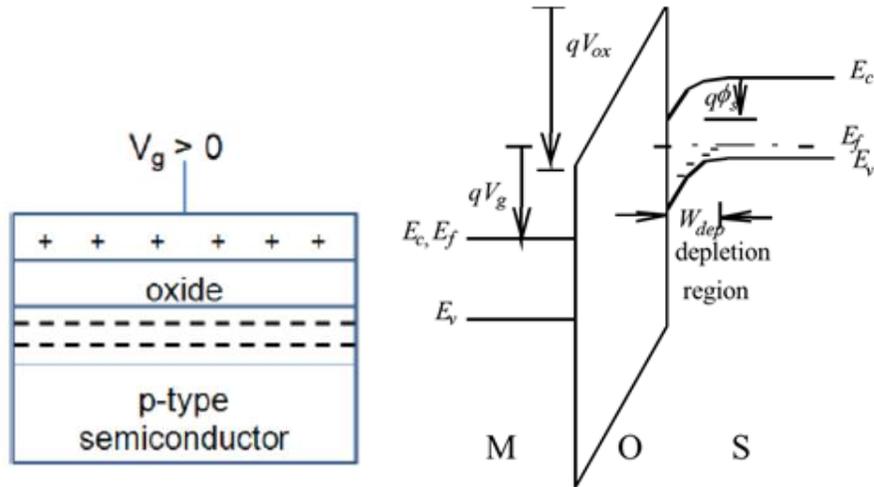


Fig. 2.12: The depletion regime in p -substrate device showing the depletion of majority carriers from the semiconductor/oxide interface when a small positive gate bias is applied and the accompanying band structure^{79,80}.

Increasing the applied voltage bias ($V_g \gg 0$) after depletion with sufficient charge will drive the device to inversion. In this case minority carriers will move to the oxide/semiconductor interface, this is dependant on the bulk generation of minority carriers and their diffusion to the interface. Minority carriers generated more than one diffusion length from the interface generally will recombine in the bulk. The onset of strong inversion indicates that the semiconductor is strongly changed to n -type at the interface as opposed to p -type in its bulk as illustrated in figure 2.13.

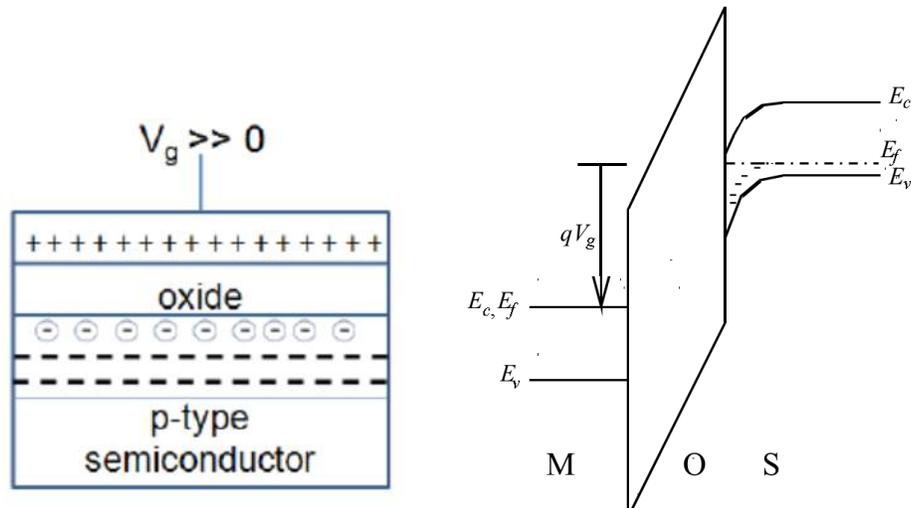


Fig. 2.13: The inversion regime in *p*-substrate device showing attraction of electrons (minority carriers) to the semiconductor/oxide interface until the concentration is higher than the hole (majority carrier) concentration, when a large positive gate bias is applied^{79,80}.

2.3.1 MOS capacitor analysis

2.3.1.1 Capacitance-Voltage (C-V)

C-V measurements provide a measure of the quality of an oxide film and can provide useful information on a MOS system including device parameters such as equivalent oxide thickness (EOT), flatband voltage (V_{fb}), determination of trapped charge via its hysteresis and an indirect measure of the level of interface defects (D_{it}). Since the MOS structure is simple to fabricate capacitance-voltage characterisation is widely used to analyse prospective materials. Overall the MOS structure is treated as a series connection of two capacitors. The total capacitance of the MOS system is composed of the oxide capacitance (C_{ox}) and the semiconductor capacitance (C_s) and is expressed in equation 2.7

$$\frac{1}{C_{total}} = \frac{1}{C_{ox}} + \frac{1}{C_s} \quad \text{Equation 2.7}$$

The capacitance of a MOS capacitor is measured as a function of the gate bias voltage using a small signal alternating voltage over a collection of operating frequencies. Figure 2.14 shows an ideal low frequency C-V curve for a p -type MOS capacitor with the regions of accumulation, depletion and inversion separated by the flatband voltage and the threshold voltage respectively. When a large negative gate bias is applied leading to accumulation behaviour, the concentration of holes at the semiconductor surface is much greater than the holes in the bulk semiconductor. This leads to a large capacitance contribution from the substrate C_s . If $C_s \gg C_{ox}$, then the contribution to C_{total} from C_s may be ignored as per equation 2.8, and therefore the measured capacitance in the accumulation region of a C-V curve is approximately equal to C_{ox}

Upon increasing the gate voltage holes are repelled from the semiconductor interface creating a depleted region at the semiconductor surface which causes a reduction in the contribution to the capacitance from C_s . Increasing the positive bias further reduces the C_s by increasing the depletion region in the semiconductor and therefore reduces the overall C_{total} . The capacitance of the system will be the oxide capacitance and a variable contribution from the depletion region.

Further increases in the positive bias, results in the attraction of electrons (minority carriers) to the semiconductor surface and facilitates the creation of an inversion layer and the contribution of the substrate decreases. The behaviour of the C-V curve is frequency dependant for MOS a capacitor, If the measurement frequency is low enough and swept in small increments e.g. 50mV then generated minority carriers have the ability to follow the applied bias and observed capacitance of the system is C_{ox} with the charge localised at the surface of the oxide and the depletion underneath.

However at higher ac measurement frequencies the minority carriers cannot respond to the applied ac bias. In this instance both the depletion region and the oxide region act as capacitors and inversion capacitance will be a product of these capacitances. An ideal low frequency C-V is presented in figure 2.14 with the onset of accumulation, depletion and inversion behaviour marked on the voltage axis. When a device is measured with larger increment of voltage then the capacitor may be biased into deep depletion, where the depletion region becomes larger than the predicted maximum width for a few milliseconds until minority carriers may be generated thermally, this manifests itself as further falling capacitance past the threshold voltage in the high frequency sweep.

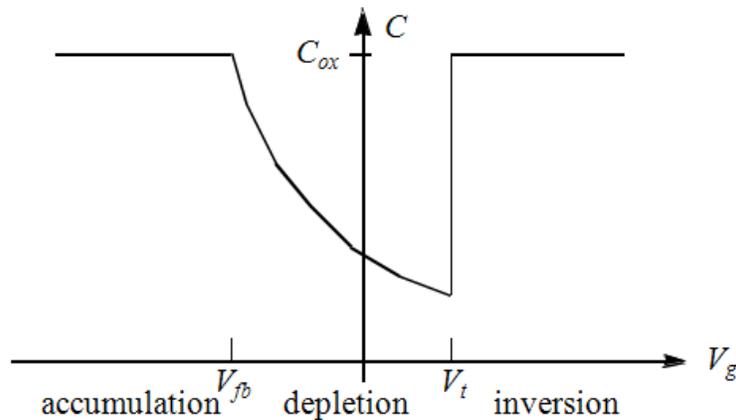


Fig. 2.14: An ideal low frequency Capacitance vs. Gate voltage diagram of a MOS capacitor fabricated on a *p*-type substrate⁸⁰.

2.3.1.2 Deviations from the ideal C-V characteristics

The high- κ /III-V interface is far from ideal and still not fully understood. Specific terminology was coined in 1980 in order to standardise nomenclature for charges in the Si/SiO₂ system, divided into four categories^{81,82} defects in the high- κ /III-V system are described in the same manner. The Si/SiO₂ system is visually represented in figure 2.15:

- i. Fixed oxide charges Q_f
- ii. Interface trapped charge Q_{it}
- iii. Oxide trapped charge Q_{ot}
- iv. Mobile ionic charge Q_m

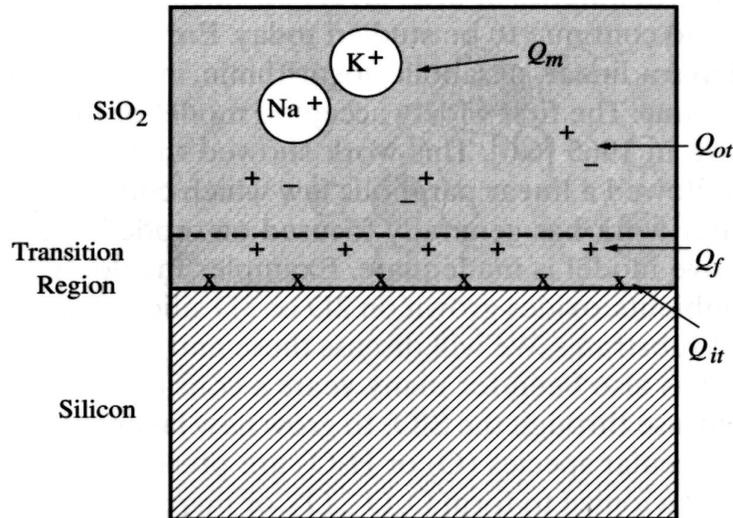


Fig. 2.15: Defect charges associated with the high- κ /III-V interface and their location in the system⁸³

Fixed oxide charge (N_{ox}): refers to charge in the oxide layer that is spatially removed from the interface but distributed through the oxide⁸². This charge does not change with respect to the applied potential and does not contribute additional capacitance to the CV curve. However fixed charge will cause a parallel shift in the CV curve with no horizontal stretch out; changing the threshold voltage for the device in question⁸⁴. Fixed oxide charge is generally introduced by unsatisfied bonding in the oxide. Positive charge will shift V_t to more negative voltages and negative charge will shift V_t to more positive voltages. The difference between the theoretical CV curve and the measured CV curve will provide a measure of the fixed charge in a MOSCAP.

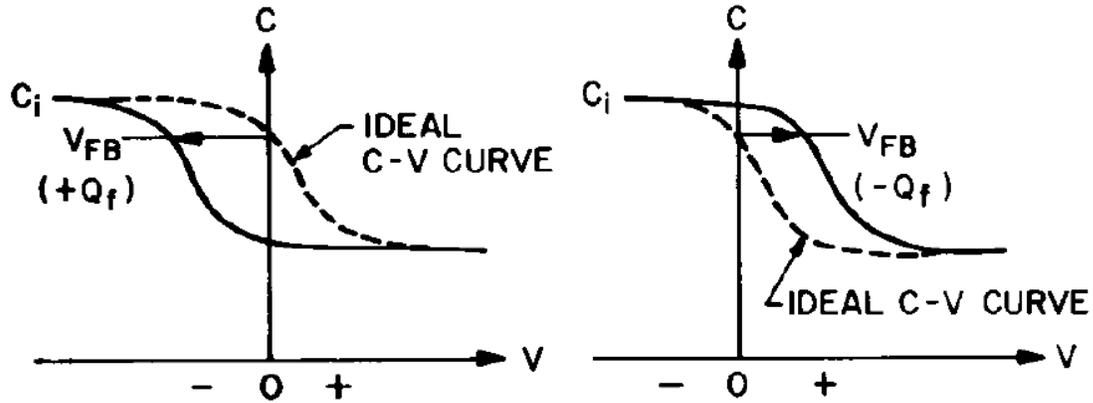


Fig. 2.16: Typical flatband shift in the C-V response due to presence of fixed oxide charges⁸⁴

Interface trapped charge (D_{it}): located at the semiconductor/oxide interface creating energy states in the band gap of the semiconductor, states will change occupancy as the gate voltage is swept approximately when the Fermi level energy is equal to the trap energy. Interface states are currently thought to be caused by the presence of As, In, Ga dangling bonds, As-As, Ga-Ga, In-In dimers and As_{Ga} antisites. Charge can flow between the semiconductor and interface states, in contrast to the fixed oxide charge. The net charge in these interface states is a function of the position of the Fermi level in the bandgap. In general for silicon devices acceptor states exist in the upper half of the bandgap and donor states exist in the lower half of the bandgap⁸⁵. An acceptor state is neutral if the Fermi level is below the state and becomes negatively charged if the Fermi level is above the state. A donor state is neutral if the Fermi level is above the state and becomes positively charged if the Fermi level is below the state. The charge of the interface states is then a function of the gate voltage applied across the MOS capacitor. The presence of interface traps increases the gate voltage needed to achieve a given surface potential because charges on the gate electrode need to neutralize both interface charges and charges in the semiconductor. The contribution of the interface trap capacitance raises the minimum capacitance of the device at low and high frequencies and will cause “stretch out” of the C-V

curve as seen in figure 2.16 below. This is not an issue for capacitors but corresponds to a degraded subthreshold swing in transistors which is very unfavourable as it affects the voltage at which the device may be switched on. A calculation of the C_{\min} and its comparison with the measured C-V curve allows an approximate determination of the interface trap density and acceptor or donor character (Appendix A).

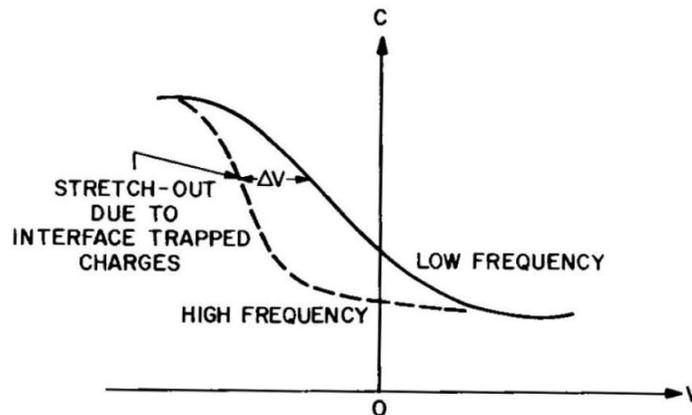


Fig. 2.17: Typical stretch-out with respect to frequency in the C-V response due to presence of interface trapped charges⁸⁴

Border traps (D_{bt}): also referred to as near interface traps and located up to 20\AA away from the interface may still change occupancy and are largely responsible for the hysteresis observed when a C-V sweep is performed from accumulation to inversion and back again. As both border traps and interface traps may capture charge carriers they are termed “switching” states, generally border traps change occupancy with a timescale related to distance from the interface. Border traps and interface traps may be differentiated by measuring a sample at elevated temperature. A temperature invariant or only weakly temperature dependant response is characteristic of charge carriers tunnelling through border traps^{86,87} whereas the interface trap minority carrier capture and emission rate is strongly dependant on temperature.

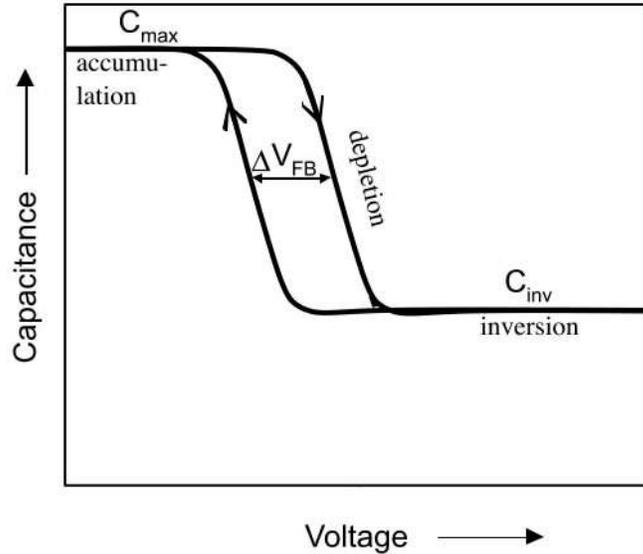


Fig. 2.18: Typical hysteresis in the C-V response due to presence of border traps⁸⁸

Mobile ionic charge: Generally mobile ionic charge is a remnant of processing and due to the presence of alkali ions such as Na^+ , K^+ , and Li^+ . The application of a gate bias causes these ions to migrate through the oxide, causing a change in the flat band voltage for the device. Modern processing techniques have all but eliminated mobile ionic charge as a source of defects in modern devices.

All of these are moieties commonly referred to as traps, although strictly speaking this is not true. A trapping event would entail the capture of an electron or hole from the conduction or valence band respectively and its subsequent re-emission to the same band. Whereas a generation-recombination event may take place also where the electron or hole is held in the energy level and an opposite charge carrier promoted to take place in a recombination reaction. Generally sites where generation-recombination takes place are found in the midgap and energy levels which are closer to the bend edges tend to trap charge carriers.

2.3.1.2 Leakage current mechanisms in MOS capacitors.

As previously mentioned low leakage current density is required for further miniaturisation of CMOS technology. Leakage current measurements are performed at reverse bias as this should increase the accumulation region width with no current flowing until a critical breakdown voltage is reached. However due to electron tunnelling and defects in the insulator gate, leakage will be observed before the breakdown threshold is reached. The most commonly discussed leakage mechanisms for thin films are direct tunnelling, Fowler-Nordheim tunnelling and Poole-Frenkel tunnelling and structural induced leakage current. Each tunnelling mechanism is observed under different circumstances with Fowler-Nordheim considered to be the dominant mechanism at high electric fields and Pool-Frenkel considered to be dominant at lower electric fields.

Direct tunnelling seen in figure 2.19 (a) below is a direct result of scaling gate oxide thickness (generally below 2nm), Scaling to decrease device size leads to an increase in gate leakage due to the probability of charge carriers existing on the other side of the gate oxide. Due to the wave nature of electrons in quantum mechanics when the electrons arrive at a potential barrier with a higher potential energy than the electron, the electron wave becomes a decaying function. Electron waves will emerge from the barrier as a traveling wave again but with reduced amplitude. In other words, there is a finite probability for electrons to tunnel through a potential barrier. The tunneling probability increases exponentially with decreasing barrier thickness. The tunneling leakage current for a given EOT for a particular oxide is dependent on the κ value of the gate dielectric, tunneling barrier height ($q\phi_r = \Phi_\beta$) and effective mass (m_{eff})

Fowler-Nordheim tunnelling (Figure 2.19 (b)) is the dominant leakage characteristic for thicker gate oxide layers (>3nm). When a MOS structure is under a large current bias, the insulator bands bend sharply and charge carriers may tunnel into these insulator bands and subsequently

into the semiconductor. This is different to direct tunnelling as it will only take place when sufficient current is applied to allow tunnelling through a triangular potential barrier.

High- κ dielectrics may also display some gate leakage at low gate bias; this can be attributed to Poole-Frenkel tunnelling (Figure 2.19 (c)) which is assisted by the traps in the bulk of the oxide. Thermal excitation of electrons allows them to emit from traps into the conduction band of the dielectric. The application of an electrical bias to the device results in a reduction in the potential energy barrier the electron must overcome to be promoted to the conduction band. This reduction in potential energy increases the probability of an electron being thermally excited out of the trap into the conduction band of the dielectric

One further mechanism which may affect the leakage current density in the system is Structural Induced Leakage Current. This occurs when local variations in surface roughness are present on the semiconductor surface or the top electrode. For a rough electrode or film, due to the fluctuation of the surface height, the local electric field will vary from place to place. At a peak of a rough surface the electric field is larger than in a valley and we expect the leakage current density to be higher at that peak than in a valley. Leakage current density is exponentially proportional to the applied electric field applied so we see a corresponding increase in the local leakage current density at these peaks. This leads to poor cross wafer uniformity being observed in devices and a large distribution of leakage and breakdown behaviours.

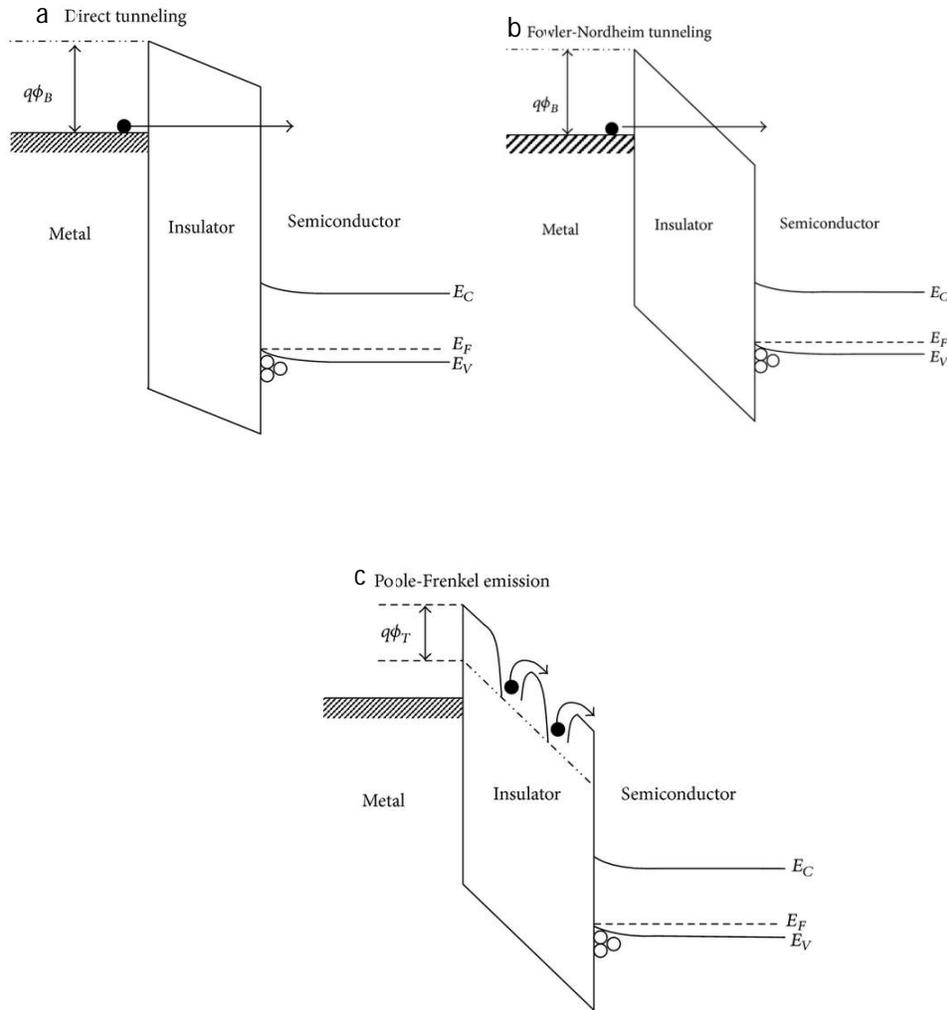


Fig. 2.19 (a) the mechanism of direct tunneling and calculated scaling limits for several oxides (b) Fowler-Nordheim tunnelling and (c) Poole-Frenkel tunneling⁸⁹

2.3.1.4 Determination of interface state density

To experimentally estimate the density of interface states (D_{it}) present in bilayer samples presented in this work the conductance method is used. This method was initially discussed by Nicollian and Brews⁹⁰ for determination of D_{it} from Si MOS devices; however it may be adapted to analyse III/V devices also⁹¹. The conductance method measures the conductivity of a sample as it is biased from the weak inversion regime to the depletion regime to limit the effect of minority carriers on the measurement. As a device is biased slowly traps with energies close to the Fermi level can change their occupancy, provided the response time is

small. Each trap has a frequency dependant trap response time determined from Shockly-Read-Hall statistics. The technique measures both the conductance and capacitance of a sample simultaneously with respect to frequency and voltage bias. The conductance is a measure of the occupancy and emission of majority carriers from the interface states, resulting in an energy loss, this energy loss is not observed at very high frequency as the interface traps cannot respond. The measurement of these parameters allows for the parallel conductance to be calculated from calculated and measured capacitances and conductances as per equation 2.10. Where C_{ox} is the calculated capacitance of the oxide, C_m is the measured capacitance of the oxide, ω is the angular frequency ($2\pi f$), G_m is the measured conductance.

$$\left\langle \frac{G_p}{\omega} \right\rangle = \frac{\omega C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2}$$

Equation 2.10

The normalised conductance (G_p/ω) is plotted as a log function of frequency and will show peaks related to interface states changing occupancy. This frequency dependant response is related to the frequency dependant trapping time constant. D_{it} is estimated from the normalised conductance peaks from equation 2.11 where the capacitance of the D_{it} response is proportional to the interface trap density and where q is the charge of an electron.

$$D_{it} = \frac{2.5}{q} \left(\frac{G_p}{\omega} \right)_{peak}$$

Equation 2.11

Limitations of the conductance method include that it cannot provide accurate estimates of the D_{it} for interfaces with a large D_{it} . Specifically where the interface trap capacitance is larger than oxide capacitance Specifically, if the The conductance method also relies on C_{ox}

being accurately known if C_{ox} is overestimated then estimates of G_p/ω will be lower than the true G_p/ω values

CV based methods to determine the density of interface traps generally make use of the high-low frequency methods previously developed for Si devices. As the capacitance-voltage curve of a MOS capacitor consists of three main components: the oxide (C_{ox}), the semiconductor (C_s) and the interface states (C_{it}) capacitance contributions, each capacitance component exhibits a different dependence on the applied bias, temperature, and measurement frequency. Assuming a constant capacitance contribution for the oxide, both the semiconductor and interface state capacitance responses vary with bias and frequency.²¹ When all the interface states are able to respond to the measurement frequency, their associated capacitance is added to the semiconductor differential capacitance which in turn is in series with the oxide capacitance. The total measured capacitance can then be expressed as

$$C_m = \left(\frac{1}{C_{ox}} + \frac{1}{C_{it} + C_s} \right)^{-1} \quad \text{Equation 2.12}$$

At low frequency, the interface traps have time to respond to the slowly changing ac signal when the signal is ramped slowly and therefore add a capacitance to the measured low frequency CV curve. When measuring the low frequency curve as low a frequency as possible is desired in order to maximize the interface state response. C_{ox} is determined experimentally from a thickness series C_{tot} is the total measured capacitance from the low frequency and high frequency CV curves respectively. The capacitance from interface states can then be calculated from equation 2.13 i.e. the difference between the high and low CV curves should only be due to the presence of C_{it} - this method is known as the Castagne-Vapaille method⁹².

$$D_{it} = \frac{C_{ox}}{q} \left(\frac{C_{tot}^{lf}}{C_{ox} - C_{tot}^{lf}} - \frac{C_{tot}^{hf}}{C_{ox} - C_{tot}^{hf}} \right) \quad \text{Equation 2.13}$$

The Terman method⁹³ makes use of a high frequency curve alone, where the measurement is taken at sufficiently high frequency that there is no contribution to capacitance from traps. Stretch out in a CV curve caused by interface traps is measured and compared to the ideal high frequency measurement and D_{it} calculated as per equation 2.14.

$$D_{it} = \frac{C_{ox}}{q} \left[\left(\frac{\delta\psi_s}{\delta V_g} \right)^{-1} - 1 \right] - C_{dos}(\psi_s) \quad \text{Equation 2.14}$$

A source of error for the CV-based methods is that the measured low frequency and high frequency CV curves are assumed to be true low and high frequency CV curves with all traps contributing to the CV at low temperatures and no contribution existing in the high frequency CV curves. The Terman method also requires comprehensive modelling to furnish an ideal CV to compare to the measured CV curve. This introduces an extra source of error as the doping density of the semiconductor must be accurately known to calculate an ideal CV curve.

2.4 Surface passivation

Initial reports of devices fabricated on III-V semiconductors had reported an invariant barrier height after the deposition of several metals as a gate electrode resulting in the Fermi level pinning phenomenon as explained in section 1.1.5. The cause for this invariant barrier height was not initially clear but became apparent three decades ago when the removal of native oxides from a GaAs wafer by Brillson et al. under ultra-high vacuum led to an “absence of Fermi level pinning”⁹⁴. Subsequent investigations by Offsey et al.⁹⁵ revealed that removal of native oxides would result in a reduction of interface defects with a corresponding

reduction of surface recombination, intrinsic band bending and the possibility of modulating the Fermi level. This led to a search for more robust and facile approaches for the removal of native oxides present on III-V semiconductors and prevent the re-oxidation of surfaces.

Standard guidelines for the passivation of silicon semiconductors were published in 1991 when Kaxiras⁹⁶ established his guidelines for “valence mending” which are also applicable to the passivation of III-V systems and are summarised as follows:

- i) The valence difference between the substrate and the surface passivant should be such that, when adsorbate atoms replace the bulk-terminated plane, all the broken covalent bonds are eliminated.
- ii) The adsorbate must exist in a bulk phase with the same local bonding geometry as in the restored surface.
- iii) The difference between the covalent radii of the adsorbate and the substrate should be as small as possible.
- iv) The difference between the bond angles of the adsorbate in its bulk phase and in the restored surface geometry should be as small as possible.
- v) Finally the formation of the restored surface should be an exothermic process but the energy released should not be large on the scale of surface bond energies, since undesired reactions such as etching may follow.

The characteristics of group VI elements lend themselves for use as passivation agents for III-V semiconductors. Chalcogenide passivation was largely investigated after 1987 when Sandroff et al. observed large increases in photoluminescence intensity from a GaAs/AlGaAs transistor by spin coating sodium sulphide salts onto the wafer at the start of device fabrication⁹⁷ This work was closely followed by Carpenter *et al.*⁹⁸ making use of Na₂S and (NH₄)₂S to passivate GaAs with an improvement in interface quality and a retarded re-

oxidation rate observed. Many subsequent combinations of etchant and passivating elements emerged in an effort to increase the photo luminescence from treated semiconductors however nearly all combinations applied in the literature have an inherent drawback when fully functioning electrical devices are to be fabricated, as summarised below in table 2.1. Experiments also suggest that thermal excitation and illumination may activate a solution and encourage sulphur binding on the surface of III-V semiconductors^{99,100} with an absence of sulphur bonding observed for *p*-type photodetectors with sulphur treatment carried out in the dark¹⁰¹.

$\text{NaS} \cdot 9\text{H}_2\text{O}$ ⁹⁷	Sodium ion contamination
S_2Cl_2 in CCl_4 ¹⁰²	Carbon contamination
$\text{P}_2\text{S}_5/\text{NH}_4\text{OH}$ & $\text{P}_2\text{S}_5/\text{NH}_4\text{S}$ ^{103,104}	<i>p</i> -type doping effect caused
$(\text{NH}_4)_2\text{S}$ ^{105, 106}	Elemental sulfur deposits on the surface, transient effect.

Table 2.1: A summary of surface passivation procedures and potential issues associated with their use.

More recently a concerted effort was made by Brennan et al. to review many past passivation processing parameters and to collate them into an ammonium sulphide etch¹⁰⁵. The efficacy of this optimised etch parameters was tested by O'Connor *et. al*¹⁰⁶ leading to largely improved performance of III-V MOSCAPs. A separate study by Gu et al.¹⁰⁷ examining the effect of etch concentration on III-V MOSFET performance reached similar conclusions with respect to optimum processing conditions for passivation from aqueous solutions of ammonium sulphide. Gas phase passivation as opposed to solution chemistry has been

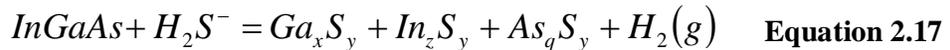
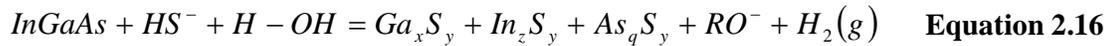
previously investigated, most commonly using H₂S and H₂S/H₂ plasma.¹⁰⁸⁻¹¹⁰ More recently Alian et al.¹¹¹ have suggested that minimal exposure to ammonium sulphide vapour rather than full immersion into a solution can provide a surface passivation as effective as aqueous solution chemistry for In_{0.53}Ga_{0.47}As.

2.4.1 Mechanism of action

The mechanism of action for aqueous ammonium sulphide passivation has been postulated by Bessolov *et al.*¹¹² In solution ammonium sulphide will disassociate to yield two possible passivation species, HS⁻ and S²⁻



With passivation taking place via:



Aqueous solution ammonium sulphide has a pH ~ 8, the main passivant species present is SH⁻ with an almost negligible amount of S²⁻ observed, which may be ignored¹¹³ and small amounts of H₂S. The choice of solvent has an impact on the passivating species present, with organic solvents shifting the equilibrium to the right, causing more H₂S to form as per equation 2.12. Bessolov and Lebedev et al. have shown that passivation of semiconductors is greatly improved from alcoholic solutions with low dielectric permittivity and solutions with increased alkalinity^{114,115}. The polarity of the sulphur solvent has been modelled to have a

large impact on the bonding method of HS^- ¹¹⁶ due to hydrogen bonding between sulphur atoms and solvent molecules upon solvation, changing the reactivity towards nucleophilic addition.

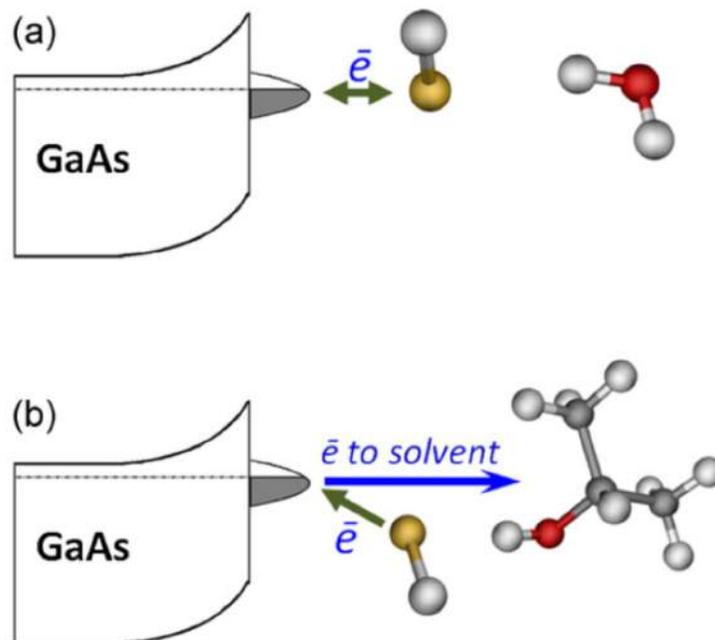


Fig. 2.20: The proposed effect of solvent polarity on surface chemistry during the passivation process¹¹⁷.

This gives rise to two types of bonding which may occur i) in aqueous solutions HS^- will act as a weak nucleophile leading to bonding which is covalent in nature, causing electrons in surface states to remain localized with only a small change in band bending. ii) Alcohol solvated ions will always be strongly nucleophilic, allowing electrons from surface states to transfer to solvent molecules (Figure 2.20), leading to ionic bonding between the surface and HS^- with an accompanying larger reduction in band bending. These two differences in mechanism lead to passivation by two sulphur atoms covalently bonding to As dimers or ionic sulphur insertion between As dimers¹¹⁸

2.4.2 Integration with current technology

While there is evidence that alcoholic solutions of ammonium sulphate lead to lower surface recombination and improved interface characteristics this is quite difficult to incorporate into modern process flows as photoresist tends to be soluble in alcohols, with several alcohols recently tested¹¹⁹ and all photoresists exhibiting damage from etching, stability was noted in aqueous solutions for up to 10 minutes however this requires the use of high quality reagents as metal contamination will adversely affect fabricated electrical devices. This provides an indication that it is possible to integrate aqueous solution passivation with current processing parameters.

Surface studies after sulphur passivation of InGaAs surfaces also exhibit a nucleation delay during subsequent ALD processes while depositing high- κ layers with TMA¹²⁰, associated with a lack of surface -OH groups, this may be an important factor when attempting to scale the gate dielectric and may be applicable to other precursors used to deposit high- κ dielectrics. Investigation of passivated interface with high- κ dielectrics by Garfunkela et al.¹²¹ reveals that 1-2 molecular layers of sulphur may be incorporated at the high- κ layer and remain mobile during device processing. Synchrotron studies have also reported the incorporation of sulphur via Arsenic displacement¹²². It has been reported that desorption of sulphur may be achieved by illumination with uv light under UHV and elevated temperature¹²³ which can provide a surface free of excess sulphur prior to the deposition of the high- κ gate oxide. Degradation of the sulphur passivation has been postulated to occur via a photo-oxidation reaction, experimental studies by Sandroff *et al.*¹²⁴ have shown that illumination of the surface in vacuum and oxygen exposure alone in the dark do not cause re-oxidation of the sulphur passivated GaAs surface, however both in conjunction cause the re-oxidation of the passivated layer.

2.5 Plasma pre-treatment

Plasma is a collection of free charged particles which contain equal numbers of positively and negatively charged particles. Plasmas are generated by the application of an electric field at a certain frequency, generally 13.56MHz or 2.45GHz for commercial systems. The application of this electric field causes the acceleration of electrons at a much faster rate in this field than other species present due to an electrons low mass. The oscillation of the electrons in the electric field causes heating, which leads to the ionization of gaseous species through collisions with energetic electrons. Subsequent species generated from these collisions may chemisorb or physisorb onto semiconductor surfaces. With the occurrence of chemisorption, volatile products may be formed by reaction of molecular ions with native oxides present on the semiconductor surface which are then released into the gas mixture in the chamber. The use of H₂/Ar plasmas on III-V semiconductors such as in this work is thought to lead primarily the ArH⁺ ion as the reactive species for etching reactions¹²⁵. As remote plasma is used in the instance H radicals will be the main species to impinge on the semiconductor surface and remove native oxides as hydrides and water. However this process also competes with depletion of the group V element from the surface as the mono- or tri-hydride, which leads to pitting of the surface of the semiconductor. Plasma treatments must be refined to selectively reduce native oxides present at the semiconductor surface without removing group V elements and degrading the semiconductor surface.

2.6 Ellipsometry

Ellipsometry is a technique which measures the change in polarization as light reflects from and transmits through a material. Electromagnetic waves consist of an electronic component and a magnetic component at 90° to each other with a fixed amplitude ratio. When considering the effects of reflection on incident light, the magnetic portion of the wave is

usually ignored. Light may be polarized in one of three ways, linearly, circularly or elliptically demonstrated in Fig.2.19. Ellipsometry uses linearly polarized light which when reflected off a sample changes polarization to elliptical. Ellipsometry measures this change in polarization and quantifies it as a change in the fixed amplitude ratio p and s components of polarised light defined as ψ and a phase difference defined as Δ . If a linearly polarized light of a known orientation is reflected at oblique incidence by a surface, the reflected light is elliptically polarized, as demonstrated in fig. 2.19

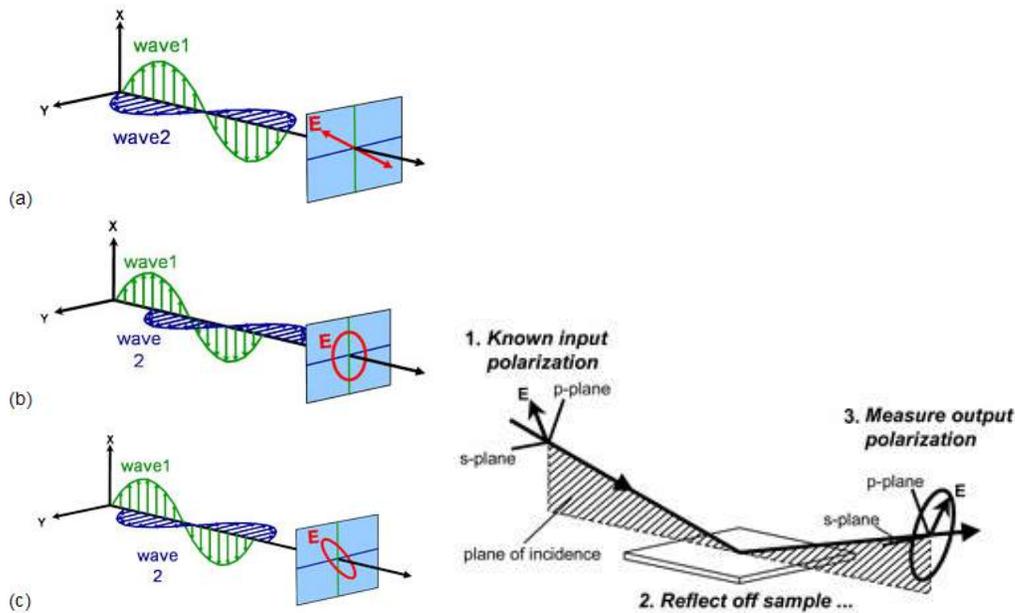


Fig. 2.21: A diagram displaying the polarization of light as linear, circular and elliptical and a schematic explanation of the ellipsometry process displaying the change in polarization of linearly polarized light as it is reflected from a sample¹²⁶.

The optical constants of the film are designated η and κ . The index (η) describes the velocity of light as it travels through the material compared to the speed of light in a vacuum. κ is the extinction co-efficient which describes the loss of energy as the wave travels through the

material. The overall refractive index of a material is a product of these two values $n = \eta + i\kappa$. Not all materials have an imaginary portion ($\kappa = 0$) e.g glass but generally $\kappa > 0$. Commonly thin films will have different optical constants than bulk films and optical constants will vary with measuring wavelength. Once a measurement has been taken it is placed into a model and a linear regression analysis conducted. To begin this process a film thickness and estimates of the optical constants must be provided. Thickness for ALD films may be estimated from the GPC of a precursor and initial estimates for optical constants from bulk films or a thickness series of films measured by CV. Once initial measurements are taken they can be subjected to an ordinary least squares linear regression analysis, schematically illustrated below in figure 2.20.

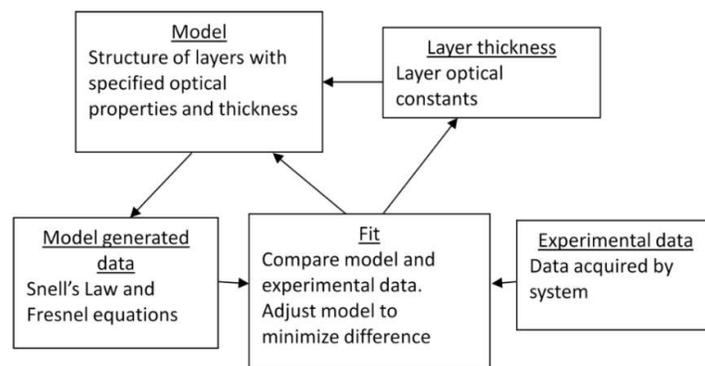


Fig. 2.22: A block diagram indicating the analysis steps from raw data measurement to fitting with an established model¹²⁷.

2.7 Electrical device fabrication and characterization

2.7.1 Lithography

Lithography is a process used in the fabrication of microelectronic devices using light to pattern masking layers on a wafer and transferring these patterns by selective dissolution of the masking layer. Lithography uses chrome masks to project the desired pattern to a film of

ultraviolet sensitive photoresist which has been uniformly spin coated onto the substrate. Subsequent treatment with chemicals will complete an etch leaving the desired pattern. A resist will comprise of several different chemical components such as a resin to offer the chemical resistance to processing, a sensitizer which will be a photo active compound sensitive to UV radiation and cause the physical properties of the resist to change after exposure to UV radiation, a solvent which will control the properties for deposition such as viscosity and some masks may have an adhesion promoter present.

Lithography may be divided on two basic properties: The type of resist that is used, either positive or negative - For positive resists, the resist is exposed with UV light wherever the underlying material is to be removed and negative resists are the opposite. The type of patterning that is used to pattern the resist may be divided to either - contact or proximity. The type of lithography used is dictated by the type of device being fabricated with each having distinct advantages. Both types of lithography use the same equipment but have large principle differences in the result obtained from exposure of the resist to UV. In negative lithography the areas which are exposed to light will be cross-link polymerized creating longer polymer chains, providing resistance to the developer chemical. Positive lithography is the opposite of this process, where areas that are exposed to light will be more soluble in the developer chemical, thus patterning the wafer. The principal differences between the use of either resist can be summarised as follows:

Resist	positive	negative
Price	high	low
Solvents	aqueous	organic
Sensitivity	low	high
Resolution	high	low

Table 2.2: A table summarising the properties of positive and negative photoresists.

Contact lithography consists of bringing the chromium mask into contact with the resist. By doing this diffraction that may occur between the mask and the resist is minimized, thus increasing the resolution of the system without having to change the exposing wavelength or the aperture of the system allowing for the fabrication of high resolution systems. However the downside to using this type of system is that the resist can become damaged by contact with the mask causing the creation of defects in the device to be fabricated, subsequently over time the constant contact with the chemical resist will also damage the mask, causing light scattering and a loss of resolution. Proximity lithography in contrast uses a separation between the resist and the mask, however, diffraction can occur between the mask and the resist causing a loss of resolution. However the absence of direct contact with the mask increases the longevity of the mask and reduces the possibility of defects being induced in the resist due to direct contact with the mask. During the fabrication of all devices in this project positive contact lithography was used in all steps, top contact metal applied and device fabrication finished by a lift off process.

2.7.2 Metallization

Metallization of samples is achieved by physical vapour deposition. The most commonly used methods of metallization make use of e-beam deposition illustrated in figure 2.23 or thermal evaporation. These deposition techniques typically occur under a vacuum of ca. 10^{-6} mbar. Vacuum is necessary to strike the tungsten filament in the electron beam and induce deposition of the metal. A low vacuum level is vital to increase the mean free path of the evaporated metal. The target material is heated and evaporated using a high energy electron beam. Electrons are generated by passing a current (~ 5 A) through a tungsten filament, and accelerated towards the source through 270° . Magnets in the apparatus guide the beam of electrons on a path to impact and heat the metal which is contained in a liner which itself is in a crucible. The crucibles are water cooled to minimise contamination from the crucible material evaporating. Deposition of the metal is controlled by the use of a feedback loop between a pair of shutters and a piezo crystal. When the metal reaches the desired deposition rate as a function of electron beam energy the bottom shutter will be removed from over the crucible being heated which allows the metal to deposit on the samples clipped to a rotating stage at the top of the apparatus. A crystal sensor measures the amount of metal evaporated and stops deposition when the desired thickness has been reached by closing the top shutter. To ensure uniform coating and a good adhesion between the films an adhesion layer of 70nm thick nickel is deposited on the devices first to ensure any atmospheric moisture will not interfere with the Au electrode deposition.

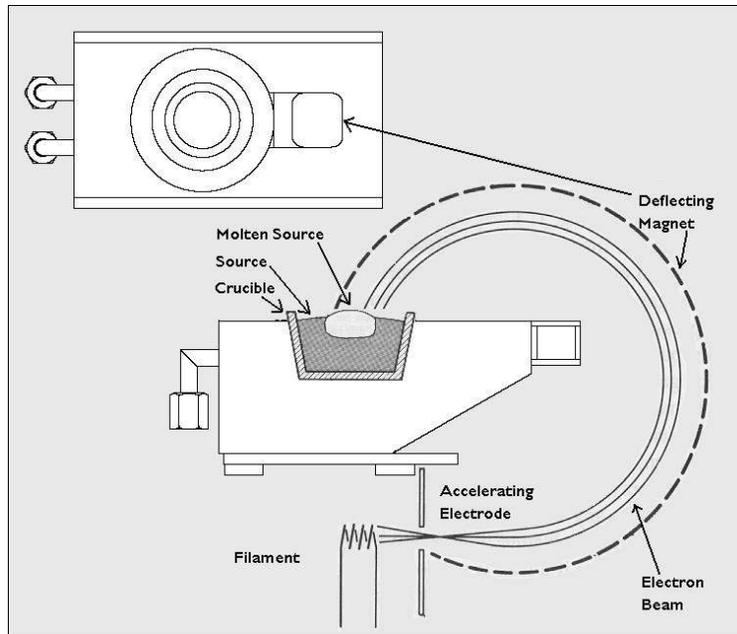


Fig. 2.23: Schematic diagram of e-beam deposition showing the generation of electrons which are accelerated towards the source material using high voltage and a system of electro magnets¹²⁸

A Thermal evaporation apparatus works on the same principle as the above e-beam but evaporation is induced using a resistive tungsten or tantalum sheet around a crucible to stimulate evaporation of an ingot of material rather than a beam of high energy electrons. This process may be initiated at higher chamber pressures and also makes use of water cooling to ensure only the target material is deposited. Several styles of “boat” for deposition are available to maximise creation of vapour species at lower voltages including larger cells which surround the sample. Because the whole cell is hot, the evaporant gases can follow an indirect route to an exit aperture without condensing, with no direct line of sight between source material and substrate and allow thermal deposition to be achieved not just vertically but also horizontally if desired.

2.7.3 Electrical characterisation

Electrical characterisation was performed on all samples, surface pre-treated samples with single oxide layers and bilayer device structures, deposited on GaAs, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and InP. Following deposition of the oxide layers, MOS structures were completed by vacuum evaporation of 70nm Ni and 90nm Au and employing a lift-off process to define MOS capacitors of various areas.

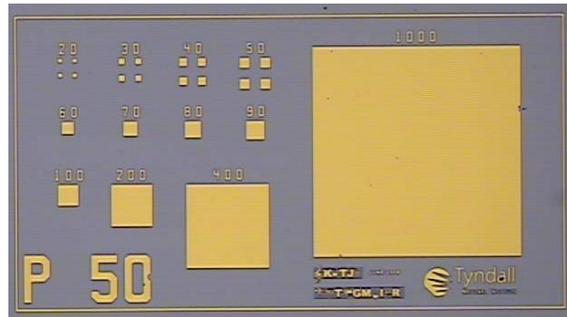


Fig. 2.24: An optical microscope view of finished capacitor devices with test sites ranging in area from $20 \times 20 \mu\text{m}$ to $1000 \times 1000 \mu\text{m}$

The dimensions of the resulting capacitor structures ranged from $20 \times 20 \mu\text{m}$ to $1000 \times 1000 \mu\text{m}$, typical measurements are performed on $50 \times 50 \mu\text{m}$ devices (illustrated in figure 2.23), with low frequency measurements made on larger $100 \times 100 \mu\text{m}$ sites to reduce noise. Capacitance versus gate voltage (C-V) and leakage current versus gate voltage (I-V) measurements were performed to determine the dielectric properties of the layers. For all measurements, the sample was positioned on the chuck which was maintained at room temperature. Metal back contacts were not deposited on the samples as the semiconductor substrates are highly doped ($\sim 10^{18} \text{cm}^{-3}$). The MOS back contact was made through the chuck and bias applied to the chuck to reduce noise and parasitic leakage pathways and a probe needle was used to contact the top gate. Open circuit calibrations were performed prior to CV

measurement to remove any parasitic capacitances from interconnect cables and adaptors and a switch matrix if used.

Initially leakage current tests were performed on multiple sites of varying areas to check the quality of the dielectric and to ensure that leakage current density scales with area. Leakage current is measured at reverse bias. These I-V tests also served to indicate an appropriate bias range which may be applied for subsequent C-V measurements without inducing undue stress on measured devices. C-V measurements were performed on multiple sites across the sample to ensure that the capacitance results were representative, reproducible, and to rule out peripheral inversion charge caused by device processing.

Multi-frequency C-V responses were measured over a frequency range from 1 kHz to 1 MHz with measurement frequencies consisting of 1 kHz, 1 kHz, 2 kHz, 4 kHz, 6 kHz, 8 kHz, 10 kHz, 20 kHz, 30 kHz, 40 kHz, 50 kHz, 60 kHz, 80 kHz, 100 kHz, 200 kHz, 400 kHz, 500 kHz, 600 kHz, 800 kHz and 1 MHz. Lower frequency measurements from 20Hz to 2MHz for bilayer *p*-type samples to observe a full inversion response where appropriate consisted of measurement frequencies 20Hz, 40 Hz, 60 Hz, 80 Hz, 100 Hz, 125 Hz, 150 Hz, 200 Hz, 250 Hz, 300 Hz, 400 Hz, 500 Hz, 600 Hz, 700 Hz, 800 Hz, 900 Hz, 1 kHz, 2 kHz, 3 kHz, 4 kHz, 6 kHz, 8 kHz, 10 kHz, 20 kHz, 40 kHz, , 60 kHz, 80 kHz, 100 kHz, 150 kHz, 200 kHz, 400 kHz, 600 kHz, 1 MHz, 1.5MHz and 2MHz, unless otherwise stated. Temperature measurements were carried out from -50°C to 120°C. All basic measurements were recorded using Agilent E4980A and Agilent B1500A meters in conjunction with a Cascade Microtech, model Summit 12971B probe station, in dry air, under no illumination. Extraction of midgap D_{it} for bilayer samples was conducted for samples under reduced temperatures as prolonged exposure to ambient conditions resulted in degraded C-V characteristics. Multi-temperature, multi-frequency measurements were conducted at room temperature for degraded bilayer

samples and C-V, G-V characteristics plotted to determine the temperature at which degraded samples correspond most closely to initial electrical characteristics to determine the reduced temperature these D_{it} measurements should be acquired at. It should also be noted that all CV measurements presented in this study are plotted as a function of device area, i.e. in units of F/m^2 and leakage current densities in F/cm^2 .

2.8 Transmission electron microscopy

Transmission electron microscopy is a technique analogous to using a light microscope, instead of using photons and glass filters to focus light a TEM makes use of an electron beam focused with electromagnetic lenses to irradiate a sample and resolve features down to $\sim 0.2\text{nm}$. This resolution is possible using TEM by making use of high energy electrons which have a small wavelength. The TEM system is divided into stages (Fig. 2.24), the electron source and initial lenses which focus the beam of electrons, further lenses which guide the beam of electrons to interact with the sample under investigation and thirdly several subsequent lenses which magnify the image and focus the beam onto a detector or CCD. The entire system is kept under vacuum to allow sufficient penetration of electrons along the length of the instrument and prevent oxidation of the filament. A current is passed through the tungsten filament, which heats up and releases electrons by thermionic emission. These electrons are then accelerated using a series of potentials applied to electrodes so as to form the electron beam. Condenser lenses are used to produce a beam of electrons of desired diameter. Images formed rely on the scattering of electrons as they pass through a thinned sample and are scattered by Rutherford scattering, this scattering is linked to the atomic number of the elements and the thickness of the sample. Larger atomic number elements having the potential to scatter more electrons as the likelihood of an electron scattering due to an interaction with an atom increases with the number of charges that the atom carries, and a thicker sample increasing the likelihood of a scattering event taking place. Thus larger atomic

number elements appearing darker in the TEM and lower atomic number elements appearing brighter. This effect is noticeable in Fig. 1.2 where the silicon substrate appears quite bright, SiGe source and drains are darker and high- κ oxides are clearly observable due to the HfO_2 .

The imaging system uses several

lenses to magnify the image and to focus the image these on the viewing screen or computer display via a detector. The diffraction lens is used when a diffraction pattern from a specific region of a sample is desired

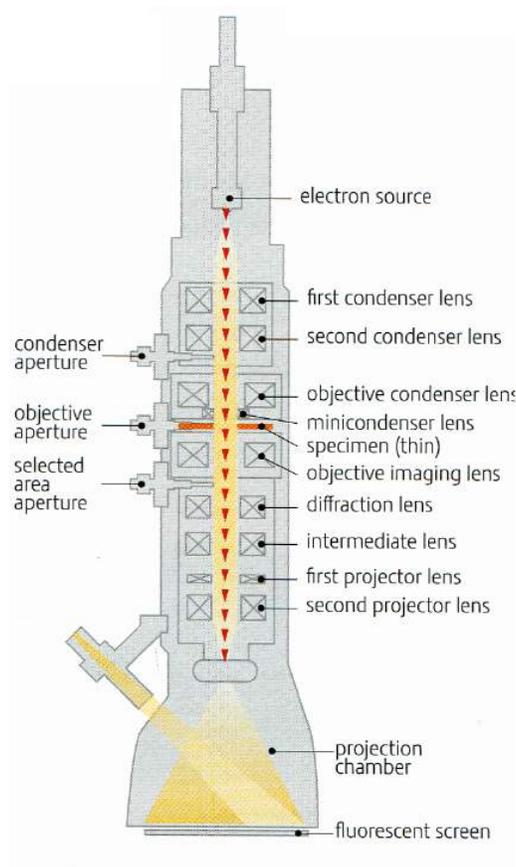


Fig. 2.25: A schematic of a transmission electron microscope¹²⁹

2.8.1 Focused ion beam milling

Focused ion milling is a technique used to thin samples down to allow electrons to pass through the sample. Typically the sample under investigation must be thinned to a maximum

thickness of 1 μm . Focused ion beam milling is used to extract a thin slice from a specific area of interest in the sample. Typical operating voltages are between 1.5 and 30 kV while milling a sample¹³⁰. To extract a lamella from the sample, it first is covered with a Pt film to protect the area of interest during the thinning process. Then a trench is milled either side of the lamella of interest and widened sufficiently to allow milling almost all around the sample. A micromanipulator is welded to the lamella of interest and the sample finally completely milled from the bulk and once extracted it is transferred to a carbon coated mesh for inspection. The main disadvantage of FIB is the possible amorphization and phase transitions which may take place dependant on the beam energy used to mill the sample

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Chapter 3: Electrical characteristics of capacitors fabricated from an amidinate precursor

Introduction

All work in this section was completed as a collaboration with Agnes Kurek of Carleton University, who carried out the ALD growth of aluminium oxide films with the electrical analysis and ellipsometry provided by the author.

Aluminium oxide films are employed in microelectronics as high- κ dielectrics (~ 8) and interface control layers (ICLs) between higher κ materials (for example, HfO_2) and III/V substrates where the native oxides of the semiconductor are unstable and give rise to high levels of electrical defects¹. Alkylaluminium compounds are generally used as precursors for ALD of aluminium oxide and are considered an “ideal ALD process”²; however these present challenges such as being pyrophoric in nature, which prohibits storage of large quantities. Aluminium amidinates are good substitutes to these precursors. The volatility of these amidinates may be tuned based on substituent groups, are non-pyrophoric yet react readily with water and are thermally stable. Recent efforts have revealed several amidinate and guanidinate compounds as potential vapour deposition precursors of copper³, silver⁴, gold⁵, titanium oxide⁶ and iridium oxide⁷. During the study detailed within this chapter, a growth

study for this new precursor was performed (Fig. 3.1); thin films of aluminium oxide were subsequently deposited and structurally and electrically characterized to determine the suitability of the precursor to deposit interlayers of aluminium oxide.

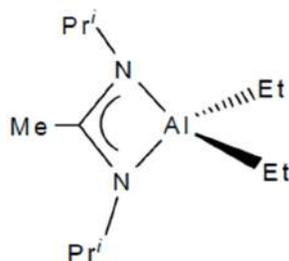


Fig. 3.1: The aluminium amidinate precursor under investigation in this work.

3.1 Experimental methodology

ALD depositions utilised a direct draw commercial reactor Cambridge NanoTech Fiji F200LLC System. High purity argon gas is continually passed through the flow tube as purge gasses at a flow rate of 40sccm and a reactor base pressure of 0.04 torr, with an operating pressure of 0.33 torr. ALD of Al_2O_3 was achieved by alternating exposures of the experimental precursor and H_2O . The precursor is held in a bubbler, maintained at 50°C with delivery tubing and ALD valves maintained at 150°C to prevent condensation during transportation, H_2O is used at room temperature with a fixed pulse time of 1s. Typical purge length for all cycles was maintained at 15s. ALD Al_2O_3 films for the initial growth study were deposited on p -Si (100). Once growth characteristics had been ascertained a brief study was performed on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ to determine the electrical characteristics of deposited Al_2O_3 layers. No growth study was performed on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ prior to deposition of aluminium oxide.

All $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ epitaxial layers used in this work were either $\sim 2 \mu\text{m}$ thick n -type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channels (doping S: $\sim 4 \times 10^{17} \text{ cm}^{-3}$) with a $\sim 0.1 \mu\text{m}$ InP buffer layer (doping S:

$\sim 4.2 \times 10^{18} \text{ cm}^{-3}$) grown by MOVPE on a 350 μm InP substrate (doping S: $3\text{-}8 \times 10^{18}$) or ~ 2 μm thick *p*-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channels (doping S: $\sim 4 \times 10^{17} \text{ cm}^{-3}$) with a ~ 0.1 μm InP buffer layer (doping Zn: $\sim 4.2 \times 10^{18}$) on a 350 μm InP substrate: doping (Zn $3\text{-}8 \times 10^{18}$). An *ex-situ* $(\text{NH}_4)_2\text{S}$ surface passivation (10%, 20 min at 25°C, rinsed in de-ionized water, dried in nitrogen) was performed on half of the III-V substrates before deposition of Al_2O_3 , with a transfer time of 5 min recorded. These passivation parameters were determined from previous physical and electrical studies^{8,9}.

Film thickness was determined with the use of a J. A. Woollam ESM-300 wide angle ellipsometer. To correct for native oxides present on Si wafers a 4in. wafer was mapped using ellipsometry and the average cross wafer thickness of the native oxide assumed for all measurements (1.68 nm). Once ALD regime growth on Si substrates was confirmed, deposition was carried out on III-V substrates, subsequently electrical capacitors were fabricated on III-V samples by lithographically defining device areas and using thermal evaporation of 50nm Ni as an adhesion layer and 70nm Au to form gate electrodes of area $2.5 \times 10^{-9} \text{ m}^2$. Devices were analysed as standard using a Cascade Microtech summit model 12971B, used with the Agilent B1500 CV enabled device analyser. Varied growth parameters are described below:

Pulse time: 0.1, 0.5, 1, 1.5, 2, 3, 4, 6s (constant temperature and no. of cycles) Fig. 3.2

GPC: 50, 80, 100, 150, 200, 250 cycles (constant pulse time and temperature) Fig. 3.3

Temperature: 175, 200 and 300°C (constant pulse time and no. of cycles) Fig. 3.4

Substrate	Pre-treatment	Temperature °C	No. cycles Al ₂ O ₃
n/p InGaAs	None	250	80
n/p InGaAs	Ex-situ (NH ₄) ₂ S	250	80
n/p InGaAs	None	300	80
n/p InGaAs	Ex-situ (NH ₄) ₂ S	300	80

Table 3.1: A Table detailing the sample set electrically investigated in this work

3.2 Growth study of Al₂O₃ on Si substrates

Initial growth studies using the experimental precursor were carried out on Si substrates. Figure 3.2 shows thickness of Al₂O₃ (nm) layers deposited with increasing amidinate pulse duration at 250°C for 100 cycles on (100) *p*-Si. A steep increase in growth is noted until exposure times of ~1s and continues to rise for further pulse times. No increase in purge times was allowed for larger exposures and no self-limiting regime was observed, this manifests itself in Fig 3.2 as an increasing growth rate with pulse duration i.e.: a switch to a CVD regime with some gas phase reactions taking place. It is not decomposition of precursor as it remains stable at the deposition temperature (250°C); this is evidenced in later results where we present a linear increase in film thickness with no. of cycles for a fixed pulse duration at 250°C.

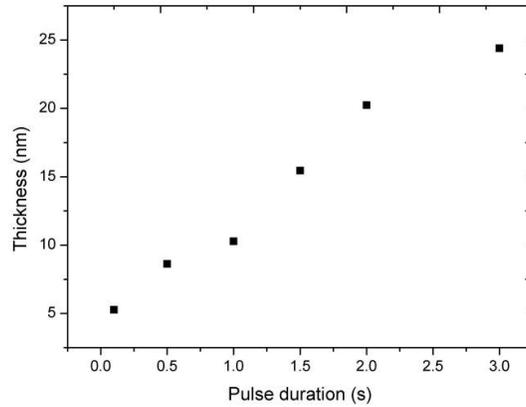


Fig. 3.2: Al₂O₃ film thickness vs. Al pulse exposure time for 100 cycles grown on Si (100) at 250°C, measured using ellipsometry.

Figure 3.3 shows the film thickness vs. the number of cycles, with a fixed amidinate precursor pulse time of 1s at a temperature of 250°C with the number of cycles varied from 50-250. Al₂O₃ films are found to exhibit a linear growth rate with a standard error in ellipsometry measurements of +/-0.02nm and an average growth rate of 1.04 Å per cycle. This consistent linear increase in film thickness with increasing number of cycles affirms that the growth takes place in an ALD regime

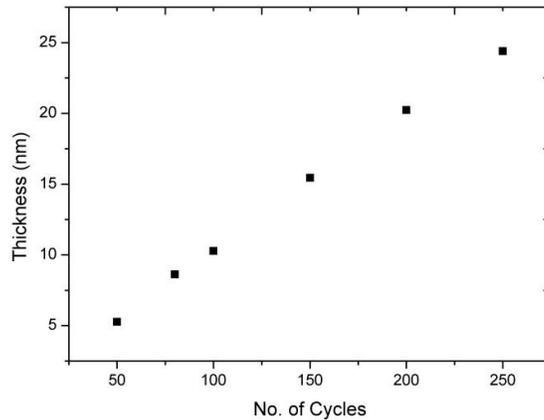


Fig. 3.3: Al₂O₃ film thickness at 250°C on Si (100) vs. no. of ALD cycles with a pulse duration of 1s measured using ellipsometry with an average growth rate of 1.04Å per cycle.

Figure 3.4 shows the growth per cycle (GPC) vs. ALD chamber temperature, with a fixed amidinate precursor pulse time of 1s for 100 cycles. There is an ALD temperature window where GPC for the compound is stable and exhibits a constant, self-limiting deposition rate; within experimental error. GPC values were 1.02Å at 175°C, 1.03Å at 250°C and 1.08 Å at 300°C, analogous values to that of 1-1.1Å per cycle observed for ALD deposition of TMA and water at similar temperatures by *Puurunen et al.*² and *Ott et al.*¹⁰

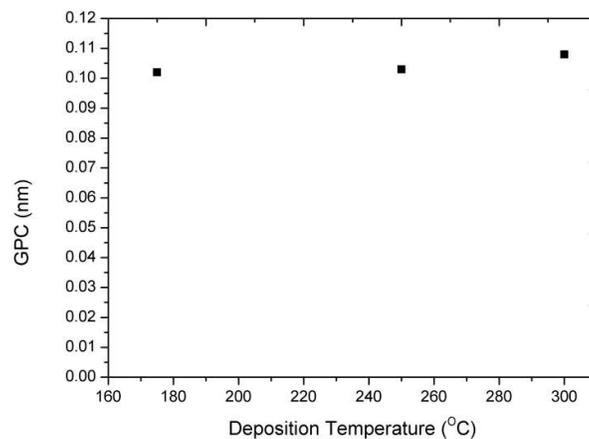


Fig. 3.4: Al₂O₃ growth per cycle at 250°C on Si (100) vs. temperature with a pulse duration of 1s and 100 cycles of deposition, measured using ellipsometry.

3.3 Characterization of Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOS

3.3.1 TEM

Figures 3.5 and 3.6 show cross sectional TEM of In_{0.53}Ga_{0.47}As samples with Al₂O₃ layers grown under equivalent conditions at 250°C and 300°C. In both cases sample B has received an ammonium sulphide etch as described earlier. Samples have either a tungsten layer or a SiO₂ layer deposited on top to enhance contrast. TEM reveals an Al₂O₃ layer thickness of 5nm for substrates which have received an ammonium sulphide etch and 2nm for those which had not. It was observed that all deposition on III-V materials is substrate inhibited; as

deposition of 80 cycles of aluminium amidinate and water with a growth rate of 1.03\AA - 1.08\AA per cycle would be expected to furnish a layer of nominal 8nm thickness. The precursor is most likely type I inhibited as type II inhibition has been associated with island formation and films^{11,12} though thin appear coalesced, leading to the conclusion that the initial GPC is quite low and will rise to a constant GPC. This behaviour was consistent across samples grown at both temperatures on both dopant types; all oxide layers were diminished in thickness with etched samples exhibiting a shorter nucleation delay. The removal of native oxides and the creation of an S- terminated surface facilitates deposition using the adiminate precursor.

This is also related to the transfer time for each sample as it has previously been shown that prompt transfer to the ALD chamber is vital to ensure the surface remains S- passivated¹⁴ and homebuilt systems take a considerable amount of time to reach a good quality vacuum. Evident in cross sections in fig.3.5 and 3.6, a bright layer can be observed between the Al_2O_3 layer and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrate, this has previously been attributed to the presence of native oxides¹⁵ which are not completely removed.

This suggests that removal of native oxides present on the surface of the semiconductor is necessary to ensure growth of an Al_2O_3 film using this precursor, generally at the deposition temperatures used in this study the surface oxides are composed of a mix of As_2O_3 and As_2O_5 making up over half of all the oxides, with oxygen transfer from indium oxides to gallium oxides with increasing temperature with approximately stoichiometric amounts of In and Ga oxides at 300°C ¹³. Typically in the TMA process at 300°C cleanup reactions will remove the +3 As oxides and +5 As oxides and AsO_x are volatile at the deposition temperature leading to an improved interface.

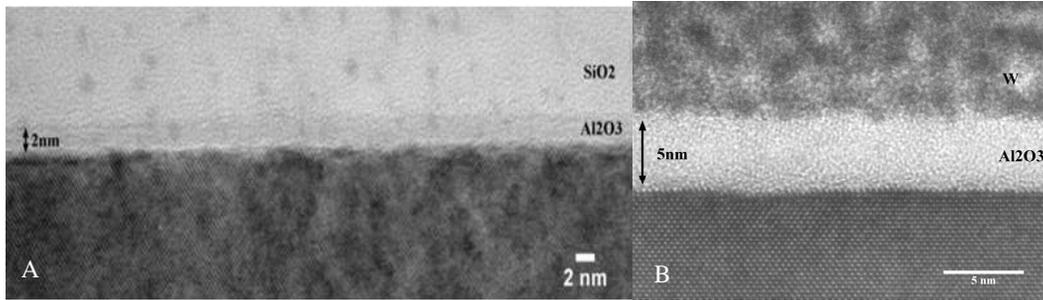


Fig. 3.5: Cross sectional TEM of Al_2O_3 growth at 250°C on A) untreated sample with a measured Al_2O_3 thickness of 2nm with SiO_2 deposited on top for contrast B) pre-treated sample with a measured Al_2O_3 thickness of 5nm with tungsten deposited on top for contrast

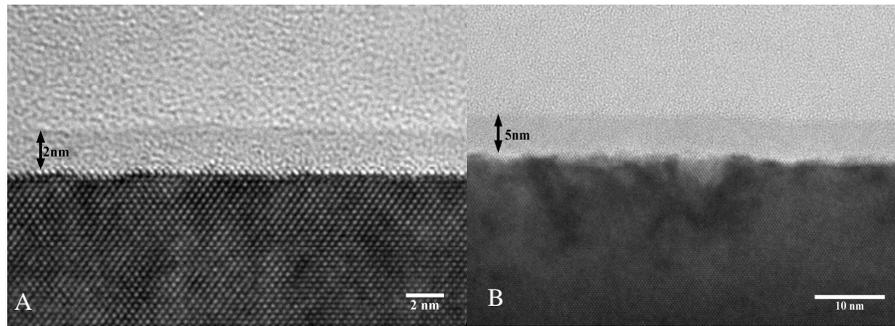


Fig. 3.6: Cross sectional TEM of Al_2O_3 growth at 300°C on A) untreated sample with a measured Al_2O_3 thickness of 2nm and B) pre-treated sample with a measured Al_2O_3 thickness of 5nm

3.3.2 Electrical characterization of n and p -Au/Ni/ Al_2O_3 / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ Capacitors

Figure 3.7 shows the leakage current density characteristics of p -type capacitors, with oxide layers grown at 250°C shown in black and red, while those grown at 300°C are shown in blue and green. Lower leakage current density is observed for samples which receive an ammonium sulphide etch, this correlates with the structural TEM data well, as a physically thicker oxide layer should have a lower leakage current density at the same applied voltage. Deposition onto untreated samples results in an aluminium oxide layer not sufficiently thick to function as an insulating layer, hence the large leakage current of all measured devices is

large and observed to saturate quickly. *p*-type samples grown at 300°C after a surface pre-treatment display increased leakage current density compared to samples grown at 250°C after the same surface treatment, the variance in leakage current density with deposition temperature may be due to the presence of a native oxide interlayer. The growth temperature also effects the quality of the dielectric as samples grown at 300°C have worse leakage current density. All samples display large leakage current however - an indication that the deposited dielectric is of poor quality regardless of deposition temperature. No C-V curves are presented for these samples as the leaky dielectric is not suitable for measuring capacitance characteristics of formed devices.

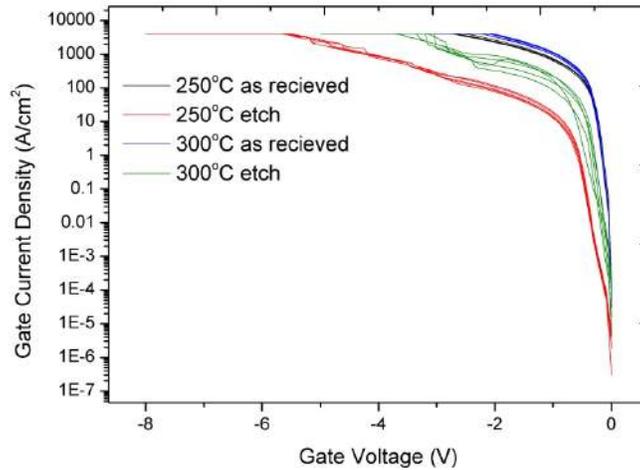


Fig. 3.7: Leakage current characteristics for 20 measured *p*-type capacitors with Al₂O₃ oxide layers grown at 250 °C without a surface treatment displayed in black, grown at 250 °C with a surface treatment displayed in red, grown at 300 °C without a surface treatment displayed in blue and grown at 300 °C with a surface treatment displayed in green.

Figure 3.8 shows the leakage characteristics for *n*-type capacitors, with oxide layers grown at 250 °C shown in black and red, oxide grown at 300 °C is shown in blue and green. Again substrates treated with the ex-situ etch have a thicker Al₂O₃ layer and a reduced leakage current density as a result. Oxide layers measured as 2nm thick again do not function as an

insulating layer leading to very large leakage of measured devices which quickly saturates. Mirroring *p*-type results Al₂O₃ films grown at 300°C generally display increased leakage current density compared to samples grown at 250°C a possible indication that 300°C is not a suitable temperature to grow this dielectric by ALD with this precursor. A further cause of these variations in leakage density may also be the presence of roughened surfaces across the wafer. These surfaces can lead to a localised increase in electric field which would result in increased leakage current for any devices measured and would account for some of the cross wafer variance seen. Finally it is worth noting that no C-V characteristics are presented for these samples. The large leakage current indicates that the dielectric deposited is of poor quality, does not hold charge and would not be suitable for C-V analysis.

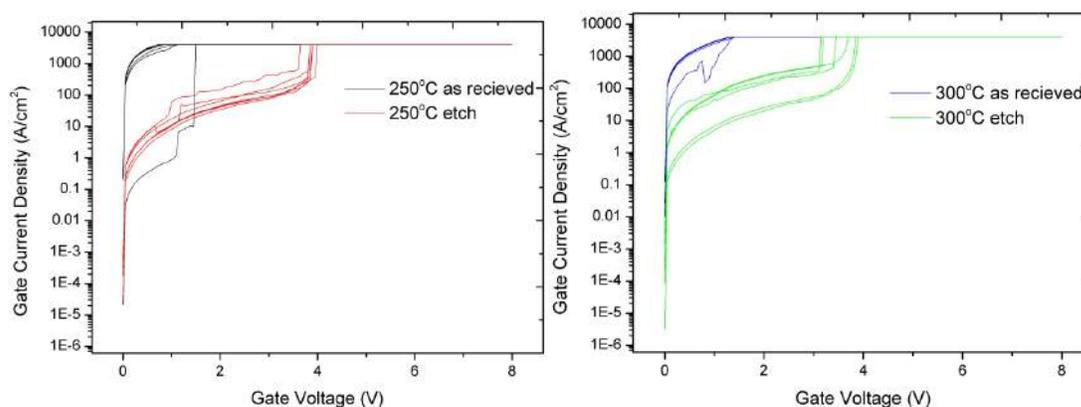


Fig. 3.8: Leakage current characteristics for 20 measured *n*-type capacitors with Al₂O₃ oxide layers grown at 250 °C without a surface treatment displayed in black, grown at 250 °C with a surface treatment displayed in red, grown at 300 °C without a surface treatment displayed in blue and grown at 300 °C with a surface treatment displayed in green.

3.4 Conclusions:

A new precursor is presented for the deposition of Al₂O₃ which has been shown to have an ALD window and linear growth rate on Silicon substrates. ALD growth on III-V native

oxides presents a large nucleation delay. Differences in leakage current density at equivalent voltages were observed between Al_2O_3 layers grown at 250°C and 300°C and we speculate it is due to changes in film density due to process temperature. TEM indicates the presence of native oxide layers between the semiconductor and the high- κ , this interlayer of native oxides will have detrimental effects on the leakage current densities of dielectric films. The large leakage current of all measured devices suggests that the dielectric deposited on III-V substrates is of poor quality.

The use of a previously examined ammonium-sulphide etch to remove native oxides and leave a $-\text{S}$ terminated surface gives a much reduced nucleation delay. Such nucleation delays are not reported for the deposition of Al_2O_3 from TMA and water, due to the well documented “clean-up” reactions of trivalent TMA with III-V native oxides¹⁵⁻¹⁷ which do not appear to take place using this amidinate precursor. Additionally the TMA and water process at 300°C generally results in a better dielectric. Further work should incorporate an etch step to remove III-V native oxides prior to deposition allowing the full growth rate of the precursor to be accessed on III-V materials. Thicker Al_2O_3 films should also be grown to allow full electrical characterization and comparison to the standard TMA/ H_2O process.

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Chapter 4: Precursor dependant self-cleaning investigations

Introduction

The self-cleaning phenomenon has been observed many times when TMA is used as a precursor for Al₂O₃ deposition on III-V materials, removing native oxides in the +3 oxidation state. This reaction has been observed chiefly on GaAs¹ and InGaAs² with some reports of self-cleaning on other substrates such as InSb³ and InAs⁴. This process has also been observed for other precursors, namely tetrakisdimethylamino-hafnium (TDMAH⁵), tetrakisdimethylamino-titanium (TDMAT⁶) and tetrakisethylmethylamino-hafnium (TEMAH⁷), indicating that oxidation state may not dictate the capacity to remove native oxides from the semiconductor surface. In this work precursors analogous to TMA are investigated for potential native oxide removal, triethyl Gallium (TEG) and trimethyl Indium (TMI) are pre-pulsed onto GaAs, In_{0.53}Ga_{0.47}As and InP substrates respectively before deposition of Al₂O₃ from TMA and water and subsequent formation of MOSCAP structures. C-V and I-V measurements were performed to investigate if treatments yield an improved III-V/high-κ interface.

4.1 Experimental methodology

All In_{0.53}Ga_{0.47}As epitaxial layers used in this work are the same as chapter 3. All GaAs (100) wafers used were either *n*-type wafers (Si doping: ~ (1-5) x 10¹⁸) or *p*-type (doping Zn: ~ 4.2 x 10¹⁸). All InP (100) wafers used were either *n*-type wafers (S doping: ~ (3-20) x 10¹⁸) or *p*-type (doping Zn: ~ (1-6) x 10¹⁸)

All depositions were carried out in a homebuilt reactor with a base pressure of 8.0×10^{-3} Torr, precursors were held at room temperature and delivered by a direct draw method. To provide reference samples, both *n*- and *p*- type substrates were used as received with a native oxide layer present and a total of 80 cycles of Al₂O₃ were deposited from TMA and water as precursors at room temperature and a chamber temperature of 300°C with 10ms pulse times and 190s purge time respectively for each precursor utilising a TMA pulse first. Samples which received a pre-pulse treatment were placed in the reactor at 300°C and exposed to either 20 pulses of TEG with a pulse duration of 100ms or 20 pulses of TMI with a 200ms pulse duration, after which the chamber was allowed to evacuate and 80 cycles of Al₂O₃ were deposited as per the reference samples.

Electrical capacitors were fabricated and measured as per chapter 3.

4.2 Gallium Arsenide devices

4.2.1 Structural characteristics of Au/Ni/Al₂O₃/GaAs capacitors

Figure 4.1 a) presents a TEM micrograph of the Au/Ni/ Al₂O₃/GaAs sample. The Al₂O₃ layer has a thickness of ~6 nm. There is a native oxide layer evident beneath the Al₂O₃ layer at the Al₂O₃/GaAs interface ca. 1nm thick indicating incomplete removal of native oxides during Al₂O₃ deposition. Figure 4.1 b) presents a TEM micrograph of the Au/Ni/Al₂O₃/GaAs sample which has received a TEG pre-pulse treatment. The Al₂O₃ layer has a thickness of ca. 6 nm. A diffuse interface is observed between the Al₂O₃/GaAs indicating an incomplete native oxide removal during the deposition of Al₂O₃. The film across the sample measured does not appear to be of uniform thickness, an indication of surface roughness in the sample measured which may cause local increases in leakage current density. This roughness manifests in the large variance in leakage current density and breakdown voltage observed for both *n*- and *p*- type devices measured.

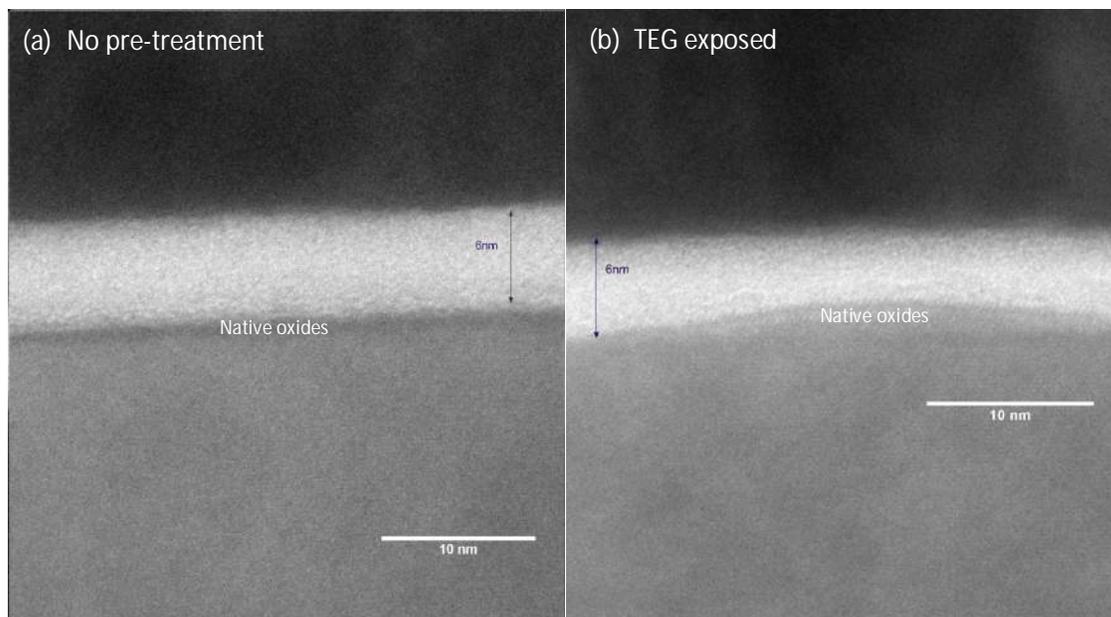


Fig. 4.1: Transmission electron micrographs of Al₂O₃ layers in Al₂O₃/GaAs MOSCAP structures a) displaying an Al₂O₃ film ~6 nm thick on GaAs and b) displaying an Al₂O₃ film ~6 nm thick grown on GaAs after exposure to TEG.

4.2.2 I-V characteristics of *n*- and *p*- Au/Ni/Al₂O₃/GaAs capacitors

Figure 4.2 displays I-V characteristics for the 18 measured *n*-type devices and the 16 measured *p*-Au/Ni/Al₂O₃/GaAs capacitors. All devices were measured as previously described, being reverse biased until a breakdown event. Non-treated *n*-type reference samples exhibit a large variation in leakage current density. This is an indication of cross-wafer dielectric non-uniformity, possibly due to the incomplete surface cleaning of GaAs by TMA leading to the presence of remaining native oxides which can act as leakage pathways and a local variation in dielectric thickness also results in structural induced leakage current. TEG pre-pulsed samples display a generally reduced leakage current density compared to reference samples; however there also exists a large distribution of leakage current densities and breakdown voltages with a breakdown range from 5.83-9.6MV observed, this is a manifestation of structural induced leakage current TEM analysis shows a rough interface

which may also increase the electronic field locally and causing an increase in leakage current. *p*-type samples display a large leakage current, with a leakage density of ca. 10 A/cm² at -1V. There appears to be a minimal influence of the pre-treatment on the I-V characteristics of *p*-type devices, with breakdown behaviour observed at low voltages for samples irrespective of surface pre-treatment. Such variation in breakdown events and large leakage of devices measured over the entire sample would suggest that the dielectric deposited is of poor quality and is the main cause of such high leakage current.

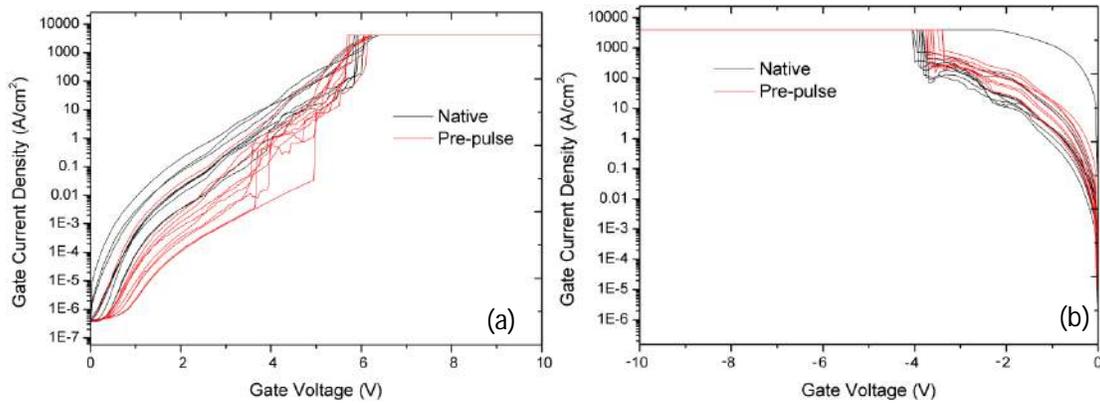


Fig. 4.2: Leakage current density characteristics for a) 18 measured *n*-Au/Ni/Al₂O₃/GaAs devices, with reference devices displayed in black and devices which have received a TEG pre-treatment displayed in red and b) 16 measured *p*- Au/Ni/Al₂O₃/GaAs reference samples displayed in black and samples which have received a TEG pre-treatment displayed in red.

4.2.3 CV characteristics *n*-type Au/Ni/Al₂O₃/GaAs capacitors

Figure 4.3 shows C-V characteristics of *n*-Au/Ni/Al₂O₃/GaAs samples. A large difference in maximum accumulation capacitance is observed between samples which receive a pre-pulse treatment and those which do not. Maximum calculated capacitance, as per the calculations in appendix A, for a structure with 6nm of Al₂O₃ is 0.012 F/m². The theoretical maximum capacitance in accumulation is exceeded for non-treated samples indicating that this is not a true C-V response. Untreated *n*-type Au/Ni/Al₂O₃/GaAs which have Al₂O₃ directly deposited

onto substrates with no pre-treatment these show a very large lateral shift in the C-V without a distortion in shape which has generally been attributed to the presence of un-passivated interface states⁸. Some stretch out is also observed which is due to the presence of interface states⁹. The native sample C-V in figure 4.3 closely resembles the Nicolian and Brews model of a GaAs capacitor with a large density of interface states and previously reported GaAs devices^{8,10,11} however this is due to the large leakage current densities seen in measured samples as the capacitance far exceeds the calculated capacitance and this should not happen for a functioning MOS capacitor and is not related to features seen in other high- κ /III-V systems¹²⁻¹⁴. TEG pre-treated Au/Ni/Al₂O₃/GaAs capacitors display a much reduced dispersion with respect to frequency and a lack of a D_{it} feature at negative voltages, a possible indication of an improved interface with Al₂O₃ after surface pre-treatment and a reduced density of interface states and a reduction in midgap traps. The reduced lateral shift with frequency may also be an indication of an improved interface. The reduced “accumulation” capacitance observed may be an indication of incomplete removal of native oxides during the deposition of Al₂O₃ some of which may remain as evidenced in the I-V characteristics and TEM analysis however no true accumulation behaviour is seen.

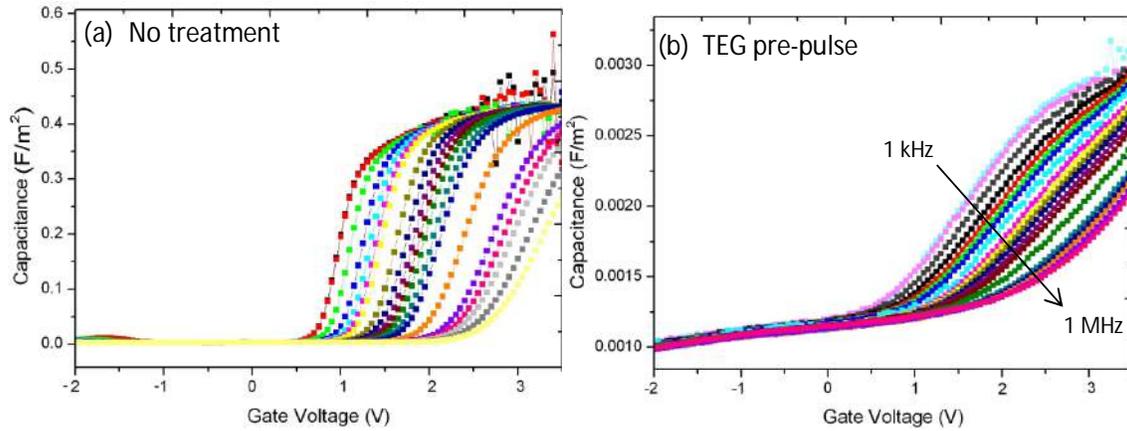


Fig. 4.3: Multi-frequency C-V characteristics of a) Reference n -Au/Ni/Al₂O₃/GaAs capacitor with no surface treatment and b) n -Au/Ni/Al₂O₃/GaAs capacitor which has received a TEG pre-pulse treatment.

Figure 4.4 shows hysteresis curves for n -Au/Ni/Al₂O₃/GaAs samples using a 1 MHz frequency sweep from accumulation to inversion and back again. In the voltage range investigated a lack of hysteresis is observed in untreated n -Au/Ni/Al₂O₃/GaAs capacitors however it should be noted that the entire C-V response is pushed out of the voltage range investigated and the scale is different to TEG treated samples which may obscure small amounts of hysteresis present. In contrast TEG pre-pulsed Au/Ni/Al₂O₃/GaAs capacitors display some hysteresis, which is indicative of the presence of border traps in the oxide¹⁴, the most important of which is the formation of the oxygen vacancy in the high- κ oxide layer, as postulated for both Al₂O₃ and HfO₂¹⁵⁻¹⁸

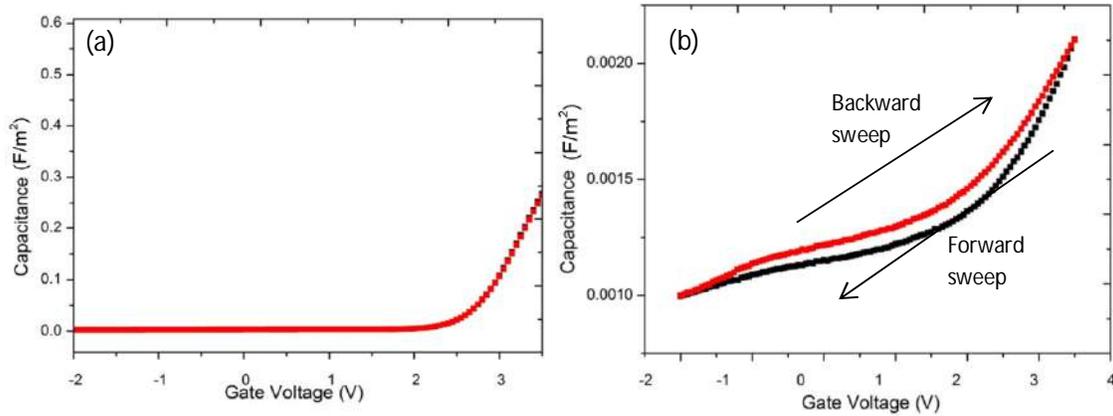


Fig. 4.4: 1MHz hysteresis sweeps with sweeps from accumulation to inversion in black and the corresponding inversion to accumulation sweep in red for a) native oxide reference sample and b) the sample which received an in-situ TEG treatment.

4.3 Indium Gallium Arsenide devices

4.3.1 Structural characteristics of Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As capacitors

Figure 4.5 displays TEM micrographs of Al₂O₃ layers under investigation. Both deposited oxide layers are noted to be amorphous and exhibit an abrupt interface between the Al₂O₃/In_{0.53}Ga_{0.47}As. The abruptness of the interface with the substrate coupled with no observable native oxides is an indication of the self-cleaning mechanism occurring during the deposition of Al₂O₃ interface control layers from TMA⁸. Measured oxide layer thickness for samples which receive no pre-treatment was 5nm Al₂O₃, samples which are exposed to TEG prior to the deposition of Al₂O₃ have a dielectric thickness of 6nm. The observed diffuse interface in fig. 4.5 (b) is a consequence of TEG pre-pulsing, indicating that some deposition of gallium oxides must take place during the treatment as TMA treatment alone is sufficient to remove enough native oxide to form an abrupt interface in reference samples. These gallium oxides would be difficult to resolve in TEM images as Ga has a similar scattering cross section to that of Al leading to confusion of the contribution of each component to the measured dielectric thickness.

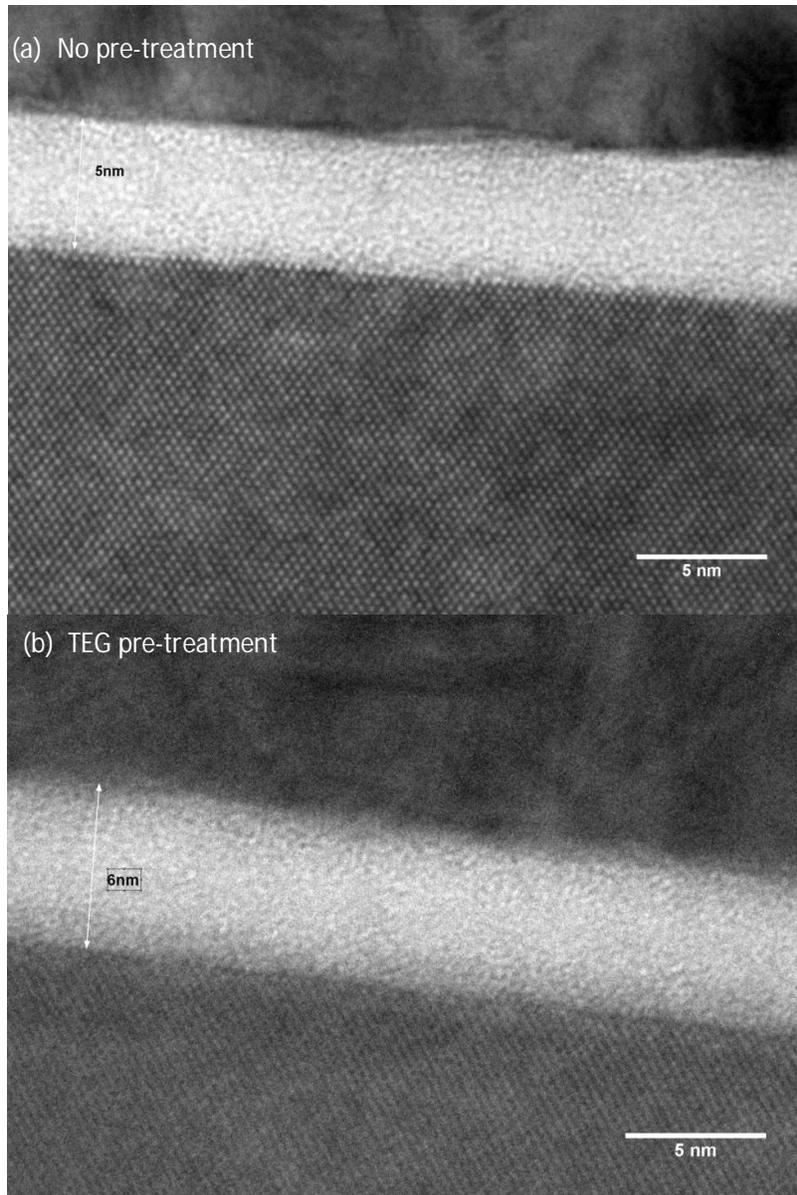


Fig. 4.5: Transmission electron micrographs of Al_2O_3 layers in $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSCAP structures a) displaying an Al_2O_3 film ~5 nm thick on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and b) displaying an Al_2O_3 film ~6 nm thick on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrate grown after exposure to TEG.

4.3.2 I-V characteristics of n- $\text{Au}/\text{Ni}/\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ capacitors

Figure 4.6 displays leakage current densities for all types of *n*- and *p*- samples. *n*-type $\text{Au}/\text{Ni}/\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ capacitors have two different leakage current density regimes

clearly observable. Breakdown voltage ranges from 5.8-10.2MV for reference samples with 5nm of dielectric and 6.5-7.3MV for TEG treated samples with 6nm of measured dielectric. Samples which receive no TEG pre-pulsing clearly exhibit a leakage current density ca. three orders of magnitude smaller at 2V than samples exposed to the pre-pulsing treatment with higher breakdown voltages observed overall for untreated samples. *p*-type Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As capacitors exhibit a similar trend, samples which receive no TEG pre-pulsing clearly exhibiting lower leakage density over the entire voltage range investigated with samples which receive the a TEG pre-treatment exhibiting leakage current densities ca. three orders of magnitude larger at the same voltages. This is attributable to growth of some Ga oxides during TEG pre-treatment, which are generally leaky and unstable resulting in the observed dielectric behaviour.

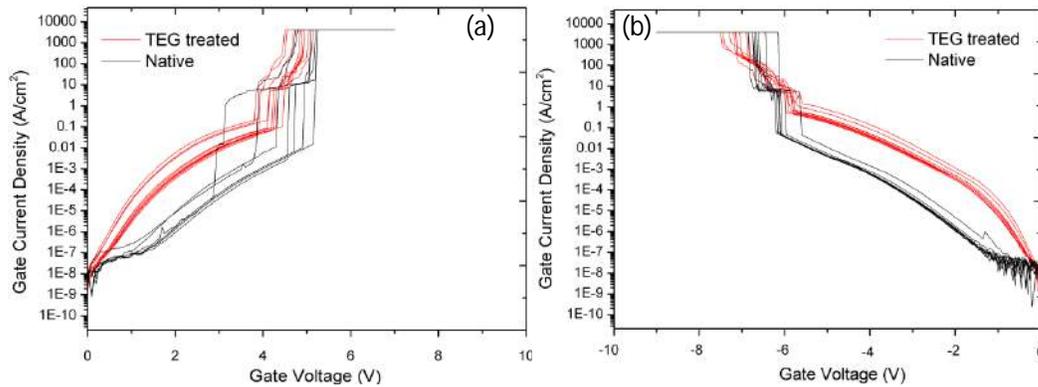


Fig. 4.6: Leakage current density characteristics of a)18 *n*-type Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As devices, reference samples are displayed in black and those which have received a TEG pre-treatment are displayed in red, and b)18 *p*-type Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As, reference devices measured are displayed in black and those which have received a TEG pre-treatment displayed in red

4.3.3 C-V characteristics of *n*- Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As capacitors

Figure 4.7 displays the C-V characteristics of *n*-Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks with and without a TEG surface treatment. Comparison of maximum accumulation capacitance achieved for both samples indicates that capacitors which receive a TEG pre-pulse treatment reach a capacitance roughly half that of samples which receive no treatment, an accumulation capacitance of 0.0036 F/m² is observed for TEG treated samples compared to the ideal calculated oxide capacitance for a 6nm Al₂O₃ film of 0.0127 F/m² as calculated per appendix A. Such a difference between the calculated oxide capacitance and the observed oxide capacitance may be accounted for if the extra 1nm thickness of the dielectric treated by TEG is a 1nm layer of Ga oxides with a low κ value. To achieve a capacitance in the accumulation region of the C-V with a value similar to that observed in figure 4.7 c the κ value of a 1nm Ga oxide layer would have to be ca. 2-3. The other way to account for this lower C_{max} is with a larger dielectric thickness, to achieve a C_{max} similar to that in C-V curves presented in figure 4.7 c the Al₂O₃ layer would have to be 12 nm thick.

Both samples measured display some dispersion in accumulation, which may be attributed to the presence of border traps present in the oxide¹²⁻¹⁴. The observed variance between initial 1 kHz sweep and the second 1 kHz sweep on the native oxide sample which is an indication of charge being trapped in deep traps, this is also present in the treated sample but obscured by subsequent frequencies in the C-V, 1kHz sweeps are presented in figure 4.8 to illustrate the difference between 1kHz sweeps. Both samples display a response at negative bias, which has been attributed to the capture and emission of minority carriers at near midgap interface defects¹⁹ and is characteristic of C-V characteristics observed for the high- κ /III-V system²⁰⁻²⁵. A large interface defect response is observed for samples which receive TEG pre-pulse treatment, with capacitance seen to go through a peak and decline again, in contrast a

continually increasing capacitance in inversion at low frequency for reference samples is observed, which may be indicative of trap states deep in the bandgap²¹.

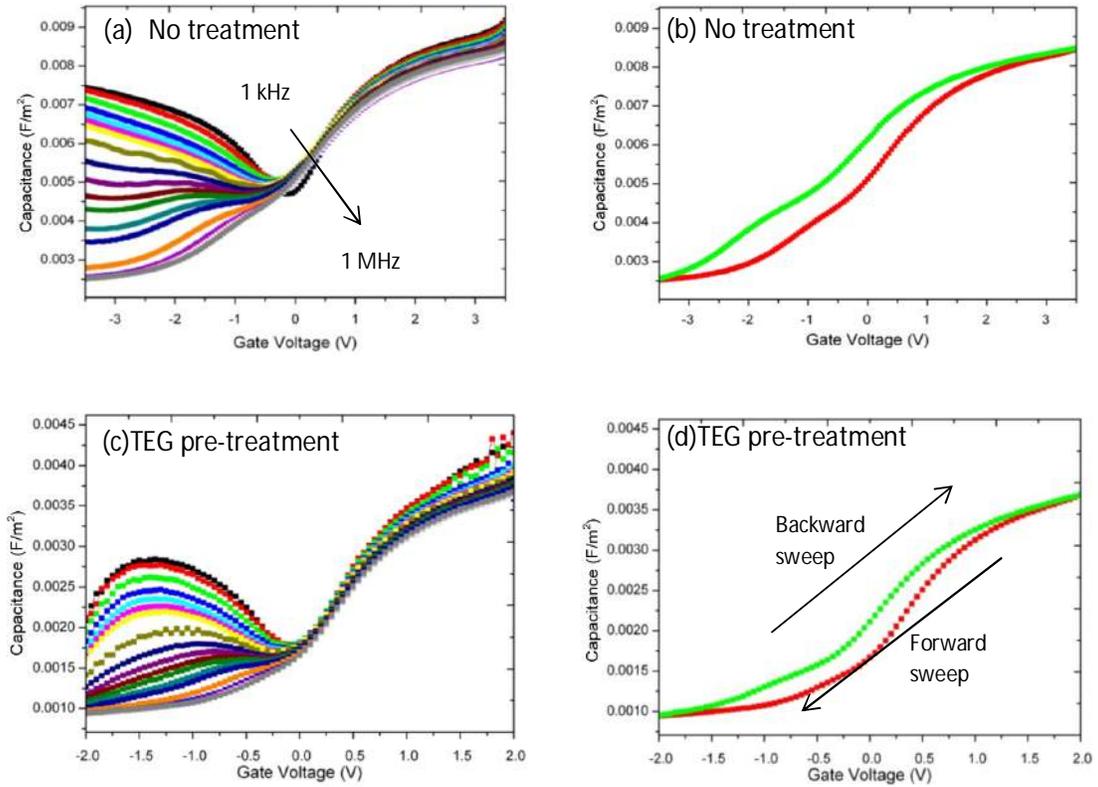


Fig. 4.7: Multi-frequency C-V characteristics of *n*-Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks with varying surface treatments, hysteresis sweeps from accumulation to inversion in red and the corresponding inversion to accumulation sweep in green a) Native sample with no treatment, b) 1MHz hysteresis of native sample 580ΔmV c) in-situ TEG treatment d) hysteresis of in-situ sample Δ100mV

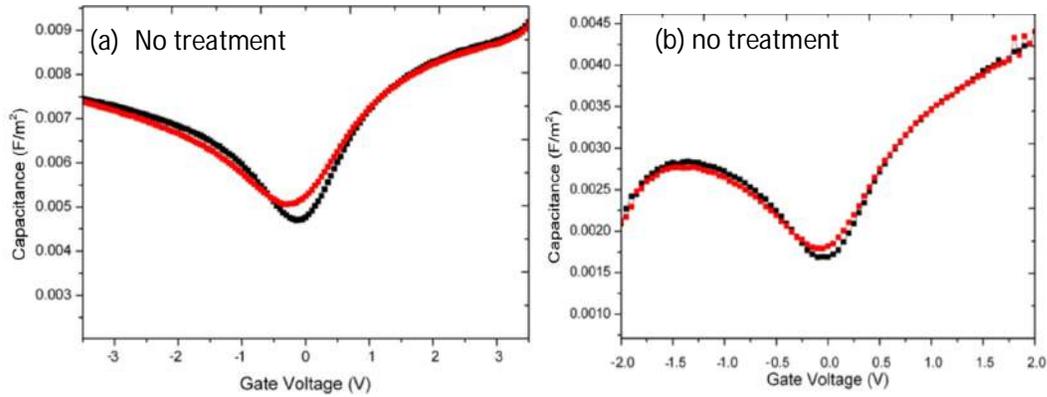


Fig. 4.8: 1 kHz frequency sweeps of n -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks with varying surface treatments. The initial 1 kHz sweep is shown in black with the second 1 kHz sweep shown in red. Both are swept forward from accumulation to depletion a) Native sample with no treatment and b) in-situ TEG treatment.

4.3.4 C-V characteristics of p -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As capacitors

Figure 4.9 displays the C-V characteristics of p -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks with and without a TEG surface pre-treatment. Comparison of maximum capacitance in accumulation of TEG pre-treated samples shows less than half (0.00225 F/m²) of the calculated maximum of 0.0127 F/m² calculated as per appendix A for an 6nm Al₂O₃ film, concurrent with observations for n -type samples. Similar to n -type samples to account for the difference in C_{\max} the extra 1nm observed in TEM would have to be accounted for as a 1nm film with a very low κ value.

Both measured samples exhibit frequency dependant dispersion in accumulation which has been considered characteristic of border traps¹²⁻¹⁴ with a larger magnitude of dispersion observed for TEG pre-pulse treated samples. A hump from -0.5V to 0.5V is observable in both samples, associated with the capture and emission of minority carriers at near midgap interface states¹⁹, with inversion like behaviour exhibited by reference samples. In contrast

the TEG pre-treated sample capacitance is observed to pass through this feature and decline with increasing bias, a feature associated with interface states¹⁹.

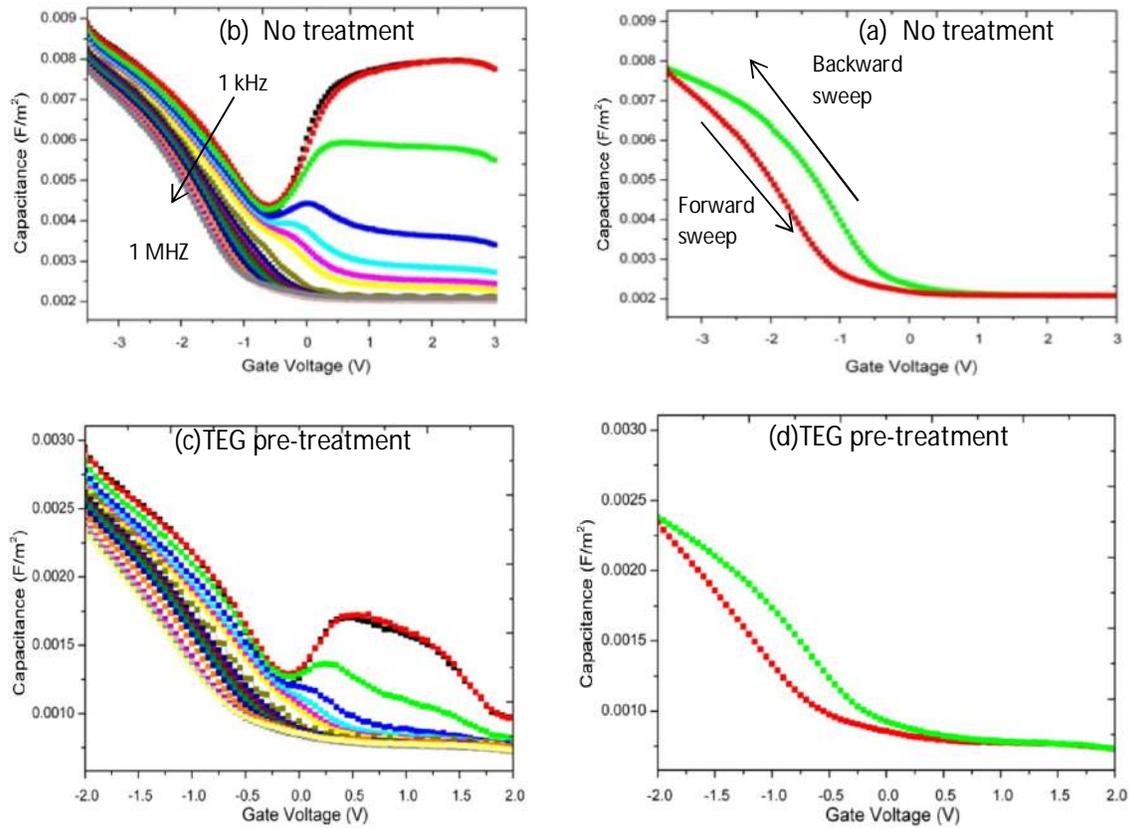


Fig. 4.9 Multi-frequency CV characteristics of p -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks with varying surface treatments, hysteresis sweeps from accumulation to inversion in red and the corresponding inversion to accumulation sweep in green a) Native sample with no treatment, b) 1MHz hysteresis of native sample Δ 520mV c) in-situ TEG treatment d) 1MHz hysteresis of in-situ sample

4.4 Indium phosphide devices

4.4.1 I-V characteristics of n -Au/Ni/Al₂O₃/InP capacitors

Figure 4.10 displays leakage current densities for n - and p - samples. n -type samples which receive no TMI pre-pulsing clearly exhibit the lowest leakage current with some variability

between measurements observed an indication of cross wafer oxide non uniformity. Samples which receive a pre-pulsing treatment of TMI exhibit extremely large leakage current densities at low voltages resembling immediate breakdown, a possible indication that pre-pulsing with TMI leads to the creation of leakage pathways or hinders the removal of native oxides during deposition from TMA and water, accounting for the large leakage current densities observed. *p*-type samples mirror *n*-type results samples which receive no TMI pre-pulsing treatment display a lower leakage current density, with large leakage current densities at low voltages observed for samples which receive a TMI pre-pulse treatment

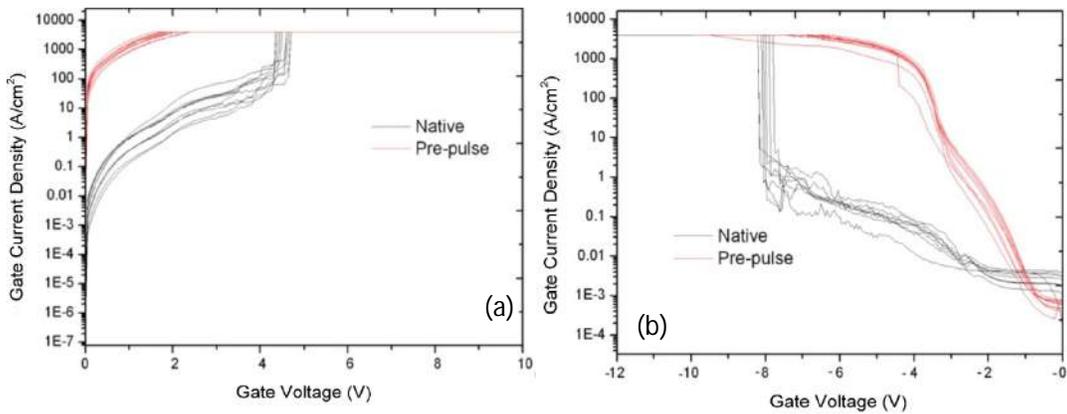


Fig. 4.10: Leakage current density characteristics of a) 18 *n*-type Au/Ni/Al₂O₃/InP devices, reference samples are displayed in black and samples which receive a TMI pre-treatment in red b) 14 *p*-type Au/Ni/Al₂O₃/InP, reference samples are displayed in black and samples which receive a TMI pre-treatment in red.

4.4.2 C-V characteristics of *n*-Au/Ni/Al₂O₃/InP capacitors

Figure 4.11 displays C-V characteristics for an *n*-Au/Ni/Al₂O₃/InP capacitor. Maximum calculated capacitance in accumulation of 0.00952 F/m² for an 8nm Al₂O₃ film is not observed, but a figure of 0.0074 F/m² is reached, an indication that there may be a contribution from native oxides present on the surface of the InP causing a drop in maximum capacitance, however capacitance lowering is also observed on III-V substrates due to the

defect trapping. Previously reported InP capacitors with either an Al₂O₃ or HfO₂ high-κ layer exhibit a large dispersion in all parts of the C-V when measured at room temperature^{26,27}. In contrast this C-V is well behaved with little dispersion observed in any part of the C-V curve. Hysteresis is observed in the bias range is ca. 400mv, typically large for high-κ/III-V capacitors and generally attributed to charge trapping in oxide layer defects, most frequently the oxygen vacancy¹⁵⁻¹⁸. No C-V analysis is provided for TMI treated samples due to the large leakage current density which rapidly saturates as seen in I-V characteristics in rendering them unsuitable for measurement fig 4.10.

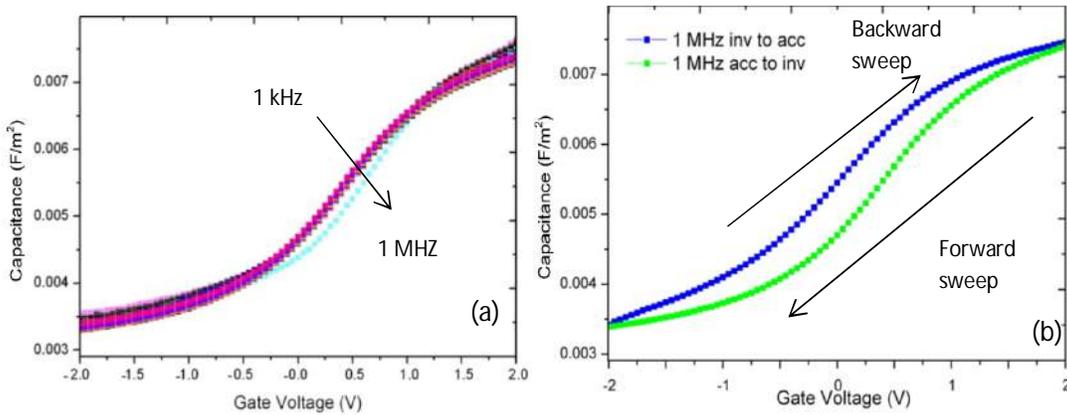


Fig. 4.11: Multi-frequency C-V characteristics of *n*-Au/Ni/Al₂O₃/InP capacitors sweeps from accumulation to inversion in green and the corresponding inversion to accumulation sweep in blue a) reference samples fabricated without receiving a surface treatment and b) hysteresis measurement of the same sample.

4.4.3 C-V characteristics of *p*-Au/Ni/Al₂O₃/InP capacitors

Figure 4.12 shows the C-V characteristics of *p*-Au/Ni/Al₂O₃/InP capacitor. Dispersion present in the “accumulation” portion of the C-V may be attributed to the presence of border traps however the complete C-V response lies outside the bias range investigated with only a small portion observable which is not true accumulation behaviour. A hump from ca. 0V to

1V may be evidenced which in other III-V/high- κ systems has been to capture and emission of minority carriers at near midgap interfaces¹⁹. Similar C-V curves have been reported for $n\text{-Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ capacitors by Alian et al.²⁸ and attributed to a large density of border traps present coupled with indium segregation from the bulk. Midgap states for InP substrates have previously been attributed to In-In dimers²⁹ and P dangling bonds³⁰, with P-P dimers and In dangling bonds suggested to create acceptor like traps^{29, 31} in the lower half of the bandgap accounting for the poor electrical characteristics of p -type devices. This may be plausible for untreated InP devices and would account for the large leakage current densities observed.

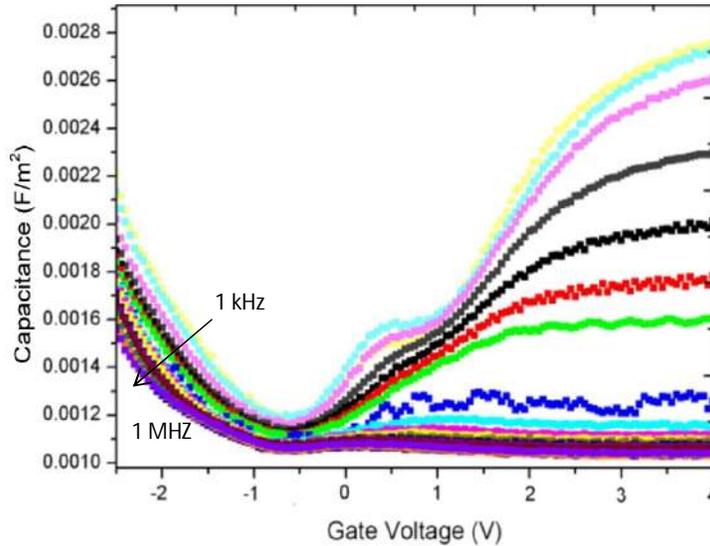


Fig. 4.12: Multi-frequency C-V characteristics of a $p\text{-Au/Ni/Al}_2\text{O}_3/\text{InP}$ reference sample fabricated without receiving a surface treatment

4.5 Summary and Conclusions

The effects of pre-pulsing TEG on GaAs and InGaAs and TMI on InP has been investigated, the broad trend across all samples tested is that pre-pulsing increases the magnitude of the midgap response and increases leakage current density, an indication that a larger number of

interface defects are formed during subsequent Al_2O_3 deposition. A minor improvement is observed for some *n*-type devices however with such a large dispersion of characteristics direct attribution of this improvement to TEG pre-treatment is not possible. Modelled data and limited in-situ studies indicate that TEG binds to the GaAs surface as a diethylgallium (DEG) species with the loss of ethylene and hydrogen through a β -elimination process or radical reaction pathways and deposition of a gallium sub-oxide³²⁻³⁷. The deposition of metallic Ga on the surface would be expected to create more leakage pathways and degrade electrical characteristics of devices. Previous studies however using reflectance anisotropy during exposure of TEG to GaAs at 573k produced no change in the reflectance anisotropy response³⁸ but there is evidence that TEG strongly absorbs at 300k and some thermal decomposition is expected at 573k with the possible formation of Ga dimers at the semiconductor surface^{39,40}.

$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ samples which receive a pre-pulse treatment all exhibit a lower capacitance than anticipated; this is possibly due to the formation of a thin interfacial layer of gallium sub-oxide, creating a metallic rich surface during the TEG pre-pulsing or incomplete removal of native oxides during Al_2O_3 deposition. Electrical characteristics of treated samples display high leakage currents with an apparent increase in the magnitude of the midgap D_{it} after treatment. Similarly *p*-type samples display increased leakage current after exposure to TEG and an increased midgap response in C-V curves, an indication that pre-pulsing TEG has a detrimental effect on interface formation during subsequent Al_2O_3 growth. This is to be expected as it has previously been reported that the presence of Indium in a GaAs surface leads to an enhancement in DEG desorption and to lower the temperature at which absorbed ethyl groups decompose to gas phase ethane thereby increasing the amount of Ga sub-oxides or Ga dimers which may be deposited on the surface⁴¹.

InP samples show degradation in electrical performance as a consequence of pre-pulsing with TMI with no measurable C-V characteristics for *p*-type samples receiving the pre-pulse treatment, the proposed cause of this is the segregation of Indium from bulk semiconductor or the deposition of Indium metal from TMI precursor. Recent experiments investigating the evolution of the Al₂O₃/InP interface from H₂SO₄ cleaned and (NH₄)₂S passivated surfaces suggests the formation of an AlPO₄ interlayer⁴² accompanied by an increase in metallic Indium and Phosphorous at the interface occurs. Previous experiments have also suggested that oxidation of the semiconductor surface may take place by In₀ and P₀ out-diffusion, which may also lead to the formation of a metallic P₀ interlayer between the oxide and the substrate with some metallic In₀ at the surface⁴³ diffusion of metallic elements would account for large leakage densities observed for TMI treated capacitors. Due to the deleterious effects of pre-pulsing treatments and the generally poor characteristics of reference samples no TEM analysis was undertaken for InP samples as currently the standard TMA and H₂O provides superior MOSFET characteristics⁴⁴.

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Chapter 5: Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As

MOSCAP's with in-situ surface treatments.

Introduction

In this study two approaches are attempted. In_{0.53}Ga_{0.47}As substrates were exposed to H₂/Ar plasma to remove native oxides and improve the Al₂O₃/In_{0.53}Ga_{0.47}As interface and compare efficacy to previously investigated ex-situ ammonium sulphide passivation. The second aim was to attempt an in-situ ammonium sulphide etch and passivation minimising any possible re-oxidation due to the unstable nature of surface passivation from sulphur solutions when exposed to atmospheric conditions, previous work on vapour phase passivation of In_{0.53}Ga_{0.47}As indicates an improvement in device performance with minimal exposure to ammonium sulphide vapour¹. The electrical characteristics of the MOS devices were determined using current-voltage (I-V) and capacitance-voltage (C-V) analysis.

General experimental overview

All In_{0.53}Ga_{0.47}As epitaxial layers used in this work were the same as wafers described in chapter 3 and were supplied by IQE with wafer no's NMRC01-5-3417-6140-C and NMRC01-5-4415-4391-B respectively.

For ex-situ etched samples discussed in section 5.1 and 5.2 ammonium sulphide aqueous solution was purchased (22%) from sigma Aldrich and used as supplied, samples which received an optimised etch prior to plasma treatment were immersed in 10% ammonium

sulphide solution for 20 minutes, rinsed with deionized water and dried under nitrogen, with a transfer time of 3 minutes recorded for removal from etching solution to insertion into the Cambridge nanotech ALD chamber. A transfer time of 5 minutes was recorded for removal from etching solution to insertion into the homebuilt reactor.

Electrical capacitors were fabricated by lithographically defining device areas and using thermal evaporation of 50nm Ni and 70nm Au to form gate electrodes of area $2.5 \times 10^{-9} \text{ m}^2$. Devices were analysed using a Cascade Microtech summit model 12971B, used with the Agilent B1500 CV enabled device analyser as previous.

In-situ ammonium sulphide experiments discussed in section 5.2 utilised a direct draw homebuilt reactor with a base pressure of 6.0×10^{-3} mbar and operational pressure of 7.1×10^{-3} mbar 5 minutes recorded and electrical devices fabricated as described previously.

To provide reference samples, both *n*- and *p*- type substrates were used as received with native oxide present and subsequent 80 cycles of Al_2O_3 deposited at 300°C . A total of 80 cycles of Al_2O_3 were deposited from trimethylaluminium and water as precursors at 300°C with 10ms pulse times and 190s purge time respectively for each precursor utilising a TMA pulse first. All in-situ samples were placed into the reactor as received at room temperature and were subsequently exposed to 50 pulses of ammonium sulphide lasting either 100ms or 500ms, before subsequent deposition of 80 cycles of Al_2O_3 at the 300°C with 10ms pulse times and 250s purge time respectively for each precursor.

5.1 In-situ plasma cleaning

5.1.1 Experimental methodology

In-situ plasma treatment experiments utilised a direct draw commercial reactor Cambridge NanoTech Fiji F200LLC System. High purity argon gas is continually passed through the flow tube as purge gas and a yields reactor base pressure of 0.04 torr. Plasma treatment consisted of exposure to an RF plasma at 13.56 MHz, which consisted of 30SCCM (standard cubic centimetres per minute) (98%)H₂/(2%)Ar with 170 SCCM Ar for a total exposure time of 60s at 300°C and a plasma power of 300W. To provide reference samples, both *n*- and *p*-type substrates were used as received with native oxide present and Al₂O₃ deposited at 300°C. A total of 80 cycles of Al₂O₃ were deposited from trimethylaluminium and water as precursors with 10ms pulse times and 10s purge time respectively for each precursor utilising a TMA pulse first. Trimethyl aluminium and water were chosen as precursors to thermally deposit Al₂O₃ to a nominal thickness of 8nm. A total of 80 cycles of Al₂O₃ were deposited as per the fabrication of reference samples.

The sample set is summarised in the following table:

Substrate	Pre-treatment	ALD Temperature °C	No. cycles Al ₂ O ₃
<i>n/p</i> InGaAs	None	300	80
<i>n/p</i> InGaAs	Ex-situ (NH ₄) ₂ S	300	80
<i>n/p</i> InGaAs	H ₂ Plasma	300	80
<i>n/p</i> InGaAs	Ex-situ (NH ₄) ₂ S and H ₂ Plasma	300	80

Table. 5.1: The sample set investigated during plasma pre-treatment experiments.

5.1.2 Electrical Analysis

5.1.2.1 I-V characteristics of *n*-Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As Capacitors

Figure 4.2 shows representative leakage current density curves of *n*-Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As capacitors. Samples which receive no surface treatment display a leakage current density $\sim 1 \times 10^{-6}$ to 1×10^{-5} A/cm² at 4V and breakdown voltages of ~ 7.62 Mv/cm. In comparison samples which receive the previously investigated ex-situ sulphur etch display a leakage current density of the order $\sim 10^{-7}$ A/cm² and display breakdown voltages of 8.85-8.87 Mv/cm which has previously been attributed to the removal of native oxides by the ammonium sulphide etch and the self-cleaning action of trimethylaluminium and the high bandgap of Al₂O₃^{2,3}. A comparable performance is observed for hydrogen plasma treated samples, which display the same leakage current at 4V $\sim 10^{-7}$ A/cm² and breakdown voltages of ~ 8.81 Mv/cm which indicates an improvement of the interface. Contrary to these observations for individual treatments the combination of plasma and an ex-situ etch shows a high leakage current of 10^{-3} A/cm² at 4V and a breakdown voltage of ~ 7.6 Mv/cm which is two orders of magnitude higher than the samples which have received no treatments at all

which display leakage current densities at 4V $\sim 10^{-5}$ A/cm². The observation of this behaviour may be an indication that consecutive treatments that etch the surface of the substrate may induce variation in surface roughness and cause some cross-wafer non-uniformity.

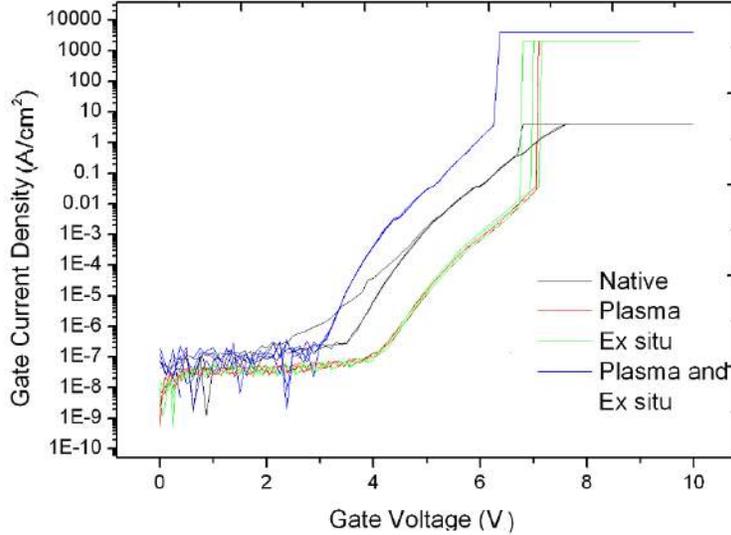


Fig. 5.1: Leakage current density characteristics for 12 measured *n*-Au/Ni- $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSCAP stacks with reference samples shown in black, plasma treated samples shown in red, ex-situ ammonium sulphide treated samples show in green and samples which receive both treatments shown in blue.

5.1.2.2 C-V characteristics of *n*-Au/Ni/ $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ capacitors

Figure 5.2 Presents multi-frequency capacitance-voltage graphs for all treated *n*-Au/Ni/ $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSCAP stacks. All samples display frequency dispersion in accumulation that is weakly dependent on frequency which has been previously attributed to the presence of border traps^{4,5} and more recently has been correlated to the presence of disorder induced gap states at the high- κ III-V interface⁶. Plasma only treated samples (5.2b) appear to have a slightly increased dispersion in accumulation consistent with an increase in border traps in the high- κ oxide. Lowest frequency dispersion observed is for samples which receive an ex-situ ammonium sulphide etch only (5.2c) with dispersion in accumulation

slightly larger for samples which receive both treatments (5.2d). Some change of the flatband voltage is also observable dependant on surface treatment, which may be tracked by reading the V_{fb} from the theoretical V_{fb} capacitance calculated as per appendix A; an indication of differing amounts of fixed charge present in the oxide. V_{fb} shift towards more positive voltages is evident indicative of the presence of negative fixed charge. This has previously been attributed to changes in the Al:O stoichiometry at the interface of Al_2O_3 films leading to increased fixed charge via unsatisfied oxygen bonds, some of this fixed charge may be removed by a forming gas anneal⁷⁻¹⁰. H_2 Plasma only treatment exhibits the largest flat band shift indicating that while it may be effective at removing native oxides at the semiconductor surface it does not lead to the formation of a good interface disrupting the transition region from the $In_{0.53}Ga_{0.47}As$ substrate to the high- κ Al_2O_3 layer.

All samples pass through a peak at negative voltage associated with minority carrier capture and emission at near midgap interface defects¹¹ considered to be characteristic of III-V surfaces irrespective of gate oxide and passivation method¹²⁻¹⁶, this has not yet fully been attributed though it is expected to be caused by atom vacancies or surface As-dimers as the possible origin of the midgap interface states. The reduction in the magnitude of this peak is indicative of a reduction of interface defects at the high- κ /III-V interface. Capacitance does not reach the calculated C_{min} of 0.00202 F/m^2 as calculated in appendix A for any sample, an indication that interaction of interface traps is causing inefficient band bending¹⁷ however the ex-situ ammonium sulphide etch samples come very close.

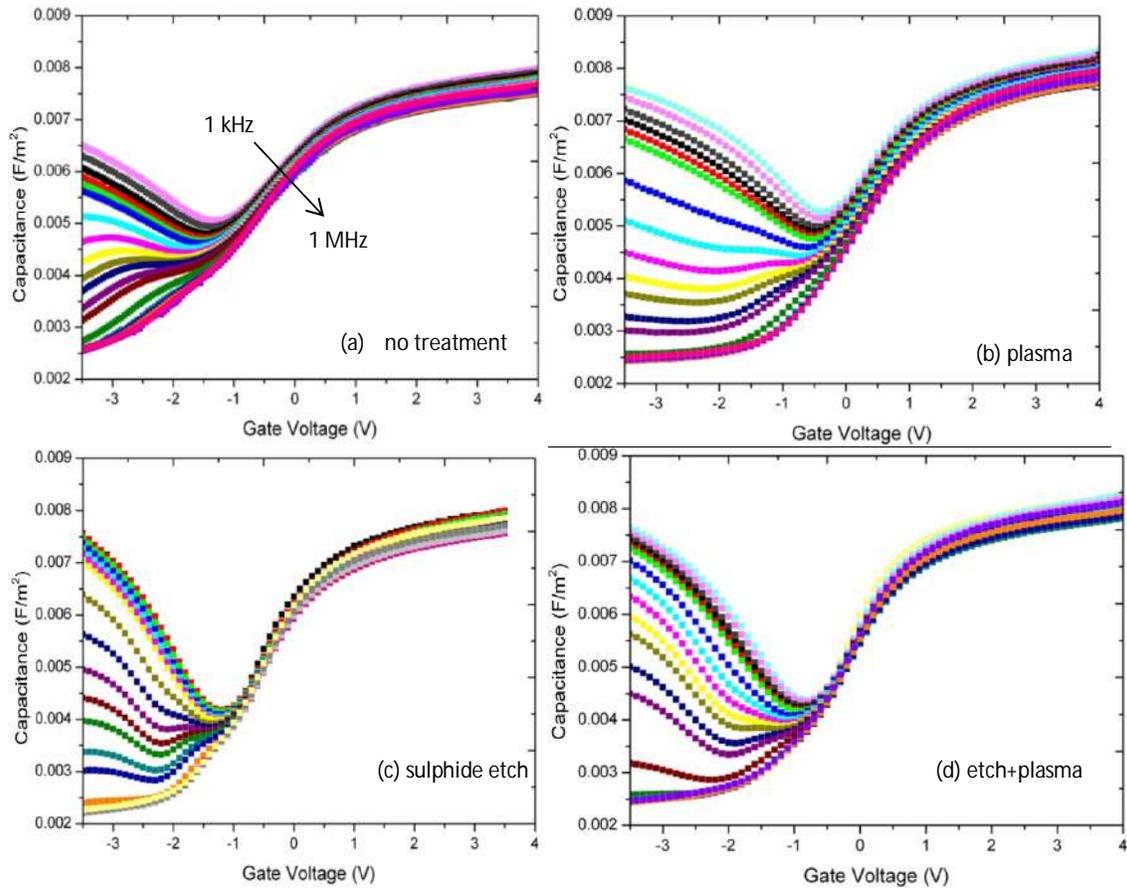


Fig. 5.2: Multi-frequency C-V characteristics of n -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks with varying surface treatments a) Reference sample with no treatment, b) Plasma treated sample c) Ex-situ ammonium sulphide etch d) Ex-situ ammonium sulphide etch and plasma treatment.

Figure 5.3 Displays high frequency (1MHz) hysteresis curves for all samples. The largest magnitude reduction achieved is for ammonium sulphide treated samples which exhibit the steepest slope and least flatband voltage shift $\Delta 220\text{mV}$. In comparison the plasma only treated sample and the sample which receives both surface preparations display more stretch out caused by charge in interface states²⁰. The negative shift observed corresponds to positive charge being trapped in border traps as the capacitor is biased into negative voltage. It has

been suggested that the charge trapping responsible for the C-V hysteresis is taking place primarily in the interfacial oxide transition layer between the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and the ALD deposited oxide. The maximum reduction in hysteresis observed for samples receiving an ex-situ etch only indicates that there is a smaller density of defects in the Al_2O_3 dielectric, indicating the ammonium sulphide etch provides the best interface with the substrate and a reduction in border traps evidenced from the reduction in hysteresis and frequency dispersion in accumulation. The larger hysteresis for samples receiving both an ex-situ etch and a plasma pre-treatment indicates that subsequent plasma treatment results in a disruption of this interface leading to an increase in switching states. Charges trapped in border traps are injected from the substrate and the observed reduction in border traps may be achieved through functionalization of the substrate with $-\text{SH}$ termination providing sufficient sites for $\text{Al}(\text{CH}_3)_3$ nucleation and resulting in a less Al poor interface. This was previously observed with negative fixed sheet charge near the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface for thin films due to an Al poor local environment and positive fixed charge distributed in the Al_2O_3 film bulk due to locally poor O environment⁹. The use of a hydrogen plasma after the ammonium sulphide etch will remove these $-\text{SH}$ terminations resulting in a smaller number of nucleation sites at the interface leading to more of the Al poor behaviour previously observed at interfaces leading to defects which may trap charge.

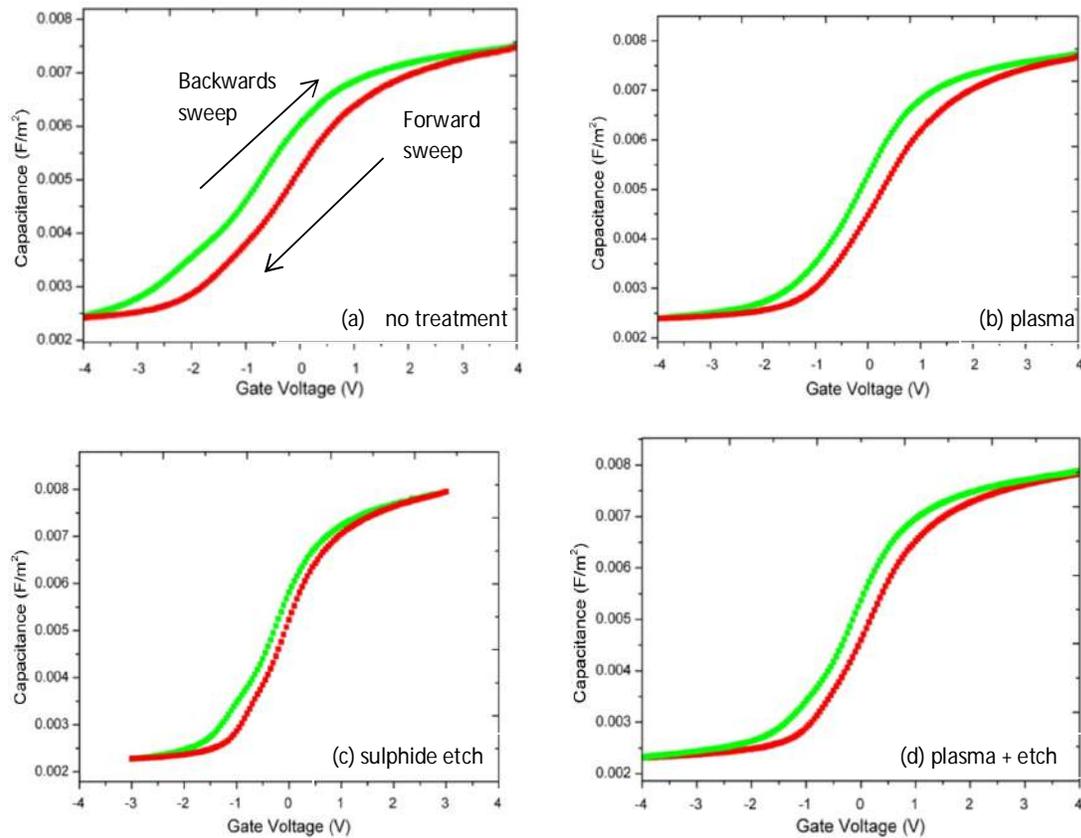


Fig. 5.3: Comparison of 1MHz frequency hysteresis of n -Au/Ni- Al_2O_3 / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOSCAP stacks with varying surface treatments, sweeps from accumulation to inversion in red and the corresponding inversion to accumulation sweep in green a) Native sample with no treatment ΔV 730 mV, b) Plasma treated sample ΔV 550 mV c) Ex-situ ammonium sulphide etch ΔV 220mV d) Ex-situ ammonium sulphide etch and plasma treatment ΔV 350 mV.

5.1.2.3 I-V characteristics of p -Au/Ni/ Al_2O_3 / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ Capacitors

Figure 5.4 shows the I-V responses for all p -Au/Ni/ Al_2O_3 / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ capacitors. In-situ plasma treated samples with and without an ex-situ ammonium sulphide etch display leakage current ca. 10^{-8} A/cm² from 0V to ca. 3V whereupon tunnelling current is observed to rise dramatically with breakdown voltages of 10.6-11 and 7.2-6.8 Mv/cm observed for plasma treatments and both treatments respectively. In contrast samples which have received an ex-

situ ammonium sulphide etch display a leakage current of 10^{-7} A/cm² until a significant increase in leakage current density is observed at ca. 4V when tunnelling current begins to rise with a breakdown events seen at 7.5-9.4 Mv/cm. Samples treated with plasma before deposition of the gate dielectric appear to exhibit less variance in breakdown voltages with a 0.3V variance observed between all breakdown events compared to the largest difference in breakdown events of 0.75V for ex-situ ammonium sulphide treated samples, an indication of good cross wafer characteristics with in-situ plasma treatments. The low leakage current density of samples which have no surface treatment may be attributable to the “self-cleaning” reactions reported to take place during the deposition of Al₂O₃ from TMA on In_{0.53}Ga_{0.47}As^{2,3}.

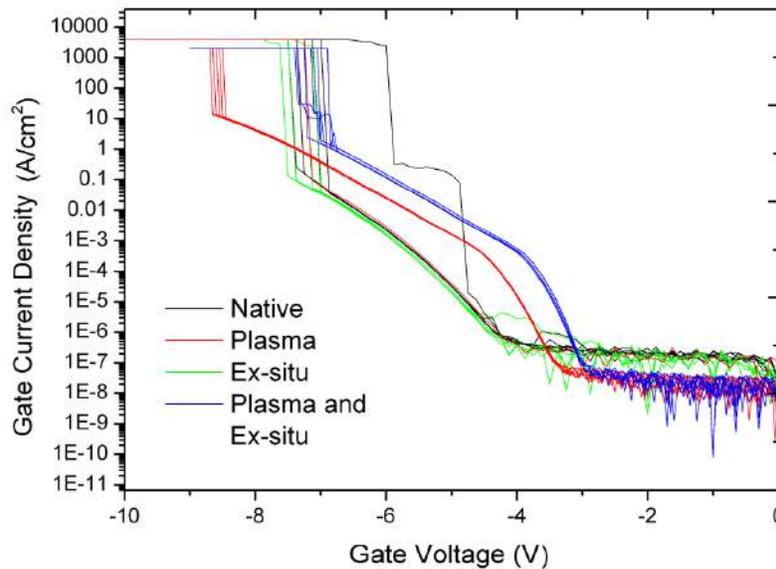


Fig. 5.4: Comparison of I-V characteristics for 18 p-Au/Ni-Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks with varying surface treatments. Reference samples are displayed in black, in-situ plasma treatments in red, ex-situ ammonium sulphide etch in green and ex-situ etch followed by in-situ plasma treatment in blue.

5.1.2.4 C-V characteristics of *p*-Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As Capacitors

Figure 5.5 shows capacitance-voltage graphs for all surface treated *p*-Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks from 1kHz to 1MHz. All samples display similar accumulation capacitance with slightly lower maximum accumulation capacitance observed for the reference sample and plasma only treated sample. This may be accounted for by the incomplete removal of native oxides, a remaining thin layer of native oxides will add to the thickness of the MOSCAP stack; lowering the capacitance slightly.

All samples display some frequency dependant dispersion in accumulation most likely due to the presence of border traps^{4,5}, lowest frequency dispersion in accumulation is observed for the ex-situ ammonium sulphide etch similar to *n*-type device observations, corresponding to a reduction in border traps. The application of both surface treatments results in a marginally increased dispersion in accumulation when compared to ex-situ ammonium sulphide treated samples, however this is less prominent than in reference samples and plasma only treated samples. The inversion portion of the C-V also exhibits a decrease in capacitance at the conclusion of the sweep for the sample which receives both treatments compared to all other samples, this is likely due to leakage current at 3.5V of ca. $7 \times 10^{-5} \text{ A/cm}^2$ evident in the I-V characteristics. For all samples a “hump” is observed from ca. 0V to 1V which has previously been attributed to minority carrier capture and emission at midgap interface states¹¹ with the smallest magnitude and a less broad peak seen for ex-situ ammonium sulphide etch samples and dual passivation treatment samples.

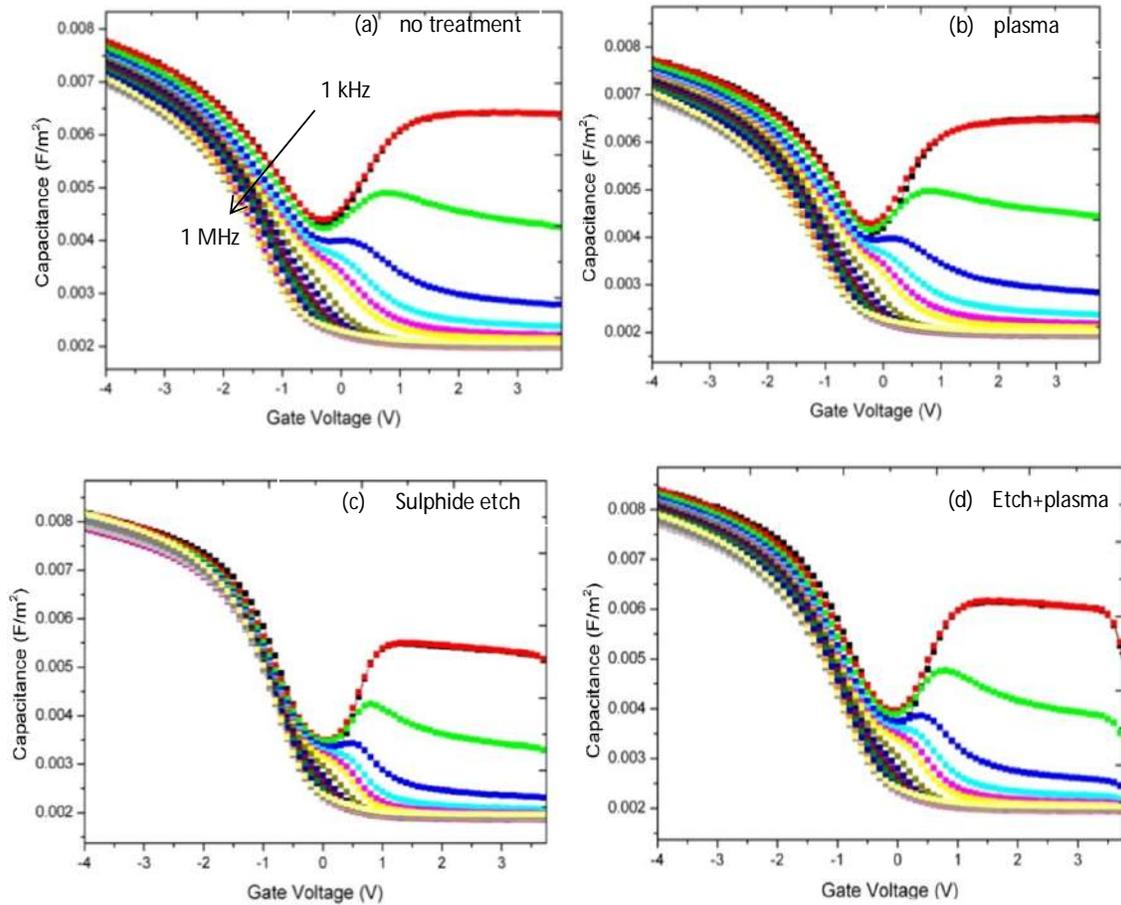


Fig.5.5: Multi-frequency C-V characteristics of p -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks with varying surface treatments a) Native sample with no treatment, b) Plasma treated sample c) ammonium sulphide etch, d) Ammonium sulphide etch and plasma treatment.

Figure 5.6 displays hysteresis measurements of p -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As. An observed shift towards positive voltage is present for all samples; it has been suggested that the charge trapping responsible for the C-V hysteresis is taking place primarily in the interfacial oxide transition layer between the semiconductor and the ALD deposited oxide¹⁹. The smallest shift is observed for the ammonium sulphide treated sample, indicating the most efficient improvement of the interface and a good quality oxide, plasma treated samples have a reduced shift compared to reference samples indicating a reduction in traps after plasma treatment. Samples receiving both treatments exhibit an increased hysteresis compared to

ammonium sulphide treated samples an indication that there is a larger density of rechargeable traps possible caused by interface degradation caused by using two cleaning techniques in series.

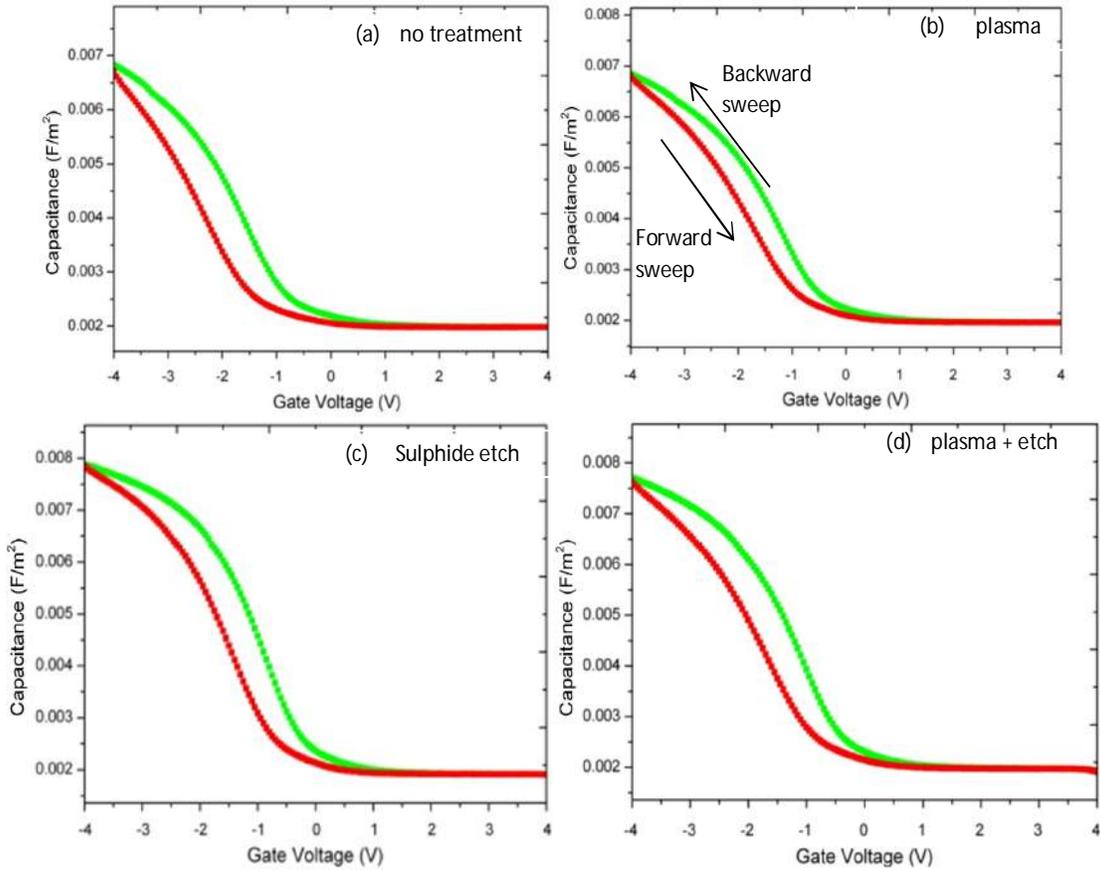


Fig. 5.6: Comparison of 1MHz characteristics of p -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks with varying surface treatments, sweeps from accumulation to inversion in red and the corresponding inversion to accumulation sweep in green a) Native sample with no treatment ΔV 650 mV, b) Plasma treated sample ΔV 550mV c) Ammonium sulphide etch ΔV 200 mV d) Ammonium sulphide etch and plasma treatment ΔV 350 mV.

5.1.3 Initial D_{it} estimation

Calculations assume a nominal thickness of 8nm for Al_2O_3 films, a dielectric constant (κ) of 8.6 previously determined from a thickness series²¹ and a doping level of $4 \times 10^{17} \text{ cm}^{-3}$ for all substrates. Details of calculation methods are included in appendix A.

Treatment	$C_{fb} (\text{F/m}^2)$	$n V_{fb} (\text{V})$	$p V_{fb} (\text{V})$	Est. $D_{it} \text{ cm}^{-2} \text{ eV}^{-1}$
Native	6.15×10^{-3}	-0.1	-2.75	1.17×10^{17}
Plasma	6.15×10^{-3}	0.67	-2.6	7.39×10^{16}
Sulphur	6.15×10^{-3}	-0.01	-1.4	4.18×10^{16}
Both	6.15×10^{-3}	0.25	-1.8	5.13×10^{16}

Table 5.2: Calculated density of interface defects for all surface treatments.

Largest magnitude reduction of interface defects and border traps is achieved with an ex-situ ammonium sulphide etch. The use of both an ex-situ etch and an in-situ plasma treatment generally lead to improved characteristics with less frequency dispersion associated with midgap defects and less accumulation dispersion associated with border traps when compared to reference samples. Plasma only treatment leads to either no improvement in accumulation behaviour or a marginal increase in dispersion, with an improvement in interface defect density observed for n -type devices and a minor improvement for p -type devices.

It is very important to note that the theoretical calculation likely overestimates the density of interface traps and does not take into account the presence of amounts of fixed charge present

in the gate oxide which would affect the reading of the flatband voltage from the calculated ideal flatband capacitance, it is used here as an indication only.

5.2 In-situ ammonium sulphide treatment

5.2.1 Experimental methodology

In-situ ammonium sulphide experiments utilised a direct draw homebuilt reactor with a base pressure of 6.0×10^{-3} mbar and operational pressure of 7.1×10^{-3} mbar. Wafer etching was carried out as previously described with a transfer time of 5 minutes recorded and electrical devices fabricated as described previously.

To provide reference samples, both *n*- and *p*- type substrates were used as received with native oxide present and subsequent 80 cycles of Al_2O_3 deposited at 300°C . A total of 80 cycles of Al_2O_3 were deposited from trimethylaluminium and water as precursors at 300°C with 100ms pulse times and 190s purge time respectively for each precursor utilising a TMA pulse first. All in-situ treated samples were placed into the reactor as received at room temperature and were subsequently exposed to 50 pulses of ammonium sulphide lasting either 100ms or 500ms, before subsequent deposition of 80 cycles of Al_2O_3 at the 300°C with 10ms pulse times and 250s purge time respectively for each precursor. A bubbler was filled with ammonium sulphide prior to each in-situ pre-pulse treatment and re-filled with fresh chemical prior to each new deposition; ammonium sulphide was pulsed 50 times with pulse duration of either 100ms or 500ms with 250s purge times.

The following table details the experiments carried out:

Substrate	Ex situ etch	In situ etch	Al ₂ O ₃ (nm)	Etch Temperature (°C)
<i>n/p</i> - InGaAs	-	-	8	-
<i>n/p</i> - InGaAs	20 minutes, 10%	-	8	25
<i>n/p</i> - InGaAs	-	50 x100ms	8	25
<i>n/p</i> - InGaAs	-	50 x 500ms	8	25

Table 5.3: The sample set investigated during in-situ passivation experiments.

5.2.2 Electrical Analysis

5.2.2.1 IV characteristics of *n*-Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As Capacitors

Figure 5.7 shows the typical IV characteristics for the Native oxide control sample, ex-situ ammonium sulphide etch, 100ms in-situ ammonium sulphide treatment, 500ms in-situ ammonium sulphide treatment. Leakage current density associated with tunnelling increases quickly for in-situ treated samples past 0.5V with the lowest leakage current density observed for reference samples which may be attributed to the “clean up” action of TMA on III-V native oxides^{2,3}. Largest increase in leakage density and lowest breakdown voltages are observed for samples receiving an ex-situ ammonium sulphide etch a possible indication of partial re-oxidation during sample transfer to the homebuilt ALD chamber which has substantial transfer and vac down times. This is best highlighted by the difference in I-V

curves for ex-situ ammonium sulphide etches in figure 5.7 and 5.10 compared to those of figure 5.1 and 5.4. Leakage current density for both in-situ treated samples is broadly similar with slightly lower leakage current density observed for samples which receive a longer total exposure time to ammonium sulphide vapour, an indication that interface improvement is reliant on exposure time however there is not a significant improvement seen over reference samples an indication that optimisation of in-situ pulse duration is needed to produce an improved surface passivation. Breakdown voltages observed are 5.6-5.9 Mv/cm for native reference samples, 4.12-4.37 Mv/cm for ex-situ treated samples, 5.1-6 Mv/cm for 100ms in-situ treated samples and 6.3-7 Mv/cm for 500ms in-situ treated samples.

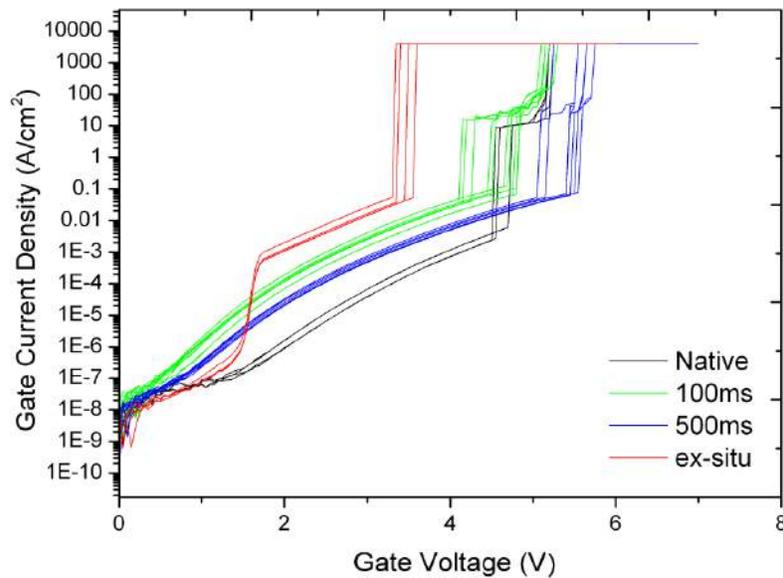


Fig. 5.7: Comparison of IV characteristics of 21 n -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks with varying surface treatments with reference devices displayed in black, ammonium sulphide etch devices displayed in red, 100ms in-situ etch displayed in green and 500ms in-situ etch displayed in blue.

5.2.2.2 CV characteristics of n -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As Capacitors

Figure 5.8 shows the C-V characteristics for all surface treatments carried out on n -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As. All samples display a similar accumulation capacitance apart from the 50x500ms in-situ treated ammonium sulphide sample, which displays a capacitance which is lower than any other sample measured, this may be accounted for by suggesting that the oxide layer in that sample may be thicker than other samples which would diminish capacitance which is unlikely as all samples were grown by the same process. Alternatively the presence of a small amount of unremoved native oxides at the interface would result in a lowered κ -value of the dielectric. A variance between initial 1 kHz sweeps easily seen in the non-treated and ex-situ ammonium sulphide sweeps is an indication of the presence of charge in deep traps in the system; this feature is diminished for 100ms in-situ treatments and almost disappears completely for 500ms treated samples indicating less charge trapping in deep traps.

Reference samples display a typical C-V of a high- κ III/V interface with a large dispersion in accumulation due to border traps^{4,5}, with no inversion characteristics observed at large negative bias rather a frequency dependant dispersion. Ex-situ ammonium treated samples display a frequency dependant defect response from ca. 0V to -1V manifesting as a hump at negative voltage accompanied which has been attributed to the capture and emission of minority carriers at midgap defects⁶ accompanied by inversion like behaviour at large negative bias, however measured capacitance approaches but does not reach the calculated minimum capacitance of 0.00192 F/m² an indication of inefficient Fermi level movement¹⁵. The C-V characteristics of the ex-situ treated sample is similar to the C-V of devices measured by O'Connor et al. where a long transfer time from the etching solution was correlated with an increase in electrically active defects²⁰. Capacitance in the inversion portion of the in-situ C-V exceeds the capacitance of all other devices, this may be correlated

with the increased leakage observed in the I-V characteristics of ex-situ passivated devices, a possible effect of the long transfer times to the homebuilt chamber. In-situ treated samples do not exhibit the same characteristics at negative voltages as ex-situ treated samples, it appears that the interface defect response is pushed to the left of the CV – an indication that a larger magnitude of fixed positive charge is present in the in-situ treated samples.

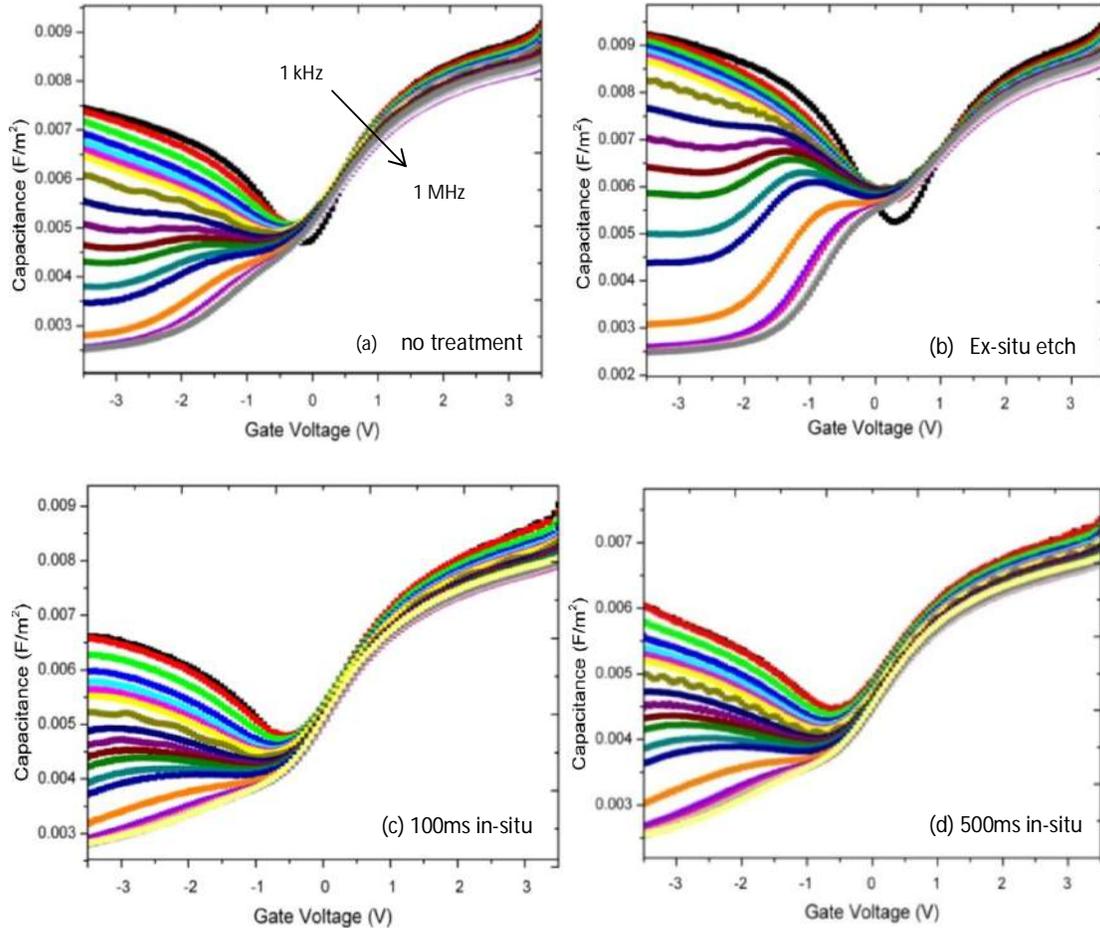


Fig. 5.8: Multi-frequency C-V characteristics of n -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks with varying surface treatments a) Native sample with no treatment, b) ammonium sulphide etch c) 100ms in-situ ammonium sulphide etch d) 500ms in-situ ammonium sulphide etch

Figure 5.9 displays 1 MHz hysteresis curves for all samples tested. All samples exhibit a negative voltage shift upon C-V sweeping from accumulation to inversion and back again. This can be accounted for as a manifestation of charge trapping in defects at the transition region from the semiconductor to the high- κ oxide¹⁹. Lowest hysteresis is observed for 500ms in-situ treated samples an indication of an improved interface between the semiconductor and the Al₂O₃ film deposited. Conversely largest hysteresis is exhibited by samples which we speculate have partially re-oxidised due to exposure to atmospheric oxygen.

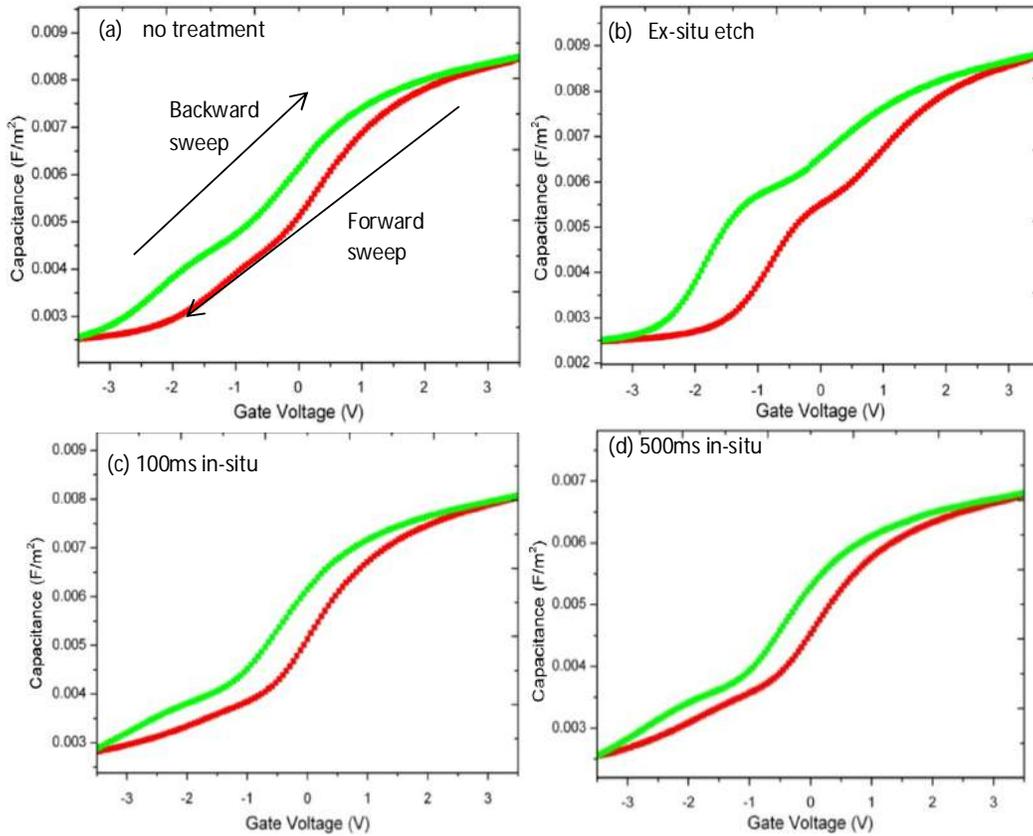


Fig.5.9: Comparison of 1MHz hysteresis characteristics of n -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks with varying surface treatments, sweeps from accumulation to inversion in red and the corresponding inversion to accumulation sweep in green a) Native sample with no treatment ΔV 650 mV, b) ammonium sulphide etch ΔV 900 mV c) 100ms in-situ etch ΔV 550 mV d) 500ms in-situ etch ΔV 150 mV.

5.2.2.3 I-V characteristics of p -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As Capacitors

Figure 5.10 shows the I-V characteristics for a) Native oxide control sample, b) Ex-situ ammonium sulphide etch, c) 100ms in situ ammonium sulphide treatment, d) 500ms in situ ammonium sulphide treatment. Leakage densities for ex-situ treated samples and reference samples are comparable over the entire voltage range with increases in leakage current density beginning at ca. 1V. In-situ treated samples exhibit larger leakage current densities over the voltage range investigated with ca. 3 orders of magnitude difference in leakage

density at 1V between in-situ treated samples and reference and ex-situ ammonium sulphide treated samples with leakages of ca. 9×10^{-8} A/cm² for reference and ex-situ samples and breakdown events seen at 7.63-8.37 Mv/cm and 7.43-7.62 Mv/cm respectively, ca. 2×10^{-6} A/cm² for 50x500ms in-situ treated samples with breakdown events at 7.8-8.4 Mv/cm and ca. 1.6×10^{-5} A/cm² with breakdown events seen at 7.2-7.75 Mv/cm for 10x100ms in-situ treated respectively. This is an indication that in-situ ammonium sulphide is not as effective as an ex-situ etch at removing native oxide and passivating the interface. Leakage current is slightly lower for samples exposed to longer ammonium sulphide pulses as was observed on *n*-type samples, again an indication that pulse times and total exposure for an in-situ process requires optimisation to achieve a level of passivation comparable to that of an ex-situ ammonium sulphide etch.

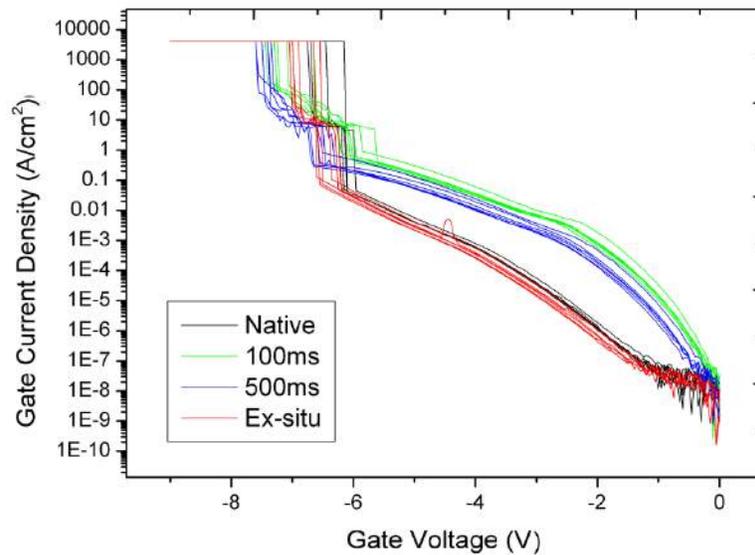


Fig. 5.10: Comparison of IV characteristics of 24 *n*-Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks with varying surface treatments with reference devices displayed in black, ex-situ ammonium sulphide exposed devices displayed in red, 100ms in-situ etch displayed in green and 500ms in-situ etch displayed in blue

5.2.2.4 C-V characteristics of p -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As Capacitors

Figure 5.11 shows the C-V characteristics for all surface treatments carried out on p -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks. Ex-situ ammonium sulphide treated samples exhibit improved C-V characteristics, with a reduced dispersion in accumulation indicating a reduction in border traps^{4,5} and a reduced defect response at negative voltages associated with midgap D_{it} ¹¹ when compared to reference samples. In-situ treated samples display a vastly changed capacitance-voltage characteristic, with the large frequency dependant dispersion in the accumulation region reported to be characteristic of border traps^{4,5} and a large magnitude of stretch out in the CV characteristics indicative of interface trapped charge¹⁸. Such magnitude of dispersion is a sign that no true accumulation regime is actually reached for in-situ treated devices. Both in-situ treated samples display a very large response from 0V to the end of the C-V sweep characteristic of capture and emission events at interface defects¹¹. The magnitude of these characteristics appears to decline at the edge of the C-V characteristics for samples with a longer total exposure time, indicating longer exposure times will be needed to effectively passivate the surface. The large difference between in-situ treated n - and p - type capacitors measured is a symptom of exhaustion of sulphur from the chemical solution used during passivation despite fresh solution being used for each treatment, leading to inadequate passivation of the semiconductor surface. No sample is seen to reach minimum calculated capacitance 0.00192 F/m² however reference samples and ex-situ treated ammonium sulphide samples approach it, an indication that interface traps effectively pin the Fermi level around midgap inhibiting inversion¹⁶ from in-situ treated samples.

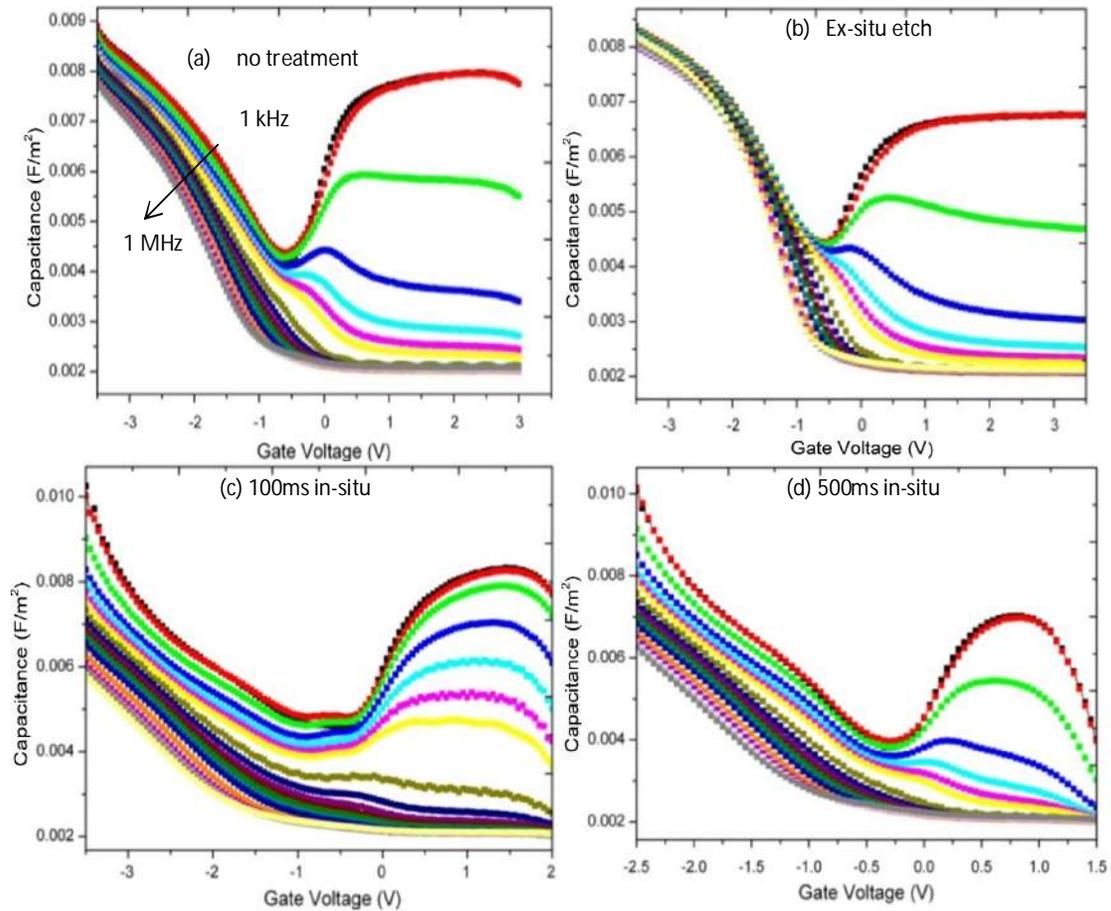


Fig. 5.11: Multi-frequency CV characteristics of p -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks with varying surface treatments a) Native sample with no treatment, b) ammonium sulphide etch, c) 100ms in-situ etch and d) 500ms in-situ etch

Figure 5.12 displays 1MHz hysteresis curves for all samples tested. All samples display a shift towards the right hand side, an indication of negative charge trapping. The difference between in-situ treated n - and p - type capacitors measured is a symptom of exhaustion of sulphur from the chemical solution used during passivation. Lowest hysteresis is observed for samples treated with an ammonium sulphide etch, however both 100ms and 500ms in-situ treated samples appear to display reduced hysteresis compared to the non-treated sample, however due to the large density of defect states and high leakage current the full C-V response is not observable in this instance.

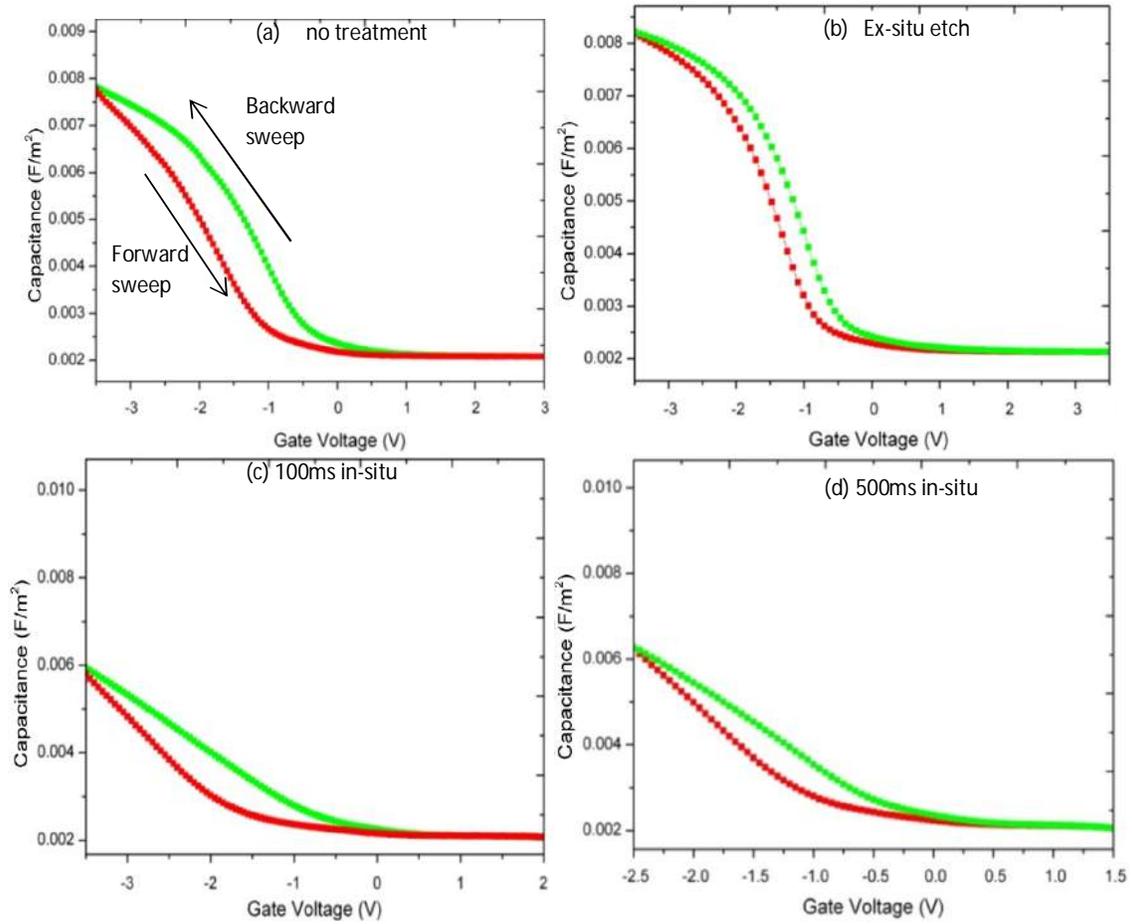


Fig. 5.12: 1MHz hysteresis sweeps of p -Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks with varying surface treatments, sweeps from accumulation to inversion in red and the corresponding inversion to accumulation sweep in green a) Native sample with no treatment ΔV 650 mV, b) ammonium sulphide etch ΔV 200 mV c) 100ms in-situ etch ΔV 700 mV d) 500ms in-situ etch ΔV 400 mV

5.2.3 Initial D_{it} estimation

Calculations assume a nominal thickness of 8nm for Al₂O₃ films, a dielectric constant (κ) of 8.6 previously determined from a thickness series¹⁹ and a doping level of $4 \times 10^{17} \text{cm}^{-3}$ for all substrates. Details of calculation methods are included in appendix A.

Treatment	C_{fb} (F/m²)	n V_{fb} (F/m²)	p V_{fb} (F/m²)	Est. D_{it} (cm²)
Native	6.15 x 10 ⁻³	0.45	-1.9	4.53 x 10 ¹⁶
Ex situ	6.15 x 10 ⁻³	0.5	1	-1.12 x 10 ¹⁶
In situ 100ms	6.15 x 10 ⁻³	0.45	-3.5	1.41 x 10 ¹⁷
In situ 500ms	6.15 x 10 ⁻³	1.45	-2.5	1.41 x 10 ¹⁷

Table 5.4: Estimated densities of interface defects for all samples investigated.

Largest magnitude reduction of interface defects and border traps is achieved with an ex-situ ammonium sulphide etch. This is not immediately obvious when looking at *n*-type ex-situ C-V characteristics due to some re-oxidation of the surface but is more obvious when looking at *p*-type samples which as a good ex-situ C-V characteristic. Both *n*- and *p*-type samples which receive in-situ passivation treatments indicate no improvement in the electrical characteristics of capacitors over that of reference samples and some degradation compared to the reference samples is observed for *p*-type in-situ treated samples, an indication that not enough ammonium sulphide vapour is being delivered to the semiconductor surface leading to incomplete surface cleaning taking place.

Theoretical calculation overestimates the density of interface traps and does not take into account the presence of amounts of fixed charge present in the gate oxide which would affect the reading of the flatband voltage from the calculated ideal flatband capacitance. These initial calculations are most likely not representative of actual D_{it} amounts in the system as in-situ *p*-type samples display poor C-V characteristics with much of the response not observable and D_{it} must be estimated from well behaved high frequency curves, D_{it}

calculations are provided here merely as estimation. The negative number calculated for ex-situ treated samples is due to the re-oxidation taking place during sample transfer seen in the figure (5.08 b), leading to the extraction being negative, which is an error.

5.3 Summary and conclusions

Investigation of leakage current density indicates that plasma treated samples possess comparable or lower leakage current densities than ex-situ ammonium sulphide passivation for *n*-type samples. Similarly for *p*-type samples the use of a plasma treatment reduces the leakage current density at device operating voltages, however at higher voltages larger tunnelling currents are observed. Analysis of multi frequency C-V curves show an improvement from in-situ plasma treated samples, smaller midgap responses were observed from all plasma treated samples indicating an improved $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface compared to no treatment at all. Concurrently an increase in border traps was observed in samples which receive both plasma treatments and an ammonium sulphide etch indicating that subsequent growth after multiple surface treatments may lead to generation of defects in the high- κ oxide an interface which has more defects than the ex-situ etch. Some V_{fb} shift is also observed for samples which receive a plasma treatment an indication of fixed charge in the oxide layer, which has previously been attributed to aluminium dangling bonds²⁰ and may be removed by subsequent hydrogen gas anneal¹⁶. For samples which receive both in-situ treatments it appears that ex-situ sulphur provides the largest component of the interface improvement, however experiments to probe the effect of the order of the treatments could show further improvements in the interface, the use of a plasma etch before surface passivation of the freshly cleaned surface may be more effective than plasma treatment after surface passivation. A comprehensive optimisation of the plasma process may also afford an

interface improvement without a subsequent increase in defects as over exposure to hydrogen plasma has been shown to cause surface roughening in III-V semiconductors²².

n-Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As samples which receive an in-situ ammonium sulphide etch display improved leakage currents when compared to an ex-situ ammonium sulphide etch. Leakage current densities observed are intermediate between ex-situ etch and the reference sample. A difference in leakage current density was observed based on exposure time for in-situ ammonium sulphide samples. 500ms treated devices exhibit leakage current density an order of magnitude lower at 2V than corresponding 100ms exposed samples. The anomalously high leakage current density from ex-situ treated ammonium sulphide samples has been attributed to the partial re-oxidation of the sample as it was transferred to the ALD chamber, O'Conner *et al.*²⁰ have demonstrated the importance of prompt transfer times to maintain surface passivation and prevent native oxide regrowth. *p*-Au/Ni-Al₂O₃/In_{0.53}Ga_{0.47}As samples which receive in-situ ammonium sulphide treatments exhibit a larger leakage current density over all voltages investigated when compared to the ex-situ ammonium sulphide process for reference samples, again longer exposure times in the chamber result in lower leakage current densities however for *p*-type samples the effect is marginal.

C-V characteristics for in-situ ammonium sulphide etch *n*-Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As samples display a dispersion in accumulation similar to ex-situ treated samples with the interface defect response at negative voltage pushed toward the extreme edge of the C-V due to the presence of interface trapped charge causing stretch out¹⁸. C-V curves for *p*-Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As display large stretch out, large dispersion in accumulation with respect to frequency and a large hump at positive voltage characteristic of interface states.

The cause of this effect we have attributed to the exhaustion of sulphur from the solution during pre-treatment causing insufficient passivation of the surface or removal of native oxides. Further work into the optimization of the delivery process may mitigate the loss of sulphur from the solution and subsequently remove some sample variability observed.

There are some further possible sulphur passivation techniques that should be investigated and compared to literature. Some early attempts at passivation using various sulphides are dealt with in the introduction, however more recent work has concentrated on the use of self-assembled layers of thiols, the most widely reported self-assembled monolayer being that from octadecanethiol (ODT)³²⁻³¹, however the stability of thiol passivation is not fully known but vapour deposition of these self-assembled monolayers of thiols has been reported to be more stable to atmospheric conditions compared to a solution based chemistry²². A second method of in situ surface passivation possible would be a combination of the in-situ plasma and in-situ sulphur passivation using a H₂, H₂/N₂ or H₂:H₂S plasma to remove native oxides and passivate the surface as has previously been investigated³²⁻³⁴

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Chapter 6: Characterisation of bilayer capacitors.

Introduction

In this work, a thin interface control layer (ICL) of Al_2O_3 was deposited at the III-V interface. The aim of the ICL was to introduce a wide bandgap material in contact with the III-V semiconductor and the high- κ layer which should increase the barrier height to tunnelling, and thereby reducing the leakage current. Previous work^{1,2} has shown significant improvement of the $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface when a thin ALD Al_2O_3 interface control layer (ICL) is included before high- κ deposition from amide precursors. We combine this process with an ammonium sulphide etch to realise capacitors with well-behaved properties. A nominal thickness of 1 nm of Al_2O_3 was selected to minimize effect on the high- κ stack and allow for further scaling. Samples were grown using identical process flows with the only difference being the HfO_2 precursor with both a chloride and an amide process being used, allowing an investigation into the effect of precursor chemistry on device performance. Previously it was noted that deposition of HfO_2 films from HfCl_4 resulted in damage to the III-V/High- κ interface from acidic reaction by-products^{3,4} and devices fabricated from such films exhibited degraded electrical characteristics due to the incorporation of large amounts of chlorine resulting in large flat band shifts⁵

A further study of the electrical properties of bilayer MOSCAP stack structures grown from the amide process at differing temperature to determine the optimum growth temperature for hafnia growth from amide precursors. Subsequent to this electrical characterisation was carried out of bilayer capacitors with a 1nm Al₂O₃ ICL and HfO₂ deposited at 240°C, 270°C and 300°C from TDMAH to determine the effect of deposition conditions on electrical characteristics of bilayer capacitors. With the best electrical characteristics determined a bilayer sample set was produced with a theoretical 1.04nm EOT (1nm Al₂O₃, 3nm HfO₂) - assuming a κ value of 8.6 for Al₂O₃ previously determined from a thickness series and a κ value of 20 for HfO₂ - to investigate if improved electrical characteristics are also evidenced in reduced thickness MOSCAP stacks and if further improvements can be made to the MOS stack.

6.1 Experimental methodology

All In_{0.53}Ga_{0.47}As epitaxial layers used in this work are the same as chapter 3.

Ammonium sulphide was purchased (22%) from sigma Aldrich and used as supplied, An *ex-situ* (NH₄)₂S surface passivation (10%, 20 min at 25 °C, rinsed in de-ionized water, dried in nitrogen) was performed on half of the III-V substrates before deposition of Al₂O₃, with a transfer time of 3 minutes recorded. These passivation parameters were determined from previous physical and electrical studies^{6,7}. Deposition of metal oxide layers was carried out using two ALD tools to provide two sample sets. Hafnium dioxide samples using the TDMAH (tetrakis-dimethylaminohafnium) precursor and water were grown in a Cambridge NanoTech Fiji F200LLC System at 275°C. An initial Al₂O₃ interface control layer was deposited from TMA and H₂O, with the nucleation delay induced from a sulphur terminated surface taken into account, 12 cycles of deposition were carried out to attempt to furnish an

interface control layer ~1nm thick prior to deposition of 50 cycles of HfO₂ from TDMAH and water. These samples are labelled CNT.

Samples grown using the HfCl₄ precursor and water were grown in an Applied Materials Gemini chamber at 275°C. Similarly to the first sample set an initial Al₂O₃ interface control layer was deposited from TMA and H₂O, with the nucleation delay induced from a sulphur terminated surface taken into account, 12 cycles of deposition were carried out to attempt to furnish an interface control layer ~1nm thick prior to deposition of 65 cycles of HfO₂ from HfCl₄ and water. These samples are labelled AMAT.

Electrical capacitors were fabricated and measured as per chapter 4

6.2 Structural characterization of bilayer capacitors

6.2.1 High resolution Transmission Electron Microscopy

Figure 6.1 displays a high magnification cross sectional TEM micrograph of the oxide bilayers. Oxide thicknesses are assessed via a method employing both bright field and dark field micrographs which are shown in appendix B. Both deposited oxide layers are noted to be amorphous and exhibit an abrupt interface between the Al₂O₃/In_{0.53}Ga_{0.47}As and Al₂O₃/HfO₂ layers. The abruptness of the interface with the substrate coupled with no observable native oxides is an indication of the self-cleaning mechanism occurring during the deposition of Al₂O₃ interface control layers from TMA⁸. Measured oxide layer thickness for TMA/HfCl₄ samples is 1.1nm Al₂O₃ and 5.8nm HfO₂ yielding a growth rate of 0.9Å per cycle for Al₂O₃ on -S terminated In_{0.53}Ga_{0.47}As and a deposition rate of 0.89Å per cycle for HfCl₄ on Al₂O₃. Measured oxide layer thickness for TMA/TDMAH is 1.2nm Al₂O₃ and 6.8nm HfO₂ yielding a growth rate of 1Å per cycle for Al₂O₃ on -S terminated In_{0.53}Ga_{0.47}As and a deposition rate of 1.36Å per cycle for TDMAH on Al₂O₃ - this is larger than expected

as the reported growth rate of TDMAH is 1.1\AA per cycle at 300°C ⁹. The thickness of the oxide bilayers is summarised in the table below.

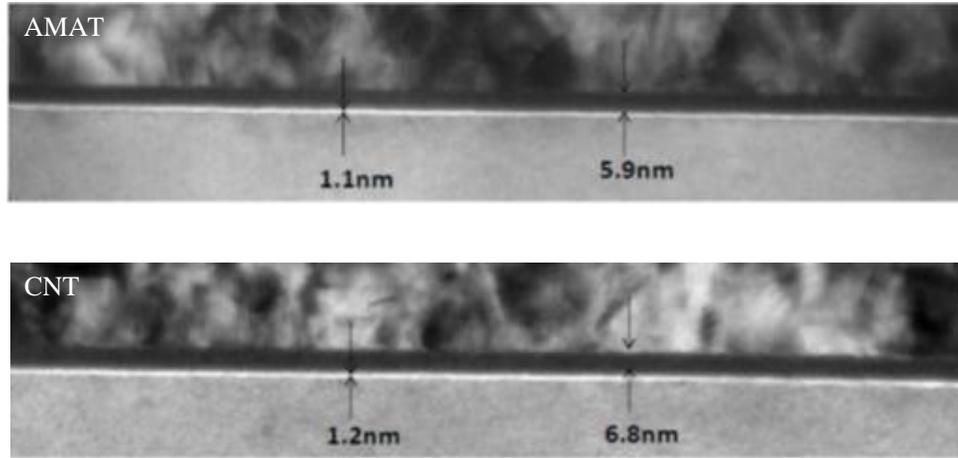


Fig. 6.1: Transmission electron micrographs of Al_2O_3 and HfO_2 layers in MOSCAP structures with a) HCl_4 as the HfO_2 precursor displaying an Al_2O_3 film ~ 1.1 nm thick and a HfO_2 film ~ 5.9 nm thick and b) TDMAH as the HfO_2 precursor exhibiting an Al_2O_3 film ~ 1.2 nm thick and a HfO_2 film ~ 6.8 nm thick

	Nominal HfO_2 thickness nm	Nominal Al_2O_3 thickness nm	Actual HfO_2 thickness nm	Actual Al_2O_3 thickness nm	Native oxide	GPC $\text{HfO}_2/\text{Al}_2\text{O}_3$
AMAT	5	1	5.8	1.1	none	$0.89\text{\AA}/0.9\text{\AA}$
CNT	5	1	6.8	1.2	none	$1.36\text{\AA}/1\text{\AA}$

Table 6.1: Summary of structural investigation by TEM.

6.3 Electrical characterization of bilayer structures

6.3.1 I-V characteristics of n-Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As Capacitors

Figure 6.2 displays leakage current density plots of *n*-Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As stacks. CNT labelled samples refer to devices grown in the Cambridge nanotech with HfCl₄ precursor and AMAT labelled samples refer to devices grown in the Applied materials Gemini dual chamber kit. Both samples exhibit low leakage currents ca. 10⁻⁷ A cm⁻² until gate voltages of ca. 4V is reached for chloride samples and 4.2 V is reached for amide samples. Breakdown voltages show a larger dispersion for TDMAH grown samples (5.25-6.5 Mv/cm) compared to chloride grown samples (6.81-7.54 Mv/cm), this may be attributed to the greater dielectric strength of HfO₂ deposited from HfCl₄. The two “steps” evidenced in leakage current may be the breakdown of one dielectric layer before the other however it is currently unclear which of the bilayers breaks down first, but it has been previously suggested that for dielectrics the larger the κ-value of the oxide the lower the breakdown field¹⁰.

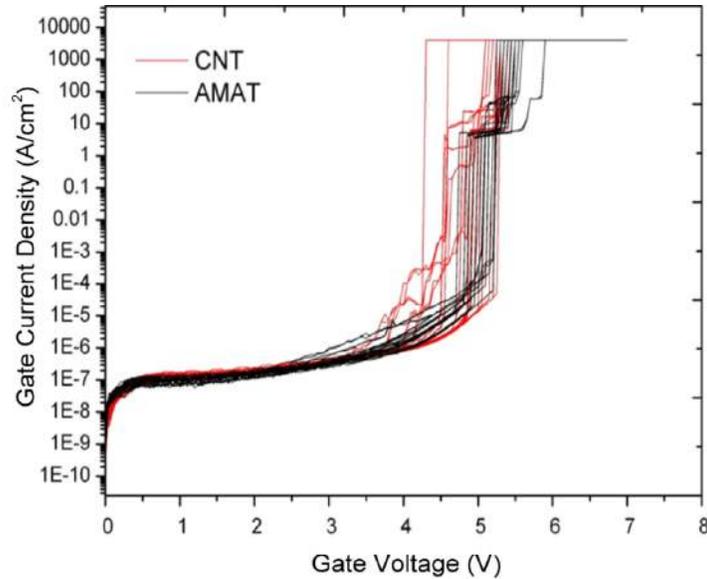


Fig. 6.2: Leakage current density characteristics of 28 *n*-Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As MOS capacitors using HfCl₄ precursor displayed in red and TDMAH precursor displayed in black.

6.3.2 C-V characteristics of *n*-Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As Capacitors

Figure 6.3 displays C-V characteristics of *n*-Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks. Lowest accumulation capacitance is seen for TDMAH grown samples, an indication that the film is thicker than the HfCl₄ film which exhibits a higher accumulation capacitance for the same sweep range; with neither sample reaching the calculated C_{ox} in accumulation – calculated to be 0.03 F/m² for AMAT fabricated samples and 0.026 F/m² for CNT fabricated samples assuming TEM thicknesses are correct. There is some dispersion in accumulation for both measured samples, which may be attributed to the presence of border traps and carrier interaction with them^{11,12}. TDMAH samples appear more stretched out than HfCl₄ samples with a larger magnitude midgap response an indication of a greater magnitude of interface states and trapping occurring in them¹³. Both samples are seen to progress through a small hump ca. 0V to -1V, which is associated with minority carrier capture and emission at near midgap interface defects¹⁴. The minimum calculated capacitance of 0.00193F F/m² is not

reached for amide process samples again assuming that the TEM thicknesses are correct using the κ value of 8.6 for Al_2O_3 previously determined from a thickness series and a κ value of 20 for HfO_2 values, an indication that the Fermi level is hampered by inefficient band bending¹⁵.

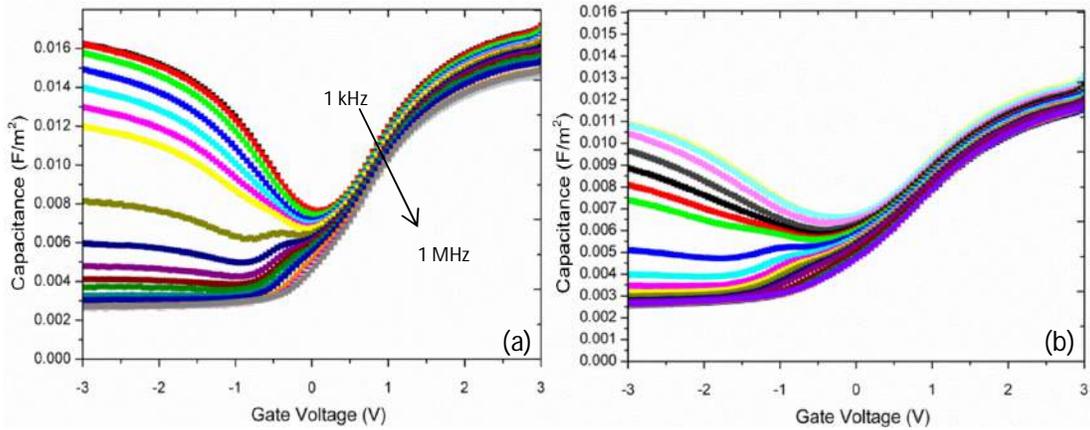


Fig. 6.3: Multi-frequency (1 kHz-1 MHz) C-V characteristics of *n*-

Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As stacks fabricated using a) HfCl₄ precursor and b) TDMAH precursor.

6.3.3 I-V characteristics of *p*-Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As Capacitors

Figure 6.4 displays leakage current characteristics of 22 *p*-Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP devices. Both samples exhibit low leakage current density broadly similar at low gate voltages, with leakage ca. 10^{-7} A cm⁻² until 2.5V, at this point the leakage current densities for both samples are seen to diverge. Breakdown voltages show a smaller dispersion for TDMAH grown samples (7.38-8.01 Mv/cm) compared to chloride grown samples (7.1-8.9 Mv/cm). P-type samples display similar leakage current density here with TDMAH samples having a physically thicker high- κ layer exhibit a marginally lower leakage current density than HfCl₄ an indication the dielectrics in this case are of similar quality.

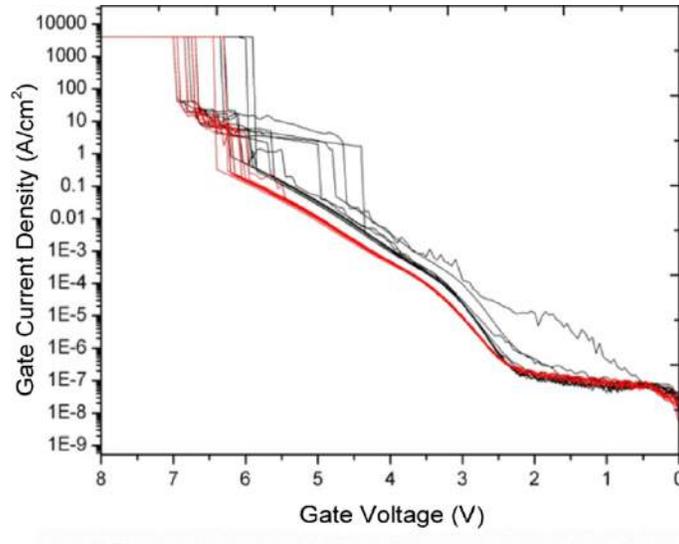


Fig. 6.4: Leakage current density characteristics of 22 p -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks using a) HfCl₄ precursor displayed in black and b) TDMAH precursor displayed in red.

6.3.4 C-V and G_m/ω characteristics of p -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As Capacitors

Figure 6.5 displays C-V characteristics of fabricated p -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks. Lowest accumulation capacitance is again evidenced in TDMAH grown samples, an indication that the film is thicker than the HfCl₄ film. Dispersion in the accumulation region is observed for both samples which is likely attributable to the presence of border traps^{11,12} with the largest magnitude dispersion observed for TDMAH grown HfO₂ samples. Both samples exhibit a frequency dependant hump at negative bias from 0V-ca.1V, which is attributable to the capture and emission of minority carriers at midgap interface defects¹³. Largest magnitude frequency dependant stretch-out is observed for TDMAH grown samples as in n -type samples, this is possibly an indication of the presence of a greater magnitude of interface states in the TDMAH grown sample¹³.

The calculated minimum capacitance is 0.002 F/m^2 for chloride fabricated samples and 0.00193 F/m^2 for amide fabricated samples indicated on the C-V curves in figure 6.5. The minimum calculated capacitance is reached for both of these samples, this is a good indication that inversion may be taking place and has been previously reported as an indication that some Fermi level modulation is taking place¹⁵ however the capacitance is not seen to plateau over the remaining C-V bias range as normally associated with inversion characteristics, this may indicate that there is some decrease in capacitance in the deep inversion portion of the C-V due to deep depletion behaviour perhaps.

To confirm a true inversion response is taking place G_m/ω vs. voltage plots are investigated as exhibited in figure 6.6. G_m/ω vs. voltage graphs indicate that conductance initially increases until a maximum value is reached and then decreases, which is considered to be characteristic of a true inversion response in the Si/SiO₂ system¹⁷. Both amide and chloride process devices exhibit this behaviour where the G_m/ω maximum values occur at approximately the same frequencies as the respective mid-capacitances indicated on the C-V, which is strong evidence of inversion taking place with maximum frequencies seen at 300 Hz and 200 Hz respectively for CNT and AMAT samples indicated by the closed star symbols. For AMAT samples there are some low frequency losses in the regions $> 2\text{V}$, most likely due to conductance losses resulting from the $\sim 1 \times 10^{-6} \text{ A/cm}^2$ gate leakage current density observed previously at 2.75V.

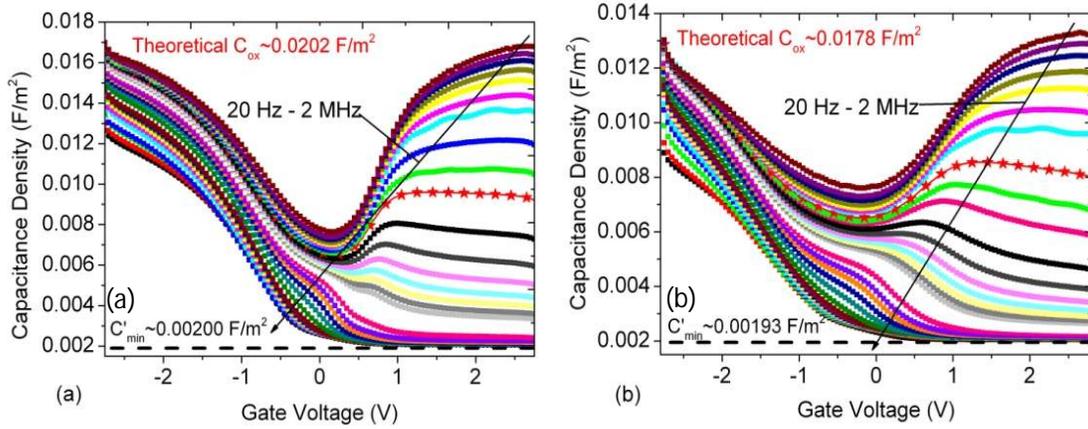


Fig. 6.5: Multi-frequency (20 Hz-2 MHz) C-V characteristics of *p*-

Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks using a) HfCl₄ precursor and b) TDMAH precursor, respective mid-capacitances are indicated by the red line closed stars.

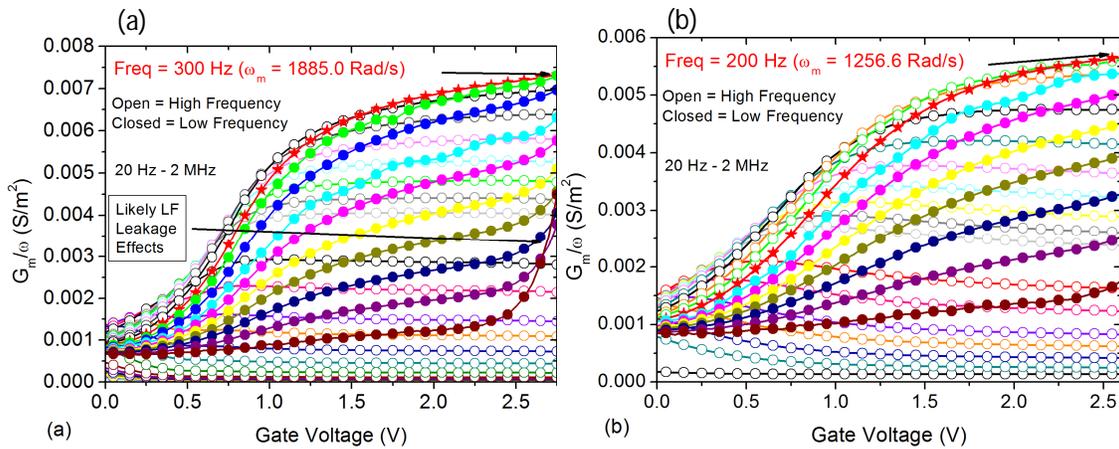


Fig. 6.6: Multi-frequency (20 Hz-2 MHz) G_m/ω -V characteristics of *p*-

Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks using a) HfCl₄ as a precursor and b) TDMAH as a precursor. Low frequencies are open and high frequencies are closed. G_m/ω peaks are indicated by closed red stars.

6.3.5 Determination of midgap D_{it} from the conductance method

Figure 6.7 displays Multi-frequency $G_p-\omega$ characteristics of *n*- and *p*-Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks. Exposure to ambient conditions for a prolonged period leads to the degradation of the bilayer structures with poor C-V

characteristics. To ensure a D_{it} measurement comparable to that of the original MOSCAP devices C-V and G-V characteristics were measured over a range of temperatures from -50°C to 120°C and the magnitude of G-V response at each temperature compared to initial measurements on bilayer capacitors at room temperature. This G-V behaviour at reduced temperature was used to identify at which temperature the degraded sample corresponds most closely to the original MOSCAP G-V characteristics in both position and magnitude. These parameters were then used to measure the midgap D_{it} via the conductance method which were -1.5 - 1.5V at -10°C for n -type AMAT samples, -1.25 – 1V at -30°C for p -type AMAT samples. TDMAH precursor samples were investigated from -1.1 - 1.2V at -30°C for n -type and -1.3 – 1.2V at -40°C for p -type. In devices examined, no peaks are observed above the background noise of the measurement, generally giving a midgap D_{it} of 2 - $4 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. The p -type samples prepared using HfCl_4 is the only one to display a prominent peak above background noise. The magnitude of the highest peak for this sample indicated a midgap D_{it} of $9.4 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$.

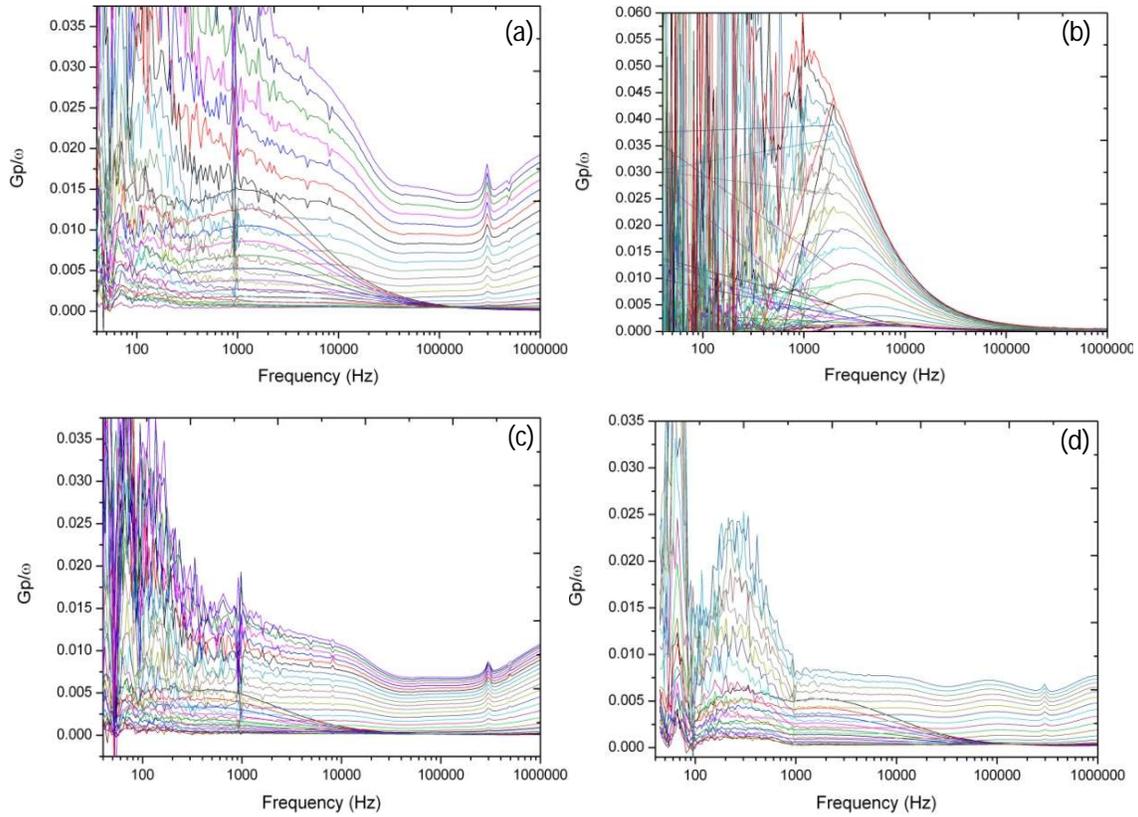


Fig. 6.7: Multi-frequency (20Hz-2MHz) $G_p-\omega$ characteristics of n and p -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks using HfCl₄ precursor over a voltage range a)-1.5-1.5V at -10°C, b)-1.25 – 1V at -30°C and TDMAH precursor over a voltage range c)-1.1.-1.2V at -30°C d)-1.3 – 1.2V at -40°C

6.4 Optimisation of amide deposition temperature

6.4.1 Experimental Methodology

Deposition of oxide layers was carried out on a Cambridge Nanotech Fiji F200LLC system, aluminium oxide was deposited at 300°C to form an ICL of nominal 1nm thickness, hafnium oxide was deposited from TDMAH at 240°C, 270°C and 300°C to a nominal thickness of 5nm, to form bilayer structures. All other methodologies carried out were the same as previously covered in section 6.1.

6.4.2 I-V characteristics *n*- Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As capacitors

Figure 6.8 displays leakage current characteristics of *n*-Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As with HfO₂ deposited from TDMAH at 240°C, 270°C and 300°C. All measured samples display a broadly similar leakage current density with bias of 10⁻⁷ A/cm² for all samples until ca. 3V whereupon leakage current increases until a breakdown event is reached. HfO₂ samples grown at 240°C appear to exhibit the lowest leakage current density with samples grown at 270°C appearing to have the highest leakage current density. Some variation may be observed in final breakdown voltage, samples grown at 270°C and 300°C display a larger range in breakdown voltage of 1.1V (9.4Mv/cm – 11.4Mv/cm) and 500mV (10.2-11.2 M v/cm) respectively compared to a range of 300mV (10.6-11.2 Mv/cm) for 240°C grown sample. The observed variability may be due to structural induced leakage caused by film cross wafer non-uniformity however all dielectric films display good behaviour with high break down voltages.

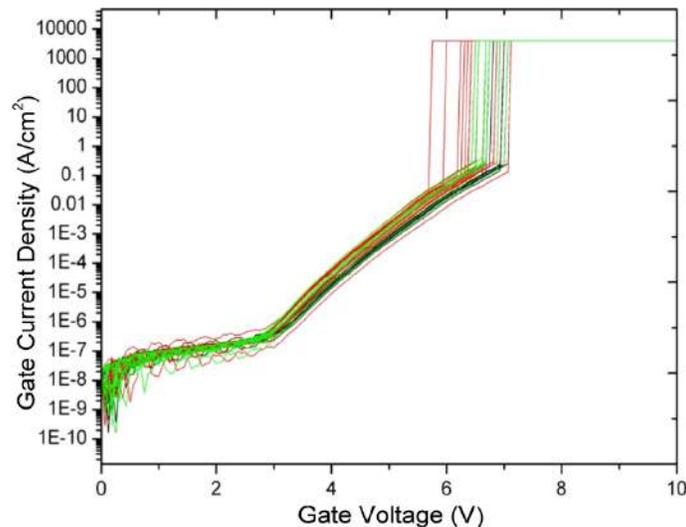


Fig. 6.8: Leakage current density characteristics of 36 *n*-Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks with HfO₂ layers grown from TDMAH at 240°C shown in black, 270°C shown in red and 300°C shown in green.

6.4.3 C-V characteristics of n -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As capacitors

Figure 6.9 displays measured C-V characteristics for n -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As capacitors with hafnia layers grown at a) 240°C, b) 270°C and c) 300°C; characteristics are broadly similar for all samples grown irrespective of temperature. All graphs display charge in deep traps, manifested as a difference between the first two 1 kHz sweeps seen in black and red respectively. All samples display a defect response from ca. -0.5V to -1.5V which has been attributed to the capture and emission of minority carriers at midgap interface states¹⁴. The accumulation region has a weakly frequency dependant response, this has previously been attributed to the presence of border traps^{11,12}. Growth from TDMAH at higher temperatures yields lower flatband voltages from 2.05V at 240°C to 1.5V AT 300°C indicating less fixed negative charge in the bulk oxide films grown at higher temperatures, an indication of an improved quality HfO₂ layer with less negative fixed charge present. Figure 6.10 displays hysteresis curves for samples grown at 240°C, 270°C and 300°C. Hysteresis is seen to decrease from 1.2V to 1V under the same bias range with a hysteresis of 1.2V observed for hafnia grown at 240°C, 1.2V for hafnia grown at 270°C and 1V for hafnia grown at 300°C, an indication that hotter temperatures leads to a better interface of the high- κ with the semiconductor with less charge trapping taking place, this is to be expected as many of the native oxides of In_{0.53}Ga_{0.47}As are volatile at 300°C.

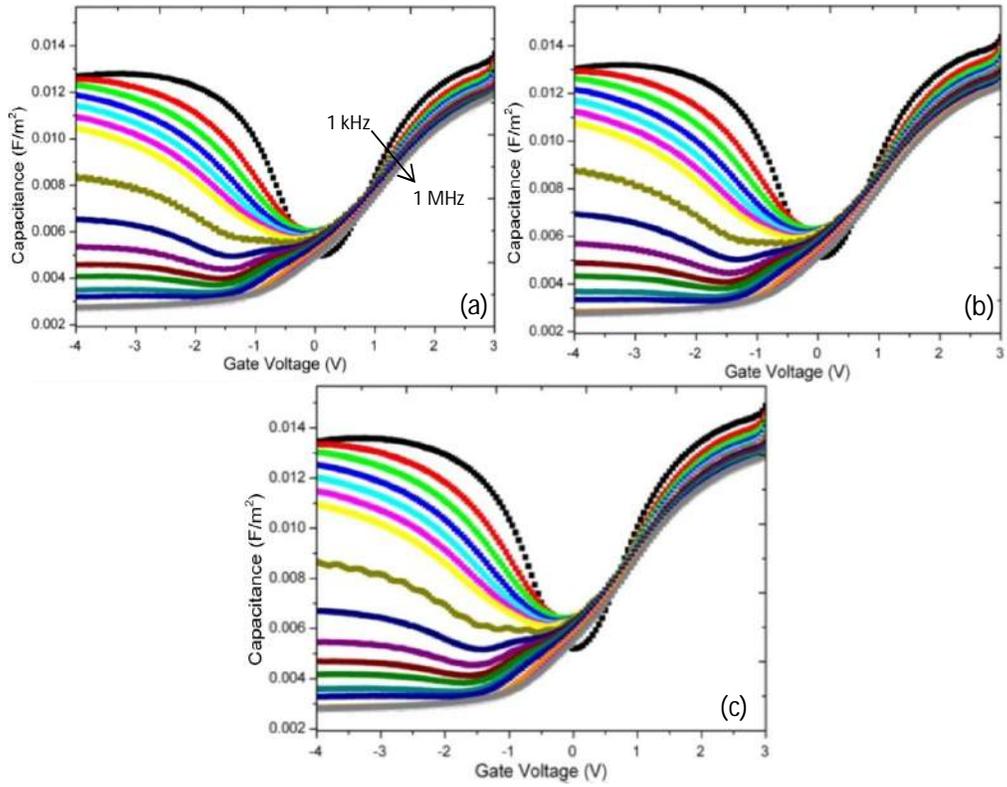


Fig. 6.9: Multi-frequency (1kHz -1Mhz) C-V characteristics for n -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As capacitors with hafnia layers grown at a) 240 °C, b) 270 °C and c) 300°C

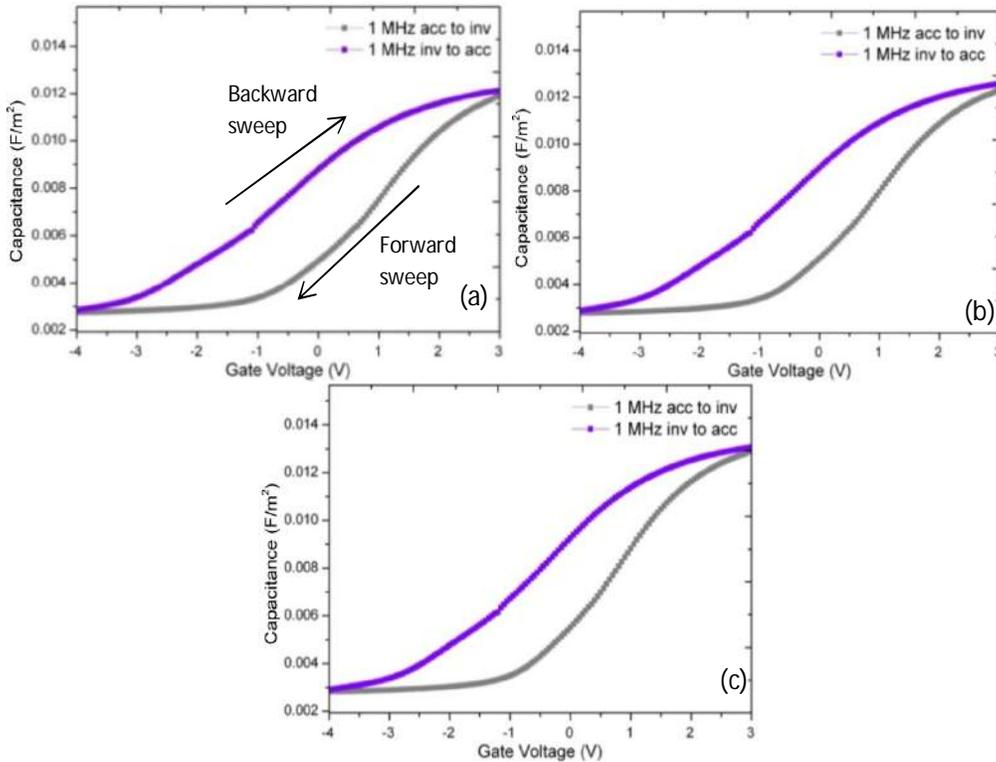


Fig. 6.10: A comparison of 1MHz Hysteresis curves for n -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As films with sweeps from accumulation to inversion in grey and the corresponding inversion to accumulation sweep in purple grown at a) 240°C Δ1.2V, b) 270°C Δ1.2V and c) 300°C Δ 1V.

6.4.4 I-V characteristics p - Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As capacitors

Figure 6.11 displays leakage current characteristics of 36 p -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As with HfO₂ layers grown at 240°C, 270°C and 300°C from TDMAH. All measured samples display similar leakage current density characteristics of ca. 10⁻⁷ A/cm² initially with leakage current density diverging at ca.4V. Complementary to n -type results HfO₂ samples grown at 240°C appear to exhibit the lowest leakage current with typical breakdown events observed at ca. 5.8V (10.2-11.8 Mv/cm) for 240°C, 5.3V (10.2-11 Mv/cm) for 270°C and 5.01V (9.8-10.2 Mv/cm) for 300°C grown devices.

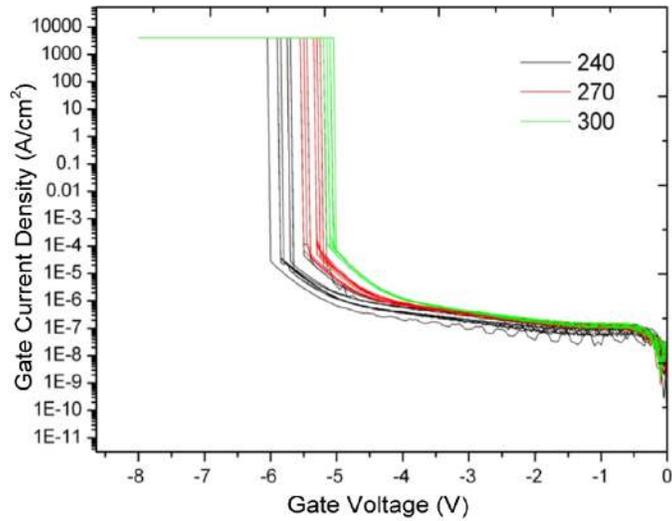


Fig. 6.11: Leakage current density characteristics of 36 p -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks grown at 240°C displayed in black, 270°C displayed in red and 300°C displayed in green.

6.4.5 C-V characteristics of p -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As

Figure 6.12 displays measured C-V characteristics for p -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As capacitors with hafnia layers grown at a) 240°C, b) 270°C and c) 300°C. Samples grown at 240°C exhibit a severely diminished capacitance in accumulation when compared to samples grown at 270°C and 300°C, generally this would indicate that a film is thicker than the other measured samples, however in corresponding n -type samples no such diminished capacitance is observed. Films are assumed to be the same thickness as all samples in this study were grown by the same process, the diminished capacitance may be accounted for by a diminished κ value of the HfO₂ grown at lower temperatures. This diminished capacitance is also accompanied by a large stretch out for the sample grown at 240°C, which is a manifestation of large amounts of interface trapped charge¹³. A weak, frequency dependant dispersion is observed in the accumulation region for all samples, which has previously been attributed to the presence of border traps in the oxide¹¹. All graphs display a difference in

capacitance between each of the 1 kHz sweeps the first in black and the second in red, which is attributable to charge present in deep traps. All samples display a defect response from ca. -0.5V to -1.5V which has been attributed to the capture and emission of minority carriers at midgap interface states¹⁴. Growth from TDMAH at higher temperatures yields lower flatband voltages, shifting from 2.05V at 240°C to 1.5V AT 300°C indicating less fixed charge in the oxide films grown at higher temperatures, an indication of an improved quality HfO₂ layer. Contrary to results for *n*-type samples hysteresis increases from 0.55V to 0.75V as the growth temperature of the sample increases from 270°C to 300°C, an indication of a an increase in traps present in the oxide layer. No hysteresis values are given for hafnia layers deposited at 240°C as the theoretical flat band capacitance was not reached at 1 MHz.

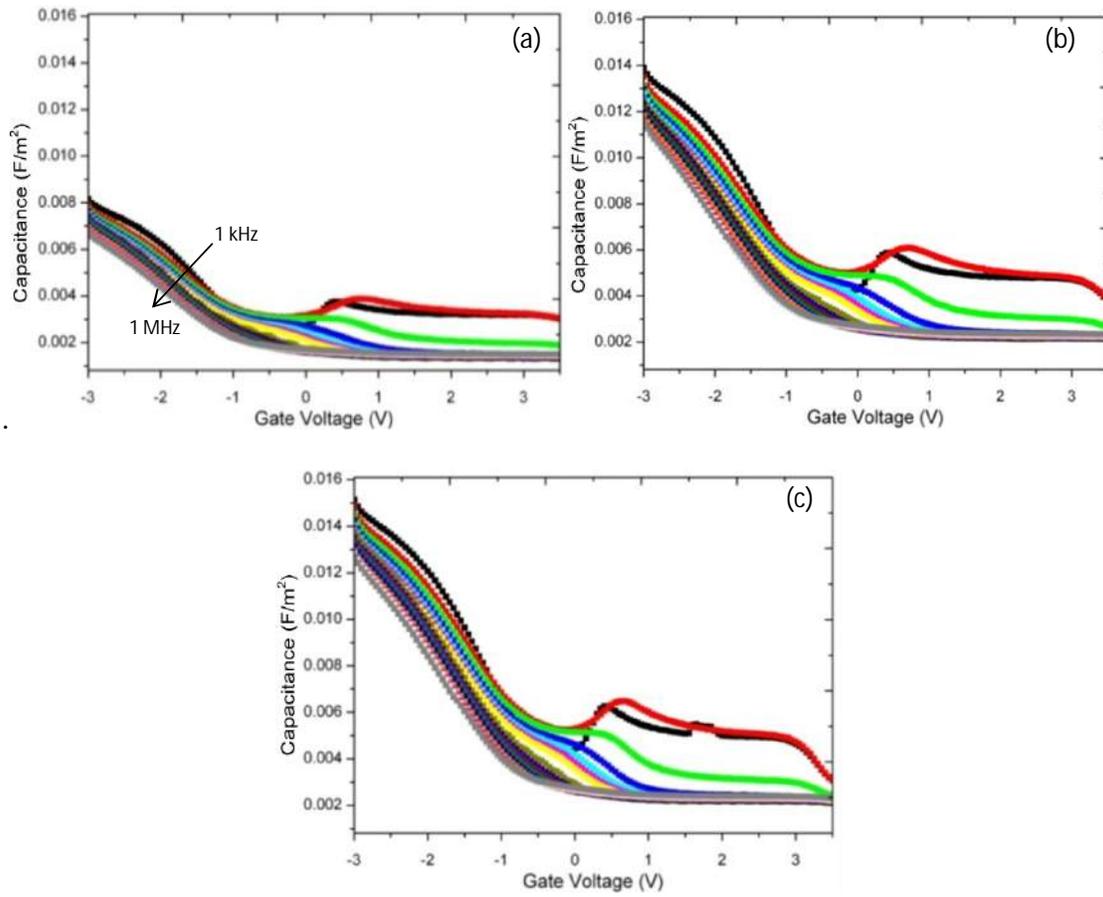


Fig. 6.12: Multi-frequency (1 kHz-1MHz) C-V for p -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As capacitors with hafnia layers grown at a) 240 °C, b) 270 °C and c) 300°C

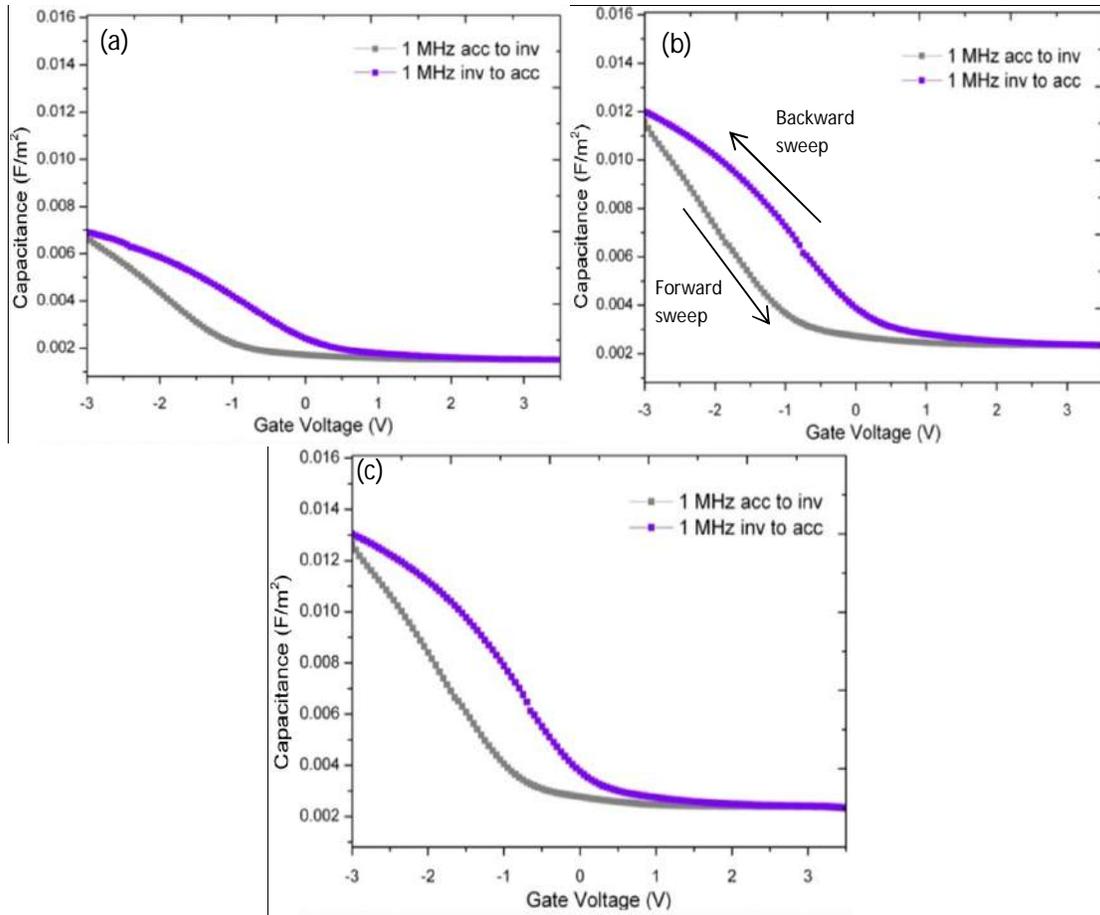


Fig. 6.13: Hysteresis for p -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As films with sweeps from accumulation to inversion shown in grey and corresponding sweeps from inversion to accumulation shown in purple, grown at a) 240°C Δ flatband capacitance not reached, b) 270°C Δ 0.55V and c) 300°C Δ 0.75V

6.5 Electrical characteristics of 1.05nm EOT bilayer structures

6.5.1 Experimental methodology

Deposition of oxide layers was carried out on a Cambridge Nanotech Fiji F200LLC system, aluminium oxide was deposited at 300°C to form an ICL of nominal 1nm thickness, hafnium

oxide was deposited from TDMAH at 300°C to a nominal thickness of 3nm, to form bilayer structures. All other methodologies carried out were the same as previously covered in section 6.1.

6.5.2 Electrical characteristics of *n*-Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As capacitors

Figure 6.14 displays leakage current density, capacitance voltage and hysteresis curves for 13 measured *n*-Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As capacitors. Samples exhibit a leakage current density of ca. 10⁻⁷ until 1.9V initially and observed to gradually with increase with applied voltage with breakdown events evidenced at 4 – 4.4V (9.75-11 Mv/cm) observed for all measured devices. Observed C-V characteristics display low dispersion in accumulation which is seen to be weakly frequency dependant, which may be caused by the presence of border traps^{11,12}. Dispersion in accumulation is reduced compared to initial bilayer structures. The difference in capacitance between the initial two 1 kHz sweeps the initial sweep in black and the second sweep in red, indicates the presence of charge in deep traps in the system. A small magnitude midgap interface defect response may be evidenced from -0.5V to -1V¹⁴. Minimum calculated capacitance of 0.0023 F/m² is approached however it is not reached at low frequency, which has previously been reported as an indication that some Fermi level pinning is taking place¹⁵. A plateau is seen in the inversion portion of the C-V for higher frequencies, which may be an indication of inversion behaviour. Hysteresis is measured by calculating the theoretical C_{fb} and reading off the V_{fb}, EOT scaled *n*-type samples exhibit a lower hysteresis value of in comparison to initial bilayer structures investigated in 6.3. Typically hysteresis charge ΔQ for scaled capacitors is 6.05 FVm⁻², compared to 30 and 26.5 FVm⁻² for the previous capacitors, an indication of the improved nature of the oxide after deposition optimisation and physical scaling.

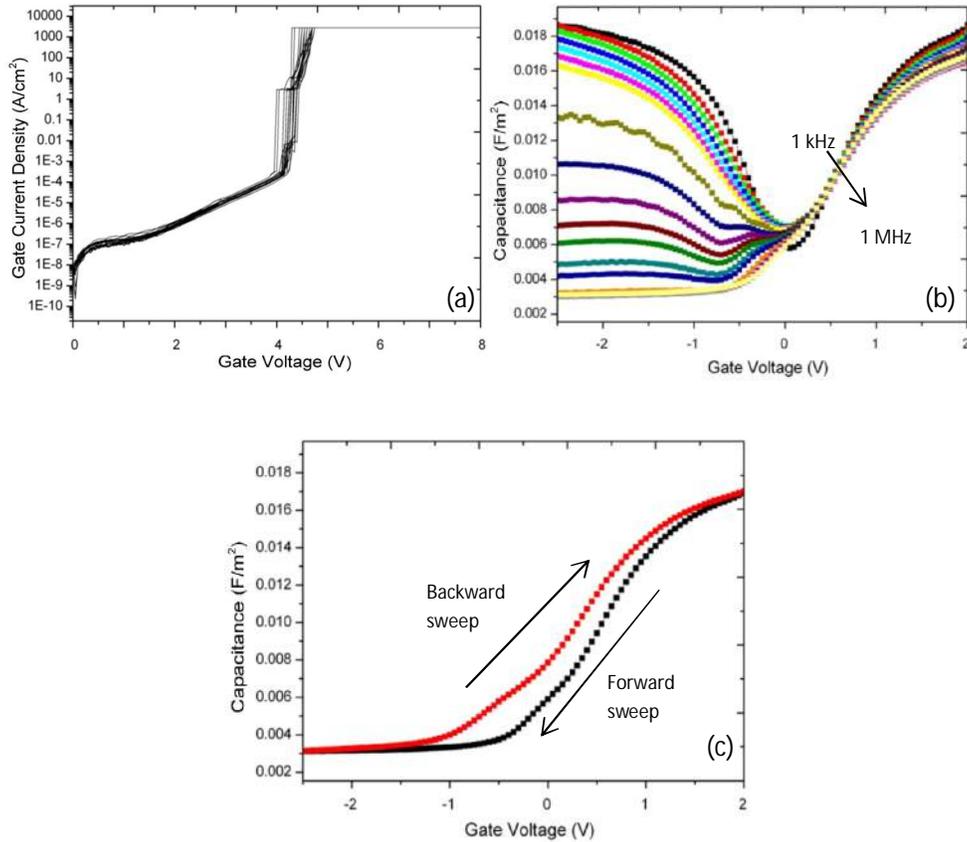


Fig. 6.14: a) I-V characteristics of 13 measured n -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP devices , multi-frequency (1 kHz-1MHz) b) C-V characteristics, c) hysteresis of Δ 0.25V of n -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks grown at 300°C with sweeps from accumulation to inversion in black and the corresponding inversion to accumulation sweep in red

6.5.3 Electrical characteristics of p -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As capacitors

Figure 6.15 displays leakage current density, capacitance voltage and hysteresis curves for 12 measured - Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As capacitors. Samples exhibit a leakage current density of ca. 10⁻⁷ Acm⁻² initially until 1.75V, followed by a large increase in leakage current density with applied voltage, an indication of Fowler-Nordheim tunnelling is taking place

until breakdown events are observed between 5.2 and 5.6V (12.5-14 Mv/cm). Observed C-V characteristics display low dispersion in accumulation which is seen to be weakly frequency dependant, which may be caused by the presence of border traps^{11,12}. Minimal difference in the capacitance of both 1 kHz sweeps displayed in black and red respectively indicates in contrast to *n*-type samples a lack of charge in deep traps. A midgap interface defect response may be evidenced from 0.25V to 0.75V. Minimum calculated capacitance of 0.0023 F/m² is approached but is not reached at low frequency, an indication that some Fermi level pinning may be taking place¹⁵. Hysteresis is measured as 350mV an improvement over devices previously measured in figure 6.3 which had an average hysteresis of 650mV, a diminished hysteresis in comparison to original bilayer structures, an indication of the improved nature of the oxide after deposition optimisation and physical scaling.

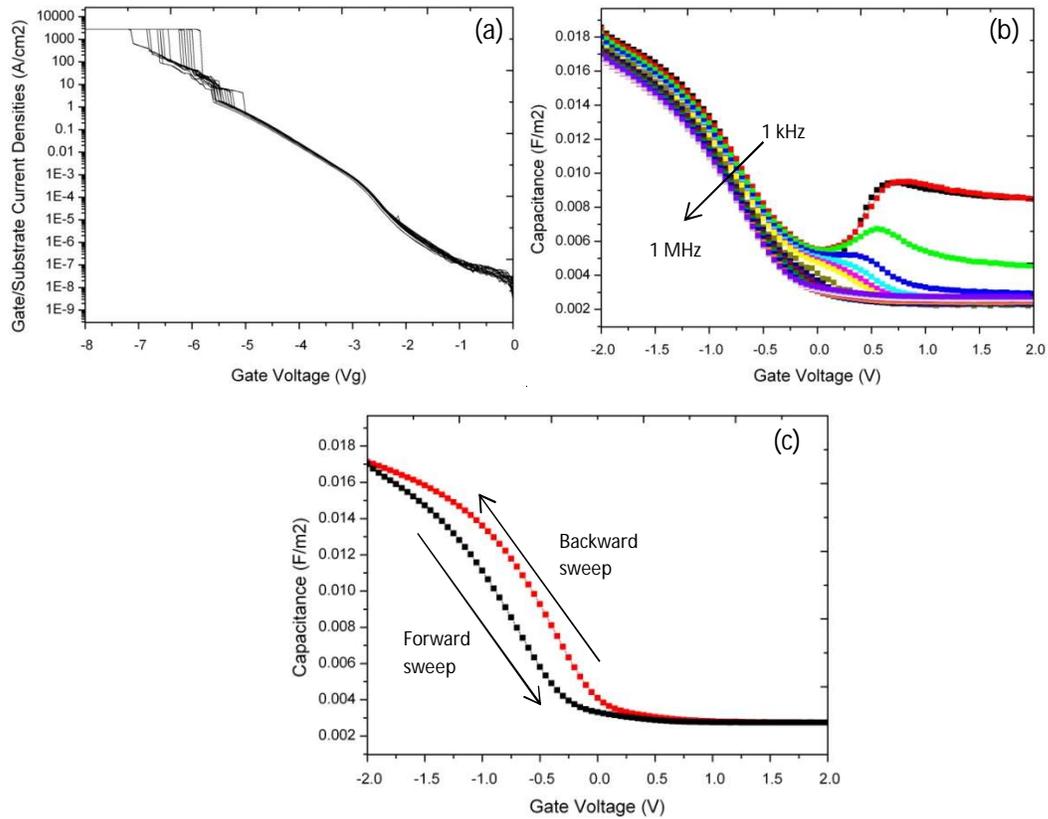


Fig. 6.15: a) I-V characteristics of 12 measured p -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP devices b) multi-frequency (1 kHz-1MHz) C-V characteristic and hysteresis c) $\Delta 0.35$ of p -Au/Ni/HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As MOSCAP stacks grown at 300°C

6.6 Summary and Conclusions

It was found that the use of a thin ~ 1 nm Al₂O₃ layer allows for the use of HfCl₄ as a precursor for the deposition of HfO₂ on III-V substrates. The chloride process was previously thought unsuitable due to possible contamination of films with residual halides leading to large flat band voltage shifts due to the accumulation of Cl⁻ ions at the high- κ /semiconductor interface which is difficult to anneal out of fabricated devices^{5, 18-20}. Some concern is also expressed as frequently HCl or Cl₂ are used to etch the semiconductor surface^{21,22} often and investigations have shown that HCl formation may damage the surface of films being grown³.

While not directly comparable to previously studied capacitors grown from HfCl_4 ²², TDMAH²⁴ and TEMA²⁵ on silicon some comparisons may be drawn. Breakdown voltages for chloride, dimethyl and methylethyl precursors were reported as 2-2.5MV/cm, 3.5-4.5MV/cm and 3.5-3.7MV/cm respectively. In this work with the inclusion of an interface control layer capacitors in this study display breakdown voltages of ca. 5.33-6.63MV/cm for *n*-type amide capacitors and breakdown voltages of 6.57-7.4MV/cm for *n*-type chloride capacitors. *p*-type devices display breakdown voltages of 7.35-8MV/cm for amide capacitors and 8-8.9MV/cm for chloride derived capacitors. This is a possible indication that the use of an interface layer allows for a reduction in leakage current density behaviour irrespective of the precursor used to fabricate the high- κ dielectric, similar to a recent report on the hysteresis of capacitors and the strong influence of the transition from substrate to high- κ interface²⁵. Dielectric constants for hafnia from these studies also varies slightly with values ranging from 11.3²⁴-16.3²⁵ reported. In this study if the TEM thicknesses are assumed to be correct a dielectric permittivity of ~ 19 for hafnia films is assumed for the purposes of calculations.

In contrast to previous work depositing HfO_2 directly on Si substrates indicated that the use of a chloride precursor leaves a native oxide layer^{3,5} and more recent work using TEMA²⁵ directly on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ ²⁶, TEM investigations reveal that there is no apparent oxide layer present for either bilayer sample, indicating that the use of a thin $\sim 1\text{nm}$ Al_2O_3 layer results in a reduction in native oxides through the self-cleaning mechanism and initially prevents any oxygen diffusion to the interface. C-V characteristics for both sets of samples are broadly similar however the thicker HfO_2 layer of the TDMAH furnished sample set leads to diminished electrical characteristics in comparison to the chloride process samples rendering a direct comparison of the samples inaccurate. Both *p*-type samples have strong evidence for inversion behaviour taking place with both amide and chloride process devices exhibit this

behaviour where the G_m/ω peaks occur at approximately the same frequencies as the respective mid-capacitances indicated on the C-V considered to be evidence for inversion behaviour in the Si/SiO₂ system. These characteristics allow us to state that HfCl₄ is a viable precursor for deposition on III-V substrates when used in conjunction with an interface control layer providing electrical characteristics broadly similar to that of amide grown HfO₂ with no obvious deterioration of electrical characteristics from chlorine incorporation or substrate etching from acidic by-products.

Optimisation of the amide deposition temperature yields some inconclusive results; C-V characteristics of devices fabricated seem to exhibit with similar performance to those grown and investigated in section 6.3. For *n*-type samples lowest hysteresis is observed for 300°C deposited samples along with reasonable leakage current densities for all temperatures indicating good dielectric behaviour. However *p*-type samples display an increase in hysteresis for samples grown at 300°C and a larger leakage current density for these samples which generally is attributed to a larger amount of defects in the oxide layer and a poorer interface with the semiconductor.

Further scaling of the bilayer structure towards a 1nm EOT was found to produce favourable results with improved electrical characteristics noted for both *n*- and *p*-type samples and similar D_{it} characteristics to initial samples recorded. Leakage current density of the samples is higher than the $\sim 1 \times 10^{-7}$ A/cm² at a V_{op} of $\pm 2V$ defined by the ITRS²⁷, however leakage current density is close to this figure. C-V characteristics for both samples are well behaved with little dispersion and a plateau in capacitance observed at higher frequencies for *n* C-V characteristics indicate the possibility of inversion taking place. However on both samples low frequency measurements should be carried out to determine the G_m/ω peak to provide

some evidence that the measured conductance reaches a peak and then begins to decline providing some evidence of inversion behaviour.

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Chapter 7: Summary and future work

The initial work presented in this thesis focused on the electrical characterisation of Al_2O_3 films grown from a new amidinate precursor. After an initial growth study on silicon substrates confirmed a growth rate of 1.03\AA at 250°C and 1.08\AA at 300°C . Similar growths were attempted on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates at 250°C and 300°C whereupon a large nucleation delay was observed on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ possibly attributable to native oxides present. TEM investigation revealed that films were ca. 2nm thick for samples which received no surface pre-treatment at either temperature. Samples which have received an ammonium sulphide etch experienced less nucleation delay with film thicknesses $\sim 5\text{nm}$, again thinner than the expected 8nm nominal thickness expected from the growth study on silicon. This reduced nominal thickness reduces the efficacy of Al_2O_3 layers as insulating layers leading to electrical characteristics which are poorer than expected.

The second aim of this work was to investigate the effects of precursor pre-pulsing for the removal of native oxides from III-V substrates to improve the high- κ interface. The application of TEG pre-pulsing was observed to not significantly degrade leakage current density with some cross wafer uniformity observed and to improve the C-V response marginally for $\text{Au/Ni/Al}_2\text{O}_3/\text{GaAs}$ devices. However similar experiments using TEG pre-pulsing on an $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrate does not replicate these electrical characteristics with samples exhibiting an increased leakage current density, reduced maximum capacitance and some degradation of the midgap D_{it} C-V characteristics. This behaviour is observed again when TMI is pre-pulsed on InP substrates before Al_2O_3 deposition with an increased leakage current density again observed with large leakage current density quickly saturating observed for all pre-pulse treated samples. The observed electrical degradation of samples is an indication that the pre-pulsing of precursors similar to TMA does not result in clean-up reactions analogous to that of TMA and the standard TMA/water process is still the most favourable.

The third focus of this work was the modification of the semiconductor surface in-situ to avoid air exposure and consequential native oxide regrowth. In-situ plasma treatment of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates prior to the deposition of Al_2O_3 provides improved electrical characteristics compared to not using any additional form of surface pre-treatment before the deposition of Al_2O_3 from TMA and water however there appears to be a concurrent increase in fixed charge in the film. The use of an in-situ plasma treatment in conjunction with an ex-situ ammonium sulphide etch was determined to degrade electrical characteristics possibly due to increased surface roughening causing carrier scattering or depletion of the group V element from the semiconductor surface.

The use of an in-situ ammonium sulphide etch on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates prior to deposition of Al_2O_3 was determined not provide sufficient surface etching and passivation compared to the ex-situ aqueous process. The large leakage current density, dispersion in accumulation and D_{it} hump are all indicative of insufficient removal of native oxides from the semiconductor surface and a poor interface. However some dependence on pulse duration was observed during these experiments, an indication that it may be possible to tune the process if the dose of sulphur and condensation in delivery lines can be controlled.

Finally the fourth aim of this work was to incorporate an interface control layer of Al_2O_3 as a modifying layer between the $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface and a comparison made between the deposition of HfO_2 from the silicon industrial standard HfCl_4 precursor and the TDMAH precursor. The use of a ca. $\sim 1\text{nm}$ ICL of Al_2O_3 was shown to provide sufficient improvement to the interface allowing the achievement of reasonable electrical characteristics using either precursor importantly allowing the use of HfCl_4 on III-V materials with no degradation for the first time. HRTEM studies indicate that the Al_2O_3 interlayer for samples furnished from the HfCl_4 process is $\sim 0.1\text{nm}$ thinner than the corresponding TDMAH process, possibly

attributable to the formation of HCl as a by-product during the deposition etching the ICL. Total thicknesses for grown samples was 1.1nm Al₂O₃ 5.8nm HfO₂ for samples from the HfCl₄ process with 1.2nm Al₂O₃ and HfO₂ 6.8nm from the TDMAH process with abrupt interfaces and no native oxide observed for either sample. A direct comparison of electrical characteristics is not possible; however both samples realise functioning capacitors with relatively low midgap D_{it} of 2-4 10¹² cm⁻² eV⁻¹ for the majority of samples measured by the conductance method. Optimisation of the TDMAH process indicates that growth of hafnia films at higher process temperatures leads to less electrical defects, manifested as a reduced D_{it} hump, a reduction in frequency dispersion, generally attributable to border traps and less hysteresis in C-V characteristics. EOT scaled samples display well behaved C-V behaviour.

7.1 Suggestions for future work

Any future work carried out with the new acetamidinate precursor should allow for a surface treatment to remove native oxides from III-V semiconductors before growth of dielectric films and to allow sufficient thickness for electrical assessment of the dielectric properties.

TEG pre-pulsing on GaAs surfaces should be repeated to ensure reproducibility of the results. If a consistent improvement in electrical characteristics is observed an in depth study of the use of TEG pre-pulse treatment in conjunction with an Al₂O₃ interlayer to improve the function of fabricated Ga-MOS capacitors should be undertaken in conjunction with a comprehensive microscopy study to determine if TEG pre-pulsing forms a layer of gallium oxides at the interface.

In-situ plasma studies may be repeated to fine tune the plasma treatment time and reduce surface roughening. Large-scale AFM studies may have to be undertaken to determine the magnitude of surface roughening taking place with respect to plasma power and exposure time. AFM studies may also confirm if group V element evolution is taking place after

plasma surface treatment. Experiments to investigate the effects of the order of surface treatments should be undertaken to determine if plasma treatment is more effective before or after ammonium sulphide surface passivation. Sulphur in-situ treatments may be tuneable as samples exhibit some variability in electrical characteristics based on pulse duration. There is also a need to resolve the issue of exhaustion of sulphur from the solution during deposition and optimisation of the passivation time and temperature.

Examination of the bilayer capacitor structures would benefit from further investigation which makes use of AFM to determine if any surface roughness is caused over large areas using the chloride precursor though interfaces appear abrupt and well defined from high resolution micrographs. Further studies to determine if any chlorine is incorporated into the gate stack and if so to determine if it is concentrated at the interface between the high- κ and semiconductor interface.

Further EOT scaling of the bilayer process would be worthwhile to determine the efficacy of the ICL process for scaled MOS structures. Further electrical characterisation would be worthwhile to ensure there is no significant impact from the use of the HfCl_4 process when depositing reduced thickness stacks. A post deposition anneal of capacitors could also improve the high- $\kappa/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface by passivation of Al^+ dangling bonds allowing for the realisation of lower overall D_{it} values. To confirm true inversion behaviour is taking place for EOT scaled samples a further sample set is required for the determination of activation energy. C-V and G-V plots may be performed at varying temperatures to facilitate the utilisation of an Arrhenius plot in order to extract the minority carrier activation energy; which determines the transition from a generation recombination regime to a drift-diffusion response considered definitively characteristic of inversion behaviour. It is possible the bilayer structure may be transferred to a basic MOSFET structure to investigate if the

favourable MOSCAP characteristics are transferrable as has previously accomplished for optimised Al₂O₃ capacitors.

Appendix A - Sample Calculations

k = Boltzmann's Constant = $1.38 \times 10^{-23} \text{J K}^{-1}$

T = temperature in Kelvin

q = electronic charge = $1.6 \times 10^{-19} \text{C}$

$\epsilon_0 = 8.854 \times 10^{-14} \text{ F/cm}$

$\epsilon_s = 13.77$ for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$

n_i = intrinsic carrier concentration @ 300K = $1 \times 10^{12} \text{ cm}^{-3}$

N_d = extrinsic doping = $4 \times 10^{17} \text{ cm}^{-3}$

1) Calculate the theoretical oxide capacitance (C_{ox})

$$C_{ox} = \frac{\epsilon_0 k}{T_{ox}}$$

For a typical sample with 8nm Al_2O_3 , $C_{ox} \sim 0.00952 \text{ F/m}^2$.

2) Calculation of minimum C-V capacitance C_{min}

For an n -type substrate: the minimum capacitance occurs in depletion when the depletion width is at its maximum, and the surface is as p -type as the bulk is n -type, satisfying

$$x_d = x_{d \max} \quad \text{and} \quad \Phi_s = 2\Phi_b$$

with

$$\Phi_s = \frac{qN_d x_{d \max}^2}{2\epsilon_0 \epsilon_s}$$

$$\Phi_b = \frac{kT}{q} \ln\left(\frac{N_d}{n_i}\right)$$

For $\Phi_s = 2\Phi_b$ and rearranging:

$$x_{d \max}^2 = \frac{4\epsilon_0 \epsilon_s}{q^2 N_d} kT \ln\left(\frac{N_d}{n_i}\right) = 50 \text{ nm}$$

$$C_{\min \text{ substrate}} = \frac{\epsilon_0 \epsilon_s}{x_{d \max}} = 0.0024 \text{ F/m}^2$$

where $C_{\min \text{ substrate}}$ is the minimum $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ capacitance contribution. The measured flatband capacitance is then the series combination of the dielectric and the substrate capacitances:

$$C_{\min} = \frac{C_{ox} C_{\min \text{ substrate}}}{C_{ox} + C_{\min \text{ substrate}}}$$

where C_{ox} is the measured oxide capacitance in accumulation.

3) Determine the flatband Voltage V_{fb} from Measured C-V

The flatband voltage is obtained by calculating the theoretical capacitance at which the flatband condition is true, and then using the capacitance voltage curve to obtain the V_{fb} value. The minimum substrate capacitance occurs in depletion when the depletion width L_D is at its maximum. The measured minimum capacitance is then the series combination of the dielectric and the substrate capacitances.

$$L_{D\text{InGaAs}} = \sqrt{\frac{\epsilon_0 \epsilon_s kT}{q^2 N_d}} = 6.7 \times 10^{-9} \text{ m}$$

$$C_{\text{InGaAsfb}} = \frac{\epsilon_0 \epsilon_s}{L_{D\text{InGaAs}}} = 0.0182 \text{ F} / \text{m}^2$$

$$C_{fb} = \frac{C_{ox} C_{\text{InGaAsfb}}}{C_{ox} + C_{\text{InGaAsfb}}} = 6.25 \times 10^3 \text{ F} / \text{m}^2$$

Two important assumptions here are that N_d the nominal doping is the current doping of the semiconductor and the measured capacitance voltage curve does not have a significant capacitive contribution due to the presence of interface states. The reading off of V_{fb} should be done from the low temperature high frequency curve where possible.

4) Determination of D_{it}

After reading off the flat band capacitance for both for both n and p -type capacitors and calculating C_{ox} the final expression for D_{it} is:

$$V_{fbn} - V_{fbp} = \frac{0.668 + qD_{it}}{C_{ox}}$$

0.668 derives from the difference in Fermi level energy in bulk n and p -type semiconductors

Position of Fermi Level in Bulk

$$\Phi_b = \frac{kT}{q} \ln\left(\frac{N_d}{n_i}\right)$$

$$\text{N Type} \rightarrow E_f = \frac{E_g}{2} + \Phi_b = 0.375 + 0.334 = 0.709 \text{ i.e. near the CB}$$

$$\text{P Type} \rightarrow E_f = \frac{E_g}{2} - \Phi_b = 0.375 - 0.334 = 0.041 \text{ i.e. near VB}$$

This assumes that Φ_b is the same for both semiconductors i.e. both have the same level of doping.

This analysis is adapted from

Journal of the Electrochemical Society, 158 (5) G103-G107 (2011)

Appendix B – Additional TEM images of bilayer structures

Figure 1 presents a low magnification cross sectional TEM micrograph of HfCl₄ furnished HfO₂ samples to provide an overview of sample structure. The InGaAs channel is measured at 2.2μm. and found to be defect free with some striations observed on the surface from focused ion beam milling.

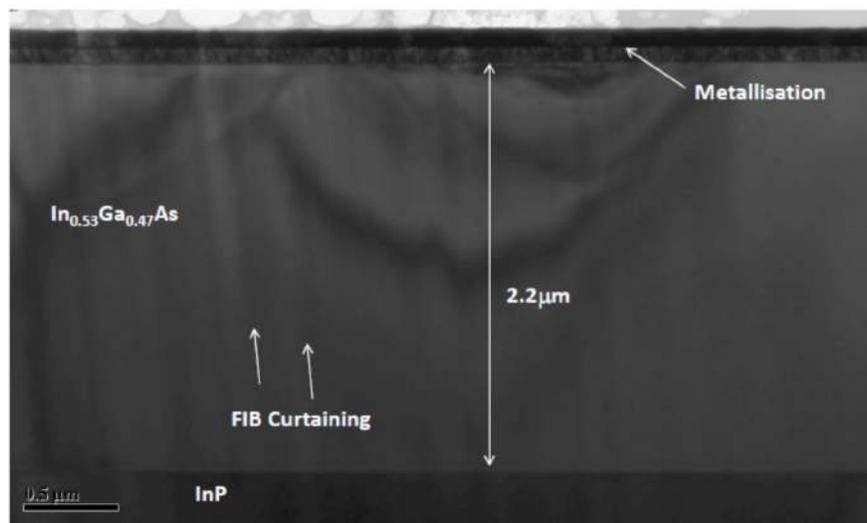


Fig. 1: Low magnification cross sectional transmission electron micrographs a sample grown in the applied materials chamber displaying the InGaAs channel, InP substrate and dual metallisation layer to create electrical contacts.

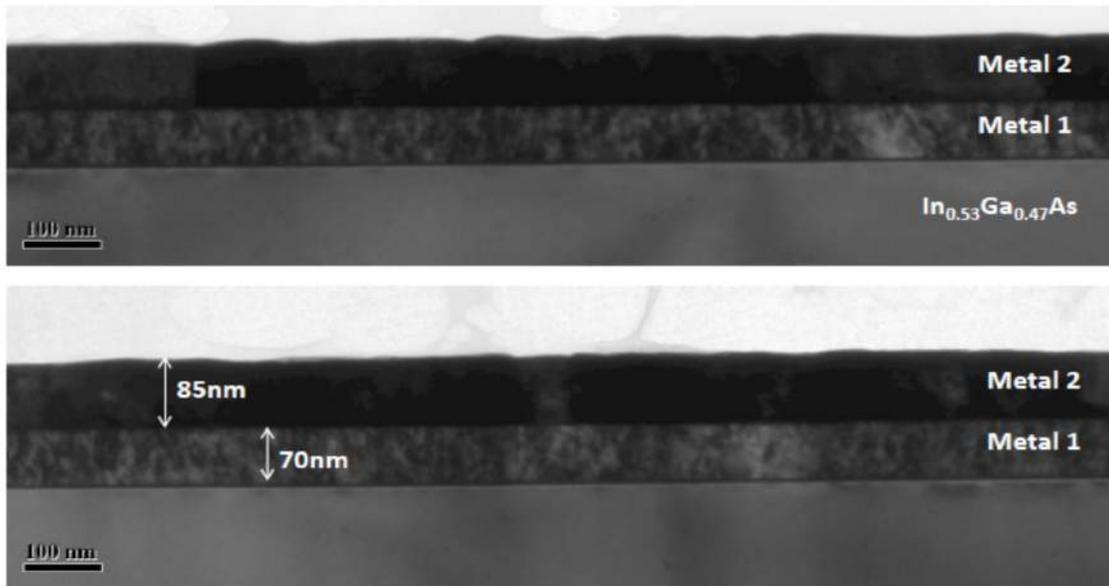


Fig. 2: An intermediate magnification TEM micrograph displaying the dual metal metallisation layer for HfCl₄ grown samples with a total thickness of 155nm

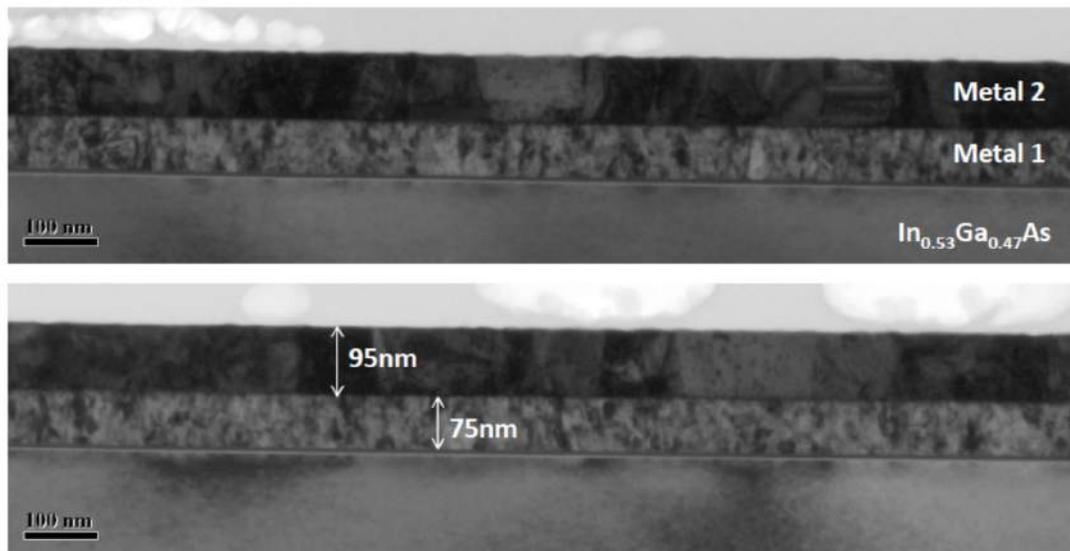


Fig.3: An intermediate magnification TEM micrograph displaying the dual metal metallisation layer for TDMAH grown samples with a total thickness of 165nm

It is noted that the gold top metallisation layer possess' a coarser grain microstructure with a combined thickness of 155nm for the Ni:Au top contact for samples grown in the Applied Materials chamber and a thickness of 165nm for samples grown in the Nanotech chamber with similar structural characteristics for samples grown in the Cambridge Nanotech.

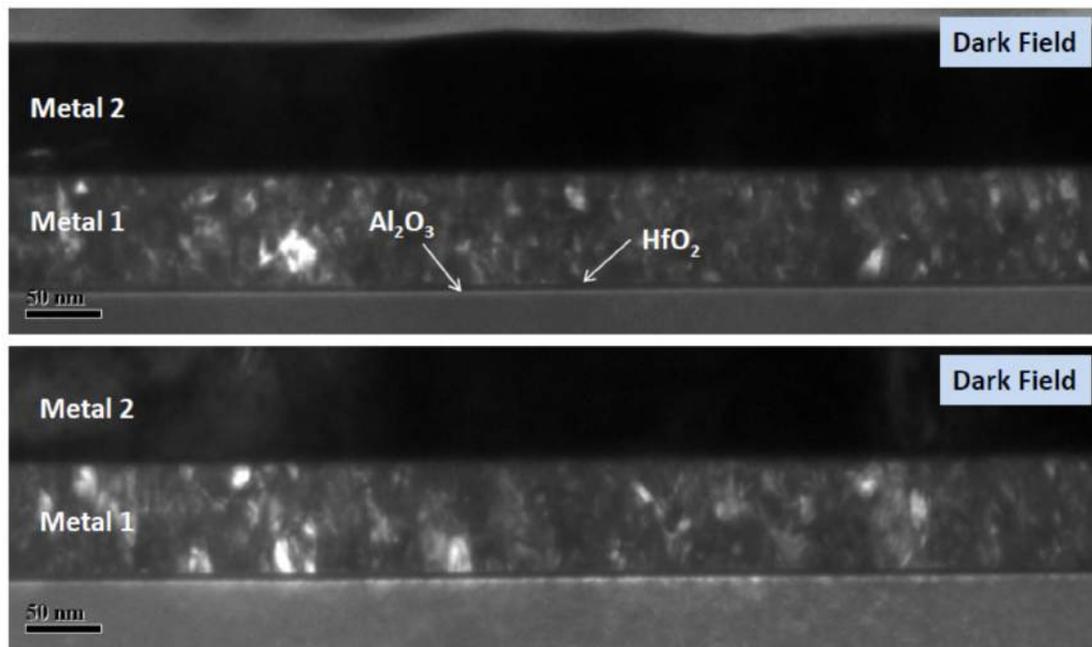


Fig. 4: Dark field images of HfCl₄ grown samples displaying fully amorphous layers, the bottom image displays some interface strain

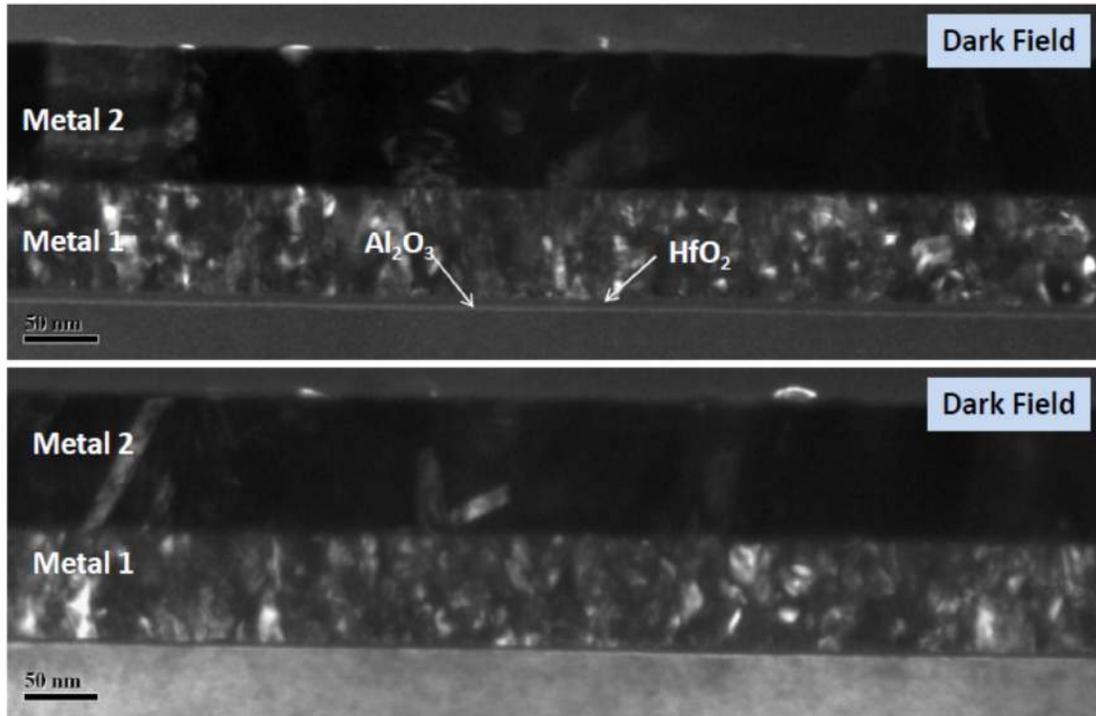


Fig. 5: Dark field images of TDMAH grown samples displaying fully amorphous layers, in contrast to other samples no substrate strain is obvious.

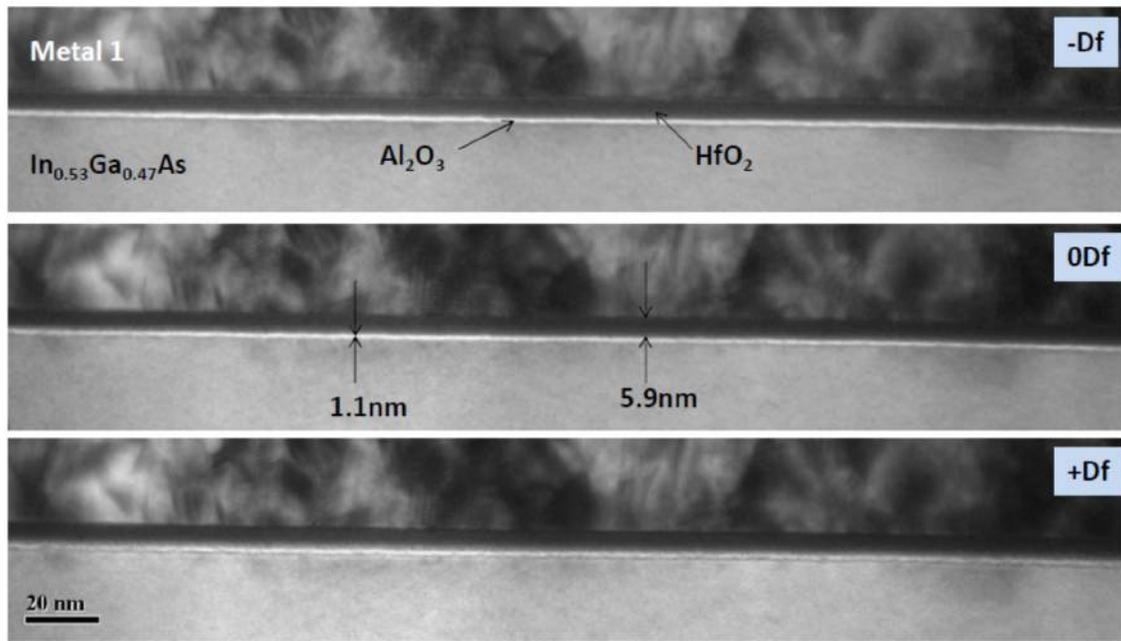


Fig. 6: Bright and Dark field images of HfCl_4 grown samples displaying the thickness of metal oxide layers measured.

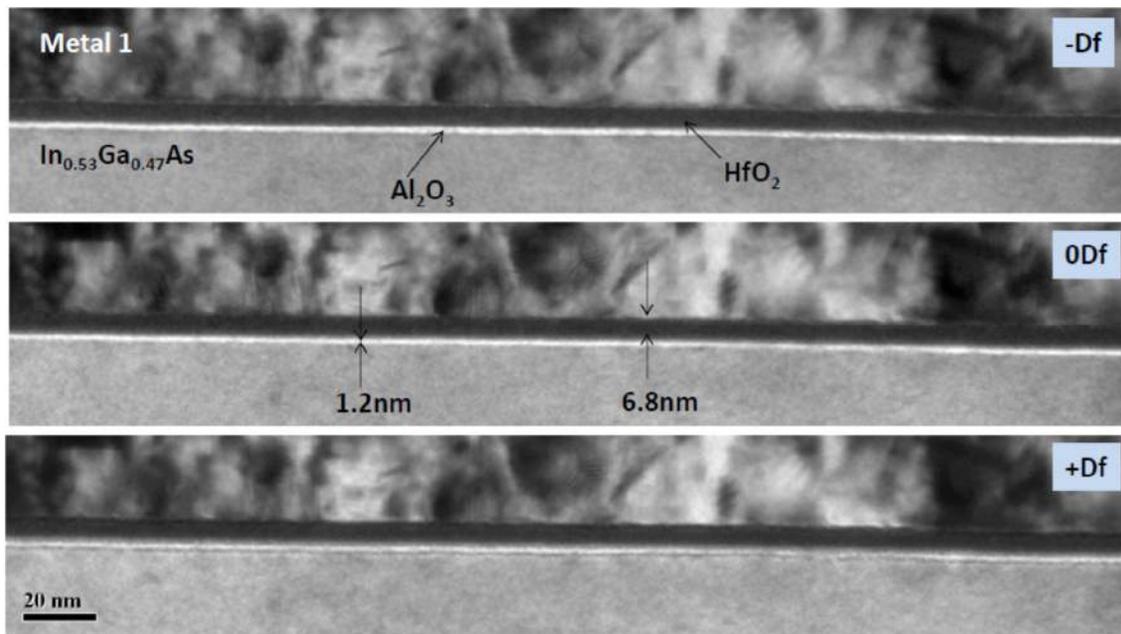


Fig. 7: Bright and Dark field images of TDMAH grown samples displaying the thickness of metal oxide layers measured.