Organo-arsenic molecular layers on silicon for high density doping

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Abstract

This article describes for the first time the controlled monolayer doping (MLD) of bulk and nanostructured crystalline silicon with As at concentrations approaching 2×10^{20} atoms cm^{-3}. Characterization of doped structures after the MLD process confirmed that they remained defect and damage free, with no indication of increased roughness or a change in morphology. Electrical characterization of the doped substrates and nanowire test structures allowed determination of resistivity, sheet resistance and active doping levels. Extremely high As-doped Si substrates and nanowire devices could be obtained and controlled using specific capping and annealing steps. Significantly, the As-doped nanowires exhibited resistances several orders of magnitude lower than the pre-doped materials.

Introduction

Controlled doping of electronic devices at the nanoscale is challenging, especially as devices transition from planar to non-planar architectures, requiring innovative methods to reliably and reproducibly dope with extremely fine control and conformality.[1-2] Conventional dopant technologies, such as ion implantation, are problematic for advanced non-planar devices, *e.g.* fin field effect transistors (finFET) due to the intrinsically high-energy nature of the bombardment process at the surface.[3] There are a number of disadvantages associated with ion implantation, including the difficulty in obtaining an abrupt implantation layer on a nanometre scale, poor control over the spatial distribution of implanted ions and often severe damage to the crystal lattice of the semiconductor. Additionally, the source gases used in ion implantation are also invariably harmful from a health and environmental perspective.[4]

An alternative approach to ion implantation is spin-on doping, which consists of depositing a dopant-containing solution onto a semiconductor surface, followed by a diffusion anneal step.

Compared to ion implantation, spin-on doping is a non-destructive and simple technique, but there are still issues associated with this approach ranging from a lack of uniformity and dose control over large areas of the substrate.[5] Additionally, residues left over from the solvent containing the dopant precursor are not easily removed from the surface.[6] Plasma doping is an emerging and promising technique due to the suppression of crystalline defect formation and the realisation of nanoscale devices with reproducible electrical characteristics.[7] The doping profiles with plasma approaches are generally more conformal than those achieved using ion implantation, however some crystal damage can still occur and problems can still be encountered when attempting to dope with multiple species at different energies in a single process.[8] Research is also continuing on the integration of dopants during nanomaterial fabrication and synthesis. This *in-situ* method of doping nanomaterials is promising but the challenges of scale-up and large scale integration in addition to the problematic concentration gradients still remain.[9]

Recently, a facile approach for controllable doping of semiconductor nanostructures was introduced, termed monolayer doping (MLD).[10] MLD comprises two steps: i) functionalization of the semiconductor surface with a p- or n-dopant containing molecule and ii) thermal diffusion of those dopant atoms into a semiconductor by a rapid thermal anneal (RTA) step. MLD has been applied to a large variety of nanostructured materials fabricated by either the "bottom-up" or "top-down" approaches. The self-assembled monolayers are formed using self-limiting reactions, commonly a hydrosilylation reaction between a hydrogen-terminated surface and a labile C=C site on the dopant containing molecule. The surface chemistry of Si is well known and established, leading to a variety of methods with which to passivate and functionalise the surface.[11–17] MLD is extremely flexible as the surface preparations, molecular footprints, capping layer and also the thermal treatment

parameters can all be finely tuned to optimise surface coverage of the molecule and diffusion of the dopant into the semiconductor surface, in addition to its ease of application to both "bottom-up" and "top-down" materials.

MLD has been demonstrated successfully using boron and phosphorus-containing molecules on bulk crystalline silicon substrates enabling the formation of sub-5 nm ultra-shallow junctions in conjunction with conventional spike annealing.[18] The technique has also successfully been applied to the doping of InAs materials and InP photovoltaics using sulfur containing monolayers.[19] MLD has also been successfully used in conjunction with nanoimprint lithography to control the lateral positioning of the molecular monolayers using selective patterning steps.[20] A variation of the MLD process, termed monolayer contact doping (MLCD), has been demonstrated for the controlled doping of Si wafers where a donor substrate functionalized with the dopant-containing monolayer is placed in contact with an acceptor substrate and annealed together. The MLCD process has been shown on bulk Si substrates and a number of Si nanowire devices.[21] More recently, Hoarfrost and co-workers demonstrated a type of MLD involving spin-on organic polymer dopants in an attempt to bridge the MLD technique and conventional inorganic spin-on dopants. Compared to traditional spin-on dopants, these polymer based spin-on dopants may be easier to remove post-anneal. [22] Most recently, Puglisi *et al* reported an application of the MLD process to arrays of Si nanowire based solar cells, achieving electrical data that proved promising for the next generation of solar cell devices.[23] These examples show the great flexibility that the MLD process has for different materials.

In this article we report for the first time the successful doping of Si using organo-arsenic molecular monolayers. Extremely high dopant concentrations, up to 2×10^{20} dopants cm^{-3}

were achieved. We also report the successful application of the technique to a number of Si nanowire devices of varying sizes down to 20 nm in width highlighting that the process leads to effective doping of nanostructures without the formation of defects or changes in nanowire morphology. These devices also display excellent electrical characteristics with significant decreases observed in their resistivity when compared to the undoped devices.

Experimental

Arsenic trichloride, anhydrous diethyl ether, stabilized deuterated chloroform and mesitylene were purchased from Acros Organics. Mesitylene was dried, distilled from calcium hydride and stored over molecular sieves before use. All other chemicals were used as received without further purification. Allylmagnesium bromide was purchased from Sigma-Aldrich and used as-received. All chemical manipulations were carried out under strictly anaerobic conditions in an atmosphere of ultra-high purity argon from Air Products Inc. using a combination of Schlenk apparatus and an inert-atmosphere glovebox. SEM imaging was carried out on an FEI Quanta FEG 650 microscope operating at 5 - 10 kV. TEM images were acquired on a JEOL 2100 HRTEM microscope operating at an accelerating voltage of 200 kV. XPS spectra were acquired on an Oxford Applied Research Escabase XPS system equipped with a CLASS VM 100 mm mean radius hemispherical electron energy analyser with multichannel detectors in an analysis chamber with a base pressure of 5.0×10^{-10} mbar. Survey scans were recorded between 0-1400 eV with a step size of 0.7 eV, dwell time of 0.5 s and pass energy of 100 eV. Core level scans were acquired with a step size of 0.1 eV, dwell time of 0.5 s and pass energy of 20 eV averaged over 10 scans. A non-monochromated Al-kα X-ray source at 200 W power was used for all scans. All spectra were acquired at a take-off angle of 90° with respect to the analyser axis and were charge corrected with respect to the C

1s photoelectric line. Data was processed using CasaXPS software where a Shirley background correction was employed and peaks were fitted to Voigt profiles.

Synthesis of Triallylarsine

Triallylarsine (TAA) was synthesised according to literature procedures. [24–26] A reaction scheme for this synthesis showing the structure of the molecule is shown in **Figure S1** in Supporting Information. Briefly, allylmagnesium bromide (138.5 ml, 138.5 mmol) was set to stir in a three-neck round bottom flask. To one arm was attached a coil condenser with an argon inlet. A pressure-equalising addition funnel containing arsenic trichloride (5.0g, 2.3 ml, 28 mmol) in anhydrous diethyl ether (25 ml) was attached to the middle arm and the remaining arm was stoppered. The arsenic trichloride solution was added to the Grignard reagent at 0 °C over a period of 30 min under vigorous stirring. On completion of the arsenic trichloride addition, the reaction was left to warm to room temperature for a further 30 min and was then heated to reflux for 2 h. The reaction was once more cooled to 0 °C after 2 h and a deoxygenated, saturated solution of NH_4Cl at 0 °C was added very slowly to neutralise remaining Grignard reagent. The mixture was filtered into a large separating funnel and the organic phase was extracted with a 25 ml portion of diethyl ether. The aqueous phase was washed separately with 3 × 25 ml portions of diethyl ether and the washings were combined with the organic phase. The organic phase was dried with granular magnesium sulfate and filtered into a round-bottom flask. Excess diethyl ether was removed by rotary evaporation and the oily residue was distilled twice using a Kugelrohr short path distillation apparatus.

General Procedure for Si Substrate Functionalization

All glassware was cleaned with a piranha wash, dried in an oven overnight at 130 °C and allowed to cool under a stream of dry Ar on the Schlenk line. TAA was dissolved in

mesitylene (5 ml) to make up a 2.5 % v/v solution. The solution was degassed and dried using several freeze-pump-thaw cycles and left to purge under a positive pressure of argon while the substrate was being prepared. A 1.5 cm^2 sample of Si was degreased, cleaned by standard RCA washes and immersed in a 20 % solution of hydrofluoric acid to remove surface oxide and metal contaminants and to induce H-passivation of the surface. The substrate was dried under a stream of dry nitrogen and placed immediately into a two neck round bottom flask under argon to prevent re-oxidation of the surface. The TAA solution was then cannulated under positive pressure of Ar into the flask containing the H-passivated Si substrate. The flask was then heated up to 180 °C under argon and left for 2 h at reflux, maintained by means of a thermocouple temperature feedback controller. The color of the solution was monitored over the course of 2 h. After the reaction had completed the substrate was removed from the vessel and immediately immersed in a vial of anhydrous toluene and sonicated to remove any physisorbed species. The sample was rinsed in a vial of fresh anhydrous toluene and sonicated in successive vials of anhydrous toluene, dichloromethane and ethanol with careful drying in a N_2 stream between each vial. The sample was kept under an inert atmosphere before removal for further processing and characterization. A schematic showing the MLD process applied here is shown in **Figure 1**

Fabrication of Nanowire Test Devices

The silicon-on-insulator (SOI) substrates were patterned using a Raith e-Line Plus electron beam lithography (EBL) system. The substrates were patterned using hydrogen silesquioxane (HSQ) (Dow Corning Corp) as the resist. The top Si layer thickness was approximately 50 nm. The substrates were firstly degreased by sonication successively in acetone and isopropylalcohol (IPA) solvents and blown dry in a stream of N_2. Following a bake at 120 °C for 5 min a 1:2 concentration solution of HSQ in methylisobutyl ketone

(MIBK) was spun on the substrates at 2000 rpm for 33 s, giving a HSQ film approximately 50 nm thick on any substrate. The substrates were again baked at 120 °C for 3 min prior to EBL exposure. EBL exposure was a two-step process where the first lithography step was carried out to pattern only the high resolution fin structures. In the second step the contact pads for the four probes were exposed. To attain a highly focused beam for the first step, a 10 kV beam voltage and 100 μm write-field was chosen. To avoid a large exposure time, the low resolution contact pads were written with 1 kV beam voltage and 400 μm write-field. After the EBL exposures, the substrates were developed in a solution of 0.25 M NaOH and 0.7 M NaCl for 15 s followed by 60 s rinse in DI water and a 15 s immersion in IPA. For the second lithography step, HSQ was spun onto the substrate with the aforementioned parameters and then exposed. A SEM micrograph of the test device is shown in **Figure S4** in Supporting Information. To transfer the HSQ pattern onto the top Si layer of the SOI substrates, they were subjected to a reactive ion etch (RIE) using Cl_2 chemistry in an Oxford Instruments Plasmalab 100 system.

Carrier Profiling

SIMS analysis was carried out at the INSA Toulouse using a CAMECA IMS 4F6 spectrometer with a Cs^+ source at 2 kV accelerating voltage and beam current of 20 nA. This low energy mode was used to analyse the composition of the sample close to the surface of the sample where the diffusion process in MLD is most effective. SIMS analysis was benchmarked using known calibration standards and samples. ECV profiling was carried out on a WEP Control CVP21 Wafer Profiler using 0.1 M ammonium hydrogen bifluoride as the etchant. Scanning parameters were automatically controlled by the instrument by selecting the appropriate sample type, layer map and etchant combination. Error did not exceed 15% for ECV analysis.

Results and Discussion

Silicon Functionalization

Initial experiments were performed on bulk crystalline silicon substrates to ensure the process could be applied successfully for the material, to develop an experimental procedure for MLD and also to perform carrier profiling and SIMS profiling that is not possible at nanoscale feature sizes.

Figure 2(a) shows a high-resolution XPS Si *2p* scan of a freshly cleaned and etched Si substrate with the inset depicting the surface after preparation. The absence of any detectable oxide features in the XP spectra indicated the presence of a close to pristine, oxide-free substrate surface necessary for MLD. **Figure 2(b)** shows an XPS survey scan of a Si substrate freshly functionalized with TAA molecules; the As *2p* and *3d* photoelectric lines are shown. The binding energy of the Si *2p* core level scan of the functionalized sample, shown in **Figure 3(a),** exhibits primarily the non-oxidised elemental peak at 99.8 eV, indicating a passivated surface which consists mainly of Si-C bonds. There is a very small presence of oxide at the higher binding energy of 103 eV[27] suggesting limited oxygen uptake during air exposure during transport to the UHV equipment. Note that the sample was transported under a positive pressure of Ar and introduced to the nitrogen-purged environment of the XPS instrument with less than 5 s of contact with air. The As *3d* spectrum acquired from the same substrate is shown in **Figure 3(b)**. The elemental As peak is shown at 42.0 eV [28] with a second peak chemically shifted to a higher binding energy of 44.8 eV. This binding energy and the chemical shift of 2.8 eV with respect to the elemental As component is consistent with the presence of an oxidised arsenic species on the surface of the substrate post-functionalization and may be attributed to oxidation of the TAA molecule in air post-reaction.[29] Again, sample exposure to air was minimized as much as possible. The atomic

percentages of the elemental As and oxidised As components were determined to be 28 % and 72 % respectively. To determine if the Si oxide peak shown in **Figure 3(a)** was associated with post-functionalization oxidation or the functionalization process itself, a blank, non-functionalized Si sample was exposed to ambient conditions for 24 h and analysed by XPS. The amount of oxide observed was very similar to that obtained for the functionalized sample after a 2 h functionalization procedure. This was observed despite several freeze-pump-thaw cycles being performed on the dopant molecule solution to remove traces of oxygen and water. The presence of this trace amount of oxide did not appear to have an appreciable effect on the dopant diffusion process.

Stability of Functionalized Samples toward Ambient Conditions

The stability of the underlying Si surface toward reoxidation is important. Regrowth of the oxide prior to rapid-thermal-anneal treatment and subsequent processing steps is undesirable. Functionalized Si is known to be more resistant to re-oxidation than non-functionalized Si.[30] To determine the resistance to re-oxidation of the underlying silicon substrate post-functionalization, a functionalized sample was left in ambient conditions for periods of time ranging from 24 h to one month and the XPS Si *2p* core level was used to determine the stability of the functionalized sample relative to a piece of unfunctionalized Si. The components corresponding to silicon oxides were monitored and recorded. The acquired stability spectra for the functionalized samples are shown in **Figure S2 (a)-(d)** (see Supporting Information) with elemental Si and oxidised Si atomic percentage concentrations labelled. The comparative spectra on the unfunctionalized Si substrates are shown in **Figure S3 (a)-(d)** (see Supporting Information). With the exception of the first 24 h, the acquired data showed no discernible difference between the rates of oxidation between a TAA functionalized substrate and a non-functionalized substrate. The rate at which the atomic

concentrations of Si oxides increased was very similar between both samples. This oxidation may be attributed to the small molecular footprint of the TAA molecule, or possibly pinhole oxidation at unreacted hydrogen passivated sites, which is consistent with the fact that H-passivated silicon surfaces are only stable in air for a matter of minutes.[13]

Estimation of Overlayer Thickness

A good indicator of the coverage and thickness of the organo-arsenic layer on Si substrates was estimated by XPS analysis of the TAA functionalised sample as shown in Figure 2(b) using a method originally defined by Cumpson, from equation 1. [31] The overlayer referred to here is the monolayer composed of the TAA molecule,

$$\ln\left(\frac{I_0 S_0}{I_s S_s}\right) - \left(\frac{\lambda_0}{\lambda_s}\right)\frac{1}{\lambda_0 \cos\theta} - \ln 2 = \ln \sinh\left(\frac{t}{2\lambda_0 \cos\theta}\right) \qquad (1)$$

where I_0 and I_s represent the respective measured peak intensities of the overlayer and substrate peaks, S_0 and S_s refer to the relative sensitivity factors for the overlayer and the substrate respectively with λ_0 and λ_s referring to the attenuation lengths of electrons in the overlayer and substrate. θ is the emission angle with respect to the surface normal. To minimise the effect of potential errors arising from surface roughness and inelastic scattering a photon emission angle of 35^o was used in conjunction with a 90^o take-off angle with respect to the sample normal. The peak intensity of the organoarsenic overlayer peak, I_o, and the peak intensity of the substrate peak, I_s, were determined using CasaXPS software after a transmission correction. The relative sensitivity factors for the substrate peak S_s and the overlayer peak S_o were obtained from the database in the XPS instrument acquisition software and manually input into the data processing software to remove instrumental factors which

may affect quantification. The attenuation length of photoelectrons in the overlayer, λ_o, was estimated using the NIST Electron Effective Attenuation Length database to be 2.6 nm. The overlayer thickness was therefore estimated to be approximately 0.5 nm, which based on the predicted molecular footprint of the TAA molecule of approximately 0.6 nm, would imply the presence of a monolayer on the Si surface. The surface was thoroughly cleaned by prolonged sonication in anhydrous solvents prior to characterization to remove all physisorbed species prior to analysis to minimize contributions from contaminants to the overlayer thickness.

Carrier Profiling

The functionalized substrates were capped with a 50 nm layer of sputtered SiO_2 and heated by rapid thermal annealing under nitrogen at varying temperatures for 5 s, to investigate the effect of temperature on the dopant depth and concentration gradient. We note that the specific composition of the capping layer and the method used for deposition can affect the monolayer integrity and diffusion process but the effect of the capping layer was not studied in this work. Use of electron beam evaporation or plasma-enhanced chemical vapour deposition could be investigated to determine the effect on the MLD process. The oxide cap was removed post anneal using a buffered oxide etch prior to further characterization. To ascertain the dopant depth, total dopant concentration and active carrier concentration a set of samples were analyzed by SIMS. **Figure 4(a)** shows SIMS derived chemical concentration *vs.* depth data of three samples thermally treated for 5 s at 950, 1000 and 1050 ^{o}C respectively. The data shows, as expected, that the higher processing temperature results in an overall higher incorporation of As in Si, with the maximum chemical concentrations approaching 2×10^{20} atoms/cm^3 at 1050 °C. **Table 1** summarises the chemical concentration data and also shows chemical dose and diffusivity (D) data extracted from the SIMS profiles

by integration, in **Figure 4(a).**

Temperature (°C)	**Dose (atoms/cm^3)**	**Max concentration (atoms/cm^3)**	***D*** **(cm^2/s)**	n_i **(atoms/cm^3)**	C/n_i
950	5.69×10^{13}	3.41×10^{19}	4.36×10^{-13}	7.00E+18	4.9
1000	3.31×10^{14}	1.04×10^{20}	1.58×10^{-12}	1.00E+19	10.4
1050	7.06×10^{14}	1.57×10^{20}	3.16×10^{-12}	1.50E+19	10.5

Table 1. Extracted data for blanket samples showing the total chemical dose and diffusivity data extracted from the SIMS profiles in **Figure 4(a)** where *D* refers to the diffusivity, n_i refers to the intrinsic carrier concentration and C/n_i is the surface impurity concentration over the intrinsic carrier concentration.

Figure 4(b) depicts the extracted diffusivity data *vs*. 1000/*T* (*T* in Kelvin) plotted in red and compared with the intrinsic diffusivities from the literature plotted in blue. The data shows that extrinsic diffusivity rates are observed in this study. The doped substrates also exhibited high carrier concentrations. The concentrations increased evenly with the rising rapid-thermal anneal temperature, *i.e.* controlled diffusion. **Figure S4** (Supporting Information) shows a representative ECV profile indicating good dopant activation. Semiconductor devices rely on the ability to form two different types of electrically-conducting layers: p-type and n-type. An electrically active dopant atom contributes a free carrier to the valence band or conduction band by creating an energy level that is very close to either band. Therefore an ideal dopant should have a shallow donor/acceptor level and a high solubility. The vast majority of MLD work to date has been concerned mainly with phosphorus- and boron-containing moieties and, to the best of our knowledge, no reports exist of MLD using As-containing liquid molecules. Concentrations approaching 6×10^{20} atoms/cm^3 have been

reported in the literature for phosphorus-MLD in conjunction with spike annealing at 1050°C using a P source with a molecular footprint of approximately 0.12 nm,[32] while concentrations as high as 10^{22} atoms/cm^3 have been noted for P-MLD using a high temperature soak anneal with spike annealing.[33] The TAA molecule has a similar molecular footprint and peak concentrations for the As-MLD process used here are of the same order of magnitude as previous P-MLD work with junction depths on average <50 nm from SIMS data in **Figure 4(a)**. Arsenic and phosphorus are considered to be the best choices for n-type doping of semiconductors based on their ionisation energies[34] and also based on their high solubilities in Si.[35] For extremely small feature size devices with complex and non-planar geometries that need abrupt shallow doping profiles it is desirable that the diffusion rate of the dopant is small. Compared to phosphorus, As has a much smaller diffusion coefficient, making it the dopant of choice for heavy and shallow n-type doping of silicon.[36] As the junction depth in the MLD process is limited by temperature and duration of anneal, the diffusion of As in Si using the MLD method could be further fine-tuned in terms of shallower junction depths by using emerging spike annealing techniques such as flashlamp annealing and laser annealing.[37–39]

Application of the MLD Strategy to Nanowire Devices

As the MLD process can be applied to various types of semiconductor surfaces, including nanostructured quasi-1D and 2D materials, an analogous arsenic doping process was attempted to controllably dope 'top-down' Si nanowires fabricated on silicon-on-insulator (SOI) substrates. Intense research continues into semiconductor nanowires due to their potential in the scaling of semiconductor devices.[40] As Si has long been the material of choice in the semiconductor industry its properties are well known and its processing technologies are well established, making Si nanowires ideal for fundamental research, while

maintaining compatibility with current electronic processing techniques for eventual integration into future technology nodes. As nanowires in general have large surface-to-volume ratios, defects trapped at Si/SiO_x interfaces have acute effects on the performance of a device by trapping and scattering mobile charge carriers.[41] The applications of certain surface passivation techniques, such as hydrogen-termination[42], can greatly reduce the density of these defects and increase the FET response of a Si nanowire channel.[43] An advantage of the MLD process developed in this study is that there is no damage to the nanowires, which might otherwise be caused by techniques such as ion implantation. Charge depletion caused by the presence of surface states can potentially limit the effective channel diameter of a nanowire. Additionally, dielectric mismatch between a nanowire and its surrounding can also cause changes in the electrical characteristics by increasing the ionisation energies for dopants which are near the nanowire surface.[44] This problem can be overcome by using good surface treatments which minimize surface damage and enable high-dopant densities and, most importantly for FET doping, high conformality which is attainable using the MLD based strategy employed here.

To properly assess the effects of the MLD process on fine features, top-down patterned Si nanowires (fins) ranging in width from 20 – 1000 nm were fabricated. The fabrication process is described in detail in the *Experimental* section. A SEM micrograph of the test structure itself is shown in **Figure S5** in Supporting Information. In essence, the structure is a 4-point probe test structure where a user-defined current is forced across the nanowire by the outer electrodes and then the inner electrodes sense the resulting voltage drop across the nanowire. The design of the contact pads ensures that the voltage drop at the nanowire is measured accurately. The nanowire resistance can be extracted from this current-voltage relationship. The raw I-V data shown in **Figure 5(a)** are of post-MLD nanowires. The

resistivity data shown in **Figure 5(b)** is from the pre- and post-MLD nanowires. In **Figure 5(a)** the current as a function of voltage is linear for all nanowires and passes through the origin. As expected, the current level can also be seen dropping as the nanowire width is scaled down. This change in the current is indicative of ohmic current conduction and good dopant activation, where even 20 nm devices were observed to conduct current very well, indicating that the MLD process was non-destructive toward the smallest nanowires. Assuming that current flows uniformly through the entire cross section of a nanowire, similarly to a metal track, the resistivity (ρ) of a nanowire can be calculated from equation 2:

$$\rho = R\frac{A}{L} \qquad (2)$$

where L refers to the length of a nanowire, A is the cross-sectional area and R is resistance. The application of this model is appropriate for sub-40 nm nanowires and FinFETs as at these dimensions the probability of having a uniformly doped cross-section is high. At the smallest sizes it can be assumed that the entire volume of the device is uniformly doped and current flows throughout the entire cross-section *i.e.* like that of a metal track. As current devices are sub-40 nm and future technologies will continue to scale, this model offers a good platform to evaluate device behaviour in current and future device technologies. **Figure 5(b)** shows both pre- and post-MLD resistivity data for nanowires. Significantly lower resistivities were obtained for post-MLD nanowires, especially those with widths less than 40 nm. There is a similar striking difference of several orders of magnitude between the resistivities of the nanowires pre- and post-MLD. The largest decrease in resistivity was observed within nanowires with dimensions under 40 nm, with a decrease of between 5 orders of magnitude for larger nanowires and 7 orders of magnitude for the smallest sized nanowires, when compared to the undoped nanowires; showing the efficacy of the MLD process on such small

feature size devices**.** **Figure S6** in Supporting Information displays resistance data for the MLD-doped nanowires.

To confirm that the MLD process did not affect nanowire morphology, cross-sectional TEM analysis of the doped nanowires was undertaken. Historically, {111} twin boundary defect formation and stacking faults are the most common problems faced when doping at small feature sizes, most often caused by ion-implantation processes. Extended defects are considered here as these defects are quite easily visible by TEM analysis. **Figure 6(a)** shows a TEM image of a section of a 40 nm Si nanowire test device. **Figure 6(b)** displays a magnified high-resolution TEM image of the same nanowire with the <111> and <100> directions indicated. The Fast Fourier Transform (FFT) shown in the inset of **Figure 6(b)** shows the highly crystalline nature of the nanowire, which is consistent with the non-destructive nature of the MLD process. There are no indications on either micrograph of any extended defects or damage to the crystal lattice, showing that the developed arsenic-MLD process as applied to bulk Si wafers also transfers very well to nanostructured devices. This is in stark contrast to ion implanted nanostructures where crystal damage is very easily visible and poly-crystalline changes can be problematic with a decreasing $W_{\text{fin.}}$

Conclusions

The doping of non-planar nanostructures is difficult due to the non-conformality of conventional doping methods in addition to the problems encountered during diffusion, during their activation, in trying to prevent their escape during the thermal processing treatments and all the while still trying to preserve the crystalline nature of the material. The controlled doping of bulk and nanostructured silicon was achieved successfully *via* the use of organo-arsenic molecular monolayers. Extremely high dopant concentrations approaching 2

$\times 10^{20}$ atoms cm^{-3} were observed for bulk Si while excellent electrical characteristics were observed for the MLD-doped Si nanostructures with the with the highest decrease in resistivity of seven orders of magnitude observed for nanowires less than 40 nm in width. The MLD process was observed to have no effect on the crystallinity of the nanowires and no visible damage or defects were observed. Research must continue on the design and characterization of suitable molecular precursors that are stable during the hydrosilylation procedure and remain stable and resistant to decomposition in ambient conditions afterwards.

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Supporting Information Available: Reaction schematics, XPS stability spectra, topography characterization and additional microscopy images are available in the Supporting Information. This material is available free of charge via the Internet at http://pubs.acs.org.

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Figures

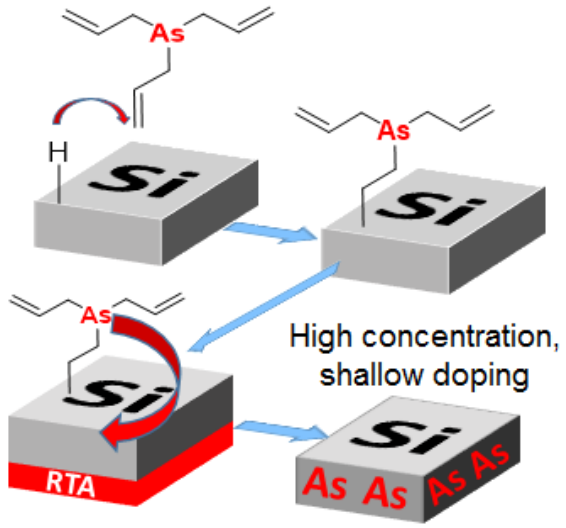

Figure 1. Schematic depicting the MLD process developed and applied in this study. A hydrosilylation reaction occurs between a reactive H-passivated Si surface and the labile C=C site on the dopant containing molecule, resulting in a covalently bonded molecular layer. The samples are then capped with 50 nm of SiO_2 and subjected to a rapid-thermal-anneal (RTA) step resulting in high concentration, shallow doping of silicon.

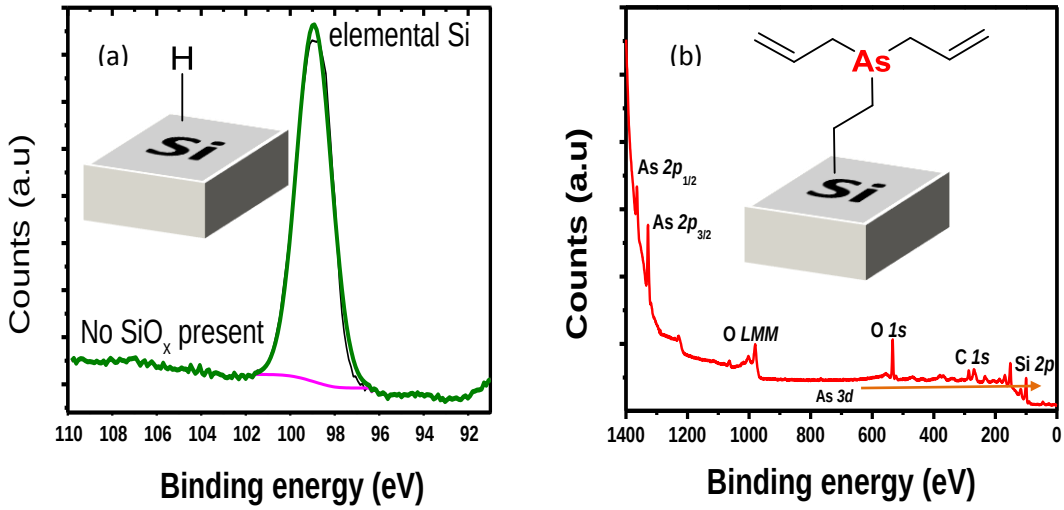

Figure 2. (a) High resolution Si 2p core level scan pre-functionalization, showing the pristine oxide-less surface required for MLD with a schematic representation inset, (b) wide, survey scan of a TAA functionalized Si surface with peaks of interest labelled. Inset shows schematic representations of the functionalized surface.

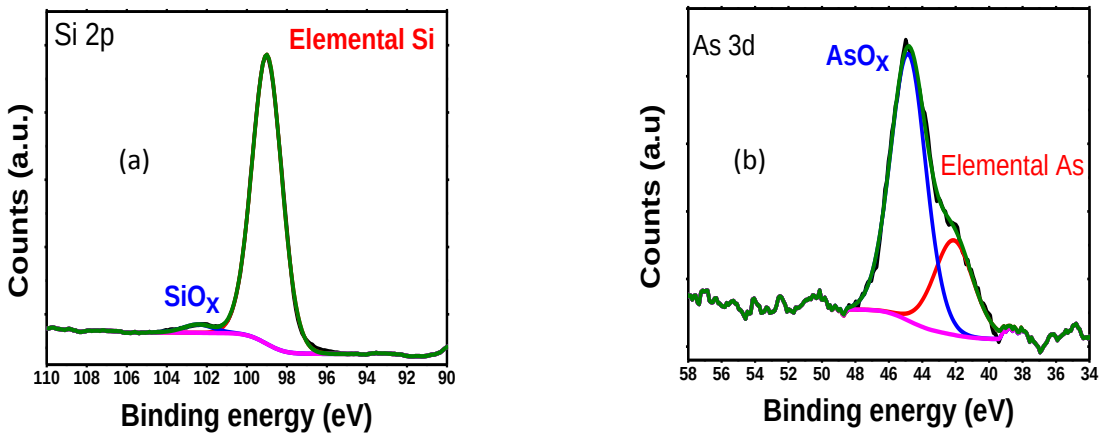

Figure 3. (a) Si *2p* core level spectrum of a freshly functionalized substrate composed primarily of elemental Si and a small shoulder peak indicating a low amount of SiO_x, (b) As *3d* core level spectrum of a TAA functionalized Si surface. The elemental components of the peak are labelled in red with the oxidised components of each sample labelled in blue.

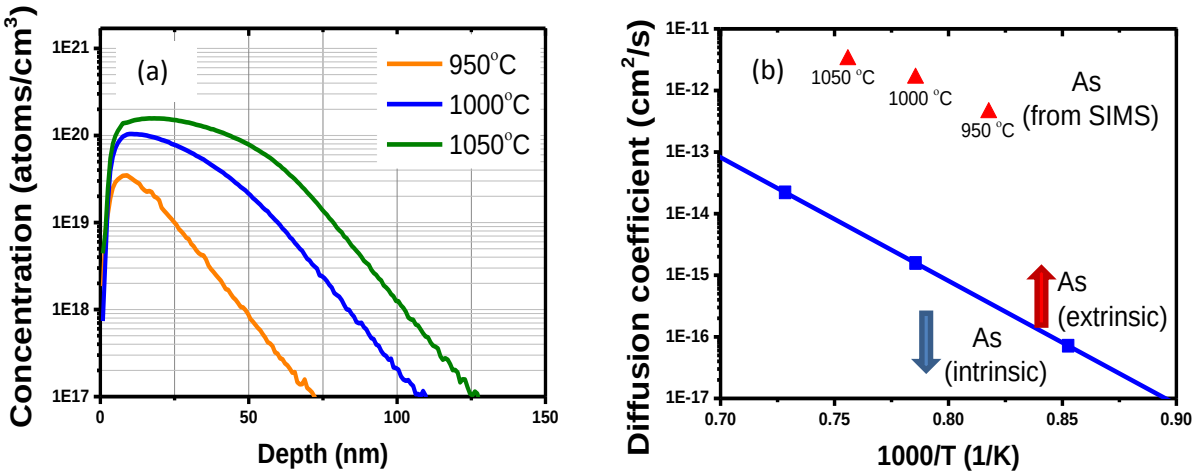

Figure 4. (a) Secondary ion mass spectrometry profiles of 3 samples processed at varying temperatures for 5 s. The carrier depths were observed to be extremely shallow with peak concentrations achieved at less than 25 nm (b) Diffusivity data extracted from SIMS analysis. As can be seen in the measured data in red, the samples exhibit diffusivity in the extrinsic regime.

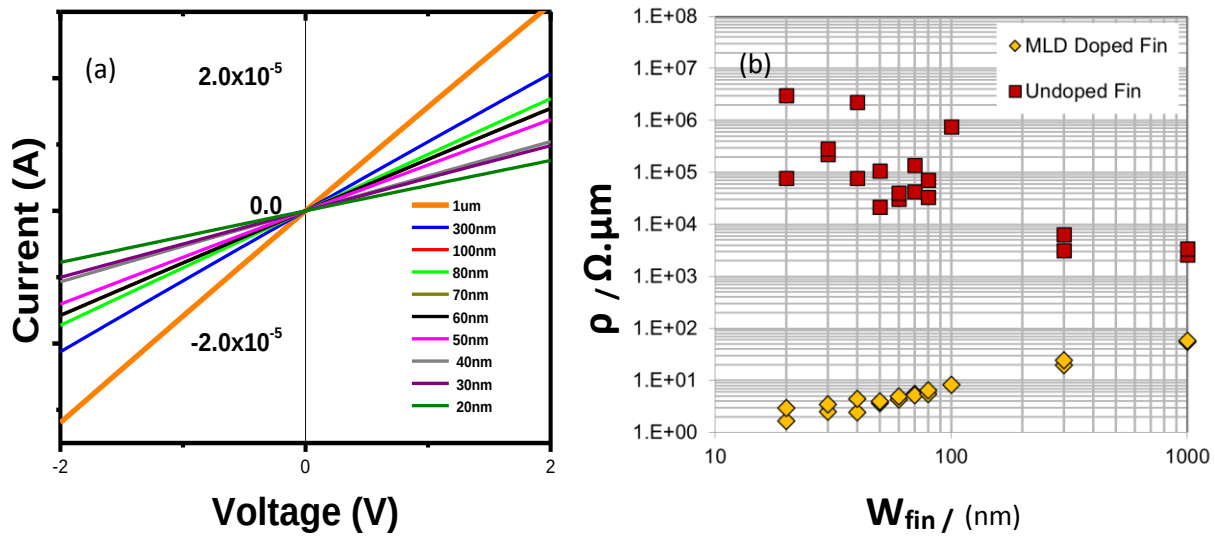

Figure 5. **(a)** Raw I-V data for post-MLD nanowires. The data is symmetrical about the origin with the current obeying Ohms law and scales with reducing nanowire width. **(b)** Resistivity of nanowires as a function of width for pre-MLD and post – MLD wires. The best results were observed for nanowires < 40 nm in width, showing that the MLD strategy employed works extremely well for small feature sizes.

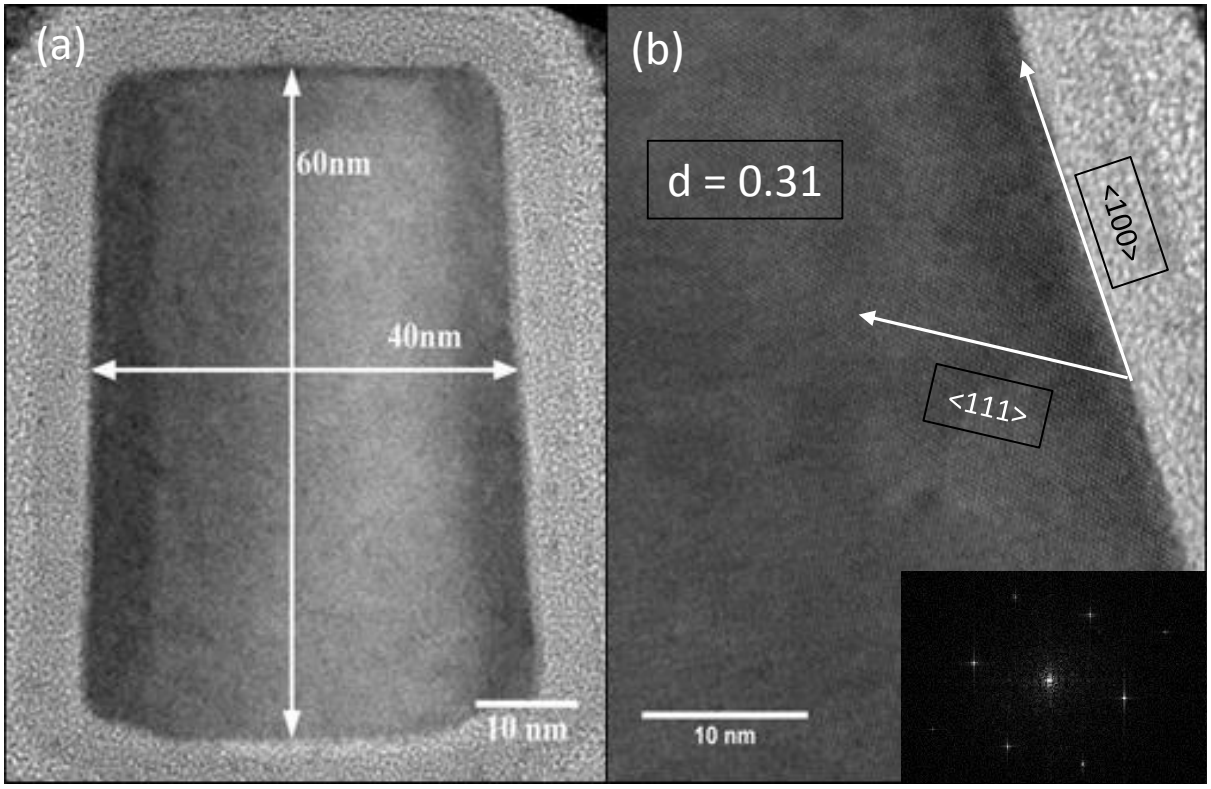

Figure 6. (a) TEM micrograph of a section of the 40 nm Si nanowire test device, (b) magnified HRTEM micrograph of the nanowire with the <111> and <100> directions indicated. The FFT shown in the inset of (b) shows the highly crystalline nature of the nanowire. There are no indications on either micrograph of any defects or damage to the crystal lattice.

TOC Graphic