Fully CMOS-compatible top-down fabrication of sub-50 nm silicon nanowire sensing devices

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Abstract

This article reports the fabrication of sub-50 nm field effect transistor (FET)-type silicon (Si) nanowire (Si NW) chemical and biological sensing devices with a junctionless architecture, as well as on the initial characterisation of their electrical and sensing performance.

The devices were fabricated using a fully complementary metal-oxide-semiconductor (CMOS)-compatible top-down process on silicon-on-insulator (SOI) wafers. The fabrication process was mainly based on high-resolution electron beam lithography (EBL) and reactive ion etching (RIE) but also included photolithography (mix-and-match lithography), thin film deposition by electron beam evaporation, lift-off, thermal annealing and wet etching.

The sensing performance of a matrix of nanowire devices, *i.e.* containing 1, 3 and 20 NWs with lengths of 0.5, 1 and 10 μm was examined. Each element of the matrix also contained five devices with different NW widths: 10, 20, 30, and 50 nm and 5 μm (a Si belt reference device). Electrical characterisation of the devices showed excellent performance as backgated junctionless nanowire transistors (JNTs): high on-currents in the range of 1-10 μA and high ratios between the on-state and off-state currents (I_{on}/I_{off}) of 6-7 orders of magnitude. In addition, the results of ionic strength sensing experiments demonstrate the very good sensing capabilities of these devices. To the best of our knowledge, these nanowire sensors are among the smallest top-down fabricated Si NW devices reported to date.

Keywords: silicon nanowire sensor, field effect transistor, junctionless nanowire transistor, top-down nanofabrication, electron beam lithography, HSQ

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1. Introduction

Si nanowires (Si NWs) have received significant academic and commercial attention due to their attractive electrical and mechanical properties and large surface area to volume ratios. Such materials are promising as channels for field effect transistors (FETs) [1] and also as sensing devices [2, 3]. The first FET-type nanowire sensors were demonstrated on grown NWs [2], which were initially the main building blocks of NW sensors (clarify what you mean by this sentence – unclear). Whilst Si NWs can be produced in reasonable quantities from 'bottom-up' synthetic methods, their post positioning and alignment remains a challenge. Issues associated with nanowire alignment are overcome by producing arrays of nanowires from 'top-down' methodologies, *e.g.* electron beam lithography (EBL). Lithography also allows better control over nanowire geometries, *i.e.* control over length, width, thickness, number and orientation along different Si crystallographic axes. These parameters are particularly important for sensing applications and have been theoretically [4] and, to some extent, experimentally investigated [5,6]. However, to the best of our knowledge, there has been no consistent experimental study of their influence on the electrical and sensing performance of sub-50 nm Si NWs.

Here we report the top-down fabrication of a range of Si NW sensing devices having various nanowire densities, lengths and widths. The operation of these devices relies on the principle of a field effect transistor. In contrast to most sensors of this type, however, our devices have a junctionless architecture [7-9], *i.e.* the source, channel (nanowires) and drain have the same dopant polarity (p-type in this case) without any junctions between them. Such devices are easier to fabricate than…(what? Traditional FETs?) since they do not require separate doping of the source and drain regions and possess a number of other advantages over the conventional inversion-mode FETs [7-9].

The devices were fabricated mainly by electron beam lithography and reactive ion etching (RIE) on silicon-on-insulator (SOI) wafers. For every single die of the wafers, a matrix of three different nanowire densities (1, 3, and 20 NWs) and lengths (0.5, 1, and 10 μm) was designed, making nine elements altogether. Each element of the matrix contained five devices with different NW widths: 10, 20, 30, and 50 nm and 5 μm (a Si belt reference device), permitting 45 different devices on a chip (see Fig. 1). The initial electrical characterisation of the devices revealed well-functioning backgated junctionless nanowire transistors (JNTs). In addition, the data obtained from ionic strength sensing experiments demonstrate their very good sensing performance.

2. Material and methods

SOI wafers with a *p*-doped top Si layer of 70 nm,a buried oxide (BOX) SiO_2 layer of 145 nm and a base Si layer of 500 μm (Soitec) were used in this study.

The top device layer of the SOI wafer was oxidised, via dry thermal oxidation, to form a thin 45 nm SiO_2 layer. As a result, the thickness of the device layer was reduced from 70 to 44 nm prior to doping with boron (B) by ion implantation to a dose of 4×10^{13} cm^{-2} at ion energy of 14 KeV and a tilt angle of 7°. Dopant activation was achieved by furnace annealing at 900 °C for 30 min in a nitrogen environment. The effective doping concentration in the Si device layer was estimated to be equivalent to $\sim 1 \times 10^{18}$ cm^{-3}.

Two EBL exposures were undertaken on a full 4" SOI wafer using a JEOL JBX 6000FS Gaussian beam direct write system operated at 50 kV. In the first exposure, alignment marks were defined in a 425 nm thick layer of ZEP520A positive resist (Nippon ZEON Corp.), using the low-resolution high-current mode of the system. The marks were etched 1.5 μm deep

through the ZEP mask with a two-stage plasma etching process. Subsequently the resist was removed and the top SiO_2 layer wet etched in 10:1 buffered oxide etchant (BOE), resulting in a Si device layer thickness of 44 nm.

In the second EBL exposure, the nanowire devices (nanowires together with the source and drain contact pads) were defined in a 50 nm thick layer of hydrogen silsesquioxane (HSQ) negative tone resist (XR-1541 from Dow Corning Corp.), using the high-resolution mode of the system and a beam current of 100 pA. In order to ensure definition of resist structures down to 10 nm, as well as full CMOS compatibility of the fabrication, an original high-contrast and low roughness development process, using 25 % tetramethylammonium hydroxide (TMAH) as the main step [10, 11], was implemented. The widely used HSQ salty developer NaOH (1 wt%) / NaCl (4 wt%) [12] was wittingly avoided since sodium is an unwanted impurity in CMOS devices [13] and wafer processing with this developer would not be allowed in our CMOS compatible Si Fab.

To transfer the HSQ lithographic pattern into the top Si layer, RIE processing with chlorine (Cl) chemistry in a Plasmalab System 100 from Oxford Instruments was used. Subsequently, an additional 200 nm SiO_2 layer was deposited on the whole surface, except the device regions, to minimise the leakage current through the buried oxide. Next, the metal contacts and interconnection were created by depositing a stack of 100 nm platinum (Pt) and 40 nm nickel (Ni) layers. Then, a passivation layer of 500 nm SiO_2 was deposited again on the whole surface, except the device regions and metal pads. These three subsequent depositions were done by electron beam evaporation in Temescal FC-2000 (metal depositions) and Leybold Lab 600 (SiO_2 depositions) systems and were respectively combined with three steps of photolithography and lift-off. The photolithography exposures were aligned to the previously exposed EBL pattern using the etched alignment marks, *i.e.* mix-and-match lithography was undertaken. To improve the conductivity of the devices, they were thermally annealed for 30 min at 425 ºC in forming gas (10 % H_2 / 90 % N_2). A cross-section of fabricated devices is schematically presented in Fig. 2.

Electrical characterisation of the devices, as well as the ionic strength sensing experiments was performed using a cascade manual probe station and Agilent semiconductor analyser B1500.

In order to demonstrate the sensing capabilities of our devices, ionic strength sensing experiments were performed. In these experiments, solutions of different ionic strengths but equivalent pH values were generated by diluting phthalate buffered solution (Fisher, pH 7) with deionised (DI) water. To make a 5× diluted solution (dilution 1), 2.0 ml of the buffer was measured into a 15 ml centrifuge tube using a syringe and the total volume of the liquid was increased to 10 ml with DI water. To make a 25× diluted solution (dilution 2), the process was repeated in a fresh centrifuge tube, but using dilution 1 in place of the buffer. A 125× diluted solution (dilution 3) was obtained using the dilution 2 stock solution.

The solutions were delivered to the NW sensors through microfluidic channels within a polydimethylsiloxane (PDMS) stamp attached to the devices. Each microfluidic PDMS stamp was fabricated using standard procedures [14] and comprised a single 200 µm-wide channel with 400 µm access holes drilled in to the top to provide an interface between the microfluidic channel and external tubing. The stamps were attached to the devices using the "stamp and stick" technique [15] in which a thin layer of wet PDMS was added to the underside of the stamp before being positioned on the device. Positioning of the devices was achieved using a micrometer-controlled positioning rig built in-house. Following curing at 60 ºC for 2 hours, a strong but non-permanent bond was formed to yield integrated sensing/fluid delivery devices (Fig. 3).

The solutions were delivered from gastight syringes (Hamilton) propelled by a syringe pump (Harvard Pump 11+) at a flow rate of 150 μL min^{-1}. The fluid flowed from the syringes through 400 μm outer diameter, 250 μm inner diameter polytetrafluoroethylene (PTFE) tubing (Cole-Parmer) which fitted snugly into the access holes drilled in the PDMS stamp.

3. Results and discussion

The junctionless architecture of our devices requires a relatively high doping level as well as a small channel cross-section (small height and width of the nanowires). Junctionless transistors operate ideally at doping levels around of 1×10^{19} cm^{-3}, although higher levels are usually used [7-9]. Such high doping levels however, might have adverse influence on the sensitivity of Si NW sensing devices [4]. Therefore, in this study a moderate doping concentration was chosen and the SOI wafer was doped to ~1×10^{18} cm^{-3}. In addition, the thickness of the top device layer was reduced by oxidation and wet etching from 70 to 44 nm, to ensure better control over the current through the channel by the backgate voltage, as well as by the top-gating effect of the charged analyte to be sensed.

The EBL definition of the nanowire devices was a very demanding task due to the variety of different devices combining single and multiple, short and long NWs with large contact pads. Such a configuration of devices leads to a significant proximity effect [16] and, hence, deviation of the NW shapes and dimensions from the designed ones. This effect was particularly noted for the short (0.5 and 1 μm) NWs where the proximity effect from the closely spaced contact pads was particularly strong. Therefore, an advanced proximity effect correction (PEC) was required, together with the precise adjustment of the exposure doses within 2-5 % process windows. As a result, high quality lithographic structures were obtained with proper shapes and dimensions very close to those anticipated, as demonstrated in Figs. 4(a) and (b). The figurse represents collages of top-view scanning electron microscopy (SEM) micrographs of structures with different number (1, 3, and 20) of short (0.5 and 1 μm) and long (10 μm) HSQ lines with the two smallest (and lithographically most demanding) designed widths: 10 nm (Fig. 4(a)) and 20 nm (Fig. 4(b)).

The chlorine based RIE of the top Si layer through the HSQ mask resulted in structures with low roughness and minimum deviations of the Si NW widths from the designed ones, as can be seen in Figs. 5(a) and (b), where top-view SEM micrographs of devices with different NW configurations are shown as an example, again for the two smallest Si NW widths: 10 nm (Fig. 5(a)) and 20 nm (Fig. 5(b)). The line edge roughness (LER) of the nanowires was estimated to be between 0.8 and 1.6 nm, which is an excellent achievement. The high quality of the Si NWs is a prerequisite to minimise the scattering of charge carriers on their sidewalls (surfaces) and, hence, for the high electrical conductance and high sensitivity of the NWs. As a comparison, in recent publications [5, 6] the roughness of the nanowires was estimated to be 5-7 nm regardless of their nominal width, which is significantly higher than in our case.

These data clearly demonstrate the advantages of using HSQ as an etch mask compared to the positive resist poly(methyl methacrylate) (PMMA) [5, 6], where the positive lithographic pattern subsequently has to be reversed into a negative one, through the deposition of a 15 nm thick chromium (Cr) layer and lift-off. In these approaches, the Cr pattern was used as a hard mask for the RIE process. This process flows using PMMA resists is not only more complicated than ours but, as mentioned above, results in a significantly higher LER, largely due to the presence of polymer aggregates that already exist in the resist solution before spin coating [17, 18] ande which are formed due to intermolecular attractions between single polymer chains [19]. Since these aggregates are not dissolved but extracted during the resist development, they appear on the surfaces of the lithographic structures causing sizeable sidewall and LER efefcts.. HSQ has a

relatively small aggregate size, between 10-15 nm [20], compared to around 30 nm for PMMA., To the best of our knowledge, the devices presented here are among the smallest top-down fabricated SiNW sensing devices reported to date.

Fig. 6 presents output characteristics (drain current I_d as a function of the drain potential V_d, I_d-V_d lines) of single and triple nanowire devices having a NW length of 0.5 μm and widths of 30 and 50 nm. These straight and symmetric I_d-V_d lines demonstrate the very good ohmic contacts between the metal contacts and the Si nanowires and the high on-currents of our devices; clear evidence of the excellent overall process quality.

Fig. 7 shows sample transfer characteristics (drain current I_d as a function of the backgate potential V_{bg}, I_d-V_{bg} curves) of single nanowire devices (having nanowire a length of 0.5 μm and the two extreme NW widths: 10 and 50 nm) for different drain bias potentials, V_d = - 0.3 V, - 0.5 V, and - 0.9 V. The I_d-V_{bg} curve for the Si belt reference device (width of 5 μm) is also shown for comparison (here V_d = -0.16 V). The results reveal well-functioning backgated JNTs with promising properties for sensing applications. The on-currents are high, in the range of 1-10 μA. The backgate potential allows good control over the current through the nanowire devices (10 and 50 nm), leading to high ratios between the on-state and off-state currents (I_{on}/I_{off}) of 6-7 orders of magnitude. This is, however, not valid for the wide (5 μm) reference device where the drain current was only slightly influenced by the backgate potential in the range of interest, even at a V_d as small as - 0.16 V. Such a significant difference in the behavior of the NW devices (10 and 50 nm) and the planar device (5 μm) could seem unexpected since the electric field induced by the backgate potential is essentially perpendicular to the device surface and the device thickness is the same in both cases. Nevertheless, it can be explained by the surface states at the sidewalls of the Si NWs, which obviously have a large influence on the current flow through the channels. This supposition is supported by the fact that the NW width has a significant influence on the V_{th} of our backgated JNTs: the V_{th} shift is around 15 V here for the 10 and 50 nm devices. As discussed below, such an effect can be used to fine tune the device properties for low-power sensing applications.

Another noteworthy feature is that in the range of interest (up to 1 V), V_d only has a considerable influence on the level of I_{on} and almost no influence on the threshold voltage V_{th}, *i.e.* small drain induced barrier lowering (DIBL), and the subthreshold slope (SS) (see Fig. 7).

FET-type Si NW sensors have the optimal sensitivity performance when operated in the subthreshold regime, where they demonstrate the highest conductance response [21, 22]. Fig.7 clearly demonstrates that the subthreshold region of the 10 nm device appears at a negative backgate bias (it is normally off), while for the 50 nm device the region in an area of positive backgate bias (the device is normally on). Therefore, both devices need a backgate potential of more than 5 V (negative for the 10 nm device and positive for the 50 nm one) in order to operate in the most preferable subthreshold regime. This compromises their power efficiency, making them unsuitable for application in autonomous sensing systems. The intermediate devices (20 and 30 nm), however, demonstrate operation in the subthreshold regime at V_{bg} = 0 (not shown here) (why not?) and would be the devices of choice for such application.

In order to test the device's response to ionic strength, different concentrations of a phosphate (?) buffer solution were prepared (pH 7). The different dilutions of buffer were flowed over the sensor whilst monitoring the drain current I_d at a constant drain potential, V_d = 1 V. Before each new dilution was administered, air was flowed through the device to ensure the previous dilution was completely removed. The data shown in Fig. 8 indicates that increasing the dilution of the buffer, hence lowering its ionic strength, leads to a significantly decreasing response and that the repeated measurement of the undiluted buffer shows that the trend is repeatable. These data clearly demonstrate the very good ionic sensing performance of our devices.

4. Conclusions

In conclusion, junctionless Si NW chemical and biological sensing devices, having diverse geometries, were fabricated with high precision by a fully CMOS-compatible top-down process on SOI wafers. The patterning of devices was based on high-resolution EBL with the negative tone electron resist HSQ and advanced PEC as well as on RIE with Cl-chemistry. The quality of the patterning was very high and resulted in structures with low roughness (between 0.8 and 1.6 nm) and minimum deviations of the Si NW widths from the designed ones; an excellent achievement for devices of such a complicated layout and diverse geometry.

Electrical characterisation of the devices revealed well-functioning backgated JNTs with high on-currents in the range of 1-10 μA (depending on the drain potentials) and high ratios between the on-state and off-state currents (I_{on}/I_{off}) of 6-7 orders of magnitude.

Finally, experiments for sensing the ionic strength of different buffer solutions (pH 7) clearly demonstrate the very good sensing capabilities of these devices. To the best of our knowledge, they are among the smallest top-down fabricated SiNW sensing devices reported to date.

Acknowledgements

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Highlights

- **Top-down fabrication of sub-50 nm silicon nanowire sensors with various geometries**
- **Excellent performance as backgated junctionless nanowire transistors (JNTs)**
- **Very good sensing capabilities**
- **Among the smallest top-down fabricated nanowire sensing devices reported to date**

Figure Captions

Figure 1. Overview of the design layout.

Figure 2. Cross-sectional schematics of fabricated devices.

Figure 3. Optical image of the microfluidic PDMS stamps on a Si NW sensor chip.

Figure 4. Collages of top-view SEM micrographs of structures with different densities (1, 3, and 20) of short (0.5 and 1 μm) and long (10 μm) HSQ lines with the two smallest designed widths: 10 nm (a) and 20 nm (b).

Figure 5. Collages of top-view SEM micrographs of Si NW devices having 1, 3, and 20 NWs of different lengths (0.5, 1 μm, and 10 μm) and the two smallest designed widths: 10 nm (a) and 20 nm (b).

Figure 6. Output characteristics (I_d-V_d lines) for devices with single and triple NWs, 0.5 μm in length and with widths of 30 and 50 nm.

Figure 7. Transfer characteristics (I_d-V_{bg} curves) at three different drain potentials (V_d = - 0.3 V, - 0.5 V, and - 0.9 V) for devices with NW widths of 10 nm, 50 nm and 5 μm (V_d = - 0.16 V) and lengths of 0.5 μm.

Figure 8. Time dependence of the drain current I_d demonstrating the ionic strength sensing results.

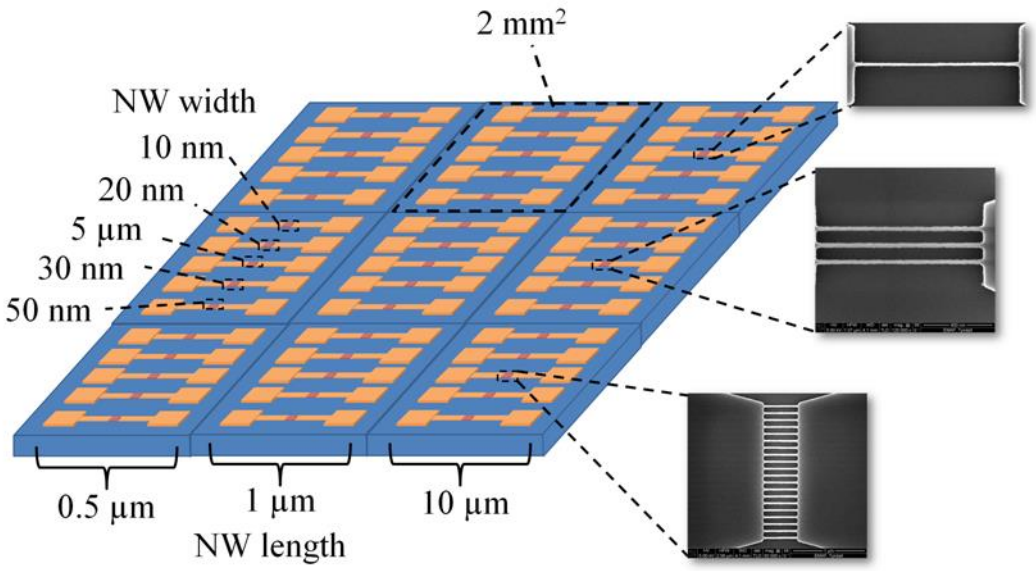


Fig. 1

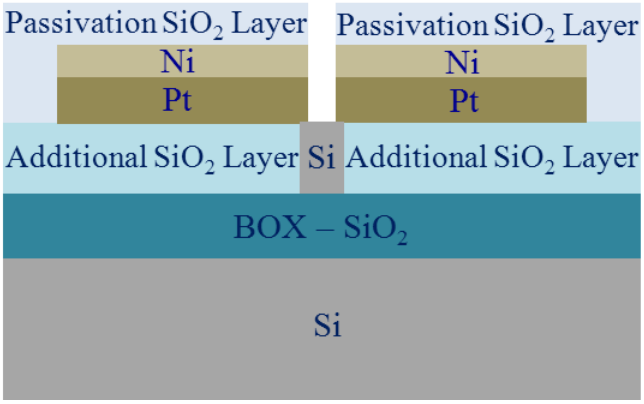

Passivation SiO_2 Layer
Passivation SiO_2 Layer
Ni
Ni
Pt
Pt
Additional SiO_2 Layer
Si
Additional SiO_2 Layer
BOX – SiO_2
Si

Fig. 2

Fig. 3

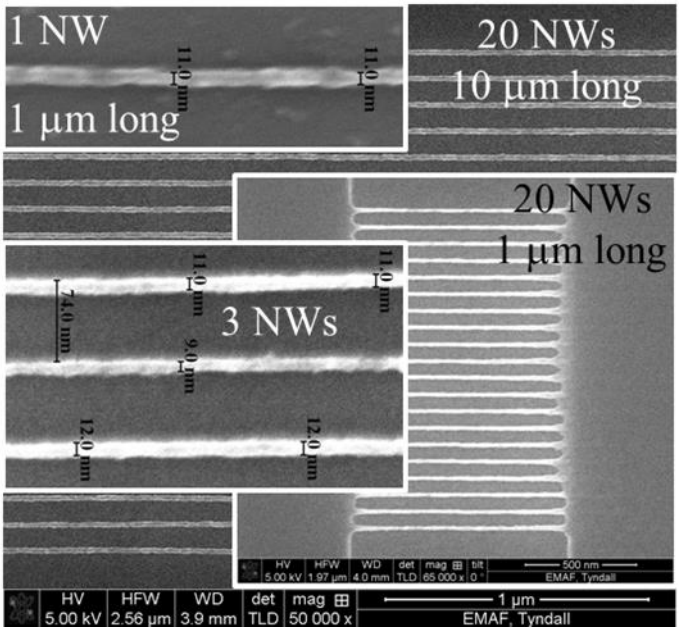

1 NW
1 µm long
11.0 nm
11.0 nm
20 NWs
10 µm long
20 NWs
1 µm long
3 NWs
11.0 nm
11.0 nm
74.0 nm
9.0 nm
12.0 nm
12.0 nm
HV
5.00 kV
HFW
2.56 µm
WD
3.9 mm
det
TLD
mag
50 000 x
1 µm
EMAF, Tyndall

Fig. 4(a)

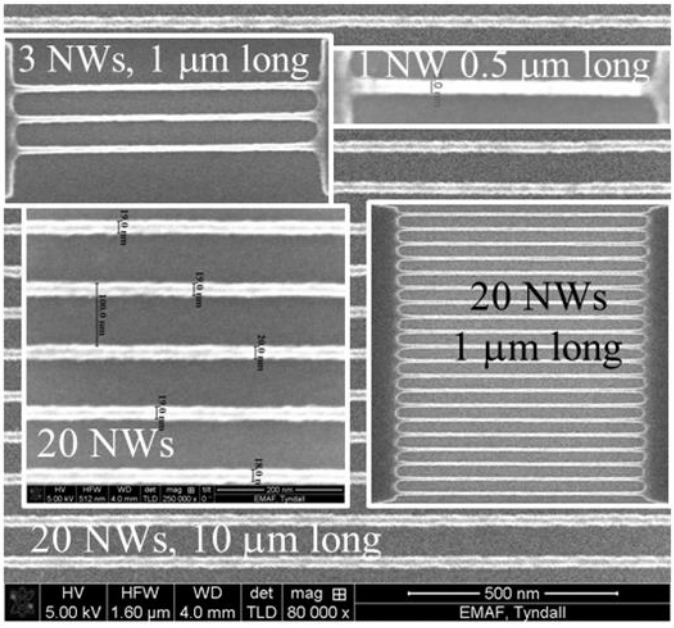

3 NWs, 1 µm long
1 NW 0.5 µm long
20 NWs
1 µm long
20 NWs
20 NWs, 10 µm long
HV
5.00 kV
HFW
1.60 µm
WD
4.0 mm
det
TLD
mag
80 000 x
500 nm
EMAF, Tyndall

Fig. 4(b)

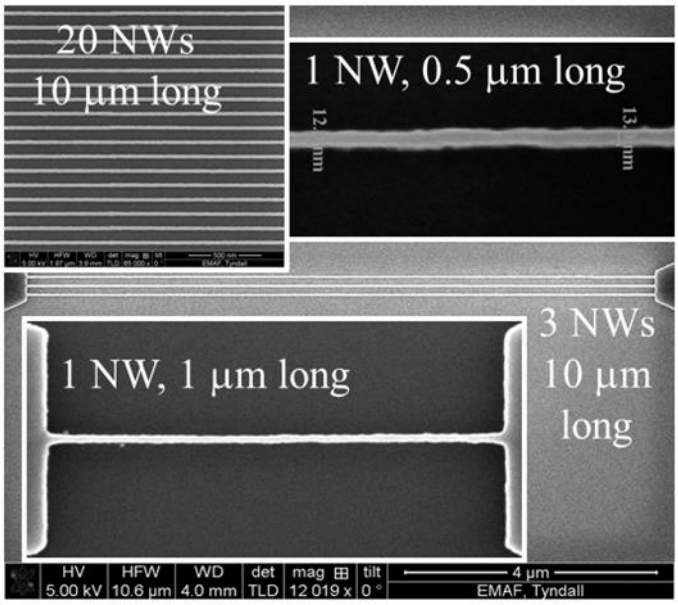

20 NWs
10 µm long
1 NW, 0.5 µm long
1 NW, 1 µm long
3 NWs
10 µm
long
HV
5.00 kV
HFW
10.6 µm
WD
4.0 mm
det
TLD
mag
12 019 x
tilt
0 °
4 µm
EMAF, Tyndall

Fig. 5(a)

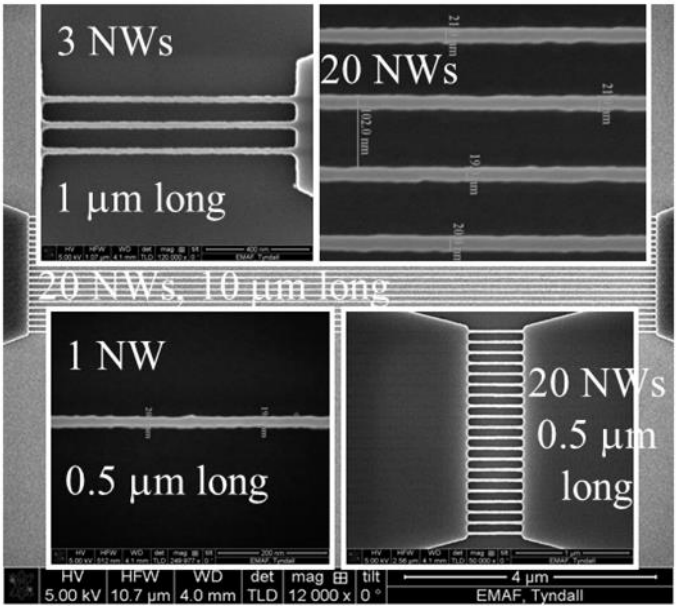

3 NWs
1 µm long
20 NWs
20 NWs, 10 µm long
1 NW
0.5 µm long
20 NWs
0.5 µm
long
HV
5.00 kV
HFW
10.7 µm
WD
4.0 mm
det
TLD
mag
12 000 x
tilt
0 °
4 µm
EMAF, Tyndall

Fig. 5(b)

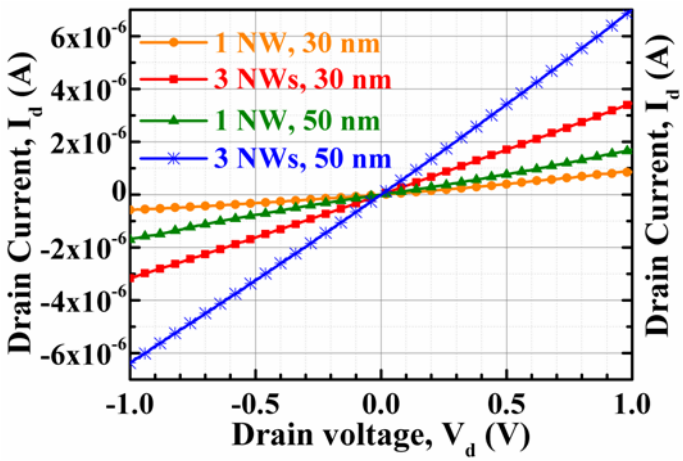

1 NW, 30 nm
3 NWs, 30 nm
1 NW, 50 nm
3 NWs, 50 nm
Drain Current, I_d (A)
Drain Current, I_d (A)
6x10^{-6}
4x10^{-6}
2x10^{-6}
0
-2x10^{-6}
-4x10^{-6}
-6x10^{-6}
-1.0
-0.5
0.0
0.5
1.0
Drain voltage, V_d (V)

Fig. 6

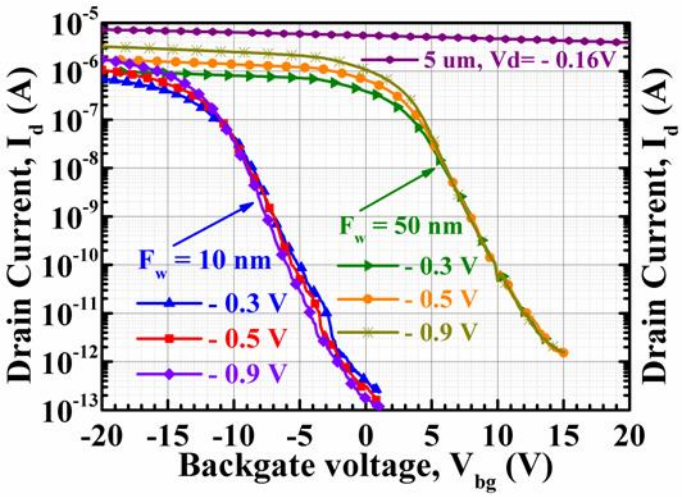

Drain Current, I_d (A)
Backgate voltage, V_{bg} (V)
5 um, Vd= - 0.16V
F_w = 10 nm
- 0.3 V
- 0.5 V
- 0.9 V
F_w = 50 nm
- 0.3 V
- 0.5 V
- 0.9 V

Fig. 7

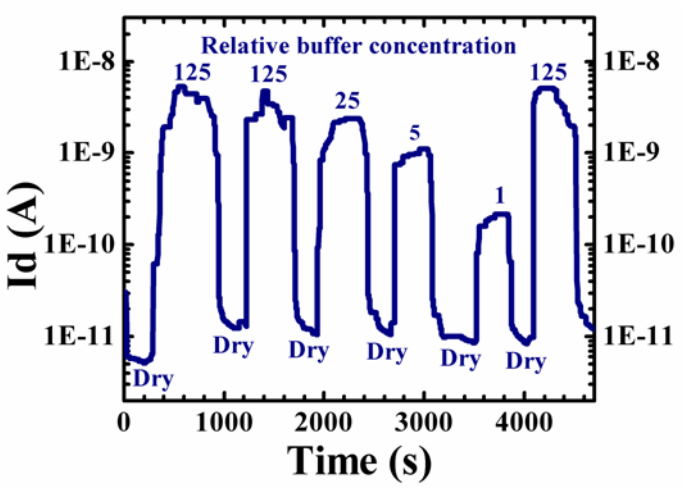
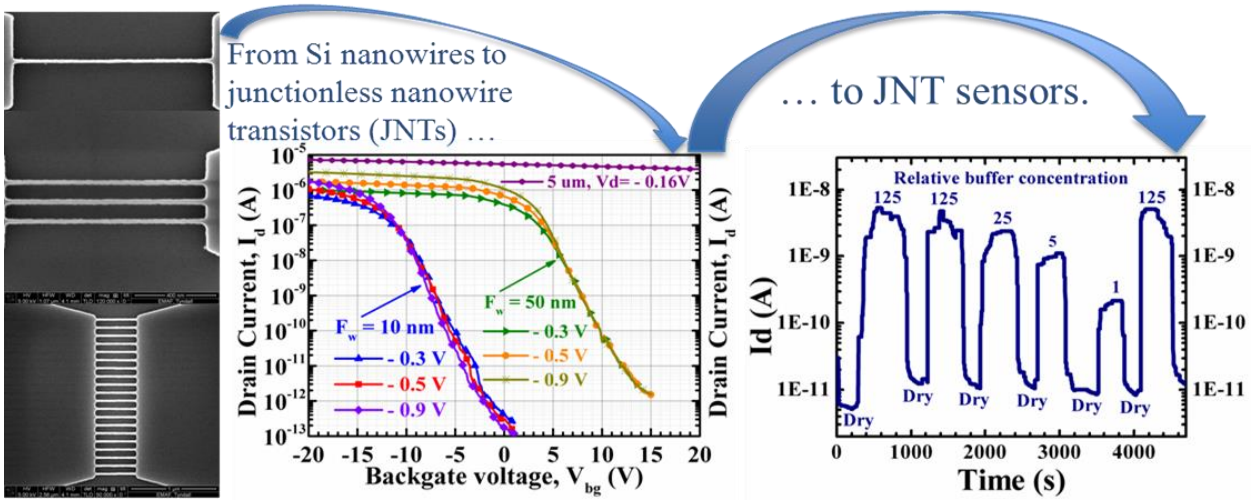

Relative buffer concentration
125
125
25
5
1
125
Dry
Dry
Dry
Dry
Dry
Dry
Dry
Id (A)
1E-8
1E-9
1E-10
1E-11
0
1000
2000
3000
4000
Time (s)

Fig. 8



Graphical Abstract