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CHARACTERISATION AND MODELLING OF DEGRADATION MECHANISMS IN RF MEMS CAPACITIVE SWITCHES DURING HOLD-DOWN OPERATION

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“They don’t think it be like it is, but it do”

- Oscar Charles Gamble

ABSTRACT

RF MEMS switches represent an attractive alternative technology to current mechanical (e.g. coaxial and waveguide) and solid-state (e.g. PIN diode and FET transistor) RF switch technologies. The materials and fabrication techniques used in MEMS manufacture enable mechanically moveable devices with high RF performance to be fabricated on a miniature scale. However, the operation of these devices is affected by several mechanical and electrical reliability concerns which limit device lifetimes and have so far prevented the widespread adoption and commercialisation of RF MEMS. While a significant amount of research and development on RF MEMS reliability has been performed in recent years, the degradation mechanisms responsible for these reliability concerns are still poorly understood. This is due to the multi-physical nature of MEMS switches where multiple mechanical and electrical degradation mechanisms can simultaneously affect device behaviour with no clear way of distinguishing between their individual effects. As such, little progress has been made in proposing solutions to these reliability concerns. While some RF MEMS switches have recently been commercialised, their success has come at the expense of decreased performance due to design changes necessarily imposed to prevent device failure. However, more high performance switches could be developed if the mechanisms responsible for reliability problems could be understood and solved.

The work of this thesis is focussed on the isolation and study of individual reliability mechanisms in RF MEMS capacitive switches. A bipolar hold-down technique is used to minimise the effects of dielectric charging and allow mechanical degradation to be studied in isolation in aluminium-based capacitive switches. An investigation of mechanical degradation leads to the identification of grain boundary sliding as the physical process responsible for the decreased mechanical performance of a switch. An alternative material for the switch movable electrode is investigated and shown to be mechanically robust.

The effects of dielectric charging are isolated from mechanical degradation using mechanically robust switches. The isolated investigation of dielectric charging leads to the identification of two major charging mechanisms which take place at the bulk and surface of the dielectric, respectively. The exchange of charge from interface traps is identified as the physical mechanism responsible for bulk dielectric charging. An investigation of surface dielectric charging reveals how this reliability concern depends on the structure and design of a switch. Finally, electrical and material means of minimising dielectric charging are investigated.

The findings and results presented in this thesis represent a significant contribution to the state-of-the-art understanding of RF MEMS capacitive switch reliability. By implementing the design changes and material solutions proposed in this work, the performance and lifetime of RF MEMS capacitive switches can be greatly improved.

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I, Cormac Ryan, certify that this thesis is my own work and I have not obtained a degree in this university or elsewhere on the basis of the work submitted herein.

Cormac Ryan

CHAPTER 1: INTRODUCTION

1.1 WHAT ARE MEMS?

The inspiration for Micro-Electro-Mechanical Systems or MEMS technology is said to have originated from the renowned physicist Richard Feynman who spoke about the possibilities of making small but moveable machines during his 1959 lecture entitled “There’s plenty of room at the bottom”. To encourage research into this area, he offered a prize of $1000 to the first person who could successfully make a working electric motor measuring only 1/64 of an inch in size. This prize was claimed less than a year later and thus the age of micro-machines was born. Research and development into the miniaturization of electronic components and movable machines continued throughout the following decades, with several examples of MEMS technologies demonstrating the viability of the emerging field.

In general, MEMS technology can be described as miniature mechanical structures (such as suspended bridges, beams, cantilevers or membranes) which are designed to sense or change some property of their immediate environment. The movement of these micron-scale (1 µm = 0.000001 m) mechanical components creates, or is caused by, an electrical signal. The sensing and actuation ability provided by these devices has many potential applications in widely-varying fields such as physics, optics, chemistry and biology. Many MEMS devices have achieved commercial success as the print heads in inkjet printers, accelerometers for airbag deployment in cars, as well as gyroscopes and inertial measurement units for mobile phone, tablet and video game interfaces.

Another area where MEMS technology is expected to find widespread use is in the field of radio-frequency (RF) communications. Modern smartphones and emerging tuneable devices require high-performance and low-loss reconfigurable resonant circuits to meet the growing demands of ubiquitous connectivity placed on device manufacturers by consumers and consumer applications. With their unique ability to integrate electronic components with three-dimensional movement, RF MEMS are poised as a key enabling technology for the realisation of virtually parasitic-free RF components and reconfigurable circuits. While several examples of RF MEMS-enabled tuneable components such as phase shifters, filters and impedance-matching networks have already been demonstrated, many challenges in the design and fabrication of RF MEMS remain to be overcome.

A device of particular interest to RF designers and engineers is an RF switch – a device which, as its name suggests, allows the transmission of a radio-frequency signal to be turned on or off. Conceptually this is a relatively simple device; it consists of two parallel metal plates, one of which can move with respect to the other. The position of these plates determines whether a signal can flow or is blocked. Signal transmission is achieved through ohmic (metal-metal) or capacitive (metal-dielectric-metal) contact between the plates. Their three-dimensional metal structure and mechanical movement combine to create RF switches with very low insertion loss and high isolation at microwave frequencies, while their fabrication methods are similar to those used in standard CMOS manufacturing and allow for high volume batch fabrication. Additionally, RF MEMS switches are small in size and weight and consume almost no power when they are operated using electrostatic actuation.

These advantageous properties allow RF MEMS switches to compete successfully with traditional electromechanical and semiconductor technologies and make them very suitable components for use in portable devices and wireless communications applications. Due to their outstanding commercial potential and high RF performance there is a significant amount of research being performed on MEMS switches amongst leading universities, research centres and semiconductor manufacturing companies including Lehigh University, IMEC, Robert Bosch, ST-Microelectronics, Texas Instruments and Hewlett Packard. Significantly, RF MEMS ohmic and capacitive switches have recently been commercialised by Analog Devices, WiSpry Inc. and Cavendish Kinetics.

1.2 THESIS MOTIVATION

While some examples of RF MEMS ohmic and capacitive switches have successfully been commercialised, the widespread adoption of this technology is stymied by several on-going reliability concerns which threaten the long-term operation of these devices. The operation of these switches is determined by the interaction of several fundamental electronic and mechanical forces which can be influenced by many detrimental mechanisms. Mechanical degradation of the moveable components can change the operational parameters of a switch over time, while the accumulation of charge in the dielectric layer of a capacitive switch can affect the forces acting on a device and cause it to fail in the ON or OFF state. While the successful commercialisation of ohmic switches suggests that mechanical concerns have been solved, capacitive switches have only achieved commercial success by removing or restricting contact with the dielectric layer – a key component which

determines the high RF performance of a switch. As such, the high RF performance of these devices has been sacrificed in exchange for more reliable operation and therefore more research and development is required before the full potential of RF MEMS capacitive switches can be unlocked.

This thesis investigates the mechanical and electrical reliability concerns of RF MEMS capacitive switches by investigating the fundamental physical mechanisms responsible for these effects. The major goal of this work is to contribute to the state-of-the-art understanding and improvement of RF MEMS reliability. This work is performed solely on devices fabricated at Tyndall National Institute; however, it is envisioned that the experimental methodology, physical understanding and solutions developed herein can be applied to other RF MEMS technologies across the wider field of research.

1.3 THESIS ORGANISATION

This chapter briefly introduces MEMS technology and describes the motivation behind this research. The rest of the thesis is organised as follows:

Chapter 2 introduces RF MEMS ohmic and capacitive switches and highlights their attractive properties by comparison with existing commercial RF switches. The fabrication process and theory of operation of capacitive switches is described in detail and their main reliability issues are briefly introduced.

Chapter 3 describes the effects of mechanical degradation and dielectric charging on the operational characteristics of a capacitive switch. A review of the current research status and understanding of degradation mechanisms in RF MEMS capacitive switches during hold-down operation is provided and the main goals and research methodology of this work are defined.

Chapter 4 presents the results of an experimental investigation into mechanical degradation in RF MEMS capacitive switches. This investigation is performed using an electrical test method which minimises the effects of dielectric charging during device operation. Experimental results which validate this method are presented, and the physical processes of mechanical degradation in RF MEMS capacitive switches are identified. The characterisation of a material solution to the problem of mechanical degradation is also described.

Chapter 5 describes the results of an experimental investigation into dielectric charging in RF MEMS capacitive switches. Fixed metal-insulator-metal devices are used to measure the charging and discharging currents across metal/dielectric interfaces and the knowledge gained by studying these currents is used to create a simple 1D model of dielectric charging in RF MEMS capacitive switches. Experimental verification of this model is provided and the physical process of bulk dielectric charging is identified.

Chapter 6 describes the measurement and analysis of dielectric charging at high electric fields in RF MEMS capacitive switches. Different capacitive switch test structures are used to identify the sources of surface charging at high electric fields, while a more limiting reliability concern is linked to the mechanism of bulk dielectric charging identified in Chapter 5. A novel material solution is proposed to eliminate this process and improve the reliability of RF MEMS capacitive switches.

Finally, **Chapter 7** reviews the main results achieved during this work, summarises their contribution to the state-of-the-art understanding of RF MEMS reliability and suggests some possible directions for future work.

CHAPTER 2:

RF MEMS SWITCH TECHNOLOGY

2.1 INTRODUCTION

A brief introduction to RF MEMS and the motivation behind this research was given in Chapter 1. This chapter provides a more detailed description of RF MEMS switch technology and is organised as follows. Section 2.2 describes the motivation for research into RF MEMS capacitive switches by comparing their performance with the alternative RF switches which are commercially-available today. RF MEMS capacitive switches have the potential to be the highest-performing RF switches; however, more work is required to improve their reliability before they can be commercialised. Following this, the RF MEMS capacitive switches which are studied in this thesis are described in detail in Section 2.3. A step-by-step description of their fabrication methods is presented, before the physics behind their principle of operation is used to derive the equations for the pull-in and pull-out voltage – two parameters which will be studied extensively throughout this work. Finally, the subject of RF MEMS reliability is introduced in Section 2.4 before the chapter concludes in Section 2.5.

2.2 WHY RF MEMS SWITCHES?

The term Radio Frequency (RF) is used to describe microwave signals with frequencies in the range of 3 kHz to 300 GHz which are used in a broad spectrum of radio communication applications. One of the highest volume RF device types in use today are switches which can control the flow of RF signals along transmission paths. Typical microwave applications include wireless communication systems (e.g. mobile phones), navigation systems (e.g. Global Positioning System – GPS), test equipment (e.g. Vector Network Analyser – VNA) and many others. Many varieties of RF switches are commercially available and can be divided into three main categories;

1. electromechanical relays,
2. solid-state switches,
3. Micro-Electro-Mechanical-Systems (MEMS) switches.

Electromechanical relays are widely used in the fields of test equipment or space communication where high performance is an important requirement, while smaller, faster and more reliable solid-state switches find use in consumer electronics such as mobile phones. The third RF switch technology, MEMS, combines the excellent RF performance of traditional electromechanical relays with the small size and integration capability of solid-state devices [1]. For many years RF MEMS switches were considered to be an emerging technology; however, their recent commercialisation by several companies has proven their maturity and applicability in several RF applications [2-4]. A brief description of each technology is given below.

Electromechanical relays such as coaxial and waveguide switches are mechanical switches which physically close or open an electrical circuit to control the propagation of a RF signal. In the ON-state, the signal flows through the device while in the OFF-state the signal is blocked. A simplified schematic of an electromechanical relay along with an actual device is shown in Figure 2.1 (a) and 2.1 (b), respectively. Four different elements are incorporated into the design of an electromechanical switch; an electromagnet, a moveable armature, a spring and a set of electrical contacts. When a current flows along the coiled wire in the figure, electromagnetic induction in the solenoid causes the armature to move into the closed position under the influence of an induced magnetic field. When the solenoid current is turned off, the magnetic field vanishes and the armature returns to the open position under the restoring force of the spring.

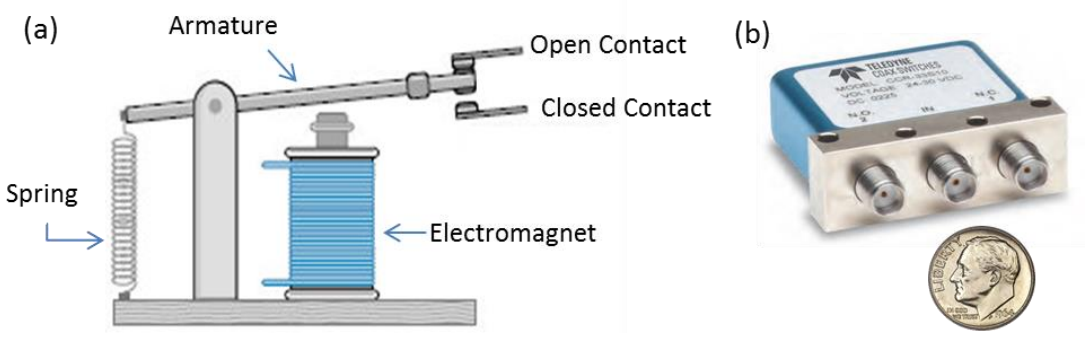

Figure 2.1: Schematic drawing of an electromechanical relay (a) and an actual electromechanical RF switch [5] next to a US 10 cent coin for comparison (b).

An alternative switching technology exists in the form of solid-state RF switches. One example of a commonly-used solid-state switch is the PIN diode which is drawn schematically in Figure 2.2 [6]. Solid-state switches can also be created using field-effect transistors (FETs); however, for brevity only the PIN diode is discussed here. A PIN diode is

made from a layer of intrinsic semiconductor with very high resistivity that is sandwiched between a layer of highly doped p-type semiconductor and a layer of highly doped n-type semiconductor. A schematic device is shown in Figure 2.2 (a). Under reverse bias conditions the intrinsic layer is depleted of charges and the device exhibits high resistance (the device is in the OFF-state). When the diode is forward biased, positive charges from the p-type region and negative charges from the n-type region are injected in to the intrinsic layer which results in lowering the device resistance (the device is in the ON-state). The circuit diagrams and equivalent circuits of a PIN diode in the OFF and ON state are shown in Figure 2.2 (b) [6].

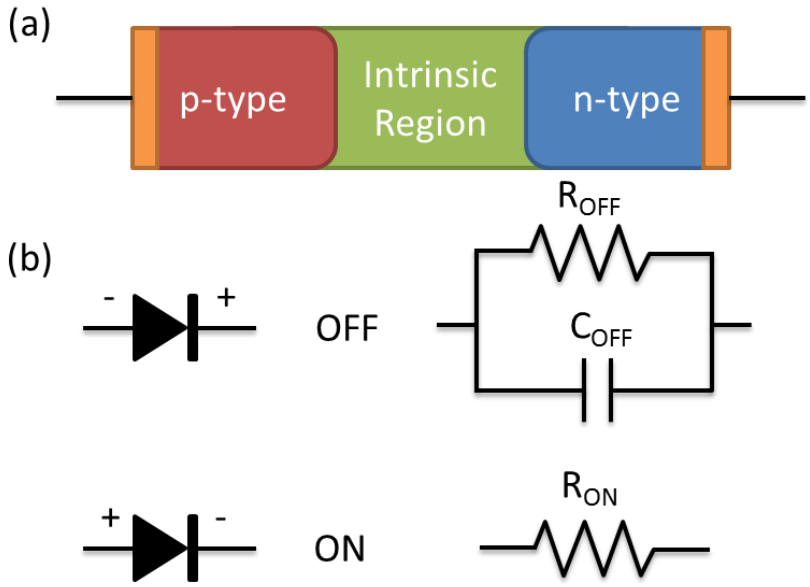

Figure 2.2: Schematic view of a solid-state PIN diode (a). Circuit diagrams and the equivalent circuits of a PIN diode under reverse-biased (OFF) and forward-biased (ON) conditions (b).

One of the most common performance specifications of RF switches is the ON-state resistance. Electromechanical relays typically have the lowest ON-state resistance due to the metal-based contact used in these devices. For example, values in the range of tens of mΩ are common for electromechanical switches, while solid-state devices with semiconductor-based switching have an ON-state resistance in the range of hundreds of mΩ. In RF switches, the ON-state resistance is encapsulated in the term “insertion loss” which is expressed in decibels and which is a measure of the power lost by a microwave signal as it flows through a device [7]. Lower levels of insertion loss mean that less signal power is lost during transmission and this can be achieved by minimizing the ON-state resistance of a switch.

Another important performance specification of RF switches is the amount of power lost by a signal through unwanted transmission in the OFF-state. Solid-state switches minimise unwanted losses by maximising the resistance of the intrinsic layer during the OFF-state. However, parasitic capacitive coupling can result in signal leakage through this layer [8]. The amount of signal power lost through an electromechanical switch is extremely low due to the physical separation between the switch contacts in the OFF-state. However, capacitive coupling across the air gap can result in parasitic signal losses, especially as the frequency of the signal increases. In RF switches the property of a device which determines signal loss in the OFF-state is called "isolation" and is measured in decibels. A higher isolation means that less signal flows through the switch when it is in the OFF-state and this can be achieved by maximising the OFF-state resistance or minimising the OFF-state capacitance.

In summary, the advantages of electromechanical relays over solid-state switches are that they provide better RF characteristics over a wider frequency range, with lower insertion loss due to metal contact and higher isolation levels due to air-gap separation [9]. However, the lack of moving parts in a solid-state switch leads to faster switching speeds (μs vs. ms) and improved long-term reliability with more consistent RF performance as the switch contacts do not degrade over time. Additionally, solid-state switches can be manufactured more cost effectively than electromechanical relays using high-volume semiconductor-based processes which also result in much smaller devices than bulky electromechanical relays (mm^3 vs. cm^3). Therefore, electromechanical relays are most often used in low volume applications with high-performance RF specifications where the cost and size of the equipment is not a primary concern.

The third RF switching technology is MEMS and a simplified diagram of a MEMS switch with a metal to metal (ohmic) contact is shown in Figure 2.3 (a). MEMS ohmic switches operate on the same principle as electromechanical relays; an electrical stimulus causes movement of a metal armature which closes or opens the circuit, thereby allowing or preventing the transmission of a RF signal. However, unlike traditional electromechanical relays, the movement of a MEMS switch armature is most often accomplished using electrostatic actuation which will be described in Section 2.3.2.

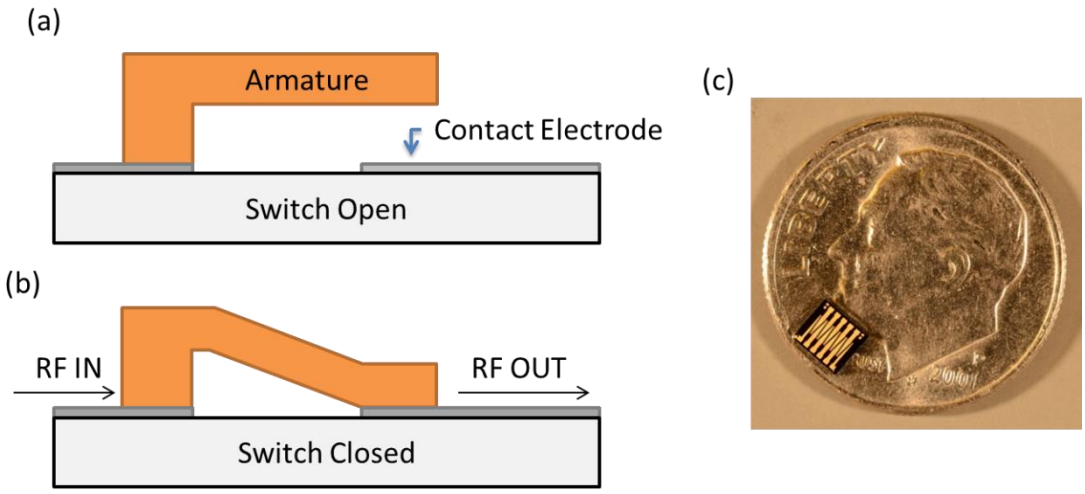

Figure 2.3: Schematic drawing of a MEMS ohmic switch in the OFF-state (a) and in the ON-state (b). A packaged die containing 400 MEMS ohmic switches placed on top of a US 10 cent coin for comparison, courtesy of General Electric (c).

RF MEMS switches are fabricated using surface micromachining and lithography techniques which are similar to those used in the fabrication of solid-state devices [10]. MEMS processing involves the deposition, patterning and etching of individual material layers to create micron-scale freestanding mechanical structures. The fabrication steps used in the creation of MEMS devices are discussed in detail in Section 2.3.1. The use of metal contacts and the physical separation between the switch electrodes means that the insertion loss and isolation of MEMS switches are comparable to traditional electromechanical switches, while the small size and weight of MEMS devices is an advantageous property derived from the use of solid-state manufacturing techniques [11]. A comparison between the properties of RF MEMS ohmic switches, electromechanical relays and PIN diodes is shown in the following table. Further details can be found in [12].

Table 2.1: A comparison between the physical and RF properties of three different RF switch technologies.

Property	Electromechanical Relay [5, 13]	PIN Diode [14]	MEMS Ohmic Switch [4, 15]
Insertion Loss	Low	Medium	Low
Isolation	High	Low	Medium
ON Resistance	Low	High	Medium
Signal Range	DC – 40 GHz	DC – 3 GHz	DC – 11 GHz
Switching Speed	Slow	Very Fast	Fast
Size	Large	Small	Small
Weight	Heavy	Light	Light
Cost per unit	$100-1000	$0.08	$10-100 desired
Lifetime (Cycles)	10 Million	Billions	5 Billion

By comparison with existing RF switch technologies it can be seen that RF MEMS are a very attractive alternative to traditional electromechanical and solid-state switches. A significant amount of research and development has been performed on MEMS devices and has culminated in the recent commercialisation of an ohmic switch by Analog devices [4, 15]. A diagram of this switch is shown in Figure 2.4. The device is constructed from a surface micromachined gold cantilever which is suspended 0.6 µm above the actuation (gate) electrode. Despite the small air-gap, the switch requires an actuation voltage of 80 V which is supplied by a co-packaged application specific integrated circuit (ASIC). Electrostatic actuation of the cantilever is achieved by applying the voltage between the beam and the gate electrode, and further details of this actuation mechanism are given in Section 2.3.2. The high actuation voltage and the use of a platinum group metal in the contact areas provide the switch with a low ON-state resistance of 1.5 Ω. Once the devices have been fabricated they are hermetically sealed using a wafer capping process to improve the switch reliability and lifetime. A discussion of RF MEMS reliability is given in Section 2.4. Targeted application areas include RF instrumentation such as switching matrices and vector network analysers where wide bandwidth, low loss switching is required.

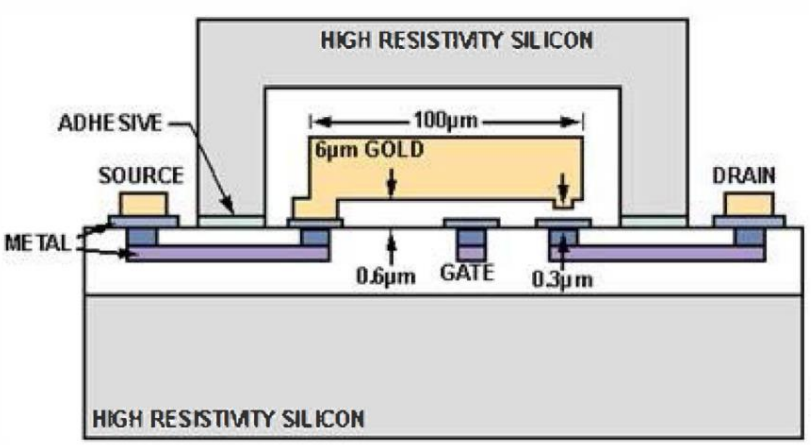

Figure 2.4: Diagram of the commercial ohmic switch from Analog devices [4].

RF MEMS Capacitive Switches (Variable Capacitors)

Another type of RF MEMS switch operates by changing the capacitance of a transmission line and this is known as a capacitive switch or a digital variable capacitor (varactor). A schematic diagram of a capacitive switch with simplified circuit models is shown in Figure 2.5. In general, capacitive switches are very similar in design and operation to ohmic switches. The mechanical principle of operation is the same in both devices whereby the moving electrode lies in one of two available positions that define the switch ON or OFF state. However, capacitive switches incorporate a dielectric layer between the moveable metal and contact electrode so that a metal-insulator-metal structure is formed after switch actuation. The dielectric layer prevents any DC signal from passing through the switch, but allows low-loss switching of high-frequency signals to be performed [11]. As such, capacitive switches and varactors are expected to find use in different applications to ohmic switches where capacitance changes are required to tune RF signals in wireless and satellite communications systems, as well as high-frequency instrumentation and radar applications [16]. Further details on capacitive switches can be found in Section 2.3.

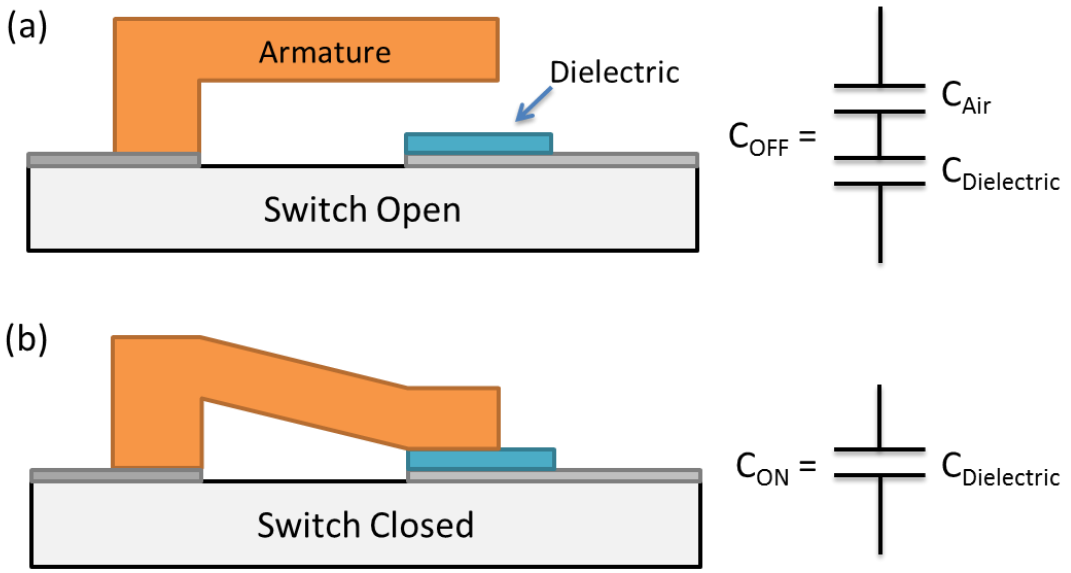

Figure 2.5: Schematic drawing of a RF MEMS capacitive switch in the OFF-state (a) and in the ON-state (b). Simplified circuit models are provided to the right of the figure.

RF MEMS capacitive switches for mobile phone applications have recently been released by WiSpry [17] and Cavendish Kinetics [18]. A diagram of the capacitive switch from Cavendish is shown in Figure 2.6. The switch is made from a bulk micromachined metal cantilever which is fully integrated within the back-end of a CMOS fabrication process. Electrostatic actuation is used to control the switch; a voltage applied between the beam and a central actuation electrode causes the cantilever to deflect and change the capacitance of the switch. However, mechanical stoppers at the contact electrode prevent the complete closure of the switch such that the variable capacitance is determined by the size of the air-gap between the cantilever and the contact electrode. Therefore, this is an air-based variable capacitor.

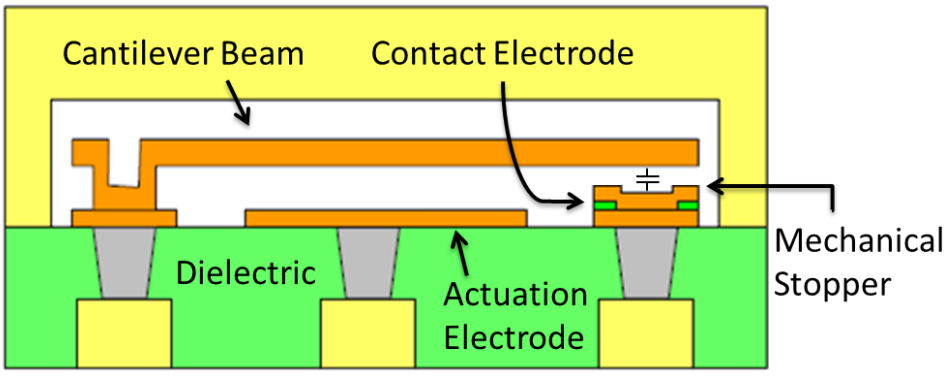

Figure 2.6: Graphical representations of the air-based capacitive switch by Cavendish Kinetics [2].

The commercial product offered by Cavendish Kinetics features arrays of these capacitive switches which can provide a high-resolution digitally-controlled variable capacitance [19]. These capacitive tuners are currently in use in several smartphones including the ZTE Nubia Z9 [20]. The capacitive switch from WiSpry is targeted at similar applications in the tuneable RF front-end market [3].

Variable capacitors can also be fabricated using different technologies such as ferroelectric varactors [21] or by placing low-loss switches in series with fixed capacitors (switched passives) [1]. For example, low-loss semiconductor switches using PIN diodes can be used to connect or disconnect arrays of fixed capacitors to achieve a digitally-controlled variable capacitance. Ferroelectric materials such as barium-strontium-titanate (BST) are used to linearly tune a capacitance over a small range by changing the electric permittivity as a function of the applied electric field [22]. A figure of merit recently defined by WiSpry [3] allows different capacitor technologies to be compared based on their performance metrics. This figure of merit is given as

$$FOM = \frac{1}{C_{on}R_{on}} \times \frac{C_{on}}{C_{off}} \times \frac{C_{on}}{Area} \times V_{rms}^2, \tag{2.1}$$

where a high FOM is associated with high performance. The first term on the right hand side of equation (2.1) represents the Q-factor of a device which indicates the performance of a switch in terms of signal losses. For a given on-state capacitance C_{on}, the value of Q can be maximised by minimising the value of R_{on}. The second term on the right hand side of equation (2.1) is the capacitance ratio of the device. Again for a given C_{on} this value can be maximised by minimising C_{off}, where a low C_{off} contributes to high isolation, while a high C_{on} is essential to create a low-impedance path for the RF signal. Thus, the capacitance ratio of a device also represents the performance of a switch in terms of signal losses; however, a trade-off exists between maximising the Q-factor and capacitance ratio of a device. The third term in equation (2.1) represents the capacitance density of a device, or the cost of achieving a certain tuning range in terms of overall die area. The final V_{rms}^2 term represents the power-handling ability of a tuneable capacitor. Detailed comparisons of several different tuneable capacitor technologies can be found in [1, 3, 21] and these are summarised in the following table.

Table 2.2: Tuneable capacitor technology comparison, adapted from [1, 3, 21].

Technology	MEMS	BST	Silicon on Insulator
Implementation	Digital Capacitor	Analog Variable Cap.	Switched Passives
Cap. Ratio	2-100	2-3	3-5
Q-Factor	50-400	30-150	30-150
Linearity, IIP3 (dBm)	>60	10-35	10-35
FOM	100+	<10	10+

An additional parameter which is important for the comparison of tuneable capacitors is the linearity of a device. Very linear devices create almost no distortion of an RF signal as it passes through, while intermodulation products generated in nonlinear devices can corrupt the transmitted signal. The three-dimensional design of RF MEMS digital capacitors contributes to the very high linearity reported in Table 2.1, as the ON-state capacitance of the MEMS switch does not vary with voltage, while the low mechanical resonant frequency of the moveable component cannot physically react to the passage of a high-frequency signal and creates no distortion [23]. Modern BST and semiconductor-based varactors are also very linear devices; however, their voltage-dependent capacitance leads to a lower linearity than MEMS switches [21].

In conclusion, it can be stated that high-performance capacitive tuners are devices with a low series resistance, a high tuning range and high linearity. The freedom of design of RF MEMS capacitive switches allows each of these criteria to be fulfilled [11] and results in the largest figure of merit of the different technologies described in Table 2.2. By examining equation (2.1), it can be seen that the figure of merit of a RF MEMS capacitive switch can be maximised by increasing the on-state capacitance of a device. This can be achieved through intimate contact between the RF electrode and a dielectric layer in the ON-state. Thus, the intermetal dielectric layer is an essential component for the realisation of high-performance RF MEMS capacitive switches. However, the commercial devices which have been released to-date avoid the use of intermetal dielectric layers in favour of air-based capacitive tuning (as employed by Cavendish Kinetics [19]) or else use mechanical stoppers to prevent intimate contact between the moveable metal and dielectric (as used by WiSpry [17]). The reason for this deliberate decrease in on-state capacitance and RF performance is due to the accumulation of charge in the dielectric layer of a capacitive switch during

operation which poses a significant threat to the reliability and lifetime of these devices [24-33].

In addition to the decreased performance caused by the lack of an intermetal dielectric in RF MEMS capacitive switches and varactors, the switch lifetime during hold-down operation has not been published for the majority of commercial devices. This is a key performance indicator for a number of applications such as redundancy switches for satellites and test instrumentation which are required to maintain their electromechanical performance and guarantee switch actuation after 10 years [34]. While the ohmic and capacitive switches commercialised by Analog Devices and Cavendish Kinetics have demonstrated cycling lifetimes of over 1 billion cycles [4, 19], only Analog Devices have reported an estimated hold-down lifetime for their ohmic switch of 7.2 years [4]. However, this is below the hold-down lifetime of 10 years or more which is required for commercial and military applications [34].

Improving the poor hold-down reliability of RF MEMS switches is hampered by a lack of understanding of the failure modes of a switch during down-state operation, even for commercial devices which have removed the intermetal dielectric layer for improved reliability. Therefore, the goal of this work is to develop an in-depth understanding of the failure modes of dielectric-based RF MEMS capacitive switches during hold-down operation. This work is performed using capacitive switches which were specifically designed at Tyndall National Institute to investigate the impact of the intermetal dielectric degradation and charging on switch performance. A description of this technology along with details of its fabrication and physics of operation is given in the next section. A discussion of the reliability concerns of RF MEMS capacitive switches during hold-down operation is given in Chapter 3; while more a more general introduction to the area of RF MEMS reliability is given in Section 2.4.

2.3 RF MEMS TECHNOLOGY AT TYNDALL NATIONAL INSTITUTE

A scanning electron microscope (SEM) image and cross-section of a typical RF MEMS capacitive switch fabricated in Tyndall are shown in Figure 2.6. The switch consists of a moveable metal membrane which is suspended by four supporting tethers over the central line of a co-planar waveguide (CPW) structure. The membrane measures 100x100 μm^2 and is composed of 1 µm thick aluminium. Holes of 2x2 µm are incorporated into the membrane to reduce gas damping effects [11] and to aid in sacrificial layer removal (see

next section). The membrane is suspended approximately 2.5-3 µm into the air. A voltage applied between the membrane and the central line of CPW causes the switch to close forming a metal-dielectric-metal structure. The typical measured actuation voltage of such a device lies in the range of 10-25 V depending on the size of the air gap and the tether design used. The CPW line is designed to have an impedance of 50 Ω, and the bottom metal used to define the CPW is 0.5 µm thick aluminium alloyed with 1% silicon (Al/1%Si).

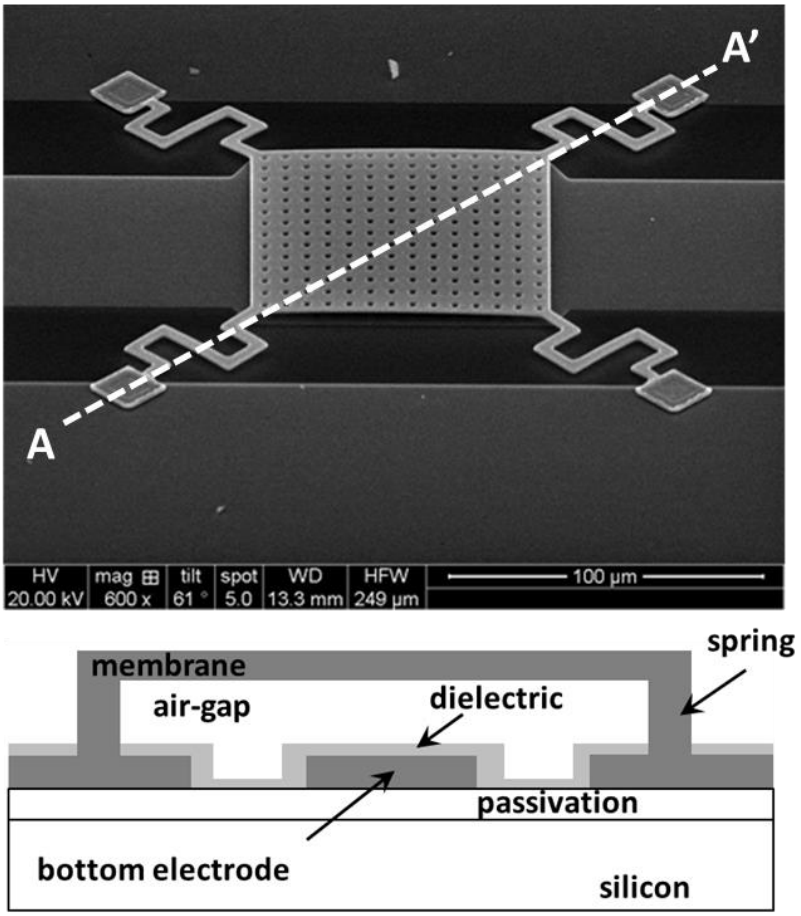

Figure 2.7: SEM image and cross-section of a capacitive switch with meander tethers fabricated at Tyndall. The cross-section is measured along the line A-A' as shown in the SEM image.

A dielectric layer of 130 nm is deposited on top of the CPW. This layer is present on the switch featured in Figure 2.7, but is transparent in the SEM image. The dielectric used is typically silicon dioxide (SiO_2) with a relative permittivity of 3.9. When the switch is open this arrangement results in an up-state capacitance C_{UP} of approximately 50 fF. The theoretical down-state capacitance C_{DOWN} is 2.66 pF when calculated using the model of an ideal metal-dielectric-metal capacitor; however, poor contact between the movable membrane and the top surface of the dielectric results in a considerably reduced down-state capacitance. Measured C_{DOWN} values of 100x100 μm^2 devices vary between

300-900 fF depending on the extent of the bottom electrode roughness. The basic steps used to create these structures are outlined in the following section.

2.3.1 MEMS Fabrication

The MEMS devices used in this work are fabricated using a technique known as surface micromachining [10]. This process involves the deposition and selective etching of individual material layers to create functional devices. The process used in Tyndall National Institute has been developed to be CMOS-compatible so that MEMS devices can be incorporated on top of completed CMOS wafers without having to remove the wafers from the clean room.

The fabrication steps necessary to create Tyndall MEMS technology are described in the following order; preparation of the substrate and bottom metal definition, dielectric passivation, sacrificial layer deposition, top metal definition and finally sacrificial layer removal.

Substrate Preparation

The default substrates used in this work are low resistivity P-type silicon wafers. Prior to switch fabrication, the wafers are cleaned and an initial layer of 500 nm SiO_2 is deposited by Plasma-Enhanced Chemical Vapour Deposition (PECVD). This oxide layer is deposited to electrically isolate the finished MEMS devices from the substrate material.

Following this, a layer of Al/1%Si sputtered on top of the initial oxide to a thickness of 0.5 µm. The Al/1%Si layer is patterned and etched to define the bottom metal electrodes of the MEMS switches which in this case form a CPW structure. At this point, the wafers are ready for dielectric deposition and a wafer at this stage of device fabrication in pictured in Figure 2.8.

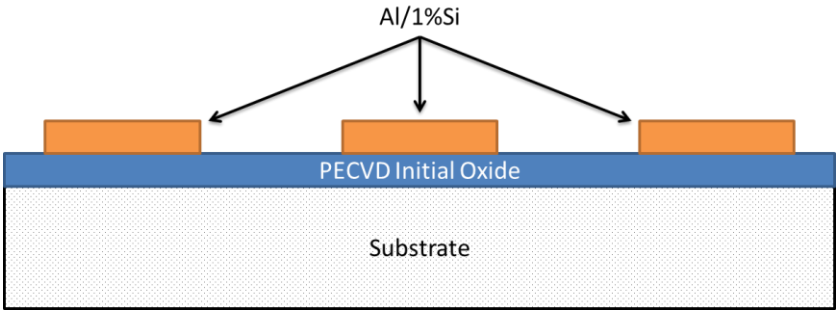

Figure 2.8: Schematic representation of the first three layers of a fabricated device.

Dielectric Passivation

The typical dielectric used in this work is PECVD SiO_2 deposited to a thickness of approximately 130 nm. Other dielectrics which may also be used include PECVD silicon nitride (SiN) and aluminium oxide (Al_2O_3) deposited by an alternative technique called atomic layer deposition (ALD). After deposition the oxide is patterned by exposing and selectively developing a layer of photoresist, as before. The dielectric is removed over regions where the switch membrane will be electrically connected to the CPW, and also from other regions of the CPW for device probing and wire-bonding purposes. A schematic representation of a device after this stage of the process is shown in Figure 2.9.

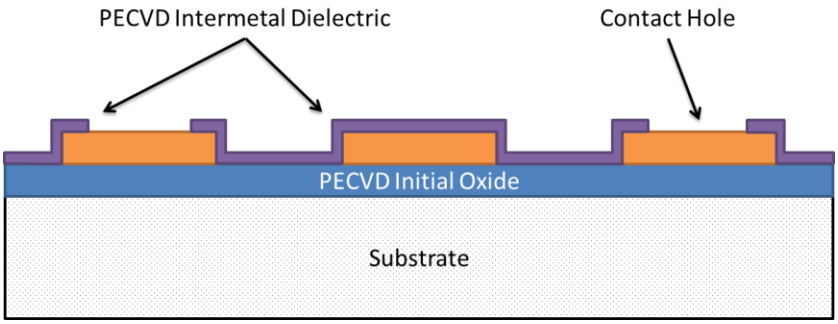

Figure 2.9: Cross-section of a device after the intermetal dielectric has been deposited and etched.

Sacrificial Layer Deposition

The sacrificial layer is a fundamental step in surface micromachining as it allows three-dimensional freestanding structures to be defined. In this case the sacrificial layer is formed using a polymer material known as polyimide (PI 2545). The polyimide is deposited onto a wafer by spin-coating to a thickness of approximately 3 µm before it is cured in an oven to solidify. The polyimide is patterned using photoresist exposition and development steps, before it is etched using oxygen plasma to define openings for the supporting anchors of the switch membrane. This stage of the fabrication process is shown in Figure 2.10.

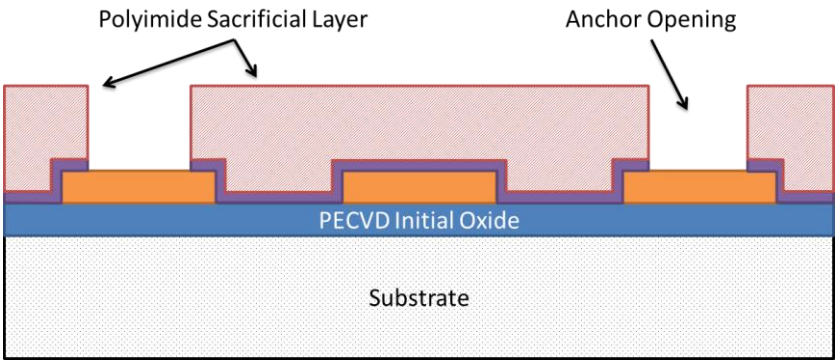

Figure 2.10: Schematic drawing of a device after the polyimide deposition and patterning process.

The final thickness of the polyimide layer after etching and resist removal is in the range of 2.5-3 µm. The thickness of this layer is critically important in MEMS fabrication as it defines the height of the device air-gap and hence the operational characteristics of a finished switch. Any roughness or inhomogeneity of the top surface of the polyimide may also negatively affect the topography of the top metal in the next fabrication step.

Top Metal Definition

Once the polyimide has been appropriately prepared the top metal is deposited using an RF sputter technique. Different metal targets may be used in the sputtering process to deposit various materials. Examples of metals used in the Tyndall process include aluminium and titanium. The metal deposition is performed at room temperature to minimize the creation of residual stress in the membrane. The switches used in this work have all been fabricated with a top metal thickness of 1 µm. After deposition, the top metal is patterned and etched to form the primary structural layers of the MEMS switches. A cross-section of a device after top metal deposition and etching is shown in Figure 2.11.

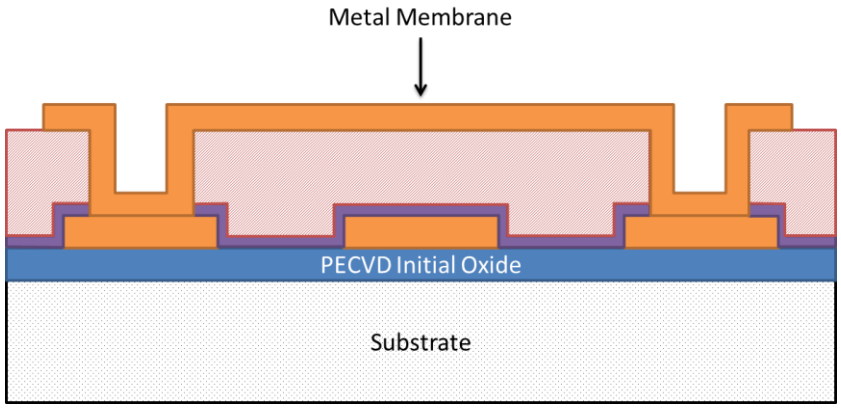

Figure 2.11: Cross-section of a device after deposition and patterning of the top metal.

Sacrificial Layer Removal

The release etch of the polyimide sacrificial layer is the final step in MEMS fabrication. This is achieved by placing the wafer into an oxygen plasma system at room temperature, where the polyimide is gradually removed during repeated etching cycles. Once the sacrificial layer has been completely removed the top metal is able to move freely and is only suspended by the four supporting tethers. A cross-section of a fully-processed capacitive switch is shown in Figure 2.12.

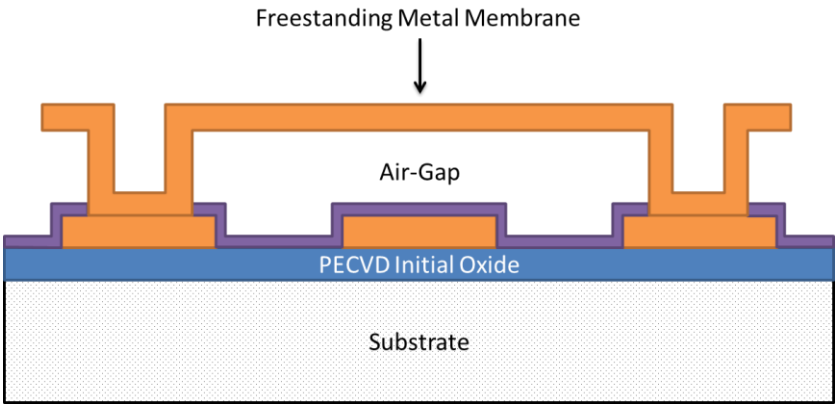

Figure 2.12: Schematic cross-section of a fully-processed capacitive switch after sacrificial layer removal.

The schematic drawings featured in the previous images are simplified descriptions of the capacitive switches which are useful for describing particular features of device design or operation. However, all capacitive switches used in this work are suspended on four springs similar to the device shown in Figure 2.7. Variations in device design include the use of different supporting tethers to alter the spring constant and operational parameters of a switch. The following images show close-up details of fully-processed capacitive switches captured using a scanning electron microscope.

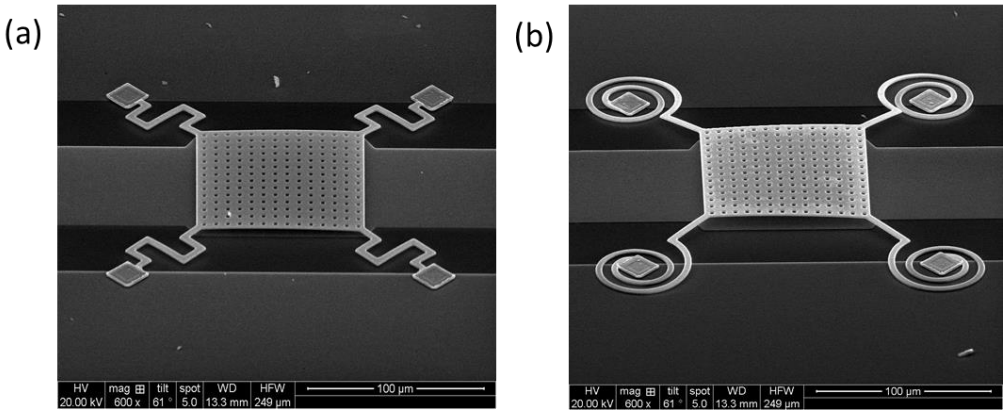

Figure 2.13: SEM images of fully-processed capacitive MEMS switches. A meander-type switch over a CPW (a) and a spiral-type switch over a CPW (b).

2.3.2 Electromechanical Model of Switch Operation

A simple one-dimensional model of a capacitive switch is shown in Figure 2.14.

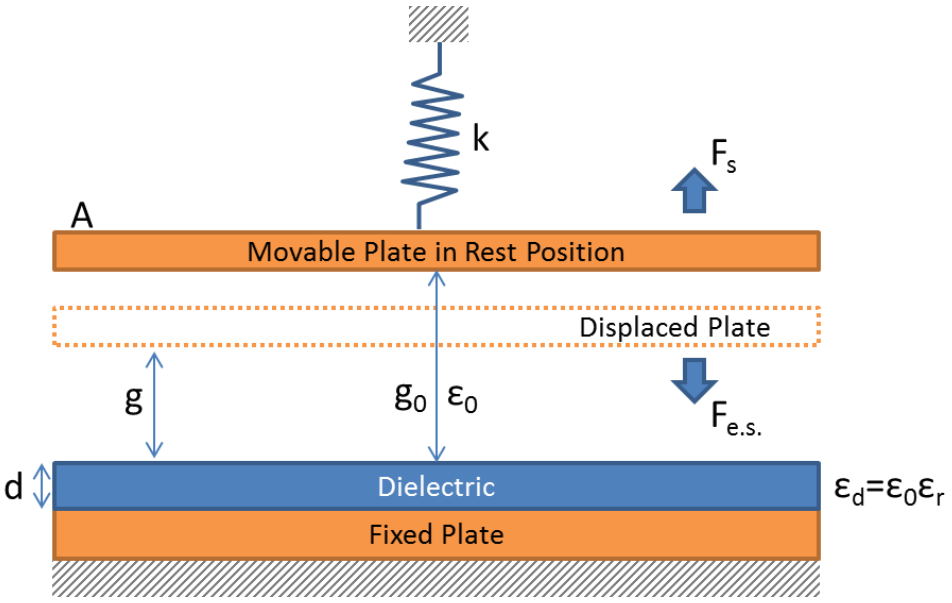

Figure 2.14: Simple 1D model of an RF MEMS capacitive switch.

In this model, the movable membrane of a capacitive switch is represented by a rigid metal plate of area A which is suspended from a fixed point by a linear spring. The representation of the moveable membrane as a rigid plate is justified by simulation results which revealed that the majority of bending takes place in the supporting tethers while the membrane remains relatively flat throughout device actuation [35]. The linear spring has an effective spring constant k which is used in lieu of the four supporting tethers and accounts for the bending and stretching of deformed beams [11]. The movable metal plate is positioned directly over a fixed metal plate with a dielectric on top such that the structure forms a parallel-plate capacitor with capacitance given by

$$C = \frac{\varepsilon_0 A}{g + \frac{d}{\varepsilon_r}}, \tag{2.2}$$

where g is the distance between the metal plates, ε_0 is the permittivity of air, and d & ε_r are the thickness and relative dielectric constant of the dielectric layer. Equation (2.2) results from a series combination of the air and dielectric capacitances. When a voltage is applied between the two metals, an attractive electrostatic force is generated which attempts to bring the top moveable metal into contact with the bottom dielectric. The magnitude of this attractive force is given by

$$F_{e.s.} = \frac{1}{2}\frac{dC}{dg}V^2 = -\frac{1}{2}\frac{\varepsilon_0 A V^2}{\left(g + \frac{d}{\varepsilon_r}\right)^2}, \tag{2.3}$$

where V is the applied voltage and (2.2) has been differentiated to obtain $\frac{dC}{dg}$. When a voltage is applied to the switch, the induced attractive electrostatic force must compete with the restoring force generated by the spring as it is stretched beyond its rest position. The magnitude of this restoring force is given by Hooke's law as

$$F_s = -k(g_0 - g), \tag{2.4}$$

where g_0 is the size of the air-gap when no voltage is applied. As the applied voltage is increased and the distance g between the metals varies, the magnitudes of the electrostatic and restoring forces also vary. The electrostatic force increases as $1/g^2$ while the restoring force increases linearly with g so that eventually a point is reached where the attractive electrostatic force overcomes the restoring spring force and the top membrane moves into contact with the dielectric layer.

The applied voltage needed to close the switch is known as the actuation or pull-in voltage, V_{PI}. An expression for this voltage can be obtained by forming a force balance equation using equations (2.3) and (2.4)

$$\frac{1}{2}\frac{\varepsilon_0 A V^2}{\left(g + \frac{d}{\varepsilon_r}\right)^2} = k(g_0 - g), \tag{2.5}$$

and rearranging the resulting expression to generate the following equation (2.6)

$$V = \sqrt{\frac{2k}{\varepsilon_0 A}(g_0 - g)\left(g + \frac{d}{\varepsilon_r}\right)^2}. \tag{2.6}$$

By differentiating (2.6) with respect to g and solving the resulting expression when $\frac{dV}{dg} = 0$ it is found that the critical point of the force balance equation occurs when the membrane has been deflected by approximately 1/3 of the original air-gap [36]. Inserting this value into (2.6) yields the following expression for the pull-in voltage

$$V_{PI} = \sqrt{\frac{8k}{27\varepsilon_0 A}\left(g_0 + \frac{d}{\varepsilon_r}\right)^3}. \tag{2.7}$$

A schematic drawing of a capacitive switch in the OFF- and ON-state is shown in Figure 2.15, where a voltage greater than the pull-in voltage has been applied to the bottom metal.

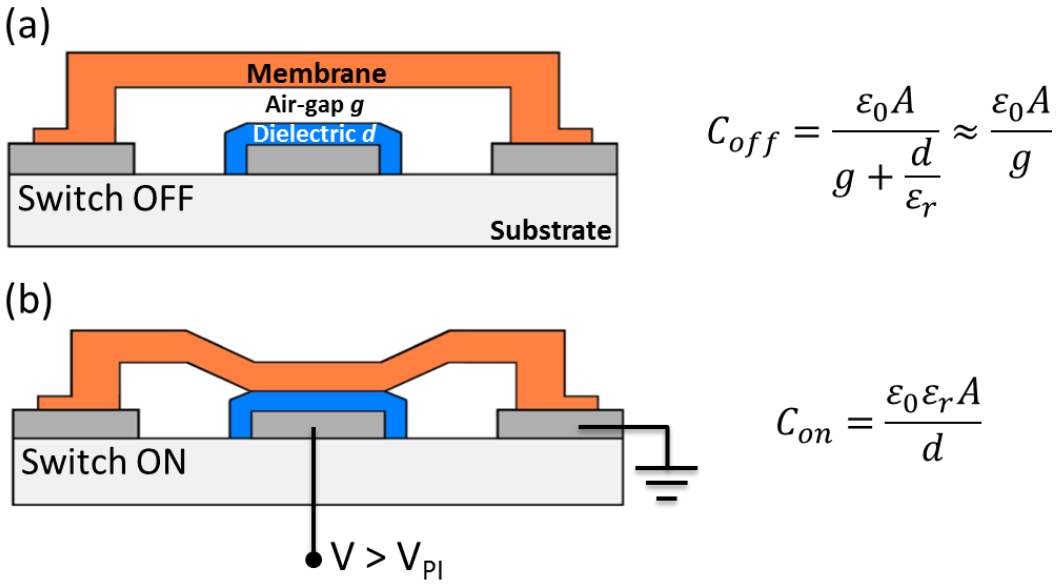

Figure 2.15: Schematic drawing of a RF MEMS capacitive switch in the off-state with no bias applied (a) and in the on-state when a voltage greater than the pull-in voltage has been applied to the bottom metal (b). Expressions for the OFF and ON state capacitances are provided to the right of the figure.

On a capacitance-voltage graph the pull-in phenomenon can be identified as a sudden increase in the value of the capacitance as the voltage is increased and the membrane moves from the up-state (i.e. air-based capacitance) to the down-state (i.e. dielectric-based capacitance). Since the electrostatic force is attractive regardless of whether a positive or negative voltage has been used, the pull-in point should be symmetrical about the zero volt mark. A representation of an ideal capacitance voltage (C-V) curve is shown in Figure 2.16.

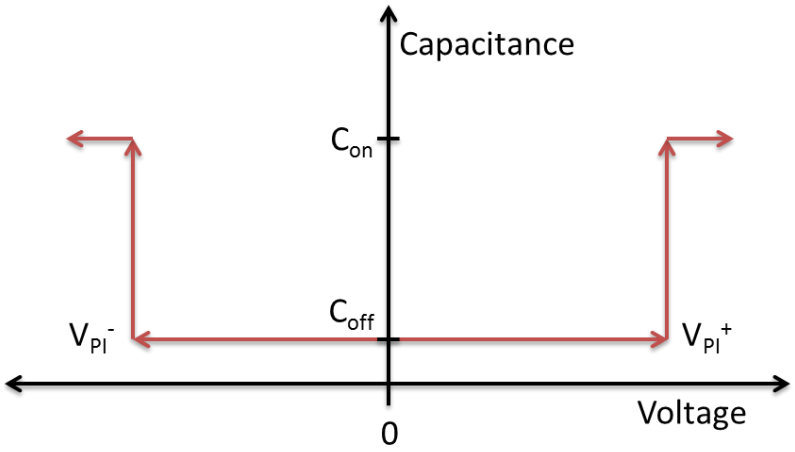

Figure 2.16: An idealised C-V curve of a MEMS capacitive switch. The evolution of the capacitance as the membrane moves from the up-state to the down-state is indicated with red arrows. In reality the off-state capacitance would not be constant but would increase slightly as the voltage approached the pull-in point.

The membrane will stay in the down-state as long as a sufficiently high voltage is applied to the device. However, the magnitude of the electrostatic force in the down-state is significantly higher than in the up-state because the distance between the electrodes is now equal to the oxide thickness. Therefore, the membrane will remain in the down-state even if the voltage is reduced below the V_{PI}. As the voltage is lowered further the magnitude of the electrostatic force decreases until the restoring spring force is greater than the attractive electrostatic force and the switch re-opens. The point at which this occurs is known as the pull-out point and the corresponding voltage is known as the pull-out voltage, V_{PO}. The difference between the pull-in and pull-out voltage results in a distinctive hysteresis of the C-V curve, as shown for an ideal capacitive switch in Figure 2.17.

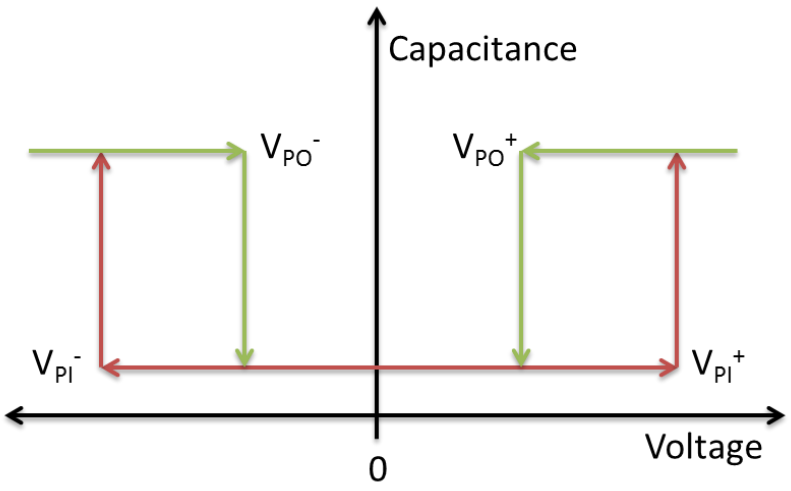

Figure 2.17: Full C-V curve of an ideal MEMS capacitive switch, showing the hysteresis between the pull-in and pull-out voltages. The evolution of the pull-out phenomenon is indicated with green arrows.

An expression for the pull-out voltage can be found by setting g = 0 in equation (2.6). Solving for V results in the following expression

$$V_{PO} = \sqrt{\frac{2k}{\varepsilon_0 A} g_0 \left(\frac{d}{\varepsilon_r}\right)^2} \,. \tag{2.8}$$

The pull-in and pull-out voltages derived in this section are widely used to characterise the reliability of RF MEMS capacitive switches. These threshold voltages change over time as a result of various degradation mechanisms and this is the subject of intense study [29, 30, 32, 37-45]. A brief introduction to the subject of RF MEMS reliability is given in the following section.

2.4 INTRODUCTION TO RF MEMS RELIABILITY AND RESEARCH AIMS

In previous years, the commercialisation of RF MEMS switches was hindered by several reliability concerns which affected the long term operation of these devices. The recent commercialisation of ohmic and capacitive switches by several companies indicates that the majority of these reliability concerns have been addressed [4, 17, 18]. However, as outlined in Section 2.2, on-going reliability concerns are preventing the commercialisation of high-performance capacitive switches which make use of intermetal dielectric layers. Indeed, the International Technology Roadmap for Semiconductors (MEMS Chapter) highlighted the continuing need to enhance the reliability and lifetime of RF MEMS switches as the biggest roadblock to their commercialisation [46]. Furthermore, the lack of

understanding of the physics of failure in these devices was identified as the primary contributing factor to their on-going reliability concerns. The failure mechanisms of RF MEMS capacitive switches can be broadly classified into extrinsic failures induced by environmental effects and intrinsic failure mechanisms caused by material degradation and these are briefly described in the following sections.

Extrinsic Reliability Issues

Many studies have shown that the lifetime of capacitive switches is influenced by the ambient conditions to which a MEMS device is exposed [47-56]. Environmental reliability concerns such as humidity and the effect of contaminants are extrinsic failure mechanisms which can be avoided by sealing devices in hermetic packages under vacuum or dry-air environments. Research into cost-effective MEMS packaging techniques is currently underway but is outside the scope of this thesis [57-61]. Moreover, the commercial devices described earlier prove that manufacturable packaging solutions have been found. Therefore, unless the package should fail, environmental concerns are no longer considered a threat to RF MEMS reliability under normal operating conditions. Additionally, while unpackaged devices are investigated in this work, all experiments are performed in a controlled dry-air environment so that environmental reliability concerns are not expected to be an issue.

Intrinsic Reliability Issues

While extrinsic failure mechanisms have been reduced, intrinsic failures due to material degradation are still being researched. These degradation mechanisms depend on the type of stress applied to a device. Initial studies were concerned with metal fatigue and fracture during cycling operation [30, 62]. However, if the moving elements of MEMS switches are designed to be several hundred microns long, while the extent of their vertical deflection is limited to several microns then mechanical failure due to fracture is not a problem [11]. Additionally, the absence of fatigue as a failure mechanism in RF MEMS has been demonstrated by the long-term cycling reliability of ohmic and capacitive switches [63-67], some of which have been shown to survive for up to 100 billion cycles without failure [68]. Early-stage capacitive switches fabricated at Tyndall National Institute have also been shown to survive for over 5 billion switching cycles without a significant change in their operational parameters [69]. The experiment had to be stopped due to time constraints on the measurement equipment and not due to device failure. Therefore, fatigue and fracture are not considered to be failure mechanisms of the capacitive switches used in this work.

As mentioned in Section 2.2, the failure modes of RF MEMS switches during hold-down operation are less well understood. For capacitive switches which use intermetal dielectric layers, the hold-down lifetime is affected by both mechanical and electrical failure mechanisms [44, 62, 70]. Mechanical degradation mechanisms such as creep and viscoelasticity can change the material properties of moveable elements during prolonged hold-down operation [71-73], while the accumulation of charge in the dielectric layers of a capacitive switch changes the electrostatic force acting on a switch membrane over time [74]. As expected from the force-balance procedure used to derive equations (2.3) – (2.7), any change in the mechanical restoring force or attractive electrostatic force as a result of mechanical degradation or dielectric charging causes a change in the pull-in and pull-out voltages of a switch.

A significant amount of research on RF MEMS reliability has been performed by studying time-dependent changes of a device C-V curve under various hold-down stress conditions [47, 49, 51, 75-91]. Initial studies attributed the observed pull-in and pull-out voltage changes to the effects of dielectric charging as mechanical degradation was assumed to be negligible [83, 92-95]. Initial research work performed by Olszewski attributed the reduction in magnitude of the pull-in and pull-out voltages (C-V narrowing) of a capacitive switch to a dielectric charging mechanism because mechanical degradation was assumed to be absent [92]. However, more recent work by Olszewski on this subject proved that mechanical degradation of the switch membrane was responsible for the observed C-V narrowing effect [96]. Additionally, recent work by other groups has shown that mechanical degradation processes such as creep and viscoelasticity are present in the thin films used in MEMS devices [97, 98].

Therefore, research groups now acknowledge that both dielectric charging and mechanical degradation effects can occur simultaneously during hold-down operation [99]. Recent research has assumed that more than one degradation mechanism is occurring in the switch and has focussed on devising ways of separating the two major reliability concerns (dielectric charging from mechanical degradation or vice versa), as unless this is achieved, individual degradation mechanisms that occur in each reliability domain cannot be properly characterised. These methods involve the creation of new measurement and analysis techniques [41, 79, 80, 100-104] or the isolated measurement of mechanical and electrical effects on dedicated test structures [71, 105-108]. A discussion of these state-of-the-art research techniques will be provided in the next chapter.

In spite of the large amount of research performed on RF MEMS reliability to date, no individual mechanical or dielectric degradation mechanisms during hold down operation have been identified in capacitive switches. It is the aim of this thesis to isolate, identify and provide solutions for these degradation mechanisms.

2.5 SUMMARY

This chapter has shown that RF MEMS can be an attractive alternative to existing RF switch technologies. Examples of recently commercialised ohmic and capacitive switches were provided. The fabrication method, physics and theory needed to understand the operation of a capacitive switch was described. The concept of RF MEMS reliability was introduced, and the reliability concerns of mechanical degradation and dielectric charging were defined as the main reasons for the delayed commercialisation of high-performance capacitive switches. These reliability concerns are active during hold-down operation, and their simultaneous presence has thus far prevented the characterisation of individual degradation mechanism in RF MEMS capacitive switches.

The following chapter will show how key device parameters change during hold-down operation as a result of mechanical degradation and dielectric charging, and will discuss how these changes may be used to identify the responsible mechanism. The state-of-the-art research techniques which are used to isolate individual reliability concerns will be discussed and a description of the research aims and methodology of this work will be provided.

CHAPTER 3:

RF MEMS CAPACITIVE SWITCH RELIABILITY – THEORY AND RESEARCH STATUS

3.1 INTRODUCTION

The unknown reliability of RF MEMS capacitive switches during hold-down operation has been identified as one area of concern which is preventing the widespread adoption and commercialisation of this technology. Despite the demonstrated high cycling lifetime of commercial switches, hold-down lifetimes of up to 10 years have still not been achieved owing to a lack of understanding of the physical processes responsible for the intrinsic failure mechanisms of a switch. Therefore, the degradation mechanisms of capacitive switches during hold-down operation need to be investigated in order to develop a deeper understanding of the physics of failure and to create novel solutions for the improvement of device reliability.

The objective of this chapter is to describe the current research status and understanding of degradation mechanisms in RF MEMS capacitive switches during hold-down operation and is organised as follows. Section 3.2 describes the intrinsic failure mechanisms of RF MEMS capacitive switches which are determined by changes in the pull-in and pull-out voltages of a switch over time. Following this, several models which were created to explain these parametric shifts are described. While these models allowed significant progress to be made in the measurement and characterisation of RF MEMS capacitive switch reliability, very little progress has been made in the identification of the underlying physical processes responsible for material degradation in capacitive switches. A discussion of this is provided in Section 3.3 where more recent methods of isolating different degradation mechanisms are described. Finally the research aims of this work are described in Section 3.4 before the chapter is summarised in Section 3.5.

3.2. CAPACITIVE SWITCH FAILURE DURING HOLD-DOWN OPERATION

Section 2.4 of the previous chapter briefly introduced the subject of RF MEMS reliability and stated that mechanical degradation and dielectric charging cause time-dependent changes in the pull-in and pull-out voltages of a capacitive switch. Over an extended period of time, these changes can cause switch failure in one of two ways; stiction or screening. Stiction occurs when the pull-out voltage crosses over the 0 V axis such that the membrane remains fixed in the down-state even when no bias is applied to a switch, as shown in Figure 3.1. The additional failure mode known as screening occurs when a change in the pull-in voltage causes the switch parameters to lie outside a specified maximum range. An example of this is also shown in Figure 3.1 where the positive pull-in voltage has increased beyond +15 V while a switch may not be designed to operate beyond this limit.

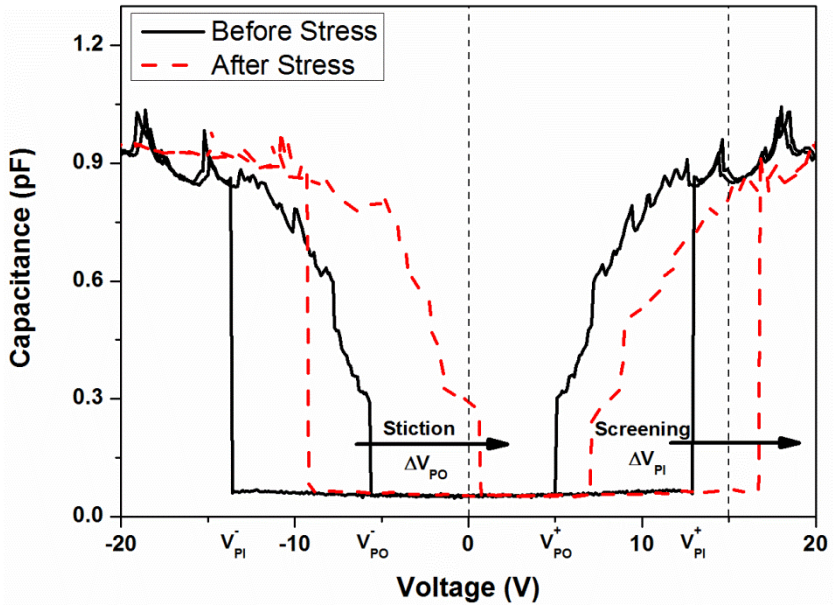

Figure 3.1: Measured shift in the C-V curve of a Tyndall capacitive switch leading to failure due to stiction and screening.

While Figure 3.1 shows the initial and final states of a switch C-V curve after a hold-down experiment, transient changes in the device C-V curve can also be used to monitor degradation of the switch parameters. An example of a transient ΔV_{PI} graph is shown in Figure 3.2. To obtain this data, a hold-down stress was applied to a device for a set period of time before a C-V sweep was performed to measure the pull-in voltage. The hold-down stress was then resumed for another set period of time and the stress/measurement process continued. A transient ΔV graph is formed when the accumulated change in the pull-in or pull-out voltage is plotted against the time of the experiment and graphs such as these are used extensively throughout this thesis.

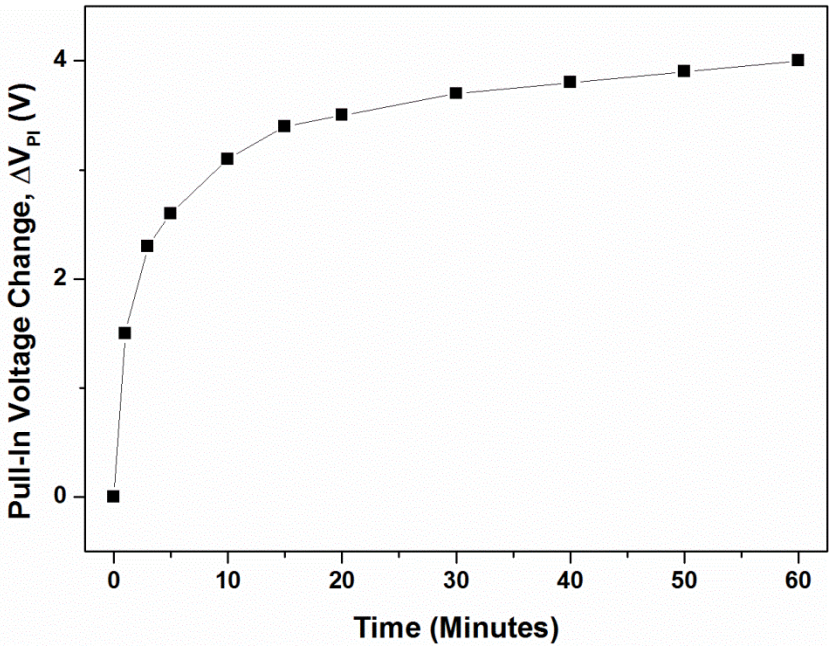

Figure 3.2: Transient change in the pull-in voltage of a capacitive switch in response to a hold-down stress over one hour. The actuation voltage was interrupted to perform C-V sweeps after 1, 3, 5, 10, 15, 20, 30, 40, 50 and 60 minutes.

Researchers have studied transient changes of the switch pull-in and pull-out voltages in order to monitor the degradation mechanisms of a switch and have observed that the transient behaviour can broadly follow either a C-V shift effect where all the parameters shift in one direction or a C-V narrowing effect where all the parameters reduce in magnitude [42, 68, 76, 100, 109-112]. Analytical models have been developed in the literature to explain the causes of C-V shift and narrowing [113, 114] and the derivation and application of these models is described in the following sections.

3.2.1 C-V Shift Effect due to Uniform Dielectric Charge

The C-V curve of an ideal capacitive switch which is symmetric about the 0 V axis was shown in Figure 2.18. This C-V curve is representative of a switch with no charge in the dielectric whose pull-in and pull-out voltages are only governed by the restoring force of the supporting tethers and the electrostatic force generated as a result of the applied bias. However, in reality, parasitic charge can exist within the dielectric layer which changes the electrostatic force between the membrane and the dielectric [74]. The presence of an additional electrostatic force causes all four threshold voltages of a device to change in what is known as the C-V shift effect. In a capacitive switch, the C-V shift effect can be recognised as the simultaneous movement of all four threshold voltages along the voltage axis in either the positive or the negative direction such that the C-V curve is no longer

symmetrical about 0 V. The direction of shift depends on the biasing scheme and the net polarity of charge within the dielectric, and for a uniform charge distribution the shift magnitude is necessarily equal for all four threshold voltages. A representation of this is shown in Figure 3.3.

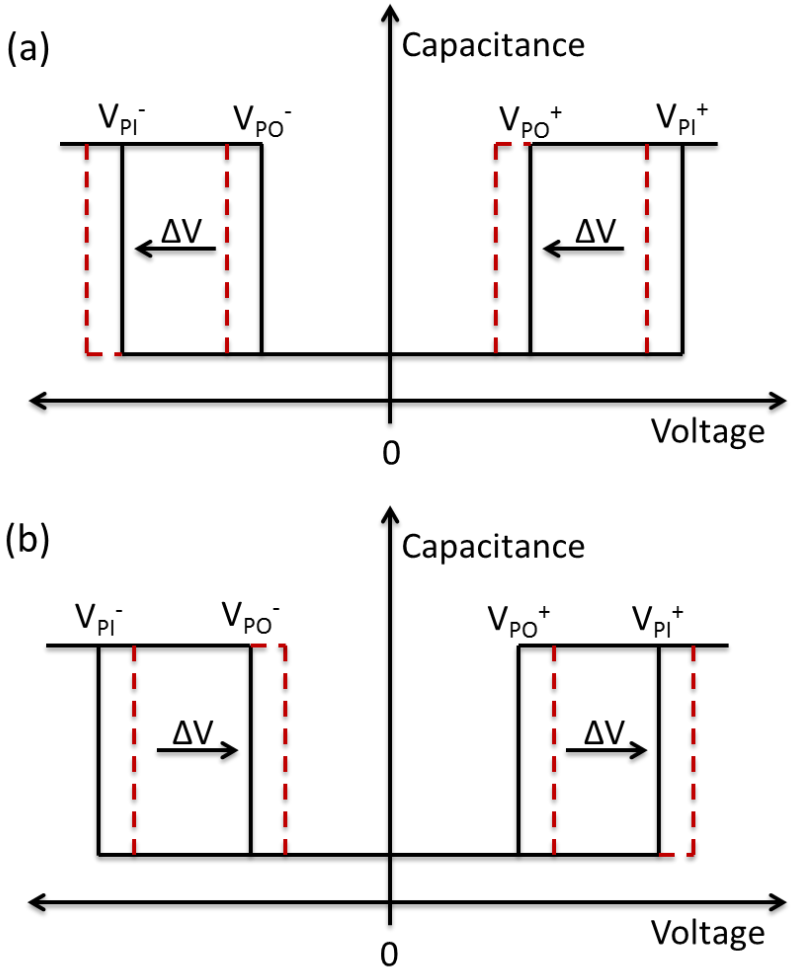

Figure 3.3: The C-V curves of an ideal capacitive switch showing a left-shift (a) and a right-shift (b) due to dielectric charging.

Parasitic charge can be created in the dielectric during processing [115] or may be added to the dielectric during switch operation [43, 47, 74, 88, 104, 109-111, 116-120]. The influence of this charge on the device threshold voltages can be understood by considering the simple case of uniform dielectric charging pictured in Figure 3.4 [113].

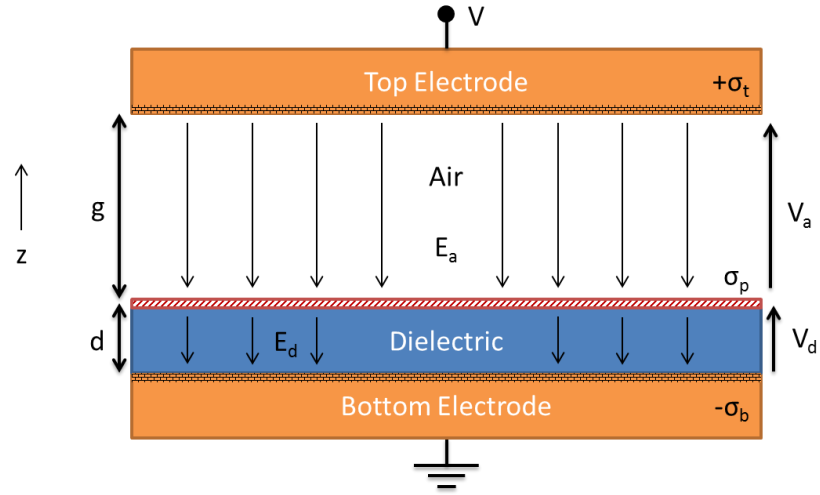

Figure 3.4: Schematic representation of a MEMS capacitive switch with a uniform distribution of parasitic charge at the top surface of the dielectric.

In Figure 3.4 a parasitic charge density σ_p is located at the top surface of a dielectric of thickness d and the charge densities on the top $+\sigma_t$ and bottom $-\sigma_b$ electrodes are arranged so that the capacitor is electrically neutral

$$\sigma_t + \sigma_b + \sigma_p = 0\,. \tag{3.1}$$

The charge densities at the top and bottom metal are supplied by the voltage source V. As a result of these charge densities, the electric fields in the air-gap and dielectric are

$$E_a = \frac{\sigma_t}{\varepsilon_0}, \tag{3.2}$$

$$E_d = \frac{-\sigma_b}{\varepsilon_0\varepsilon_r} = \frac{\sigma_t + \sigma_p}{\varepsilon_0\varepsilon_r}\,. \tag{3.3}$$

The voltage applied to the capacitor is divided between the air-gap and dielectric such that

$$V = E_a g + E_d d\,. \tag{3.4}$$

By substituting (3.2) and (3.3) into equation (3.4) an expression for the charge density on the top electrode as a function of the applied voltage and parasitic charge density can be obtained

$$\sigma_t = \frac{V - \frac{\sigma_p d}{\varepsilon_0\varepsilon_r}}{\frac{g}{\varepsilon_0} + \frac{d}{\varepsilon_0\varepsilon_r}}\,. \tag{3.5}$$

An equation for the electrostatic force experienced by the membrane of a capacitive switch as a result of an applied voltage was given in Chapter 2 as

$$F_{e.s.} = -\frac{1}{2}\frac{\varepsilon_0 A V^2}{\left(g + \frac{d}{\varepsilon_r}\right)^2}. \tag{3.6}$$

Re-arranging this equation reveals that

$$F_{e.s.} = -\frac{A}{2\varepsilon_0}\left(\frac{\varepsilon_0}{g + \frac{d}{\varepsilon_r}}\right)^2 V^2, \tag{3.7}$$

where the expression in brackets can be recognised from Chapter 2 as the total capacitance per unit area of the device, arising from a series combination of the air and dielectric capacitances. Since the charge on a capacitor is given by $Q = CV$ and the charge on the top plate is the induced charge σ_t, expression (3.7) may be re-written in a more compact form as

$$F_{e.s.} = -\frac{A}{2\varepsilon_0}\sigma_t^2. \tag{3.8}$$

By replacing σ_t with (3.5), an expression for the electrostatic force acting on the top electrode as a function of the applied voltage and parasitic charge in the dielectric can be obtained

$$F_{e.s.} = -\frac{A}{2\varepsilon_0}\frac{\left(V - \frac{\sigma_p d}{\varepsilon_0 \varepsilon_r}\right)^2}{\left(\frac{g}{\varepsilon_0} + \frac{d}{\varepsilon_0 \varepsilon_r}\right)^2}. \tag{3.9}$$

Thus the electrostatic force acting on the membrane has been modified by the influence of a parasitic potential

$$V_p = -\frac{\sigma_p d}{\varepsilon_0 \varepsilon_r}. \tag{3.10}$$

It is important to note that the electrostatic force in (3.9) is proportional to the difference between the applied voltage and the parasitic potential and that both the voltage and potential can have a positive or negative polarity. Therefore, depending on their respective polarities the electrostatic force responsible for switch operation can be either enhanced or reduced. This is shown in Figure 3.5 where the electrostatic force is calculated using (3.9) for three different cases of parasitic charging; an ideal switch with no dielectric charge, and

equal but opposite parasitic charge densities of +10 x 10^{-4} and -10 x 10^{-4} C/m^2. The calculation was performed for a switch with physical parameters A = 100x100 µm^2, d = 130 nm, ε_0 = 8.85x10^{-12} F/m, ε_r = 3.9 and g_0 = 3 µm.

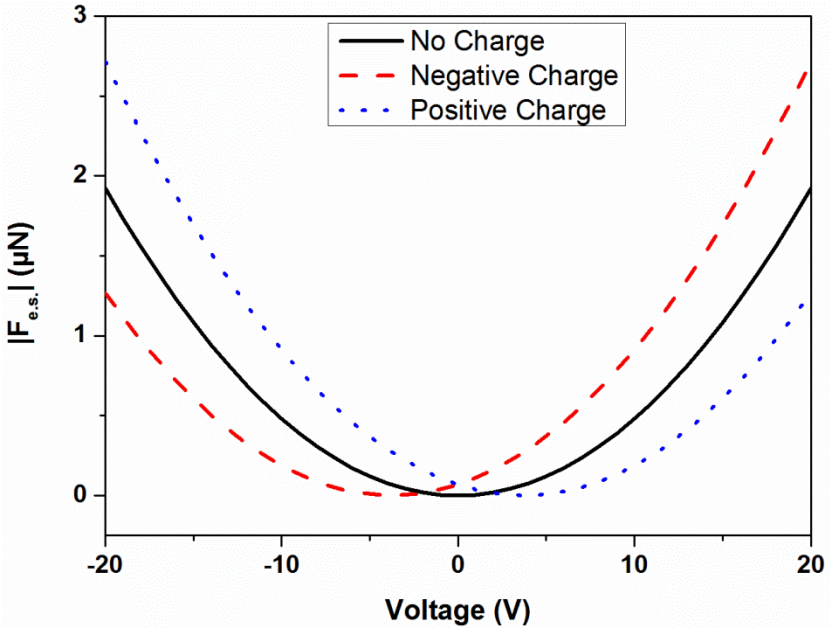

Figure 3.5: The electrostatic force exerted on the top membrane of a capacitive switch as a function of the applied voltage for a fixed air-gap of 3 µm and three different parasitic charge densities of zero (solid black line), -10 x 10^{-4} C/m^2 (dashed red line) and +10 x 10^{-4} C/m^2 (dotted blue line).

It is seen that for a bias applied to the top metal, force enhancement occurs if the bias is of the opposite polarity to the parasitic charge, while force reduction occurs if the bias is of the same polarity as the parasitic charge. The enhancement or reduction of the electrostatic force has the effect of shifting the entire C-V curve along the voltage axis, which can be seen if the force-balance procedure of Chapter 2 is repeated to obtain expressions for the modified pull-in and pull-out voltages of a charged capacitive switch;

$$V_{PI} = \pm\sqrt{\frac{8k}{27\varepsilon_0 A}\left(g_0 + \frac{d}{\varepsilon_r}\right)^3} + \frac{\sigma_p d}{\varepsilon_0 \varepsilon_r}, \tag{3.11}$$

$$V_{PO} = \pm\sqrt{\frac{2k}{\varepsilon_0 A} g_0 \left(\frac{d}{\varepsilon_r}\right)^2} + \frac{\sigma_p d}{\varepsilon_0 \varepsilon_r}. \tag{3.12}$$

Thus, under the influence of uniform dielectric charge the expressions for the pull-in and pull-out voltage have been modified by a term which is dependent on the density of trapped charge and the position of this charge sheet within the dielectric. The resulting C-V shift is equal for both the pull-in and pull-out voltages and is greatest when the charge is

located at the top surface of the dielectric. Additionally, the direction of C-V shift is dependent on the polarity of the trapped charge and the applied bias but also on the biasing scheme. For example, the model derived in this section assumed that the bottom metal was grounded with the high potential (positive or negative bias) applied to the top metal in which case positive charge will cause a right-shift of the C-V curve while negative charge will result in a left-shift. However, if the top metal is grounded and the high potential (bias) is applied to the bottom electrode then the direction of C-V shift will be reversed and this will be shown experimentally in Chapter 4.

Wibbeler was the first to propose an analytical model of uniform dielectric charging to interpret his results obtained on gold-coated silicon cantilevers [113]. The 10-20 μm thick cantilevers were fabricated over dielectric layers composed of PECVD SiO_2 or SiN-SiO_2-SiN stacks, and the up-state deflection of the cantilevers was monitored while voltages of up-to 500 V were applied to the bottom electrode. The deflection of the test structures was monitored using a laser sensor as the applied bias was swept from positive to negative values and vice versa. Symmetric deflection vs. voltage curves were measured on cantilevers which were fabricated without dielectric layers, while a negative offset was measured on dielectric-based cantilevers. The negative offset was used to calculate the density of positive parasitic charge using a uniform charging model under the assumption that the charge was located at the dielectric surface. Additionally, increased offsets in the positive and negative direction were measured after high-voltage stress, which indicated that negative and positive parasitic charge densities had been created in the dielectric after positive and negative voltage sweeps, respectively. In each case, the polarity and magnitude of the parasitic charge was determined using a uniform charging model where the charges were assumed to be located at the surface of the dielectric. Wibbeler proposed that air-breakdown was the cause of dielectric charging in his devices, but never confirmed this through measurement. Moreover, while air-breakdown leading to uniform surface charging may indeed have occurred during the high voltage stressing, the cantilever beams never made contact with the intermetal dielectric layer so that the same charging explanation may not be applicable to other devices.

Reid simulated a capacitive switch under various states of uniform dielectric charging to model the C-V shifts measured on fixed-fixed beam RF MEMS capacitive switches with a 200 nm thick SiN dielectric layer [121]. To verify the simulation results, the charge state of real switches was characterised using a fast RF measurement method to record the full C-V

curve. A left-shift was observed in all four threshold voltages which was attributed to a fixed negative parasitic charge density assumed to be located in the centre of the dielectric. Following this, the physical parameters and parasitic charge density of the simulated switch were adjusted until approximate agreement was obtained between the measured and simulated C-V curves. The uniform charging model predicted that each threshold voltage would shift by the same amount; however, this was not the case in the real capacitive switches where unequal C-V shifts were measured. Therefore, while the uniform charging model could approximate the charge state of the dielectric, it could not fully reproduce the measured C-V curves.

Van Spengen studied dielectric charging in fixed-fixed beam capacitive switches fabricated with 200 nm thick SiN dielectric layers [122]. Full C-V curves were measured while the switches were stressed using 30 V unipolar square wave biases of different frequencies. Approximately symmetric right-shifts were observed in the C-V curves of capacitive switches which were attributed to a uniform distribution of negative parasitic charge in the dielectric. However, equal right-shifts of all four threshold voltages were predicted by the uniform charging model which disagreed with the measurement results. The differences between the modelled and measured results were attributed to errors in the model assumptions, such as the membrane not behaving as a perfectly rigid plate.

Yuan also studied dielectric charging in RF MEMS capacitive switches composed of gold fixed-fixed beams with a 220 nm thick PECVD SiON dielectric layer [109]. The switches were characterised by two methods: applying repeated voltage sweeps to the bottom electrode to measure positive and negative pull-in voltage shifts, and by using RF measurements to measure full C-V curves. Positive and negative C-V shifts could be alternately created by stressing devices with positive and negative voltages, and these were interpreted as the effects of negative and positive dielectric charge based on Wibbeler's uniform charging model. The same direction of C-V shift was observed when RF methods were used to measure full C-V curves; however, the measured shift was not equal for all four threshold voltages which could not be explained using the uniform charging model. Instead, Yuan interpreted this behaviour as evidence of the rapid migration of charge within the dielectric layer during a C-V measurement. He hypothesised that the effect of this mobile charge would become more prominent as it neared the dielectric surface and become less prominent as it moved towards the bottom electrode. However, no physical mechanism of charge migration was proposed.

In later work, Yuan used metal-insulator-metal (MIM) structures to characterise charging in the dielectric layers of RF MEMS capacitive switches at various electric fields and temperatures [88, 116, 118]. The MIM capacitors were fabricated using Au/Ti electrodes and a 300 nm thick SiO_2 dielectric. Transient charging and discharging currents were measured while voltages of up to 40 V were applied to the MIM devices. The transient currents were fitted with exponential models to calculate the density of injected charge during measurements. The calculated value was input to a uniform charging model to predict the corresponding ΔV_{PI} shift of MEMS switches. To confirm these model predictions, only the negative pull-in voltage shift of RF MEMS capacitive switches was measured under different field and temperature conditions. A right-shift of the negative pull-in voltage was measured after each stress, which was believed to be caused by negative charge injection from the bottom electrode. Agreement could be obtained between the measured and modelled pull-in voltage changes when the depth of charge within the dielectric was varied. However, the depth of charge was found to be different in each case with no physical explanation provided. Additionally, because only one pull-in voltage change was measured, it was impossible to know if the switches were solely affected by uniform dielectric charging or if some other mechanism also influenced the device behaviour.

Yuan's use of a single ΔV_{PI} to characterise dielectric charging stemmed from the fact that unequal C-V shifts were observed when full C-V curves were measured which could not be explained using a uniform charging model [109]. Similar behaviour was also observed by other researchers who believed that additional charge was being added to the switch during C-V measurements when the moveable membrane made contact with the dielectric layer [112, 123]. To overcome this problem, an alternative non-contact capacitance-voltage measurement technique was proposed which could measure the offset of the C-V curve without causing contact between the top metal and dielectric.

This technique was originally pioneered by Herfst [124] following non-contact measurements of parasitic charge performed by Reid [123]. Herfst investigated the effects of three different C-V measurement techniques on fixed-fixed beam RF MEMS capacitive switches fabricated using 400 nm thick SiN dielectrics. Two of the techniques were based on traditional methods of actuating a device to record the pull-in voltage, while for the non-contact technique a swept voltage was applied to a device such that the bias magnitude always remained below the pull-in point. In the up-state, the attractive electrostatic force acting on the switch membrane varies with the square of the applied voltage as shown in

Figure 3.5. Therefore, a parabolic capacitance versus voltage curve is obtained and in the absence of dielectric charge the minimum of this curve should lie at 0 V. When charge exists in the dielectric, the voltage at which the capacitance is minimised ($V_{C\min}$) is offset from the 0 V position and the direction and magnitude of this offset reflects the polarity and density of parasitic charge within the dielectric. An example of this is shown in Figure 3.6.

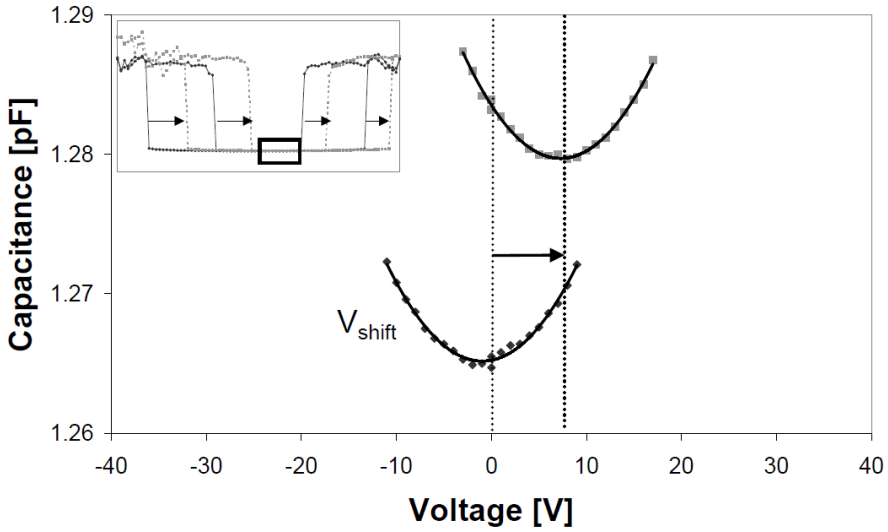

Figure 3.6: A right-shift in the V_{Cmin} of a capacitive switch following DC stress at 65 V for 727 seconds. Inset: the corresponding full C-V curve, from [124].

Herfst performed repeated C-V measurements using all three techniques to monitor the charging effects of each. An increasing C-V shift was observed following repeated measurements using each technique; however, the measured shift was significantly lower when the non-contact $V_{C\min}$ method was used. This result showed that the $V_{C\min}$ method could be used to characterise the C-V shift of a capacitive switch without fully actuating the membrane, thereby minimising the risk of dielectric charging during the measurement procedure.

Koutsoureli used the $V_{C\min}$ method to monitor the discharging of RF MEMS capacitive switches following electrical stresses over different durations and electric field levels [80, 125, 126]. The devices under investigation were bridge-type capacitive switches composed of Ti-Au membranes with 250 nm thick SiN intermetal dielectric layers. Prior to measurement, the switches were initially charged in the down-state by applying positive DC biases in the range of 20-40 V to the bottom electrode. After 5-15 minutes of electrical stress, the bias was removed and the discharging of the device was monitored by

measuring the up-state bias for capacitance minimum for periods of up-to 14000 seconds. The transient $V_{C\min}$ data was fitted with a stretched exponential equation and the time derivative of this equation was used to calculate the discharging current of the devices. The injected charge was approximated by a uniform sheet of positive charge at the top surface of the dielectric, and the discharging process was believed to be governed by charge hopping and percolation processes which occurred under low intrinsic electric field levels. This assumption was deemed appropriate by the use of amorphous and disordered PECVD dielectric films, where these processes are expected to dominate the discharging behaviour. However, no physical evidence of these discharging mechanisms was provided.

Based on the experimental results presented in this section, it can be seen how the uniform charging model allowed the effects of dielectric charging and discharging to be characterised on different device architectures using a variety of experimental techniques. However, very little agreement was obtained amongst the literature where a multitude of different charging mechanisms (air-breakdown, charge injection, hopping) were proposed to explain the observed C-V shift effect. Additionally, while the uniform charging model was able to approximate the C-V shift behaviour observed on RF MEMS capacitive switches, asymmetric C-V shifts were often observed which could not be explained using such simple analysis. The observation of unequal C-V shifts was attributed by researchers to the creation of additional charge during C-V measurements which interfered with experimental results. Therefore, the $V_{C\min}$ technique was developed which allowed the C-V shift effect to be measured without contact between the moveable membrane and dielectric. However, in effect, this new technique simply avoided the problem of measuring asymmetric C-V curves which could not be explained by uniform dielectric charging.

The uniform dielectric charging model was derived for an ideal device under the assumption that all electric fields and distributions of charge in the dielectric were uniform. However, in real devices the charge may be distributed throughout the dielectric layer due to non-uniform charging during down-state operation. Non-uniform charging is an unavoidable consequence of the presence of holes in the top metal membrane. A SEM image of the top metal of a capacitive switch is shown in Figure 3.7 (a). The holes in the membrane are primarily added to MEMS devices to aid in the removal of sacrificial layers during the final processing steps of switch fabrication, but may also be used to relieve residual stress in the membrane and increase the switching speed of devices [11]. The varying electric field present in the vicinity of these holes can cause distributed dielectric

charging, even for an ideal device with 100% contact between the membrane and dielectric.

Non-uniform dielectric charging will also occur in RF MEMS capacitive switches as a result of the intermittent contact between the membrane and dielectric. To illustrate this, a SEM image of the top surface of the dielectric of a Tyndall capacitive switch is shown in Figure 3.7 (b). The dielectric roughness may be caused by several fabrication steps, such as the deposition of the oxide [127] or the plasma ashing of the polyimide during the final release etch of capacitive switches [128]. The rough contact between the membrane and dielectric creates charging 'hot spots' on the top surface of the dielectric where various peaks are in contact with the metal while adjacent troughs are not [47, 120, 129]. Localised increases in the electric field may facilitate dielectric charging at these points [42].

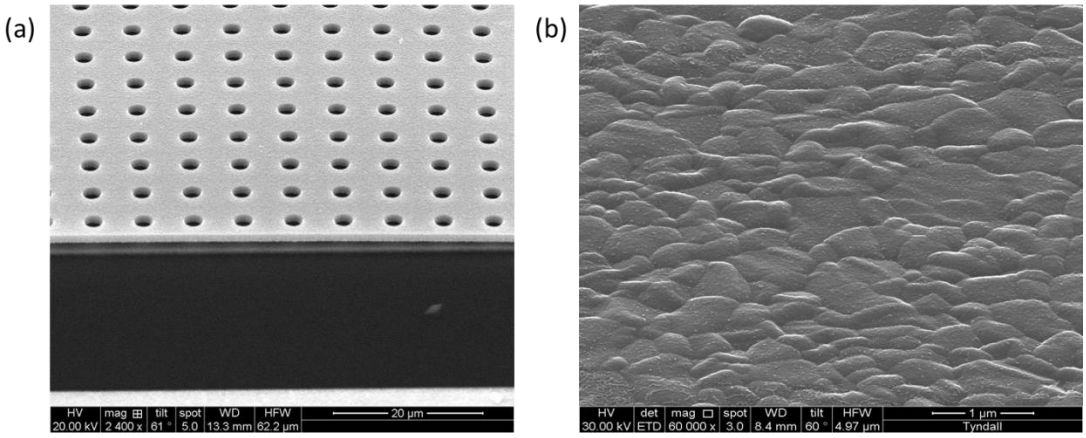

Figure 3.7: SEM image of the array of holes present in the top metal of a capacitive switch fabricated at Tyndall National Institute (a). An SEM image of the rough dielectric surface of such a device is shown in (b).

Therefore, it can be understood how non-uniform distributions of dielectric charge are created in capacitive switches during down-state stress. The differences between the real charge-state of a dielectric and the overly-simplified assumptions of the uniform charging model may explain why a uniform distribution of charge could not account for the unequal and asymmetric C-V shifts observed in capacitive switches. An alternative analytical model of non-uniform dielectric charging was proposed to explain these effects, and the derivation of this model is described in the following section.

3.2.2 C-V Narrowing Effect due to Non-Uniform Dielectric Charge

Another C-V curve instability which has been experimentally observed but which cannot be explained by a uniform charging model is the C-V narrowing effect. C-V narrowing in a capacitive switch can be recognised as a decrease of all four threshold voltages over time and a simplified representation of this is shown in Figure 3.8.

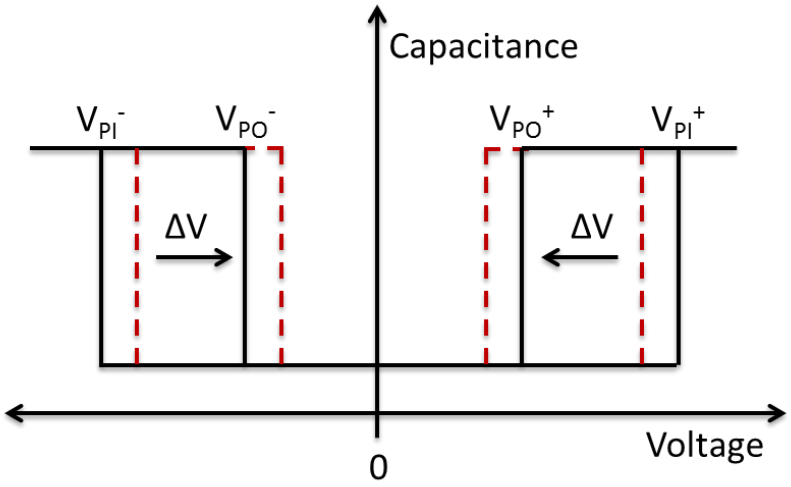

Figure 3.8: The narrowing effect in the C-V curve of an ideal switch.

Reid first reported narrowing on fixed-fixed beam capacitive switches fabricated using 200 nm SiN dielectrics [112]. In his experiments various triangular waveforms were applied to the top metal of a switch while the evolution of the pull-in and pull-out voltages was monitored using an RF technique. Shifts in the C-V curve were measured when a positive or negative DC offset was overlaid with the RF signal. The direction of shift corresponded with the bias polarity of the DC offset and could be explained using a uniform charging model. However, only narrowing was observed when a bipolar signal with no voltage offset was applied to the switch. Reid proposed that the narrowing effect was caused by an increase in the magnitude of charge in the dielectric over time while the polarity of the transferred charge was inverted with each voltage cycle.

Two years later, Rottenberg derived an analytical model which could explain both the shift and narrowing of the C-V curve as a result of dielectric charging [114]. To explain the narrowing phenomenon, he proposed that more than one polarity of charge may be present in the dielectric at the same time and that these charges were distributed non-uniformly throughout the dielectric volume. The simplest case of non-uniform charging can

be represented by two charge densities of opposite polarity located at the top surface of a dielectric and a schematic of this situation is shown in Figure 3.9.

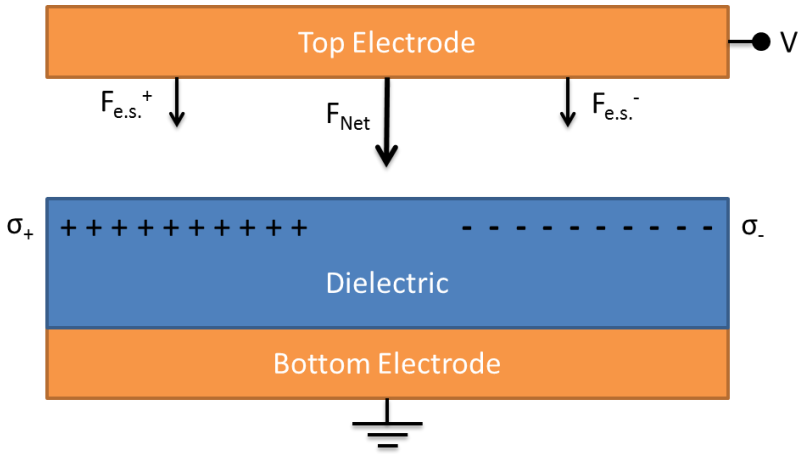

Figure 3.9: A non-uniform distribution of charge at the top surface of a dielectric. The charges have equal density but opposite polarity and their net effect results in an attractive electrostatic force F_{Net} without any voltage offset.

In Figure 3.9 two different polarities of charge are present at the top surface of the dielectric. The positive and negative charge densities generate an attractive electrostatic force $F_{e.s.}^{+} \propto \left(V - V_p\right)^2$ and $F_{e.s.}^{-} \propto \left(V + V_p\right)^2$ respectively between the membrane and the dielectric in a similar fashion to uniform dielectric charging derived in the previous section. However, the net effect of the two distributions of dielectric charge is an electrostatic force $F_{Net} \propto V^2 + V_p^2$, where V_p is defined in (3.10). Due to the presence of the squared terms, this will result in an enhancement of the net electrostatic force regardless of the polarity of the parasitic charge or the applied bias. This is shown in Figure 3.10 where the electrostatic force acting on the top membrane is plotted for two different cases of parasitic charging; an ideal switch with no charge in the dielectric and for two charge distributions of equal magnitude and opposite polarity as shown in Figure 3.9. The calculations were made using (3.9) for the same switch parameters given in the previous section.

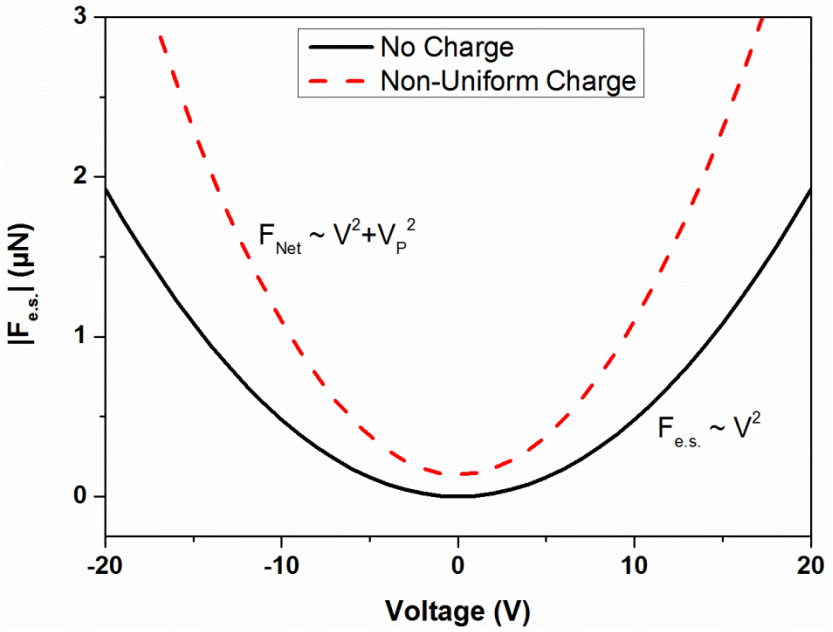

Figure 3.10: The enhancement of the net electrostatic force acting on the moveable membrane of a capacitive switch as a result of a non-uniform distribution of dielectric charge.

It is important to note that even though the net dielectric charge is zero, the net electrostatic force is not zero even when no bias is applied to the switch. This causes all four threshold voltages of a switch to decrease in magnitude without any recorded C-V shift, as shown schematically in Figure 3.8.

An analytical model of the effects of non-uniform charging can be obtained by repeating the force-balance procedure used to derive equations (3.11) and (3.12). Following Rottenberg [117], a more general situation is considered where an unknown distribution of charge is present in the dielectric which can be represented by a volume charge density $\rho(x,y,z)$. The charge distribution creates a built-in voltage offset $V(x,y,z)$ between the switch electrodes. In the presence of an additional voltage offset, the equation for the electrostatic force $F_{e.s.}$ between the electrodes is given by [114]

$$F_{e.s.} = -\frac{\varepsilon_0}{2}\int_A \frac{\left(V - V(x,y,z)\right)^2}{\left(d/\varepsilon_r + g\right)^2}\,dA, \tag{3.13}$$

where V is the bias applied to the device, d is the dielectric thickness, g is the size of the air-gap, and ε_0 and ε_r are the permittivities of the air and dielectric, respectively.

By replacing the unknown voltage offset by an equivalent mean and standard deviation $V(x,y,z)=\overline{V}+\delta_V$, the expression in equation (3.13) can be expanded and simplified to obtain [100]

$$F_{e.s.}=-\frac{\varepsilon_0 A}{2}\frac{\left(V-\overline{V}\right)^2+\delta_V^2}{\left(d/\varepsilon_r+g\right)^2}. \tag{3.14}$$

The expressions for the pull-in and pull-out voltages can now be found by following the force balance procedure described in Chapter 2. The modified pull-in and pull-out voltages under the influence of distributed dielectric charge are given by

$$V_{PI}=\overline{V}\pm\sqrt{\frac{8k}{27\varepsilon_0 A}\left(g_0+\frac{d}{\varepsilon_r}\right)^3-\delta_V^2}\,, \tag{3.15}$$

$$V_{PO}=\overline{V}\pm\sqrt{\frac{2k}{\varepsilon_0 A}g_0\left(\frac{d}{\varepsilon_r}\right)^2-\delta_V^2}\,. \tag{3.16}$$

These equations show that the mean dielectric charge $\overline{V}$ has the effect of shifting the C-V characteristic to the left or right in an equivalent manner to uniform dielectric charging derived in the previous section. In the absence of any dielectric charge, equations (3.15) and (3.16) return to the expressions for the pull-in and pull-out voltages of RF MEMS capacitive switches derived in Chapter 2.

Due to its position under the square root sign, it can be seen that the variance of the charge distribution δ_V^2 is responsible for narrowing of the C-V characteristic as any increase of this value will cause a decrease in the V_{PI} and V_{PO}. Moreover, equations (3.15) and (3.16) show that an equal amount of charge variance will cause a larger decrease in the V_{PO} than the V_{PI}. To demonstrate this, the pull-in and pull-out voltage changes of a capacitive switch were calculated under various amounts of charge variance and zero mean charge and the results are shown in Figure 3.11. It can be seen that the pull-out voltage is significantly more sensitive to non-uniform charging than the pull-in voltage. The initial values were calculated for an ideal switch with A = 100x100 μm^2, d = 130 nm, ε_0 = 8.85x10^{-12} F/m, ε_r = 3.9, g_0 = 3 μm and k = 5 N/m.

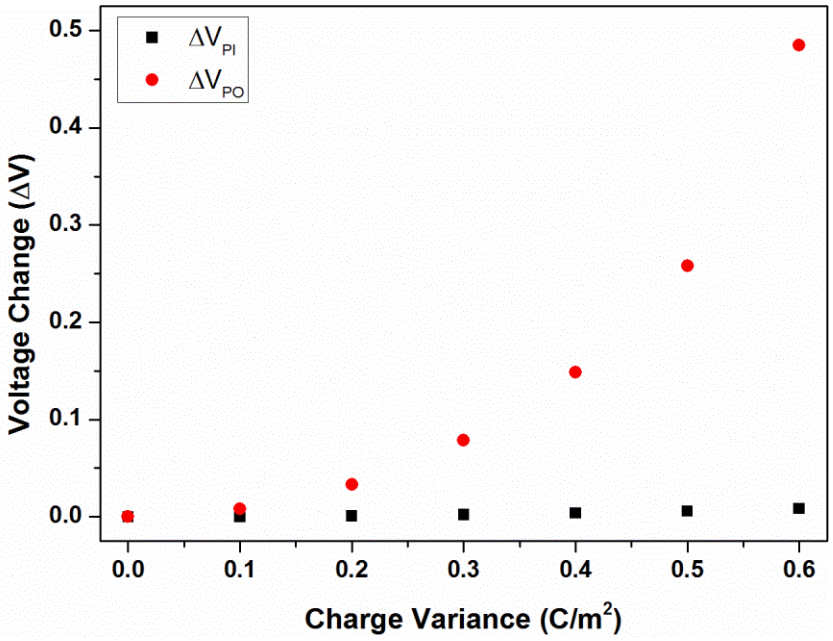

Figure 3.11: Calculated changes in the pull-in and pull-out voltages of a capacitive switch under increasing levels of charge variance. The pull-out voltage is significantly more sensitive to non-uniform charging than the pull-in voltage.

Czarnecki measured narrowing in the C-V curves of fixed-fixed beam capacitive switches fabricated using AlCu membranes and 200 nm thick AlN intermetal dielectric layers [130]. Positive and negative unipolar square-wave biases were applied to the bottom metal of capacitive switches while the effects of dielectric charging were monitored through periodic measurements of the full C-V curve. The effects of C-V shift and narrowing were observed after stressing at both voltage polarities, while a change in the direction of C-V shift was observed as the stress bias was increased. The change in direction of C-V shift and the simultaneous presence of C-V shift and narrowing was taken as proof that two (or more) different charging mechanisms were acting on the switch at the same time, in accordance with the model of non-uniform dielectric charging proposed by Rottenberg [117]. Czarnecki proposed that the different charging mechanisms could cancel, mitigate or enhance each other's influence on the switch, resulting in C-V shift, C-V narrowing or a combination of these effects. Furthermore, he proposed that the two different charge types were located in the substrate dielectric and intermetal dielectric, respectively. While finite element simulations were performed to verify that opposite polarity charges placed in the intermetal and substrate dielectric could result in narrowing of the C-V curve, no physical mechanisms were proposed to explain how the simultaneous substrate and intermetal dielectric charging occurred.

Herfst also measured narrowing in the C-V curve of RF MEMS capacitive switches fabricated using AlCu membranes and 425 nm thick SiN dielectric layers [110]. A device was stressed using +45 V applied to the top metal while the charge state of the dielectric was monitored using 2 methods; a fast RF method to measure full C-V sweeps and the non-contact $V_{C\min}$ method which, aside from preventing additional charge injection during measurements, is also not affected by narrowing of the C-V curve. C-V shifts were measured using both methods and were found to be in agreement. Following Rottenberg's model, the C-V shift effect was attributed to the net polarity of charge in the dielectric, while the narrowing effect was believed to be caused by a laterally non-uniform charge distribution.

Further to this, Herfst directly measured a laterally non-uniform charge distribution in the dielectric of a RF MEMS capacitive switch [129]. A high stress voltage was applied to a switch until a significant amount of C-V narrowing was observed. The top electrode was then removed and the surface potential of the dielectric was measured using Scanning Kelvin Probe Microscopy. A clear difference was seen between the surface potential of the dielectric which was in contact with the top metal and that which was directly underneath a hole and this was associated with an increased density of injected charge at these areas. A non-uniform distribution of dielectric charge was also measured in areas where the switch had been in contact with the dielectric, where several hot spots of large surface potential were recorded. This is shown schematically for a simplified switch cross section in Figure 3.12.

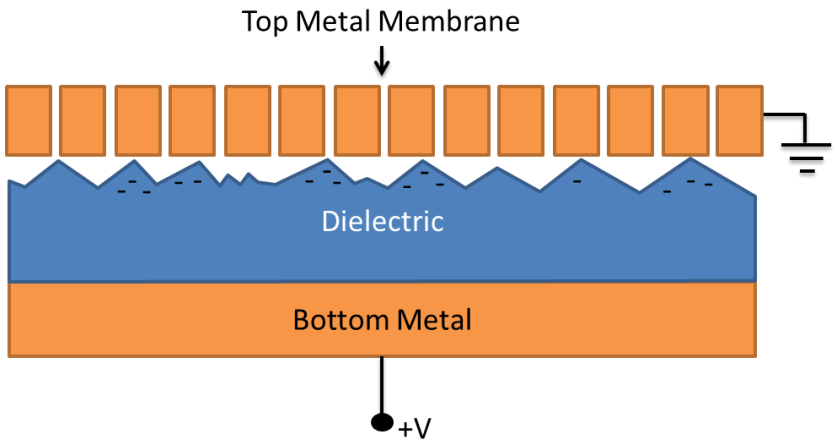

Figure 3.12: Schematic switch cross-section showing how a rough metal-dielectric interface and the presence of holes in the top metal membrane can contribute to non-uniform dielectric charging.

The theory and experimental results discussed in this section have shown how the effects of C-V shift and narrowing can be attributed to non-uniform dielectric charging. Furthermore, the results obtained by Herfst have shown that non-uniform dielectric charging is an unavoidable consequence of electrostatic actuation in a capacitive switch. Tis can be understood from the presence of a rough metal-dielectric interface and the presence of holes in the top metal membrane, as shown schematically in Figure 3.12. However, while significant progress has been made in understanding the effects of dielectric charging in RF MEMS capacitive switches and while some physical processes responsible for these degradation mechanisms have been proposed by researchers [80, 109, 113, 130], these physical processes have not been proven to be responsible for the observed degradation of the pull-in and pull-out voltages. This is because the experimental results may have been influenced by an additional degradation mechanism which was not taken into account during the measurement procedure. A discussion of the effects of this degradation mechanism is given in the following section.

3.2.3 C-V Narrowing Effect due to Mechanical Degradation

By examining equations (2.7) and (2.8) for the pull-in and pull-out voltages of a capacitive switch it can be seen that narrowing of the C-V curve can also occur if any of the parameters under the square root sign decreases in magnitude. Since the device area A and dielectric thickness d do not change over time and the permittivities of the air ε_0 and dielectric ε_r are constant, it can be seen that C-V narrowing will occur if the effective spring constant k or air-gap g_0 decrease in magnitude. Moreover, it can be seen that a change in the spring constant or air-gap will have a greater effect on the pull-in voltage than on the pull-out voltage, which is in opposition to the C-V narrowing effect of non-uniform charging. This is shown in the Figure 3.13 where changes in the pull-in and pull-out voltage have been calculated under various states of mechanical degradation. It can be seen that the pull-in voltage is significantly more sensitive to mechanical degradation than the pull-out voltage. The initial values were calculated using equations (2.7) and (2.8) for an ideal switch with the same parameters as in Section 3.2.1 and a spring constant k = 5 N/m. Degraded values have been calculated for a simultaneous decrease in the spring constant and air-gap.

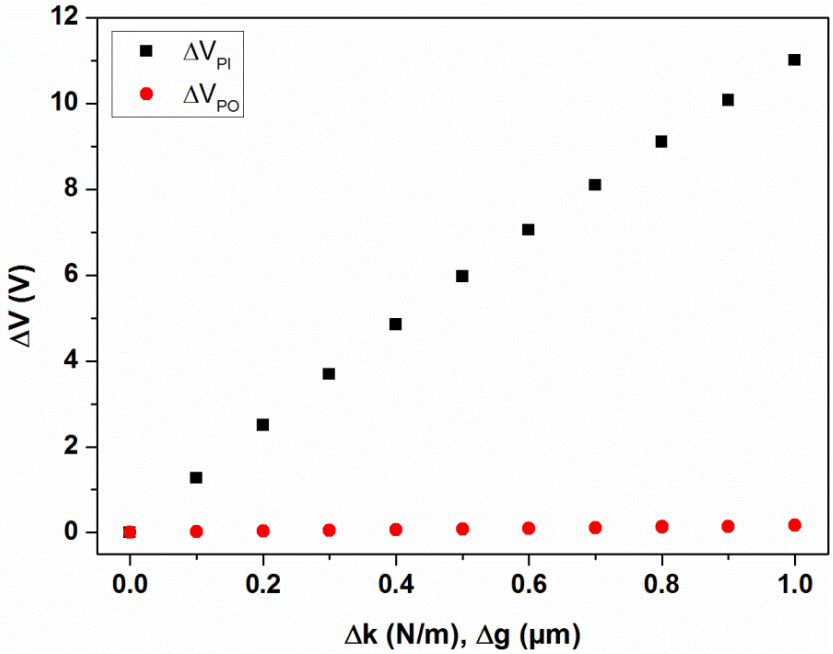

Figure 3.13: The change in the pull-in and pull-out voltages of a capacitive switch as a result of mechanical degradation. The pull-in voltage is significantly more sensitive to mechanical degradation than the pull-out voltage.

As discussed in Section 2.4, mechanical degradation was not considered as a reliability concern of RF MEMS capacitive switches due to the demonstrated high cycling lifetime of moveable membranes [63-67]. However, recent experiments have shown that mechanical degradation is a concern for RF MEMS switches [96, 100]. For example, by comparing the normalised pull-in and pull-out voltage changes of a capacitive switch, Herfst demonstrated that mechanical degradation and dielectric charging can simultaneously affect switch operation and contribute to narrowing of the C-V curve [100]. Additionally, previous work performed by Olszewski has shown that narrowing in the C-V curve of a capacitive switch was caused by mechanical degradation of the membrane material [96]. This work was performed on two types of capacitive switches which were fabricated using 1 µm thick aluminium membranes and either 140 nm PECVD SiO_2 or 14 nm native Al_2O_3 dielectrics. A low DC bias of 8 V was applied to both switches to hold them in the down-state for 3000 seconds while the positive and negative pull-in voltages were measured using periodic C-V sweeps. In both cases narrowing of the C-V curve was observed which appeared to saturate at approximately 0.7 V and this is shown in Figure 3.14. The approximately equal narrowing of each device demonstrates that this is a mechanical concern and not related to dielectric charging.

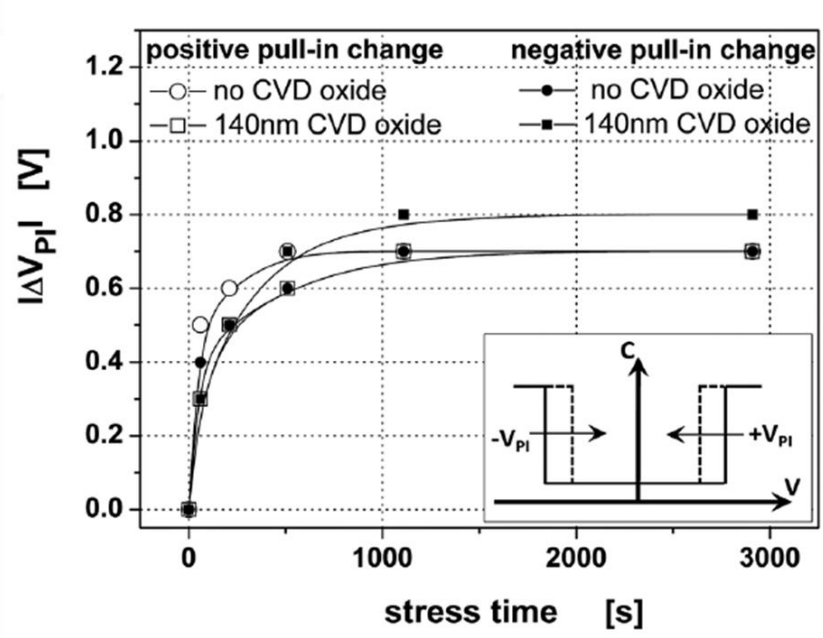

Figure 3.14: Narrowing in the C-V curve of two different RF MEMS capacitive switches; one which had a PECVD dielectric and one which did not.

Since the electric field in both switches during the stress time was estimated to be 0.6 MV/cm and 6 MV/cm while the magnitude of narrowing was approximately the same in each case, it was concluded that the C-V narrowing effect was not caused by dielectric charging. Rather, because both switch membranes had been actuated over the same distance of approximately 2 µm during the stress time it was believed that mechanical degradation of the membrane material was responsible for the narrowing effect. This same phenomenon was reported in [92] for aluminium switches which were biased below their pull-in point, which suggests that narrowing due to mechanical degradation can even affect device operation when a switch is stressed in the up-state.

Therefore, mechanical degradation of the moveable components in RF MEMS capacitive switches must be accounted for in any reliability study. However, this was not considered in the majority of publications on RF MEMS reliability where multiple degradation mechanisms may have affected the experimental results. Evidence of the simultaneous presence of multiple degradation mechanisms can be found in the widespread use of stretched exponential models to fit experimental data [26, 75, 86, 101, 111, 131-136]. A stretched exponential model is constructed from linear combinations of exponential functions which can represent a wide range of different processes acting simultaneously [137]. However, the contributions of individual processes to the overall exponential behaviour cannot be distinguished. As such, while the general field- and temperature-

acceleration of switch degradation has been well documented using stretched exponential models [79, 86, 111], no identifying characteristics of the individual physical degradation mechanisms have been observed.

The identification and characterisation of individual degradation mechanisms cannot be performed unless experimental methods and devices are employed which isolate the effects of these mechanisms when a number of different processes occur simultaneously. Recently, the focus of the research community has shifted towards the experimental isolation of mechanical degradation and dielectric charging effects in RF MEMS capacitive switches and a discussion of the research methods used to achieve this aim is given in the following section.

3.3 STATUS OF RESEARCH ON THE ISOLATION OF DEGRADATION MECHANISMS IN RF MEMS CAPACITIVE SWITCHES

3.3.1 Dielectric Charging Isolation Methods

V_{Cmin} Method

The $V_{C\min}$ method discussed in Section 3.2.1 allows the shift effect of dielectric charging in RF MEMS capacitive switches to be studied without the influence of mechanical degradation, as the offset of the C-V curve is not affected by narrowing of the pull-in characteristic [111]. However, in the event that multiple dielectric charging processes are active in a switch, the offset of the $V_{C\min}$ technique will only reveal the net effect and polarity of the dominant charge type within the dielectric, equivalent to the C-V shift effect of the mean dielectric charge $\overline{V}$ in equations (3.15) and (3.16). Therefore, the $V_{C\min}$ technique may not allow individual charge contributions to be identified. Additionally, if the value of the capacitance minimum is changed through a decrease in the spring constant or switch air-gap [109] then this will result in an incorrect estimate of the magnitude of charge trapped in the dielectric [80]. Therefore, while this measurement technique can be broadly used to characterise dielectric charging in RF MEMS capacitive switches, the calculated charge densities obtained using this method will be affected by mechanical degradation of the switch properties during hold-down stress.

Average Pull-In Voltage Method

The C-V shift effect of the mean dielectric charge can also be obtained if the average pull-in voltage change is calculated. The average pull-in voltage change can be calculated from the following expression when both the positive and negative pull-in voltages (V^+ and V^-) are measured using standard C-V sweeps

$$V_{Average} = \frac{V^+ + |V^-|}{2}. \tag{3.17}$$

An increase in $V_{Average}$ indicates that a right-shift has taken place, while a decrease in $V_{Average}$ shows that a left-shift has occurred. In [110], Hefst showed that the C-V shift results obtained using the $V_{Average}$ and $V_{C\min}$ methods were equivalent. The same technique was used by Mulloni to distinguish between the effects of C-V shift and narrowing when both effects occurred simultaneously [41]. The effect of C-V narrowing was calculated based on the difference between the pull-in voltages

$$V_{Difference} = \frac{V^+ - |V^-|}{2}, \tag{3.18}$$

where a decrease in $V_{Difference}$ signified that C-V narrowing had occurred.

The switches investigated by Mulloni were composed of 2 µm thick gold membranes and 100 nm thick low-temperature oxide intermetal dielectric layers. The devices were held in the down-state for 12 hours by a bias greater than the pull-in voltage while periodic C-V sweeps were used to record any change in the pull-in and pull-out voltages. Both shift and narrowing effects were observed in the C-V curves of capacitive switches, and these were attributed to the simultaneous effects of non-uniform dielectric charging and mechanical degradation. The C-V shift and narrowing phenomena were analysed in more detail by separating their contributions using (3.17) and (3.18); however, no physical processes responsible for these effects were proposed. This is because the $V_{Average}$ and $V_{Difference}$ calculations can be used to distinguish between the net effects of C-V shift and narrowing; however, they cannot differentiate between the contributions of mechanical degradation and non-uniform dielectric charging, or the effects of more than one dielectric charging mechanism when multiple charging mechanisms are occurring simultaneously.

Normalised Pull-In Voltage Method

The dominant effects of non-uniform dielectric charging or mechanical degradation can be identified by studying changes in the normalised pull-in and pull-out voltages [100]. Recall that non-uniform dielectric charging has a greater narrowing effect on the pull-out voltage than on the pull-in voltage, as shown in Figure 3.11. Similarly, mechanical degradation has a much greater narrowing effect on the pull-in voltage than on the pull-out voltage, as shown in Figure 3.13. Therefore, if the magnitudes of pull-in and pull-out voltage narrowing are compared, the dominant effects of mechanical degradation or non-uniform dielectric charging can be observed.

This was shown by Herfst when he compared the pull-in and pull-out voltage changes of an aluminium-alloy capacitive switch under three different electrical stress patterns: a DC bias voltage, a 1 Hz symmetric square wave and 200 Hz fast voltage pulses [100]. Full C-V curves were periodically recorded using a fast RF technique to minimise charging during the measurement procedure and C-V narrowing was observed in each case. Using the theories of non-uniform charging and mechanical degradation, Herfst showed that two distinct trends could be expected when the pull-in and pull-out voltages decreased as a result of increasing charge variance or a decreasing air-gap. This is shown in Figure 3.15, where the theoretical pull-in and pull-out voltage values are normalised to the initial pull-in voltage value at time $t = 0$.

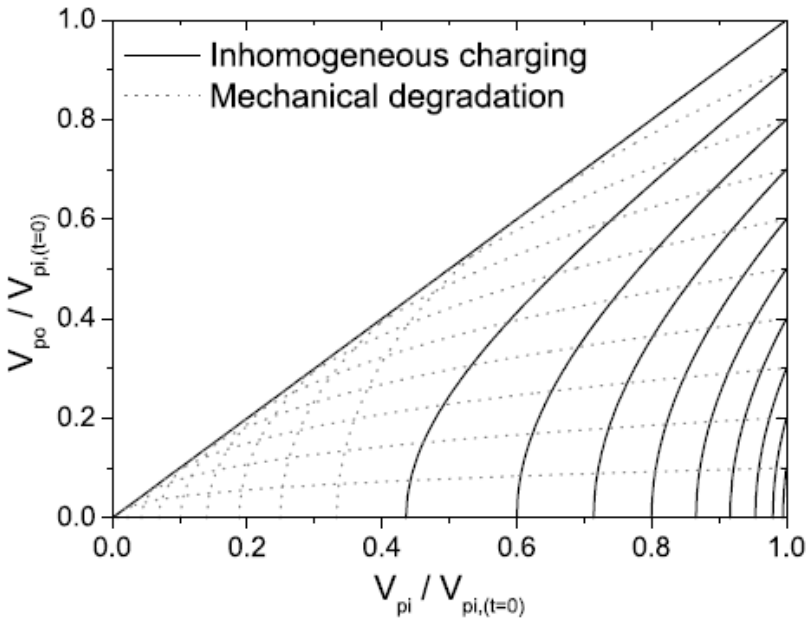

Figure 3.15: Two distinct trends are observed in the decrease of V_{PO} (normalised to V_{PI} at t = 0) as a function of the normalised V_{PI} as a switch degrades due to non-uniform charging and mechanical degradation [100].

By analysing the normalised pull-in and pull-out voltage values obtained from the three different experiments, Herfst was able to determine that both non-uniform dielectric charging and mechanical degradation simultaneously affected device operation and that the dominant mechanism was dependent on the actuation scheme employed. Plastic deformation was proposed as the physical mechanism of mechanical degradation; however, no experiments were performed to confirm this and no physical mechanisms of dielectric charging were proposed.

While the normalised pull-in and pull-out voltage changes enable researchers to conclude whether mechanical degradation or non-uniform dielectric charging is the dominant mechanism of C-V narrowing, the underlying physical mechanisms cannot be identified when more than one is occurring simultaneously. This is because both the mechanical and dielectric charging degradation processes exhibit similar time-dependencies which makes the limited experimental data sets very difficult to interpret. However, through further observation (for example by studying the recovery of mechanical degradation or dielectric charging), more information may be gained about the underlying processes and this will be shown experimentally in the following chapters.

Current Measurement Technique

The measurement of charging and discharging currents can be used to assess the dielectric charging properties of devices without the influence of mechanical degradation. Transient current measurements on MIM devices have widely been used to characterise the charging and conduction properties of thin dielectric films used in MEMS fabrication [25, 26, 108, 138-140]. In this technique a constant DC bias is applied to a device and the time-dependent charging current flowing through the circuit is recorded. Upon removal of the DC bias, the discharging current flowing in the opposite direction is also recorded. The field- and temperature-dependence of these currents have been studied by Lamhamdi [25, 26, 138, 139] and Exarchos [108, 140] to characterise the conduction and polarisation processes of MIM devices; however, no corresponding experiments were performed on MEMS capacitive switches.

Yuan [88, 116, 118] and Peng [89] have related the charging currents of MIM devices to pull-in voltage changes in MEMS capacitive switches. However, the two devices types were correlated using single polarity pull-in voltage measurements and uniform charging models, where the pull-in voltage changes were measured on aluminium-based capacitive switches that had not been proven to be mechanically robust. Similar correlations have been

performed by Papaioannou [77, 102, 141] and Koutsoureli [103, 104, 142-144] using simultaneous measurements of $V_{C\min}$ shifts in capacitive switches and transient currents in MIM devices. The $V_{C\min}$ shifts were related to different polarisation and conduction mechanisms using a uniform charging model; however, it was acknowledged that the results may have been affected by mechanical degradation which had not been taken into account during the measurement procedure [80].

MIM capacitors are very useful devices for studying the charging behaviour of MEMS switches as their structure approximates an ideal capacitive switch in the down-state. However, it is known that MIM capacitors cannot replicate the non-uniform charging behaviour of real capacitive switches due to differences in the design and fabrication of both device types [145, 146]. To avoid this problem, current measurements may also be performed on MEMS capacitive switches [147] and related to pull-in voltage or $V_{C\min}$ changes measured on the same devices. However, care must be taken to ensure the membrane material is first experimentally proven to be mechanically robust. Details of an investigation into dielectric charging in mechanically robust capacitive switches are given in Chapter 5, while a discussion of methods which can be used to characterise mechanical degradation is contained in the following section.

3.3.2 Mechanical Degradation Isolation Methods

An isolated study of the mechanical properties of thin metal films has been performed by several groups using bulge testing techniques where the deformation of a suspended membrane was assumed to approximate the displacement of a MEMS device under electrostatic actuation [97, 148]. In this method, a layer of material was fabricated in a special chamber where the pressure on one side of the material was varied while a vacuum was maintained on the other. The pressure difference on either side of the membrane caused the film to bulge outwards and allowed the mechanical properties of the material to be calculated based on the radius of curvature of the bulge. The extracted properties were used to create a mechanical model of a corresponding RF MEMS capacitive switch and demonstrated qualitatively how the restoring force changed over time as a result of mechanical degradation [97]. However, no tests were performed on real MEMS switches to confirm the simulation results.

Alternative test methods have been developed which allow the mechanical properties of actual MEMS devices to be studied. Scanning white light interferometry (SWLI) was used by

van Gils to monitor the deformation of an aluminium capacitive switch in the down-state over a period of time [73] where it was assumed that any change in the switch topography was the result of mechanical degradation only. However, charge was created in the dielectric as a result of the electrostatic actuation method and this adversely affected the measurement results. Dielectric charging during mechanical experiments can be avoided using specialized test structures without dielectric layers [105]; however, new test methods are required to enable isolated tests of mechanical degradation to be performed on RF MEMS capacitive switches which use intermetal dielectric layers.

3.4 PROBLEM STATEMENT AND RESEARCH AIMS

While significant progress has been made in the measurement, modelling and characterisation of RF MEMS capacitive switch reliability, limited progress has been made in identifying the underlying physical processes responsible for mechanical degradation and dielectric charging in these devices. It is hypothesised that early research methods were unable to identify different degradation mechanisms because the pull-in and pull-out voltage changes which were studied were simultaneously affected by both mechanical degradation and dielectric charging, while the measurement methods and models originally used to characterise these effects assumed that only one degradation mechanism was affecting the switch behaviour. While more recent analytical techniques allow the effects of C-V shift and narrowing to be distinguished from the overall changes measured in a switch C-V curve, the data can only represent the net effect of dielectric charging or mechanical degradation, with no way to isolate the underlying physical processes when more than one mechanism is occurring simultaneously. More insight has been gained into the mechanisms of dielectric charging using specialised test structures including MIM capacitors; however, correlations between these experiments and the degradation of real RF MEMS capacitive switches have also been hindered by the simultaneous presence of multiple degradation mechanisms.

In order to study the underlying physical processes responsible for mechanical degradation in RF MEMS capacitive switches, an alternative stress technique is required which can mechanically stress the membrane without causing dielectric charging. Similarly, in order to characterise the physical processes of dielectric charging, mechanically robust membranes need to be developed and experimentally verified to exhibit no mechanical degradation. Once these two goals are achieved, the observable effects of C-V shift and narrowing can

be related to the degradation of material properties and subsequently to the physical processes responsible. Therefore, the research aims of this thesis are:

1. To devise an electrical method which can mechanically stress fully processed RF MEMS capacitive switches without causing dielectric charging. This will allow the physical processes of mechanical degradation to be identified and correlated to the observed degradation of the switch parameters.
2. To develop a mechanically robust metal for use as a moveable membrane. The mechanical reliability of fully processed capacitive switches fabricated using this metal will be proven using the mechanical stress method. This new mechanically robust material will enable the physical processes of charging in intermetal dielectric layers to be identified and correlated to the observed degradation of the switch parameters.
3. To study in detail the physical processes responsible for mechanical degradation and dielectric charging in order to understand their causes and propose and validate solutions.

The development of the mechanical stress method and the results of experiments performed to characterise mechanical degradation in aluminium-based RF MEMS capacitive switches are described in Chapter 4, while Chapters 5 and 6 discuss the results of dielectric charging experiments performed on RF MEMS capacitive switches which are fabricated using a new mechanically robust aluminium alloy.

3.5 SUMMARY

This chapter provided a description of the effects of dielectric charging and mechanical degradation in RF MEMS capacitive switches. The effects of these degradation mechanisms on the C-V curve of a capacitive switch and the analytical models which were developed to describe them were derived in Section 3.2. Several state-of-the-art research methods designed to study these effects were discussed in Section 3.3, where the difficulty in performing an isolated measurement due to the simultaneous presence of more than one degradation mechanism was identified as a major roadblock to the improved understanding of reliability in RF MEMS. Based on this conclusion, the research aims of this thesis were outlined and the structured experimental approach which will be implemented to improve MEMS reliability was described. This process begins in the next chapter which

describes the development of a new electrical test method that allows mechanical degradation effects to be studied in isolation in RF MEMS capacitive switches.

CHAPTER 4:

MECHANICAL RELIABILITY

4.1 INTRODUCTION

As previously discussed, the mechanical reliability of RF MEMS capacitive switches is usually assessed via long-term cycling experiments. The ability of modern devices to survive for billions of cycles without failure is an encouraging indication of their resistance to fatigue and fracture. However, while capacitive switches are expected to undergo many switching cycles during their lifetime, another mode of operation for these devices involves long durations in the 'on' state where different mechanical degradation mechanisms may come into play. Therefore, the state-of-the-art research methodology needs to be changed so that the mechanical reliability of capacitive switches is also assessed via long-term hold-down tests. However, when DC voltages are used to mechanically stress a device, the results of such tests may be compromised by the accumulation of charge in the intermetal dielectric layer of a capacitive switch as discussed in Chapter 3. Therefore, alternative test methodologies need to be developed which allow long-term actuation of a device to be performed without causing dielectric charging. The development of this test method and the subsequent investigation of mechanical degradation in RF MEMS capacitive switches is the subject of this chapter, which is organised as follows.

Section 4.2 outlines the development of an electrical test method which allows the mechanical degradation of capacitive switches to be studied in isolation. This method is experimentally shown to minimise dielectric charging and, using this technique, it is proven that mechanical degradation is the dominant degradation mechanism of aluminium switches. Based on these results aluminium switches were selected for an in-depth investigation of mechanical degradation effects and the results of this are given in Section 4.3. The investigation leads to the identification of creep and linear viscoelastic mechanisms for the first time in RF MEMS capacitive switches. These mechanisms are found to result in permanent and reversible changes in the operational parameters of a capacitive switch. As a consequence of these findings, a mechanically-robust aluminium alloy was proposed as an alternative structural material for use in MEMS devices. Section

4.4 describes the fabrication and characterisation of new switch technology using this alloy. Finally conclusions are drawn in Section 4.5.

4.2 MEASUREMENT OF MECHANICAL DEGRADATION

In Chapter 3 it was shown how the effects of C-V shift and narrowing are caused by material degradation in RF MEMS capacitive switches. In order to characterise the mechanical and electrical degradation mechanisms and identify the physical processes responsible for these effects, it is necessary to study them in isolation. A problem arises when both mechanical degradation and non-uniform dielectric charging occur simultaneously, as C-V narrowing can be caused by either of these mechanisms and it can be very difficult to isolate the effects of both on device performance. This can be particularly problematic when electrostatic actuation is used to mechanically stress a switch, as DC bias voltages are known to cause dielectric charging in proportion to the magnitude and duration of the applied signal [93, 136, 149, 150]. For this reason it is desirable to develop an alternative means of stressing a device which can reduce or eliminate the effects of dielectric charging so that C-V measurements can be used in the study of mechanical degradation. A bipolar hold-down stress method has been developed which can be used to minimise dielectric charging in fully-functional capacitive switches [151]. This technique can be used to mechanically stress a device so that the effects of mechanical degradation may be studied in isolation [152]. A description of this bipolar hold-down method is given in the following section.

4.2.1 The Bipolar Hold-Down Stress Method

Schematic diagrams of DC and bipolar hold-down signals are shown in Figure 4.1 (a) and (b). These signals can be applied to actuate capacitive switches to the down-state from time = 0 until the end of a stress time t_{stress}. During DC stressing the moveable membrane is continuously held in the down-state using a voltage magnitude which is greater than the pull-in voltage ($V_{DC} > V_{PI}$). Continuous actuation of the membrane may also be achieved using a bipolar hold-down signal with $\pm V_{Bip} > \pm V_{PI}$ and with a transition time between bipolar voltage polarities ($+V_{Bip}$ to $-V_{Bip}$ and vice versa) which is faster than the mechanical response time of the switch. In this situation the moveable membrane cannot mechanically react to changes between bias levels and remains in the down-state over the entire stress time.

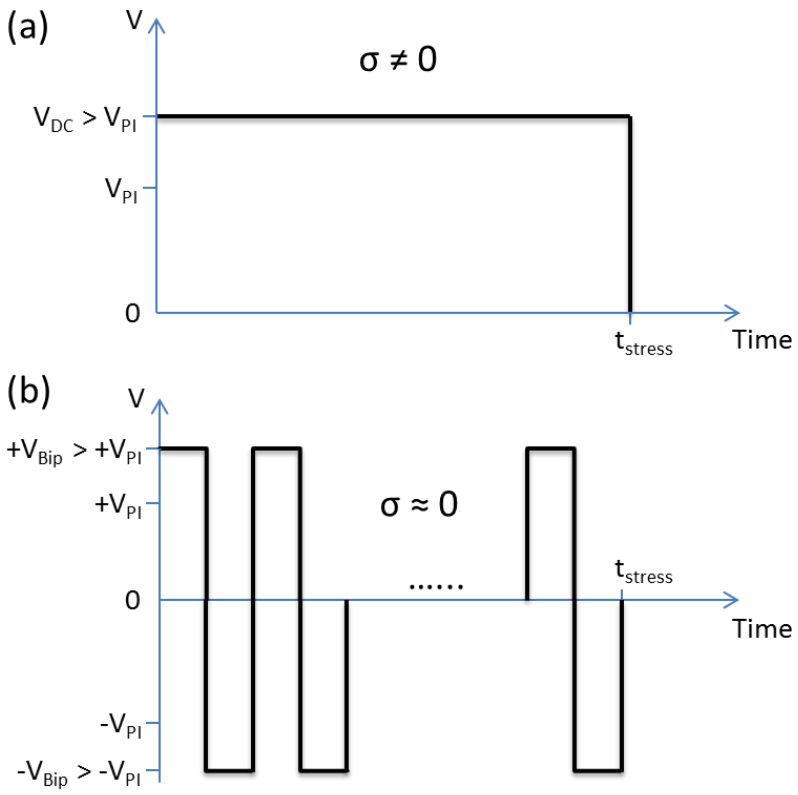

Figure 4.1: Schematic DC (a) and bipolar hold-down signals (b) used in this work. The bipolar signal has a 50% duty cycle and is expected to minimise the amount of dielectric charge σ created during the stress time.

The capacitive switches used in this work exhibit a switching time (the time required to move from the open state to the closed state and vice versa) of approximately 40 µs. The switching times were obtained using laser Doppler vibrometry to measure the movement of a switch membrane in response to an oscillating actuation signal. The membrane velocity was measured using a Polytec MSA-400 microsystem analyser while a 50 Hz unipolar bias was used to repeatedly actuate the membrane. The switch actuation and release times were extracted from the resulting velocity vs. time graph. The obtained switching times are plotted against the number of actuations in Figure 4.2.

A bipolar signal with a 50% duty cycle and a frequency of 100 kHz was viewed on an oscilloscope and found to have a transition time of approximately 0.5 µs, i.e. the time required for the signal to change from high level to low level and vice versa, as shown in Figure 4.3. The transition time of the bipolar signal is an order of magnitude faster than the mechanical response time of the switch. Therefore, if this bipolar signal was applied to a switch the very short transition time would ensure the membrane remained in the down-state for the duration of the experiment. Henceforth, any reference to bipolar hold-down signals will refer to a 100 kHz signal with a 50% duty cycle unless otherwise stated.

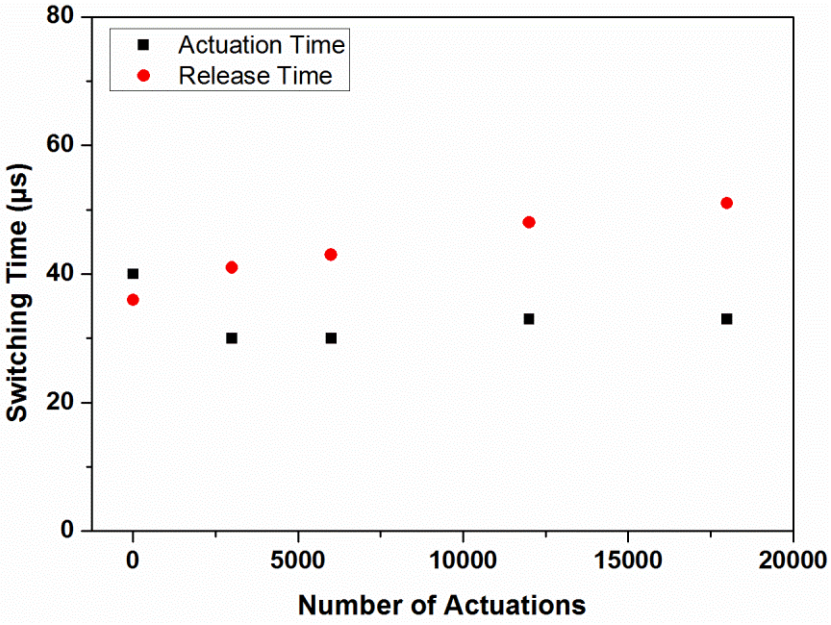

Figure 4.2: The switching times of a 100 µm^2 straight-type capacitive switch measured during a repeated cycling test.

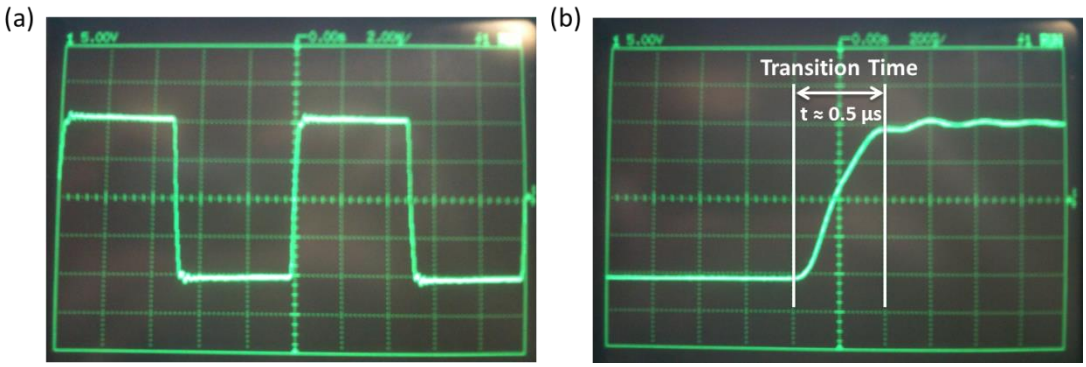

Figure 4.3: A typical square-wave bipolar signal used in this work is captured on a digital oscilloscope (a). The transition time of the signal is measured to be approximately 500 ns (b).

It is hypothesised that during the bipolar stress any dielectric charging which occurs under one voltage polarity is balanced by a subsequent amount of dielectric charging which takes place under the opposite voltage polarity. Therefore, any change in the device C-V curve is expected to be the result of mechanical degradation only. This hypothesis is investigated in the following section by comparing the effects of DC and bipolar hold-down signals on MEMS capacitive switches. Following the theory discussed in Chapter 3, it is expected that the net effect of dielectric charging after DC stress will result in a measurable C-V shift. If no such shift is observed when a bipolar hold-down signal is used then the method will be deemed successful.

4.2.2 Experimental Validation of the Bipolar Hold-Down Method on Titanium Switches

In this section experiments are described which show that the bipolar hold-down signal minimises the effects of dielectric charging in RF MEMS capacitive switches. Capacitive switches fabricated using titanium membranes were chosen to verify the charge-elimination properties of the bipolar hold-down method as titanium is a high strength metal (yield strength = 100-225 MPa [153]) and was therefore expected to be resistant to the effects of mechanical degradation. The effects of dielectric charging in titanium switches were first characterised by applying a -25 V DC bias to the bottom metal of a capacitive switch. Capacitance-voltage sweeps were performed to measure the pull-in and pull-out voltages at the beginning of the experiment and after the DC stress had been applied for 15 minutes. The full C-V curves of the titanium switch measured before and after the DC stress are shown in Figure 4.4.

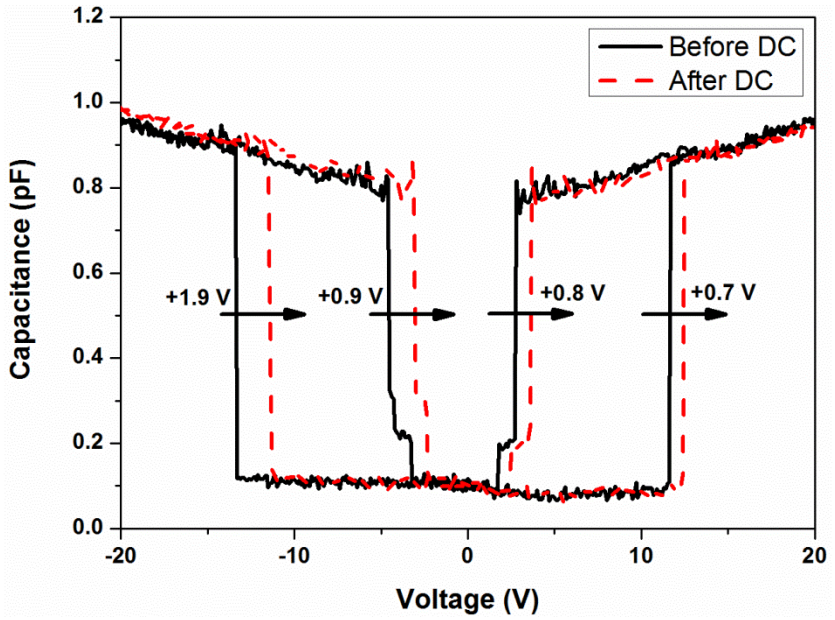

Figure 4.4: The C-V curves of a titanium switch measured before (black solid line) and after (red dashed line) 15 minutes DC stress at -25 V.

The DC stress resulted in a right-shift of the C-V curve, indicating that dielectric charging had taken place. For a measurement signal applied to the bottom electrode a right-shift indicates that negative dielectric charging has occurred. However, an asymmetric shift was observed in the positive and negative pull-in voltages which may have been caused by a combination of C-V shift and narrowing due to dielectric charging and mechanical degradation effects.

To gain further insight into the degradation mechanisms affecting the switch, the experiment was repeated for a longer stress time of 1 hour while transient changes in the positive and negative pull-in voltages were measured using periodic C-V sweeps. Only changes in the pull-in voltages were measured as this was where the asymmetry occurred. At the end of the stress phase, the bias was removed and the recovery of the switch under zero bias conditions was monitored for another hour. The same sequence of periodic C-V sweeps was used during both the stress and recovery periods to ensure that the measurement procedure had no effect on the charging results. At the end of the experiment, the measured ΔV_{PI} data was analysed to separate the effects of shift and narrowing from the overall changes in the switch C-V curve. The $V_{Average}$ and $V_{Difference}$ calculations used by Mulloni to separate the effects of C-V shift and narrowing were introduced in Chapter 3. The same calculations were used here, where the *Narrowing* and the *Shift* of the capacitive switch at time t were calculated using the following formulae

$$\Delta V_{Narrowing}(t) = V_{Average}(t) - V_{Average}(t=0), \tag{4.1}$$

$$\Delta V_{Shift}(t) = V_{Difference}(t) - V_{Difference}(t=0). \tag{4.2}$$

When the shift and narrowing are calculated in such a fashion both values will equal zero at time $t = 0$. $\Delta V_{Narrowing}$ will decrease as mechanical degradation or non-uniform dielectric charging occurs, while ΔV_{Shift} will increase or decrease depending on the direction of C-V shift as a result of uniform dielectric charging. The pull-in voltage shift and narrowing of the titanium switch was calculated during one hour of -25 V DC stress followed by one hour of recovery and these results are shown in Figure 4.5.

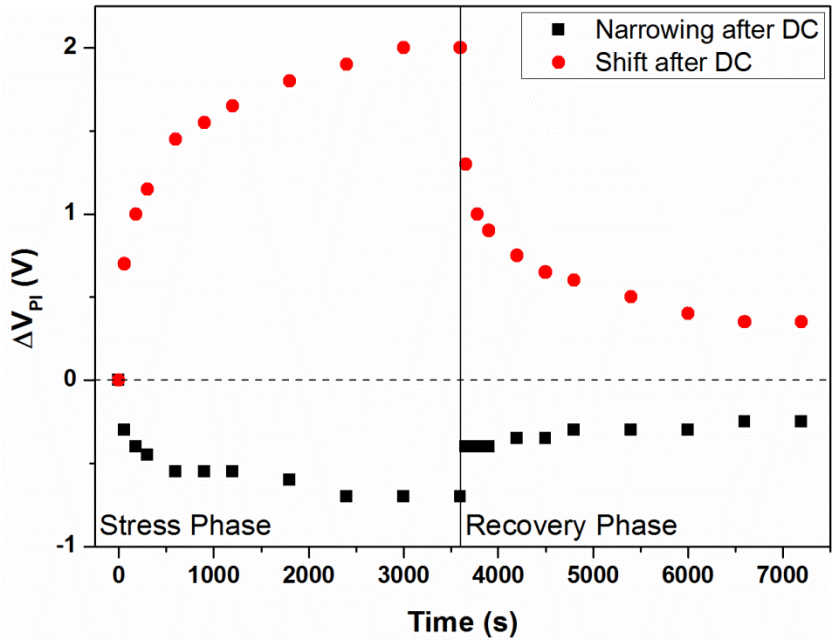

Figure 4.5: The *Shift* and *Narrowing* of titanium switch pull-in voltages in response to DC stress at -25 V.

During DC stress a time-dependent C-V shift was observed which peaked at ΔV_{Shift} = 2 V before gradually recovering to within 0.5 V of the initial condition once the stress bias had been removed. The C-V curve shifted to the right in agreement with the results obtained in Figure 4.4. As before, for a bias applied to the bottom metal a right-shift indicates that negative dielectric charging has occurred. Narrowing of the switch C-V curve was also observed during DC stress. The amount of narrowing peaked at $\Delta V_{Narrowing}$ = -0.7 V before returning to within 0.25 V of the initial condition. The narrowing effect may be due to a combination of mechanical degradation and non-uniform dielectric charging. More insight could be gained if dielectric charging could be removed so that the narrowing due to mechanical degradation could be studied in isolation. To achieve this, the previous experiments were repeated using a ±25 V bipolar hold-down signal with a 50% duty cycle and a frequency of 100 kHz and the results of this are shown in Figure 4.6.

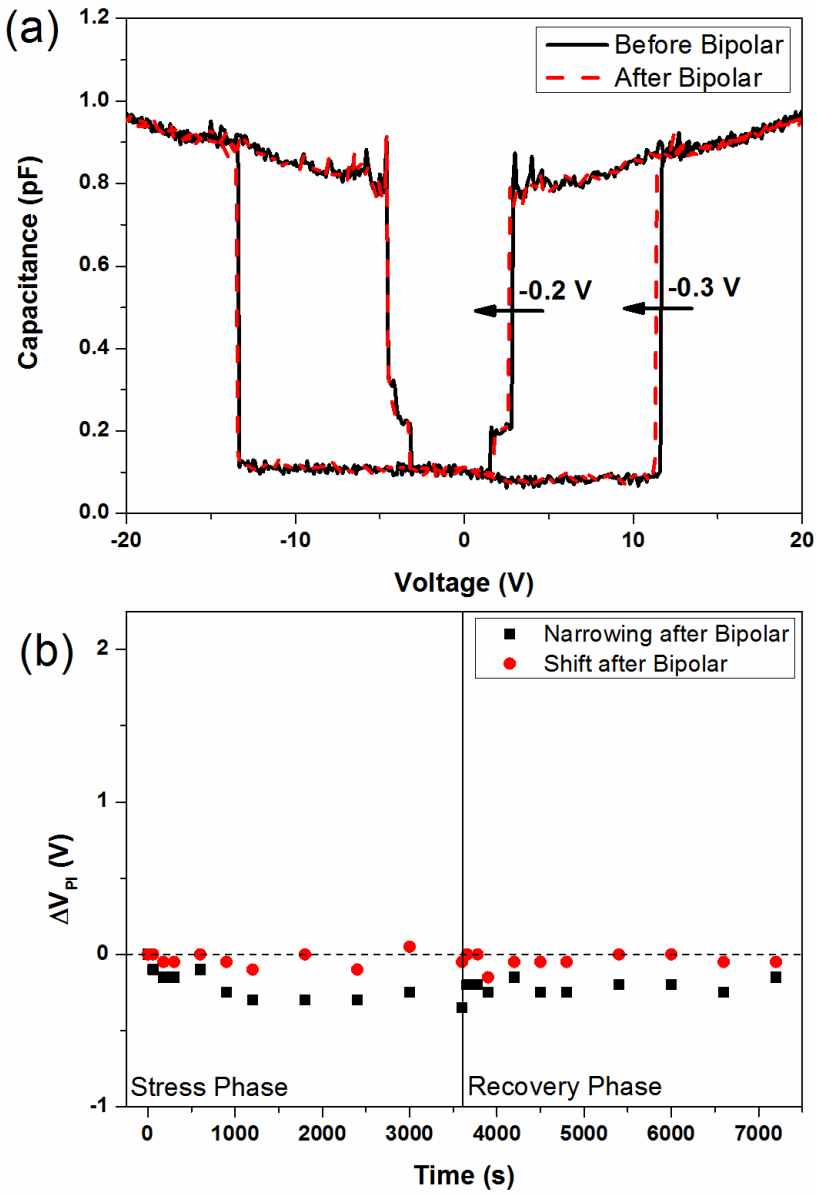

Figure 4.6: The C-V curves of a titanium switch measured before (black solid line) and after (red dashed line) 15 minutes of bipolar stress at ±25 V (a) and the *Shift* and *Narrowing* of the pull-in voltages of a titanium switch during an hour-long stress and recovery experiment at ±25 V (b). The vertical scale is the same as in Figure 4.5 for comparison.

Figure 4.6 (a) shows the C-V curve of a titanium switch measured before and after 15 minutes of bipolar hold-down stress. A left-shift was observed in the positive threshold voltages while no change was observed in the negative threshold voltages. The fact that the full C-V curve does not shift in one direction shows that dielectric charging has been successfully minimised by the application of a bipolar hold-down bias. However, the asymmetric shift observed in Figure 4.6 (a) suggests that either mechanical degradation or non-uniform dielectric charging continue to affect the operational characteristics of the device.

As before, to gain more information about the mechanisms affecting the device behaviour the experiment was repeated for a longer duration while periodic C-V sweeps were used to monitor any change in the pull-in voltages. By consulting the *Shift* and *Narrowing* data of Figure 4.6 (b) it can be seen that no significant shift was observed in the pull-in voltages of the titanium switch following the bipolar hold-down stress. This result confirms that the bipolar hold-down signal has successfully minimised the effects of dielectric charging in the capacitive switch. However, some narrowing was still observed in Figure 4.6 (b) following bipolar stress. Since it has been shown that the bipolar hold-down signal has minimised the effects of dielectric charging, the remaining narrowing can be attributed to mechanical degradation of the switch membrane. The asymmetry observed in the C-V narrowing may be an artefact of the measurement sequence and this will be discussed in Section 4.2.3. This result confirms that a bipolar hold-down signal can be used to study the effects of mechanical degradation in RF MEMS capacitive switches in isolation. However, because only a limited amount of mechanical degradation was observed on titanium switches a different test structure was required so that more analysis could be performed.

Aluminium has also been used as a structural material in RF MEMS capacitive switches fabricated at Tyndall National Institute. As aluminium is a softer metal than titanium (yield strength = 15-20 MPa [154]) it was expected to be much more susceptible to the effects of mechanical degradation. Therefore, the experiments presented in this section were repeated on capacitive switches fabricated using aluminium membranes. Switches with straight tethers were chosen for this investigation as these have been shown to be more susceptible to mechanical degradation when compared to alternative tether designs [35]. The increased sensitivity to mechanical degradation is caused by the poor ability of the straight tethers to dissipate mechanical stress built-up during actuation, whereas more flexible designs can accommodate the mechanical stress without significant changes to their spring constant and air-gap. The results of DC and bipolar experiments performed on straight-type aluminium capacitive switches are presented in the following section.

4.2.3 Characterisation of the Bipolar Hold-Down Method on Aluminium Switches

Aluminium capacitive switches were characterised following the same procedure applied to titanium switches in the previous section. First, a -25 V DC bias was applied to a switch for 15 minutes and full C-V curves were measured before and after the stress time to characterise the effects of dielectric charging. Then the experiment was repeated for a

longer duration while periodic C-V sweeps were used to measure any changes in the pull-in voltages. The measurement data was analysed using equations (4.1) and (4.2) to separate the effects of Shift and Narrowing from the overall changes in the device C-V curve. The results of both experiments are shown in Figure 4.7.

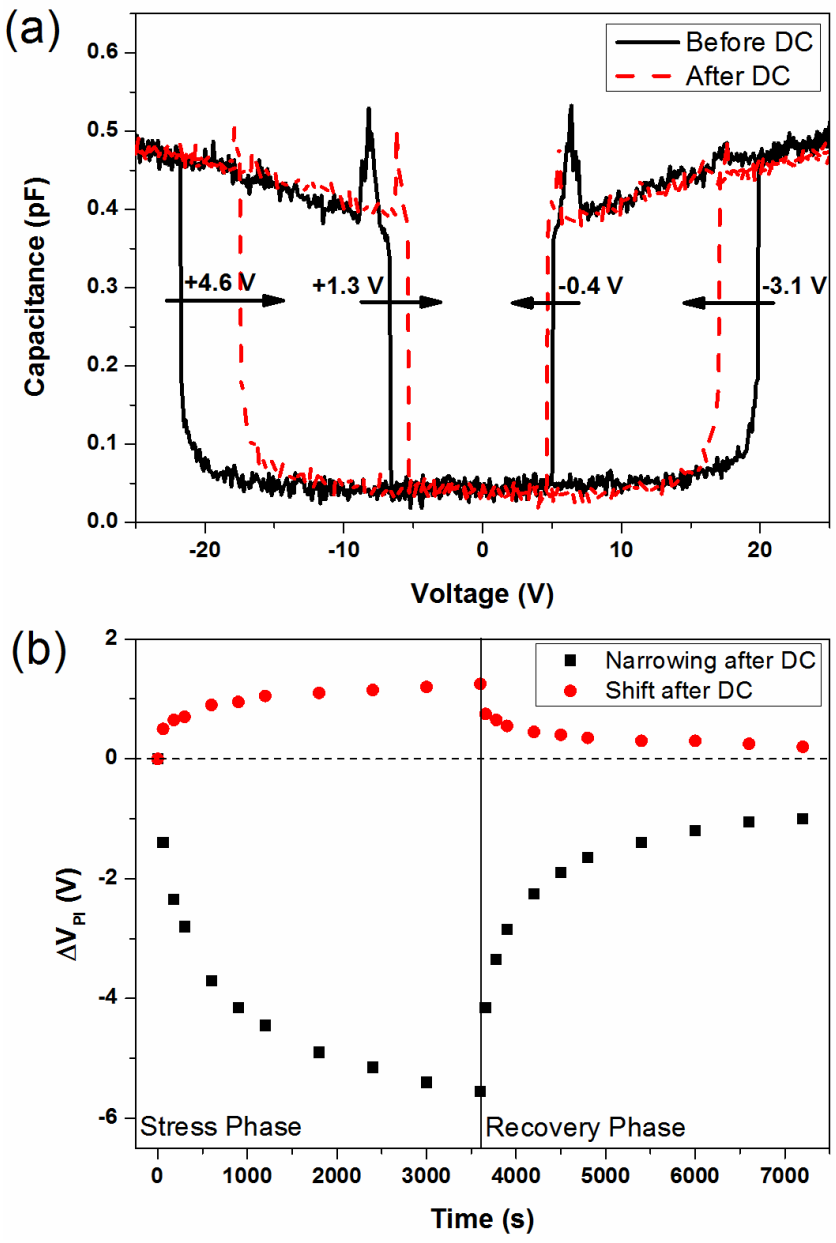

Figure 4.7: The C-V curves of an aluminium switch before (black solid line) and after (red dashed line) 15 minutes DC stress at -25 V (a) and the *Shift* and *Narrowing* of an aluminium switch during an hour-long stress and recovery experiment at -25 V DC (b).

In comparison to titanium switches, a reduced down-state capacitance of 0.5 pF was measured on the aluminium switch. The reduced down-state capacitance is due to a slightly rougher bottom electrode whose roughness was mirrored in the top surface of the

dielectric, as the PECVD dielectric formed a conformal layer on top of the electrode. Despite this physical difference between the two device types, the same dielectric of 130 nm SiO_2 was used in both cases and so the dielectric charging response was expected to be similar in each device.

Asymmetric narrowing of the switch C-V curve was seen after DC stress in Figure 4.7 (a). While this type of result indicates that both mechanical degradation and dielectric charging have taken place simultaneously, the greater amount of narrowing seen in the pull-in window indicates that mechanical degradation is mainly responsible for the C-V narrowing measured in this case, as discussed in Section 3.2.3. The amount of narrowing is more pronounced on the negative side of the C-V curve, which suggests that a right-shift due to dielectric charging has been superimposed on the narrowing effect. As the measurement signal was applied to the bottom electrode, this indicates that negative dielectric charging has taken place. The same polarity of dielectric charge was observed after DC stressing of the titanium switch in Figure 4.4. The fact that similar C-V shifts have been observed on titanium and aluminium switches under identical DC bias conditions confirms that the dielectric charging mechanism of the PECVD oxide has not been affected by the roughness of the bottom electrode.

This is confirmed by the time-dependent right-shift of the pull-in voltages which was measured during -25 V DC stress in Figure 4.7 (b). The shift magnitude peaked at 1.25 V after one hour of DC stress before gradually returning to within 0.2 V of its initial condition at the end of the recovery time. The C-V shift observed on the aluminium switch was lower than that observed on the titanium switch which may be due to the reduced contact area between the aluminium membrane and dielectric. However, since the time-dependent trend of the C-V shift observed after DC stress was common for both titanium and aluminium switches, it is believed that this effect was caused by the same dielectric charging mechanism. Therefore, since the bipolar hold-down signal was shown to minimise the effects of dielectric charging in titanium switches, it is expected that the same result will be obtained on aluminium-based RF MEMS capacitive switches. To verify this, the experiments were repeated using a ±25 V bipolar hold-down signal and the results are shown in Figure 4.8.

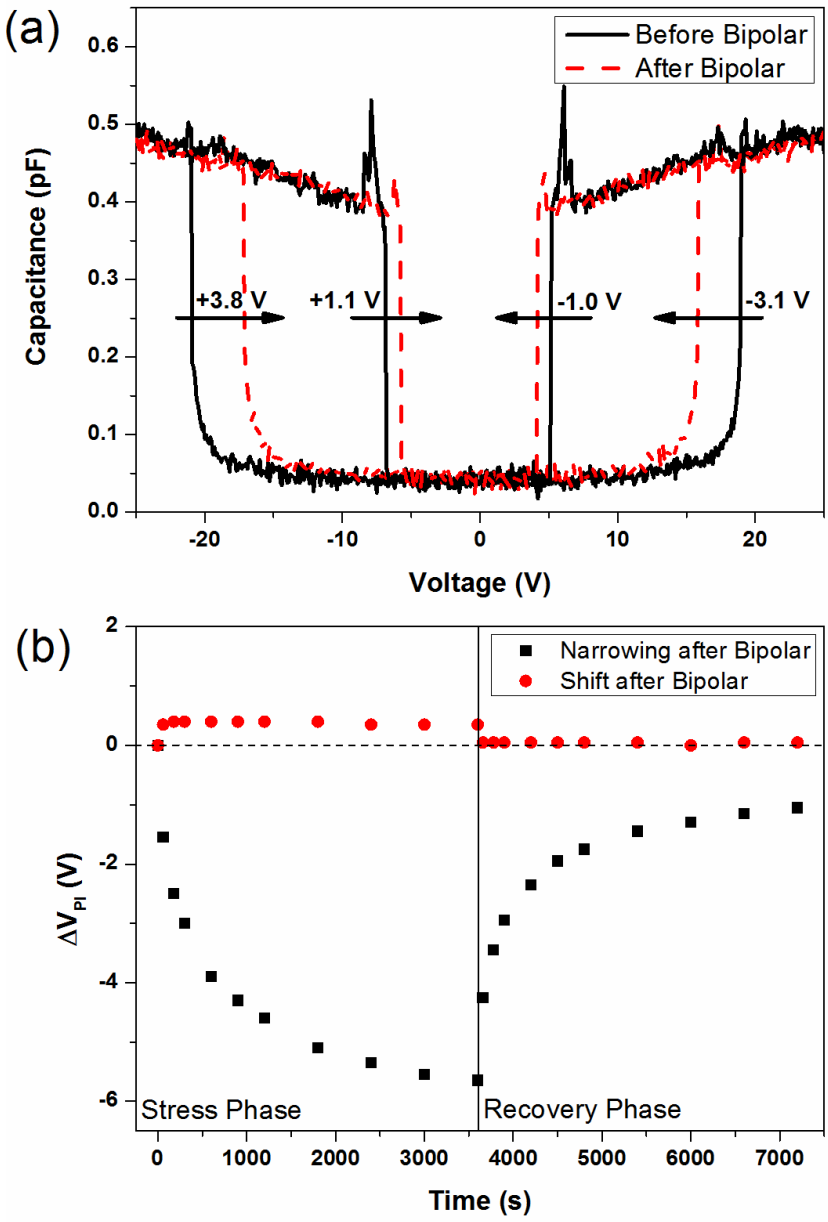

Figure 4.8: The C-V curves of an aluminium switch measured before (black solid line) and after (red dashed line) 15 minutes bipolar stress at ±25 V (a) and the *Shift* and *Narrowing* of an aluminium switch during an hour-long stress and recovery experiment at ±25 V (b).

In Figure 4.8 (a) it can be seen that narrowing of the C-V curve still occurs; however, it is now approximately symmetric about the 0 V axis. The fact that narrowing occurs regardless of whether a DC or bipolar bias has been applied indicates that mechanical degradation is the dominant degradation mechanism of aluminium switches. This is confirmed by the transient narrowing of the pull-in voltages shown in Figure 4.8 (b) which peaks at the same magnitude ($\Delta V_{Narrowing}$ ≈ -5.6 V) after DC and bipolar stress. As before, the *Narrowing* was recoverable and returned to within 0.5 V of its initial condition after the stress bias had been removed.

A 0.4 V *Shift* was also observed in the aluminium device after bipolar stress; however, this behaved very differently to the *Shift* observed after DC stress. In contrast to the time-dependent shift in Figure 4.7 (b), the 0.4 V shift in Figure 4.8 (b) appeared immediately after the bipolar stress was applied, it remained approximately constant while the stress was maintained and it disappeared immediately after the stress was removed. In contrast to the time-dependent C-V shifts observed after DC stress on aluminium and titanium switches, the instant 0.4 V shift is uniquely observed on the aluminium switch during bipolar stress. Since it has been shown that the bipolar signal succeeds in removing the effects of dielectric charging, it must be concluded that the observed C-V 'shift' is caused by some other mechanism. As the constant 'shift' was only measurable while the bipolar signal was being applied, it is hypothesised that the rapid recovery of some mechanical degradation in the time it takes to perform two sequential C-V measurements is responsible for the observed offset of the C-V curve. In this series of experiments a negative C-V sweep was measured first followed by a positive C-V sweep. However, the limited speed of the measurement equipment created a 20 second delay between the measurements of each pull-in voltage. If some mechanical degradation recovered in the time between each C-V sweep then less narrowing would be measured on the positive V_{PI} than on the negative V_{PI} and the C-V curve would appear to be artificially right-shifted. To test this hypothesis, the same experiment was repeated on the same device with the sweep order reversed i.e. a positive C-V sweep was performed first followed by a negative C-V sweep. As before the transient ΔV data was analysed using the *Shift* and *Narrowing* calculations and these results are compared with the previous experiment in Figure 4.9.

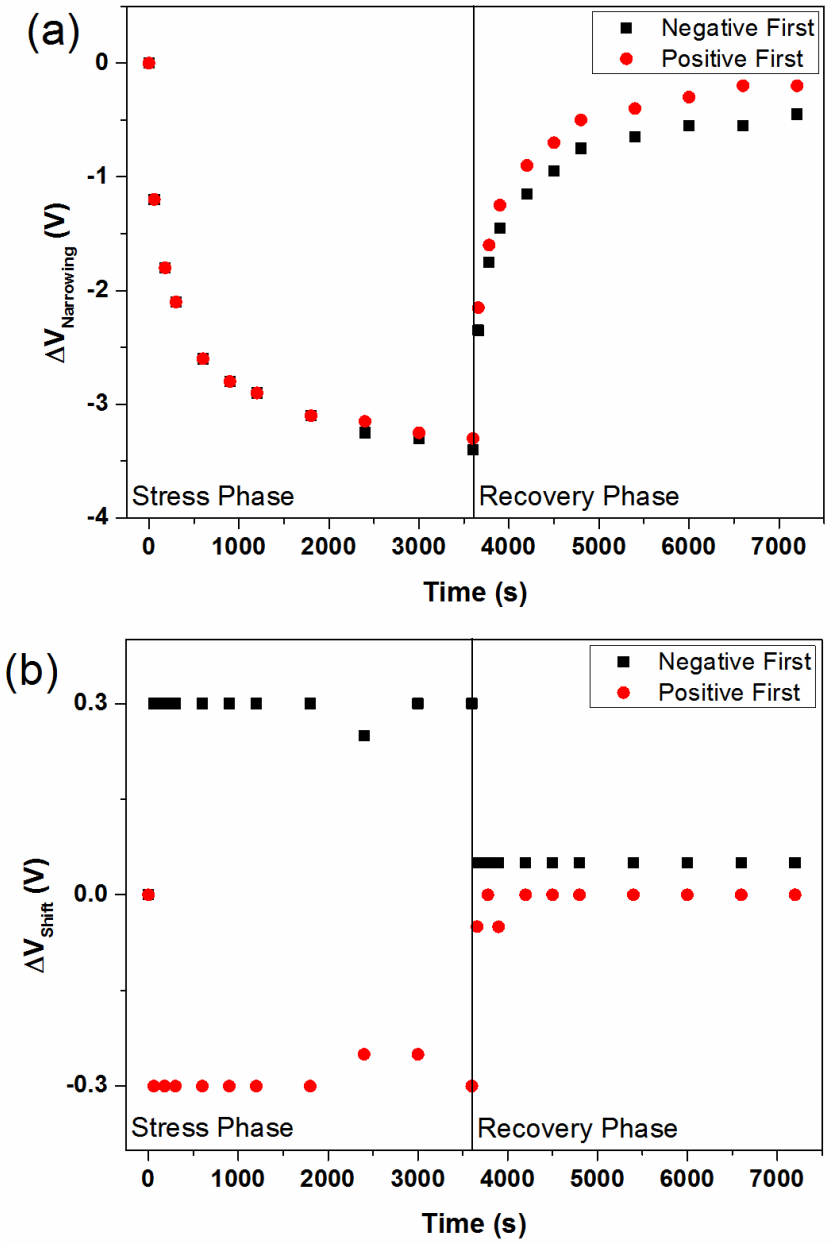

Figure 4.9: The calculated *Narrowing* (a) and *Shift* (b) of an aluminium switch during two bipolar hold-down experiments. The same bipolar stress was used in each case, but the order of C-V sweeps was changed from negative first (black squares) to positive first (red circles).

The same magnitude of narrowing was observed in each experiment in Figure 4.9 (a), which indicates that the same amount of mechanical degradation occurred in each case. The same magnitude of shift was also observed in Figure 4.9 (b); however, the direction of C-V shift was reversed. Dielectric charging caused by the C-V sweeps can be discounted as the source of this shift as the same pattern of C-V measurements was used during all stress and recovery phases, while the effect was only measurable during the stress phase. Additionally, given that this effect was not observed on titanium devices, and given that mechanical degradation is the dominant degradation mechanism of aluminium devices, it

can be concluded that the measured 'shift' was caused by the rapid recovery of mechanical degradation during the time delay between two sequential C-V sweeps.

Therefore, the measured 'shift' or offset is dependent on the order in which the C-V sweeps were performed and is an artefact of the measurement procedure. As mentioned previously, the limited speed of the laboratory equipment creates a 20 second delay between sequential C-V sweep measurements. This is a function of the measurement procedure and may be avoided if faster equipment is used. Alternatively, the 20 second interval created between sequential C-V sweeps can be avoided if only one polarity C-V sweep is measured. Not only will this reduce the time required for the experiment to be performed, it will also allow the full extent of mechanical degradation which has taken place during a stress cycle to be measured using only one polarity C-V sweep. Moreover, since it was shown in Chapter 3 that pull-in voltages are more sensitive to mechanical degradation than pull-out voltages, only one pull-in voltage of the same polarity as the stress bias will be measured to take full advantage of this effect.

To validate this method, a series of experiments was performed where various negative DC biases and bipolar signals were used to stress an aluminium device. Different voltage magnitudes were used to accelerate dielectric charging while the same mechanical stress was maintained for each voltage by holding the membrane in the down-state for an equal amount of time in each case. The transient pull-in voltage changes were measured by performing periodic C-V sweeps, as before. However, in this case only the negative pull-in voltage was measured during the stress time. The device was allowed to completely recover before each experiment was performed and the results of this are shown in Figure 4.10 (a).

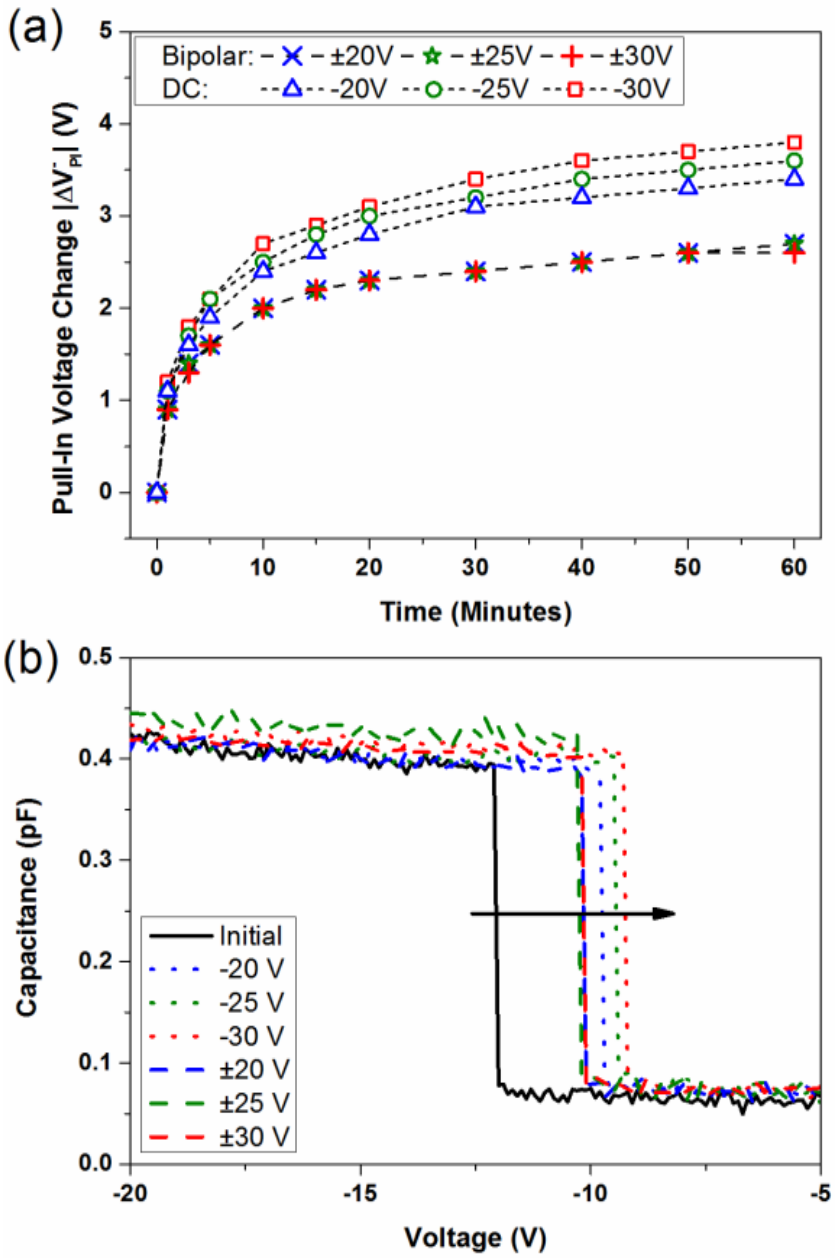

Figure 4.10: The change in the negative pull-in voltage (ΔV_{PI}^-) of an aluminium switch as it is held in the down-state using different DC and bipolar biases (a). Note that the C-V curve narrows during each test, while a superimposed right-shift due to dielectric charging results in an increased ΔV_{PI} at the end of each DC stress period (b).

DC biases of -20 V, -25 V and -30 V and bipolar biases of ±20 V, ±25 V and ±30 V were applied to the switch for one hour while changes in the negative V_{PI} were monitored. The negative pull-in voltage decreased during each measurement which corresponds to narrowing of the C-V curve, while in Figure 4.10 (b) it can clearly be seen that using a DC bias to stress the device resulted in a larger change of the pull-in voltage than in any case where a bipolar bias was used. The voltage-dependent change due to DC biasing is proof

that dielectric charging has occurred as an additional right-shift has been superimposed on top of the narrowing effect. Almost no difference in ΔV_{PI} was observed between each of the bipolar biases; therefore, the overlapping stress characteristics in Figure 4.10 (a) and (b) confirm that purely mechanical degradation has taken place as a result of the bipolar method. Moreover, these results confirm that the C-V curve offset observed in Figures 4.8 (b) and 4.9 (b) is a measurement artefact which can be avoided if only one polarity C-V sweep is performed. Therefore, only one polarity C-V sweep will be used for the rest of this chapter to characterise the effects of mechanical degradation in aluminium-based RF MEMS capacitive switches.

This section has shown that mechanical degradation in capacitive switches can be isolated through the application of a bipolar hold-down signal. The identification of different mechanical degradation mechanisms may then be achieved by studying the stress and recovery curves of these switches for recognisable traits [152]. This method allows standard electrical characterisation techniques to be used for the investigation of mechanical degradation in MEMS switches. Additionally, it was shown that the dominant degradation mechanism in a capacitive switch depends on the composition of the movable electrode. Since mechanical degradation is the dominant reliability mechanism in aluminium switches, devices featuring aluminium membranes were selected for the study and characterisation of mechanical degradation effects. The following sections contain details of experiments and analysis performed on aluminium switches to identify the different mechanical degradation effects present in a switch.

4.3 CHARACTERISATION OF MECHANICAL DEGRADATION

4.3.1 The Creep Effect

Mechanical tests on thin metal films and cantilevers have shown that these test structures can be affected by permanent and recoverable material deformation as a result of the increased mechanical stress and strain created during device actuation [71, 97, 98, 148, 155]. Since the dimensions and composition of the aluminium membranes used in this work are similar to the structures investigated in [71, 97, 98, 148, 155], it is expected that the same mechanical deformation processes will be present. In order to observe these effects, repeated bipolar stress and recovery experiments were performed on a switch while periodic C-V sweeps were used to monitor the material deformation through changes in the pull-in voltage. The effects of individual degradation mechanisms could not be

distinguished during the stress period when multiple degradation mechanisms simultaneously affected the device pull-in voltage; however, by monitoring the recovery of the switch after the removal of the bias, a distinction could be made between the effects of permanent and recoverable mechanical deformation. For example, pull-in voltage changes due to plastic deformation (or creep) of the membrane material can be identified if the V_{PI} does not return to its initial value at the end of the experiment. To investigate the mechanical degradation of switches, a virgin device with an aluminium membrane was subjected to repeated stress and recovery cycles while the negative pull-in voltage change was monitored. The switch was mechanically stressed for one hour using a ±25 V bipolar hold-down voltage and was then allowed to recover for another hour under zero bias. This stress and recovery pattern was repeated sequentially 6 times for a total experimental duration of 12 hours and the ΔV_{PI} results of this experiment are shown in Figure 4.11.

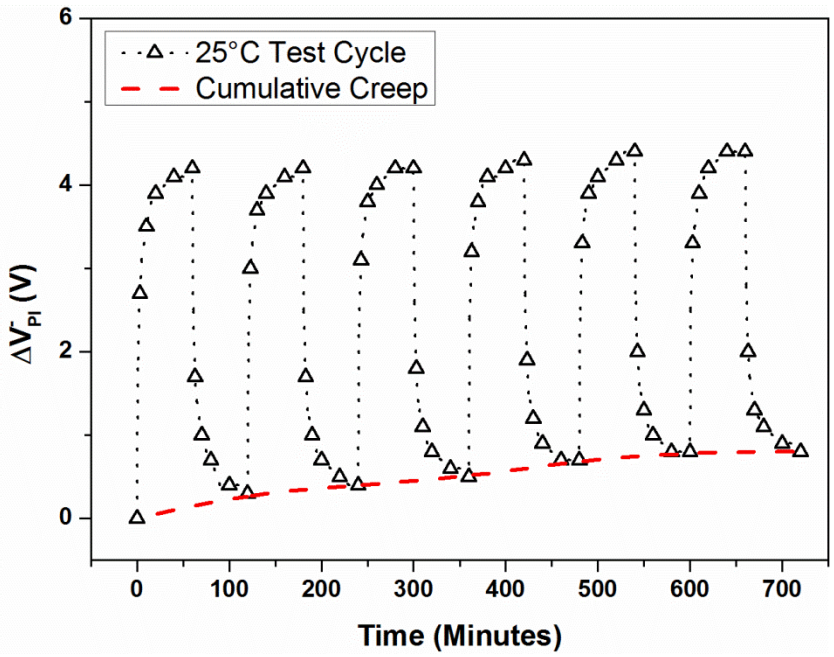

Figure 4.11: Evolution of the creep effect in an aluminium switch. The black dotted line and triangles trace the magnitude of C-V narrowing and recovery during 6 strain/recovery cycles, while the red dashed line indicates the accumulated ΔV_{PI} over time.

In Figure 4.11 the ΔV_{PI} over the course of the experiment is indicated by hollow triangles while the final measurement points after recovery are joined with a red dashed line as a visual aid. It can be seen that during an individual stress/recovery cycle the V_{PI} changed by as much as 4 V before recovering close to the initial, unstressed value. However, after each recovery period some ΔV_{PI} had not recovered. Over time this resulted in a cumulative change in the pull-in voltage. This plastic deformation is a mechanical degradation

mechanism known from materials science and has been observed to occur in metals, ceramics and polymers [156-159]. The amount of plastic deformation (creep) which takes place in a material is dependent on the material properties, the magnitude and duration of the applied stress and the temperature of the material during the application of a load [160]. For a given applied stress, the creep effect undergoes a three-stage evolution where the rate of creep initially decreases with time until a steady-state regime is attained, before it increases again and results material failure [161]. Plastic material deformation takes place through the movement of dislocations or the diffusion of atoms through the material lattice [162] and is caused by an increase in strain in response to an applied stress [163].

The experimental data of Figure 4.11 indicates that the creep effect tends towards saturation with repeated stress/recovery cycles as indicated by the red dashed line. It is hypothesised that this phenomenon is caused by holding the switch in the down-state for a sufficiently long period of time to allow the steady-state creep regime to be attained. Therefore, by subjecting a switch to a constant stress level for a sufficient amount of time it is hypothesised that the majority of creep can be saturated. Then whatever remaining mechanical deformation is measured at lower stress levels can be assumed to be the product of transient mechanical degradation only. By observing the recoverable ΔV_{PI} after each stress period, the creep effect can be assumed to be fully saturated when the final recovered V_{PI} value no longer changes with subsequent test cycles. This appears to occur in Figure 4.11 where the total ΔV_{PI} due to the creep effect at 25°C was 0.8 V. However, since the creep effect is highly dependent on the stress conditions to which a material is exposed [160], if the experimental conditions are changed (for instance by exposing the device to higher temperatures or increased stress levels) then more creep will occur in the device material which would cause a further change in the V_{PI}. To investigate this, the experiment was repeated at higher temperatures using sequential stress and recovery cycles to monitor to accumulated deformation of the switch. The results of an experiment performed on the same switch at 35°C are shown in Figure 4.12.

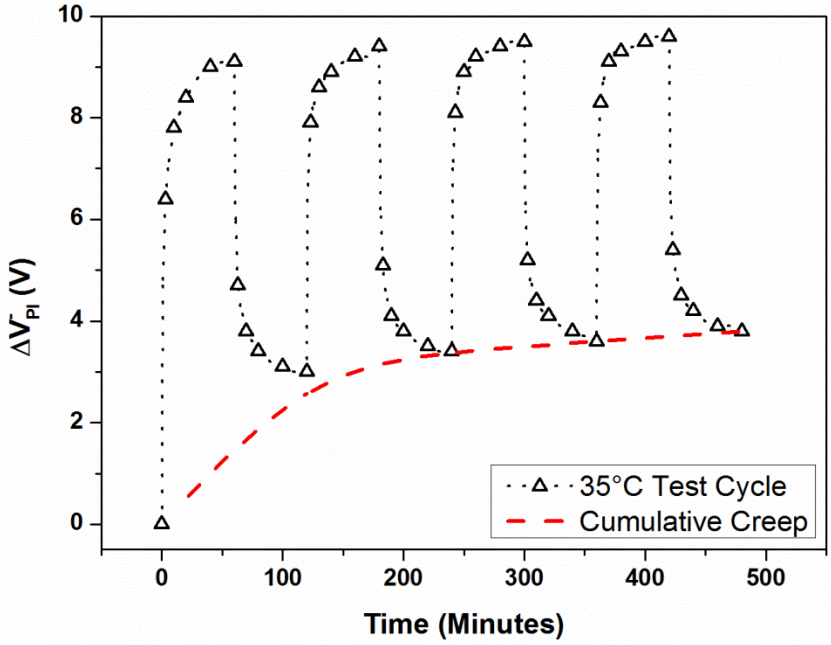

Figure 4.12: The transient (black dotted line) and cumulative (red dashed line) change in the negative V_{PI} of a capacitive switch during a mechanical stress experiment at 35°C.

The temperature acceleration of mechanical degradation can immediately be seen by the large increase in ΔV_{PI} during individual stress cycles. In Figure 4.12 the bipolar stress at 35°C initially results in a pull-in voltage change of approximately 9 V before recovering to within 3 V of the unstressed value, resulting in a recoverable ΔV_{PI} of 6 V which was measured consistently throughout the experiment. Following several stress and recovery cycles the unrecovered ΔV_{PI} appeared to be saturating at approximately 3.5 V; however, an equipment failure forced the experiment to be stopped prematurely after 8 hours. Once the effects of transient mechanical deformation had fully recovered the temperature of the chamber was increased to 45°C and the experiment was repeated. This result is shown in Figure 4.13.

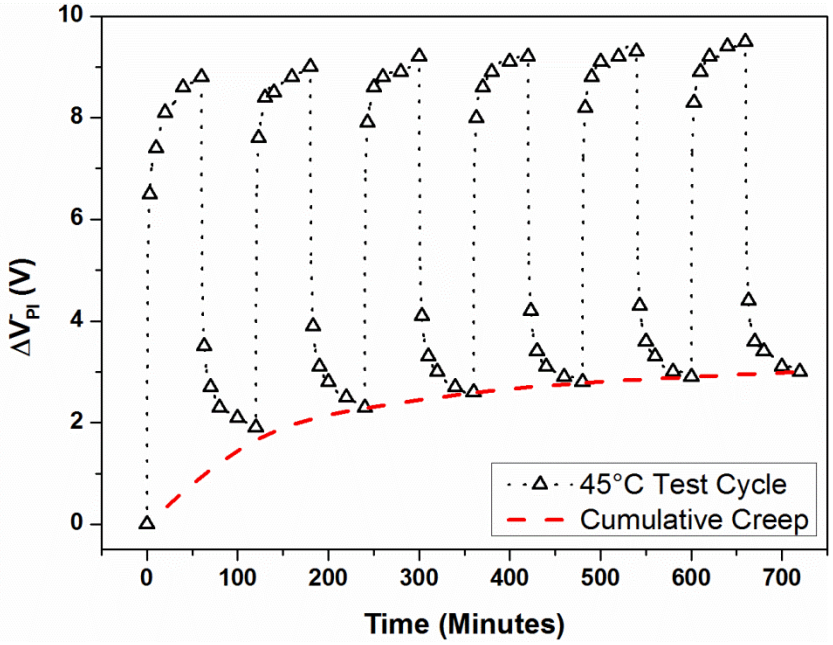

Figure 4.13: The transient (black dotted line) and cumulative (red dashed line) change in the negative V_{PI} of a capacitive switch during a mechanical stress experiment at 45°C.

At 45°C the bipolar stress caused an initial ΔV_{PI} of approximately 9 V before recovering to within 2 V of the unstressed value. This recoverable ΔV_{PI} of 7 V was measured consistently throughout the experiment and indicates that the transient component of mechanical degradation has been further accelerated by temperature. At the end of 6 stress and recovery cycles the creep effect amounted to an unrecovered ΔV_{PI} of approximately 3 V; however, the saturation of this effect had not yet been observed. While this result suggests that more long-term stress periods at 45°C may be required before the creep effect is completely saturated, by saturating the majority of creep at higher temperatures it can be assumed that the mechanical degradation experienced at lower stress levels should be the product of recoverable material deformation mechanisms only.

The results in this section have shown that the plastic mechanical deformation due to the creep effect is a serious reliability concern in MEMS switches fabricated using aluminium membranes. On a single device a cumulative change in V_{PI} of 0.8 V was measured at 25°C, subsequently followed by cumulative changes of 3.8 V and 3 V as the temperature was increased to 35°C and 45°C, respectively. Therefore, the three experiments depicted in Figures 4.11-4.13 resulted in a plastic deformation of the switch material which amounted to a pull-in voltage change of approximately 7.5 V. As RF MEMS capacitive switches for space applications are expected to function over a temperature range of -50°C to 125°C [164] and the creep effect can result in large pull-in voltage changes over a small fraction of

this range, it can be understood how the plastic deformation of switch material during hold-down operation is a serious reliability concern for the long-term operation of these devices. However, it has been shown that the creep effect can be saturated at a particular level of stress and strain by holding a device in the down-state for a sufficient amount of time. Once the creep effect has been saturated in such a fashion, an isolated study of any remaining transient mechanical degradation of the switch material can be performed. Details of experiments to investigate this are given in the following sections.

4.3.2 The Viscoelastic Effect

Transient and recoverable mechanical degradation such as that reported in the previous section is believed to be caused by a material stress relaxation mechanism known as the viscoelastic effect [97, 98, 148, 155]. The viscoelastic effect is characterised by a time-dependent relationship between stress and strain [165, 166] and has been observed to occur in a wide range of materials including polymers, metals, quartz and human tissue [167-170]. The viscoelastic response of metals is caused by the movement of material grains through a process called grain boundary sliding (GBS) [166, 171-173]. Back-stresses are generated by this granular rearrangement that cause the material to return to its original form once the applied stress has been removed.

Time-dependent material deformations have been observed in thin metal films [97, 148] and MEMS varactors [106, 174] which show viscoelastic behaviour; however, no measurements of the viscoelastic effect have been performed on functional MEMS switches. The viscoelastic effect may be studied in capacitive switches by observing the time-dependent effect it has on the device pull-in voltage, $\Delta V_{PI}(t)$. Recall that the V_{PI} of a capacitive switch is given by equation (2.7) as

$$V_{PI} = \sqrt{\frac{8k}{27\varepsilon_0 A}\left(g_0 + \frac{d}{\varepsilon_r}\right)^3}\,. \tag{4.3}$$

In the absence of dielectric charging, any change in the pull-in voltage will be caused by a change in the spring constant k and/or air gap g_0, as discussed in Chapter 3. The Young's modulus of a material can be thought of as a spring constant for solids [175], and for viscoelastic materials the Young's modulus follows a time-dependent relationship that depends on the ratio of the stress and strain in the material [176]. Therefore, for a moveable membrane composed of viscoelastic material, this time-varying modulus will cause a time-dependent change of the pull-in voltage $\Delta V_{PI}(t)$. A further classification of

mechanical degradation – linear viscoelasticity, requires that the relaxation modulus be independent of the magnitude of stress and strain [148]. Therefore, for a linear viscoelastic material, it is expected that the time dependence of material stress relaxation during a strain cycle to be equal to its recovery during a recovery cycle. This phenomenon was investigated by monitoring the ΔV_{PI} of a device during one hour of bipolar stress followed by one hour of recovery under no bias. Figure 4.14 shows the results of such an experiment performed on a creep-saturated aluminium device at room temperature. On this graph the stress and recovery characteristics have been overlaid to highlight the similarity of their time dependence.

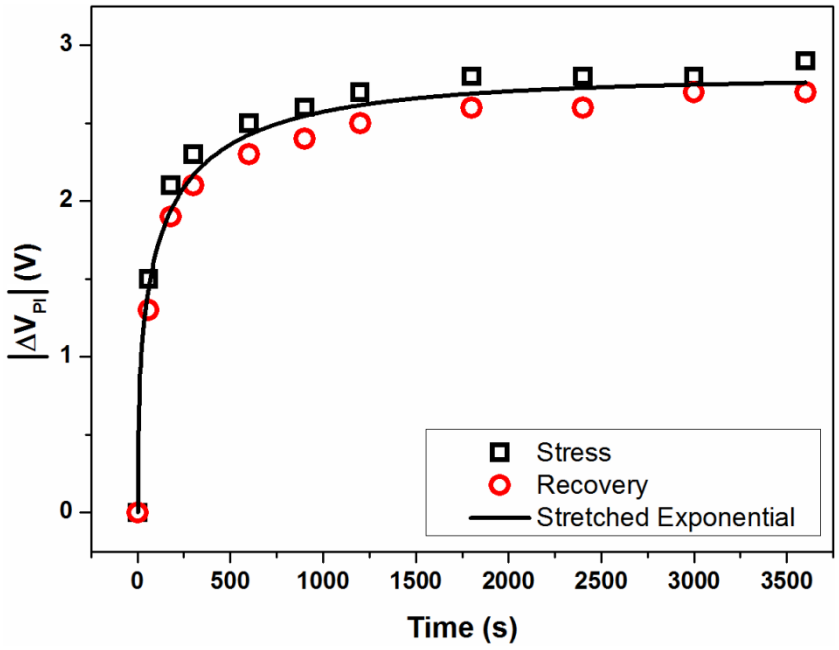

Figure 4.14: Overlaid stress and recovery characteristics obtained from viscoelastic tests on a creep-saturated aluminium switch. The solid line corresponds to a stretched-exponential fit with time constant τ = 121 ± 9 seconds.

The experimental data has been fitted using a stretched exponential model which takes the form

$$\Delta V_{PI}(t) = \Delta V_{PI,R}\left(1-\exp\left(-\left(\frac{t}{\tau}\right)^{\beta}\right)\right), \tag{4.4}$$

where $\Delta V_{PI}(t)$ represents the change in the pull-in voltage over time, $\Delta V_{PI,R}$ is the relaxed pull-in voltage change, τ is the characteristic time constant of the process and the dimensionless stretching factor $0 < \beta < 1$ accounts for the multiple time constants needed to describe real experimental data [177]. A distribution of time constants more accurately

reflects the time-dependent deformation of a viscoelastic material [158, 178] as this behaviour depends on several processes including the movement of molecular segments of different lengths and the varying sizes and orientations of material grains. The stretched exponential equation (4.4) is based on the Generalised Maxwell model [179] which is widely used to model the viscoelastic response of materials [176]. This model is composed of as many spring-dashpot combinations as are required to accurately represent the different time constants of a stress relaxation mechanism. Similar models with multiple elements have also been used to describe the viscoelastic deformation of thin metal films where a sufficient number of components were placed in series until a satisfactory fit was obtained [97, 98]. The model expressions in these instances can be long and complicated, taking the forms of finite sums or Prony series. For the sake of simplicity, these models may be reduced to much smaller expressions represented by a stretched exponential function [137].

Excellent agreement was obtained between the measured data and the model (4.4) for the stress and recovery curves in Figure 4.14. While the recovery curve is offset from the stress curve by an average value of 0.1 V which may be due to a residual dielectric charging effect, a characteristic time constant of $\tau = 121 \pm 9$ seconds was found to fit the data in both cases with a R^2 value of 0.998 for stress and 0.997 for the recovery data. Therefore, the stress and recovery characteristics show the same time-dependence and hence identify linear viscoelasticity as the mechanism responsible for the transient mechanical degradation observed in aluminium switches.

There are several processes which are known to cause transient stress relaxation behaviour such as grain boundary sliding or the diffusion of atoms within a material [168-170]. The primary degradation mechanism responsible for stress relaxation can be identified by calculating the activation energy of the process and comparing this with known values from the literature [155]. The activation energy can be obtained by studying the temperature dependence of the viscoelastic effect on creep-saturated devices. Details of this characterisation are described in the following section.

4.3.3 Temperature Acceleration of the Viscoelastic Effect

Further characterisation of the viscoelastic effect was performed by investigating the temperature dependence of transient mechanical degradation in creep-saturated aluminium switches. As before, a bipolar bias was used to mechanically stress a device for one hour while periodic C-V sweeps were used to monitor the ΔV_{PI}. When the switch had

fully recovered the experiment was repeated at a higher temperature. However, a maximum temperature of 35°C was used during mechanical stress experiments to ensure that temperature acceleration of the creep effect did not affect the measurement results. The results of these experiments are shown in Figure 4.15.

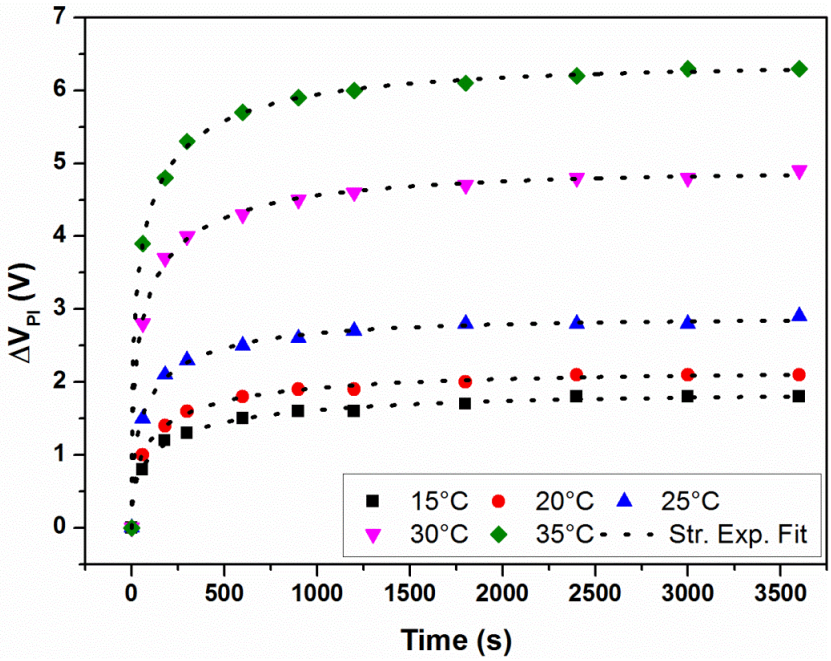

Figure 4.15: Temperature acceleration of the viscoelastic effect in an aluminium switch. The stretched exponential model (4.10) has been used to fit each set of data.

The temperature acceleration of the viscoelastic effect can clearly be seen by the increased ΔV_{PI} with increasing temperature. The stretched-exponential model (4.4) was used to fit the data for each temperature, and the obtained fitting parameters are shown in Table 4.1.

Table 4.1: Fitting parameters for a stretched-exponential model applied to the temperature data of Figure 4.15.

Temperature	R^2	$\Delta V_{PI,R}$ (v)	τ (s)	β
15°C	0.9964	1.85	194	0.44
20°C	0.9979	2.14	159	0.45
25°C	0.9978	2.87	109	0.44
30°C	0.9989	4.90	85	0.40
35°C	0.9996	6.36	69	0.37

It can be seen that higher temperatures decreased the characteristic time constant of the viscoelastic effect τ, which may also be expressed as an increase in the rate constant $\kappa = 1/\tau$ [180].

The temperature dependence of the rate constant can be used to extract the activation energy E_A of the process using an Arrhenius equation [181]

$$\kappa = A\exp\left(\frac{-E_A}{k_B T}\right), \tag{4.5}$$

where k_B is the Boltzmann constant and T is the absolute temperature measured in kelvins. An Arrhenius plot was created from the natural logarithm of the rate constant plotted against the inverse temperature as shown in Figure 4.16. Straight line fitting to the data allowed the activation energy of the process E_A = 0.41 eV to be calculated. This value is very close to the reported value of 0.4 eV for the activation energy of grain boundary diffusion in aluminium [182, 183].

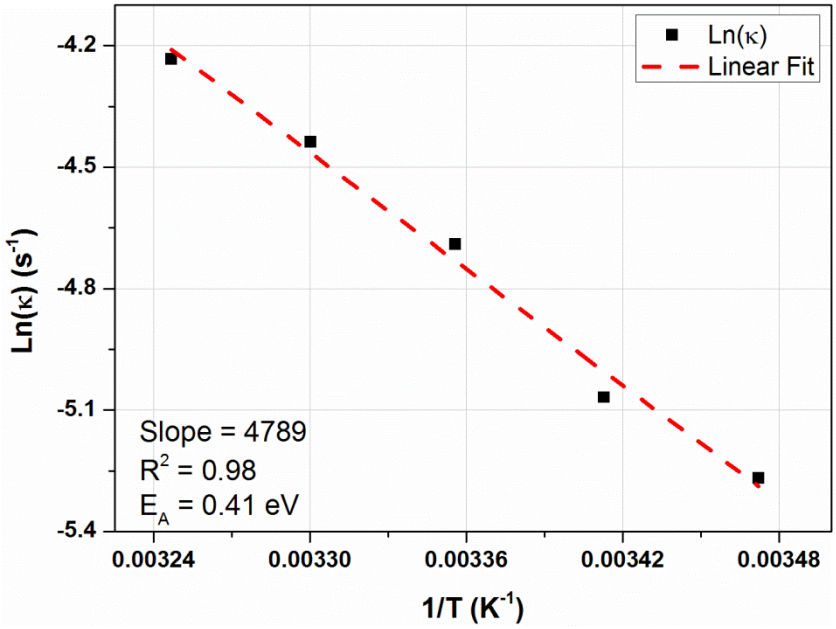

Figure 4.16: Arrhenius plot of the viscoelastic effect.

Grain boundary diffusion is a stress relaxation mechanism of structural bulk materials at high temperatures and it has also been found that the small grain sizes present in micron-scale thin films allow this phenomenon to be observed at room temperature [162, 166, 171-173]. The measured relaxation times are dependent on grain size and grain orientation, as well as the rate of atomic transport [162]. At room temperature, the

relaxation time of grain boundary sliding in aluminium thin films has been calculated to be approximately 90 seconds [178]. This value is in close agreement to the modelling results contained in Table 4.1 and confirms that stress relaxation due to grain boundary sliding is responsible for the measured viscoelastic effect in RF MEMS capacitive switches with aluminium membranes.

In summary, the results and analysis described in this section are the first experimental evidence that the movement of dislocations through grain boundary sliding is the cause of transient mechanical degradation in aluminium-based RF MEMS capacitive switches. Additionally, it is hypothesised that a similar mechanism known as diffusional creep may be responsible for the permanent mechanical deformation measured on the same switches [161]. Therefore, if an alternative material could be engineered where movement of material grains was hindered by some means, then more mechanically robust MEMS devices could be fabricated. Fortunately, several methods of material strengthening are already known to the engineering community. Methods such as work hardening and solid solution strengthening improve the yield stress of a material by introducing further dislocations or lattice distortions into the material which impede dislocation motion [184]. Alternatively when two materials are alloyed, precipitates of one material may form around the grains of the other which make it more difficult for dislocation motion to occur [185]. This strengthening mechanism is known as precipitation hardening and is used in this work to develop an aluminium alloy for use in MEMS devices. Details of the fabrication and characterisation of devices made using this material are given in the following section.

4.4 MATERIAL SOLUTION TO MECHANICAL DEGRADATION

Switches fabricated using aluminium membranes have been shown to be particularly susceptible to mechanical degradation in the form of viscoelasticity and creep. Even though aluminium metal is a very attractive material for use in RF MEMS devices due to its high conductivity (37 MS/m [186]), established fabrication know-how and ease of integration with CMOS fabrication processes, it has been concluded that pure aluminium is an unsuitable structural material for use in capacitive switches. At the beginning of this chapter switches fabricated with titanium membranes were shown to be mechanically more reliable. However, the lower conductivity of titanium (2.4 MS/m [186]) may prove to be a prohibitive factor for its use in RF MEMS capacitive switches where low loss is a key design parameter. For these reasons, the development of an alternative material in the form of an aluminium-titanium (Al-Ti) alloy for MEMS applications is currently underway in

Tyndall National Institute. It is hoped that this alloy will retain the high conductivity of aluminium, while the inclusion of titanium will improve the mechanical stability of the material.

Previous work by Lee [178] on aluminium alloyed with 1.5% titanium has shown that titanium precipitates are formed along aluminium grain boundaries when these two materials are alloyed. These precipitates prevented the occurrence of grain boundary sliding and hence reduced the mechanical degradation of the metal. In this work an aluminium alloy of similar composition has been developed for use in MEMS switches. Fabrication details and the results of mechanical characterisation tests performed on these new devices are given in the following section. It will be shown that devices fabricated with the first generation Al-Ti alloy show superior mechanical performance to the previous aluminium and titanium switches.

4.4.1 Device Fabrication

The fabrication of RF MEMS capacitive switches incorporating the first generation of a new Al-Ti alloy follows the same process as described in Chapter 2 with the inclusion of two important differences. Firstly, the devices are now fabricated on high-resistivity silicon wafers with a 2 µm thick initial oxide deposited by PECVD. The thickness of the initial oxide has been increased to isolate the switch from the substrate material in an attempt to improve the RF performance and flatten the low-frequency C-V curve [187, 188]. Secondly, while the bottom electrode remains composed of aluminium with 1% silicon, an additional 50 nm thick titanium-nitride layer is sputtered on top to reduce the roughness of this electrode and hence improve the capacitance ratio of the device. Aside from these two changes, the remaining fabrication steps proceed as normal until the Al-Ti alloy is sputtered to form the movable membrane. The Al-Ti membrane is composed of 95% aluminium with 5% titanium and was cold-sputtered at an RF power of 1 kW to a thickness of approximately 1 µm.

4.4.2 Device Characterisation

The study of dielectric charging in these devices is the subject of later thesis chapters, while their mechanical characterisation by electrical means is described here. The typical C-V curve of an Al-Ti switch is shown in Figure 4.17. Despite the inclusion of the smoothening titanium-nitride layer, the rough bottom metal/dielectric interface results in a down-state capacitance of approximately 800 fF. As an initial test of mechanical reliability, Al-Ti switches were stressed using a ±25 V bipolar hold-down bias for 15 minutes in an

experiment which is identical to the bipolar characterisation presented in Figures 4.6 (a) and 4.8 (a).

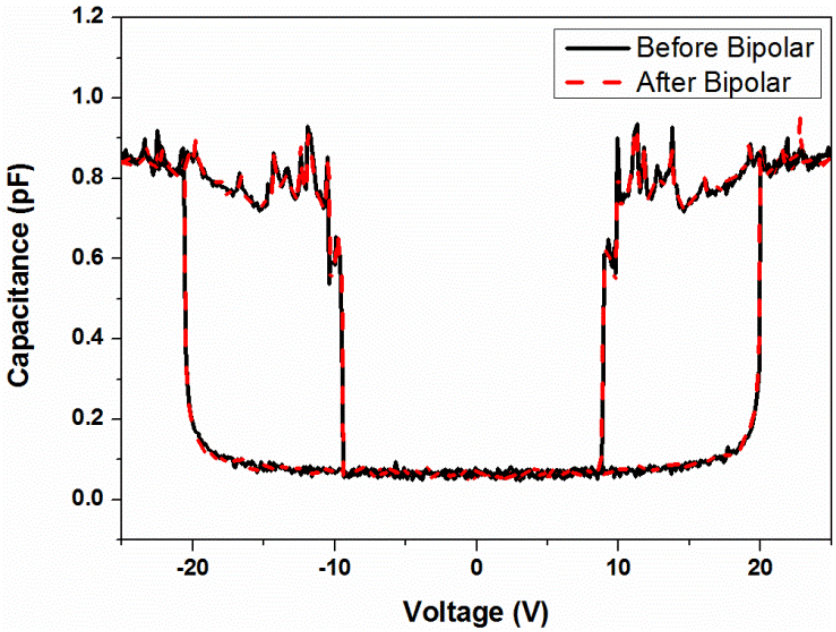

Figure 4.17: The C-V curves of a 100x100µm^2 Al-Ti switch measured before (black solid line) and after (red dashed line) 15 minutes bipolar hold-down stress at ±25 V.

No change in the pull-in or pull-out voltages was measured after 15 minutes of bipolar stress, demonstrating the superior mechanical performance of the Al-Ti alloy over switches made from pure aluminium or titanium. Similar experiments were performed at different temperatures to assess the mechanical reliability of the alloy over the device operational range. A similar switch was heated to 100°C and held in the down-state for one hour using a ±15 V bipolar bias. In this instance C-V narrowing of at most 0.2 V was observed, as shown in Figure 4.18.

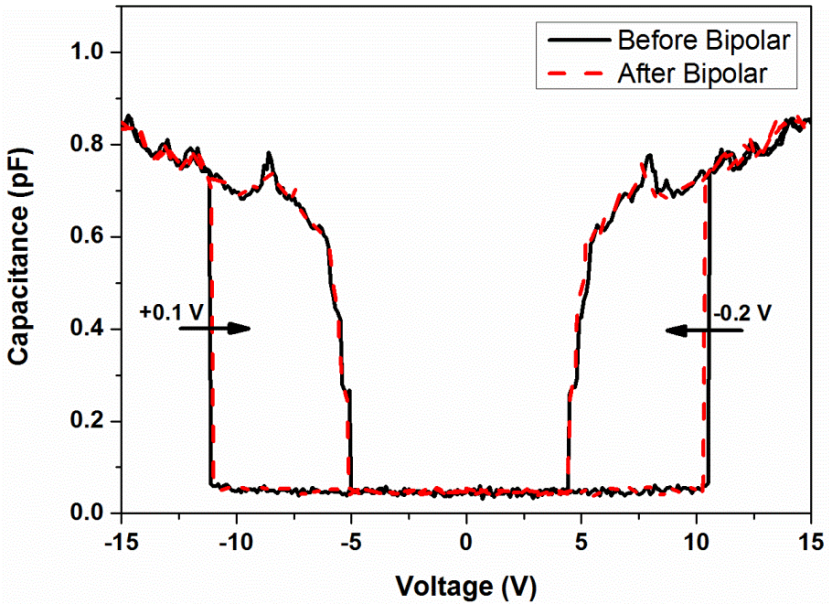

Figure 4.18: C-V curve of an Al-Ti switch showing 0.2 V of narrowing after 1 hour of mechanical stress at 100°C.

These results show that a mechanically robust material may be created by alloying aluminium with titanium. The sheet resistance of this layer was measured to be approximately 160 mΩ/sq, corresponding to a resistivity of 160 nΩ m. This value is lower than the resistivity of titanium (420 nΩ m) but is approximately six times higher than the resistivity of pure aluminium (27 nΩ m) [186]. Therefore, while the use of this alloy can improve the mechanical reliability of capacitive switches, it will lead to a trade-off in the performance of devices in terms of increased RF losses. Further development on the Al-Ti alloy is taking place in Tyndall National Institute to increase the conductivity of the material but maintain the improved mechanical properties that have been obtained.

Based on similar studies by Lee [178], it has been concluded that the increased mechanical reliability is caused by titanium precipitates which form along aluminium grain boundaries and prevent the occurrence of grain boundary sliding. As these devices are not susceptible to large amounts of mechanical degradation they are particularly suitable for the study of dielectric charging in RF MEMS capacitive switches. For this reason, capacitive switches fabricated using the new Al-Ti alloy will be used for the characterisation of dielectric charging in the following chapters.

4.5 SUMMARY

This chapter described the characterisation of mechanical degradation in RF MEMS capacitive switches. An electrical test method was introduced which minimized the effects of dielectric charging and allowed mechanical degradation to be studied in isolation. Capacitive switches fabricated using aluminium and titanium membranes were tested using this method and it was determined that mechanical degradation was the dominant degradation mechanism of aluminium switches. Aluminium switches were therefore used in conjunction with this method for the study of mechanical reliability.

The permanent ΔV_{PI} caused by the creep effect was identified by performing repeated actuation and recovery cycles on a switch. Once the creep effect had been saturated, the remaining time-dependent change in the pull-in voltage was used to identify the linear viscoelastic effect for the first time in RF MEMS capacitive switches. This was accomplished by fitting the data with a stretched exponential model derived from the generalised Maxwell theory of viscoelasticity and the same characteristic times for the stress and recovery cycles were calculated. Analysis of the temperature dependence of the viscoelastic effect allowed the activation energy of the process to be calculated. This was used to identify grain boundary sliding as the stress relaxation mechanism responsible for the viscoelastic behaviour measured in these devices.

Finally, it was determined that membranes made from pure aluminium were not suitable for use in RF MEMS capacitive switches due to the effects of mechanical degradation. A new aluminium-titanium alloy was then proposed as a more mechanically reliable material and is currently under development in Tyndall. Switches fabricated with a first generation of this alloy were characterised using the same methods applied to titanium and aluminium switches and did not exhibit significant mechanical degradation under the same stress conditions. This confirmed that the new Al-Ti alloy has removed the effects of mechanical degradation and suggests that devices fabricated using this alloy will be particularly suitable for an isolated study of dielectric charging in RF MEMS capacitive switches.

In the remainder of this thesis various experimental techniques and device architectures will be employed to isolate different dielectric charging mechanisms in capacitive switches fabricated using the new Al-Ti alloy. These charging mechanisms will be studied to develop an increased understanding of their causes and effects and quantify their influence on RF MEMS reliability.

CHAPTER 5:
DIELECTRIC CHARGING CHARACTERISATION

5.1 INTRODUCTION

As discussed in Chapter 3, RF MEMS capacitive switches suffer from multiple reliability concerns including mechanical degradation and dielectric charging. Attempting to study the degradation mechanisms responsible for these reliability concerns can be made difficult when they occur simultaneously and have a similar effect on the device C-V curve. In the previous chapter, a new experimental technique was described which allowed the effects of mechanical degradation to be isolated in RF MEMS capacitive switches. Following a study of these effects, a new aluminium-titanium alloy was investigated and was found to be mechanically robust. Therefore, switches fabricated using this alloy would be particularly suitable for an isolated study of dielectric charging mechanisms, as it can be assumed that any change in the device C-V curve will be the result of dielectric charging only.

The aim of this chapter is to isolate different dielectric charging mechanisms in RF MEMS capacitive switches and is organised as follows. Section 5.2 describes the preliminary results of dielectric charging experiments performed on Al-Ti capacitive switches. Two different types of dielectric charging are identified which affect the bulk and the surface of the dielectric, and an investigation of bulk dielectric charging is undertaken. Charging and discharging currents are measured on metal-insulator-metal devices to assess the dielectric charging mechanisms across metal/dielectric interfaces and details of these experiments are given in Section 5.3. Through these experiments it is found that border charging processes are responsible for the transient currents measured in MIM devices. Following this, a model is proposed which relates the measured currents to pull-in voltage changes in capacitive switches. The derivation of this model and its experimental validation are described in Section 5.4. Finally, this chapter concludes with a summary in Section 5.5.

5.2 PRELIMINARY CHARGING CHARACTERISATION

As described in the introduction to this chapter, an isolated investigation of dielectric charging in RF MEMS can now be performed by studying the degradation of capacitive switches which are fabricated using the new Al-Ti alloy. Since these switches have been shown to be mechanically robust, DC biases can be used to electrically stress the device while any resulting C-V shift or narrowing can be assumed to be the product of dielectric charging only. As a first step in the characterisation of dielectric charging, the transient pull-in voltage shift of Al-Ti capacitive switches was monitored in response to various applied DC biases. A lower limit of 15 V was set as the minimum stress voltage as this was sufficient to actuate the majority of the switches. An upper limit of 45 V was set as the maximum stress voltage because above this level the switches became stuck in the down-state during the stress period and no data could be obtained from subsequent C-V measurements. One such result is shown in Figure 5.1 where a device no longer opened after 30 minutes of stress at -45 V. This is an example of the stiction failure mechanism described in Chapter 3.

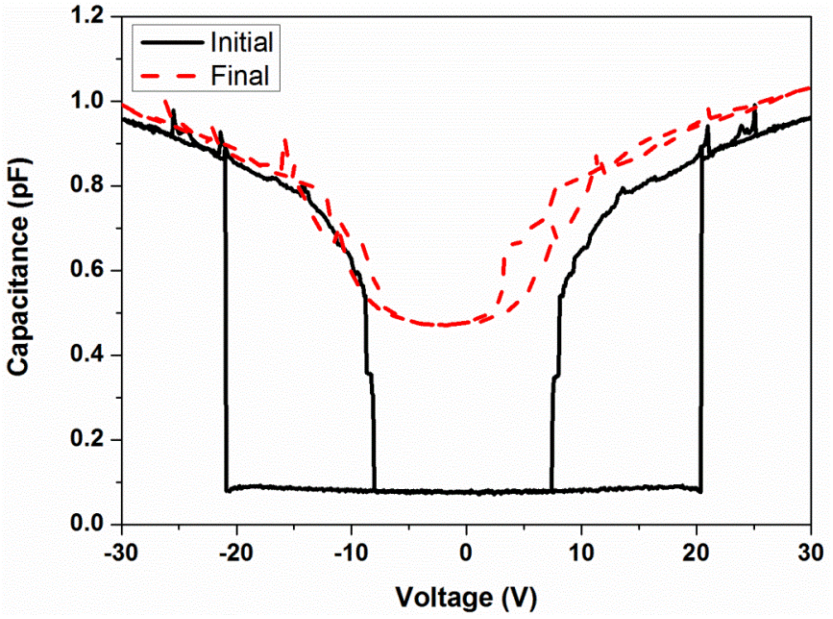

Figure 5.1: C-V curves before (solid black line) and after (dashed red line) -45 V had been applied to an Al-Ti device for 30 minutes. The failure of the switch to re-open has been attributed to dielectric charging.

DC stress biases of both polarities were applied to the bottom electrode of the capacitive switches while periodic C-V sweeps were used to monitor any changes in the pull-in voltage. After 30 minutes of stress the DC bias was removed and the same series of C-V sweeps were used to monitor the recovery of dielectric charge. The results of these tests are shown in Figure 5.2.

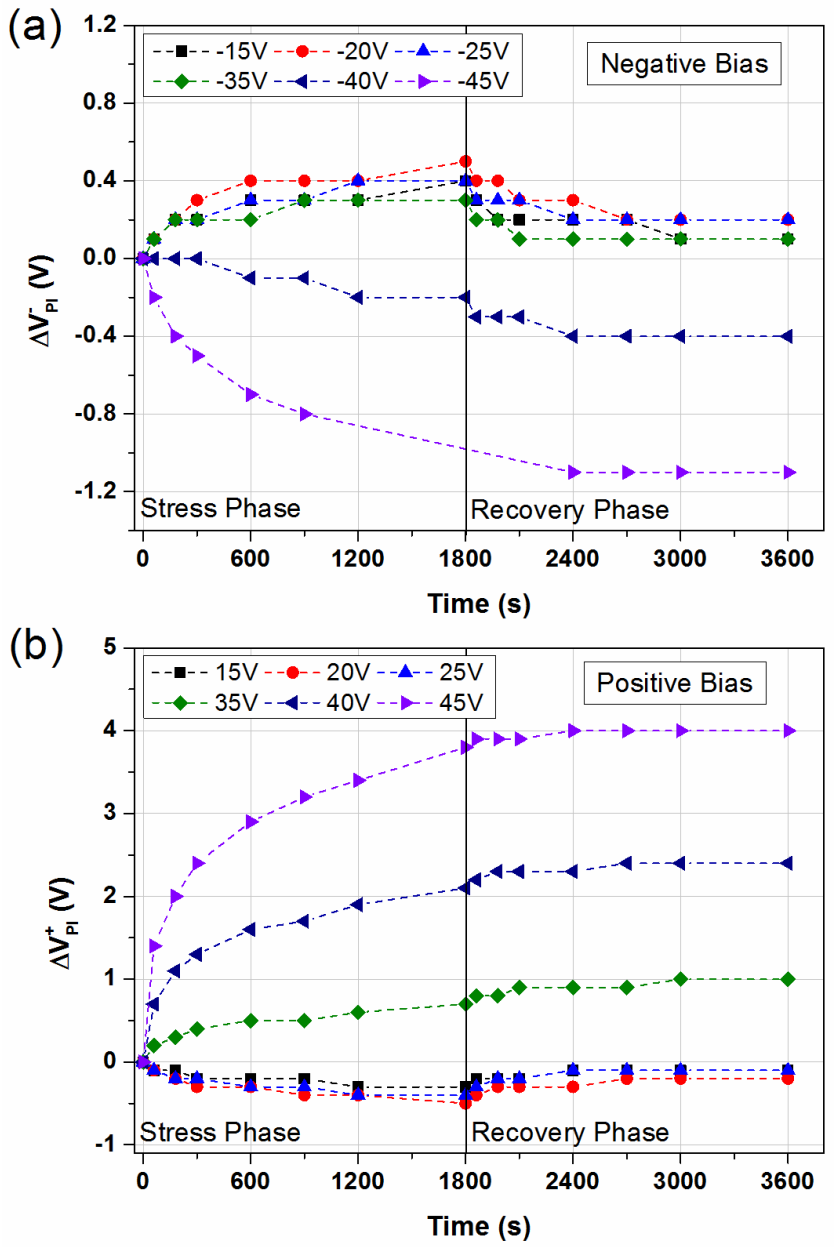

Figure 5.2: C-V shifts measured on Al-Ti switches under different negative (a) and positive (b) DC biases.

Two completely different charging responses can be identified by studying the C-V shifts in Figure 5.2 (a) and (b). In every case a DC bias caused a shift of the C-V curve; however, the direction of the shift changed as the bias magnitude was increased. In Figure 5.2 (a) negative biases in the range of -15 V to -35 V caused a right-shift of the C-V curve. This same behaviour was observed on titanium switches in Chapter 4 and corresponds with negative charging of the dielectric. However, a left-shift of the C-V curve was measured when the stress bias was increased to -40 V and -45 V. For a bias applied to the bottom metal, this kind of shift indicates that positive dielectric charging has taken place.

The opposite behaviour was seen to occur in Figure 5.2 (b) for devices stressed using positive DC biases. Stress voltages in the range of +15 V to +25 V caused a left-shift of the C-V curve indicating that positive dielectric charging had taken place, while higher voltage magnitudes caused a right-shift of the C-V curve indicating that negative dielectric charge was present. Therefore the primary difference between the two charging responses is:

- Lower voltages cause net dielectric charging of the same polarity as the stress bias.
- Higher voltages cause net dielectric charging of the opposite polarity as the stress bias.

Note that the stress bias was applied to the bottom electrode in each case. Additionally, for either stress polarity the magnitude of the C-V shift was greatly increased once the direction of shift was reversed. The shift magnitude after 30 minutes stress at -45 V could not be measured as the device was temporarily stuck in the down-state between 1200 and 2100 seconds.

A second difference between these two charging behaviours may be observed by monitoring the recovery of the C-V shift. The dielectric charge created under lower voltage conditions was reversible in time. This can be seen in Figure 5.2 (a) and (b) where the C-V shifts after low-voltage stress decreased to approximately 0.1 V after 30 minutes of recovery. While it is not shown here, the switches returned to their initial condition after several hours at zero bias. However, the dielectric charge created under higher voltage conditions did not recover during the measurement time; the V_{PI} shift continued to increase even after the DC bias had been removed. After several minutes a steady-state condition was reached where the C-V curve did not shift any more. This is seen to be true for both voltage polarities in Figure 5.2 (a) and (b). Therefore the second difference between the two charging responses is:

- Lower voltages cause dielectric charging which is reversible in the same time scale as the stress time.
- Higher voltages cause dielectric charging which does not recover in the same time period as the stress time.

This type of charging behaviour was previously reported by Peng who associated these properties with the effects of charge located at the bottom and top of the intermetal dielectric layer [120]. According to his theory, when a bias is applied to a switch charge is injected from the bottom electrode into the dielectric and remains near the vicinity of the

bottom metal/dielectric interface. In a similar fashion, charge can be injected from the moveable membrane into the top surface of the dielectric and remains trapped near the dielectric/air/metal interface. Once the voltage is removed and the membrane returns to the up-state, charge near the bottom metal/dielectric interface is removed by tunneling to the bottom metal. This happens over a similar time scale as the charging time and thus, bottom (or bulk) charging is recoverable. However, charge which is injected at the top surface remains trapped near the air interface once the top metal is removed. Therefore, this charge must traverse the dielectric thickness under the influence of an internal electric field before it can be discharged through the bottom metal. As such, the discharging time of this type of top (or surface) charge is considerably longer than bulk charge and may not disappear within a conveniently observable time [47]. Further studies have found that surface charging takes place at higher voltages than bulk charging and is dependent on the atmospheric conditions to which a device is exposed [47, 49, 51, 55]. Additionally, owing to the location of surface charge at the top of the dielectric layer, the shift effect of surface charging is considerably greater than the effect of bulk charge, as discussed in Section 3.2.1.

Given the clear distinction between the effects of bulk and surface charging in RF MEMS capacitive switches, it is convenient at this point to divide the work of characterising and understanding their respective charging mechanisms into two chapters which focus on them separately. An investigation into surface charging at higher electric fields is the subject of Chapter 6, while this chapter is focussed on understanding the dielectric charging behaviour of RF MEMS capacitive switches which are stressed using lower electric fields.

5.3 BULK CHARGING CHARACTERISATION AT LOW ELECTRIC FIELDS

Low electric fields are defined as voltage levels where the effects of surface dielectric charging have not been observed within the time frame of the previous stress and recovery experiments. Referring to Figure 5.2, it can be seen that the effects of surface charge are observed during positive DC stress at bias levels of +35 V and above and during negative DC stress at bias levels of -40 V and above. Therefore, to isolate bulk dielectric charging the maximum voltage used during these experiments was set below these levels. The maximum electric field applied to devices during this investigation was 2.5 MV/cm. For a dielectric thickness of 130 nm which is typical of devices used in this work, this electric field level corresponds to a maximum applied voltage of 32.5 V. Additionally, Figure 5.2 shows that bulk dielectric charging recovers quickly once the stress bias has been removed.

Therefore, this degradation mechanism may be adversely affected by pauses during a stress measurement in a similar fashion to the rapid recovery of mechanical degradation reported in Chapter 4. To avoid this, single-polarity C-V sweeps were used to characterise bulk dielectric charging. Moreover, C-V sweeps of the same polarity as the stress bias were used to preserve the same voltage polarity applied across the dielectric at all times.

A first step into this investigation is shown in Figure 5.3 where the ΔV_{PI} of a capacitive switch is shown under three different electrical stress conditions. The same switch was used in each case but was allowed to completely recover before subsequent tests were performed. In this experiment low-field DC biases of +15 V and -15 V and a bipolar hold-down signal of ±20 V were applied for one hour while any change in the pull-in voltage was measured using periodic C-V sweeps. After 60 minutes the bias was removed and the recovery of the device was also measured. Positive pull-in voltages were measured during positive stress while negative pull-in voltages were measured during negative stress to maintain the same stress polarity across the dielectric at all times. Only positive C-V sweeps were used to monitor the ΔV_{PI} during bipolar stress.

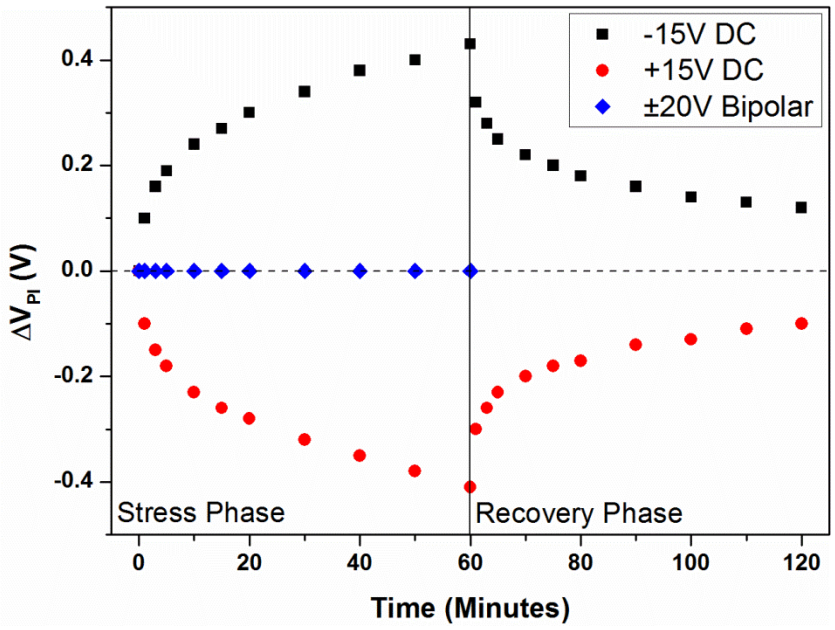

Figure 5.3: Measured pull-in voltage change of a capacitive switch undergoing three different electrical stress tests. Opposite and symmetric C-V shifts are observed for +15 V and -15 V and no change in V_{PI} is observed for ±20 V bipolar bias.

No change in the pull-in voltage was measured over one hour of bipolar stress, confirming that these devices are not subject to mechanical degradation. In the absence of mechanical degradation, C-V shifts of equal magnitude and opposite direction were observed under DC

biases of equal magnitude and opposite polarity. This result is the first experimental evidence of the exact symmetry of positive and negative dielectric charging and discharging processes at low electric fields in RF MEMS capacitive switches which have been proven to be mechanically robust.

Following this, transient current measurements were performed in an attempt to gain more insight into the charging and conduction properties of the dielectric layer. The transient charging currents of the switch were measured while a constant DC bias greater than the pull-in voltage was applied to the bottom electrode. DC biases of +15 V and -15 V were used to charge the dielectric, while ample time was given between each measurement to allow the switch to recover fully. The results of this experiment are shown in Figure 5.4.

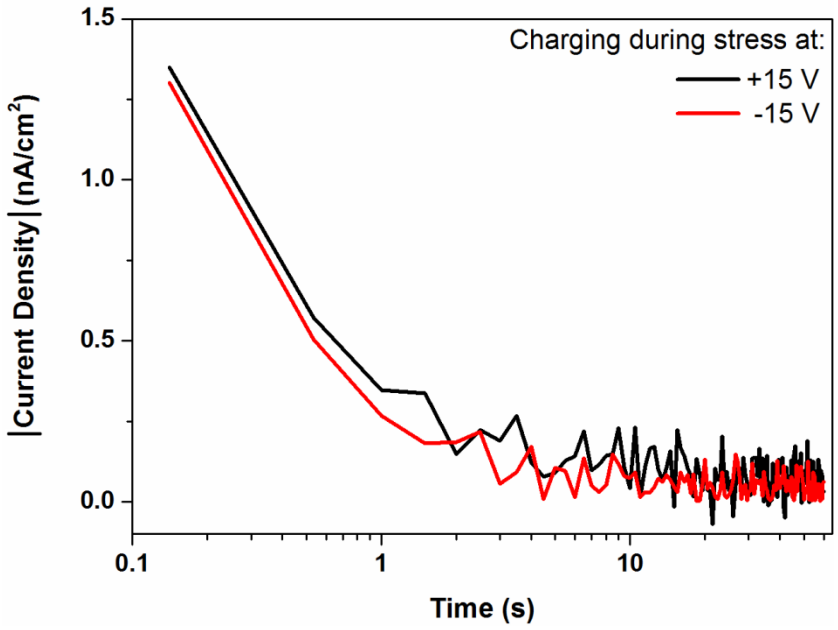

Figure 5.4: Transient charging currents measured at +15 V (black) and -15 V (red) on a MEMS capacitive switch.

Figure 5.4 shows that transient charging currents were measurable on MEMS capacitive switches over short time scales; however, these currents decayed to noise levels in approximately 10 seconds. The polarity-independence of the charging process is evident from Figure 5.4 as the data for positive and negative polarities are approximately overlaid. The symmetric charging currents display the same trend as the symmetric C-V shifts observed after DC stress in Figure 5.3, which suggests that whatever physical mechanism is causing the transient currents is likely to be responsible for the observed pull-in voltage shifts. Discharging currents could not be measured on capacitive switches once the bias

was removed and the membrane returned to the up-state. Therefore, to enable discharging currents to be measured the experiment was repeated on MIM devices which were fabricated on a separate wafer using a similar process to the MEMS switches. However, the MIM devices were fabricated with an aluminium top metal and without a TiN layer on top of the bottom electrode. DC biases of +15 V and -15 V were again used to charge the dielectric and the measured charging and discharging currents are shown in Figure 5.5.

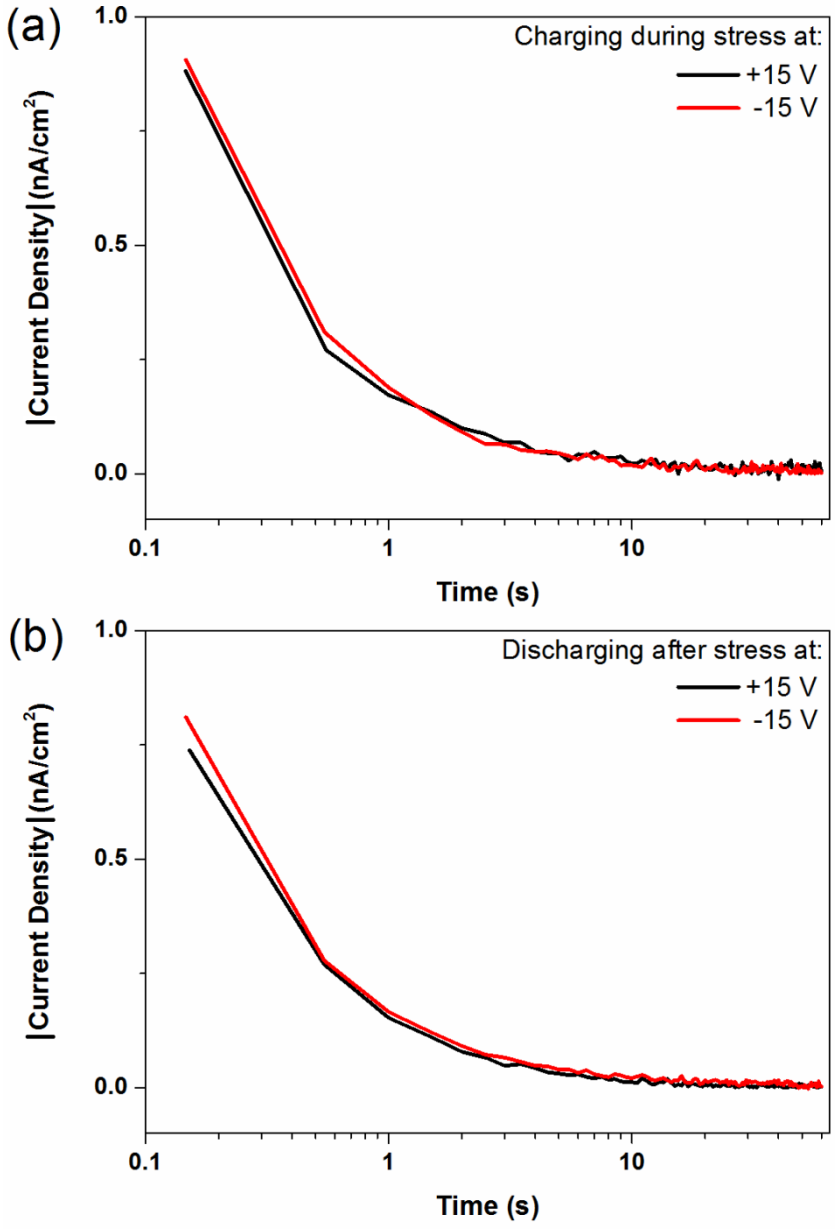

Figure 5.5: The transient charging (a) and discharging (b) current densities measured on MIM devices at +15 V (black) and -15 V (red).

Transient charging and discharging currents were measurable on MIM devices and in each case these currents decayed to noise levels over the duration of the experiment. The bias polarity-independence of the MIM charging and discharging processes can be seen in Figure 5.5 where the currents are overlaid in both (a) and (b). The fact that a similar polarity-independent transient charging process was measured on MIM and MEMS devices indicates that the same process is responsible for the transient currents measured in each case. Additionally, the presence of a polarity-independent discharging current in MIM devices suggests that a similar mechanism may be present in MEMS switches, even if it cannot be measured. In particular, the presence of such a mechanism could explain the transient and symmetric ΔV_{PI} recovery observed after DC stress in Figure 5.3. Therefore, a correlation may exist between the symmetric charging and discharging currents observed on MIM devices and the ΔV_{PI} observed on MEMS capacitive switches. Thus, the characterisation of these transient charging and discharging currents may allow us to identify the physical process of bulk dielectric charging in RF MEMS capacitive switches. However, because transient discharging currents cannot be measured on MEMS switches, MIM devices will be used for the characterisation of this process.

5.3.1 Current Transients in MIM Devices

The voltage dependence of the transient charging and discharging process was investigated in MIM devices by charging the dielectric using several electric fields in the range of 0.2-1.2 MV/cm. Charging currents were measured for DC biases of both polarities and all biases were applied to the top metal of the device for 5 minutes. At the end of the stress time the bias was removed and the discharging currents were recorded for another 5 minutes. The measured charging and discharging current densities are plotted on a log-log scale in Figure 5.6 (a) and (b), respectively.

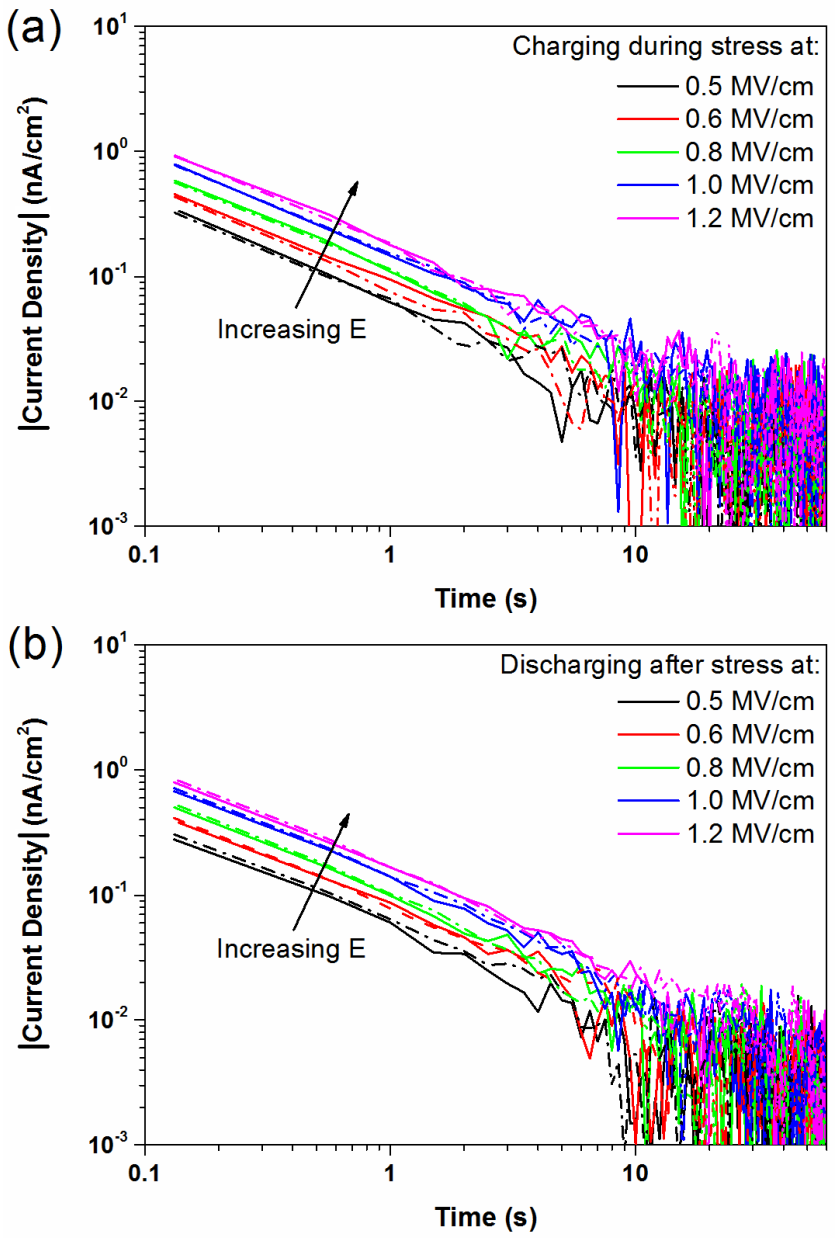

Figure 5.6: Charging current densities (a) and discharging current densities (b) measured on a typical MIM device over a range of electric field levels. Solid lines correspond to positive bias, while negative biases are represented by dash-dot lines.

The transient charging and discharging currents were observed to increase in magnitude with the applied bias. However, the polarity-independence of the process did not change as the data for positive and negative biases were approximately overlaid at each electric field level. Additionally, the same time-dependence of the charging and discharging process was observed in each case as the measured currents followed an identical decaying trend over time. This can be seen in Figure 5.6 where the charging and discharging currents form approximately parallel lines when plotted on a log-log scale.

The temperature-dependence of the charging process was also investigated by varying the temperature of the experiment while stressing a MIM device with a constant positive electric field of 1.5 MV/cm. As before, charging and discharging currents were measured over the course of the experiment and these results are shown in Figure 5.7 (a) and (b), respectively.

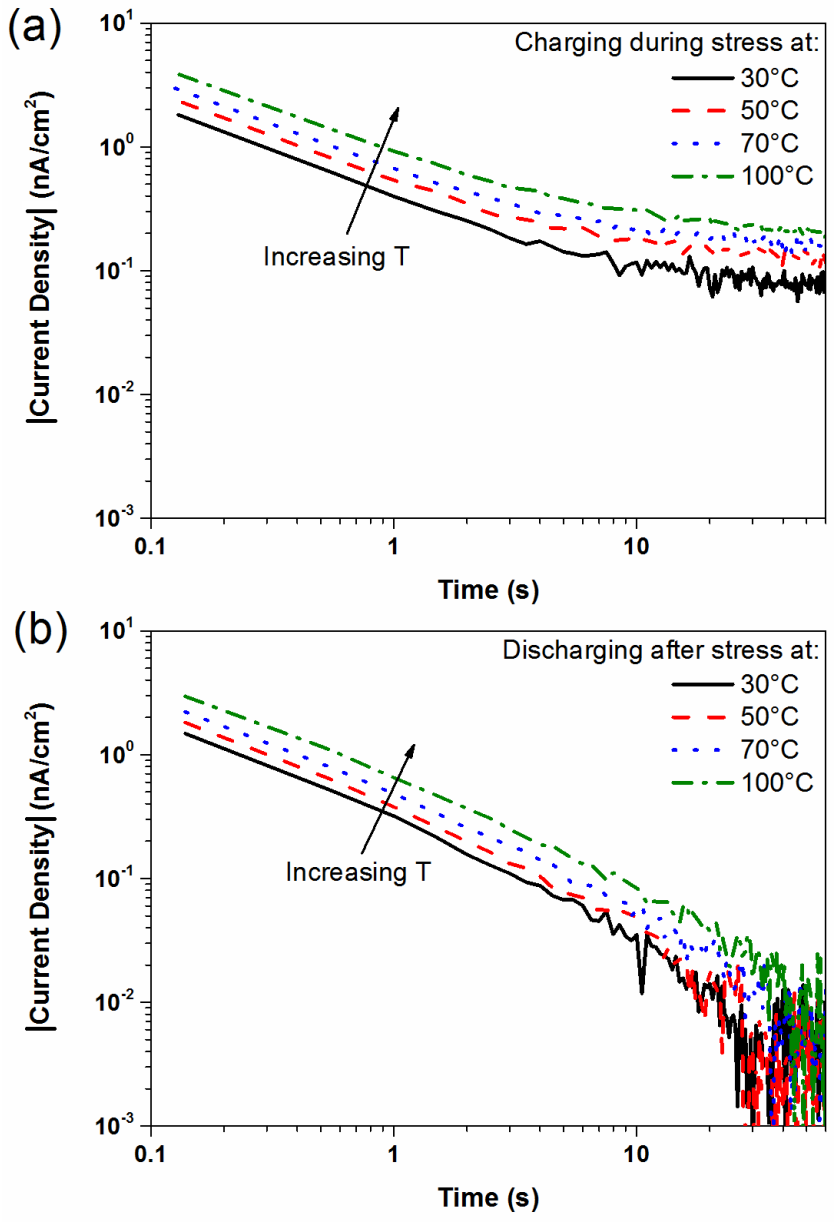

Figure 5.7: Charging current densities (a) and discharging current densities (b) measured on a typical MIM device over a range of temperatures. A constant positive electric field of 1.5 MV/cm was used to charge the device in each case.

In Figure 5.7 it can be seen that both the charging and discharging currents increased with temperature. The charging currents did not completely decay during the measurement time which suggests that an additional temperature-accelerated conduction mechanism may have contributed to the measurement results. However, the discharging currents followed the same decaying trend observed in Figure 5.6 which indicates that the same discharging process was active at all voltages and temperatures studied. Therefore, because conduction currents may have been measured together with transient charging currents, it was decided to use the discharging current transient (DCT) data to characterise the physical process of bulk dielectric charging.

Further information on the discharging process was gained by fitting the DCT data with an appropriate model and observing how the parameters changed over voltage and temperature. Exponential functions are commonly used in the literature to fit the DCTs measured on MIM and MEMS devices [25, 26, 116, 118, 119, 133, 146, 147, 189]; however, it was found that the DCT data obtained from devices in this work could be accurately modelled using a power-law function of the form

$$I(t) = I_0 t^{-m}, \tag{5.1}$$

where I_0 is the peak current at the beginning of the measurement and the time dependence of the current decay is determined by the value of the exponent m. This value can be obtained from the slope of a straight line fit to the data when it is plotted on a log-log scale. Linear fitting was performed on the logarithmic data of Figures 5.6 (b) and 5.7 (b) and an average exponent m = 0.89 was extracted across all measurements. This value was observed to be approximately constant as a function of electric field strength and temperature, while the peak current increased approximately linearly with the electric field strength and followed an exponential relation over temperature. An Arrhenius plot was constructed from the peak current values over temperature and this is shown in Figure 5.8. Straight line fitting to the Arrhenius data allowed the activation energy of the process E_A = 0.11 eV to be calculated.

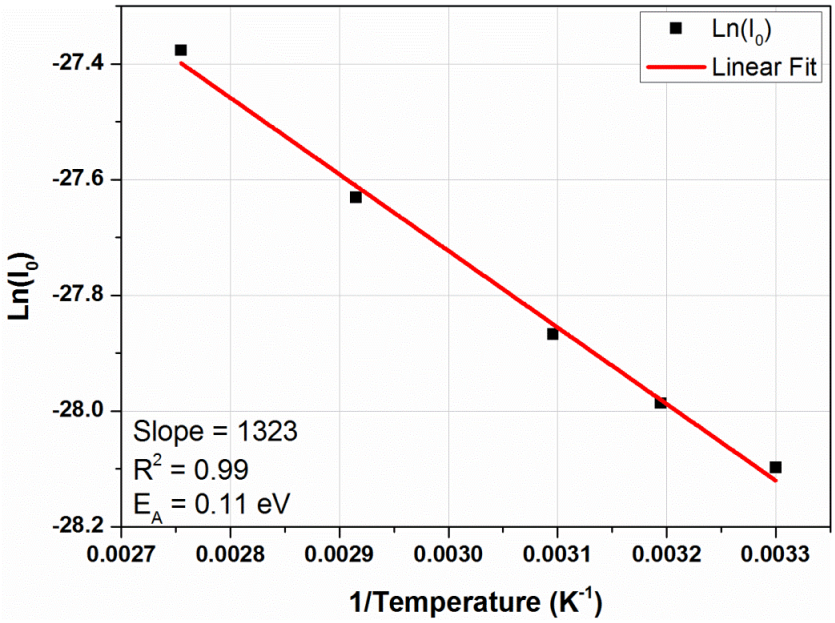

Figure 5.8: Arrhenius plot of the extracted peak currents from linear fitting to MIM DCT data. The extracted activation energy and fitting parameters are indicated on the graph.

A similar power-law model with exponent ≈ 1 has been used to describe the transient stress-induced leakage current (SILC) observed in MOS and flash memory devices [190, 191]. The leakage current caused by the SILC effect has been attributed to a trap-assisted-tunneling process through very thin dielectric films [192]. However, such a process cannot account for the charging and discharging of thicker oxides (> 100 Å) where the transient charging and discharging currents were observed to decay to noise levels over time with a similar power law dependence as was observed in Figures 5.6 and 5.7 [190, 193]. Instead, this behaviour was attributed to the filling and emptying of amphoteric border traps which are located within several nm of the silicon-oxide and metal-oxide interfaces [190, 191, 193-197]. Amphoteric traps are caused by electrically active dangling bonds which, depending on their occupancy can be neutral, positively or negatively charged [198]. The filling and emptying of these border traps has been successfully described using the tunnelling front model [191, 199, 200] which was created to account for the correlation between the transient shift of threshold voltages and the transient discharging currents in MOS devices following the removal of a bias voltage [201, 202]. A similar model for MIM devices is shown in Figure 5.9 and shows that the traps with the highest tunneling probability – those closest to the oxide interface – are charged first. Note that an equivalent charging process of the opposite polarity may simultaneously take place at the other metal/dielectric interface [203] but for simplicity only electron injection at the right-hand interface is shown.

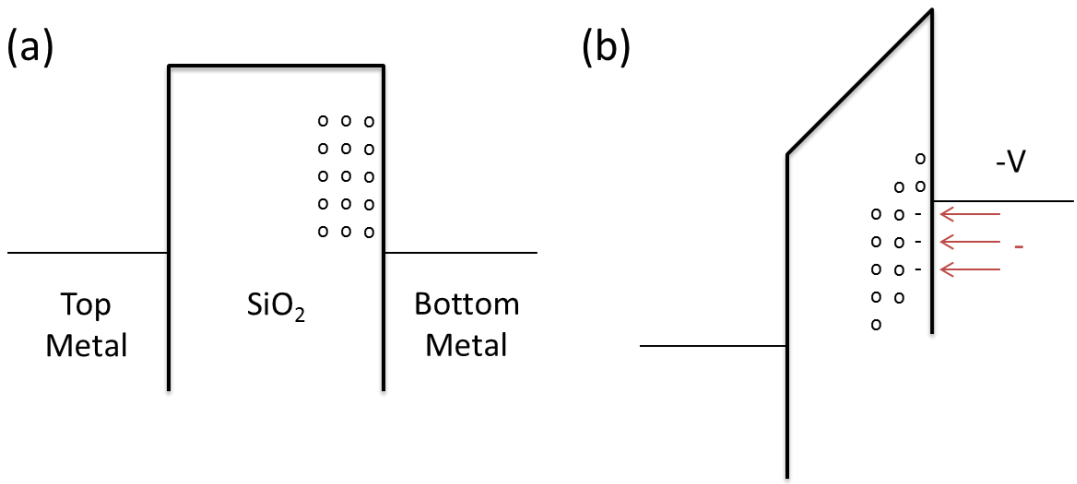

Figure 5.9: Uncharged traps (o) at the interface between a metal and dielectric under zero bias (a). These traps become filled (-) when a negative bias is applied to the bottom metal and they fall below the Fermi level of the adjacent metal (b).

Following this, charge may move deeper into the oxide due to a trap-assisted-tunneling process [192, 204] as shown in Figure 5.10. The transient behaviour of the charging current is caused by the exponential fall-off of the quantum mechanical tunnelling probability of an electron with distance into the oxide [199]. This general feature of direct tunnelling is responsible for the logarithmic time-dependence of the charging process which approximates 1/t when plotted on a log scale [205, 206]. Deviations from this 1/t behaviour can be attributed to localised band-bending as trap sites are filled or emptied, and can also be due to a non-uniform distribution of trap sites within the dielectric [191, 199]. Once the bias is removed, a similar trap-assisted tunneling process governs the discharging of the dielectric [191, 207] as shown in Figure 5.11.

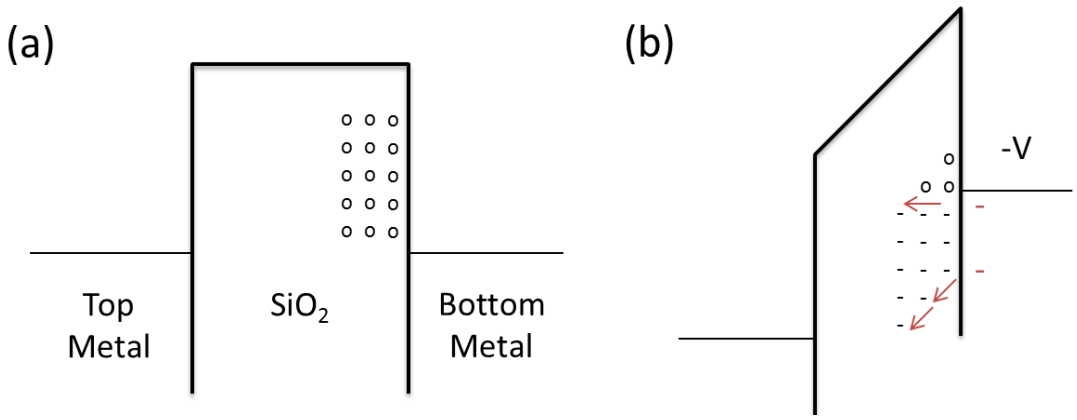

Figure 5.10: Uncharged interface traps (o) and near-interface, or border traps, in a MIM structure under zero bias (a). The border traps become filled (-) via a trap-assisted-tunneling process when a negative bias is applied to the bottom metal (b).

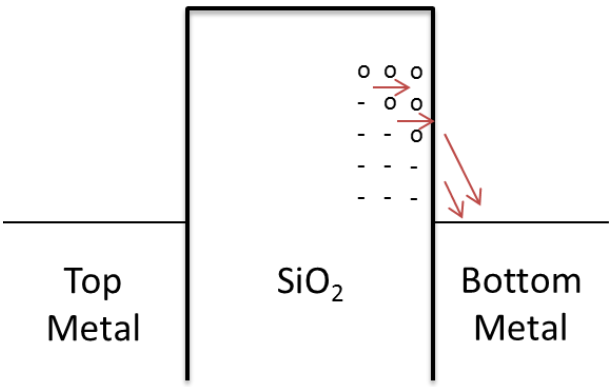

Figure 5.11: Trap-assisted discharging of the filled border traps (x) under zero-bias conditions.

Studies have shown that the charging and discharging currents caused by the SILC effect are approximately equal with bias polarity [207] and are accelerated by field and temperature with an activation energy of approximately 0.1 eV [190, 208]. Given the similarities observed between the experimental data contained in this section and the transient SILC effect reported in the literature, it is believed that a similar process is responsible for the transient charging and discharging currents measured on MIM devices in Figures 5.6 and 5.7. Since the same oxide deposition process was used to fabricate the MIM and MEMS devices investigated in this work, it is hypothesised that the transient SILC effect is also responsible for the symmetric and polarity-independent charging behaviour observed on MEMS switches at low electric fields. To verify this, a simple analytical model is proposed which uses established SILC theory to explain the transient ΔV_{PI} measured on MEMS devices. Details of the derivation and experimental verification of this model are provided in the following section.

5.4 MODELLING THE TRANSIENT SILC EFFECT IN RF MEMS CAPACITIVE SWITCHES

5.4.1 Model Derivation

In this section a simple 1D model is proposed to explain the symmetric and reversible nature of bulk dielectric charging in RF MEMS capacitive switches. Based on transient SILC theory, it is assumed that all of the trapped charge is located in close proximity to the bottom metal/dielectric interface of the capacitive switch [193, 195, 196, 209]. Additionally, it is assumed that a spatial distribution of border traps exists within the dielectric but that this can be approximated by a uniform sheet of charge. This is justified by the approximate 1/t behaviour observed in the charging and discharging currents of the

PECVD oxide used in this work, which correlates with a uniform distribution of traps in the dielectric [191, 199] as discussed in the previous section. By modelling the trapped charge $Q_{Trapped}$ as a uniform charge sheet with centroid located at a position z inside the oxide, the charge distribution of an ideal capacitive switch in the down-state can be drawn schematically as in Figure 5.12.

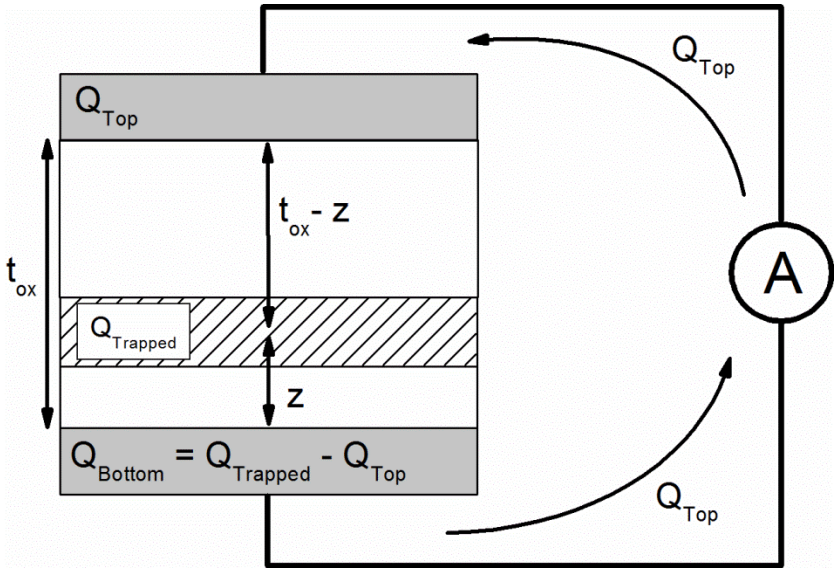

Figure 5.12: Model of the charge distribution on an ideal capacitive switch in the down state.

In this situation the trapped charge density has induced charges on the top and bottom electrodes so that the capacitor is electrically neutral,

$$Q_{Trapped} = -\left(Q_{Top} + Q_{Bottom}\right). \tag{5.2}$$

The electric field between the capacitor plates is divided between the regions above and below the trapped charge, and using Gauss' Law it can be shown [210] that the induced charge on the top electrode Q_{Top} is related to the amount of trapped charge by

$$Q_{Top} = -\frac{z}{t_{ox}} Q_{Trapped}, \tag{5.3}$$

where t_{ox} is the distance between the two capacitor plates. When a bias is applied to close the switch and charging occurs, the majority of charge tunnels from the bottom electrode into the dielectric to form a charge layer at a depth z.

The charge which is induced on the top electrode must therefore be supplied by the external circuit such that

$$I_{meas} = \frac{d}{dt} Q_{Top} = -\frac{z}{t_{ox}} \frac{d}{dt} Q_{Trapped}. \tag{5.4}$$

This current is the measured charging current flowing through the circuit. During the discharging phase when the membrane has returned to the up-state the effective capacitor thickness has increased to $t_{ox} + \varepsilon_d t_{air}$. According to equation (5.3), this increase in effective capacitor thickness will significantly reduce the induced charge on the top electrode and therefore explains why discharging currents are not measurable on capacitive switches in the up-state.

In Chapter 3, a uniform distribution of dielectric charge was shown to shift the pull-in voltage of a capacitive switch by an amount proportional to the density and location of the charge inside the dielectric,

$$\left|\Delta V_{PI}\right| = \frac{\sigma_p z}{\varepsilon_0 \varepsilon_r}. \tag{5.5}$$

By rearranging this equation and providing an initial estimate for the location of the charge centroid z, the amount of trapped charge in the oxide can be obtained from the expression

$$Q_{Trapped} = \frac{\varepsilon_0 \varepsilon_r A}{z} \Delta V_{PI}, \tag{5.6}$$

since the charge density $\sigma_p = \frac{Q_{Trapped}}{A}$, where A is the area of the dielectric. Combining equations (5.4) and (5.6) results in an expression which can be used to calculate the charging current in a capacitive switch based on the measured ΔV_{PI}

$$I_{meas} = -\frac{\varepsilon_0 \varepsilon_r A}{t_{ox}} \frac{d}{dt} \Delta V_{PI} = -C_{ox} \frac{d}{dt} \Delta V_{PI}. \tag{5.7}$$

In this way, even though the magnitude of the charging current may drop below the sensitivity of the measurement equipment, equation (5.7) can be used to calculate the amount of charging taking place so long as the pull-in voltage continues to change. Note that equation (5.7) is independent of the position of the charge centroid and the remaining physical constants equate to the oxide capacitance C_{ox}.

5.4.2 Model Verification

To test the applicability of the model, a capacitive switch was charged for one hour using a negative DC bias while the ΔV_{PI} was periodically recorded using C-V sweeps. The bias was applied at the bottom electrode and various electric fields in the range of 1-2.5 MV/cm were applied across the dielectric to ensure device actuation but maintain the stress in the low-field regime. The measured ΔV_{PI} values were converted into currents using equation (5.7). Charging currents at the bottom electrode were also recorded during the first 10 seconds of stress until the noise floor of the measurement equipment was reached. The measured and calculated charging currents are shown in Figure 5.13. A straight line fit has been included on the graph to verify that the two sets of data can be related using a single power law.

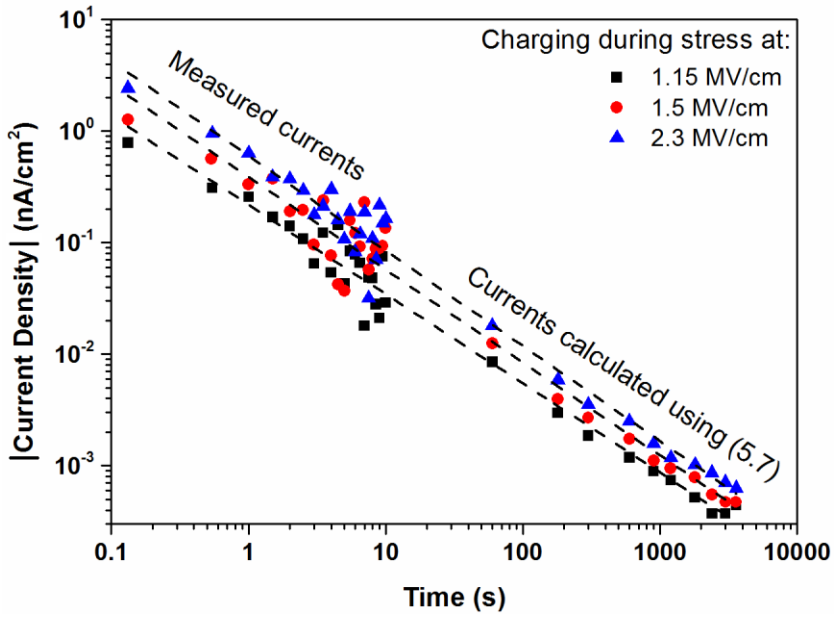

Figure 5.13: Measured and calculated charging current densities for negative electric fields in the range of 1-2.5 MV/cm recorded on a capacitive switch. The dashed lines correspond to linear fitting across each data set.

The agreement between the measured currents and the model (5.7) establishes that charge exchange at the bottom metal/dielectric interface is responsible for the charging currents and the ΔV_{PI} measured on these capacitive switches. Furthermore, it can be concluded that any charging which may be taking place at the top metal/dielectric interface is insignificant in this bias regime. To further confirm that the ΔV_{PI} and charging currents are due to the transient SILC mechanism, the model was tested over a range of temperatures and this data is shown in Figure 5.14. A maximum temperature of 55°C was

chosen to accelerate dielectric charging but minimise any potential mechanical degradation effects which are accelerated by temperature [97].

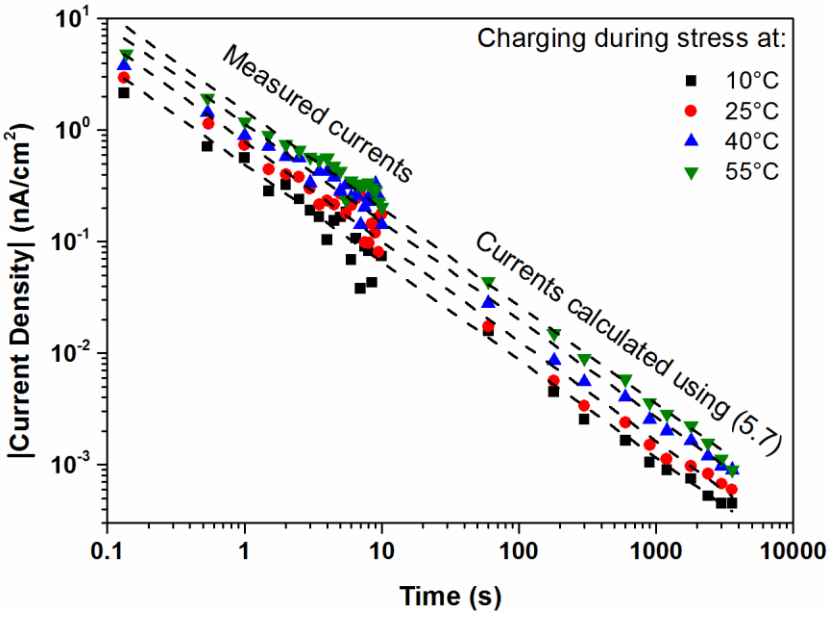

Figure 5.14: Measured and calculated MEMS charging current densities recorded over a range of temperatures at a constant electric field of -2.3 MV/cm. The dashed lines correspond to linear fitting across each data set.

The measured and calculated current densities are observed to increase with temperature while a straight line fit can be used to relate both sets of data over all temperatures investigated. The MEMS charging currents exhibit similar behaviour to MIM devices over field and temperature and can also be described by a power law process with an average exponent m = 0.86. This value was observed to be approximately constant as a function of electric field strength and temperature. The difference between this value and the exponent obtained on MIM devices may be due to the fact that DCTs were used to characterise the border trapping process in MIM devices while charging currents were measured on RF MEMS capacitive switches. Therefore, it is possible that a temperature-accelerated conduction mechanism may have affected the MEMS results. However, the fact that the measured and calculated charging current densities agree over all voltages and temperatures shows that dielectric charging due to current conduction has not affected the capacitive switches and the degradation mechanism of bulk dielectric charging has indeed been isolated by the measurement method.

The measured peak current values increased approximately linearly with the electric field strength and followed an Arrhenius relation over temperature. The Arrhenius plot for capacitive switches is shown in Figure 5.15 where an activation energy of 0.14 eV was extracted. This value also differs from the activation energy calculated on MIM devices which may be due to the necessary use of charging currents to characterise MEMS switches. However, both values are in close agreement with reported values of approximately 0.1 eV for the activation energy of border trapping processes [190, 208] which confirms that the charging and discharging of border traps is responsible for the transient and recoverable ΔV_{PI} measured on RF MEMS capacitive switches under low electric field stress. These results are the first experimental evidence of dielectric charging due to border trapping processes in RF MEMS capacitive switches.

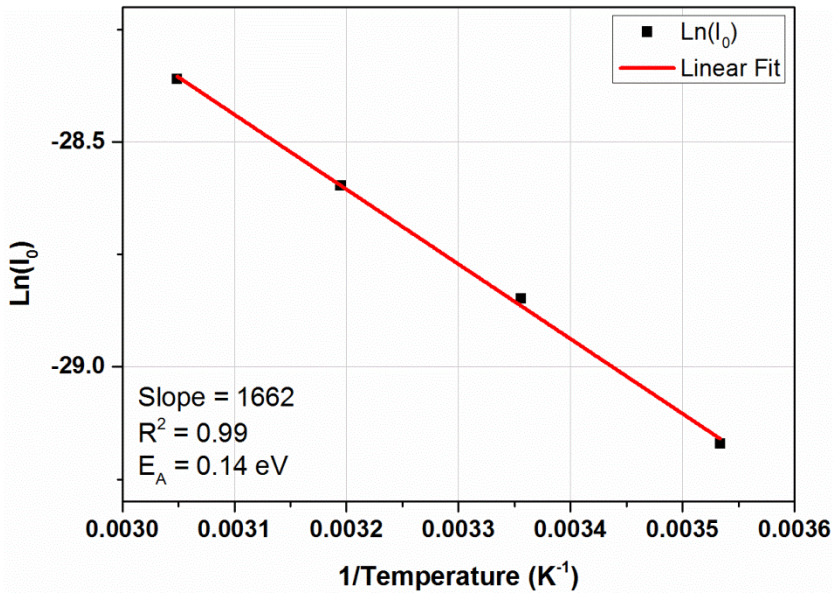

Figure 5.15: Arrhenius plot generated using peak charging current values obtained on MEMS capacitive switches. The calculated activation energy and fitting parameters are indicated on the graph.

Previous transient SILC experiments on MOS devices have demonstrated power-law charging and discharging processes with exponents which are independent of the charging bias magnitude and polarity [207] but which depend on the trap distribution inside the dielectric [191]. For instance, it was shown that the exponent changes after a high-field (>5 MV/cm) stress which causes additional traps to be generated inside the dielectric [194]. Given that the electric fields applied to devices in this work are limited to 2.5 MV/cm and that repeated measurements on MEMS and MIM devices have shown little change in the charging and discharging exponent with bias, polarity or temperature, it can be concluded that no new traps are being generated in the dielectric for this range of electric fields [207].

5.5 SUMMARY

This chapter has described the characterisation of dielectric charging effects in RF MEMS capacitive switches which are biased using low electric fields. An initial investigation on capacitive switches revealed the presence of two distinctly different charging mechanisms which were proposed to affect the bulk and surface of the dielectric, respectively. An investigation into low-field bulk dielectric charging mechanisms was undertaken on MIM devices by studying their transient charging and discharging currents. Using this approach the symmetric and reversible nature of bulk dielectric charging was reported for the first time.

Further investigations into the transient charging and discharging currents of MIM devices revealed the presence of a charging mechanism whose properties were the same as the stress-induced leakage current known from MOS technology. The voltage and temperature dependence of this mechanism lead to the identification of the charging and discharging of border traps as the physical process responsible for the transient currents measured on MIM devices. Following this, a model was created based on SILC theory which allowed the transient charging currents measured on RF MEMS capacitive switches to be related to the ΔV_{PI} changes observed during stress at low electric field levels. The agreement of this model with measured data confirmed for the first time that the charging and discharging of border traps was responsible for the symmetric and reversible pull-in voltage changes measured at low electric fields in RF MEMS capacitive switches.

This chapter was focussed on the characterisation of bulk dielectric charging at low electric fields in RF MEMS capacitive switches. An investigation into surface dielectric charging at higher electric fields will follow in the next chapter.

CHAPTER 6:

INITIAL EXPERIMENTAL INVESTIGATION OF SURFACE CHARGING & SOLUTION METHODS FOR BULK DIELECTRIC CHARGING

6.1 INTRODUCTION

The effects of surface charge were first noted in Chapter 5 when dielectric charging experiments were performed on mechanically-robust Al-Ti capacitive switches. In the absence of mechanical degradation, a clear distinction could be made between two different types of dielectric charging which affected the bulk and surface of the dielectric, respectively. It was seen that due to its proximity to the air gap, charge created at the dielectric surface had a much greater shift effect on device C-V curves than bulk charge. Thus, surface charging is a reliability mechanism of grave concern to the designers of RF MEMS capacitive switches and it is imperative that the causes of surface charging be understood so that steps can be taken to prevent its occurrence. This chapter describes the results of an investigation into surface dielectric charging in RF MEMS capacitive switches and is organised as follows.

Section 6.2 describes the measurement and analysis methods used to investigate surface charging on capacitive switches. Transient changes in the C-V curve of a switch are studied in Section 6.3 while steady-state C-V shifts are used to characterise surface dielectric charging in Section 6.4. Several test structures were conceived to reduce the amount of surface charging which takes place in capacitive switches, and the design and charging characterisation of these devices is also described in this section. In spite of the proven mechanical reliability of Al-Ti membranes, a voltage-dependent C-V narrowing of the pull-out window was observed during charging experiments. Based on measurement results it was concluded that the observed C-V narrowing was due to non-uniform bulk dielectric charging and an investigation into methods of removing this reliability concern from RF MEMS capacitive switches was performed. The results of this investigation are discussed in Section 6.5 before this chapter concludes in Section 6.6.

6.2 MEASUREMENT & ANALYSIS METHODS

In the previous chapter, low DC voltages and single-polarity C-V sweeps were used to characterise the effects of bulk dielectric charging. As stated in Section 5.2, a limit was placed on the maximum DC bias voltage which was applied to switches to restrict the magnitude of the electric field across the dielectric and prevent the accumulation of surface charge. Additionally, single-polarity C-V sweeps of the same polarity as the stress bias were used to preserve the polarity of the electric field which was placed across the dielectric at all times. In this chapter electric fields higher than the threshold value will be used to intentionally create surface charge in switches. However, the use of high electric fields will also cause increased bulk dielectric charging to occur as it was shown in Chapter 5 that bulk charging increases approximately linearly with the applied electric field.

In Chapter 5 bulk dielectric charge was shown to have the same polarity as the stress bias while surface charge was of the opposite polarity as the stress bias. This could be seen in Figure 5.2 where the direction of C-V shift after DC stress changed as the stress bias was increased. Therefore, as a result of the observed changeover from bulk-dominated to surface-dominated dielectric charging it was expected that two different charge polarities would be present in the dielectric at the same time. Moreover, it was believed that the presence of the two different charge types would correspond to a non-uniform distribution of dielectric charge and lead to narrowing of the C-V curve as discussed in Chapter 3. Therefore, single-polarity C-V sweeps would no longer be sufficient to characterise this type of dielectric charging.

Single polarity C-V sweeps were originally used for the characterisation of switch reliability as they minimised the amount of time the membrane spent in the up-state at zero bias in between stress periods. In Section 4.2.3 it was shown that the time delay between two sequential C-V measurements during a mechanical stress experiment caused an artificial shift of the C-V curve as a result of the rapid recovery of the viscoelastic effect. In Chapter 5 bulk charge was also seen to rapidly recover once the stress bias was removed in a similar fashion to the viscoelastic effect reported in Chapter 4. Therefore, single-polarity C-V sweeps were also used to minimise the recovery of bulk charge during the stress phase and allow the full effect of dielectric charging to be measured. However, it was now necessary to measure the full C-V curve of a capacitive switch to characterise the effects of surface charge on device operation. Therefore, to accommodate this change in the measurement procedure and still preserve the charge state of the dielectric the stress and measurement

technique was optimised to minimise the amount of time the membrane spent in the up-state between stress periods. A graphical representation of the performance of a full C-V sweep using the new stress and measurement procedure at +15 V DC is shown in Figure 6.1.

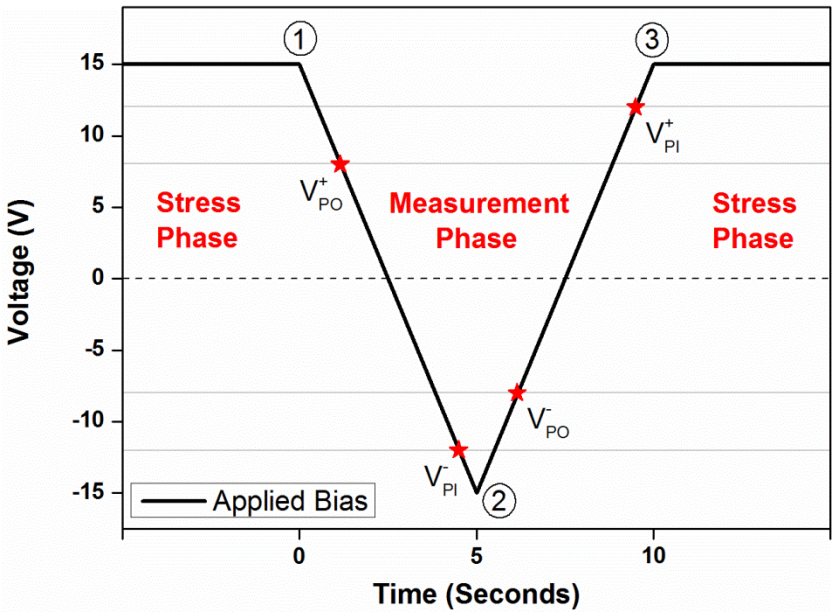

Figure 6.1: Sample diagram of the optimised stress and measurement procedure for +15 V DC bias. The varying bias is represented by the thick black line, the values of the pull-in and pull-out voltages of the switch are represented by horizontal grey lines, and the points at which they are measured are represented by red stars where they intersect the applied bias line.

The stress and measurement procedure proceeds as follows; at the beginning of the experiment the switch is held in the down-state using +15 V. At the end of the stress time ① the bias is not turned off but is gradually decreased towards -15 V in one continuous sweep. The positive pull-out voltage is measured as the bias is decreased, while the negative pull-in voltage is measured as the bias becomes increasingly negative. Once the voltage reaches its lower limit at -15 V ② it begins to increase again in the positive direction allowing the negative pull-out and positive pull-in voltages to be measured. At the end of the measurement procedure ③ the switch is held in the down-state at +15 V and the stress process continues for another set period of time. The amount of time required for the full C-V sweep to be performed depends on the maximum and minimum voltages used. In general, all four threshold voltages can be measured in approximately 10 seconds using this method. As such, the device spends no more than 5 seconds in the up-state during the measurement procedure and any disturbance of charge in the dielectric is minimised. The new stress and measurement procedure was used to monitor the charging

and discharging of AlTi capacitive switches over a range of DC bias conditions. The resulting data was analysed using the *Shift* (4.1) and *Narrowing* (4.2) calculations defined in Chapter 4 and an example of the results obtained is shown in Figure 6.2.

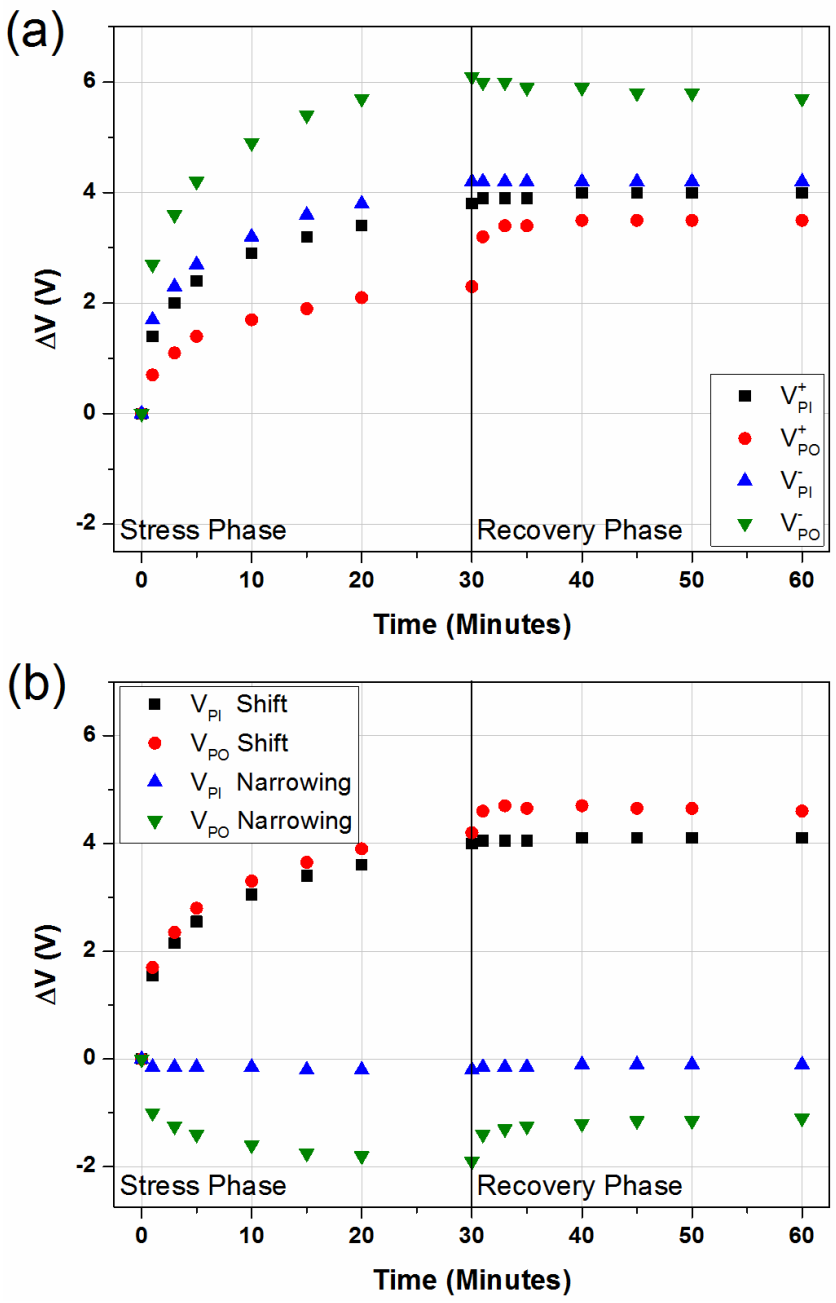

Figure 6.2: ΔV data recorded on an Al-Ti capacitive switch following 30 minutes of stress and recovery at +45 V. The measured C-V shifts are presented in (a) while the *Shift* and *Narrowing* results are shown in (b).

Figure 6.2 (a) shows that all four threshold voltages shifted to the right following DC stress at +45 V. For a bias applied to the bottom metal of a switch, this result indicates that negative dielectric charging has taken place. A difference in the shift magnitude of each threshold voltage was observed where the negative pull-out voltage shifted by +6.1 V, the

positive pull-out voltage shifted by +2.3 V, and only the positive and negative pull-in voltage shifts were in approximate agreement at +3.8 V and +4.2 V respectively. During the recovery phase the negative pull-out voltage shift decreased and the positive pull-out voltage shift increased in magnitude. The same behaviour was observed in the pull-in voltage shifts so that they were approximately equal at the end of the recovery phase.

The different behaviour displayed by each threshold voltage meant that very little insight could be gained by studying the unprocessed data of Figure 6.2 (a) and further analysis was required before the effects of simultaneous bulk and surface charging became clear. The processed results in Figure 6.2 (b) show that the *Shift* and *Narrowing* of the pull-in and pull-out voltages have been clearly segregated from the unprocessed experimental data. The shift magnitude of the pull-in and pull-out voltages now follows the same trend at all measurement stages and results in a net right-shift of 4 V at the end of the stress phase. The additional right-shift of the pull-in and pull-out voltages observed during the recovery phase can be attributed to the disappearance of positive bulk charge when the bias was removed.

The difference between the unprocessed ΔV_{PO} values in Figure 6.2 (a) is now understood to have been caused by a narrowing of the pull-out voltage window. In Figure 6.2 (b) this is seen to increase with time to almost 2 V at the end of the stress phase before gradually recovering once the stress bias was removed. Recoverable narrowing was also observed in the pull-in window but only attained a maximum value of 0.2 V at the end of the stress phase. By referring to the theory of non-uniform dielectric charging derived in Chapter 3, it can be seen that narrowing of the C-V curve is caused by the variance of charge within the dielectric. It is hypothesised that the charge variance is caused by the simultaneous presence of positive and negative bulk and surface charge. The amount of charge and hence the variance increased with time and reached its maximum value at the end of the stress phase before recovering once the DC bias was removed.

The theory of non-uniform dielectric charging derived in Section 3.2.2 attributes the C-V *Shift* effect to the influence of the mean charge in the dielectric. Negative surface charge was present in the switch after the high voltage stress at +45 V and this can be seen from the overall right-shift observed in Figures 6.2 (a) and (b). The additional right-shift of the pull-out voltage observed during the recovery phase may be attributed to the disappearance of positive bulk charge when the bias was removed. Therefore, the observed *Shift* results correlate well with the expected presence of two different polarities

of charge in the dielectric. While at present there is no known method to physically separate the effects of surface and bulk dielectric charging, the effects of surface charge may be studied in isolation by allowing sufficient time after an experiment for bulk charge to disappear. This 'steady-state' method is based on the fact that bulk dielectric charge has been seen to recover within the time frame of an experiment while surface charge persists for a much longer duration. Therefore, the final shifted pull-in and pull-out voltage values of an experiment will be used to characterise the effects of surface dielectric charging and this data will be analysed in Section 6.4. Transient dielectric charging as a result of the combined effects of bulk and surface charge will be analysed in the next section.

6.3 TRANSIENT CHARGING ANALYSIS

A series of charging experiments were performed on Al-Ti capacitive switches where positive and negative DC voltages in the range of 15-45 V were applied to the bottom metal. Transient changes in the device C-V curves were measured using the procedure outlined in the previous section. Each switch was stressed for 30 minutes before being allowed to recover for an additional 30 minutes. The experimental data was analysed using the *Shift* (4.1) and *Narrowing* (4.2) calculations and it was observed that the combined effects of bulk and surface charging resulted in a time-dependent narrowing of the C-V curve which increased with the magnitude of the applied bias. The maximum narrowing measured at the end of each stress phase was collated and these values are plotted as a function of the stress bias in Figure 6.3.

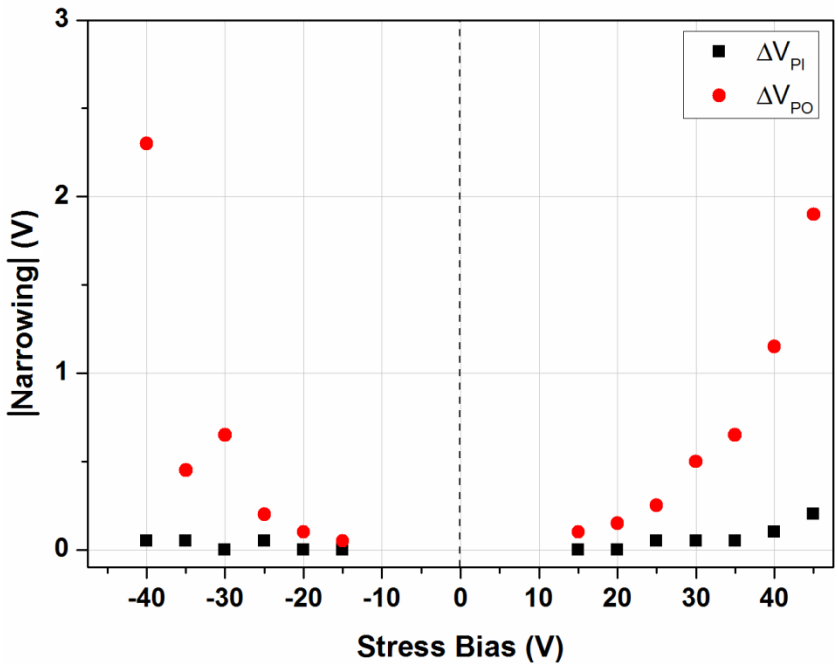

Figure 6.3: Magnitude of the narrowing experienced by the pull-in and pull-out voltages after 30 minutes of stress at various DC biases.

Figure 6.3 shows that C-V narrowing occurred primarily in the pull-out window. There was almost no effect on the pull-in voltage with a maximum narrowing of 0.2 V measured after 30 minutes of stress at +45 V. DC stress at -45 V caused the capacitive switch to become stuck in the down-state so that the *Narrowing* calculation could not be performed. The theory [114, 117] and experimental evidence [100] of C-V narrowing as a result of non-uniform dielectric charging were discussed in Chapter 3. However, the voltage-dependence of this process has never previously been demonstrated. Therefore, the results presented here are the first experimental evidence of voltage-dependent C-V narrowing as a result of non-uniform dielectric charging in RF MEMS capacitive switches.

The voltage-dependent C-V narrowing partially recovered once each stress bias had been removed and this is shown for a selection of data in Figure 6.4. An explanation for the recoverable nature of C-V narrowing as a result of non-uniform dielectric charging was proposed by Herfst who used Kelvin-Probe Force Microscopy to measure the electrical potential of a dielectric surface following a high-voltage stress [129]. Herfst observed that the surface charge density gradually diffused over time, moving from areas of high potential to areas of low potential before decaying generally. Based on these results Herfst suggested that gradual diffusion decreased the lateral non-uniformity of the surface charge over time and hence reduced the observed C-V narrowing. A similar mechanism may explain the reversible nature of the V_{PO} narrowing shown in Figure 6.4, while the remaining

narrowing and long-term C-V shift can be explained by the persistent effects of non-uniform surface charge. However, because V_{PO} narrowing was observed after DC stress voltages as low as 15 V while the effects of surface charging did not become apparent until 30 V and above (see Figure 5.2), it is hypothesised that the voltage-dependent V_{PO} narrowing is also related to the presence of non-uniform bulk dielectric charge. The recoverable nature of bulk dielectric charging can explain the partially recoverable V_{PO} narrowing observed in Figure 6.4, while the long-term narrowing can be attributed to the effects of surface charge.

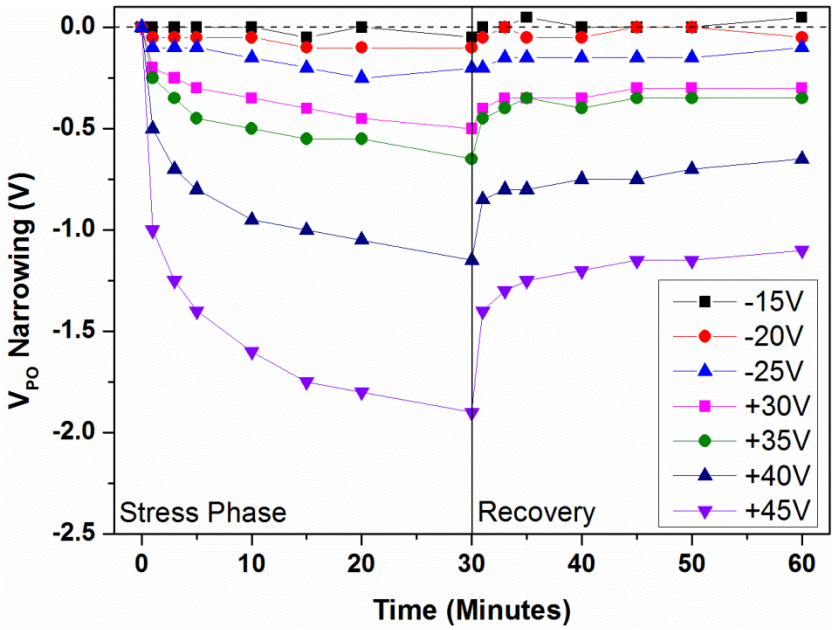

Figure 6.4: Voltage-dependence of the transient and partially-recoverable pull-out voltage narrowing effect.

In Section 3.2.2 it was shown that non-uniform dielectric charging is an unavoidable consequence of the electrostatic operation of capacitive switches due to the dielectric roughness and design of the moveable membrane. Therefore, it is unsurprising that C-V narrowing due to non-uniform dielectric charging is observed to occur at all stress voltages in Figure 6.3, even at bias levels as low as 15 V. However, this effect would not be observed if only pull-in voltage changes were measured, as Figure 6.3 and Figure 3.11 show that narrowing due to non-uniform dielectric charging predominantly affects the pull-out voltage window. Therefore, non-uniform bulk dielectric charging can be approximated by a uniform charging model when only the pull-in voltage change is measured. Moreover, this explains why the simple 1D model derived in Section 5.4 was able to describe the uniform border trapping process of a capacitive switch even though a distributed dielectric charging model would be more realistic.

The results presented in this section show that non-uniform bulk dielectric charging is a significant reliability concern of capacitive switches. Narrowing of the pull-out voltage window during stress can lead to device stiction even if the pull-in voltage values are still within operational limits. This can explain the switch failure due to stiction after -45 V stress reported in Figure 5.1. A C-V shift of 0.8 V was measured immediately before the device became stuck in the down-state, while the initial pull-out voltage values were approximately equal to ±8 V. As the low C-V shift cannot account for the failure of the device to re-open after stress, it must be concluded that the unexpected stiction was caused by the disappearance of the pull-out window as a result of V_{PO} narrowing.

Therefore, contrary to the opinions expressed in the literature that bulk dielectric charging is tolerable so long as surface dielectric charging can be avoided [44, 86], it is proposed that the elimination of non-uniform bulk dielectric charging is equally important to improve the long-term reliability of RF MEMS capacitive switches. Additionally, the removal of bulk charging would also allow a more rigorous characterisation of surface charging in RF MEMS capacitive switches to be performed, as the transient properties of this reliability concern could then be studied in isolation. A method of removing bulk dielectric charging from RF MEMS capacitive switches was developed as part of this work and details of this are given in Section 6.5. However, fully processed switches with reduced border traps were not fabricated in time for this research and so an initial examination of surface charging was performed using steady state charging data, as described previously. Details of this investigation are given in the following section.

6.4 STEADY-STATE CHARGING ANALYSIS

As described in Section 6.2, the steady state voltage shift of a capacitive switch can be used to characterise surface charging once the effects of bulk charge have disappeared. A similar steady-state characterisation method was originally used by Peng to identify bulk and surface charging in RF MEMS capacitive switches which were fabricated using aluminium membranes [47, 120]. However, when aluminium is used as the membrane material it is possible that transient mechanical degradation could be mistaken for bulk dielectric charging, while permanent changes caused by material creep could be attributed to the effects of surface dielectric charging. To avoid this, all experiments were performed on mechanically-robust Al-Ti capacitive switches so that any changes in the device C-V curve could be attributed to dielectric charging only.

To characterise the long-term charging effects of capacitive switches, several Al-Ti devices were stressed using DC biases of both polarities in the range of 15-45 V. All biases were applied to the bottom metal for 30 minutes. After 30 minutes of stress the bias was removed and the effects of bulk charge were allowed to recover in the off-state for another 30 minutes. The full C-V curves of each switch were measured using the stress and measurement technique described in Section 6.2. This data was analysed using the *Shift* calculation defined in Chapter 4 and the final *Shift* value obtained from each switch is plotted against the stress bias in Figure 6.4.

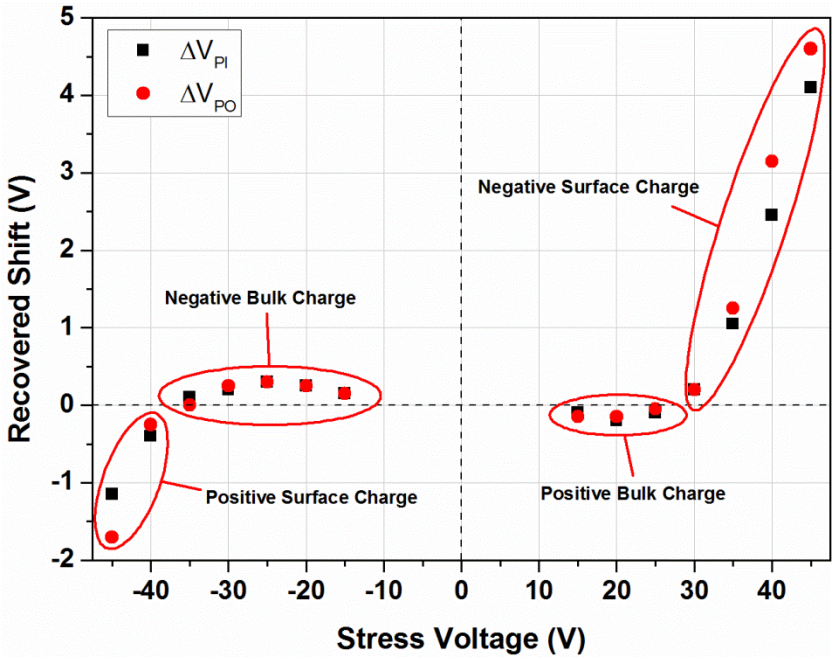

Figure 6.4: Shift of the pull-in and pull-out voltages of Al-Ti capacitive switches after 30 minutes of stress at various DC biases followed by 30 minutes of recovery at zero bias. Regions dominated by bulk and surface charging are indicated on the graph.

Stress voltages which predominantly cause bulk dielectric charging can be identified in Figure 6.4 where the C-V shift is close to being zero at the end of the recovery time and the direction of any remaining shift indicates that the charge is of the same polarity as the stress bias. Recall that for a bias applied to the bottom metal, a right-shift indicates that negative dielectric charging has taken place while a left-shift indicates that positive dielectric charging has occurred. In Figure 6.4 it can be seen that the dominant effects of bulk dielectric charging occur between -15 V and -35 V for negative stress and between +15 V and +25 V for positive stress and these regions are indicated on the graph.

Surface charging of the opposite polarity as the stress bias dominates the switch behaviour at high stress voltages and these regions are also indicated on the graph. From Figure 6.4 it can be seen that surface charging occurs at different bias levels for each voltage polarity. The capacitive switches are dominated by negative surface charging after positive voltage stress at +30 V, while the effects of positive surface charging do not dominate the switch behaviour until a negative stress bias of at least -40 V is applied. Moreover, the effects of negative surface charging appear to be more harmful to switch operation than positive surface charging, as the resulting C-V shift is significantly higher following positive stress than negative stress at the same voltage magnitude. Consequently, this indicates that device lifetime may be prolonged through the use of negative DC biases applied to the bottom electrode which minimise the amount of surface charging taking place. However, even if the rate of surface charging is reduced in such a fashion, the long-term accumulation of charge at the dielectric surface remains a limiting reliability mechanism of capacitive switches. Therefore, alternative means of reducing or eliminating the amount of surface charging which takes place in capacitive switches are desired, and tests on several test structures designed to investigate this are described in the next section.

6.4.1 Test Structure Design to Reduce Surface Charging

Another set of Al-Ti capacitive switches were fabricated to investigate several design changes which were implemented to reduce the amount of surface charging taking place. Three different device wafers were fabricated in parallel to minimize any processing differences between them and schematic drawings of the resulting capacitive switches are shown in Figure 6.5.

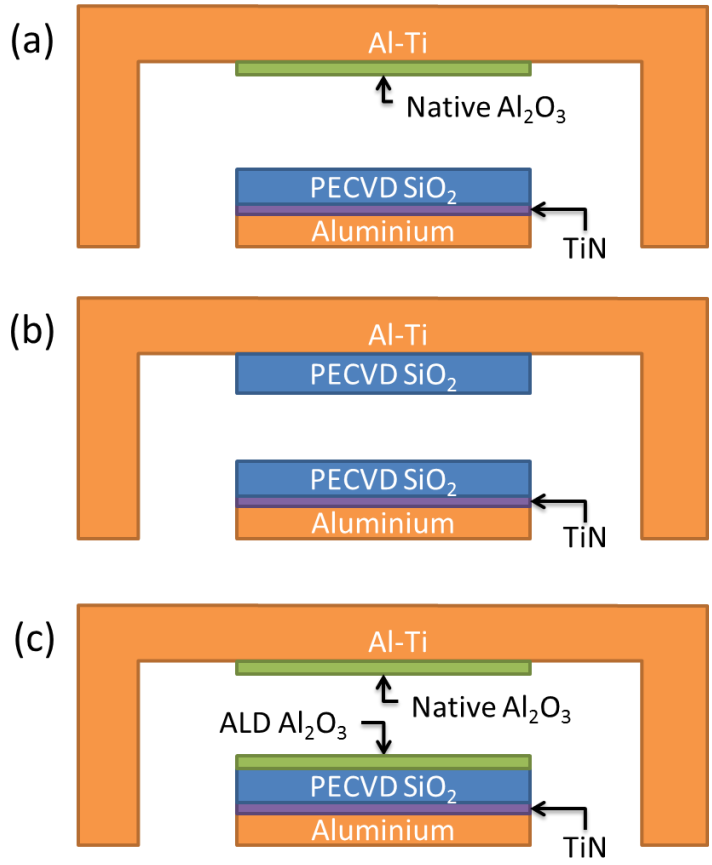

Figure 6.5: Schematic drawings of the three different switch designs used to investigate surface charging. A standard switch with native oxide (a), a switch fabricated with a top and bottom PECVD SiO_2 dielectric (b) and a standard switch with an additional 2 nm layer of ALD Al_2O_3 on top of the bottom dielectric (c).

The first switch pictured in Figure 6.5 (a) is a standard MEMS capacitive switch which was fabricated to act as a control device. However, based on the results of previous device characterisation [211] a more realistic picture of the switch metal/dielectric interfaces has been used where a native oxide layer is included on the underside of the top metal. The native Al_2O_3 layer is grown by exposure to oxygen plasma during the sacrificial layer release step of device fabrication and is expected to be approximately 10 nm thick [212, 213]. More details of this material are provided in Section 6.5.3.

As discussed in Chapter 3, it is hypothesised that localised high electric fields present at the rough top metal/dielectric interface may cause surface charging to occur when the membrane is in the down-state [47, 49, 51, 55]. To overcome this, the standard switch design has been modified to include a thicker top dielectric fabricated on the underside of the moveable membrane and this device is pictured in Figure 6.5 (b). By separating the top metal from the rough dielectric surface with a thick oxide layer, it is expected that a reduced electric field will be present at the dielectric interface which will result in less

surface charging. During fabrication, the membrane material was sputtered directly on top of the upper dielectric so that no native oxide is expected to be present on the underside of the top metal. PECVD SiO_2 was used for both dielectric layers and was deposited to a thickness of approximately 54 nm in each case. In this way the total dielectric thickness (108 nm) is comparable to the standard oxide thickness which has been used thus far (130 nm) and should allow a direct device-to-device comparison to be performed.

Finally, it is hypothesised that the damaging effects of plasma ashing and dry etching processes during device fabrication can facilitate surface charging by increasing the density of charge traps near the top surface of the bottom dielectric [214, 215]. In an effort to reduce this, a third switch design was fabricated with an additional layer of Al_2O_3 grown on top of the bottom dielectric using atomic layer deposition and this is shown in Figure 6.5 (c). The Al_2O_3 layer is harder than the underlying SiO_2 [216, 217] and was deposited to a thickness of 2 nm to protect the underlying SiO_2 from plasma damage during the final polyimide release etch. It is hypothesised that the thin alumina layer will reduce the density of charge traps present near the top dielectric interface. The results of dielectric charging tests performed on each of these capacitive switches are given in the following section.

6.4.2 Test Structure Experimental Results and Analysis

Each switch technology was tested under similar conditions as those applied to standard Al-Ti capacitive switches; a range of DC voltages of both polarities were applied to the switches until clear evidence of surface charging was recorded. Each bias was applied to the bottom metal for 30 minutes while the changes in all four threshold voltages were measured. After 30 minutes of DC stress the bias was removed and the recovery of each switch was measured for another 30 minutes. The *Shift* of each device was calculated at the end of the recovery time and these data are displayed in Figure 6.6. To simplify the analysis, only *Shift* values obtained from changes in the pull-out voltage are shown and the V_{PO} data from Figure 6.4 is also included for comparison.

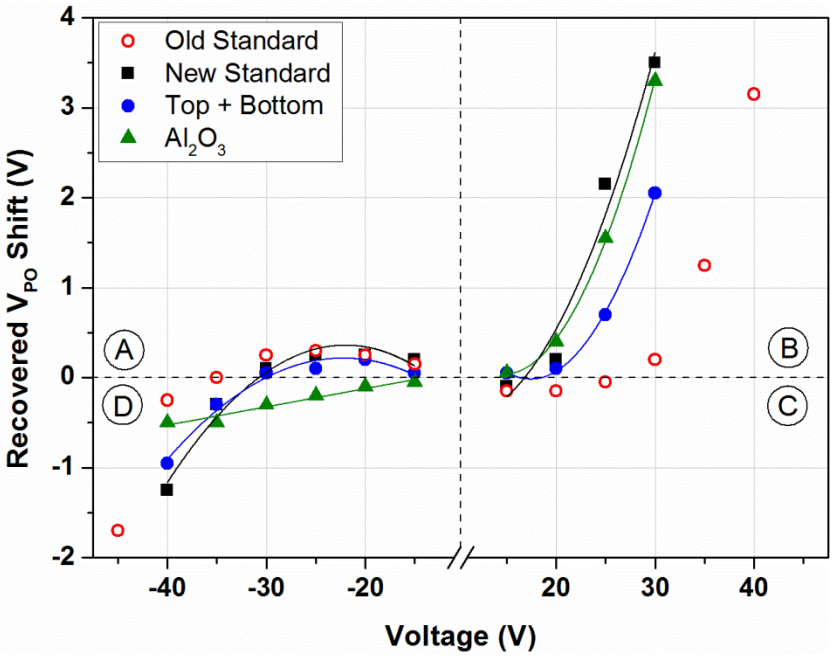

Figure 6.6: Shift values calculated from ΔV_{PO} data of four different switch technologies after 30 minutes of stress at various DC biases followed by 30 minutes of recovery at zero bias. The charging behaviour of each switch can be classified into four different regions A, B, C or D which correspond to positive or negative bulk or surface charging.

Similar to Figure 6.4, the results of Figure 6.6 can be divided into four regions where the effects of bulk and surface charging are dominant and these regions are indicated by the letters A, B, C and D on the graph. As before, regions dominated by bulk dielectric charging can be identified where the C-V shift is close to being zero at the end of the recovery time and the direction of any remaining shift indicates that the charge is of the same polarity as the stress bias. Conversely, regions dominated by surface charging can be seen where the V_{PO} shift is non-zero at the end of the recovery time and the direction of shift indicates the charge is of the opposite polarity to the stress bias. The letters (A) and (C) in Figure 6.6 indicate regions where the charging behaviour is dominated by the effects of negative and positive bulk charging, respectively. While regions (B) and (D) show where the charging is dominated by negative and positive surface charging, respectively.

By observing the direction of the pull-out voltage shift at each voltage value, it can be seen that negative surface charging took place after high positive voltage stress while positive surface charging took place after high negative voltage stress. Therefore, no single design modification was sufficient to eliminate the effects of surface charging. In fact, the new switches appeared to be even more susceptible to surface charging that the old standard switches. While the new standard switches displayed the familiar curved trend of

increasing ΔV_{PO} with increasing voltage, negative surface charging occurred at a lower positive threshold voltage than before (+20 V instead of +30 V) and positive surface charging also occurred at a lower negative threshold voltage than before (-35 V instead of -40 V). The increased susceptibility to dielectric charging may be due to processing differences between the old and new Al-Ti switches. While all of the wafers were fabricated at the same time, the new designs were stored in the clean room for a number of months before being released for testing. The wafers were stored with their polyimide sacrificial layers intact and the final release etch was performed as new devices were required. While the sacrificial layer was intentionally left on to preserve the underlying structures, the polyimide material is known to absorb moisture from the air [218] which may have affected the underlying dielectrics. Therefore, the device architectures featuring Top + Bottom dielectrics and Al_2O_3 layers deposited by atomic layer deposition will be compared with the new standard switches, as all of these were stored and processed at the same time.

The charging behaviour of all three device types was dominated by the effects of negative surface charging following positive voltage stress at biases of +20 V and above. However, the C-V shift of devices with a top and bottom dielectric layer (T+B) was significantly lower than the other two designs at stress voltages higher than +20 V. Based on previous device characterisation it is estimated that the standard and Al_2O_3 devices have a 10 nm thick native oxide layer on the underside of the membrane [211]. As described previously the T+B device has 54 nm thick PECVD oxide layer on the underside of the membrane. The lower C-V Shift results for positive bias shown in Figure 6.6 indicate that negative surface charging has been reduced by the presence of a thicker top dielectric. This may be attributed to the lower electric field present at the dielectric/dielectric interface of T+B devices, or to the alternative dielectric material used on the underside of the top metal or a combination of both effects.

For negative bias, the ΔV_{PO} shift of the new standard and T+B devices followed a very similar curved trend and transitioned from bulk-dominated negative charging to surface-dominated positive charging as the stress bias was increased. However, the Al_2O_3 devices exhibited a completely different charging response and appeared to be affected by positive surface charging after stress biases as low as -15 V. Additionally, the C-V shift due to positive surface charging increased in a linear fashion with increasing stress bias and appeared to saturate after -35 V. All three device types have a PECVD SiO_2 bottom dielectric. However, the Al_2O_3 devices have an additional ALD alumina layer which was

deposited to protect the underlying SiO_2 dielectric from plasma damage. The alumina layer appears to have reduced the amount of negative surface charging which takes place at high voltages and this effect may be leveraged to create more reliable devices under negative stress biases.

Therefore, while these devices have not solved the problem of surface dielectric charging, the results obtained in this section have shown that the composition of the top dielectric strongly influences negative surface charging under positive voltage stress, while the top surface of the bottom dielectric is responsible for positive surface charging under negative voltage stress. Based on these results, it can be stated that the use of thin alumina layers on the top surface of the bottom dielectric and negative actuation voltages applied to the bottom electrode represent the most promising approach to improve surface charging in RF MEMS capacitive switches.

While the characterisation of surface charging was restricted by the limits imposed by steady-state charge analysis, some insight has been gained on the physical origins of surface charge. Based on the results obtained in this section where all biases were applied at the bottom electrode, it is hypothesised that negative surface charging is caused by charge injection from the top electrode during positive stress while positive surface charging is caused by electron de-trapping from the bottom dielectric during negative stress. In the future a more detailed characterisation of surface charging could be performed if switches were fabricated in which bulk dielectric charging has been removed. In the previous chapter it was shown how bulk dielectric charging is caused by the injection and de-trapping of charge to and from border traps located within several nm of the bottom metal/dielectric interface of a switch. Border traps of this type have long been a source of concern in the fields of MOS and flash-memory devices [190, 191, 202, 219]. Over time, researchers of MOS technology have developed several methods of reducing the border trap density in their devices. The same techniques were applied to MEMS capacitive switches in an attempt to reduce the border trap density and improve device lifetime, and details of this investigation are given in the following section.

6.5 METHODS TO SOLVE BULK CHARGING

A significant amount of research has been performed in MOS devices on the causes and effects of border trapping processes [190, 191, 193, 195, 197, 207, 209]. There are several different oxide defects which are known to function as border traps including oxygen

vacancies [202, 220], lattice impurities [193] and dangling or broken bonds [128, 221]. Over the years several fabrication methods which alleviate the border trapping phenomenon have been developed using techniques such as thermal annealing [222-224], plasma treatments [128, 225] and various modifications to the fabrication process [205, 221]. The following sections contain details of experiments designed to test the applicability of several processing techniques to solve the border trapping problem in RF MEMS capacitive switches.

6.5.1 Thermal Annealing

Thermal annealing is a widely-used semiconductor fabrication technique for thermal oxidation, dopant activation and the redistribution of impurities at high temperature [10]. Moreover, it has been shown on thermally-grown silicon oxides that post-deposition annealing decreases the density of interface traps [222-224, 226, 227] with higher temperatures being more effective at passivating the trap sites [228, 229]. During high-temperature annealing, it is believed that reactive elements present in the ambient gas are incorporated into the oxide and passivate trap sites by reducing the number of strained and dangling bonds [128, 223, 224]. In the semiconductor industry these anneals are performed at temperatures in excess of 400°C which are too high for use with MEMS devices. In a previous investigation it was determined that MEMS devices fabricated at Tyndall National Institute can withstand thermal treatments up to 400°C without damage [230]. Higher temperatures resulted in cracking of the Al/1%Si layer used for the bottom electrodes. The devices tested were cantilever beams featuring an aluminium top metal, and were annealed before the sacrificial polyimide layer had been removed. Based on these results a maximum annealing temperature of 400°C was chosen for this investigation.

The effects of thermal annealing on SILC transients in silicon dioxide were investigated using MIM devices as a strong correlation between the charging properties of these devices and MEMS switches was demonstrated in Chapter 5. Moreover, MIM devices with dimensions of up to 1 mm^2 were available for study which should have been more sensitive to changes in the border trap density than standard MEMS switches. The MIM devices were annealed at 400°C for 30 minutes in three different ambient gases. These gases were forming gas (a mixture of hydrogen and nitrogen), nitrogen and 'humid' nitrogen which is N_2 bubbled through water before entering the furnace [231]. One control group of MIM devices did not receive any anneal. All devices were fabricated on the same wafer which was diced into pieces for the different annealing steps. Transient charging and discharging

currents were measured on each of the four device types to investigate the effects of the thermal anneal on the border trap density. Biases of both polarities were applied to the top metal of the devices in the range of 5 V to 30 V. Discharging currents were studied to avoid the influence of conduction currents on transient current measurements, as before. The discharging current densities obtained after 1 minute of stress at +30 V are shown in Figure 6.7.

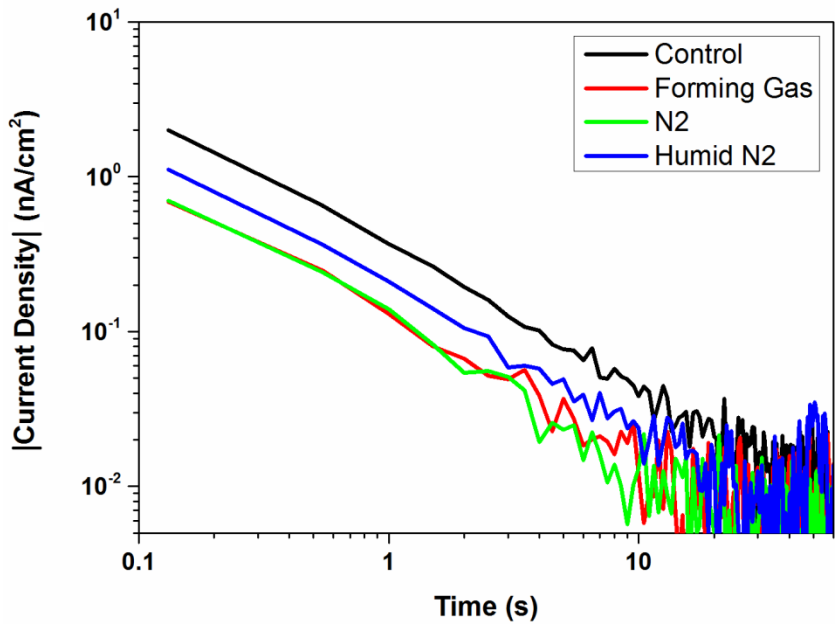

Figure 6.7: DCTs measured on four different MIM devices after being charged for one minute at +30 V.

These currents decayed to noise levels in approximately 10 seconds. While the annealing step did not eliminate the SILC transients it can be seen that the magnitude of the current density was reduced by the thermal anneal. The size of the reduction was slightly greater when forming gas or nitrogen was used. These gases decreased the current density by a factor of 3. If the devices were to be annealed at higher temperatures or for longer times the SILC effect may be further reduced, but the greater thermal stress could also damage the devices. Rather than attempt to decrease the number of existing traps through a post-processing anneal, an ideal solution would be to minimize the number of traps which are created during the fabrication process itself. A modified PECVD oxide recipe was investigated to reduce the number of border traps and the results of this are described in the following section.

6.5.2 Modified PECVD SiO_2 Recipe

It is known that the border traps responsible for SILC processes are formed when a high voltage stress is applied to a dielectric [190, 191, 193, 207, 221]. However, in the devices

investigated in this work it is believed that a sufficient density of border traps exists in as-deposited films to allow transient SILC currents to be measured without applying a high voltage. The presence of the SILC effect in as-deposited PECVD dielectrics has been reported before [232]. However, very little attention has been paid to the physical processes responsible for the formation of these border traps [233]. It has been widely reported that the charging properties of PECVD dielectrics are dependent on the deposition conditions used during fabrication [104, 142, 234]. Many factors can affect the deposition conditions such as the ratio of gases involved, the gas flow rate, the chuck temperature and the RF power used. An exhaustive investigation of the potential improvements to PECVD deposition as a result of process modification is outside the scope of this thesis. However, a comparison between two different PECVD recipes which were developed in Tyndall has been made.

The dielectric films used in this work were deposited using an Electrotech Delta 201 PECVD reactor. The standard oxide recipe used 430 W RF power and featured gas flow rates of 2000 standard cubic centimetres per minute (sccm) of N_2O and 140 sccm of SiH_4. The SiO_2 films grown using this recipe have a deposition rate of approximately 1.5 µm per minute. As this deposition rate is quite high for MEMS devices where oxide thicknesses in the 100 nm range are desired, an alternative recipe was developed to achieve a much slower deposition rate. The modified recipe used 100 W RF power and gas flow rates of 1000 sccm and 20 sccm for N_2O and SiH_4, respectively. The significantly lower RF power and gas flow rates resulted in a deposition rate of approximately 325 nm per minute.

To investigate if the slower oxide deposition rate led to a reduction in the border trap density of PECVD oxides, the two deposition conditions were compared using metal-insulator-silicon (MIS) devices, as MIS devices required fewer processing steps and could be fabricated more rapidly than MIM devices. These devices were fabricated using highly-doped n-type silicon wafers as the bottom electrode with a 130 nm thick SiO_2 dielectric deposited on top. The devices were biased in accumulation mode for testing and evaluation purposes. Current-voltage characteristics were measured with the bias applied to the top metal. The voltage was swept from 0 V to 100 V in 1 V steps. DCTs were also measured after the devices had been charged with various positive DC biases. The results of these tests are shown in Figure 6.8.

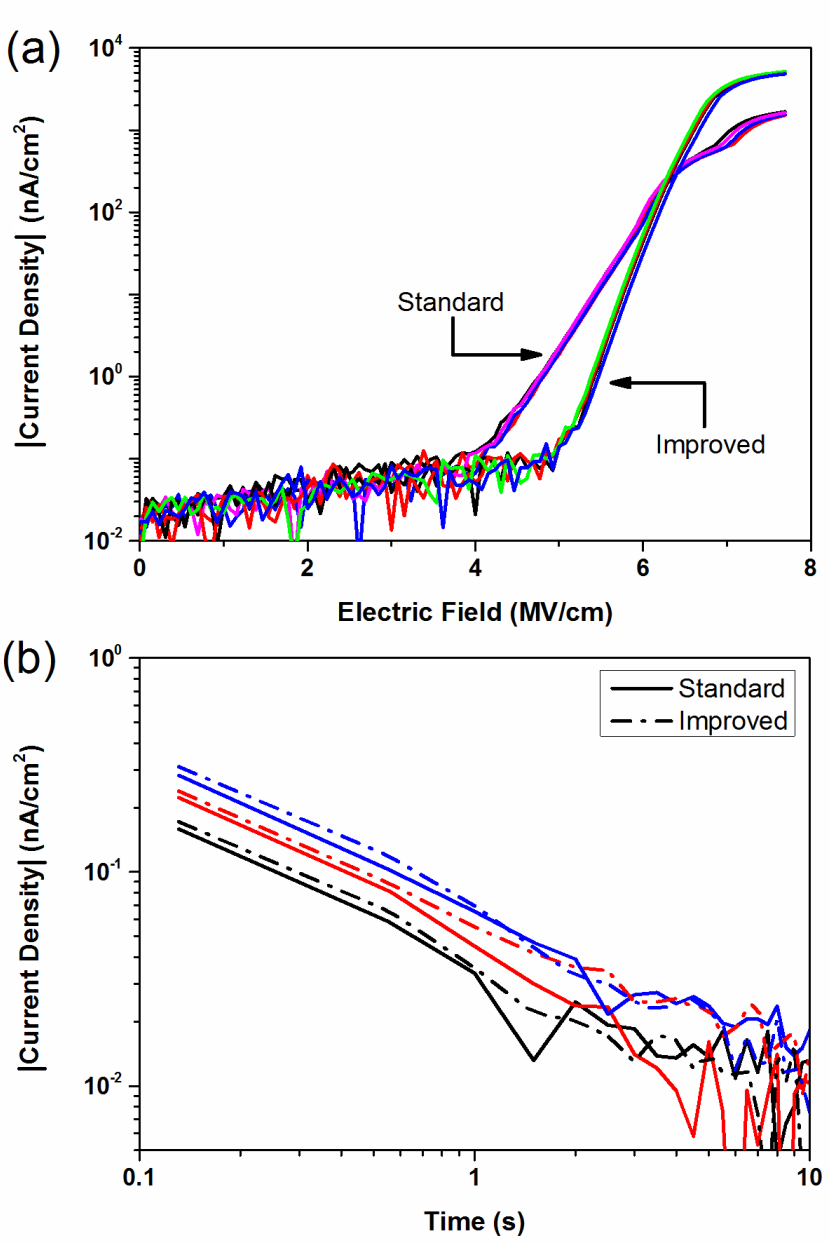

Figure 6.8: J-E characteristics measured on the standard and modified oxides (a) and DCTs recorded on both dielectrics after being charged at 1.9 MV/cm (black), 2.5 MV/cm (red) and 3 MV/cm (blue) (b).

Low-level charging currents which gradually increased with voltage were measured on both devices and are shown in Figure 6.8 (a). No significant difference between the two PECVD oxides was seen until the onset of conduction at 4 MV/cm in the standard oxide and at 5.5 MV/cm in the modified oxide. Additionally, no improvement in transient currents was observed between the two dielectrics as can be seen in Figure 6.8 (b) where the DCTs of standard and modified devices are almost overlaid after each voltage stress. This result indicates that the density of border traps at the silicon-oxide interface has not been affected by modifying the deposition recipe. However, the transient current densities

reported in Figure 6.8 (b) are an order of magnitude lower than the border trap current densities obtained on either MIM or MEMS devices. This result indicates that the number of border traps at the silicon-oxide interface is lower than at the metal-oxide interface or, alternatively, that the additional processing steps used in MIM and MEMS fabrication increase the border trap density by a factor of 10. This increase in border trap density may be due to damage caused by the plasma etching and ashing steps necessary for MEMS manufacture [214]. The optimisation of the fabrication process in order to reduce border traps will be the subject of future work.

PECVD dielectrics are particularly suitable for use in MEMS devices where thick dielectric layers are required in tandem with a low thermal budget. However, the film quality and interfacial properties of PECVD dielectrics suffer from a lack of high temperature annealing [128]. Although significant progress has been made in improving the electrical properties of PECVD oxides [234], thermally-grown silicon dioxide is known to possess superior structural and electrical characteristics [235, 236]. Unfortunately, silicon oxides grown by thermal oxidation cannot be used in MEMS devices which feature metal bottom electrodes. However, it is known that native oxides are formed on exposed metal surfaces over time through the natural process of corrosion [237]. While in the most well-known cases this oxidation is an unwanted and detrimental effect (e.g. rust), if a native oxide of sufficiently high quality could be grown in a controllable fashion, then this could have beneficial effects on border charging processes at metal/dielectric interfaces. An investigation into the use native oxides in RF MEMS capacitive switches is described in the following section.

6.5.3 Native Oxide Test Structures

It is known that native aluminium oxide (alumina, Al_2O_3) is formed on aluminium surfaces which are exposed to air. At room temperature the thicknesses of these layers are reported to be in the range of 2-5 nm [238, 239] however the oxide thickness may be increased by using accelerated growth conditions such as elevated temperatures and oxygen plasmas [212, 213]. In previous work, a test wafer was fabricated to measure the native oxide thickness found on capacitive switches which were fabricated in Tyndall [211]. This wafer was processed as far as the bottom metal deposition step following the standard switch fabrication procedure described in Chapter 2. Thus, the wafer featured a 0.5 µm thick blanket layer of Al/1%Si deposited on top of the substrate and initial oxide. After deposition of the metal the wafer was ashed for 30 minutes in oxygen plasma to replicate the usual polyimide removal process. Following this, a sample of the wafer was prepared

for transmission electron microscopy (TEM) analysis by depositing platinum on top of the aluminium layer. A TEM image of the wafer cross-section is shown in Figure 6.9 where the area of interest has been enlarged. It can be seen that a layer of material is present between the aluminium and platinum which is believed to be the native oxide grown due to ashing. This layer is approximately 10 nm thick, which agrees with reported values for aluminium oxide thickness grown by microwave-induced plasma [213] and provides an estimate for the native oxide thickness quoted in Section 6.2.1.

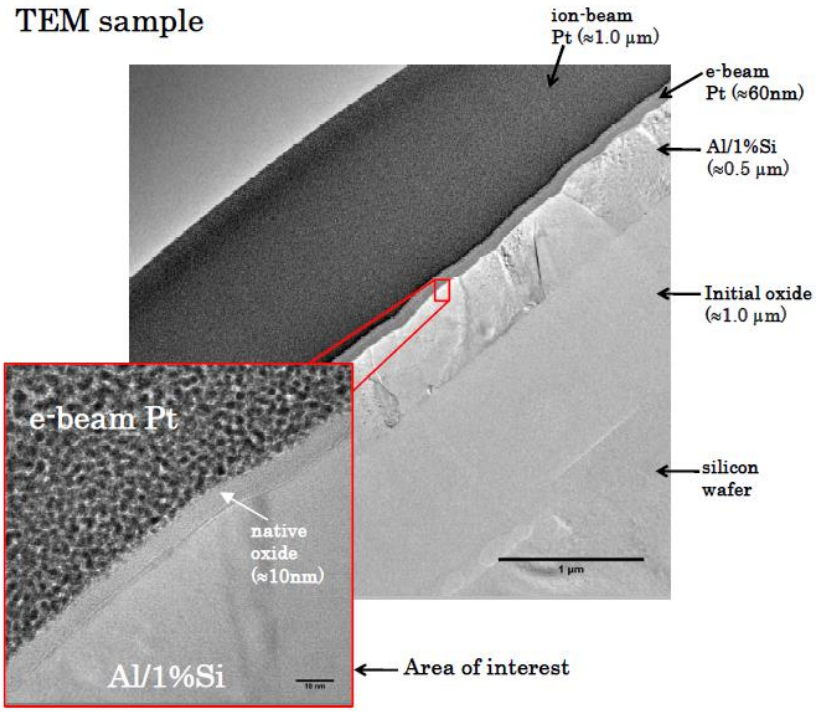

Figure 6.9: TEM image of the test wafer fabricated to investigate the native oxide thickness grown after plasma ashing. The enlarged area shows a 10 nm thick native oxide layer sandwiched between the electron-beam deposited platinum and the sputtered bottom metal. Reprinted from [211], with permission.

RF MEMS capacitive switches fabricated using aluminium membranes were chosen to characterise this native oxide. These devices were fabricated following the standard procedure but without any dielectric layer deposition, such that the only oxide present is the native alumina grown during the polyimide removal process. This native oxide is expected to grow equally well on both the top and bottom metals so that the total oxide thickness is estimated to be approximately 20 nm. Given this low dielectric thickness, the capacitive switches were designed to have a low pull-in voltage [115] to avoid the creation of excessively-high electric fields during measurements. Devices with an area of 200x200 μm^2 were tested across the wafer, and typical C-V and I-V characteristics are shown in Figure 6.10.

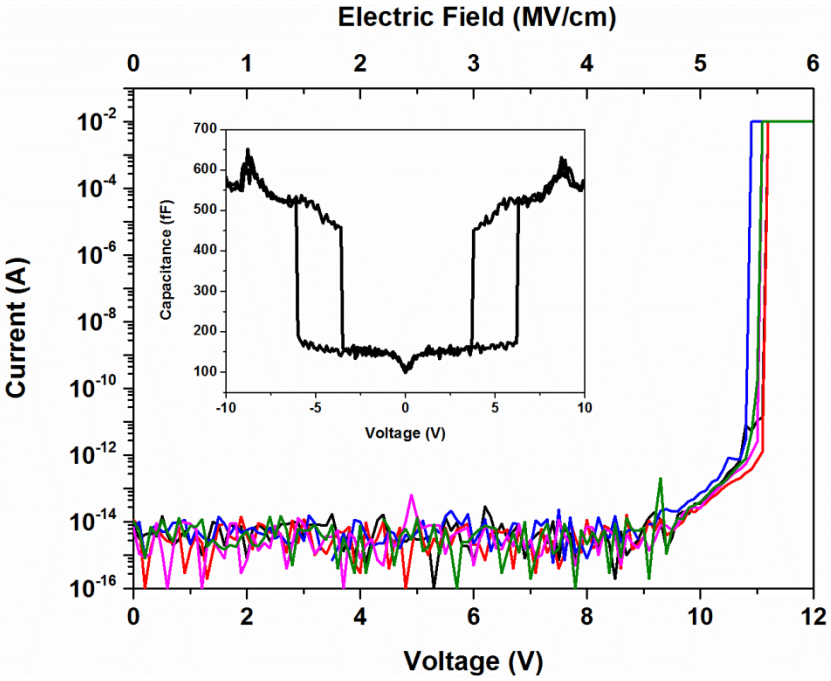

Figure 6.10: I-V graph measured on five dielectricless switches showing that no current is measured after pull-in until conduction begins at 9 V (4.5 MV/cm). The average breakdown field is 5.5 MV/cm. Inset: A typical C-V curve measured on dielectricless switches. The spikes in the C-V curve are caused by conformal movement of the membrane in the down-state, while the dip in the C-V curve around 0 V is caused by substrate parasitics [187,188].

The average pull-in voltage of these devices was approximately 5.7 V. From Figure 6.10 it can be seen that no currents were measured after pull-in until an electric field greater than 4 MV/cm was reached. After this the conduction current increased with voltage until dielectric breakdown occurred at an average electric field of 5.5 MV/cm. This breakdown field falls within reported values for Al_2O_3 [211]. C-V and I-V characteristics were also measured on identical 200x200 μm^2 devices fabricated on a separate wafer which included a 130 nm PECVD SiO_2 dielectric. A comparison of the current versus electric field of both device types is shown in Figure 6.11.

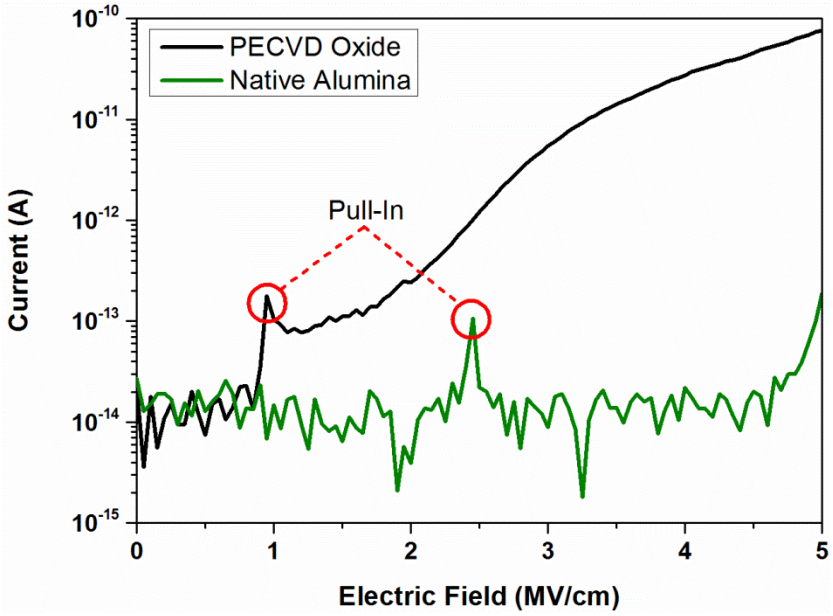

Figure 6.11: Comparison between the I-E characteristics obtained from RF MEMS capacitive switches featuring PECVD SiO_2 and native Al_2O_3 dielectrics. The point of pull-in can be identified by a current spike as indicated on the graph.

Figure 6.11 compares the currents measured on PECVD SiO_2 and native Al_2O_3 devices as a function of the increasing electric field. In both cases the electric field was increased from 0 MV/cm to 5 MV/cm at a ramp rate of 0.05 MV/cm per second. The pull-in point of the SiO_2 device can clearly be seen by the abrupt increase in current when the membrane makes contact with the dielectric at 1 MV/cm. Following this the measured current increases with the electric field. A current spike corresponding to pull-in can also been seen on the native Al_2O_3 device at 2.5 MV/cm which is caused by an increase in stored charge as a result of the sudden increase in capacitance. Thereafter, no current is visible on the native Al_2O_3 device until conduction begins around 4.5 MV/cm, similar to the results presented in Figure 6.10. Based on these results it can be concluded that the conduction properties of native alumina are much better than PECVD SiO_2. We hypothesise that the difference in conduction currents is due to a different density of border traps in both dielectrics. To confirm this, charging current transients were also measured on both dielectrics to test for the presence of border traps. A positive electric field of 3 MV/cm was applied across each dielectric to ensure the membrane was in the down-state and to avoid the influence of large leakage currents on the transient current measurement. Only one polarity electric field was used as it was shown in Chapter 5 that the charging currents are symmetrical with respect to the bias polarity. The results of these tests are shown in Figure 6.12.

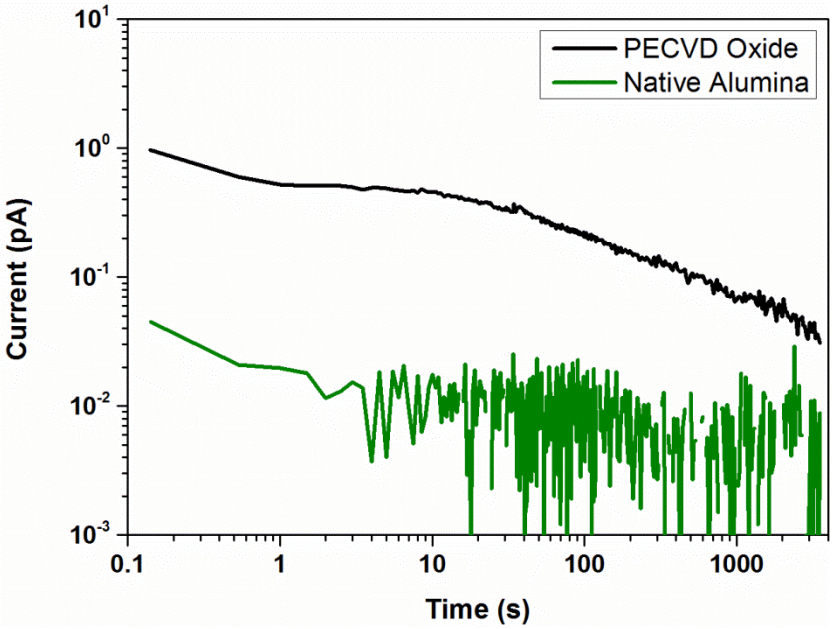

Figure 6.12: A comparison between the transient charging currents measured at 3 MV/cm on capacitive switches with PECVD SiO_2 and native Al_2O_3 dielectrics. The charging current measured on the native oxide falls to noise levels after 1.5 seconds.

A transient charging current was measured on the PECVD SiO_2 which gradually decayed over the duration of the experiment. The peak current value was measured at approximately 1 pA. A transient charging current of peak value 45 fA was also measured on the native alumina and decayed to noise levels after 1.5 seconds. In accordance with the findings of Chapter 5, the presence of transient currents indicates that border traps are present in both dielectrics; however, the significant difference in the peak currents suggests that the density of border traps is more than one order of magnitude lower in the thermally-grown native alumina than in the PECVD film. The presence of border traps is an unavoidable natural phenomenon as no dielectric film will ever be completely free of defects. However, this result shows that the problem of border charging in RF MEMS capacitive switches can be minimized if thermally-grown native oxides are incorporated into the device design. Different dielectric layers may then be deposited in the usual way on top of the native oxide to increase the breakdown field of the device. The fabrication and characterisation of these types of capacitive switches will be the subject of future work.

6.5.4 Electrical Solution to Bulk Charging

An alternative solution to the problem of bulk dielectric charging may exist through the use of bipolar actuation schemes. In Chapter 4, the bipolar hold-down method was shown to minimise the effects of dielectric charging in RF MEMS capacitive switches so that the effects of mechanical degradation could be studied in isolation. However, aside from showing evidence that the method was successful, no further tests were described to establish how the bipolar method minimised the amount of charge in the dielectric. Bipolar actuation schemes have previously been investigated by several authors [89, 90, 112, 151, 240] who proposed that the charge minimization ability of bipolar signals could be attributed to an equal and opposite amount of charging which takes place under the opposite polarity cycles of a bipolar signal [89, 90, 112], or to the equal charging and discharging of a dielectric under the alternating polarity voltage signals [151, 240]. However, no physical processes have been proposed to explain these theories.

In Chapter 5 the bias polarity-independent charging and discharging of border traps was shown to be responsible for the symmetric and recoverable dielectric charging of MIM and MEMS devices. It is believed that the same process is responsible for the charge-elimination ability of the bipolar hold-down method used in this work. To verify that this method can be used to solve bulk dielectric charging, an Al-Ti switch was held in the down-state for 24 hours using a ±15 V bipolar bias. Full C-V curves were measured at the beginning and end of the experiment and these are shown in Figure 6.13.

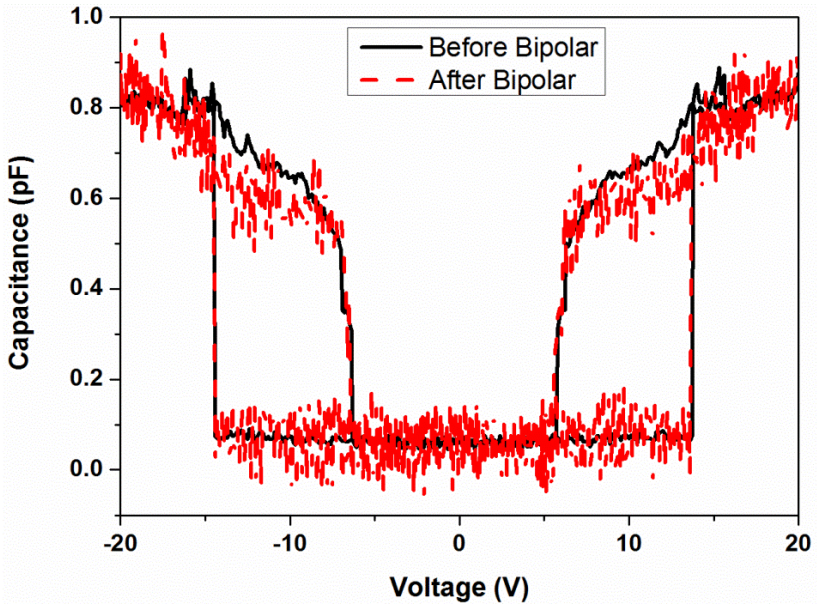

Figure 6.13: The C-V curves of an Al-Ti capacitive switch measured before (solid black line) and after (dashed red line) 24 hours of bipolar stress at ±15 V.

The C-V curve measured after 24 hours of bipolar stress was considerably noisier than the C-V curve measured at the beginning of the experiment. This may have been caused by movement of the electrical probes during the experiment which changed the calibration of the measurement setup. In spite of the decreased capacitance measurement sensitivity, the abrupt changes in capacitance due to the pull-in and pull-out phenomena could still be readily identified. From Figure 6.13 it can be seen that a maximum narrowing of 0.2 V was measured on the capacitive switch as a result of the long-term bipolar stress. This narrowing was asymmetric, which suggests that it may have arisen as a result of non-uniform dielectric charging during the stress time. However, the approximately-overlaid C-V characteristics of Figure 6.13 show that the switch was still functional after 24 hours of bipolar hold-down stress, which confirms that a 50% duty cycle bipolar signal can be used to minimise bulk dielectric charging in RF MEMS capacitive switches with SiO_2 dielectrics. An investigation into the remaining C-V narrowing and the applicability of this method to other device architectures and dielectrics will be the subject of future work.

6.6 SUMMARY

This chapter has described the characterisation of dielectric charging at high electric fields in RF MEMS capacitive switches. Section 6.2 introduced the measurement and analysis methods which were used to characterise the effects of bulk and surface dielectric charging when both were simultaneously present in a switch. In Section 6.3 the simultaneous presence of two different charge polarities was shown to cause narrowing of the C-V curve in proportion to the magnitude of the applied bias. In Section 6.4 the steady-state C-V shift of capacitive switches was used to study the effects of surface charging in isolation once sufficient time had been allowed for bulk charge to recover. This steady-state analysis technique was used to characterise several test structures which were designed to reduce the effects of surface charging by modifying the electric field and trap density present at the top dielectric surface. While these structures did not eliminate the effects of surface charging, it was found that the composition of the top and bottom dielectric surfaces had a strong influence on the amount of negative and positive surface charging taking place in a capacitive switch.

Analysis of the transient pull-in and pull-out voltage changes of capacitive switches allowed the voltage-dependence of C-V narrowing as a result of non-uniform dielectric charging to be identified for the first time. The recoverable nature of the narrowing effect identified non-uniform bulk dielectric charging as the most likely cause of C-V narrowing and an

investigation into methods of minimising or eliminating bulk dielectric charging in capacitive switches was described in Section 6.5. The border trapping phenomenon had been identified as the physical process responsible for bulk charging in Chapter 5. Through an investigation of several fabrication techniques designed to minimise the effects of border traps in MOS devices, it was found that the growth of native oxides on the bottom electrode of MEMS switches significantly reduced the density of border traps at this interface. Additionally, the bipolar hold-down method was shown to be an electrical solution to bulk dielectric charging in switches with SiO_2 dielectrics.

CHAPTER 7:

CONCLUSIONS & FUTURE WORK

The 2013 ITRS roadmap on MEMS technology states that there is a continuing need to extend the knowledge of the physics of failure in RF MEMS capacitive switches. The lack of understanding of the physical processes responsible for material degradation is a major contributing factor to the delayed commercialisation and widespread use of this technology. Therefore, the main goal of this thesis was to contribute to the state-of-the-art understanding of RF MEMS reliability through the characterisation of individual degradation mechanisms in fully-processed capacitive switches. Throughout this work it has been shown how changes in the C-V curve of capacitive switches can be related to the degradation of material properties and subsequently to the physical processes responsible for material degradation. Substantial progress has been made in identifying the physical processes which cause switch degradation and failure and the results achieved so far are summarised in this chapter.

7.1 THESIS SUMMARY

Chapter 1 briefly introduced MEMS technology and described the motivation for research into RF MEMS switches in particular.

Chapter 2 provided a more detailed description of RF MEMS switches and explained the fabrication and theory of operation of capacitive switches. Equations for the pull-in and pull-out voltages were derived and these operational parameters were highlighted as important tools for the characterisation of switch reliability. A brief introduction was given to the area of RF MEMS capacitive switch reliability and it was shown that while some devices have achieved commercial success, the degradation of material properties during hold-down operation continues to be a limiting reliability concern of capacitive switches. In particular, it was shown how high-performance switches can only be realised once the problem of dielectric charging has been addressed.

Chapter 3 described the failure mechanisms of stiction and screening which limit the lifetime of capacitive switches during hold-down operation. Various modelling approaches were used to show how the measurable effects of C-V shift and narrowing can be related to

the degradation of switch material. The difficulty associated with isolating either of these effects when both occur simultaneously was highlighted as the primary reason for the failure to identify any physical processes responsible for material degradation in RF MEMS capacitive switches during hold-down operation. Following this, several state-of-the-art research methods designed to isolate individual degradation mechanisms were discussed. Finally, the research methodology used in this thesis to isolate and identify the different degradation mechanisms was described.

Chapter 4 introduced the bipolar hold-down mechanical stress method which was used to remove dielectric charging and thereby isolate mechanical degradation in RF MEMS capacitive switches. Several tests were described which proved the validity of this method and which identified mechanical degradation as the primary degradation mechanism of aluminium switches. The degradation of aluminium switches was examined to characterise the different mechanical degradation mechanisms which were present and this resulted in the first identification of linear viscoelasticity due to grain boundary sliding in RF MEMS capacitive switches. This was identified by saturating the permanent creep effect using repeated hold-down stress experiments. Finally, a new aluminium-titanium alloy was investigated as a material solution to the problem of mechanical degradation in MEMS switches. Characterisation of this alloy showed that it was considerably more robust than either of the aluminium or titanium switch technologies which preceded it.

In **Chapter 5** an investigation of dielectric charging was undertaken on mechanically robust Al-Ti capacitive switches. The isolated study of dielectric charging allowed two different types of charge to be identified which affected the bulk and surface of the dielectric, respectively. MIM devices were selected for a study of bulk charging effects across metal/dielectric interfaces. Transient charging and discharging currents were measured and the voltage- and temperature-dependence of these currents was used to identify the transient stress-induced leakage current as the charging mechanism of MIM devices. The theory behind this reliability concern indicated that border traps located near the metal/dielectric interfaces were responsible for the observed charging behaviour. Using an original model, it was confirmed that the charging and discharging of border traps was the physical process responsible for the reversible C-V shifts measured in MEMS devices at low electric field levels.

Chapter 6 described the results of an investigation into dielectric charging at high electric fields in RF MEMS capacitive switches. A new stress and measurement technique was used to characterise the effects of dielectric charging when two types of charge with opposite polarities were simultaneously present in a capacitive switch. Transient voltage-dependent C-V narrowing was observed which was related to non-uniform bulk dielectric charging, while the steady-state C-V shift at the end of the recovery time was used to characterise the effects of surface charging. Using this method, the charging characteristics of three different test structures were compared and the influential role of the top and bottom dielectric interfaces on positive and negative surface charging was identified. Additionally, several methods of reducing bulk dielectric charging were investigated and it was found that the incorporation of native oxide layers on top of the bottom electrode was the most effective method of minimising the amount of border traps in RF MEMS capacitive switches, while bipolar hold-down schemes can provide an electrical solution to bulk charging at low electric field levels.

Finally, **Chapter 7** summarises the work that has been performed in this thesis. Several important conclusions are drawn based on these results, and some possible directions for future work are discussed.

7.2 CONCLUSIONS

Several contributions to the state-of-the-art understanding of RF MEMS capacitive switch reliability have been made in this work. These include the identification of grain boundary sliding in thin aluminium films as the physical mechanism responsible for switch mechanical degradation and the identification of border trap charging in silicon dioxide as the physical mechanism responsible for the switch degradation due to dielectric charging. Novel material solutions have been also been proposed to mitigate these concerns.

This work has shown for the first time that the physical processes responsible for degradation in RF MEMS capacitive switches can be identified through an isolated study of individual reliability concerns. It has been shown that bipolar voltages can be used to minimise the effects of dielectric charging so that mechanical degradation can be studied in isolation. In mechanically-robust capacitive switches, it has been shown that bulk and surface dielectric charging can be isolated by studying their transient C-V shift effects over a range of electric field conditions.

As a result of the structured approach to isolating different degradation mechanisms used in this thesis, grain boundary sliding leading to permanent and recoverable material deformation has been identified as the physical process responsible for mechanical degradation in aluminium-based switches. Plastic deformation caused by the creep effect leads to a cumulative permanent change in the switch characteristics, while the viscoelastic effect leads to a transient and recoverable deformation. Both effects can be mitigated if the membrane material is fabricated using the new aluminium-titanium (Al-Ti) alloy which was shown to be mechanically-robust.

In mechanically-robust Al-Ti capacitive switches, the charging and discharging of border traps located near the bottom metal-dielectric interface was identified as the physical process responsible for the dielectric charging effect. This process is responsible for the symmetric and recoverable shifts of switch characteristics measured at low electric fields. The growth of native oxide layers at this interface has been shown to be a promising material solution to the problem of bulk dielectric charging, while the charge-minimization ability of bipolar hold-down signals has also been shown to provide an electrical solution to this issue.

While the transient effects of surface charging could not be studied due to the simultaneous presence of bulk charging effects, tests on steady-state charging characteristics in structures with two dielectric layers allowed the influence of the top and bottom dielectrics on negative and positive surface charging to be observed. Based on this initial investigation, it was shown that a thin layer of aluminium oxide deposited on the top surface of the bottom dielectric can decrease the amount of negative surface charging, while a thicker top dielectric can reduce the amount of positive surface charging.

The results of this thesis have shown that once the underlying physical processes of switch reliability concerns are correctly identified, solutions in the form of novel materials or design changes can be developed. Therefore, it is believed that the most promising solution to improve the performance of capacitive switch technology is to use a dielectric-based architecture together with a stacked dielectric layer and mechanically robust metal, rather than removing the dielectric layer or reducing contact between the membrane and dielectric to improve device reliability due to charging effects as discussed in Chapter 2. A graphical representation of the improvements to Tyndall's capacitive switch design generated by this work is shown in Figure 7.1 where the Al_2O_3 layers have been deposited by thermal oxidation and atomic layer deposition, respectively.

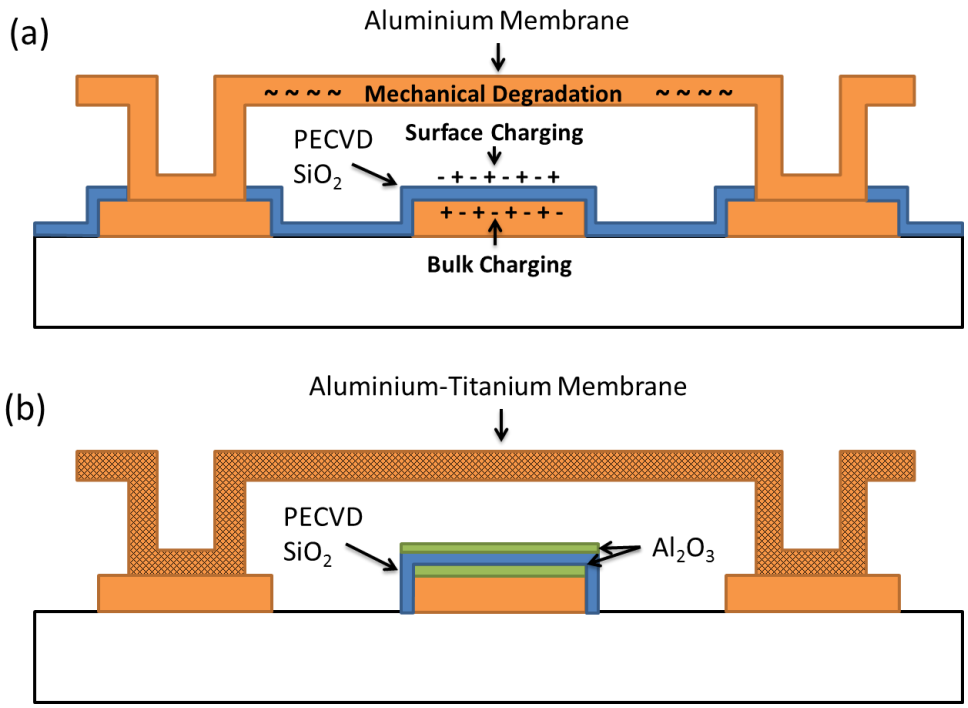

Figure 7.1: Graphical representation of the design and materials used in the fabrication of RF MEMS capacitive switches at the beginning (a) and end (b) of the research performed in this work.

In conclusion, the major goal of this research was to identify the physical processes responsible for reliability problems in RF MEMS capacitive switches and this has been achieved. The results presented in this thesis have been the first to identify the physical processes responsible for mechanical degradation and bulk dielectric charging in capacitive switches. These results validate the experimental methods and structured research approach used.

The advances in the state-of-the-art understanding of RF MEMS capacitive switch reliability contained in this thesis were achieved using simple experimental methods and analysis techniques which enabled standard C-V and I-t measurements to be used to characterise fully-functional capacitive switches. It is believed that the methodology used in this research can be replicated on other technologies with similar results provided care is taken to ensure that only one degradation mechanism is being measured at a time. Therefore, even though the results and analysis contained in this work have been measured on capacitive switch technology developed at Tyndall National Institute that use aluminium membranes and silicon dioxide dielectrics, it is believed that the measurement and analysis methods can be applied across the wider field of MEMS research.

7.3 FUTURE WORK

Although progress has been made in the identification and characterisation of the physical processes responsible for reliability problems in RF MEMS capacitive switches, more work is required to optimise the material solutions which have been proposed and to characterise them over a wider range of stress conditions.

The problem of mechanical degradation in RF MEMS capacitive switches has been mitigated by fabricating switch membranes using an aluminium-titanium alloy which was proven to be mechanically robust. However, the conductivity of this new alloy was found to be lower than the conductivity of pure aluminium which had been used previously, so that the electrical performance of these switches may be degraded by the increased resistivity of the metal. Therefore, further development is required to optimise the trade-off between the mechanical reliability and electrical performance of the Al-Ti alloy. This will involve the mechanical and electrical characterisation of Al-Ti test structures which will be fabricated using different amounts of titanium during the sputtering process.

By incorporating a thin native aluminium oxide layer on the top surface of the bottom electrode, it has been shown that bulk dielectric charging can be reduced in the switches investigated in this work. The native oxide devices which were tested in this work were designed to have a low pull-in voltage so that the charging properties of the native oxide layer could be tested without causing dielectric breakdown. However, while the low threshold voltages allowed low electric fields to be used, they also increased the fragility of the devices to degradation mechanisms which increased the failure rate. Therefore, by increasing the overall dielectric thickness, larger actuation voltages can be employed to investigate the border trap-reducing properties of the aluminium oxide layer while preserving the functionality of the switches. To achieve this, capacitive switches with a dielectric stack composed of thick PECVD silicon dioxide sandwiched between two thin layers of aluminium oxide will be investigated.

Following this, an investigation of surface dielectric charging will be performed on the next generation of capacitive switches fabricated using Al-Ti alloys and stacked dielectrics. Based on previous studies, it is expected that these new switches will exhibit increased reliability due to the elimination of mechanical degradation and bulk dielectric charging. Therefore, these devices will allow the transient effects of surface dielectric charging to be studied in isolation. Based on previous measurement results, it is believed that surface charging is caused by the injection and de-trapping of charge from the contacting dielectric

surfaces at the dielectric-air interface of a capacitive switch. Future work will investigate the physical processes responsible for surface charging under both stress polarities. Once the physical processes have been identified, material solutions to the problem of surface charging will be investigated. For example, the use of alternative dielectric materials on the top surface of the bottom dielectric and the inclusion of a thicker top dielectric have proven to be influential in the surface charging behaviour of capacitive switches. While the initial data was acquired in the presence of other degradation mechanisms, these material solutions will be investigated further once the effects of surface dielectric charging have been isolated.

After the investigation of surface charging effects, the reliability of RF MEMS capacitive switches should be characterised as a function of incident RF power and in radiation environments, as satellite applications represent a significant future market for these devices.

In summary, significant progress has been made in understanding the physics of reliability of RF MEMS capacitive switches in this work, and a direction for future research has been defined.

APPENDIX A:

LIST OF PUBLICATIONS ARISING FROM THIS WORK

JOURNAL PUBLICATIONS:

1. **C. Ryan**, Z. Olszewski, R. Houlihan, C. Mahony, and R. Duane, "A simple electrical test method to isolate viscoelasticity and creep in capacitive microelectromechanical switches," *Applied Physics Letters,* vol. 104, p. 061908, 2014.

2. **C. Ryan**, Z. Olszewski, R. Houlihan, C. O'Mahony, A. Blake, and R. Duane, "Identification of the transient stress-induced leakage current in silicon dioxide films for use in microelectromechanical systems capacitive switches," *Applied Physics Letters,* vol. 106, p. 172904, 2015.

3. Z. Olszewski, R. Houlihan, **C. Ryan**, C. O'Mahony, and R. Duane, "Experimental isolation of degradation mechanisms in capacitive microelectromechanical switches," *Applied Physics Letters,* vol. 100, pp. 233505-4, 2012.

4. C. O'Mahony, Z. Olszewski, R, Hill, R. Houlihan, **C. Ryan**, K. Rogers, C. Kelleher, R. Duane and M. Hill, "Reliability assessment of MEMS switches for space applications: laboratory and launch testing," *Journal of Micromechanics and Microengineering,* vol. 24, p. 125009, 2014.

CONFERENCE PUBLICATIONS:

1. **C. Ryan**, Z. Olszewski, R. Houlihan, C. O'Mahony, and R. Duane, "Design for Reliability in RF MEMS Capacitive Switches," presented at the Royal Irish Academy Wireless Research Colloquium on Communications and Radio Science into the 21st Century, Dublin, Ireland, 2012.

2. **C. Ryan**, Z. Olszewski, R. Houlihan, C. O'Mahony, and R. Duane, "Capacitive Microelectromechanical Switch for Space Applications," presented at the Radiation and Dosimetry in Various Fields of Research, Nis, Serbia, 2012.

3. **C. Ryan**, Z. Olszewski, R. Houlihan, C. O'Mahony, and R. Duane, "Comparison of Tether Designs for Reliable Operation of RF MEMS Capacitive Switches," presented at the 24th Micromechanics and Microsystems Europe, Espoo, Finland, 2013.

4. **C. Ryan**, Z. Olszewski, R. Houlihan, C. O'Mahony, A. Blake, and R. Duane, "Dielectric Charging at Low Fields in RF MEMS Capacitive Switches," presented at the WODIM 2014, The 18th Workshop on Dielectrics in Microelectronics, Kinsale, Ireland, 2014.

5. **C. Ryan**, Z. Olszewski, R. Houlihan, C. O'Mahony, A. Blake, and R. Duane, "Investigation of Bipolar Dielectric Charging in RF MEMS Capacitive Switches," presented at the MEMSWAVE 2014, La Rochelle, France, 2014.

6. Z. Olszewski, **C. Ryan**, R. Houlihan, C. O'Mahony, and R. Duane, "MEMS capacitive switch with a stable actuation voltage over a broad temperature range," in *Design, Test, Integration & Packaging of MEMS/MOEMS, DTIP*, Cannes, France, 2012.

7. C. O'Mahony, Z. Olszewski, R. Houlihan, **C. Ryan**, and R. Duane, "From Substrate to Space: Packaging and Deployment of RF MEMS Switches for Satellite Applications," presented at the 24th Micromechanics and Microsystems Europe, Espoo, Finland, 2013.

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