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Authors	Long, Brenda;Alessio Verni, Giuseppe;O'Connell, John;Shayesteh, Maryam;Gangnaik, Anushka S.;Georgiev, Yordan M.;Carolan, Patrick B.;O'Connell, Dan;Kuhn, K. J.;Clendenning, Scott B.;Nagle, Roger E.;Duffy, Ray;Holmes, Justin D.
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Doping Top-down e-Beam Fabricated Germanium Nanowires Using Molecular Monolayers

B. Long,[a,b,c] G. Alessio Verni,[a,b] J. O'Connell, [a,b] M. Shayesteh,[a] A. Gangnaik,[a,b] Y. M. Georgiev,[a,b] P. Carolan,[a] D. O'Connell,[a] K. J. Kuhn,[d,e] S. B. Clendenning,[e] R. Nagle,[a] R. Duffy,[a] and J. D. Holmes.[a,b,c]*

[a]Tyndall National Institute, University College Cork, Lee Maltings, Dyke Parade, Cork, Ireland,

[b]Materials Chemistry & Analysis Group, Department of Chemistry, University College Cork,

[c]Advanced Materials and BioEngineering Research (AMBER), Trinity College Dublin, Dublin 2, Ireland,

[d]Currently Department of Materials Science and Engineering, Cornell University, Ithaca, NY, USA.

[e]Components Research, Intel Corporation, Hillsboro, Oregon, USA.

[*]correspondence to: brenda.long@ucc.ie

KEYWORDS: Molecular layer doping; nanowires, semiconductors; germanium; conformal; non-destructive.

ABSTRACT

This paper describes molecular layer doping of Ge nanowires. Molecules containing dopant atoms are chemically bound to a germanium surface. Subsequent annealing enables the dopant atoms from the surface bound molecules to diffuse into the underlying substrate. Electrical and material characterization was carried out, including an assessment of the Ge surface, carrier concentrations and crystal quality. Significantly, the intrinsic resistance of Ge nanowires with widths down to 30 nm, doped using MLD, was found to decrease by several orders of magnitude.

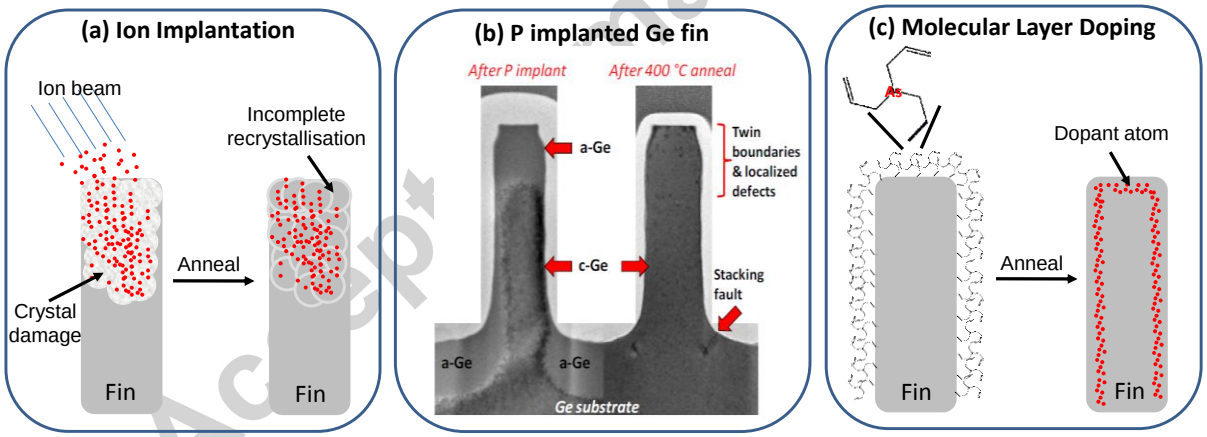
INTRODUCTION

State-of-the-art microprocessors contain several billion transistors over a ~6 cm^2 area.[1] This enormous device density has been made possible by continuous transistor scaling. However, in the last 10 to 15 years issues, such as increased leakage current, directly related to device scaling, [2] have necessitated radical changes in fabrication procedures, one of which has been the need to transition from planar to non-planar device architectures.[3]

Traditional architectures, with planar bulk substrates and highly doped channels for short-channel-effect control became problematic due to scaling, necessitating the development of non-planar devices (*e.g.* multigate FETs such as FinFETs). These architectures enabled better switching control, minimizing leakage current issues. Unfortunately, standard industrial techniques for doping, *e.g.* ion implantation, were designed for the former.[4] Doping, or the introduction of impurity atoms, a fundamental process step in the fabrication of integrated circuits, allows tuning of the electrical properties of the semiconductor material. Ion implantation, however, is destructive to the crystal structure of the semiconductor and too mono-

directional for modern device architectures. These problems are depicted graphically in Scheme 1(a). A TEM cross-section of a Ge fin that has been implanted with P is shown in Scheme 1(b). Amorphisation of the crystal structure of the target substrate is normal after implantation but subsequent high temp annealing induces recrystallization. On planar substrates this was satisfactory however for non-planar device architectures, residual defects, such as twin boundaries, remain. Furthermore, as the fin width decreases further complete recrystallization, even with defects, will not be possible.[5]

Scheme 1. (a) Depiction of ion implantation and associated problems for small dimension fin structures, (b) cross sectional TEM of ion implanted Ge fin pre- and post-anneal indicating presence of residual defects in recrystallized structure and (c) depiction of MLD as a process that will overcome problems associated with ion implantation.



Molecular layer doping (MLD), pioneered by the Javey Group [6] has been shown to non-destructively dope planar Si substrates. Since then a number of III-V materials have been doped using molecular layers.[7-10] MLD is based on surface functionalization and has the potential for precise atomistic control of the dopant position and composition on the surface of a

semiconductor (as depicted in Scheme 1 (c)). Thermal decomposition of this molecular layer enables the freed-up dopant atoms to diffuse into the underlying semiconductor. Furthermore, minimal damage to the crystal structure of this substrate occurs, due to the gentle nature of the process.

As well as exploring new methods for doping, new materials with higher carrier mobilities than Si are also being investigated. To date improved performance has been achieved mostly through transistor scaling with the economic benefit of reusing existing infrastructure. For this trend to continue moving to a high carrier mobility material which can enable reduced power consumption (by delivering a fixed drive current and circuit speed at a reduced power supply voltage) is a priority. Materials such as graphene,[11] transition metal dichalcogenides (TMDs) [12]and III-Vs [13] are being considered. Germanium (Ge), however, is a particularly attractive replacement for Si due to its enhanced electron and hole mobilities, and CMOS (complementary metal oxide semiconductor) compatibility, allowing Ge to be processed on existing Si technology platforms. Recent progress of ultra-shallow doping of n-type Ge using phosphorus has included several works using phosphine, as well as tunable δ-doping with near-monolayer P using P_2[14-18]. However these works were based on doping planar surfaces, and to the best of our knowledge were not yet transferred to nanowire device applications.

In general, processing and chemical techniques employed by Si are broadly transferrable to Ge, however, due to the unstable oxide of Ge, the surface chemistry is vastly more challenging. This study focuses on MLD of Ge with arsenic for a variety of reasons: 1) the relatively high equilibrium solubility of arsenic in Ge and 2) arsenic ability to in-diffuse in Ge. In this research, molecules containing arsenic were chemically bound in self-limiting monolayers to Ge surfaces resulting in doped substrates after annealing. Material characterization showed that the integrity

of the surface was maintained and the underlying crystal structure was not damaged, while electrical characterization showed several orders of magnitude decrease in resistance.

MATERIALS AND METHODS

All chemicals, purchased from Sigma-Aldrich were reagent grade and used as received. All experiments on unpatterned substrates were carried out on Ge(100) wafers purchased from Umicore, These substrates had p-type doping in the concentration range of 5-9 $\times$ 10^{16} at/cm^3. The nanowire samples were fabricated from undoped (100) germanium-on-insulator (GeOI), with a Ge thickness of 50 nm.

Material and Electrical Characterization: Atomic force microscopy (AFM) was implemented in tapping/non-contact mode at room temperature over a 3×3 μm scanning area. Cross-sectional transmission electron microscopy (TEM) was carried out using JEOL 2100 HRTEM operated at 200 kV. Cross-section samples were obtained by using FEI's Dual Beam Helios Nanolab system. For electrical characterisation Keithley 37100 and Keithley 2602 parameter analyser were used. Secondary ion mass spectrometry (SIMS) was performed on doped samples to obtain the total dopant concentration. SIMS analysis typically has a standard error of 20 % in concentration and a 10 % relative error from sample to sample. SIMS analysis was carried out on a CAMECA IMS 4FE6 system, available at the UMS-CNRS Castaing Characterization Centre in Toulouse. Electrochemical capacitance voltage (ECV) profiling was used to determine the active carrier concentration in doped samples, using thiron as the etchant. The technique uses an electrolyte-semiconductor Schottky contact to create a depletion region, which behaves like a capacitor. The measurement of the capacitance provides information of the electrically active

doping densities. Depth profiling is achieved by electrolytically etching the semiconductor between the capacitance measurements. The process is repeated for multiple steps, generating a carrier profile. It is a destructive technique, as there is a crater on the sample after the measurement is finished. No special test structure is required, it is performed on an unpatterned surface. For ECV data presented here, errors did not exceed 20 %. X-ray photoelectron spectroscopy (XPS) was carried out with a VG Scientific Escalab MKII system using Mg X-rays at 1253 eV. Survey scans were performed using a pass energy of 200 eV and core level scans at a pass energy of 20 eV.

MLD Procedure: Synthesis of triallyarsine (TAA) was carried out using a published procedure.[19] As TAA is a toxic material it should be handled with care using adequate PPE. Due to its unstable nature it must be stored in an inert atmosphere while minimizing its exposure to air during transfer.

Substrate Preparation: Ge was degreased by sonicating in acetone for 180 s, rinsed in IPA and dried under a stream of nitrogen, before being immersed in a 10 % HF solution for 10 min, removed and dried under a stream of nitrogen. Ge was prepared immediately prior to reaction with TAA to minimize any possible re-oxidation.

Reaction of TAA with Ge: A solution of TAA in IPA (1:5) was degassed using 3 × freeze/thaw cycles and transferred to a quartz flask containing the clean Ge substrate. The sample was irradiated for 2 h with UV light (λ = 254 nm) after which it was removed and rinsed several

times with IPA and acetone. All functionalization experiments were carried out in an inert atmosphere.

Capping Layer Deposition: SiO_2 capping layers were deposited used three different methods: 50 nm of oxide was sputtered, evaporated or deposited using CV538 +53D. The annealing step was carried out in the presence if these oxides, after which they were removed using a standard BOE etch.

GeOI Nanowire Fabrication and Doping: The procedure for the fabrication of GeOI nanowires was previously published.[7] GeOI nanowire samples was degreased and immersed in HBr (10 %) for 10 min to remove the native oxide and passivate with Br termination. The functionalization procedure was the same as for blanket samples. No capping layer was applied as removing it would damage the underlying oxide in the GeOI.

RESULTS AND DISCUSSION

MLD was first carried out on blanket samples as a number of our analysis techniques (e.g. AFM, ECV, SIMS) required large areas for analysis. Initial process parameters necessary to diffuse dopant atoms from molecules attached to the surface into the underlying Ge, were established before transferring the process to the nanowires.

A hydrogermylation reaction, developed by the Buriak Group[20] was used to chemically bind the arsenic-containing-molecule, triallylarsine (TAA), to the Ge surface forming a self-limiting monolayer that allows the number of dopant atoms exposed to the substrate to be controlled.

Based on a calculation where each TAA molecule occupies an ~1 nm^2 area and assuming the dopant depth is confined to 10 nm, doping levels as high as 10^{20} atoms/cm^3 can be delivered to the underlying substrate. As attractive feature of MLD is that the doping concentration can be fine-tuned by changing the size of the organic cage surrounding the dopant atom.

Initial studies focused on the annealing conditions required to diffuse dopant atoms from molecules attached to the surface into the substrate. Rapid thermal annealing (RTA) was employed to achieve this. The use of RTA required a thermal budget to be established where the aim is to maximize the concentration of dopant atoms while minimizing their diffusion depth. Initial thermal budgets employed were 650 °C for 60 s and 700 °C for 300 s. Data from these anneals were obtained from both electrochemical capacitance voltage (ECV) and secondary ion mass spectrometry (SIMS) profiling (Figure 1).

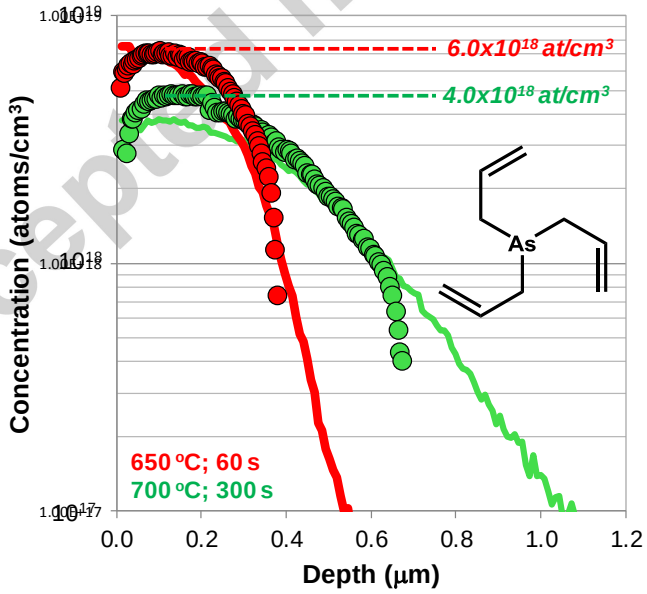


Figure 1: SIMS (solid line) versus ECV for carrier profiling of arsenic doped Ge performed by MLD. Rapid thermal annealing carried out using two thermal budgets as indicated.

ECV measures the active dopant concentration while SIMS measures the total dopant concentration. Interestingly, both ECV and SIMS gave the same dopant profiles within experimental error, suggesting that all the diffused dopant atoms have been activated.

The diffusion at 700 °C was considered too deep whilst at low annealing temperatures (*i.e.* 550 °C) significantly lower concentrations ($<10^{18}$ cm^{-3}) of the dopant atoms were incorporated into Ge. For these reasons, 650 °C was considered the optimal annealing temperature in our system. Further optimisation showed that annealing at 650 for 10 s gave best results.

Capping Layer: Traditional MLD processing uses a capping layer for the annealing step to prevent evaporation of the molecular layer. However, the nanowires for this study were fabricated on GeOI, therefore from a processing point of view it would be beneficial to avoid using a capping layer as the underlying GeOI oxide may be affected during capping layer removal. In this study silicon oxide (SiO_2) was deposited by three different methods onto the surface of TAA-functionalised Ge substrates. 50 nm of SiO_2 was deposited by 1) sputtering, 2) chemical vapour deposition (CVD) and 3) evaporation. A forth sample was processed alongside these where no capping layer was used. In all cases the samples were annealed for 10 s at 650 ^{o}C.

Figure 2 shows the data from the capping layer study. Evaporated SiO_2, known to be less dense and more porous, showed lower carrier concentrations when compared with either CVD deposited or sputtered SiO_2. Most interesting however was the sample with no capping layer, although the incorporated carrier concentration was less than for some of the capped samples, it

was still reasonable. Though there will be competition between the dopant atoms' diffusion into the underlying Ge v's evaporation into the chamber these results clearly shows the preference for the As to diffuse into the substrate. Hence, this data shows that it is possible to reduce the complexity of the MLD process, by reducing the number of steps required, *i.e.* no capping layer, which holds significant industrial value.

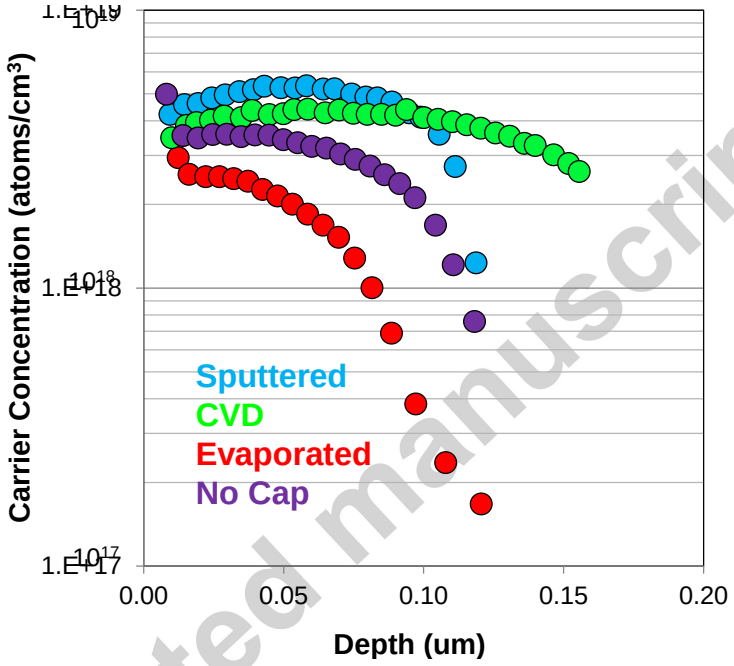


Figure 2: ECV results for samples with various (or no) SiO_2 capping layers. RTA was carried out for 1 s at 650 °C.

Reduced resistance in top-down GeOI Nanowires: In order to properly evaluate MLD-based doping process for nanowires, top-down patterned Ge nanowires were fabricated (three nanowires of each size ranging from 30 nm to 1000 nm in diameter were measured). The test structure used to electrically characterize the access resistance modification by MLD is shown in a representative SEM image as an inset in Figure 3. The device constructed was a four probe structure, with a user-defined current forced through the outer two electrodes, and the inner two electrodes used to sense the voltage drop across the nanowire.

The current in the nanowire was fixed, set by the test equipment. Electrodes were set to "sense" mode by defining them as a current source on the parameter analyser tool, with the current set to zero. There was no current flow into the sense electrodes, so there should be no voltage drop at those pads, and thus the voltage drop across the nanowire only can be extracted, as shown in Figure 3. There might be a voltage drop at the contact pads through which the current is forced, however because of the design of the test structure, any drop was filtered out. Representative current versus voltage characteristics are shown in Figure 3 for Ge nanowires with a range of widths. The current was found to be linearly dependent on the voltage and passed through the origin. As the nanowire width was scaled the current level dropped, as expected. Before the MLD process was applied to the nanowires, the current was in the pico-Amp range. Hence the MLD process has altered the resistance of the nanowires by several orders of magnitude.

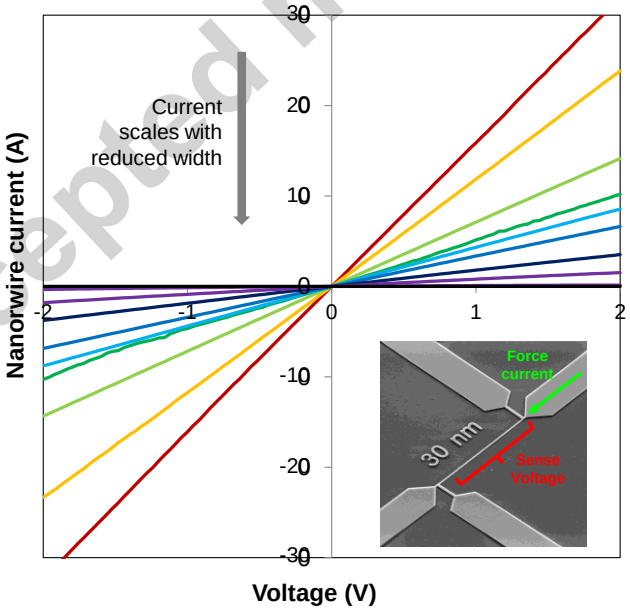


Figure 3: I-V data showing scaling of current with reduced width of nanowire. The inset shows the SEM of a 30 nm test structure.

TEM analysis of MLD-doped nanowires was performed to determine their crystal quality post-processing. Doping thin body semiconductors by conventional means, *i.e.* ion implantation, often leads to the formation of visible crystal defects such as twin boundary defects and stacking faults [5] usually easily detectable by TEM imaging. We don't wish to claim that post-MLD the semiconductor is entirely defect-free (many crystal defects are too small for this kind HR-TEM imaging), but we do wish to state the typical defects associated with impurity doping nanowires (e.g. {111}s, etc.) are not present, which in itself is an achievement.

Figure 4 (a) shows a TEM cross section of a 50 nm test structure while Figure 4(b) shows a high resolution image of a Ge nanowire post-MLD where the <111> and <100> directions are shown. The Fast Fourier Transform (FFT) shown in the inset of Figure 4(b) shows the highly crystalline nature of the nanowire, consistent with an absence of stacking fault and defects and consistent with the gentle nature of the MLD process.

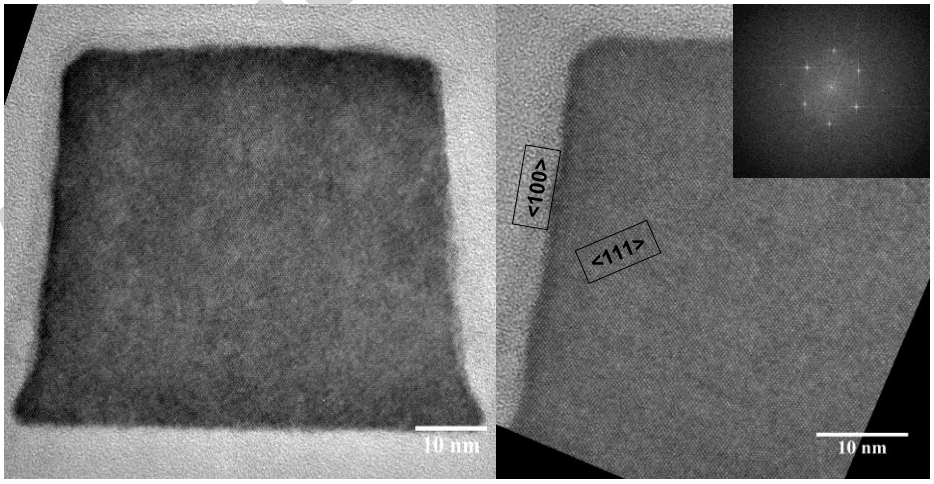


Figure 4 (a) TEM micrograph of a section of the 50 nm Ge nanowire test device, (b) Magnified HRTEM micrograph of the nanowire with the <111> and <100> directions indicated. The FFT shown in the inset of (b) shows the highly crystalline nature of the nanowire. There are no indications on either micrograph of any defects or damage to the crystal lattice.

CONCLUSIONS

This study reports the first demonstration of MLD of Ge nanowires. Doping levels of 6×10^{18} atoms/cm^3 were consistently achieved, but RTA was found to be a limiting factor in achieving carrier concentrations of $>10^{19}$ atoms/cm^3 in Ge. Future work will involve exploration of more advance annealing techniques such as laser and flashlamp annealing. This MLD procedure was transferred from blanket samples to GeOI nanowires with diameters down to 30 nm, where the resistance of the nanowires was reduced by several orders of magnitude. High resolution TEM analysis shows that there are no visible defects generated during this process. Furthermore, for the first time our study showed that even without a capping layer MLD of Ge was successful, an important consideration for application of this process in industry.

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