

Title	Inversion in the In _{0.53} Ga _{0.47} As metal-oxide-semiconductor system: Impact of the In _{0.53} Ga _{0.47} As doping concentration
Author(s)	O'Connor, Éamon; Cherkaoui, Karim; Monaghan, Scott; Sheehan, Brendan; Povey, Ian M.; Hurley, Paul K.
Publication date	2017-01-19
Original citation	O'Connor, É., Cherkaoui, K., Monaghan, S., Sheehan, B., Povey, I. M. and Hurley, P. K. (2017) 'Inversion in the In _{0.53} Ga _{0.47} As metal-oxide-semiconductor system: Impact of the In _{0.53} Ga _{0.47} As doping concentration', Applied Physics Letters, 110, 032902 (5pp). doi:10.1063/1.4973971
Type of publication	Article (peer-reviewed)
Link to publisher's version	http://dx.doi.org/10.1063/1.4973971 Access to the full text of the published version may require a subscription.
Rights	© 2017, the Authors. Reproduced with the permission of AIP Publishing from Applied Physics Letters, 110, 032902 (5pp). doi:10.1063/1.4973971 https://publishing.aip.org/authors/copyright-reuse
Item downloaded from	http://hdl.handle.net/10468/4021

Downloaded on 2018-04-24T08:31:37Z



UCC

University College Cork, Ireland
Coláiste na hOllscoile Corcaigh

Inversion in the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ Metal-Oxide-Semiconductor system:

impact of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ doping concentration

É. O'Connor, K. Cherkaoui, S. Monaghan, B. Sheehan, I. M. Povey, and P. K. Hurley.

¹*Tyndall National Institute, University College Cork, Cork, Ireland.*

E-mail address of corresponding author: eamonoconnor33@gmail.com

$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ metal-oxide-semiconductor (MOS) capacitors with Al_2O_3 gate oxide and a range of n and p -type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ epitaxial concentrations were examined. Multi-frequency capacitance-voltage and conductance-voltage characterization exhibited minority carrier responses consistent with surface inversion. The measured minimum capacitance at high frequency (1MHz) was in excellent agreement with the theoretical minimum capacitance calculated assuming an inverted surface. Minority carrier generation lifetimes, τ_g , extracted from experimentally measured transition frequencies, ω_m , using physics based a.c. simulations, demonstrated a reduction in τ_g with increasing epitaxial doping concentration. The frequency scaled conductance, G/ω , in strong inversion allowed the estimation of accurate C_{ox} values for these MOS devices.

Historically, a variety of issues have impeded progress for the incorporation of high- k dielectrics on III-V semiconductors for future CMOS applications.^{1,2} Not least among these is the complexity of the high- k III-V interface which typically has a high density of electrically active defects.^{3,4,5} Interface state density (D_{it}) values in excess of 10^{12}cm^{-2} are commonly reported which is almost two orders of magnitude higher than that achievable in SiO_2/Si systems. Passivation of these defects to acceptable levels has not proved to be trivial and also renders reliable characterization and interpretation of device behavior difficult.⁶ Such a high D_{it} can restrict Fermi level movement across the semiconductor bandgap and in the case of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, prevent surface inversion at the semiconductor/oxide interface. To date, only a limited number of studies in the literature have demonstrated sufficient reduction in D_{it} to allow the observation of true surface inversion and an associated minority carrier behavior, in the capacitance-voltage (CV) response of MOS capacitors on either n -type or p -type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$.^{7,}

^{8, 9, 10}

31 In recent work we reported on a study of the minority carrier response of both n -type and p -
32 type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ metal-oxide-semiconductor (MOS) devices formed using an optimized 10%
33 ammonium sulfide ($(\text{NH}_4)_2\text{S}$) treatment.⁷ D_{it} was sufficiently reduced such that a clear minority
34 carrier response associated with inversion of the oxide/ $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface was observed for
35 both n -type and p -type devices. In order to extend this work, in this letter we present a method to
36 confirm true surface inversion in $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors based on the use of a wide
37 range of n and p -type doping concentrations, ranging over two orders of magnitude from
38 $\sim 1 \times 10^{16} \text{ cm}^{-3}$ to $\sim 2 \times 10^{18} \text{ cm}^{-3}$. This is in order to examine if the measured minimum capacitance
39 scales correctly with the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ doping concentration based on a maximum depletion
40 width calculated assuming the surface is inverted. This follows an approach reported by
41 Callegari *et al* for GaAs MOS devices.¹¹ In addition the effect of the doping concentration on the
42 minority carrier generation lifetime in the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, τ_g , is examined. Finally, for these
43 variable doping series samples, we utilize a recently reported method¹² to accurately estimate
44 oxide capacitance, C_{ox} , where it was found that the peak magnitude of the angular frequency
45 scaled conductance, G/ω , was equal to $C_{ox}^2/2(C_{ox}+C_D)$, in strong inversion, where C_D is the
46 semiconductor depletion capacitance.

47 The details of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ epitaxial layers used in this work are as follows. Firstly,
48 using p -doped (Zn at $\sim 2 \times 10^{18} \text{ cm}^{-3}$) $\text{InP}(100)$ as a starting substrate, $\sim 2 \mu\text{m}$ p - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layers
49 were grown by MOVPE with the following dopant (Zn) concentrations (cm^{-3}): 1.4×10^{16} ,
50 3.3×10^{16} , 1.8×10^{17} , 2.7×10^{17} , and 2.0×10^{18} . Using n -doped (S at $\sim 2 \times 10^{18} \text{ cm}^{-3}$) $\text{InP}(100)$ as a
51 starting substrate, $\sim 2 \mu\text{m}$ n - $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layers were grown by MOVPE with the following
52 dopant (Si) concentrations (cm^{-3}): 7.8×10^{15} , 3.0×10^{16} , 2.0×10^{17} , 6.0×10^{17} , and 2.0×10^{18} . These
53 doping concentrations were determined by Electrochemical Capacitance-Voltage (ECV)
54 Profiling. $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surfaces were initially rinsed for 1 minute each in acetone, methanol,
55 and isopropanol, immediately followed by immersion for 20 minutes at room temperature in
56 $(\text{NH}_4)_2\text{S}$ with a concentration of 10% in deionised H_2O . These optimized passivation parameters
57 were determined from previous physical and electrical studies^{13,14} and subsequently also reported
58 for MOSFET devices.¹⁵ The Al_2O_3 layers were grown by atomic layer deposition (ALD) at
59 300°C (Cambridge NanoTech, Fiji F200LLC), using alternating pulses of TMA ($\text{Al}(\text{CH}_3)_3$) and
60 H_2O . TEM indicated an Al_2O_3 thickness of $\sim 7 \text{ nm}$ for the growth run on p -type samples and a
61 thickness of $\sim 5 \text{ nm}$ for the separate ALD growth run on n -type samples. Finally, gate contacts \sim

62 160 nm thick were formed by e-beam evaporation of Ni (70nm), and Au (90nm), using a lift-off
 63 process. Electrical measurements were recorded using an Agilent E4980A, and were performed
 64 on-wafer in a microchamber probe station (Cascade, Summit 12971B) in a dry air, dark
 65 environment (dew point $\leq 203\text{K}$).

66 For an MOS device in strong inversion the depletion layer width reaches a maximum
 67 value, which is related to the doping concentration and the relative permittivity of the
 68 semiconductor.¹⁶ The equation governing the maximum depletion width, included here for
 69 completeness, is given in Equation [1] below where: ϵ_0 is the permittivity of free space; ϵ_s is the
 70 semiconductor permittivity; k is Boltzmann's constant; n_i is the intrinsic semiconductor carrier
 71 concentration; N_D is the semiconductor doping concentration.¹⁷

$$72 \quad x_{d_max} = \sqrt{\frac{4\epsilon_0\epsilon_s kT \ln(N_D/n_i)}{q^2 N_D}} \quad [1]$$

73 From this equation, as the semiconductor doping level is increased this maximum depletion
 74 width is reduced, which in turn is reflected in an increase in the depletion capacitance (C_D) of the
 75 semiconductor in inversion. The theoretical minimum capacitance ($C_{\text{min-theor}}$) of a gate stack is
 76 the series combination of C_D and C_{ox} . It is thus expected that for an inverted surface, the
 77 minimum measured gate stack capacitance ($C_{\text{min-meas}}$) will increase as a function of doping
 78 concentration. Utilizing different doping concentrations $C_{\text{min-meas}}$ at high frequency can be
 79 compared with $C_{\text{min-theor}}$ as calculated by assuming the semiconductor surface is inverted. In the
 80 case of devices where the D_{it} is high, Fermi level movement will be restricted such that it will not
 81 be possible to reach the minimum capacitance. Where substrates with variable doping levels are
 82 available this provides a means to investigate if the oxide-semiconductor interface state
 83 concentration has been reduced to levels which allow surface inversion to be achieved. This
 84 approach was used previously for GaAs MOS structures to investigate improvements in the CV
 85 characteristics of plasma deposited Ga oxide films on GaAs substrates.¹¹

86 Figure 1(a) plots the 1 MHz CV responses for the p -type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS devices with
 87 varying dopant concentrations. The 1 MHz curves were chosen in order to minimize any
 88 contribution of interface states to the measured CV response. Open symbols represent $C_{\text{min-theor}}$
 89 for each doping concentration and calculated using a C_{ox} value in this case of 0.0075 F/m^2 , taken

90 from the measured capacitance at low frequency (20 Hz), and at a gate bias of 1.75V. C_{ox} was
91 chosen at 20Hz as this was the lowest frequency that could be measured with the instrument
92 used, and previous work has shown that the CV at 20Hz provides a very close approximation to
93 the C_{ox} obtained using a quasi-static CV.¹⁸ It is clear that the measured minimum capacitance
94 increases as expected with doping and that there is excellent agreement between the measured
95 and theoretical minimum capacitance values, providing strong evidence that the $In_{0.53}Ga_{0.47}As$
96 surface is inverted. This is notable considering that the change in doping concentration is over
97 two orders of magnitude. It is also significant that the measured CV curves go flat with
98 increasing positive gate bias, which is further support that D_{it} has been reduced to an extent to
99 allow sufficient Fermi level movement that permits surface inversion. Figure 1(b) shows the 1
100 MHz CV responses for the n -type $In_{0.53}Ga_{0.47}As$ MOS devices with changing epitaxial layer
101 dopant concentrations. As in the case of the p -type samples, there is excellent agreement between
102 the measured (open symbols) and theoretical (closed symbols) capacitance values. The
103 theoretical minimum capacitance, $C_{min-theor}$, for each doping concentration was calculated using a
104 C_{ox} value in this case of 0.0093 F/m^2 , taken from the capacitance measured at low frequency
105 (20Hz), and at a gate bias of -3.75V. When plotting the measured capacitance versus the
106 theoretical value, (@1.75 V_{gate} for p -type and at @-3.75 V_{gate} for n -type), Figure 2 demonstrates
107 that there is close to a linear relationship in both cases. The inversion of the n -type $In_{0.53}Ga_{0.47}As$
108 MOS is of particular note, as for the $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS system the interface state density
109 is generally reported to rise steeply towards the valence band edge,^{19,20,21} and the ability to invert
110 the Al_2O_3/n - $InGaAs$ surface indicates that the surface preparation and ALD growth conditions
111 have not only reduced D_{it} near the mid gap energy, but also results in D_{it} reduction from mid-gap
112 to the valence band edge.

113 For all samples the multi-frequency CV and GV responses (20 Hz to 1 MHz) also exhibited the
114 characteristic signatures of inversion behavior for $In_{0.53}Ga_{0.47}As$ MOS devices.⁷ As an example
115 illustration the CVs in Figure 3(a) and (b) are plotted for the devices in this study ($1.8 \times 10^{17} \text{ } p$ -
116 type and $6.0 \times 10^{17} \text{ } n$ -type) having doping levels similar to those used in previous reports on
117 inverted $In_{0.53}Ga_{0.47}As$ MOS devices, in order to show the behavior is consistent.^{7,22} Space
118 limitations preclude showing the multi-frequency CV for all samples. One of the signatures for
119 an inverted surface is that in strong inversion the measured conductance normalized by

120 frequency, G/ω , peaks at the transition frequency, ω_m .^{7,12,23} This relationship is observed for all
121 samples in the study (not shown).

122 For an inverted surface the multi-frequency C-V and G-V responses can also be used to
123 investigate the minority carrier lifetime in the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer and the capacitance of the gate
124 oxide.^{12,22} For the case of surface inversion, the transition frequency, ω_m , is inversely related to
125 the minority carrier generation lifetime, τ_g , in the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, and the peak value of G/ω is
126 related to the oxide capacitance, C_{ox} . Considering firstly the case of the minority carrier lifetime,
127 the G/ω recorded at a gate bias of $1.75 V_{\text{gate}}$ for p -type and at $-3.75V_{\text{gate}}$ for n -type are plotted in
128 Figure 4. One observation of note over both n and p -type samples in Figure 4 is that the
129 transition frequency at which G/ω peaks in inversion increases as the semiconductor doping
130 concentration is increased. Figure 5(a) plots this change for p -type and n -type devices. For a
131 minority carrier supply provided through mid-gap state generation, this behavior is expected as
132 the minority carrier lifetime τ_g values generally decrease with increasing doping concentration.
133 These observations are therefore consistent with previous work on similar device structures
134 indicating that at room temperature the dominant mechanism for the supply of minority carriers
135 is a generation-recombination process through mid-gap bulk defects in the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$
136 depletion region.⁷ These results are not consistent with a border trap²⁴ contribution to the
137 observed minority carrier response. The results in Figure 5(a) also indicate that at similar doping
138 levels the transition frequency for the n -type samples is generally one order of magnitude higher
139 than for the corresponding p -type samples.

140 A Synopsis Sentaurus device simulator was employed to perform physics based ac simulations,
141 where the value of τ_g in the simulations is altered to achieve a match between the transition
142 frequency of the physics based ac simulations and the experimental transition frequency values
143 in Figure 5(a). The resulting τ_g are plotted in Figure 5(b) demonstrating a marked decrease with
144 increasing doping concentration for both n and p -type devices. The fact that higher generation
145 lifetimes at similar doping levels are observed for p -type compared to n -type samples is possibly
146 related to inequalities in the bulk $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ properties arising from differences in the
147 epitaxial growth conditions for the p and n -type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layers. However, further analysis
148 of this is beyond the scope of the current study. Previous work also demonstrated that it is
149 possible to passivate some of the bulk mid-gap traps in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ through H_2/N_2 annealing,

150 as indicated by an increase in τ_g .^{22,25} It is noted that all samples in each doping series in this work
151 were processed simultaneously with the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ surface seeing identical conditions and
152 therefore should have comparable D_{it} . Interface states do not contribute to the observed minority
153 carrier response because in strong inversion interface states are either full (p -type) or empty (n -
154 type). Therefore changes in surface potential arising from modulation of the small signal a.c.
155 voltage applied to the gate will not significantly affect their occupancy.²²

156 C_{ox} is an important parameter in device analysis, for example with regard to D_{it} extraction.
157 These doping series samples can also be utilized with regard to the C_{ox} extraction method we
158 published recently,¹² where it was demonstrated that in strong inversion the maximum value of
159 G/ω at ω_m is equal to $C_{ox}^2/2(C_{ox}+C_D)$. In the current study the oxide thickness is fixed while the
160 doping concentration is varied. Therefore, for a given C_{ox} , as doping concentration increases, C_D
161 will increase and it would be expected using the above relationship that the value of G/ω would
162 decrease. Figure 6 plots the expected theoretical values of G/ω versus doping, for various values
163 of C_{ox} . The measured G/ω values are plotted as open symbols, with the dashed blue lines
164 representing an approximate fitting to those points in each case. It is seen that the experimental
165 values follow the trend of the theoretical values quite closely. In Figure 6 (a) it is evident that the
166 curve calculated using C_{ox} of 0.0075 F/m^2 is in very good agreement with the experimental G/ω
167 data. In the case of the n -type devices the 0.0093 F/m^2 for C_{ox} provides a good approximation
168 over most of the doping range, although some deviation is observed in the experimental data for
169 the two highest doping concentrations. These observations are important also in validating the
170 calculations of the theoretical minimum capacitances described earlier in regard to Figure 1 and
171 2, where the C_{ox} values used to extract the theoretical minimum capacitances were 0.0075 F/m^2
172 and 0.0093 F/m^2 for p -type and n -type samples respectively, determined from the measured
173 capacitance at 20Hz. Therefore the C_{ox} values that provide the best fit in both n and p -type cases
174 in Figure 6 are in agreement with the C_{ox} measured at low frequency (20Hz).

175 In summary, p -type and n -type $\text{Au/Ni/Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors with
176 semiconductor doping concentrations ranging from 10^{16}cm^{-3} to 10^{18}cm^{-3} exhibited behavior
177 consistent with surface inversion. The measured minimum capacitance at 1 MHz scales correctly
178 with the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ doping concentration based on a maximum depletion width calculated
179 assuming the surface is inverted, providing evidence that the interface state concentration was

180 reduced to a level which allows inversion of the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interface for both n and p
181 type doped $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. The minority carrier generation lifetime in the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, τ_g , was
182 found to decrease with increasing doping concentration. C_{ox} values extracted using a method
183 based on the relationship between the capacitance and conductance in strong inversion exhibited
184 excellent agreement with the C_{ox} measured at low frequency (20 Hz). It is notable that this was
185 illustrated previously using an Al_2O_3 thickness series on both n and p -type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ in
186 which case the doping was fixed and C_{ox} varied with dielectric thickness²², and also that results
187 from physics based a.c simulations show the relationship to be generally true.¹² Those results,
188 combined with the results of this variable doping study, indicate that the equality of the
189 maximum value of G/ω at ω_m being equal to $C_{\text{ox}}^2/2(C_{\text{ox}}+C_D)$ in inversion, is a reliable tool to
190 obtain an accurate estimate of C_{ox} , and most significantly that this method can be applied for any
191 MOS system in inversion, regardless of the oxide or semiconductor material.

192

193 The authors acknowledge the following colleagues from Tyndall National Institute for their
194 contribution: Dr. Kevin Thomas and Dr. Emanuele Pelucchi for MOVPE growth; Dr. Pat
195 Carolan for TEM analysis, and Dan O’Connell for lithography and gate metallization. The
196 authors acknowledge Dr. Rafael Rios (retired) formerly of Intel Components Research, Oregon,
197 for providing the physics based CV simulations. This work was supported in part by Science
198 Foundation Ireland under the “INVENT” project 09/IN.1/I2633; and in part by the European
199 Commission through the project entitled “Compound Semiconductors for 3D Integration
200 COMPOSE3” under Grant FP7-ICT-2013-11-619325; and the project entitled “Integration of III-
201 V Nanowire Semiconductors for Next Generation High Performance CMOS SOC Technologies,
202 (INSIGHT)” under Grant H2020-ICT-2015-688784. É. O’Connor acknowledges the financial
203 support of the European Union funded Marie Curie fellowship “FACIT” (FP7-PEOPLE-2013-
204 IEF 628523).

205

206

207 Figure 1. 1MHz CV responses at 295K for (a) Au/Ni/7nm-Al₂O₃/*p*-In_{0.53}Ga_{0.47}As and (b)
208 Au/Ni/5nm-Al₂O₃/*n*-In_{0.53}Ga_{0.47}As MOS devices with dopant concentrations ranging from ~ 10¹⁶
209 cm⁻³ to 10¹⁸ cm⁻³. The theoretical values (open symbols) were estimated using a C_{ox} value of
210 0.0075 F/m², and 0.0093 F/m² for the *p*- and *n*-type devices respectively.

211

212 Figure 2. Plot of measured versus theoretical minimum capacitance for: (a) different *p*-type
213 doping concentrations, with the measured values being those at a gate bias of 1.75 V in Fig. 1(a);
214 and (b) different *n*-type doping concentrations, with the measured values being those at a gate
215 bias of -3.75 V in Figure 1(b).

216

217 Figure 3: Multi-frequency CV responses at 295K of (a) *p*-type and (b) *n*-type
218 Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As, devices, with In_{0.53}Ga_{0.47}As doping concentrations of 2.7x10¹⁷ cm⁻³
219 and 6.0x10¹⁷ cm⁻³, and Al₂O₃ thicknesses of ~ 7 nm and 5 nm, respectively. The CV responses
220 with increasing positive gate bias for the *p*-type devices, and with increasing negative gate bias
221 for the *n*-type devices, are consistent with the CV behavior arising from a minority carrier
222 response in inversion.

223

224 Figure 4. G_m/ω plotted versus ω in strong inversion for (a) Au/Ni/7nm Al₂O₃/*p*-In_{0.53}Ga_{0.47}As,
225 and (b) Au/Ni/5nm Al₂O₃/*n*-In_{0.53}Ga_{0.47}As devices. The values of G/ω were taken at a gate bias
226 of 1.75 V for *p*-In_{0.53}Ga_{0.47}As devices and at a gate bias of -3.75 V for *n*-In_{0.53}Ga_{0.47}As devices,
227 utilizing the multi-frequency GV data. Note, the frequency scaled conductance, G/ω, can also be
228 expressed in units of F/m².

229

230 Figure 5. (a) Increase in transition frequency, ω_m, as a function of In_{0.53}Ga_{0.47}As doping
231 concentration for *p*-type (star) and *n*-type (circle) MOS devices. (b) Decrease in the minority

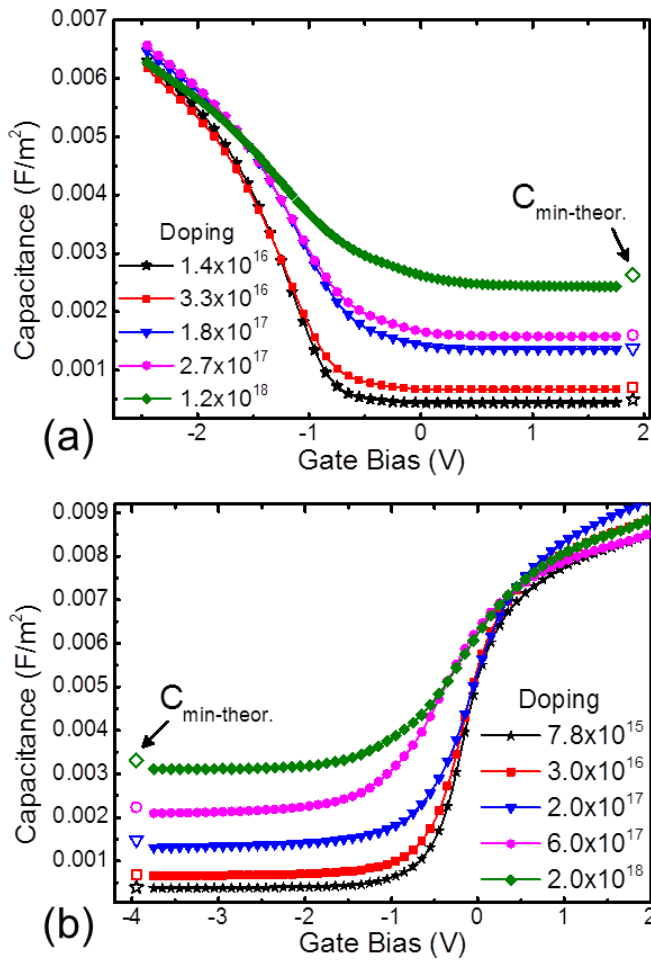
232 carrier generation lifetime, τ_g , with increasing doping for p -type (star) and n -type (circle) MOS
 233 devices.

234

235 Figure 6. Peak G/ω in inversion as a function of doping concentration for (a) p -type and (b) n -
 236 type Au/Ni/Al₂O₃/In_{0.53}Ga_{0.47}As devices. Different C_{ox} values were used to compute the
 237 corresponding theoretical G/ω values at each doping level according to the
 238 $(G/\omega)_{max}=C_{ox}^2/2(C_{ox}+C_D)$ relationship. The measured peak G/ω values in strong inversion are
 239 plotted as open symbols, and fitted with the dashed line. Note, the frequency scaled conductance,
 240 G/ω , can also be expressed in units of F/m².

241

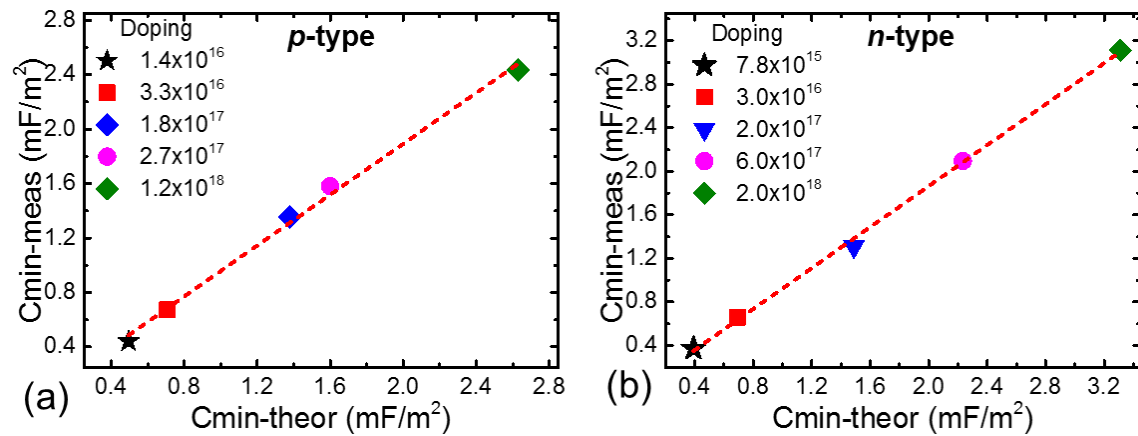
242 Figure 1



243

244

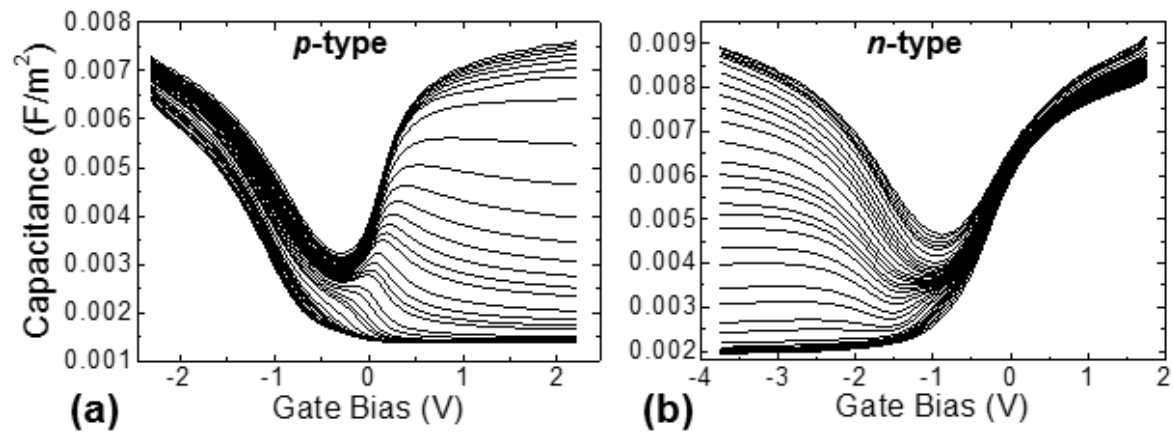
245 Figure 2



246

247

248 Figure 3



249

250

251

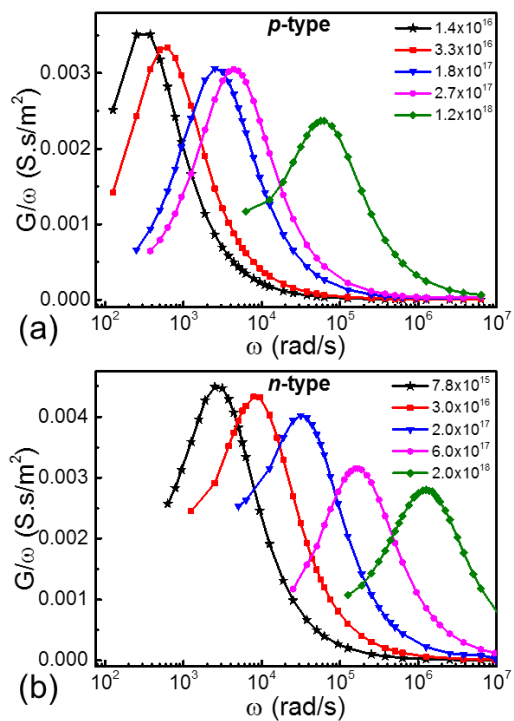
252

253

254

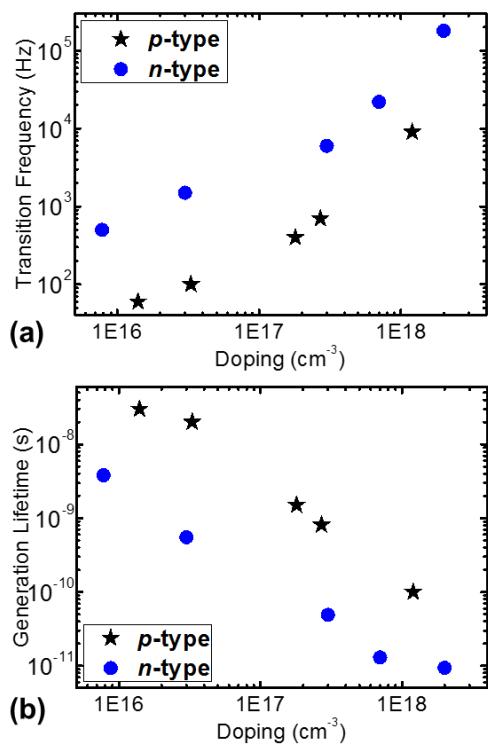
255

256 Figure 4



257

258 Figure 5

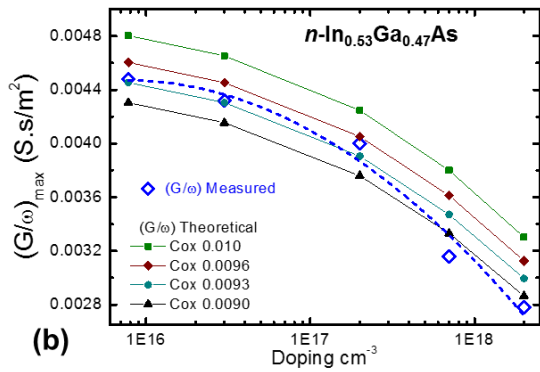
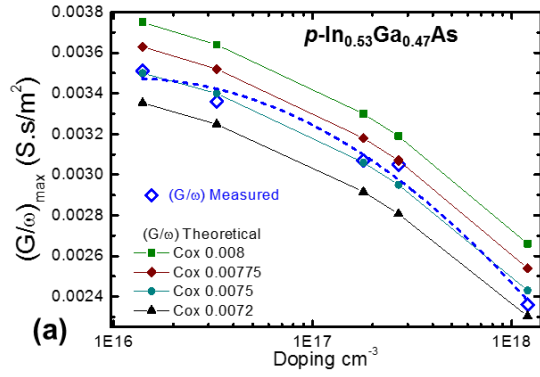


259

260

261

262 Figure 6



263

264

-
- ¹ J. Del Alamo, *Nature*, **479**, 317 (2011).
- ² I. Thayne, S. Bentley, M. Holland, W. Jansen, X. Li, D. Macintyre, S. Thom, B. Shin, J. Ahn, P. McIntyre, *Microelec. Eng.*, **88**, 1070 (2011).
- ³ C. L. Hinkle, E. M. Vogel, P. D. Ye R. M. Wallace, *Curr. Opin. Sol. State Mat. Sci.* **15**, 188 (2011).
- ⁴ H.-P. Komsa, A. Pasquarello, *Microelec. Eng.*, **88**, 1436 (2011).
- ⁵ J. Robertson, Y. Guo, and L. Lin, *J. Appl. Phys.*, **117**, 112806 (2015).
- ⁶ R. Engel-Herbert, Y. Hwang, and S. Stemmer, *J. Appl. Phys.*, **108**, 124101 (2010).
- ⁷ E. O'Connor, S. Monaghan, K. Cherkaoui, I. M. Povey, and P. K. Hurley, *Appl. Phys. Lett.*, **99**, 212901, (2011).
- ⁸ H. C. Lin, W-E. Wang, G. Brammertz, M. Meuris, and M. Heyns, *Microelec. Eng.*, **86** 1554 (2009)
- ⁹ H. D. Trinh, E. Y. Chang, P. W. Wu, Y. Y. Wong, C. T. Chang, Y. F. Hsieh, C. C. Yu, H. Q. Nguyen, Y. C. Lin, K. L. Lin, and M. K. Hudait, *Appl. Phys. Lett.*, **97**, 042903 (2010).
- ¹⁰ T. D. Lin, Y. H. Chang, C. A. Lin, M. L. Huang, W. C. Lee, J. Kwo, and M. Hong, *Appl. Phys. Lett.*, **100**, 172110 (2012).
- ¹¹ A. Callegari, P. D. Hoh, D. A. Buchanan, and D. Lacey, *Appl. Phys Lett.*, **54**, 332 (1989).
- ¹² S. Monaghan É. O'Connor, R. Rios, F. Ferdousi, Liam Floyd, E. Ryan, K. Cherkaoui, I. M. Povey, K. J. Kuhn, and P. K. Hurley, *IEEE Trans .Elec. Dev .*, **61**. 4176, (2014).
- ¹³ É. O'Connor B Brennan, V Djara, K Cherkaoui, S Monaghan, SB Newcomb, R Contreras, M Milojevic, G Hughes, ME Pemble, RM Wallace, PK Hurley, *J. Appl. Phys.*, **109**, 024101 (2011).
- ¹⁴ B. Brennan, M. Milojevic, C. L. Hinkle, F. S. Aguirre-Tostado, G. Hughes, and R. M. Wallace, *Appl. Surf. Sci.*, **257** 4082–4090 (2011).
- ¹⁵ J. J. Gu, A. T. Neal, and P. D. Ye, *Appl. Phys. Lett.*, **99**, 152113 (2011).
- ¹⁶ S. M. Sze, “*Physics of Semiconductor Devices*”, J. Wiley & Sons, (1981).
- ¹⁷ The In_{0.53}Ga_{0.47}As permittivity and intrinsic carrier concentration parameters were taken from: <http://www.ioffe.ru/SVA/NSM/Semicond/GaInAs/index.html>

-
- ¹⁸ S. Monaghan, É. O'Connor, I. M. Povey, B. J. Sheehan, K. Cherkaoui, B. J. A. Hutchinson, P. K. Hurley, F. Ferdousi, R. Rios, K. J. Kuhn, and A. Rahman, *J. Vac. Sci. Technol. B*, **31**, 01A119, (2013).
- ¹⁹ D. Varghese, Y. Xuan, Y. Q. Wu, T. Shen, P. D. Ye, and M. A. Alam, *Proc. IEEE Int. Electron. Devices Meet.*, p. 379, (2008).
- ²⁰ A. Ali, H. Madan, S. Koveshnikov, S. Oktyabrsky, R. Kambhampati, T. Heeg, D. Schlom, and S. Datta, *IEEE Trans. Electron Devices*, **57** (4), p. 742, (2010).
- ²¹ H.-P. Chen, Y. Yuan, B. Yu, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell, and Y. Taur, *IEEE Trans. Electron Devices*, **59** (9), p. 2383, (2012).
- ²² E. O'Connor, K. Cherkaoui, S. Monaghan, B. Sheehan, I. M. Povey, and P. K. Hurley *Microelec. Eng.*, **147**, p325 (2015).
- ²³ E. Nicollian, J. Brews, *MOS Phys. and Tech.*, Wiley, (1982).
- ²⁴ Y. Yuan, L. Wang, B. Yu, B. Shin, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell, and Y. Taur, *IEEE Elec. Dev. Lett.*, **32**, p485, (2011).
- ²⁵ V. Djara, K. Cherkaoui, M. Schmidt, S. Monaghan, É. O'Connor, I. M. Povey, D. O'Connell, M. E. Pemble, and P. K. Hurley, *IEEE Trans. Elec. Dev.*, **59**, 1084, (2012).