<table>
<thead>
<tr>
<th><strong>Title</strong></th>
<th>Electrical characterization of top-gated molybdenum disulfide field-effect-transistors with high-k dielectrics</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Author(s)</strong></td>
<td>Bolshakov, Pavel; Zhao, Peng; Azcatl, Angelica; Hurley, Paul K.; Wallace, Robert M.; Young, Chadwin D.</td>
</tr>
<tr>
<td><strong>Publication date</strong></td>
<td>2017-05-05</td>
</tr>
<tr>
<td><strong>Type of publication</strong></td>
<td>Article (peer-reviewed)</td>
</tr>
<tr>
<td><strong>Link to publisher's version</strong></td>
<td><a href="http://dx.doi.org/10.1016/j.mee.2017.04.045">http://dx.doi.org/10.1016/j.mee.2017.04.045</a></td>
</tr>
<tr>
<td><strong>Rights</strong></td>
<td>© 2017 Elsevier B.V. This manuscript version is made available under the CC-BY-NC-ND 4.0 license <a href="http://creativecommons.org/licenses/by-nc-nd/4.0/">http://creativecommons.org/licenses/by-nc-nd/4.0/</a></td>
</tr>
<tr>
<td><strong>Embargo information</strong></td>
<td>Access to this article is restricted until 24 months after publication at the request of the publisher.</td>
</tr>
<tr>
<td><strong>Embargo lift date</strong></td>
<td>2019-05-05</td>
</tr>
<tr>
<td><strong>Item downloaded from</strong></td>
<td><a href="http://hdl.handle.net/10468/4062">http://hdl.handle.net/10468/4062</a></td>
</tr>
</tbody>
</table>

Downloaded on 2020-06-03T08:43:54Z
Accepted Manuscript

Electrical characterization of top-gated molybdenum disulfide field-effect-transistors with high-k dielectrics

Pavel Bolshakov, Peng Zhao, Angelica Azcatl, Paul K. Hurley, Robert M. Wallace, Chadwin D. Young

PII: S0167-9317(17)30190-9
Reference: MEE 10550
To appear in: Microelectronic Engineering
Received date: 23 February 2017
Revised date: 10 April 2017
Accepted date: 27 April 2017

Please cite this article as: Pavel Bolshakov, Peng Zhao, Angelica Azcatl, Paul K. Hurley, Robert M. Wallace, Chadwin D. Young, Electrical characterization of top-gated molybdenum disulfide field-effect-transistors with high-k dielectrics, Microelectronic Engineering (2017), doi: 10.1016/j.mee.2017.04.045

This is a PDF file of an unedited manuscript that has been accepted for publication. As a service to our customers we are providing this early version of the manuscript. The manuscript will undergo copyediting, typesetting, and review of the resulting proof before it is published in its final form. Please note that during the production process errors may be discovered which could affect the content, and all legal disclaimers that apply to the journal pertain.
Electrical characterization of top-gated molybdenum disulfide field-effect-transistors with high-k dielectrics

Pavel Bolshakov(1)*, Peng Zhao(1), Angelica Azcatl(1), Paul K. Hurley(2), Robert M. Wallace(1), and Chadwin D. Young(1)

1Department of Materials Science and Engineering, The University of Texas at Dallas, 800 West Campbell Road, Richardson, Texas 75080, USA

2Tyndall National Institute, University College Cork, Lee Maltings Complex, Dyke Parade, Mardyke, Cork, Ireland

*Corresponding author, pavel.bolshakov@utdallas.edu

Abstract

High quality HfO$_2$ and Al$_2$O$_3$ substrates are fabricated in order to study their impact on top-gate MoS$_2$ transistors. Compared with top-gate MoS$_2$ FETs on a SiO$_2$ substrate, the field effect mobility decreased for devices on HfO$_2$ substrates but substantially increased for devices on Al$_2$O$_3$ substrates, possibly due to substrate surface roughness. A forming gas anneal is found to enhance device performance due to a reduction in charge trap density of the high-k substrates. The major improvements in device performance are ascribed to the forming gas anneal. Top-gate devices built upon Al$_2$O$_3$ substrates exhibit a near-ideal subthreshold swing (SS) of ~69 mV/dec and a ~10× increase in field effect mobility, indicating a positive influence on top-gate device performance even without any backside bias.

Keywords: MoS$_2$; top-gated transistor; HfO$_2$; Al$_2$O$_3$; high-k; substrate;
1. Introduction

At the moment, transition metal dichalcogenides (TMDs) are one group of 2D materials that is being studied as a possible replacement for the semiconductor channel in future field-effect-transistor (FET) technology that require low power, high mobility devices[1][2][3][4]. Chief among them is molybdenum disulfide (MoS$_2$)[5][6], which has some of the earliest studies that report high mobility values (>200 cm$^2$/V-s), high $I_{ON}/I_{OFF}$ ratios (~10$^6$), and low subthreshold swing (~74 mV/dec) for top-gate, few-layer MoS$_2$ devices, usually fabricated on SiO$_2$/Si substrates[7]. While recent studies have demonstrated back-gate devices with HfO$_2$ and Al$_2$O$_3$ dielectrics[8][9][10] with high mobility values as a result of the high-k screening effect[11], few have studied the effects of these high-k dielectric substrates ("substrate" = HfO$_2$/Si or Al$_2$O$_3$/Si) on a top-gate devices structure akin to the silicon-on-insulator (SOI) technology in use today.

With high-k materials such as HfO$_2$ being utilized in current CMOS technology, their integration with TMDs can be advantageous for future applications. One recent bottleneck that has been overcome is the functionalization treatment of the inactive MoS$_2$ surface using a UV-ozone process that allows a uniform, high-k dielectric to be deposited[12]. With a proven top-gate MoS$_2$ FET fabrication process[13], an understanding of the effects of the unbiased back-gate dielectric on top-gate device performance is needed. In this paper, we demonstrate and discuss the use of high-k dielectric substrates in conjunction with a forming gas ("FG":5%H$_2$/95%N$_2$) anneal and their effect on top-gate MoS$_2$ devices.

2. Experimental

HfO$_2$ (~10nm) and Al$_2$O$_3$ (~15nm) were deposited onto Si using an atomic layer deposition (ALD) process. Metal-oxide-semiconductor (MOS) capacitors were fabricated and an FG anneal study was performed to achieve an optimal annealing temperature of 400 °C (1 hour) in order to establish the anneal impact on interface traps and achieve high quality dielectric substrates for top-gate devices. For the MoS$_2$ devices, high-k substrates used for the MOS capacitors had MoS$_2$ exfoliated onto them, with the source and drain patterns using photolithography and Cr/Au (20nm/150nm) deposited in a high-vacuum (10$^{-6}$ mbar) evaporation and lift-off process. Afterwards, these back-gate devices were FG annealed at 400 °C, with pre- and post-anneal I-V measurements. Both sets of MoS$_2$ devices (HfO$_2$ and Al$_2$O$_3$ substrates) were then functionalized using a 15 minute, in-situ UV-ozone treatment followed by a ALD of 4nm of HfO$_2$ at 200 °C. This combination of the FG anneal and UV-ozone treatment is done to reduce any residual, process induced contamination from lithography prior to top-gate dielectric formation[14][15][16]. The last step of the process involved the deposition of a Cr/Au top gate using the same process as the source/drain, converting back-gate devices into top-gate, 3-terminal FETs as shown in Fig. 1. C-V and I-V measurements were performed using a Cascade Microtech station in conjunction with a Keithley 4200 SCS and an Agilent E4980A LCR meter.

![Fig. 1. Cross-section (left) and top-view (right) of the final top-gate device structure.](image)

3. Results and Discussion

Frequency dependent C-V measurements were performed from 500Hz to 500kHz on HfO$_2$ and Al$_2$O$_3$ capacitors. Fig. 2 shows the low dispersion C-V curves after a 400 °C FG anneal, with the insets showing the high dispersion "hump" before annealing, which is typically attributed to interface traps ($Q_{It}$). While the dispersion in accumulation, typically attributed to series resistance ($R_s$), did reduce slightly after FG annealing, the $Q_{It}$ was the most impacted by the FG annealing for both HfO$_2$ and Al$_2$O$_3$ as the dispersion is nearly non-existent in the depletion region post anneal.

![Fig. 2. C-V frequency dependence for (a) HfO$_2$ and (b) Al$_2$O$_3$ capacitors post 400 °C FG anneal with the insets showing high dispersion before annealing.](image)

Initially, the FG annealing was performed at 200 °C, 300 °C, and 400 °C, and the C-V measurements were done pre- and post-anneal. Interface trap density ($D_{it}$) was extracted using Low-High Frequency method[17] with Fig. 3 showing the trend of $D_{it}$ reduction as a function of FG annealing temperature. While both high-k dielectrics show a major reduction in $D_{it}$, the Al$_2$O$_3$ appears to have the lowest $D_{it}$ of 2*10 cm$^2$eV$^{-1}$ post 400 °C anneal, suggesting an Al$_2$O$_3$ substrate may yield a better interface than a HfO$_2$ substrate for the deposition conditions used.
Using HfO$_2$ and Al$_2$O$_3$ substrates, several back-gate MoS$_2$ FETs were fabricated in order to study the effect of the FG anneal on device performance and compare the substrates. As the MoS$_2$ flakes were untreated\cite{18,19}, their thickness was kept relatively the same (~4-5nm) in order to lower variability amongst devices. The I-V characteristics of the devices were measured pre- and post-anneal at 400 °C, with the statistics of the SS$_{MIN}$ and I$_{ON}$/I$_{OFF}$ shown in Fig. 4a. With an average I$_{ON}$/I$_{OFF}$ of ~10$^{3}$ and SS$_{MIN}$ of ~365 mV/dec pre-anneal, the performance of the HfO$_2$ devices improved in all instances with an average I$_{ON}$/I$_{OFF}$ of ~10$^{3}$ and SS$_{MIN}$ of ~156 mV/dec post-anneal. For the Al$_2$O$_3$ devices, with an average I$_{ON}$/I$_{OFF}$ of ~10$^{3}$ and SS$_{MIN}$ of ~207 mV/dec pre-anneal and an average I$_{ON}$/I$_{OFF}$ of ~10$^{3}$ and SS$_{MIN}$ of ~100 mV/dec post-anneal, there was also significant device improvement. This increase in performance can be attributed not only to passivation as a result of the FG anneal, but also to a possible reduction in impurities at the backside MoS$_2$/(HfO$_2$ or Al$_2$O$_3$) interface. It is worth noting that even though the net difference in device improvement was approximately the same, the post-anneal performance for devices on Al$_2$O$_3$ substrates was better than for devices on HfO$_2$ substrates. This may partly be as a result of better adhesion during MoS$_2$ exfoliation as the Al$_2$O$_3$ substrate yielded a greater number of few-layer flakes than the HfO$_2$ substrate, possibly due to substrate surface roughness as discussed later in this section.

There was also a beneficial effect of the FG anneal on the contacts as (Fig. 4b) the I$_D$-V$_D$ shows Schottky behavior (inset) pre-anneal and Ohmic behavior post-anneal, potentially reducing the need for sulfur passivation treatments\cite{20,21,22}. While these back-gate devices can be useful to study the effects of the FG anneal, full device evaluation is limited, especially since current CMOS technology does no use this device structure. To properly compare the effect of the HfO$_2$ and Al$_2$O$_3$ substrates, a top-gate FET structure is needed.

Converting from a back-gate to a top-gate FET allows for continuous study of the same MoS$_2$ flake. The back-gate devices on HfO$_2$ and Al$_2$O$_3$ substrates, already FG annealed at 400 °C, all had UV-ozone functionalization treatment followed by in-situ HfO$_2$ ALD, converting to a top-gate FET with a Cr/Au (20nm/150nm) gate (Fig. 1). These devices were electrically characterized without any back-gate bias and their field effect mobility ($\mu_{FE}$) statistics are shown in Fig. 5, along with those of top-gate devices characterized on SiO$_2$ substrates. There was a ~10x increase in mobility for devices on Al$_2$O$_3$ substrates compared to devices on HfO$_2$ substrates. The HfO$_2$ substrates appear to have yielded devices with mobility values worse than those of devices on SiO$_2$ substrates.

![Fig. 3. Interface trap density (D$_{it}$) extraction shows Al$_2$O$_3$ substrates with lower D$_{it}$ values than HfO$_2$ substrates as a function of FG annealing temperature.](image1)

![Fig. 4. (a) Several back-gate FETs on high-k substrates pre- and post-anneal indicating a beneficial trend in device performance. (b) I$_D$-V$_D$ characteristics of a back-gate FET pre-inset) and post-anneal indicates a beneficial effect on the contacts.](image2)

![Fig. 5. Mobility statistics of multiple top-gate FETs shows a ~10x improvement in field effect mobility ($\mu_{FE}$) on Al$_2$O$_3$ substrates over HfO$_2$ substrates.](image3)

Comparing the I$_D$-V$_G$ of two best top-gate devices in Fig. 6, the device on a HfO$_2$ substrate (inset) demonstrates a poor I$_{ON}$/I$_{OFF}$ of ~10 and a high SS$_{MIN}$ of ~1400 mV/dec, while the device on an Al$_2$O$_3$ substrate demonstrates a good I$_{ON}$/I$_{OFF}$ of ~10$^{6}$ and a near-ideal SS$_{MIN}$ of 69 mV/dec. Even though the devices on both high-k substrates had good performance as FG annealed back-gate devices and went through the same top-gate conversion, those on Al$_2$O$_3$ substrates showed an improvement while those on HfO$_2$ substrates became worse as a top-gate device than as a back-gate device. This suggests that for MoS$_2$, a high-quality Al$_2$O$_3$ substrate may provide a beneficial effect to top-gate devices under the conditions stated earlier as opposed to HfO$_2$ substrates, with further study required for combinations of top-gate dielectrics and TMDs.
10 Vg for top-gate FETs show a subthreshold swing (SS) from ~1400 mV/dec for a HfO2 substrate (inset) to a near-deal ~69 mV/dec for Al2O3 substrate.

To determine a possible origin of the better device performance on Al2O3 substrates than on HfO2 substrates, atomic force microscopy (AFM) was used to ascertain surface roughness. AFM images shown in Fig. 7 demonstrate the average RMS roughness of the Al2O3 substrate to be 0.19 nm, compared to 0.25 nm for the HfO2 substrate. There are also indications of contaminants on the HfO2 surface, most likely attributed to carbon residue. The surface roughness of the backside dielectric appears to influence the exfoliated MoS2 flake size and top-gate device performance.

Fig. 6. I0-Vg for top-gate FETs show a subthreshold swing (SS) from ~1400 mV/dec for a HfO2 substrate (inset) to a near-deal ~69 mV/dec for Al2O3 substrate.

Fig. 7. AFM images of (a) Al2O3 substrate and (b) HfO2 substrate with an RMS roughness value of 0.19 nm and 0.25 nm, respectively.

4. Conclusions

High quality HfO2 and Al2O3 substrates were fabricated for top-gate MoS2 field-effect-transistors and their impact on device performance was compared. A forming gas anneal was used to reduce the interface trap density and passivate these high-k substrates. The devices on Al2O3 substrates demonstrated much better performance compared to those on HfO2 substrates, possibly due to substrate surface roughness. This suggests a better interface is formed between the Al2O3 substrate and the MoS2 material, leading to a near-ideal subthreshold swing of 69 mV/dec for a top-gate device. This work provides insights into utilizing high-k substrates for top-gate devices in future applications of TMD materials.

Acknowledgement

This work was supported in part by the US/Ireland R&D Partnership (UNITE) under the NSF award ECCS-1407765, and the center for Low Energy Systems Technology (LEAST), one of six SRC STARNet Centers, sponsored by MARCO and DARPA.

References

Graphical abstract

- FE Mobility (cm²V⁻¹s⁻¹)
- SiO₂: 11.2
- HfO₂
- Al₂O₃

Drain Current (A)
SS (mV/dec)
Top-Gate Voltage (V)
Highlights

- Top-gate MoS$_2$ FETs were fabricated on high-k dielectric substrates
- A forming gas anneal enhances device performance with a reduction in $D_{it}$
- Top-gate devices on Al$_2$O$_3$/Si showed better performance than on HfO$_2$/Si
- AFM images suggest that substrate surface roughness affects device performance