42.6 Gb/s Fully Integrated All-Optical XOR Gate

J.M. Dailey, S.K. Ibrahim, R.J. Manning, R.P. Webb, S. Lardenois, G.D. Maxwell, and A.J. Poustie

Abstract

We demonstrate an SOA-based all-optical high-speed Mach-Zehnder interferometer exclusive- OR (XOR) gate fabricated in a silica III-V hybrid-integration technology platform. The device includes integrated time delays for rapid differential operation as well as integrated phase shifters for fine tuning of power splitters and interferometer bias enabling highly optimized XOR gate operation. XOR functionality is verified through inspection of the output pulse sequence and the carrier-suppressed output spectrum. A 2.3 dB penalty for a 42.6 Gb/s RZ-OOK signal at a 10^{-9} bit error rate is observed.

Introduction

Demand for higher signal processing bandwidths in the core and metro networks continues unabated as data traffic continues to grow rapidly worldwide. Aggregate transmission rates in the hundreds and thousands of Gb/s are being actively pursued, and debate continues on whether or not the electronics needed to operate in these regimes will be too costly [1, 2]. A well championed solution is the development of all-optical processing techniques, which promise ample bandwidth through the exploitation of ultrafast (~fs-ps) processes. All-optical exclusive-OR (XOR) logical gates are of special interest due to their use in constructing a number of higher level logic functions including e.g. parity checkers, pseudo-random pulse generators, firewalls, and packet header processors [3].

Semiconductor optical amplifiers (SOAs) have garnered particular interest as all-optical processors due to their high level of integrability and relatively large nonlinearities in tiny volumes, leading to smaller switching energies and packages more suited for telecoms-type applications [4]. Furthermore, bandwidth limitations arising from slow interband carrier dynamics have been greatly ameliorated through differential switching techniques in SOA-based interferometer structures relying on cross-phase modulation (XPM).

In this letter we report on a novel highly integrated XOR gate based on differentially switched SOAs in a Mach-Zehnder interferometer (MZI) operating at 42.6 Gb/s, and its bit-error rate (BER) penalties. This device has a higher level of integration than previously reported [5]: differential signal delays are included on-chip along with variable power splitters for both data channels. Together with the variable phase shifters in the MZI arms, these enable highly optimized gate operation [6]. We are the first, to our knowledge, to demonstrate this high level of photonic integration for an all-optical XOR gate and to report such low BER penalties at 40 Gb/s [7].

XOR Operation Principle

The XOR gate was fabricated by CIP Technologies using a hybrid-integration platform [5] incorporating nonlinear InP-based SOAs with low-loss planar silica waveguides, and is shown in Fig. 1. The SOAs are strained multiple-quantum-well devices with an effective length of 2 mm and 10% to 90% gain recovery times of ~ 33ps. A Peltier cooler is included for temperature stability. The continuous-wave (cw) probe at λ_{XOR} is injected into the gate and is made to destructively interfere at the MZI output through appropriate SOA and phase shifter bias settings. When a return-to-zero (RZ) pulse is injected into the channel A power splitter, the non-delayed pulse saturates SOA1 and through XPM opens a switching window, carving the rising edge of the probe output pulse.

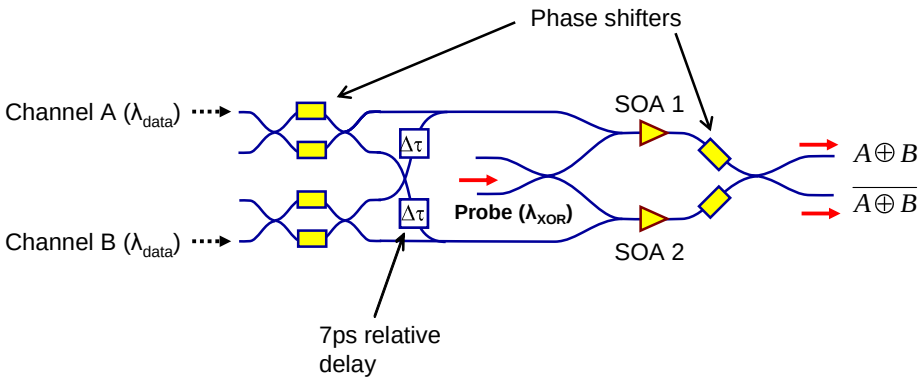

Fig. 1 The hybrid-integrated XOR gate, with all components shown integrated on-chip.

At a time Δτ (~7 ps) later the delayed pulse enters SOA2 and closes the switching window, forming the falling edge of the output pulse. The pulse delay was chosen specifically for the 42.6 Gb/s data rate, and the ultimate operational speed of the gate is limited by the choice of this delay and the SOA recovery times. This is an AND operation between channel A and the probe. Fig. 1 also shows an AND gate for channel B placed symmetrically inside the device, and when an input pulse enters the channel B power splitter a pulse also emerges from the output. However, if there is a pulse at channel A as well as channel B, the two SOAs are identically saturated resulting in zero relative phase shift and no output pulse. This switching behaviour describes XOR operation. Note that the phase shifters at the channel A and B inputs enable continuously variable power splitters which together with the probe phase shifters are essential for open output eyes with high extinction [6]. The SOAs' amplified spontaneous emission (ASE) 3-dB bandwidth was measured to be greater than 40 nm indicating a large operational bandwidth. The SOAs have been designed to minimize polarization sensitivity, though because of the birefringence of the passive waveguides the device displays a polarization dependence on both the probe and data inputs.

Experimental Setup

The data channels were implemented using the 2 ps output pulses (λ_{data} = 1560nm) from a commercial mode-locked laser synchronized to a 10.65 GHz RF clock. The pulse stream was modulated with a pseudorandom binary sequence (PRBS) of length 2^7-1, using a lithium niobate optical modulator, and was then passively multiplexed up to a 42.6 Gb/s stream. The data was divided into two channels (A and B) with the introduction of some relative optical delay. The use of erbium doped fibre amplifiers (EDFAs) and optical attenuators enabled control over the data input power to the gate. A performance optimum corresponded with data input powers around 5 dBm, or pulse energies of approximately 150 fJ. The cw probe input (λ_{XOR} ~= 1552.5nm) power was 1 dBm and polarization controllers for both the data and probe signals enabled optimization of the output eyes. The SOA bias currents were 548 and 488 mA. Ideally the bias currents would be identical, and the disparity here is attributed to a small excess loss asymmetry in the gate. The SOAs and Peltier element comprise the largest current sinks in the package and the total electrical power consumption was ~ 3 W with no optical inputs.

Results

XOR operation is verified in Fig 2 where we show the traces from a high-speed optical sampling oscilloscope when the device is operated in both AND as well as XOR modes. The upper trace (AND Gate A) is the output when channel B is turned off, and similarly the middle trace (AND Gate B) is the output when channel A is turned off. When both channels are input to the device, the result is shown in the bottom trace (XOR Gate) and by comparing all three traces the appropriate XOR logical operations are verified. The extinction ratio for the output XOR signal measured from the scope trace is 11 dB.

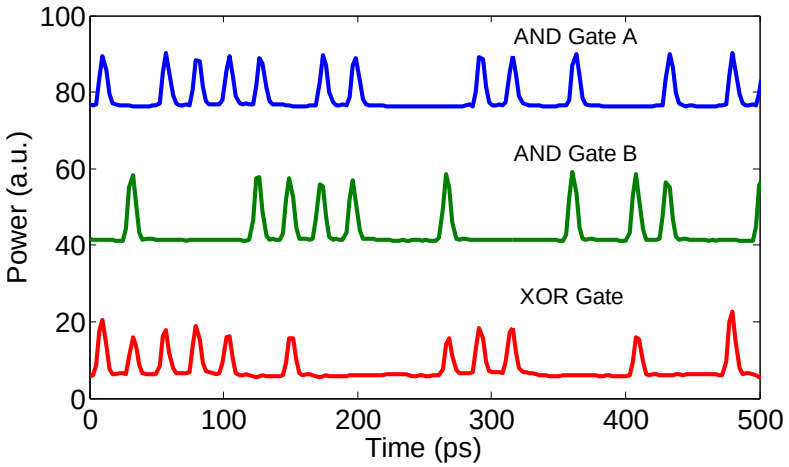

Fig 2. Time domain probe output from gate operating in AND (upper and middle traces) and XOR modes (bottom trace). Power offsets between traces are arbitrary.

We also verify correct device operation by examining the probe output spectra shown in Fig 3. The upper spectrum shows the output when channel A is turned off, and the device acts as an AND gate for channel B. The 42.6 GHz sideband harmonics can be clearly seen in relation to the carrier frequency at $\lambda_{XOR} \sim 1552.5$nm. The bottom spectrum shows the output when both channels are input to the device, and we note that this spectrum is derived from the output pulses corresponding to AND operations on channels A and B, i.e. if both channels input zero or one then there is no pulse output. Channels A and B trigger the two SOAs in opposite order, and the resultant "A" and "B" output pulses have opposing phase shifts. The PRBS sequence ensures that an "A" or "B" pulse is equally likely in the output, and so on average, the carrier is suppressed and the output spectrum resembles that of a differential phase-shift keyed (DPSK) signal.

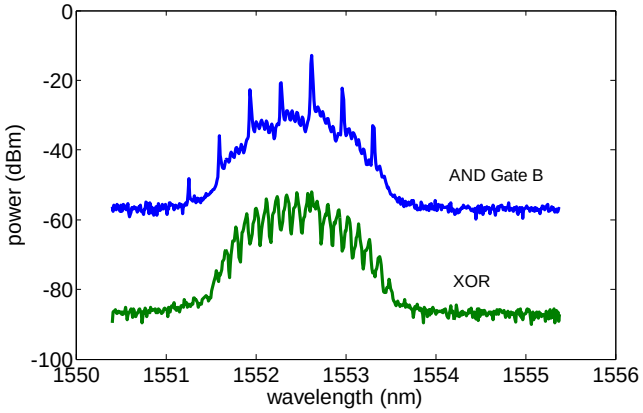

Fig 3. The probe output spectra for both AND and XOR modes. Power offset between traces is arbitrary.

Finally, we filter the data signal from the device output and send the XOR signal to an optically preamplified receiver. In Fig 4 we show the results from measuring the bit error rate (BER) as a function of receiver input power. The back-to-back (B2B) channel is plotted with circles, and shows the BER when a data channel is directly input to the receiver. The two AND gate results are also shown as the data with squares and diamonds. Linear fits to the data indicate that the penalties for gates A and B at a BER of 10^{-9} are 2.3 and 1.2 dB, respectively. We believe that the discrepancy in penalties may be due to a residual asymmetry in the fabrication leading to a better extinction ratio for channel B than for channel A. The XOR data are shown with triangle markers and indicate a measured penalty of 2.3 dB, though we believe that penalties approaching the B gate penalty may be possible by addressing the fabrication asymmetries

discussed earlier. However, we do not expect XOR performance to equal that of an individual AND gate due to the increased operational bandwidth needed for XOR operation: when a binary "one" is input to both data channels each SOA receives two pulses separated by $\Delta\tau$ = 7ps, i.e. a temporal separation less than a bit slot.

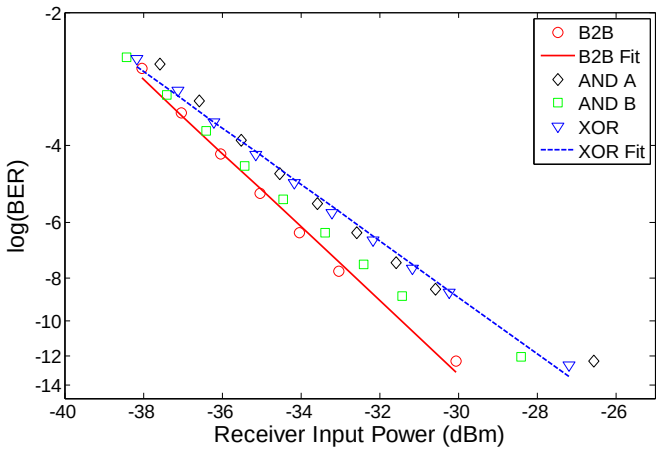

Fig 4. BER vs input power for XOR gate. XOR operates with 2.3 dB penalty at a BER of 10^{-9}.

Conclusions

We have demonstrated a high-speed all-optical XOR gate fabricated in a hybrid-integration technology platform. The fully integrated device includes phase shifters and power splitters that can be adjusted for highly optimized gate operation. The output signal experiences only a 2.3 dB penalty at 42.6 Gb/s and we believe smaller penalties, closer to the 1.2 dB AND gate penalty, are within reach of this technology.

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