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This Letter presents an analysis of the zero temperature coefficient (ZTC) bias in junctionless nanowire transistors (JNTs). Unlike in previous works, which had shown that JNT did not present a ZTC point, this work shows that ZTC may occur in JNTs depending mainly on the series resistance of the devices and its dependence on the temperature. Experimental results of drain current, threshold voltage, and series resistance are presented for both long and short channel n and p-type devices. © 2012 American Institute of Physics. [http://dx.doi.org/10.1063/1.4744965]

The junctionless nanowire transistor (JNT) is a heavily doped device that presents a constant doping profile from source to drain.1–3 This device has been recently proposed as a promising alternative to the miniaturization of advanced metal-oxide-silicon (MOS) technologies without the need of ultrasharp doping concentration gradients to form junctions.3 JNTs have already exhibited advantages in relation to their inversion-mode (IM) counterparts, such as reduced drain induced barrier lowering (DIBL), reduced electric field in the conduction path, and improved short-channel effects.4–6

The characterization of JNTs at high and low temperatures (T) has been reported in Refs. 7 and 8, respectively. In both works, the JNT did not present a zero temperature coefficient (ZTC) point, i.e., a gate voltage bias in which the drain current remains the same independently of the temperature. This point in conventional MOS devices is related with both the mobility and threshold voltage on the temperature for nMOS JNTs is described by

\[ T = \frac{\mu}{q C_0} \]

\[ T = \frac{C_0}{C_2} \]

The measured transistors present mask width of 80 nm. The effective width of about 20 nm. The measured devices present 10 nm nitride spacers at each side of the gate between the end of the channel and the source/drain regions.

The drain current (\( I_{DS} \)) was obtained as a function of the gate voltage (\( V_G \)) for n and p-type devices at low drain bias (\( V_D = 40 \text{ mV} \)) over a wide temperature range. Figure 1 presents the measured \( I_{DS} \) vs. \( V_G \) curves for both nMOS (A) and pMOS (B) devices with channel length of 50 nm. One can note that the nMOS transistors present a ZTC point whereas the pMOS ones do not. In Figures 1(c) and 1(d), the \( I_{DS} \) vs. \( V_G \) characteristics are exhibited for n and p-type devices with \( L = 10 \mu \text{ m} \), respectively. Differently to observed for short devices, in this case, both nMOS and pMOS transistors exhibit the ZTC point, contrarily to the previously published data.7,8 As mentioned, the occurrence of the ZTC point in conventional MOS devices is related with both the mobility and threshold voltage. In JNTs, the absence of ZTC has been related to \( V_{TH} \), since previous works reported a much higher dependence on \( T \) (\( dV_{TH}/dT \)) in relation to similar inversion-mode devices.7,8 The threshold voltages were extracted for the short devices (\( L = 50 \text{ nm} \)) of Figs. 1(a) and 1(b) using the charge-based method described in Ref. 12. The \( V_{TH} \) values are presented in Fig. 2 as a function of the temperature. In previous works, the absolute \( dV_{TH}/dT \) variation obtained in JNTs varied between 0.6 and 1.7 mV/K.7,8 Therefore, one can note that the devices measured in this work exhibit a lower dependence on \( T \) in relation to the previous ones.

According to Ref. 13, the dependence of the threshold voltage on the temperature for nMOS JNTs is described by

\[ \frac{dV_{TH}}{dT} = \frac{\partial V_{FB}}{\partial T} - \left( \frac{q}{\varepsilon_S} \left( \frac{W H}{2H + W} \right)^2 + \frac{q W H}{C_{ox}} \right) \frac{\partial N_D}{\partial T}, \]

where \( V_{FB} \) is the flatband voltage, \( C_{ox} \) is the gate capacitance per unit of length, and \( q \) and \( \varepsilon_S \) have their usual meaning. The devices measured in Refs. 7 and 8 have a gate oxide (SiO2) thickness around 10 nm and P+ polysilicon gate. The first

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The term in the right side of Eq. (1) is related to the dependence of the flatband voltage on $T$. As a metal gate is used in the measured JNTs, the $V_{FB}$ variation is only related to the Fermi level dependence on $T$. The second term depends on the doping concentration variation with $T$ ($dN_D/dT$), multiplied by a dimensions-dependent factor. Considering that the devices in the present work and in the previous ones present similar doping concentration, the $dN_D/dT$ term is also similar. However, as the devices studied in this work present a much lower EOT (with respect to the works of Refs. 7 and 8), $C_{ox}$ increases, diminishing the dimensions-dependent factor and, consequently, the second term. Therefore, $dV_{TH}/dT$ variation obtained for the JNTs evaluated in this work is similar to the ones obtained for triple-gate inversion mode devices.\(^7,14\)

The second parameter to which the ZTC point is generally related in inversion-mode devices is the carrier mobility. According to Ref. 7, $\mu$ presents a weak dependence on the temperature in JNTs. Fig. 3 presents the maximum transconductance ($g_{m,max}$) extracted for the long devices ($L = 10 \mu m$) of Figs. 1(c) and 1(d). It is worth mentioning that $g_{m,max}$ is directly proportional to the low field mobility. The $g_{m,max}$ has been extracted for the longer devices such that the effect of the series resistance is negligible. The maximum transconductance of the long measured transistors presents a significant dependence on the temperature. It can be noted that $g_{m,max}$ almost doubles its value when the temperature is reduced from 480 K to room temperature for both n and p-type devices with concentration around $5 \times 10^{18}$ cm\(^{-3}\). For the devices with doping concentration of $10^{19}$ cm\(^{-3}\), the $g_{m,max}$ increase is about 60% and 75% for the p and n-type JNTs, respectively. Therefore, it is clear that the long-channel devices present a considerable mobility dependence on the $T$, despite the previous results.\(^7\) The increase in the threshold voltage and in the mobility when $T$ is reduced explains the ZTC bias in long devices, just like for conventional MOS inversion-mode devices. However, this cannot explain the ZTC point absence for the shorter pMOS JNTs and also for the previous works.

The regions under the nitride spacers at source/drain create a parasitic resistance, which can affect the JNTs behavior. The series resistances ($R_S$) were extracted for both n and p-type transistors using the method proposed by Dixit et al.\(^15\) and are exhibited in Fig. 4 as a function of the temperature. One can see that $R_S$ follows different trends for nMOS and pMOS devices: in the former, $R_S$ diminishes with $T$ reduction whereas for the latter the opposite behavior is obtained. The series resistance diminution with $T$ has also been observed for triple-gate inversion-mode devices\(^14\) and is attributed to the increase of the mobility, which reduces the resistivity. The $R_S$ in a doped silicon layer is inversely proportional to both mobility and doping concentration.
reduction due to the incomplete carrier ionization. As al-

to note that for the measured nMOS devices

For a conclusion, the shorter measured p-type devi-
cases, no ZTC point has been observed due to the series resis-
tance and its higher dependence on the temperature, which is
related to the incomplete ionization. All the n-type devices
presented a ZTC point. However, it can be noted that this
point is closer to the threshold voltage for the longer devices,
since the effect of the series resistance is less pronounced.
For the previous works,7,8 where the devices presented no
ZTC bias, this is related to the much higher series resistance.

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wire transistors.

FIG. 3. Maximum transconductance as a function of the temperature for the
long devices ($L = 10 \mu m$) of Figs. 1(c) and 1(d).

Although the doping concentrations are close to the
Mott transition ($\sim 10^{18}$--$10^{19}$ cm$^{-3}$),16 which means that the
semiconductor behaves like a metal, $N_A$ and $N_D$ suffer a
reduction due to the incomplete carrier ionization.$^{17}$ As al-
ready mentioned in Ref. 13, this partial carrier ionization can
affect, for instance, $V_{TH}$ since it is directly proportional to
the concentration. When the temperature is reduced, the
effects of the incomplete ionization increase, therefore
diminishing $N_D$ and $N_A$, which rises $R_S$. So, there are two
effects with different trends: the mobility, which tends to
reduce $R_S$ for lower $T$, and the incomplete carrier ionization
that presents the opposite behavior. From Fig. 4, one can
note that for the measured nMOS devices $R_S$ is mainly
related to the mobility whereas for the p-type ones the dop-
ing concentration is dominant.

Using Altermatt et al. model,18,19 the ionization rate can
be calculated for the doping elements used in n and p-type
devices for different concentrations. This model considers
that the activation energy drops as a function of the doping
concentration.17 It also considers that the incomplete ionization is
partially compensated by the fraction of carriers that remains
bound to dopant clusters above the Mott transition.18 This
leads to a full ionization at high dopant densities. The ioniza-
tion rate obtained for phosphorous doped silicon with
\[ N_D = 1 \times 10^{19} \text{ cm}^{-3} \]
varies between 0.94 and 0.97 for the $T$
range between 300 and 500 K, whereas for $N_D = 5 \times 10^{18} \text{ cm}^{-3}$
the ionization rate varies between 0.88 and 0.95. For boron
doped silicon with $N_A = 1 \times 10^{19} \text{ cm}^{-3}$ and $5 \times 10^{18} \text{ cm}^{-3}$,
the ionization rate varies in the ranges 0.90–0.95 and 0.82–
0.92, respectively, for the same $T$ range. For lower concen-
trations, there is a higher dependence of the ionization ratio
on the temperature. Also, it can be noted that for boron, the
ionization rate is lower than for phosphorous and presents a
higher dependence on the temperature. Therefore, it is
expected a higher effect of the incomplete ionization on
p-type devices than on n-type ones, which agrees with Fig. 4.

As a conclusion, the shorter measured p-type devi-
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