Negative-bias-temperature-instability and hot carrier effects in nanowire junctionless p-channel multigate transistors

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Negative-bias-temperature-instability and hot carrier effects in nanowire junctionless p-channel multigate transistors

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Negative-bias-temperature-instability (NBTI) and hot-carrier induced device degradation have been experimentally compared between accumulation mode (AM) p-channel multigate transistors (pMuGFETs) and junctionless (JL) pMuGFET. NBTI degradation is less significant in junctionless pMuGFETs than AM pMuGFETs. The threshold voltage shift is less significant in junctionless transistors than AM transistors. The device simulation shows that the peak of lateral electric field and the impact ionization rate of AM device are larger than those of junctionless devices. © *2012 American Institute of Physics*. [doi:10.1063/1.3688245]

Although the multigate transistor (MuGFET) is considered as the most promising candidate for future nanometer electronic devices due to the excellent control of short channel effects, an ultra-shallow and perfectly abrupt junction with infinite concentration gradient in source and drain junction is required to minimize impurity diffusion and to reduce short channel effects in MuGFETs.[1] Therefore, the diffusion of source and drain impurities is a bottleneck to the fabrication of nanometer scale MuGFETs. As a volume of MuGFET approaches to around $10^{-17}\,cm^{-3}$, the number of impurity atoms in the devices is less than about 10^3. Due to the random nature of ion implantation, doping diffusion, and other process involved in the doping of silicon film, the number and position of impurity atoms are subject to stochastic variation. This leads to the unavoidable variation of various device parameters.[2]

Recently, a junctionless transistor and nanowire pinch-off FET, for which the channel doping concentration and type are the same as in the source and drain region, have been proposed.[3,4] The device characteristics are the same as inversion mode or accumulation mode devices. The device characterization of junctionless (JL) transistors including the improvement of subthreshold slope, the reduced short channel effects, zero-ram characteristics, low temperature conductance oscillation, and noise properties has been reported.[5–9]

At present levels of gate oxide thickness and electric fields, negative-bias-temperature-instability (NBTI) and hot carrier effects are reported to be a serious reliability problem in nanometer scale p-channel multigate transistor (pMuGFET). Especially, hot carrier induced device degradation is increased at high temperature due to the combined NBTI and hot carrier effects.[10] As far as we know, there is no study of NBTI and hot-carrier effects on JL pMuGFETs.

In this work, NBTI and hot-carrier induced device degradation has been experimentally compared between accumulation mode (AM) and JL pMuGFET. A possible mechanism for less NBTI and hot carrier effects in JL transistors is proposed.

JL transistors were fabricated on SOI wafer with a 340 nm top silicon layer and a 400 nm buried oxide. The resistivity of the p-type is 10–20 Ω cm. The silicon film was thinned down to 10 nm and patterned to form silicon nanowires using electron beam lithography and reactive ion etching. A 10 nm gate oxide was then grown by dry oxidation. The ion implantation was performed to dope the devices uniformly P^+ with a concentration of $1 \times 10^{19}\,cm^{-3}$for JL pMuGFETs. AM tri-gate nanowire pMuGFETs were fabricated as well with undoped channels ($N_A = 2 \times 10^{15}\,cm^{-3}$). A 50 nm polysilicon layer was deposited by LPCVD on the gate oxide and doped N^{++} for both devices. The source and drain regions were formed using BF_2 ion implantation, but no source or drain implant was performed on the JL pMuGFETs. The fabricated AM and JL devices have a pi-gate structure. The final thickness of the silicon film is 10 nm. The gate length studied here is 1 μm, and the extension depth of the pi-gate in the buried oxide is approximately 10 nm. This device has a 40 nm drawn width which is reduced to 30 nm by processing. NBTI stress was applied with gate electrode held at a constant negative bias of $V_{GS} = -7.0$ V under a temperature 120 °C while the source and drain electrode were grounded. In order to characterize the hot-carrier effects, devices were stressed for 3600 s with the drain voltage held at −8.0 V and for different gate bias values.

Fig. 1 shows the comparison of NBTI-induced threshold voltage shifts (ΔV_{TH}) between AM and JL devices. Generally, the NBTI process is a field dependent and not a voltage dependent process. Due to the channel potential grounded to zero during NBTI stress as mentioned in Ref. 11, the gate bias of $V_{GS} = -7$ V was applied for the same oxide field in both devices. We confirmed from the device simulation that the oxide field was the same for both devices when the same gate bias voltage was applied. It is worth noting that the NBTI degradation in JL devices is a little bit less than the one in AM devices. Generally, the rate for the Si-H bond dissociation in the reaction–diffusion model for NBTI is proportional to the injected hole concentration; we reckon as shown in Fig. 2 that the less NBTI degradation in JL devices

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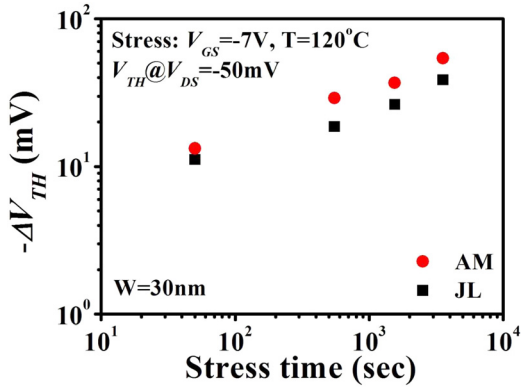

FIG. 1. (Color online) Comparison of NBTI-induced ΔV_{TH} between AM and JL pMuGFETS.

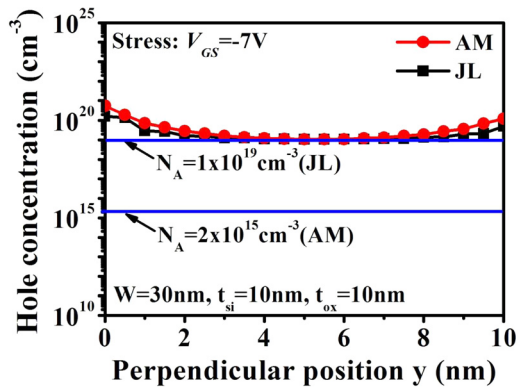

FIG. 2. (Color online) Comparison of hole concentration at the surface between AM and JL pMuGFETs.

is due to the less hole concentration at the surface of silicon film than AM devices. The time dependence of the threshold voltage shift, ΔV_{TH}, varies as the stress time to the power n, where n is equal to 0.2 for both devices. This result indicates that device degradation is predominantly determined by the generation of interface states for both devices.

Generally, the hot carrier induced degradation depends on the gate voltage in p-channel MOSFETs. At low gate bias, hot electrons generated by impact ionization are injected into the gate oxide, which leads to a reduction of the absolute value of the threshold voltage and increases saturation current.

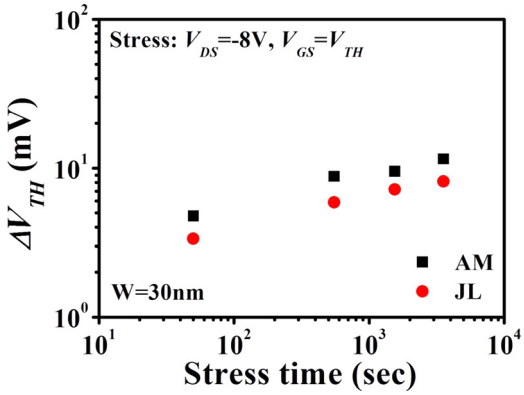

FIG. 3. (Color online) Comparison of ΔV_{TH} between AM and JL pMuGFETs.

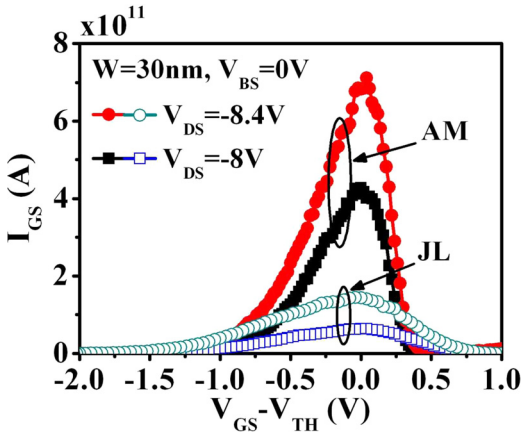

FIG. 4. (Color online) Comparison of a gate current between AM and JL pMuGFETs.

Fig. 3 shows the comparison of hot-carrier induced threshold voltage shifts ΔV_{TH} between AM and JL pMuGFETs. We observed that the threshold voltage shifts to a positive direction and the drain saturation current increases after stress for both devices. This increase in drain saturation current is associated with trapping the injected electrons in the gate oxide. From Fig. 3, it can be clearly observed that ΔV_{TH} is less significant in JL transistors than AM transistors. To explain the less significant hot carrier effects in JL devices, the comparison of the measured gate current between AM and JL devices is depicted in Fig. 4. It is clear that the gate current in AM devices is larger than JL devices, and the maximum gate current appears at $V_{GS} = V_{TH}$ for both devices. The larger gate current in AM devices indicates that the more hot electrons inject into the gate oxide layer.[12] The maximum gate current at $V_{GS} = V_{TH}$ corresponds to the maximum device degradation in both devices.

In order to explain the less hot carrier degradation in JL transistor, the devices were simulated using the three-dimensional ATLAS simulation software.[13] A plot of the comparison of lateral electric field and the impact ionization rate between AM and JL devices is depicted in Fig. 5. It is clearly seen that the peaks of lateral electric field and impact ionization rate in JL device are lower than AM devices. And also the peaks of lateral electric field and impact ionization rate in JL devices are located inside the drain region, as previously shown in Ref. 5.

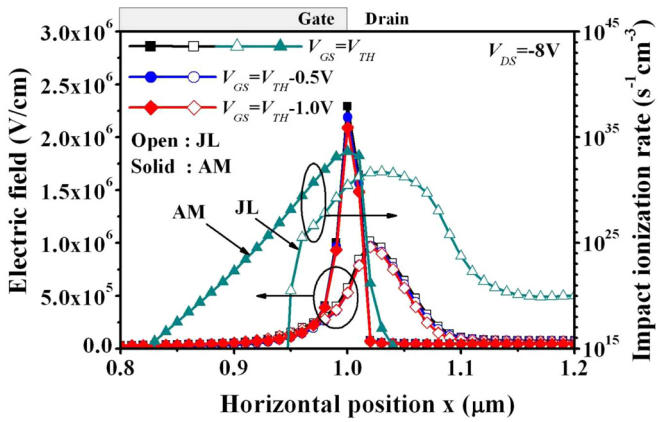

FIG. 5. (Color online) Comparison of lateral field and impact ionization between AM and JL pMuGFETs.

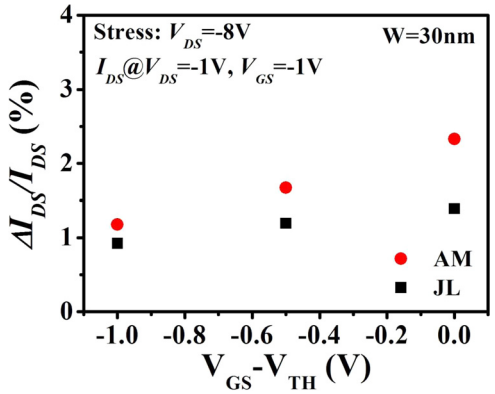

FIG. 6. (Color online) Comparison of $\Delta I_{DS}/I_{DS}$ as a function of stress gate voltages $V_{GS}-V_{TH}$.

Fig. 6 shows a plot of drain current shifts ($\Delta I_{DS}/I_{DS}$) as a function of stress $V_{GS}-V_{TH}$. The hot carrier degradation of JL pMuGFET is less significant than that of AM pMuGFET for all gate bias voltages. The device degradation is the largest at $V_{GS}=V_{TH}$. This result agrees well with the measured gate current.

In conclusion, NBTI degradation is a little bit less in junctionless pMuGFETs than AM pMuGFETs. The hot carrier degradation is also less significant in junctionless transistors than AM transistors. The lesser degradation is due to the smaller gate current in junctionless transistor. The device simulation shows that the peaks of lateral electric field and the impact ionization rate of junctionless transistor are lower than those of AM transistors, and they are located within the drain region.

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