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<th>Title</th>
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<tr>
<td>Publication date</td>
<td>2011</td>
</tr>
<tr>
<td>Type of publication</td>
<td>Article (peer-reviewed)</td>
</tr>
</tbody>
</table>
[http://dx.doi.org/10.1063/1.3626038](http://dx.doi.org/10.1063/1.3626038)  
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Field-effect mobility extraction in nanowire field-effect transistors by combination of transfer characteristics and random telegraph noise measurements

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Citation: Appl. Phys. Lett. 99, 073502 (2011); doi: 10.1063/1.3626038
View online: http://dx.doi.org/10.1063/1.3626038
View Table of Contents: http://aip.scitation.org/toc/apl/99/7
Published by the American Institute of Physics

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Field-effect mobility extraction in nanowire field-effect transistors by combination of transfer characteristics and random telegraph noise measurements

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(Received 20 June 2011; accepted 28 July 2011; published online 16 August 2011)

A technique based on the combined measurements of random telegraph-signal noise amplitude and drain current vs. gate voltage characteristics is proposed to extract the channel mobility in inversion-mode and accumulation-mode nanowire transistors. This method does not require the preliminary knowledge of the gate oxide capacitance or that of the channel width. The method accounts for the presence of parasitic source and drain resistance effect. It has been used to extract the zero-field mobility and the field mobility reduction factor in inversion-mode and junctionless transistors operating in accumulation mode. © 2011 American Institute of Physics.


The extraction of carrier mobility in the channel of nanowire (NW) multigate field-effect transistors (MuGFETs) requires the knowledge of both the gate oxide thickness and dimensions of the nanowire cross section. This is true for both inversion mode (IM) and accumulation mode (AM) devices. The gate capacitance of a single NW MuGFET is almost impossible to measure because of its very small value, and usually the measurements are carried out on a large number of NW devices connected in parallel to increase overall gate capacitance. Using this technique, one can only extract a value of the mobility that is averaged over a large number of nanowires; this method is not accurate because of the statistical variation of physical parameters such as cross section or line edge roughness from one nanowire to the next. In this letter, we propose to combine measurements of the random telegraph noise (RTN) amplitude and drain current dependence on applied gate voltage (RTN(V_G), I_D(V_G)) to extract carrier mobility on a single nanowire metal-oxide-semiconductor field-effect transistor (MOSFET). Both IM and junctionless (JL) nanowire transistors were measured.1,2

Multigate silicon NW n-channel MOSFETs with pi-gate architecture were fabricated on UNIBOND® silicon-on-insulator wafers. The width and thickness of the devices are approximately 10 nm × 10 nm and the gate length is 1 μm. The gate oxide and buried oxide (BOX) thickness are 7 nm and 340 nm, respectively. The channel p-type doping concentration of the “standard” IM pi-gate MOSFETs is 2 × 10¹⁸ cm⁻³; the source and drain are doped n-type with a concentration of 1 × 10²⁰ cm⁻³. The JL MOSFETs have the same dimensions as the IM devices but are characterized by a uniform n-type doping concentration of 1 × 10¹⁹ cm⁻³ in the source, drain, and channel regions. The I_D(V_G) characteristics and RTN in drain current were measured using an Agilent B1500A semiconductor parameter analyzer. The RTN was measured above threshold in both of types of devices.

The I_D(V_G) characteristics, normalized transconductance (g_m = dI_D/dV_G), and transconductance derivative (d^2I_D/dV_G^2) vs. gate voltage were measured for NW IM and JL MOSFETs in linear operation (V_D = 50 mV). The transconductance derivative allows one to determine the threshold voltage, V_T. The measured values are 0.20 V and 0.33 V, respectively (see Fig. 1 of Ref. 5). Assuming the gate voltage is large enough to create accumulation layer in the JL device, the drain current in the IM and JL MOSFETs can be written as follows:

$$I_{D,IM} = \mu_{eff}C_{OX} W \frac{L}{V_G - V_{TH}} V_D$$

(1)

and

$$I_{D,AM} = \mu_S C_{OX} W \frac{L}{(V_G - V_{FB})} V_D + \frac{q\mu_B n_s S}{L} V_D,$$

(2)
where $\mu_{\text{eff}} = \mu_0 / (1 + \theta(V_G - V_{TH}))$ in Eq. (1) is the effective mobility in the inversion channel; $\mu_0$ is the mobility at zero electric field and $\theta$ is the gate-field mobility reduction factor. The first and second terms in Eq. (2) represent the current flowing in the accumulation channel and the bulk of the device, respectively. In this expression, $\mu_s$ and $\mu_b$ are the electron mobility in the accumulation layer and the bulk channel, respectively; $n_s$ is the electron density in the bulk of the nanowire and $S$ is the cross sectional area of the nanowire; $L$ and $W$ are the length and width of the channel, respectively; and $C_{OA}$ is the gate oxide capacitance. The flat-band voltage $V_{FB}$ of the JL MOSFET can be estimated from the $I_d(V_G)$ characteristics using expression (2). It is found at the intersection point between two extrapolated straight lines corresponding to the accumulation current and the bulk current. Our estimations give us that $V_{FB} = 0.55$ V. In the rest of this, we will only consider the operation of the JL MOSFET in AM, i.e., for $V_G > V_{FB}$.

The RTN of the drain current was measured as a function of gate voltage for $V_G > V_{TH}$ in the IM MOSFET and $V_G > V_{FB}$ in the JL device. Fig. 1 shows that the normalized amplitude of the RTN signal, $\Delta D/ID$, decreases when the gate voltage is increased and is correlated to the variation of the transconductance-to-current ratio, $g_m/ID$, with $V_G$. It has been demonstrated that dependence of $g_m/ID$ on $V_G$ in an IM MOSFET can be written as follows:

$$\frac{\Delta D}{ID} = \frac{q}{WLC_{OX}} \times \frac{g_m}{ID} \approx \frac{q}{WLC_{OX}(V_G - V_{TH})} \times \left\{ 1 + \frac{1}{1 + \theta^{-1}(V_G - V_{TH})} \right\} = \frac{K}{V_G - V_{TH}},$$

where $K = q/WLC_{OX}$ and $\gamma = (V_G - V_{TH}) = 1 + 1/1 + \theta^{-1}(V_G - V_{TH})$; $\gamma = 1$ if $\theta(V_G - V_{TH}) << 1$ and $\gamma = 2$ if $\theta(V_G - V_{TH}) >>> 1$. Using Eq. (3), the value of $K$ and product of the gate oxide capacitance by the channel width can be obtained from the slope of $\gamma(\Delta D/ID)$ vs. $(V_G - V_{TH})^{-1}$, as long as we know the channel length, $L$. In case of the junctionless transistor operating in linear regime and for $V_G > V_{FB}$, the $V_{TH}$ must be replaced by $V_{FB}$ in Eq. (3).

To extract $\gamma(V_G - V_{TH})$, we must first determine the value of $\theta$. In the presence of a non-negligible source and drain resistance, $R_{SD}$, the term $\theta$ in Eq. (3) has to be replaced by $\theta' \equiv \theta + W/C_{OX}/L/h_0R_{SD} = \theta + h_0R_{SD}$, where $h_0 = W/C_{OX}/L$. It can be shown that measured resistance, $R_m$, can be expressed as

$$R_m = R_{SD} + \theta h_0^{-1} + \frac{h_0^{-1}}{(V_G - V_{TH})} = R_{SD} + \frac{h_0^{-1}}{(V_G - V_{TH})},$$

and the term $\theta'$ can be written $\theta' = R_{SD}^* h_0$. Assuming the same dependence of the surface channel mobility on field in AM devices as in IM transistors, we can write $\mu_s = \mu_{s0} / (1 + \theta(V_G - V_{FB}))$ for the mobility in the accumulation channel. From the measurements of the device resistance $R_m$ vs. $(V_G - V_{TH})^{-1}$ (IM devices) or $R_m$ vs. $(V_G - V_{FB})^{-1}$ (AM devices), two parameters can be extracted: the slope of the curves yields the value of $h_0^{-1}$ and the point of intersection of the these slopes with the $V_G$ axis yields $(V_G - V_{TH})^{-1} = 0$ for the IM MOSFET or $(V_G - V_{FB})^{-1} = 0$ for the JL device, which in turn yields the value of to $R_{SD}^*$ (see Fig. 2(a)). Once $h_0$ and $R_{SD}^*$ are known, one can extract the value of $\theta'$ (we find $\theta_{IM} = 0.735 V^{-1}$ and $\theta_{JL} = 0.938 V^{-1}$) and one can calculate $\gamma$ (see Fig. 2(b)). One can also estimate the value of $K_{IM}$ (extracted value: $K_{IM} = 1.6 \times 10^{-4} V$) from the dependence of $\gamma(\Delta D/ID)$ on $(V_G - V_{TH})^{-1}$ or the value of $K_{IL}$ (extracted value: $K_{IL} = 3.75 \times 10^{-4} V$) from the dependence of $\gamma(\Delta D/ID)$ on $(V_G - V_{FB})^{-1}$ (see Fig. 2(b)).

In an IM MOSFET in linear regime, the transconductance is given by $g_m = C_{OX} W V_D / \mu_{FE}$. The field-dependent mobility, $\mu_{FE}$, can thus be written as

$$\mu_{FE} = \frac{L}{C_{OX} W V_D} g_m = \frac{K L^2}{q V_D} g_m.$$

Fig. 3 presents the dependence of $\mu_{FE}$ on gate voltage both for an IM MOSFET and a JL MOSFET with surface accumulation $(V_G > V_{FB})$ with $L = 1 \mu m$ and $V_D = 50 mV$. Using the following expression:
\[ \mu_0 = \frac{\beta_0 L}{W_{COX}} = \frac{1}{q} \beta_0 KL^2, \]  

one can estimate the value of \( \mu_0 \) and \( \mu_{so} \) for both the IM MOSFET and the JL MOSFET. From the measurements, we find that the zero-field surface mobility in the IM MOSFET, \( \mu_0 \), is equal to 735 cm\(^2\)V\(^{-1}\)s\(^{-1}\). In the highly doped JL MOSFET, \( \mu_{so} = 97 \text{ cm}^2\text{V}^{-1}\text{s}^{-1} \). The estimation of mobility in a JL device is quite sensitive on the accuracy if \( V_{FB} \) determination. For example, increasing \( V_{FB} \) from 0.55 to 0.75 V decreases \( K_{JL} \) from \( 3.75 \times 10^{-4} \) V to \( 1.87 \times 10^{-4} \) V and increases of the \( \beta_0 \) from \( 4.2 \times 10^{-6} \) to \( 9.3 \times 10^{-6} \) \( \Omega^{-1}\text{V}^{-1} \). This that can reduce the estimated \( \mu_{FE} \) by factor of 2 but has only a small influence (12%) the calculated value of \( \mu_{so} \).

In conclusion, by combining measurements of random telegraph noise with data from the \( I_D(V_G) \) characteristics of IM and AM MOSFETs, one can estimate the effective mobility and its field dependence in surface inversion or accumulation channels, without preliminary knowledge of the gate capacitance or the channel width of the devices.

This work was supported by the Science Foundation Ireland Grant Nos. 05/IN/1888 and 10/IN.1/12992 and was enabled by the Programme for Research in Third-Level Institutions. This work was supported in part by the European Community (EC) Seventh Framework Program through the Networks of Excellence NANOSIL and EUROSOI+ under Contract Nos. 216171 and 216373.