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Field-effect mobility extraction in nanowire field-effect transistors by combination of transfer characteristics and random telegraph noise measurements

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A technique based on the combined measurements of random telegraph-signal noise amplitude and drain current vs. gate voltage characteristics is proposed to extract the channel mobility in inversion-mode and accumulation-mode nanowire transistors. This method does not require the preliminary knowledge of the gate oxide capacitance or that of the channel width. The method accounts for the presence of parasitic source and drain resistance effect. It has been used to extract the zero-field mobility and the field mobility reduction factor in inversion-mode and junctionless transistors operating in accumulation mode. © *2011 American Institute of Physics.* [doi:10.1063/1.3626038]

The extraction of carrier mobility in the channel of nanowire (NW) multigate field-effect transistors (MuGFETs) requires the knowledge of both the gate oxide thickness and dimensions of the nanowire cross section. This is true for both inversion mode (IM) and accumulation mode (AM) devices. The gate capacitance of a single NW MuGFET is almost impossible to measure because of its very small value, and usually the measurements are carried out on a large number of NW devices connected in parallel to increase overall gate capacitance. Using this technique, one can only extract a value of the mobility that is averaged over a large number of nanowires; this method is not accurate because of the statistical variation of physical parameters such as cross section or line edge roughness from one nanowire to the next. In this letter, we propose to combine measurements of the random telegraph noise (RTN) amplitude and drain current dependence on applied gate voltage ($RTN(V_G)$, $I_D(V_G)$) to extract carrier mobility on a single nanowire metal-oxide-semiconductor field-effect transistor (MOSFET). Both IM and junctionless (JL) nanowire transistors were measured.[1,2]

Multigate silicon NW n-channel MOSFETs with pi-gate architecture were fabricated on UNIBOND® silicon-on-insulator wafers. The width and thickness of the devices are approximately 10 nm × 10 nm and the gate length is 1 μm. The gate oxide and buried oxide (BOX) thickness are 7 nm and 340 nm, respectively. The channel p-type doping concentration of the "standard" IM pi-gate MOSFETs is 2×10^{18} cm^{-3}; the source and drain are doped n-type with a concentration of 1×10^{20} cm^{-3}. The JL MOSFETs have the same dimensions as the IM devices but are characterized by a uniform n-type doping concentration of 1×10^{19} cm^{-3} in the source, drain, and channel regions. The $I_d(V_g)$ characteristics and RTN in drain current were measured using an Agilent B1500A semiconductor parameter analyzer. The RTN was measured above threshold in both of types of devices.

The $I_D(V_G)$ characteristics, normalized transconductance ($g_m = dI_D/dV_G$), and transconductance derivative ($dg_m/dV_G = d^2I_D/dV_G^2$) vs. gate voltage were measured for NW IM and JL MOSFETs in linear operation ($V_D = 50$ mV). The transconductance derivative allows one to determine the threshold voltage, V_T.[3,4] The measured values are 0.20 V and 0.33 V, respectively (see Fig. 1 of Ref. 5). Assuming the gate voltage is large enough to create accumulation layer in the JL device, the drain current in the IM and JL MOSFETs can be written as follows:

$$I_{D_IM} = \mu_{eff} C_{OX} \frac{W}{L}(V_G - V_{TH})V_D \quad (1)$$

and

$$I_{D_AM} = \mu_S C_{OX} \frac{W}{L}(V_G - V_{FB})V_D + \frac{q\mu_b n_c S}{L} V_D, \quad (2)$$

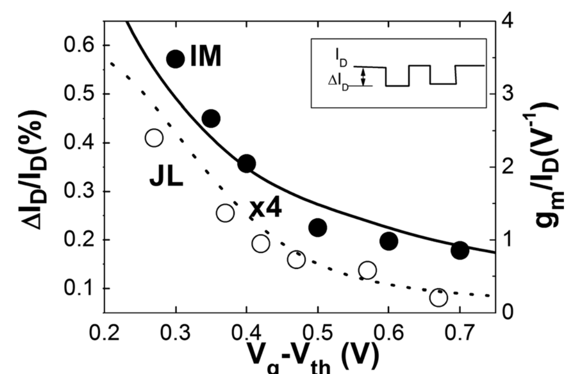

FIG. 1. Relative RNT amplitude of drain current (circles) and g_m/I_D (lines) vs. gate voltage overdrive for IM (filled circles) and JL (empty circles) MOSFETs. Inset: Schematic picture of measurement of the relative RTN amplitude.

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where $\mu_{eff} = \mu_0/1 + \theta(V_G - V_{TH})$ in Eq. (1) is the effective mobility in the inversion channel; μ_0 is the mobility at zero electric field and θ is the gate-field mobility reduction factor. The first and second terms in Eq. (2) represent the current flowing in the accumulation channel and the bulk of the device, respectively. In this expression, μ_S and μ_b are the electron mobility in the accumulation layer and the bulk channel, respectively; n_c is the electron density in the bulk of the nanowire and S is the cross sectional area of the nanowire; L and W are the length and width of the channel, respectively; and C_{OX} is the gate oxide capacitance. The flat-band voltage V_{FB} of the JL MOSFET can be estimated from the $I_D(V_G)$ characteristics using expression (2). It is found at the intersection point between two extrapolated straight lines corresponding to the accumulation current and the bulk current.[6] Our estimations give us that $V_{FB} = 0.55$ V. In the rest of this, we will only consider the operation of the JL MOSFET in AM, i.e., for $V_G > V_{FB}$.

The RTN of the drain current was measured as a function of gate voltage for $V_G > V_{TH}$ in the IM MOSFET and $V_G > V_{FB}$ in the JL device. Fig. 1 shows that the normalized amplitude of the RTN signal, $\Delta I_D/I_D$, decreases when the gate voltage is increased and is correlated to the variation of the transconductance-to-current ratio, g_m/I_D, with V_G.[6] It has been demonstrated that dependence of g_m/I_D on V_G in an IM MOSFET can be written as follows:

$$\frac{\Delta I_D}{I_D} = \frac{q}{WLC_{ox}} \times \frac{g_m}{I_D} \approx \frac{q}{WLC_{OX}(V_G - V_{TH})} \times \left\{1 + \frac{1}{1+\theta^{-1}(V_G - V_{TH})^{-1}}\right\} = \frac{K\gamma}{V_G - V_{TH}}, \quad (3)$$

where $K = q/WLC_{OX}$ and $\gamma \equiv \gamma(V_G - V_{TH}) = 1 + 1/1 + \theta^{-1}(V_G - V_{TH})^{-1}$; $\gamma = 1$ if $\theta(V_G - V_G) \ll 1$ and $\gamma = 2$ if $\theta(V_G - V_{TH}) \gg 1$.[5] Using Eq. (3), the value of K and product of the gate oxide capacitance by the channel width can be obtained from the slope of $\gamma(\Delta I_D/I_D)$ vs. $(V_G - V_{TH})^{-1}$, as long as we know the channel length, L. In case of the junctionless transistor operating in linear regime and for $V_G > V_{FB}$, the V_{TH} must be replaced by V_{FB} in Eq. (3).

To extract $\gamma(V_G - V_{TH})$, we must first determine the value of θ. In the presence of a non-negligible source and drain resistance, R_{SD}, the term θ in Eq. (3) has to be replaced by $\theta^* \equiv \theta + WC_{OX}/L\mu_0 R_{SD} = \theta + \beta_0 R_{SD}$, where $\beta_0 = WC_{OX}/L\mu_0$.[6] It can be shown that measured resistance, R_m, can be expressed as

$$R_m = R_{SD} + \theta\beta_0^{-1} + \frac{\beta_0^{-1}}{(V_G - V_{TH})} = R_{SD}{}^* + \frac{\beta_0^{-1}}{(V_G - V_{TH})}, \quad (4)$$

and the term θ^* can be written $\theta^* = R_{sd}{}^*\beta_0$. Assuming the same dependence of the surface channel mobility on field in AM devices as in IM transistors, we can write $\mu_S \equiv \mu_{S_{eff}} = \mu_{s0}/1 + \theta(V_G - V_{FB})$ for the mobility in the accumulation channel. From the measurements of the device resistance R_m vs. $(V_G - V_{TH})^{-1}$ (IM devices) or R_m vs. $(V_G - V_{FB})^{-1}$ (AM devices), two parameters can be extracted:

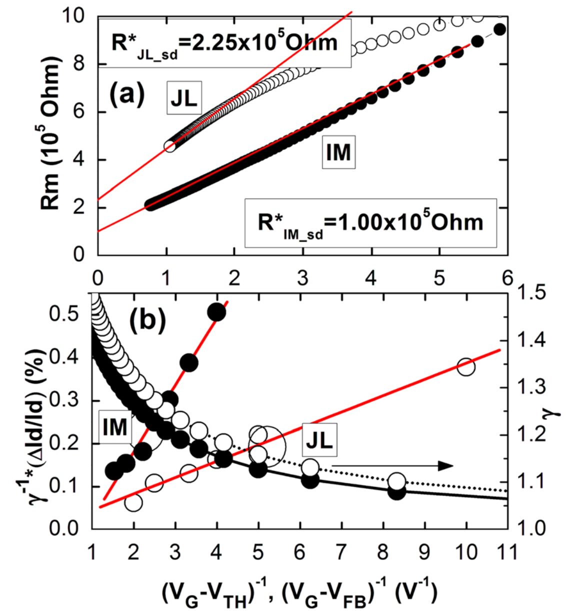

FIG. 2. (Color online) Measured resistance (a), gamma, and relative RNT amplitude of drain current corrected on gamma (b) vs. gate voltage overdrive for IM (filled circles) and JL (empty circles) MOSFETs.

the slope of the curves yields the value of $\beta_0{}^{-1}$ and the point of intersection of the these slopes with the V_G axis yields $(V_G - V_{TH})^{-1} = 0$ for the IM MOSFET or $(V_G - V_{FB})^{-1} = 0$ for the JL device, which in turn yields the value of to $R_{sd}{}^*$ (see Fig. 2(a)). Once β_0 and $R_{sd}{}^*$ are known, one can extract the value of θ^* (we find $\theta_{IM}{}^* = 0.735$ V^{-1} and $\theta_{JL}{}^* = 0.938$ V^{-1}) and one can calculate γ (see Fig. 2(b)). One can also estimate the value of K_{IM} (extracted value: $K_{IM} = 1.6 \times 10^{-3}$ V) from the dependence of $\gamma(\Delta I_D/I_D)$ on $(V_G - V_{TH})^{-1}$ or the value of K_{JL} (extracted value: $K_{JL} = 3.75 \times 10^{-4}$ V) from the dependence of $\gamma(\Delta I_D/I_D)$ *on* $(V_G - V_{FB})^{-1}$ (see Fig. 2(b)).

In an IM MOSFET in linear regime, the transconductance is given by $g_m = \frac{C_{OX}W}{L} V_D \mu_{FE}$.[6] The field-dependent mobility, μ_{FE}, can thus be written as

$$\mu_{FE} = \frac{L}{C_{OX}WV_D} g_m = \frac{KL^2}{qV_D} g_m \quad (5)$$

Fig. 3 presents the dependence of μ_{FE} on gate voltage both for an IM MOSFET and a JL MOSFET with surface accumulation ($V_G > V_{FB}$) with $L = 1$ μm and $V_D = 50$ mV. Using the following expression:

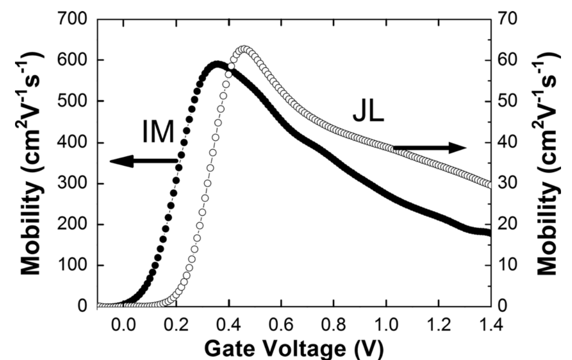

FIG. 3. Surface field-effect electron mobility vs. gate voltage for the IM and JL nanowire MOSFETs.

$$\mu_0 = \frac{\beta_0 L}{W C_{OX}} = \frac{1}{q}\beta_0 K L^2, \quad (6)$$

one can estimate the value of μ_0 and μ_{s0} for both the IM MOSFET and the JL MOSFET. From the measurements, we find that the zero-field surface mobility in the IM MOSFET, μ_0, is equal to 735 cm^{2}V^{-1}s^{-1}. In the highly doped JL MOSFET, $\mu_{S0} = 97$ cm^{2}V^{-1}s^{-1}. The estimation of mobility in a JL device is quite sensitive on the accuracy if V_{FB} determination. For example, increasing V_{FB} from 0.55 to 0.75 V decreases K_{JL} from 3.75×10^{-4} V to 1.87×10^{-4} V and increases of the β_0 from 4.2×10^{-6} to 9.3×10^{-6} Ω^{-1}V^{-1}. This that can reduce the estimated μ_{FE} by factor of 2 but has only a small influence (12%) the calculated value of μ_{S0}.

In conclusion, by combining measurements of random telegraph noise with data from the $I_D(V_G)$ characteristics of IM and AM MOSFETs, one can estimate the effective mobility and its field dependence in surface inversion or accumulation channels, without preliminary knowledge of the gate capacitance or the channel width of the devices.

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