<table>
<thead>
<tr>
<th><strong>Title</strong></th>
<th>Structural and electrical analysis of the atomic layer deposition of HfO2/n-In0.53Ga0.47As capacitors with and without an Al2O3 interface control layer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Author(s)</strong></td>
<td>O'Mahony, Aileen; Monaghan, Scott; Provenzano, G.; Povey, Ian M.; Nolan, M. G.; O'Connor, Éamon; Cherkaoui, Karim; Newcomb, Simon B.; Crupi, Felice; Hurley, Paul K.; Pemble, Martyn E.</td>
</tr>
<tr>
<td><strong>Publication date</strong></td>
<td>2010</td>
</tr>
<tr>
<td><strong>Type of publication</strong></td>
<td>Article (peer-reviewed)</td>
</tr>
</tbody>
</table>
| **Link to publisher's version** | http://aip.scitation.org/doi/abs/10.1063/1.3473773  
http://dx.doi.org/10.1063/1.3473773  
Access to the full text of the published version may require a subscription. |
| **Rights** | © 2010 American Institute of Physics. This article may be downloaded for personal use only. Any other use requires prior permission of the author and AIP Publishing. The following article appeared in O’Mahony, A., Monaghan, S., Provenzano, G., Povey, I. M., Nolan, M. G., O’Connor, É., Cherkaoui, K., Newcomb, S. B., Crupi, F., Hurley, P. K. and Pemble, M. E. (2010) ’Structural and electrical analysis of the atomic layer deposition of HfO2/n-In0.53Ga0.47As capacitors with and without an Al2O3 interface control layer’, Applied Physics Letters, 97(5), pp. 052904 and may be found at http://aip.scitation.org/doi/abs/10.1063/1.3473773 |
| **Item downloaded from** | http://hdl.handle.net/10468/4337 |

Downloaded on 2018-12-20T19:22:21Z
Structural and electrical analysis of the atomic layer deposition of HfO$_2$/n-In$_{0.53}$Ga$_{0.47}$As capacitors with and without an Al$_2$O$_3$ interface control layer

A. O'Mahony, S. Monaghan, G. Provenzano, I. M. Povey, M. G. Nolan, É. O'Connor, K. Cherkaoui, S. B. Newcomb, F. Crupi, P. K. Hurley, and M. E. Pemble

Citation: Appl. Phys. Lett. 97, 052904 (2010); doi: 10.1063/1.3473773
View online: http://dx.doi.org/10.1063/1.3473773
View Table of Contents: http://aip.scitation.org/toc/apl/97/5
Published by the American Institute of Physics

Articles you may be interested in
1-nm-capacitance-equivalent-thickness HfO$_2$/Al$_2$O$_3$/InGaAs metal-oxide-semiconductor structure with low interface trap density and low gate leakage current density
Applied Physics Letters 100, 132906 (2012); 10.1063/1.3698095

Electrical analysis of three-stage passivated In$_{0.53}$Ga$_{0.47}$As capacitors with varying HfO$_2$ thicknesses and incorporating an Al$_2$O$_3$ interface control layer
Structural and electrical analysis of the atomic layer deposition of HfO$_2$/n-In$_{0.53}$Ga$_{0.47}$As capacitors with and without an Al$_2$O$_3$ interface control layer

A. O’Mahony,$^{1, a}$ S. Monaghan,$^1$ G. Provenzano,$^{1, 2}$ I. M. Povey,$^1$ M. G. Nolan,$^1$ E. O’Connor,$^1$ K. Cherkauoli,$^1$ S. B. Newcomb,$^2$ F. Crupi,$^2$ P. K. Hurley,$^1$ and M. E. Pemble$^1$

$^1$Tyndall National Institute, University College Cork, Lee Maltings, Prospect Row, Cork, Ireland
$^2$Dipartimento di Elettronica, Informatica e Sistemistica, Università della Calabria, Via P. Bucci, 87036 Arcavacata di Rende (CS), Italy
$^3$Glebe Laboratories, Glebe Scientific Ltd., Newport, County Tipperary, Ireland

(Received 30 March 2010; accepted 25 June 2010; published online 6 August 2010)

High mobility III-V substrates with high-$k$ oxides are required for device scaling without loss of channel mobility. Interest has focused on the self-cleaning effect on selected III-V substrates during atomic layer deposition of Al$_2$O$_3$. A thin ($\sim$1 nm) Al$_2$O$_3$ interface control layer is deposited on In$_{0.53}$Ga$_{0.47}$As prior to HfO$_2$ growth, providing the benefit of self-cleaning and improving the interface quality by reducing interface state defect densities by $\sim$50% while maintaining scaling trends. Significant reductions in leakage current density and increased breakdown voltage are found, indicative of a band structure improvement due to the reduction/removal of the In$_{0.53}$Ga$_{0.47}$As native oxides. © 2010 American Institute of Physics. [doi:10.1063/1.3473773]

A critical technological challenge in the integration of high $k$-dielectrics on III-V channels is the control of the high-$k$/III-V interface. Although the interfacial chemistry of the high-$k$/Si system is similar to the SiO$_2$/Si system,$^4$ the high-$k$/III-V system is more complex, due to competition between the various native oxide species at the interface,$^2$ resulting in growth of a poor quality interfacial layer.$^{3, 6}$ In recent work,$^3$ reductions in interface state defect densities ($D_{it}$) were achieved by pre-treatment of the In$_{0.53}$Ga$_{0.47}$As surface prior to atomic layer deposition (ALD) of HfO$_2$ ($k \sim 16$–25, band gap ($E_g$) $\sim 5.8$–6.0 eV)$^{7, 9}$ The native oxides of In$_{0.53}$Ga$_{0.47}$As (Ga$_2$O$_3$, In$_2$O$_3$, and As$_2$O$_3$) have low band gaps (3.6–4.8 eV) (Refs. 2 and 9) and $k$-values of 8–10 when relating the reported$^9$ $k$-value for Ga$_2$O$_3$ and In$_2$O$_3$ with the approximate refractive indices ($n \sim 1.9$ for all) through the equation $n^2 \cdot k$ and the Moss Inverse Law,$^{11}$ for the refractive index, $k$-value and energy band gap. They are detrimental to the band structure of high-$k$/III-V devices by increasing the leakage current and creating potential wells in the native oxide layer between the high-$k$ oxide and the substrate. The self-cleaning Al$_2$O$_3$ ALD process is reported to reduce or remove the III-V native oxides.$^{12, 15}$ However, devices employing Al$_2$O$_3$ ($k \sim 8.6$–11.6, $E_g \sim 8.8$ eV) (Refs. 8, 9, and 12) as the gate oxide are limited for scaling due to its low $k$-value.

In this work, the structural and electrical properties of Pd/HfO$_2$/n-In$_{0.53}$Ga$_{0.47}$As devices (HfO$_2$: nominal thickness $\sim$3, $\sim$4, and $\sim$5 nm) with/without an $\sim$1 nm Al$_2$O$_3$ interface control layer (ICL), are examined using high resolution transmission electron microscopy (HR-TEM) and current/voltage measurements (J/V, CV, and GV, respectively). The devices are labeled: s1$_{\sim 3}$, s1$_{\sim 4}$, s1$_{\sim 5}$ (e.g., sample, $\sim$1 nm Al$_2$O$_3$, $\sim$5 nm HfO$_2$ is labeled s1$_{\sim 5}$). As a control, devices were fabricated without the Al$_2$O$_3$ ICL [nominal $\sim$5 nm HfO$_2$ only (label: s0$_{\sim 5}$)]. The motivation for this work is: (i) to detect any improvement in the quality and structure of the interface using the bilayer approach; (ii) to investigate if an Al$_2$O$_3$ ICL improves the electrical performance of devices by modifying the metal-oxide-semiconductor (MOS) band structure; (iii) to determine if scaling is possible with an Al$_2$O$_3$ ICL using reducing thicknesses of HfO$_2$.

The $\sim$2 $\mu$m n-type (S: $\sim$4 $\times$ 10$^{17}$ cm$^{-3}$) In$_{0.53}$Ga$_{0.47}$As channels had a $\sim$0.1 $\mu$m InP buffer layer (S: $\sim$2 $\times$ 10$^{18}$ cm$^{-3}$) on a $\sim$350 $\mu$m InP substrate (S: $\sim$3–8 $\times$ 10$^{18}$ cm$^{-3}$). All In$_{0.53}$Ga$_{0.47}$As layers were grown by MOVPE. An ex situ three-stage surface-pre-treatment process [HCl, NH$_4$OH, and (NH$_4$)$_2$S] was performed on the n-In$_{0.53}$Ga$_{0.47}$As/InP substrates which has previously been shown to be beneficial to device performance.$^3$ The Al$_2$O$_3$ and HfO$_2$ layers were deposited in a Cambridge NanoTech Fiji F200LLC ALD system, at 250 °C. The ALD of Al$_2$O$_3$, and HfO$_2$ employed alternating pulses of TMA/CH$_3$OH, tetrakis(ethylmethylamino)hafnium (TEMAH) [Hf[N(CH$_2$)$_3$(CH$_3$)$_4$]/H$_2$O, respectively. MOS structures were completed by vacuum evaporation of $\sim$200 nm of Pd at a deposition rate of 2.5 Å/s using a lift-off process. No ohmic back contacts were formed.

Figures 1(a) and 1(b) present cross-sectional HR-TEM micrographs of s1$_{\sim 5}$ and s0$_{\sim 5}$, confirming the physical oxide and nominal thicknesses are in close agreement: s1$_{\sim 5}$ [Fig. 1(a)] has a $\sim$5.3 nm HfO$_2$ layer, and a $\sim$1.2 nm Al$_2$O$_3$ layer. s0$_{\sim 5}$ [Fig. 1(b)], has a $\sim$4.9 nm HfO$_2$ layer. All oxide layers are amorphous. Comparison between Figs. 1(a) and 1(b) shows a $\sim$0.7 nm native oxide layer at the high-$k$/n-In$_{0.53}$Ga$_{0.47}$As interface when no Al$_2$O$_3$ ICL is deposited, which is indicative of an Al$_2$O$_3$ self-cleaning effect on the native oxide, for sample s1$_{\sim 5}$.

Figure 2(a) presents a cross-sectional HR-TEM micrograph of s1$_{\sim 3}$. The physical thicknesses of HfO$_2$ and Al$_2$O$_3$ are $\sim$3.2 nm and $\sim$1.2 nm, respectively. Figure 2(b), a plan-view HR-TEM micrograph for sample s1$_{\sim 5}$, reveals the epitaxial 2 $\mu$m n-In$_{0.53}$Ga$_{0.47}$As layer to be defect-free,

---

$^{a}$Electronic mail: aileen.omahony@tyndall.ie.
with an associated negligible root mean square (rms) surface roughness of <1 nm.

Figure 3 shows (a) JV responses and (b) the measured 1 kHz CV responses, along with the simulated

CV curves for all samples. The inset to Fig. 3(a) shows the capacitance equivalent thickness (CET) versus HR-TEM extracted HfO2

physical thickness plot for the bilayer sample set (s1_3, s1_4, s1_5), with a linear fit. Figure 3(a), when assessing the bilayer sample set only, shows that leakage current density response for sample s0_5 is substantially lower for the s1_5 (Al2O3 ICL) devices, compared to s0_5 devices. (b) Measured and simulated (from the 1D Poisson–Schrödinger solver) 1 kHz CV responses for all samples. Inset to (a) shows the CET vs physical thickness with a linear fit.

FIG. 1. Cross-sectional HR-TEM micrographs of (a) s1_5, with ~5.3 nm HfO2 and ~1.1 nm Al2O3, and (b) s0_5, with ~4.9 nm HfO2 and a ~0.7 nm native oxide layer.

FIG. 2. HR-TEM micrographs of (a) s1_3 (cross-sectional), with ~3.2 nm HfO2 and ~1.2 nm Al2O3, and (b) s1_5 (plan-view) shows a defect free n-In0.53Ga0.47As substrate layer.

FIG. 3. (Color online) (a) JV responses for all samples, with significantly lower leakage for the s1_5 (Al2O3 ICL) devices, compared to s0_5 devices. (b) Measured and simulated (from the 1D Poisson–Schrödinger solver) 1 kHz CV responses for all samples. Inset to (a) shows the CET vs physical thickness with a linear fit.
layer, evidenced by HR-TEM in combination with the electrical results, indicates that the Al₂O₃ is likely to be removing the native oxides via the self-cleaning process.

Figures 4(a) and 4(b) show the multifrequency CV responses for samples s0_5 and s1_5, respectively. The insets to Figs. 4(a) and 4(b) show the corresponding GV responses. We observe an increased Dₙ response in both the CV and GV profiles for sample s0_5 when compared to the equivalent response for sample s1_5, which includes (over the entire voltage range) an increased CV and GV stretch-out and frequency dispersion. In the voltage range −1 to 0.25 V, the absence of minority carriers is assumed, corresponding to the depletion regime. An approximation to the Conductance Method indicates that samples s0_5 and s1_5 have estimated Dₙ values of ~8 × 10¹² cm⁻² eV⁻¹ and ~4 × 10¹² cm⁻² eV⁻¹, respectively. Due to the absence of distinct equivalent parallel conductance (Gₚ/ω) peaks as observed in SiO₂/Si systems, this is derived assuming zero standard deviation in band bending using values of Gₚ/ω at −1 V and taken at 30 kHz. While it is noted that the Gₚ/ω magnitudes may be affected by the approximation conditions, and any possible minority carrier contribution, the relative difference provides a valid estimate. There is approximately a 50% reduction in Dₙ when including an Al₂O₃ ICL.

In summary, it is found that the inclusion of a thin Al₂O₃ ICL (~1 nm) at the HiF₀₂/In₀.₅₃Ga₀.₄₇As interface improves the structural and electrical properties of Pd/HiF₀₂/n-In₀.₅₃Ga₀.₄₇As devices. The inclusion of the Al₂O₃ ICL improves the breakdown voltage and reduces leakage current densities by approximately three orders of magnitude at 3 V by increasing the barrier height to tunneling from the In₀.₅₃Ga₀.₄₇As conduction band into the oxide. No apparent native oxide layer is observed at the high-k/In₀.₅₃Ga₀.₄₇As interface when using an Al₂O₃ ICL, suggesting that the Al₂O₃ ALD process is self-cleaning the In₀.₅₃Ga₀.₄₇As native oxides. Combining the structural and electrical results we find a QM correction factor of ~0.7 nm. The inclusion of an ICL causes an approximate 50% reduction in Dₙ, thereby improving the quality of the interface.

The authors thank Dan O’Connell, Tyndall National Institute, for sample processing; the ERASMUS program; Science Foundation Ireland’s FORME Strategic Research Cluster (Grant No. 07/SRC/11172); IRCSET; and Intel Ireland for the award and support (inc. Roger E. Nagle) for a scholarship to A. O’M.

16Professor G. Snider, University of Notre Dame, one-dimensional (1D) Poisson–Schrödinger solver, parameters used with HR-TEM oxide thicknesses: Al₂O₃: k=9, E₁₂ = 8.8 eV, ΔE₁ = 7.3 eV, ΔE₂ = 0 eV, HfO₂: k=20, E₁₂ = 6.0 eV, and ΔE₁₂ = 2.25 eV. In₀.₅₃Ga₀.₄₇As native oxide: k=9, E₁₂ = 4.1 eV, ΔE₁ = 1.5 eV. InP/In₀.₅₃Ga₀.₄₇As thickness/doping as specified. Temperature=300 K.