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Low subthreshold slope in junctionless multigate transistors

Chi-Woo Lee,[1] Alexei N. Nazarov,[2] Isabelle Ferain,[1] Nima Dehdashti Akhavan,[1] Ran Yan,[1] Pedram Razavi,[1] Ran Yu,[1] Rodrigo T. Doria,[1,3] and Jean-Pierre Colinge[1,a)]
[1]*Tyndall National Institute, University College Cork Lee Maltings, Prospect Row, Cork, Ireland*
[2]*Lashkaryov Institute of Semiconductor Physics, Kiev, Ukraine*
[3]*Departamento de Engenharia Elétrica, CentroUniversitário da FEI, São Bernardo do Campo, Brazil and LSI/PSI/USP/University of São Paulo, São Paulo, Brazil*

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The improvement of subthreshold slope due to impact ionization is compared between "standard" inversion-mode multigate silicon nanowire transistors and junctionless transistors. The length of the region over which impact ionization takes place, as well as the amplitude of the impact ionization rate are found to be larger in the junctionless devices, which reduces the drain voltage necessary to obtain a sharp subthreshold slope. © *2010 American Institute of Physics*. [doi:10.1063/1.3358131]

The active power consumption of transistors and integrated circuits is proportional to the square of the supply voltage. On-chip supply voltage has been reduced from 5 to 1.1 V during the past 20 years, and supply voltages as low as 0.6 V are being contemplated for future low-power applications. The off-to-on switching capability of the metal-oxide-semiconductor field-effect transistor (MOSFET) is represented by the slope of the drain current-gate voltage curve in subthreshold operation, called the "subthreshold slope." The subthreshold slope of a classical transistor has a theoretical best value limit of 60 mV/decade at room temperature. That value of subthreshold slope is, unfortunately, no longer sufficient to ensure high on/off current ratios when supply voltages as low as 0.6 V are contemplated, and it becomes desirable to design transistors that have a subthreshold slope lower than the theoretical limit of 60 mV/decade.

Impact ionization can be used in silicon-in-insulator (SOI) MOSFETs to obtain subthreshold slopes below $(kT/q)\ln(10)=60$ mV/decade at room temperature. The mechanism for subthreshold slope reduction involves impact ionization in the high-field region found at the drain junction when the device is in saturation. The hole current generated by impact ionization (we consider here an n-channel device) increases the potential of the transistor body in the channel region, which in turn decreases threshold voltage and increases the drain current. The increase of current increases the impact ionization rate, which completes a positive-feedback loop. As a result of this positive feedback the device current latches rapidly from the off to the on state and subthreshold slopes below 60 mV per decade can be observed. This effect was first described by Davis *et al.*[1] in 1982 and has been widely documented since.

Table I lists different publications describing measurement of subthreshold slope reduction using impact ionization. The Table lists the value of the subthreshold slope (*SS*) as well as the number of decades of drain current over which the effect is observed. To be complete, one needs to mention that "parasitic" bipolar junction transistor action in the MOSFET's NPN structure can also be triggered, which accentuates the effect and creates hysteresis in the $I_D(V_G)$ curves.[2–5]

It is generally accepted that the threshold energy for impact ionization is 1.5 times the energy band gap at room temperature which corresponds to 1.68 eV in the case of silicon but impact ionization currents have been detected in MOSFETs for drain voltages as low as 1.1 V.[6] A heavily doped MOSFET without junctions, called the junctionless multigate transistor, has recently been proposed. The device is a multigate silicon nanowire (or nanoribbon) with a pi-gate (multigate) architecture and a uniform, heavy doping concentration across the device.[7,8] The fabricated devices reported here have a width ranging from 20 to 50 nm, a thickness ranging from 5 to 10 nm and a gate length of 1 μm. The gate oxide thickness is 10 nm and the buried oxide thickness is 340 nm. The junctionless transistors are n-channel devices with a unoform n-type doping concentration of 10^{19} cm^{-3} in the source, drain and channel region. A

TABLE I. Subthreshold slope (*SS*), drain voltage (V_{DS}), number of decades over which SS$<$60 mV/decade, year of publication, type of measurement, and material used to fabricate SOI MOSFETs with impact-ionization reduction of the subthreshold slope.

SS (mV/dec)	V_{DS} (V)	Decades	Year	Measurement	Material	Ref.
130→73	3	4	1986	Experiment	Si	1
20	5	5	1990	Experiment+simulation	Si	3
$<$5	1	1	2008	Simulation	Si	4
$<$5	1	5	2008	Simulation	Ge	4
$<$10	11.6	2	2008	Experiment	Si	5

a)Electronic mail: jean-pierre.colinge@tyndall.ie.

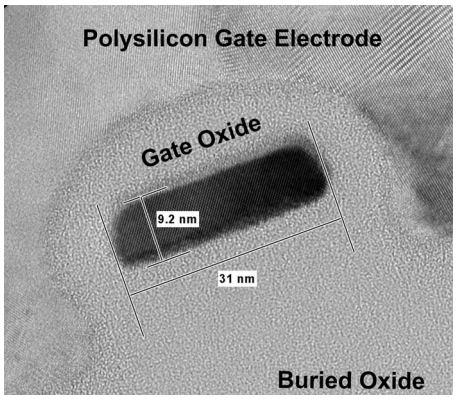

FIG. 1. High-resolution TEM cross section of a junctionless nanowire silicon transistor.

high-resolution TEM picture of the cross section of a junctionless transistor is shown in Fig. 1. "Standard" inversion-mode pi-gate MOSFETs were fabricated as well. These have the same dimensions as the junctionless devices, but have a p-type channel doping concentration of 2×10^{18} cm^{-3} and an n-type doping concentration of 10^{20} cm^{-3} in the source and drain. The junctionless devices have a P^+-polysilicon gate electrode and the pi-gate MOSFETs have an N^+-polysilicon gate.

Figure 2 shows the measured drain current as a function of gate voltage in an inversion-mode pi-gate MOSFET. The device width is 40 nm and the channel length is 1 μm. When a drain voltage, V_{DS}, of 3 V is applied, the subthreshold slope, *SS*, is 63 mV/decade. V_{DS} needs to be increased to 3.5 V or higher to obtain sub-60 mV/dec slopes. The curves are shown for both forward and reverse V_G scans, and very little hysteresis is observed.

Figure 3 shows the measured drain current as a function of gate voltage in a junctionless MOSFET. The device dimensions are the same as in Fig. 2. In this device, sub-60

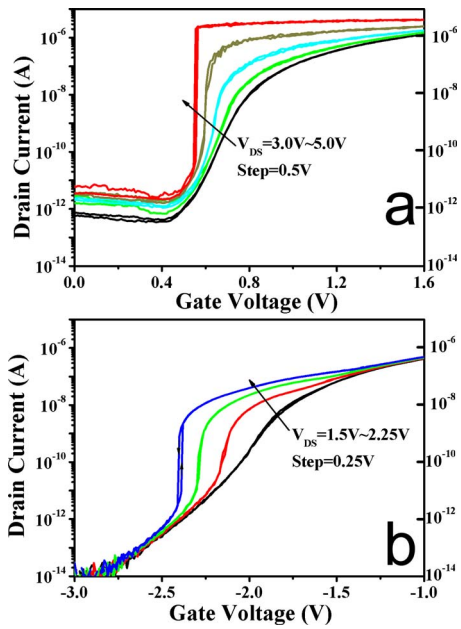

FIG. 2. (Color online) (a) Measured drain current vs gate voltage in an inversion-mode pi-gate nanowire MOSFET. W_{si}=40 nm, T_{si}=8 nm, L=1 μm; (b) Measured drain current vs gate voltage in a junctionless pi-gate nanowire MOSFET. W_{si}=40 nm, T_{si}=8 nm, L=1 μm.

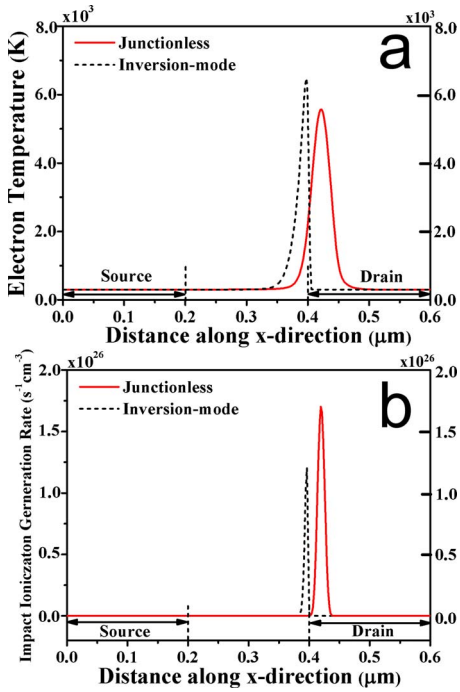

FIG. 3. (Color online) Simulated electron temperature (a) and Impact ionization rate (b) from source to drain in an inversion-mode pi-gate nanowire MOSFET and a junctionless pi-gate nanowire MOSFET. V_{DS}=2.2 V, $V_{GS}=V_{TH}-200$ mV.

mV/dec subthreshold slope appears for a drain voltage as low as 1.75 V, i.e., approximately half value needed for the standard inversion-mode device. A drain voltage of 1.75 V corresponds to 1.56 times the band gap energy of silicon.

In order to understand why the effect of impact ionization is larger in the junctionless device, we have used numerical simulation tools. The devices were simulated using the ATLAS simulator[9] using the following parameters for the junctionless devices: Silicon nanowire width, W_{si}=20 nm; silicon nanowire thickness, T_{si}=5 nm, gate oxide thickness, T_{ox}=10 nm, a gate length of 200 nm, and source/drain extension length of 200 nm. The uniform n-type doping concentration in the nanowire is $N_D=10^{19}$ cm^{-3}. Inversion-mode pi-gate MOSFETs were simulated as well using the same parameters as the junctionless devices, but with p-type channel doping concentration of 2×10^{18} cm^{-3} in the channel region and n-type doping concentration of 10^{20} cm^{-3} in the source and drain.

Figure 3 shows the electron temperature and rate of impact ionization from the source contact (at x=0) to the drain contact (at x=0.6 μm). The part of the device covered by the gate electrode extends from x=0.2 to 0.4 μm. The drain voltage is 2.2 V and the gate voltage is set to be 200 mV lower than V_{TH}, which is approximately the gate voltage at which corresponds the regions of minimum subthreshold slopes are observed in Figs. 2(a) and 2(b). The devices are turned off, and as expected, a high electric field is found at the drain junction of the inversion-mode pi-gate MOSFET, which holds the bulk of the applied drain bias. The peak field is in the channel region, right next to the metallurgical junction. In the junctionless device, the drain potential drop is found inside the drain electrode, outside of the region covered by the gate. This is because current blocking is caused by pure electrostatic pinchoff of the heavily doped nanowire structure. The entire channel region is pinched off, and the

bulk of the drain potential drop is found in the drain, near the gate electrode. Figure 3(a) shows the electron temperature from source to drain in both devices. The impact ionization multiplication factor (M-1) is related to the electron temperature T_e by the following relationship:

$$(M-1) = \int \alpha T_e(x) dx, \quad (1)$$

where α is the ionization rate.[10] In a classical device with junctions, the highest electron temperature is reached in the channel region next to the drain junction. In the junctionless device, on the other hand, the region of high electric field which accelerates the electrons to high temperatures, is located in the drain itself. As can be seen from Fig. 3(a), the peak electron temperature is slightly lower in the junctionless device than in the trigate FET, but the high T_e region extends over a wider area, such that the integration of (1) yields a larger multiplication factor is larger in the junctionless device. In addition, band gap narrowing in silicon amounts to 67 and 157 meV for doping concentrations $N_D = 10^{19}$ and 5×10^{19} cm^{-3}, respectively,[11] which can increase ionization rate coefficient in an non-negligible way in the heavily doped junctionless device.

The impact ionization rate from source to drain is shown in Fig. 3(b). In the junctionless device, the peak of ionization is found well inside the drain. The integration of the impact ionization rate over the entire device yields a generation current in the junctionless device that is equal to a few hundred picoamperes, which is significantly larger than the current in absence of impact ionization. This increases the total drain current and causes a reduction of V_{TH}. A positive feedback loop mechanism is thus triggered as the current is impact ionization is produced. This gives rise to the sharp threshold slope is observed in Fig. 2(b). The junctionless structure seems more efficient than the inversion-mode structure at increasing the length of the impact ionization region and, therefore, at maximizing the mechanism that causes a sharp subthreshold slope. Based on these observations, one can speculate that using the junctionless architecture on germanium nanowire transistors (band gap energy=0.6 V), it might be possible to obtain sub-60 mV/dec slopes for drain voltages of 1 V or less.

In conclusion, impact ionization is compared between standard inversion-mode multigate silicon transistors and junctionless transistors. The region over which impact ionization takes place is found to be much larger in the junctionless devices, which reduces the drain voltage necessary to obtain a sharp subthreshold slope. Based on these observations, one can speculate that using the junctionless MOSFET on germanium might make it possible to obtain sub-60 mV/dec slopes for drain voltages of 1 V or less.

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