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Temperature and frequency dependent electrical characterization of $HfO_2/In_xGa_{1-x}As$ interfaces using capacitance-voltage and conductance methods

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Electrical properties of metal-oxide-semiconductor capacitors using atomic layer deposited HfO_2 on *n*-type GaAs or $In_xGa_{1-x}As$ (x=0.53, 0.30, 0.15) epitaxial layers were investigated. Capacitance-voltage (*CV*) measurements indicated large temperature and frequency dispersion at positive gate bias in devices using *n*-type GaAs and low In content (x=0.30, 0.15) $In_xGa_{1-x}As$ layers, which is significantly reduced for devices using $In_{0.53}Ga_{0.47}As$. For $In_{0.53}Ga_{0.47}As$ devices, the *CV* response at negative gate bias is most likely characteristic of an interface state response and may not be indicative of true inversion. The conductance technique on $Pd/HfO_2/In_{0.53}Ga_{0.47}As/InP$ shows reductions in interface state densities by $In_{0.53}Ga_{0.47}As$ surface passivation and forming gas annealing (325 °C). © *2009 American Institute of Physics*. [DOI: 10.1063/1.3089688]

One of the main technological challenges associated with the fabrication of devices incorporating high dielectric constant (k) gate materials on III-V channels is the understanding of electrically active interface state defects and their passivation. Recent studies investigating high-k oxides on Si reveal interface state defects similar to those observed in the SiO_2/Si system.[1] However, the interface chemistry for high-k materials on III-V substrates is a more complex system, with the possibility for more than one substrate element, and its native oxides, to contribute to interfacial defects. The detrimental effect of high interface state density (D_{it}) on high-k/III-V device characteristics has motivated extensive research on both *in situ* and *ex situ* passivation of the high-k/III-V interface in an attempt to reduce D_{it}.[2–7] In this work we examine the electrical properties of atomic layer deposited (ALD) HfO_2 thin films on *n*-type GaAs or $In_xGa_{1-x}As$ (x=0.53, 0.30, 0.15) layers with Pd metal gates. The motivation for this approach is to assess whether the change of energy gap from GaAs (~1.42 eV) to $In_{0.53}Ga_{0.47}As$ (~0.75 eV) is reflected in a change in electrically active interface defects. A detailed D_{it} analysis for unpassivated and passivated $Pd/HfO_2/n\text{-}In_{0.53}Ga_{0.47}As/InP$ structures using the conductance method developed for the SiO_2/Si system is also presented.[8] In addition, the effect of low temperature forming gas annealing (FGA) on the electrical properties of unpassivated $Pd/HfO_2/n\text{-}In_{0.53}Ga_{0.47}As/InP$ structures is examined.

The $In_xGa_{1-x}As$ device stacks employed InP substrates [S: $(1-3)\times10^{18}$], for x=0.53, or GaAs substrates (Si: 5×10^{17}), for x=0.30 and 0.15, on which buffer layers were grown prior to growth of the epitaxial layers. The buffer layers (and doping concentrations) for $In_xGa_{1-x}As$ were 0.1 μm InP (S: 2×10^{18}), 0.35 μm GaAs (Si: $1\times10^{17}/cm^3$), 1 μm GaAs (Si: $1\times10^{17}/cm^3$), for x of 0.53, 0.30, and 0.15, respectively. The epitaxial layer thickness (and doping) of the $In_xGa_{1-x}As$ was 2 μm (S: 4×10^{17}), 0.05 μm (Si: $1\times10^{17}/cm^3$), 0.03 μm (Si: $1\times10^{17}/cm^3$), for x of 0.53, 0.30, and 0.15, respectively. The $In_xGa_{1-x}As$ (x=0.53, 0.15) epitaxial layers were grown by metal-organic vapor-phase epitaxy, as was the InP buffer layer, whereas the $In_{0.30}Ga_{0.70}As$ epitaxial layer and all GaAs layers were grown by molecular beam epitaxy. In the case of the GaAs (Si: 5×10^{17}) sample, no subsequent growth of a buffer layer was performed. All HfO_2 layers were deposited in a separate ALD reactor at 250 °C by alternating pulses of H_2O and the HfO_2 precursor TDMA-Hf ($Hf[N(CH_3)_2]_4$), the first pulse being that of the Hf precursor. Capacitor structures were completed by vacuum evaporation of ~100 nm of Pd (deposition rate of ~2.5 Å/s) using a lift-off process. No Ohmic back contacts to the devices were formed. The *ex situ* three-stage passivation was performed prior to ALD growth as follows: 3.7% HCl, 3 min at 25 °C; 3% NH_4OH, 3 min at 25 °C; 1% $(NH_4)_2S$, 5 min at 75 °C; rinse in de-ionized water; and blow dry wafers with N_2.[9] FGA ($5\%H_2/95\%N_2$) was performed cumulatively after gate metallization at 250 and 325 °C for 30 min.

Figures 1(a) and 1(b) present *CV* responses (10 kHz) for a range of measurement temperatures (−50 to 75 °C) for $In_{0.53}Ga_{0.47}As$ and GaAs devices, respectively. By varying the measurement temperature, it has been shown to be possible to access interface defects over an increased portion of the semiconductor energy gap and assess their effect on the *CV* characteristics.[10] Room temperature *CV* multifrequency responses for the $In_{0.53}Ga_{0.47}As$ and GaAs devices are shown as the insets to Figs. 1(a) and 1(b), respectively. Devices fabricated on $In_{0.15}Ga_{0.85}As$ and $In_{0.30}Ga_{0.70}As$ epitaxial layers display very similar temperature dependent and multifrequency *CV* profiles (not shown) to that of the GaAs. The average percentage capacitance dispersions per decade of frequency at a gate voltage V_{gate}=4 V are ~ 30%, 15%, and 23%, for GaAs, $In_{0.15}Ga_{0.85}As$, and $In_{0.30}Ga_{0.70}As$, respec-

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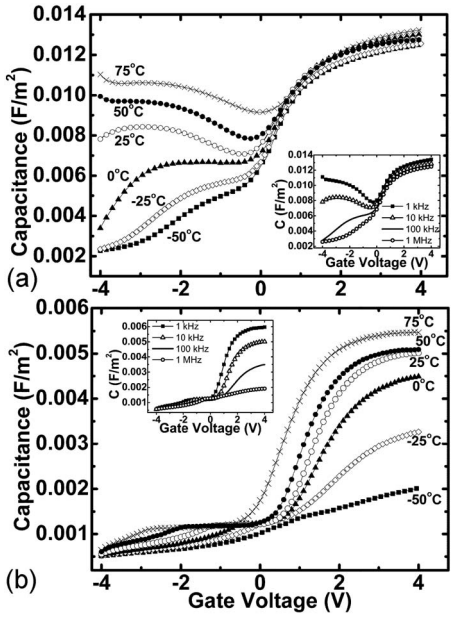

FIG. 1. 10 kHz *CV* response with varying temperature (−50 to 75 °C) of (a) unpassivated Pd/9.5 nm ALD HfO_2/n-$In_{0.53}Ga_{0.47}As/InP$ and (b) unpassivated Pd/11.4 nm ALD HfO_2/n-GaAs. The average percentage capacitance dispersions per 25 °C step of the temperature (−50 to 75 °C) at V_{gate}=4 V are 1.7% ($In_{0.53}Ga_{0.47}As$), 8.5% ($In_{0.30}Ga_{0.70}As$), 6.9% ($In_{0.15}Ga_{0.85}As$), and 16.7% (GaAs). Insets (a) and (b) show corresponding room temperature *CV* frequency variation (1 kHz to 1 MHz) in unpassivated $In_{0.53}Ga_{0.47}As$ and GaAs devices, respectively. The thicknesses of the [HfO_2, and interface oxide layer (IL)] for unpassivated $In_xGa_{1-x}As$ and GaAs devices measured by transmission electron microscopy are as follows: $In_{0.53}Ga_{0.47}As$ (9.5 nm, 1.0 nm), $In_{0.30}Ga_{0.70}As$ (9.2 nm, 0.9 nm), $In_{0.15}Ga_{0.85}As$ (14.0 nm, 1.1 nm), and GaAs (11.4 nm, 1.3 nm).

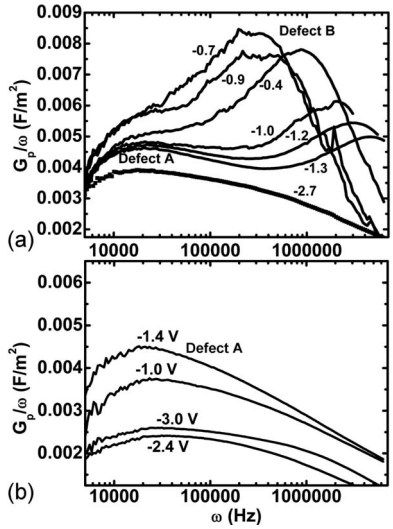

FIG. 2. G_p/ω vs ω ($\omega=2\pi\times$frequency) at 75 °C for selected and representative gate voltage bias points (indicated), for (a) unpassivated and (b) three-stage *ex situ* passivated Pd/10.3 nm ALD HfO_2/n-$In_{0.53}Ga_{0.47}As/InP$. IL thickness for the passivated $In_{0.53}Ga_{0.47}As$ device is 1.3 nm.

tively. This is reduced to <3% for $In_{0.53}Ga_{0.47}As$ devices. It should be noted that the $In_{0.30}Ga_{0.70}As$ epitaxial layer (0.05 μm) is beyond the critical thickness (0.012 μm) contributing to a higher number of dislocations in this epitaxial layer. For the $In_{0.53}Ga_{0.47}As$ devices, there is little variation in capacitance at V_{gate}=4 V with either temperature [Fig. 1(a)] or frequency [Fig. 1(a) inset], indicating that the devices are most likely in accumulation and that it is possible to move the Fermi level (E_f) at the $In_{0.53}Ga_{0.47}As/HfO_2$ interface to the conduction band edge (E_c). However, for the GaAs substrate, the large capacitance dispersion with temperature [Fig. 1(b)] and frequency [Fig. 1(b) inset] at V_{gate} =4 V suggests that the interface state capacitance (C_{it}) dominates the semiconductor (C_s) and oxide capacitance (C_{ox}). For this case of $C_{it} \gg C_{ox}$, the fact that the measured capacitance can approach the value of C_{ox} does not necessarily imply that the devices are in accumulation.[2,11,12] The observation that we can achieve accumulation for $In_{0.53}Ga_{0.47}As$, but not for $In_{0.30}Ga_{0.70}As$, $In_{0.15}Ga_{0.85}As$, and GaAs, suggests the presence of interface defects, which become electrically inactive as the energy gap of the semiconductor is changed from GaAs to $In_{0.53}Ga_{0.47}As$. Theeten *et al.*[13] observed a similar effect where a defect response, which is dominant in the case of lower In content (<0.35) devices, becomes insignificant for higher In content devices. The values of the energy gap and electron affinity are $In_{0.53}Ga_{0.47}As$ (0.75 and 4.5 eV), $In_{0.30}Ga_{0.70}As$ (1.01 and 4.31 eV), $In_{0.15}Ga_{0.85}As$ (1.21 and 4.19 eV), and GaAs (1.43 and 4.07 eV).[14,15] These values indicate the defects responsible for the observed frequency dispersion at positive gate bias for GaAs and $In_xGa_{1-x}As$ (x=0.15, 0.30) devices, are located in the range 4.07 to 4.5 eV from the vacuum level. Atomic identification of the defects is beyond the capabilities of the electrical characterization techniques used in the present study.[16]

In the case of the $In_{0.53}Ga_{0.47}As$ stack, the dispersion observed in the *CV* as a function of both temperature and frequency, for V_{gate} in the range of −1 V to −4 V, is characteristic of interface defects and is unlikely to be representative of true inversion at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface.[17] Similar frequency dependent *CV* profiles to those in the inset to Fig. 1(a) have previously been reported irrespective of the high-k layer, passivation approach, and $In_{0.53}Ga_{0.47}As$ growth method, suggesting that these interface states originate from the $In_{0.53}Ga_{0.47}As$ surface or interfacial oxides.[3–5] With respect to GaAs, frequency dispersion in the depletion region has been observed by Brammertz *et al.* for devices at temperatures higher than 120 °C, which are attributed to mid-gap interface states in GaAs.[18]

In quantifying the interface state defect density contributions to the *CV* and *GV* responses, the conductance technique, as developed for Si/SiO_2 systems, is applied here to the $Pd/HfO_2/In_{0.53}Ga_{0.47}As/InP$ devices.[8,19,20] The technique involves measuring the capacitance and conductance at a constant V_{gate} while applying a logarithmic frequency sweep from 50 Hz to 1 MHz. The analysis inherently assumes the $HfO_2/In_{0.53}Ga_{0.47}As$ surface is in depletion where only majority carriers interact with the interface traps, and an accurate estimate of D_{it} can be extracted. If the $HfO_2/In_{0.53}Ga_{0.47}As$ surface is in weak inversion, the analysis will significantly overestimate the D_{it} value.[21]

Figures 2(a) and 2(b) show estimates of G_p/ω versus ω curves for unpassivated and three-stage passivated $Pd/HfO_2/In_{0.53}Ga_{0.47}As/InP$ structures, respectively. The measurement temperature is 75 °C for all devices, as no G_p/ω peaks were observed at −50 and 25 °C. The plot in Fig. 2(a) shows two maximum peak profiles at low and high angular frequencies, and at different gate voltages within depletion, which may possibly be characteristic of two defects with distinct energy levels, termed (A) and (B), re-

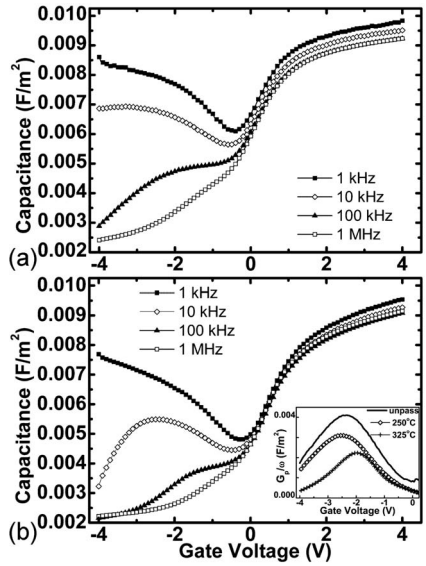

FIG. 3. Room temperature *CV* frequency variation (1 kHz to 1 MHz) in (a) unpassivated and (b) post-325 °C FGA, Pd/HfO_2/*n*-$In_{0.53}Ga_{0.47}As$/InP devices. The average percentage capacitance dispersions per decade of frequency (1 kHz to 1 MHz) at V_{gate}=4 V are 2.4%, 2.4%, and 1.8% for the unannealed, post-250 °C FGA, and post-325 °C FGA devices, respectively. The inset to (b) shows G_p/ω vs V_{gate} for an unpassivated $In_{0.53}Ga_{0.47}As$ device, and following 250 and 325 °C postmetallization FGA.

spectively. Similar methods have been used to analyze multiple defects in SiO_2/Si systems.[22] A peak D_{it} of 1.7×10^{13} $cm^{-2}\,eV^{-1}$ is calculated for defect (A) and 1.5×10^{13} $cm^{-2}\,eV^{-1}$ for defect (B). Figure 2(b) shows the G_p/ω versus ω plots for the three-stage passivated $In_{0.53}Ga_{0.47}As$ devices, with similarly broad profiles to those reported by Mui *et al.*[20] for $Si_3N_4/In_{0.53}Ga_{0.47}As$ interfaces. No peak for defect (B) is evident, while for defect (A) D_{it} is estimated to be 1.6×10^{13} $cm^{-2}\,eV^{-1}$. The similarity in the defect (A) D_{it} indicates that the three-stage surface passivation has had little impact on this defect, while it significantly reduces the contribution of defect (B).

Figures 3(a) and 3(b) show room temperature *CV* multifrequency responses for unpassivated and post-325 °C FGA, Pd/HfO_2/*n*-$In_{0.53}Ga_{0.47}As$/InP devices, respectively. The FGA results in a noticeable reduction in the frequency dispersion both at V_{gate}=4 V and also in the transition region from depletion to accumulation at $V_{gate}\sim0$ to 1 V. The *CV* dispersion for V_{gate} in the range of −1 to −4 V, which is characteristic of interface defects, is also visibly reduced following 325 °C FGA. The inset to Fig. 3(b) shows the relative reductions in the maximum peaks of G_p/ω versus V_{gate} for an unpassivated $In_{0.53}Ga_{0.47}As$ device, and following 250 and 325 °C postmetallization FGAs. We see a reduction in the maximum peak magnitude of G_p/ω from the pre-FGA unpassivated device to the post-FGA at 325 °C device, as well as a change in peak profile, corresponding to a total estimated D_{it} of 1.0×10^{13} $cm^{-2}\,eV^{-1}$ from defect (A) only, for the 325 °C post-FGA device, with no clear evidence of a peak for defect (B). Similar improvements in the *CV* frequency dispersion and in the relative peaks of G_p/ω versus V_{gate} have also been observed in post-325 °C FGA devices employing a Pt gate electrode.

In summary, it is found that the large temperature and frequency dispersion in *CV* responses at positive gate bias for devices with HfO_2 layers on *n*-type GaAs and low In content (x=0.30, 0.15) $In_xGa_{1-x}As$ is significantly reduced using high In content (x=0.53) epitaxial layers, suggesting that it is only possible to achieve true accumulation for the $In_{0.53}Ga_{0.47}As$ devices. However, the *CV* responses at negative gate bias indicate a significant interface state contribution and may not be representative of true inversion at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface. An estimation of D_{it} using the conductance technique indicates that densities for these $HfO_2/In_{0.53}Ga_{0.47}As$ devices remain too high for practical device applications, but it has been shown that a three-stage $In_{0.53}Ga_{0.47}As$ surface passivation and postmetallization FGA at 325 °C can provide a significant reduction in interface state defect densities.

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