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In situ H$_2$S passivation of In$_{0.53}$Ga$_{0.47}$As/InP metal-oxide-semiconductor capacitors with atomic-layer deposited HfO$_2$ gate dielectric

E. O’Connor, R. D. Long, K. Cherkaoui, K. K. Thomas, F. Chalvet, I. M. Povey, M. E. Pemble, and P. K. Hurley
Tyndall National Institute, University College Cork, Lee Maltings, Prospect Row, Cork, Ireland

B. Brennan and G. Hughes
School of Physics, Dublin City University, Glasnevin, Dublin 9, Ireland

S. B. Newcomb
Glebe Scientific, Ltd., Newport, County Tipperary, Ireland

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We have studied an in situ passivation of In$_{0.53}$Ga$_{0.47}$As, based on H$_2$S exposure (50–350 °C) following metal organic vapor phase epitaxy growth, prior to atomic layer deposition of HfO$_2$ using Hf[N(CH$_3$)$_2$]$_4$ and H$_2$O precursors. X-ray photoelectron spectroscopy revealed the suppression of As oxide formation in air exposed InGaAs surfaces for all H$_2$S exposure temperatures. Transmission electron microscopy analysis demonstrates a reduction of the interface oxide between the In$_{0.53}$Ga$_{0.47}$As epitaxial layer and the amorphous HfO$_2$ resulting from the in situ H$_2$S passivation. The capacitance-voltage and current-voltage behavior of Pd/HfO$_2$/In$_{0.53}$Ga$_{0.47}$As/InP structures demonstrates that the electrical characteristics of samples exposed to 50 °C H$_2$S at the end of the metal-organic vapor-phase epitaxy In$_{0.53}$Ga$_{0.47}$As growth are comparable to those obtained using an ex situ aqueous (NH$_4$)$_2$S passivation. © 2008 American Institute of Physics.

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In order to continue complementary metal oxide semiconductor (CMOS) development beyond the 22 nm node, alternative channel materials in combination with high dielectric constant (k) gate layers are currently under investigation. One of these approaches is to use high-mobility III-V materials such as InGaAs and GaAs as channel layers. In GaAs and GaAs channel layers, high mobility substrates offer the potential for increased transconductance at reduced voltages, increasing performance at supply voltages ≤1 V. However, a significant factor which has contributed to the use of such materials is the lack of stable, high quality gate insulators on III-V channels. A gate oxide is required with high dielectric constant and sufficiently low density of interface states to avoid Fermi level pinning at the interface with the III-V substrate. As atomic layer deposition (ALD) of high-k dielectrics on Si is becoming a reality in manufactured devices, recent research is investigating this approach for use in III-V based devices. A number of groups have also investigated surface passivation of the In$_{0.53}$Ga$_{0.47}$As substrate prior to oxide deposition. In situ gaseous passivation is preferable to ex situ aqueous techniques which are more likely to introduce contaminants such as C, Na, and heavy metals, as well as increasing InGaAs surface roughness. In addition, both ALD and MOVPE are more attractive techniques than MBE for use in manufacturing technology. In this work, we evaluate an in situ passivation performed at the end of the MOVPE growth of high indium content lattice matched In$_{0.53}$Ga$_{0.47}$As grown on InP substrates. The technique is based on the exposure of the In$_{0.53}$Ga$_{0.47}$As surface to H$_2$S at the end of the growth process, prior to gate dielectric formation. The approach is particularly suited to MOVPE III-V growth as H$_2$S is used as a n-type dopant source for InGaAs. The gate oxide employed in this work is ALD grown HfO$_2$ using the metal organic precursor Hf[N(CH$_3$)$_2$]$_4$.

In$_{0.53}$Ga$_{0.47}$As lattice-matched epitaxial layers of thickness 2 μm and S doped to 4 × 10$^{17}$/cm$^3$ were grown in a MOVPE system immediately following growth of a 0.1 μm InP buffer layer (S doped, 2 × 10$^{18}$/cm$^3$) on n-type InP(100) wafers (S doped, (1−3) × 10$^{18}$/cm$^3$). In situ passivation of the InGaAs surface was performed in the MOVPE chamber immediately after growth by flowing H$_2$S over the samples at a flow-rate of 0.1 SCCM (SCCM denotes cubic centimeter per minute at STP), at three different temperatures (50, 200, or 350 °C), for 90 min in a H$_2$ carrier gas. Subsequently the wafers were moved to an ex situ ALD reactor involving ~90 s ambient exposure. HfO$_2$ layers (~3−15 nm) were deposited at a temperature of 250 °C by alternating pulses of H$_2$O and the HfO$_2$ precursor Hf[N(CH$_3$)$_2$]$_4$, the initial pulse being that of the Hf precursor. MOS structures were completed by vacuum evaporation of ~100 nm of Pd using a deposition rate of 2.5 Å/s, and lift-off, to define capacitors of various areas. No Ohmic back contacts to the InP were formed. Ex situ aqueous sulfur (S) passivation was performed in ambient by dipping InGaAs/InP samples in (NH$_4$)$_2$S diluted to 20% in de-ionized water at ~60 °C for 20 min. The Pd/HfO$_2$/In$_{0.53}$Ga$_{0.47}$As/InP structures examined in this work experienced no annealing following either dielectric deposition or gate metal formation. Passivated InGaAs surfaces were studied using x-ray photoelectron spectroscopy (XPS), following ~60 s ambient exposure before loading to the XPS system, to evaluate the effectiveness of the in situ passivation approach in suppressing native oxide regrowth. XPS spectra of a sample passivated using ex situ aqueous (NH$_4$)$_2$S are also included for comparison. Figure 1(a) shows a comparison of the S 2s peak for all samples. XPS does detect S on the InGaAs surface for both the 350 °C in situ passivated sample and the ex...
situ aqueous S passivated sample, but in the case of the 50
and 200 °C in situ passivated samples no S is detected on
the surface. XPS spectra of the As 3d core level for the unpa-
ssivated and passivated samples are shown in Fig. 1(b). This
XPS peak is selected to examine the effect of the passivation
on suppressing native oxide growth due to the large chemical
shift between the As 3d peak and that of the arsenic oxide.
In the case of the unpassivated sample, a peak is observed at
≈45 eV and assigned to As$_2$O$_3$. In the case of all the in situ
passivated samples this peak is not evident, indicating that
this approach is effective in preventing As$_2$O$_3$ formation on
the InGaAs surface. This is desirable as it has been reported
that the unstable As$_2$O$_3$ can react to form elemental As which
will be in equilibrium with the H$_2$ MOVPE carrier gas may
assist in allowing H passivation to occur by reducing hydro-
gen desorption from the surface. The possibility that hydro-
gen passivation occurs in this process is subject to further
investigation.

Figure 2(a) compares high frequency capacitance voltage
(CV) curves for the unpassivated device and the various
in situ passivation approaches for a nominal ALD HfO$_2$
thickness of 9 nm. The minimum capacitance ($C_{\text{min}}$), at $V_g$
=−2 V, is approaching the expected theoretical value of
0.0019 F/m$^2$, calculated for these structures assuming inver-
sion at the InGaAs/HfO$_2$ interface.$^{13}$ The device fabricated
on the 50 °C in situ passivated surface (50 °C device) dis-
plays the highest maximum capacitance in accumulation ($C_{\text{max}}$) and also exhibits the sharpest transition from deple-
tion to accumulation. The inset of Fig. 2(a) shows the current
density-voltage (JV) characteristics for unpassivated and in situ
passivated MOS structures. All structures exhibit low leakage
current density (≈5×10$^{-7}$ A/cm$^2$ at $V_{th}$+1 V), demonstrating
that these ALD HfO$_2$ films on InGaAs are highly insulating. It is lowest in the case of the 50 °C device, 
≈5×10$^{-8}$ A/cm$^2$ at $V_{th}$+1 V. Figure 2(b) shows multifold
frequency CV curves measured over the range of
1 kHz–1 MHz for the 50 °C device. The low frequency CV
behavior observed in the 1 kHz curve has been reported pre-
viously in narrow bandgap materials.$^{14,16}$ The inset of Fig.
2(b) shows the CV hysteresis curve for the 50 °C device,
which has the lowest measured hysteresis, ≈380 mV around
$C_{\text{th}}$. These levels of frequency dispersion and hysteresis are to
be expected as no postdeposition thermal anneal was per-
fomed on these MOS structures.$^9$ The fact that the 50 °C
passivated device, which XPS showed to have no detectable
S signal at the surface, displays the best electrical properties
is further evidence that S is not the primary passivating ele-
ment for the in situ process. It is possible to speculate that
hydrogen may be passivating the InGaAs surface. One pos-
sibility is low temperature dissociative adsorption of H$_2$S
to produce H–S and H species which may bond to As at the
epitaxial layer surface. This has been observed in previous
studies of H$_2$S treatment of GaAs(001).$^{17}$ In addition, the
fact that H species formed on the surface by H$_2$S dissociation
will be in equilibrium with the H$_2$ MOVPE carrier gas may
assist in allowing H passivation to occur by reducing hy-
drogen desorption from the surface. The possibility that hy-
drogen passivation occurs in this process is subject to further
investigation.

Figure 3(a) shows a bright field transmission electron
microscopy (TEM) micrograph for a 50 °C in situ H$_2$S pas-
sivated InGaAs device with a 9.4 nm HfO$_2$ layer and a
0.8 nm thick interfacial layer (IL) between the HfO$_2$ and
InGaAs. This is less than half the thickness of the IL of
1.9 nm measured by TEM for the unpassivated device [Fig.
3(b)]. This indicates that this in situ passivation technique
is effective in significantly inhibiting interfacial oxide growth.
Considering that the maximum H$_2$S flow rate was limited to
0.1 SCCM in this MOVPE process, there is scope for refine-
ment and potential improvement of this in situ passivation
technique.

CV curves for a thickness series of 3, 9.4, and 16.8 nm
thick ALD HfO$_2$ layers on 50 °C in situ passivated InGaAs
are shown in Fig. 4(a). The inset plots the $C-V$ response for
the three thicknesses. As expected, the leakage current den-
sity at $V_{th}$+1 V is significantly higher for the 3 nm device,
≈2×10$^{-6}$ A/cm$^2$, compared to ≈3×10$^{-8}$ A/cm$^2$ and 2
×10$^{-8}$ A/cm$^2$ for the 9.4 and 16.8 nm devices, respectively.
slightly higher interface state density. The in situ CV both devices. Both devices have a similar passivated devices.

For these HfO₂ layers, we estimate a HfO₂ k value of ~23. Figure 4(b) compares the electrical characteristics of a 9.4 nm thick ALD HfO₂ layer (0.8 nm IL) deposited on InGaAs passivated in situ by H₂S flow at 50 °C, and an 11 nm thick ALD HfO₂ layer (1.3 nm IL) on InGaAs passivated ex situ in aqueous NH₄S. Although a slight V₉ shift is apparent, a similar profile is observed in the CV curves of both devices. Both devices have a similar C₀max in accumulation while the in situ passivated device appears to have slightly higher interface state density. The JV plot in the inset of Fig. 4(b) shows similar leakage current density at V₀ = +1 V with a higher electric breakdown field for the in situ passivated device. This demonstrates that the in situ passivation approach employed in this work can achieve results comparable to those obtained using ex situ aqueous (NH₄)₂S passivation.

In summary, we have studied an in situ passivation of In₀.۵₅Ga₀.۴۷As performed using the H₂S dopant source (50–350 °C) at the end of MOVPE growth prior to deposition of ALD HfO₂. XPS analysis revealed the suppression of As oxide growth on in situ passivated InGaAs layers. The MOS device, which experienced a passivation temperature of 50 °C, displays the best electrical characteristics, with TEM indicating a significant reduction in interfacial oxide thickness compared to the unpassivated and (NH₄)₂S passivated devices. The potential for developing this passivation approach for use in future CMOS applications is demonstrated by the fact that results comparable to those obtained using ex situ aqueous (NH₄)₂S passivation can be achieved.

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FIG. 3. Bright field TEM micrographs of Pd/9 nm(nominal) ALD HfO₂/InGaAs/InP MOS devices for (a) in situ 50 °C H₂S passivated InGaAs and (b) unpassivated InGaAs. The actual HfO₂ layer [and interfacial layer (IL)] thicknesses measured by TEM were 5.2 nm (1.9 nm IL) unpassivated device, 9.4 nm (0.8 nm IL) 50 °C device, 13.5 nm (0.9 nm IL) 200 °C device, 10.8 nm (0.9 nm IL) 350 °C device, and 11 nm (1.3 nm IL) (NH₄)₂S passivated device.

FIG. 4. (a) CV (100 kHz) curves and inset JV (same legend) for nominal 3, 9, and 15 nm thick ALD HfO₂ layers on 50 °C in situ passivated InGaAs. The actual HfO₂ (and IL) thicknesses from TEM were 3 nm (0.8 nm IL), 9.4 nm (0.8 nm IL), and 16.8 nm (0.9 nm IL). No significant degradation of the bulk and interface properties is observed after repeated CV measurement of the MOS structures. (b) CV (100 kHz) and inset IV (same legend) characteristics for in situ 50 °C H₂S passivated and ex situ aqueous (NH₄)₂S passivated devices.