In situ \( \text{H}_2\text{S} \) passivation of \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} / \text{InP} \) metal-oxide-semiconductor capacitors with atomic-layer deposited \( \text{HfO}_2 \) gate dielectric

E. O’Connor, R. D. Long, K. Cherkaoui, K. K. Thomas, F. Chalvet, I. M. Povey, M. E. Pemble, and P. K. Hurley

B. Brennan and G. Hughes

S. B. Newcomb

Citation: Appl. Phys. Lett. 92, 022902 (2008); doi: 10.1063/1.2829586

View online: http://dx.doi.org/10.1063/1.2829586

View Table of Contents: http://aip.scitation.org/toc/apl/92/2

Published by the American Institute of Physics
**In situ** $\text{H}_2\text{S}$ passivation of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ metal-oxide-semiconductor capacitors with atomic-layer deposited $\text{HfO}_2$ gate dielectric

E. O’Connor, R. D. Long, K. Cherkaoui, K. K. Thomas, F. Chalvet, I. M. Povey, M. E. Pemble, and P. K. Hurley

Tyndall National Institute, University College Cork, Lee Maltings, Prospect Row, Cork, Ireland

B. Brennan and G. Hughes
School of Physics, Dublin City University, Glasnevin, Dublin 9, Ireland

S. B. Newcomb
Glebe Scientific, Ltd., Newport, County Tipperary, Ireland

(Received 13 July 2007; accepted 7 December 2007; published online 14 January 2008)

We have studied an *in situ* passivation of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, based on $\text{H}_2\text{S}$ exposure (50–350 °C) following metal organic vapor phase epitaxy growth, prior to atomic layer deposition of $\text{HfO}_2$ using $\text{Hf}[[\text{N(CH}_3)_2]_4$ and $\text{H}_2\text{O}$ precursors. X-ray photoelectron spectroscopy revealed the suppression of As oxide formation in air exposed InGaAs surfaces for all $\text{H}_2\text{S}$ exposure temperatures. Transmission electron microscopy analysis demonstrates a reduction of the interface oxide between the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ epitaxial layer and the amorphous $\text{HfO}_2$ resulting from the *in situ* $\text{H}_2\text{S}$ passivation. The capacitance-voltage and current-voltage behavior of Pd/$\text{HfO}_2$/$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ structures demonstrates that the electrical characteristics of samples exposed to 50 °C $\text{H}_2\text{S}$ at the end of the metal-organic vapor-phase epitaxy $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ growth are comparable to those obtained using an *ex situ* aqueous (NH$_4$)$_2$S passivation. © 2008 American Institute of Physics.

[DOI: 10.1063/1.2829586]

In order to continue complementary metal oxide semiconductor (CMOS) development beyond the 22 nm node, alternative channel materials in combination with high dielectric constant ($k$) gate layers are currently under investigation. One of these approaches is to use high-mobility III-V materials such as InGaAs and GaAs as channel layers. $^1$–$^6$ High mobility substrates offer the potential for increased transconductance at reduced voltages, increasing performance at supply voltages $\leq$1 V. However, a significant factor which has inhibited the use of such materials is the lack of stable, high quality gate insulators on III-V channels. A gate oxide is required with high dielectric constant and sufficiently low density of interface states to avoid Fermi level pinning at the interface with the III-V substrate. As atomic layer deposition (ALD) of high-$k$ dielectrics on Si is becoming a reality in manufactured devices, recent research is investigating this approach for use in III-V based devices. $^7$–$^8$ A number of groups have also investigated surface passivation of the In$_x$Ga$_{1-x}$As substrate prior to oxide deposition. $^9$–$^{11}$ *In situ* gaseous passivation is preferable to *ex situ* aqueous techniques which are more likely to introduce contaminants such as C, Na, and heavy metals, as well as increasing InGaAs surface roughness. In addition, both ALD and MOVPE are more attractive techniques than MBE for use in manufacturing technology. In this letter, we evaluate an *in situ* passivation performed at the end of the MOVPE growth of high indium content lattice matched In$_{0.53}$Ga$_{0.47}$As grown on InP substrates. The technique is based on the exposure of the In$_{0.53}$Ga$_{0.47}$As surface to $\text{H}_2\text{S}$ at the end of the growth process, prior to gate dielectric formation. The approach is particularly suited to MOVPE III-V growth as $\text{H}_2\text{S}$ is used as a $n$-type dopant source for InGaAs. The gate oxide employed in this work is ALD grown $\text{HfO}_2$ using the metal organic precursor $\text{Hf}[[\text{N(CH}_3)_2]_4$. $^{12}$

In$_{0.53}$Ga$_{0.47}$As lattice-matched epitaxial layers of thickness 2 $\mu$m and S doped to $4 \times 10^{17}/\text{cm}^3$, were grown in a MOVPE system immediately following growth of a 0.1 $\mu$m InP buffer layer (S doped, $2 \times 10^{19}/\text{cm}^3$) on $n$-type InP(100) wafers (S doped, $(1–3) \times 10^{16}/\text{cm}^3$). *In situ* passivation of the InGaAs surface was performed in the MOVPE chamber immediately after growth by flowing $\text{H}_2\text{S}$ over the samples at a flow-rate of 0.1 SCCM (SCCM denotes cubic centimeter per minute at STP), at three different temperatures (50, 200, or 350 °C), for 90 min in a $\text{H}_2$ carrier gas. Subsequently the wafers were moved to an *ex situ* ALD reactor involving $\sim$90 s ambient exposure. $\text{HfO}_2$ layers ($\sim 3$–$\sim 15$ nm) were deposited at a temperature of 250 °C by alternating pulses of $\text{H}_2\text{O}$ and the $\text{HfO}_2$ precursor $\text{Hf}[[\text{N(CH}_3)_2]_4$, the initial pulse being that of the $\text{Hf}$ precursor. MOS structures were completed by vacuum evaporation of $\sim 100$ nm of Pd using a deposition rate of 2.5 Å/s, and lift-off, to define capacitors of various areas. No Ohmic back contacts to the InP were formed. *Ex situ* aqueous sulfur (S) passivation was performed in ambient by dipping InGaAs/InP samples in (NH$_4$)$_2$S diluted to 20% in de-ionized water at $\sim 60$ °C for 20 min. The Pd/$\text{HfO}_2$/$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ structures examined in this work experienced no annealing following either dielectric deposition or gate metal formation.

Passivated InGaAs surfaces were studied using x-ray photoelectron spectroscopy (XPS), following $\sim$60 s ambient exposure before loading to the XPS system, to evaluate the effectiveness of the *in situ* passivation approach in suppressing native oxide regrowth. XPS spectra of a sample passivated using *ex situ* aqueous (NH$_4$)$_2$S are also included for comparison. Figure 1(a) shows a comparison of the S 2$s$ peak for all samples. XPS does detect S on the InGaAs surface for both the 350 °C *in situ* passivated sample and the *ex
situ aqueous S passivated sample, but in the case of the 50 and 200 °C in situ passivated samples no S is detected on the surface. XPS spectra of the As 3d core level for the unpassivated and passivated samples are shown in Fig. 1(b). This XPS peak is selected to examine the effect of the passivation on suppressing native oxide growth due to the large chemical shift between the As 3d peak and that of the arsenic oxide. In the case of the unpassivated sample, a peak is observed at ~45 eV and assigned to As2O3. In the case of all the in situ passivated samples this peak is not evident, indicating that this approach is effective in preventing As2O3 formation on the InGaAs surface. This is desirable as it has been reported that the unstable As2O3 can react to form elemental As which results in Fermi level pinning.10,13 The absence of S on the surface of the 50 and 200 °C samples and the fact that As2O3 formation was inhibited on both, indicate that S may not be the primary passivating element in this process.

Figure 2(a) compares high frequency capacitance voltage (CV) curves for the unpassivated device and the various in situ passivation approaches for a nominal ALD HfO2 thickness of 9 nm. The minimum capacitance (Cmin), at Vg = −2 V, is approaching the expected theoretical value of 0.0019 F/m2, calculated for these structures assuming inversion at the InGaAs/HfO2 interface.13 The device fabricated on the 50 °C in situ passivated surface (50 °C device) displays the highest maximum capacitance in accumulation (Cmax) and also exhibits the sharpest transition from depletion to accumulation. The inset of Fig. 2(a) shows the current density-voltage (JV) characteristics for unpassivated and in situ passivated MOS structures. All structures exhibit low leakage current density (<5 × 10−7 A/cm2) at Vth+1 V, demonstrating that these ALD HfO2 films on InGaAs are highly insulating. It is lowest in the case of the 50 °C device, ~5 × 10−8 A/cm2 at Vth+1 V. Figure 2(b) shows multifrequency CV curves measured over the range of 1 kHz–1 MHz for the 50 °C device. The low frequency CV behavior observed in the 1 kHz curve has been reported previously in narrow bandgap materials.14–16 The inset of Fig. 2(b) shows the CV hysteresis curve for the 50 °C device, which has the lowest measured hysteresis, ~380 mV around Cth. These levels of frequency dispersion and hysteresis are to be expected as no postdeposition thermal anneal was performed on these MOS structures.9 The fact that the 50 °C passivated device, which XPS showed to have no detectable S signal at the surface, displays the best electrical properties is further evidence that S is not the primary passivating element for the in situ process. It is possible to speculate that hydrogen may be passivating the InGaAs surface. One possibility is low temperature dissociative adsorption of H2S to produce H–S and H species which may bond to As at the epitaxial layer surface. This has been observed in previous studies of H2S treatment of GaAs(001).17 In addition, the fact that H species formed on the surface by H2S dissociation will be in equilibrium with the H2 MOVPE carrier gas may assist in allowing H passivation to occur by reducing hydrogen desorption from the surface. The possibility that hydrogen passivation occurs in this process is subject to further investigation.

Figure 3(a) shows a bright field transmission electron microscopy (TEM) micrograph for a 50 °C in situ H2S passivated InGaAs device with a 9.4 nm HfO2 layer and a 0.8 nm thick interfacial layer (IL) between the HfO2 and InGaAs. This is less than half the thickness of the IL of 1.9 nm measured by TEM for the unpassivated device [Fig. 3(b)]. This indicates that this in situ passivation technique is effective in significantly inhibiting interfacial oxide growth. Considering that the maximum H2S flow rate was limited to 0.1 SCCM in this MOVPE process, there is scope for refinement and potential improvement of this in situ passivation technique.

CV curves for a thickness series of 3, 9.4, and 16.8 nm thick ALD HfO2 layers on 50 °C in situ passivated InGaAs are shown in Fig. 4(a). The inset plots the JV response for the three thicknesses. As expected, the leakage current density at Vth+1 V is significantly higher for the 3 nm device, ~2 × 10−6 A/cm2, compared to ~3 × 10−8 A/cm2 and 2 × 10−7 A/cm2 for the 9.4 and 16.8 nm devices, respectively.
slightly higher interface state density. The passivated devices. Both devices have a similar passivated device. This demonstrates that the in situ passivation approach employed in this work can achieve results comparable to those obtained using ex situ aqueous (NH₄)₂S passivation.

In summary, we have studied an in situ passivation of In₀.₅₅Ga₀.₄₇As performed using the H₂S dopant source (50–350 °C) at the end of MOVPE growth prior to deposition of ALD HfO₂. XPS analysis revealed the suppression of As oxide growth on in situ passivated InGaAs layers. The MOS device, which experienced a passivation temperature of 50 °C, displays the best electrical characteristics, with TEM indicating a significant reduction in interfacial oxide thickness compared to the unpassivated and (NH₄)₂S passivated devices. The potential for developing this passivation approach for use in future CMOS applications is demonstrated by the fact that results comparable to those obtained using ex situ aqueous (NH₄)₂S passivation can be achieved.

The authors thank Dan O’Connell, Tyndall National Institute, for sample processing. The authors acknowledge useful discussions with Niti Goel, Wilman Tsai, and Marko Radosavljevic, Intel Corporation. The authors would like to acknowledge the following for financial support of this work: Science Foundation Ireland (05/I1N/1751); Irish Research Council for Science, Engineering, and Technology, Intel Ireland.

For these HfO₂ layers, we estimate a HfO₂ k value of ~23. For these HfO₂ layers, we estimate a HfO₂ k value of ~23. For these HfO₂ layers, we estimate a HfO₂ k value of ~23. For these HfO₂ layers, we estimate a HfO₂ k value of ~23. For these HfO₂ layers, we estimate a HfO₂ k value of ~23. For these HfO₂ layers, we estimate a HfO₂ k value of ~23. Figure 4(b) compares the electrical characteristics of a 9.4 nm thick ALD HfO₂ layer (0.8 nm IL) deposited on InGaAs passivated in situ by H₂S flow at 50 °C, and an 11 nm thick ALD HfO₂ layer (1.3 nm IL) on InGaAs passivated ex situ in aqueous (NH₄)₂S. Although a slight Vfb shift is apparent, a similar profile is observed in the CV curves of both devices. Both devices have a similar Cmax in accumulation while the in situ passivated device appears to have slightly higher interface state density. The JV plot in the inset of Fig. 4(b) shows similar leakage current density at Vfb +1 V with a higher electric breakdown field for the in situ passivated device. This demonstrates that the in situ passivation approach employed in this work can achieve results comparable to those obtained using ex situ aqueous (NH₄)₂S passivation.

FIG. 3. Bright field TEM micrographs of Pd/9 nm(nominal) ALD HfO₂/InGaAs/InP MOS devices for (a) in situ 50 °C H₂S passivated InGaAs and (b) unpassivated InGaAs. The actual HfO₂ layer (interfacial layer [IL]) thicknesses measured by TEM were 5.2 nm (1.9 nm IL) unpassivated device, 9.4 nm (0.8 nm IL) 50 °C device, 13.5 nm (0.9 nm IL) 200 °C device, 10.8 nm (0.9 nm IL) 350 °C device, and 11 nm (1.3 nm IL) (NH₄)₂S passivated device.

FIG. 4. (a) CV (100 kHz) curves and inset JV (same legend) for nominal 3, 9, and 15 nm thick ALD HfO₂ layers on 50 °C in situ passivated InGaAs. The actual HfO₂ (and IL) thicknesses from TEM were 3 nm (0.8 nm IL), 9.4 nm (0.8 nm IL), and 16.8 nm (0.9 nm IL). No significant degradation of the bulk and interface properties is observed after repeated CV measurement of the MOS structures. (b) CV (100 kHz) and inset JV (same legend) characteristics for in situ 50 °C H₂S passivated and ex situ aqueous (NH₄)₂S passivated devices.