A Passive Circuit Based RF Optimization Methodology for Wireless Sensor Network Nodes

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Keywords: Passive, Optimization Methodology, Return Loss, Wireless Node, RF performance.

Abstract. Return loss of wireless sensor network (WSN) node indicates the impedance matching between signal ports of the RF chip and the antenna, and thus shows the transmission efficiency in the signal path. All circuit components, including capacitors, inductors, PCB tracks, packaging parasitic and RF ports were modeled as equivalent passives, to achieve accurate simulation result of return loss of the WSN node. An optimization methodology of return loss was proposed based on the parameter sweep of the equivalent passive network simulation. With the help of the methodology, some critical components' values were changed to obtain optimized RF performance for the wireless node. Measurements matched the analysis and simulation well and showed great improvement.

Introduction

The design of WSN nodes is challenging due to the requirements for low cost, low power consumption and miniaturization. To meet these demands, in some cases, advanced packaging technologies such as wire bonding [1] and flip chip [2] were applied.

There were lots of researches and publications focus on the characterization [3, 4] of the above technologies. Characterization of the advanced packaging technologies was carried out and the material aspect properties were well studied. However, very little attention was paid to understanding the advanced packaging's impact on RF performance. The packaging impacts of the technologies are still not clear and also worth investigating.

On the other hand, circuits such as filter and balun were well understood as separate function blocks [5, 6]. Electrical engineers were used to designing all these circuit blocks for ordinary PCB and didn't know what would happen if using advanced packaging technologies.

So there is lack of methods to link all the advanced packaging technologies and essential circuit blocks in RF prospect of view. A methodology was proposed in this paper to solve this problem.

The return loss (or called scattering parameter S11) was used to indicate the level of impedance matching of the RF signal path. All the circuit elements, such as packaging, substrate, balun, parasitic and transmission lines, are modeled and put into the simulation of return loss. By doing so, a general methodology of performing system level analysis of RF circuit was provided. Based on the modeling and simulation, a parameter sweep procedure was carried out to obtain optimized return loss performance.

Design and Passive Modeling of the RF Circuit

The schematic of a typical WSN RF circuit, including antenna port, filter, balun, packaging and RF ports, is shown in Fig. 1. It is obvious that the RF circuit is active, which makes it rather difficult to be simulated.

In this paper, all the components were converted to their equivalent passive models and thus could be used for simulation in Spice or Ansoft Designer. Moreover, some advanced subjects like the PCB tracks and packaging parasitic were also models as passives.

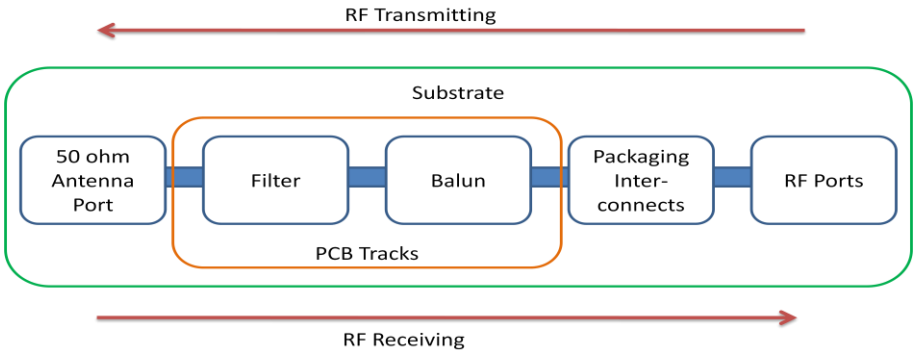

Fig. 1. System schematic of WSN RF circuit

Antenna Port: Assume 50ohm antenna was adopted. (Same procedure could be applied to other impedance's antenna.) It was straightforward to model the antenna port as a 50 ohm Microwave port, to which the radio signal will be applied.

Filter: Due to the space limitation of WSN nodes, three-element filters, which can have a 'T' or 'π' topology, would usually be a good solution. The components can be chosen symmetric or not, depending on the required frequency characteristics. The high-pass T filter in the Fig. 2 has low impedance at high frequencies, and high impedance at low frequencies. That means that it can be inserted in a transmission line, resulting in the high frequencies being passed and low frequencies being reflected. Likewise, for a low-pass π filter, the circuit can transmit low frequencies and reflect high frequencies. WSN nodes, which normally work on several hundred MHz or even GHz, should be connected with a high-pass T filter as illustrated in Fig. 2.

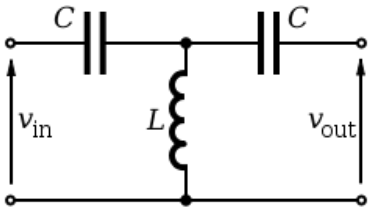

Fig. 2. High-pass T filter

Matching problem rises with the use of the unbalanced T filter to the balanced radio chip pins. Thus a balun is developed to solve this problem.

Balun: A balun circuit is designed to convert between balanced and unbalanced electrical signals. Baluns are designed to have a precise 180-degree phase shift, with minimum loss and equal balanced impedances. An L-C balun showed in Fig. 3 was designed for this purpose.

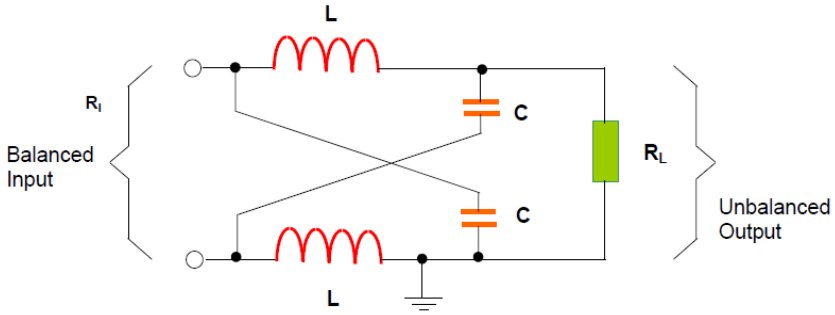

Fig. 3. Schematic diagram of an L-C lumped balun

This design is essentially a bridge and is known as a 'lattice-type' balun. It consists of two capacitors and two inductors, which produce the ±90 degree phase shifts. The diagram below (Fig. 3) shows the circuit diagram of the Balun.

Non-ideal Passive Models: In the previous discussion, all the passive components in the filter or the balun were treated as ideal, which means no parasitic. To improve the model's accuracy, the non-ideal parasitic was used.

Take capacitor's model for example. Fig. 4 provides the parasitic model of capacitor.

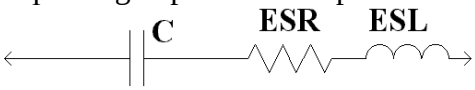

Fig. 4. Capacitor's non-ideal model

C is the primary capacitance, with the desired value. ESR is the equivalent series resistance. ESL is the equivalent series inductance. The ESR and ESL could be obtained from the manufacturer datasheet or Ansoft Designer vendor library, or by Ansoft Q3D simulation.

The non-ideal models of resistor and inductor could be generated similarly. The passives would behave frequency dependent due to the parasitic. These non-ideal passive models enabled a closer approximation of the measurement, especially for high frequency operation.

RF Ports: The input and output ports of RF chip for the frequency signals were no doubt active. The trick to model these ports as passives was measuring the impedance and generating an equivalent circuit for a specified frequency.

Fig. 5 shows the power amplifier (PA) lumped-element model in transmitting (left) and receiving (middle) modes and low noise amplifier (LNA) lumped-element model (right) [7]. The optimum PA port impedance values for the desired working frequency range were obtained by impedance measurements. The equivalent circuits for both models were calculated according to the impedance. The LNA input impedance could also be modeled.

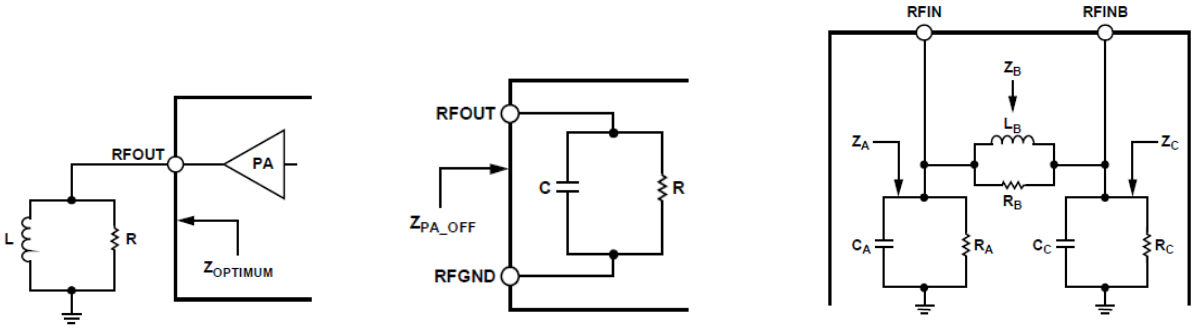

Fig. 5. PA lumped-element model in transmit mode (left), receive mode (middle) and Lumped-Element Model of LNA (right)

Packaging Interconnect: The packaging technologies of the RF chip were also considered. Two typical packaging technologies, wire-bonding and flip-chip, were modeled, with the interconnect parasitic extracted by Ansoft Q3D Extractor simulation [8].

The left of Fig. 6 shows the geometry of the wire-bonding interconnection inside the chip packaging. The structure "A" is the pad of the die, while "B" is the pad of the quad flat nonlead (QFN) package. The metal used for the wire-bonding was gold, with a height of 0.5mm and length of 2.4mm, which is the average length of all the wire-bonding.

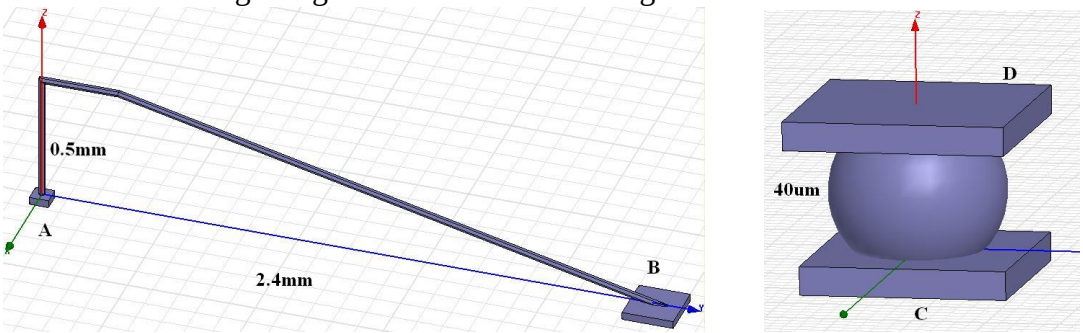

Fig. 6. The 3D structures of wire-bonding (left) and flip chip (right)

The right of Fig. 6 shows the geometry of the flip-chip interconnection. The solder ball, conducting the die and the board, was made of gold, with a height of 40 μm. The structure "D" was the pad of the die, while "C" the pad of the PCB board for flip chip. The equivalent circuit is presented by a sub-circuit in PSpice or Ansoft Designer.

Substrate: The substrate stack-up was modeled with the parameters of dielectric constant, thickness, loss tangent, copper metallization and grounding. These parameters took into effect because the PCB tracks on the substrate were performing as micro-stripe lines.

PCB Tracks: Not only the discrete components, but also the PCB tracks should be modeled as circuit components. All the PCB tracks were modeled as micro-stripe lines.

Simulation of Return Loss (S11)

S-parameter is a powerful way to describe an electrical network, compatible in describing large and complex networks. S-parameters change with frequency, load impedance, source impedance and network topology.

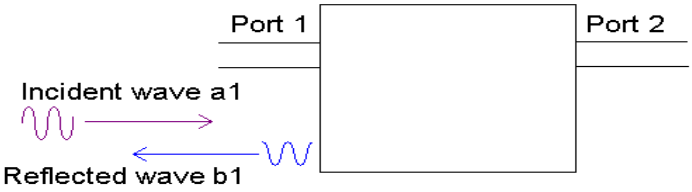

Fig. 7. Schematic illustrating return loss

Return loss, or S11, refers to the signal reflected at Port 1 for the signal incident at Port 1, as shown in Fig. 7. S11 describes the level of impedance matching at the observed port. Smaller S11 leads to better matching and thus more power efficiency. On the other side, large S11 indicates poor matching and low efficiency.

By putting all the parts, including the interconnect parasitic, the passive value and parasitic, the PCB substrate and tracks, LNA and PA lumped-element models, into the Ansoft Designer circuit, simulation results of return loss at the antenna connector could be obtained.

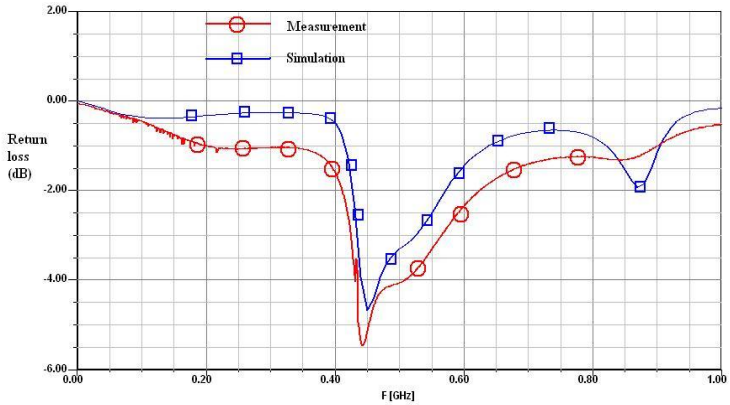

Fig. 8. A simulation and measurement example of return loss

An example of return loss by simulation and measurement of a WSN node is presented in Fig. 8. The working frequency was 433MHz and return loss could only reach as little as -4dB, which means very poor impedance matching. In this case, re-design of the circuit was required.

Methodology of RF Optimization by Simulation Parameter Sweep

Since there are lots of parameters potentially can affect return loss, it is not an easy task to tell which has the greatest impact. The standard deviation is a widely used measure of the variability or dispersion from the mean value.

Let X be a random variable with mean value μ:

$$\boldsymbol{E}[X] = \mu \quad (1)$$

Here the operator $\boldsymbol{E}$ denotes the average or expected value of X. Then the standard deviation of X is defined as:

$$\sigma = \sqrt{\boldsymbol{E}[X-\mu]^2} \quad (2)$$

The standard deviation is related to the mean value μ, which might be different for all parameters. To get rid of the impact of the mean value, the coefficient of variation (CV) could be used. In probability and statistics theories, the coefficient of variation is a normalized measure. It is defined as the ratio of the standard deviation to the mean:

$$C_V = \frac{\sigma}{\mu} \quad (3)$$

By sweeping the parameter with the largest coefficient of variation on return loss, the most significant parameter was targeted. Repeat this sweep procedure for all the relevant parameters, until a desired return loss was finally obtained [8].

Measurements Verification

Following the optimization procedure proposed, sweep of passive components' values was performed for an optimized return loss simulation result. Finally the new values of the passives were applied for PCB assembly.

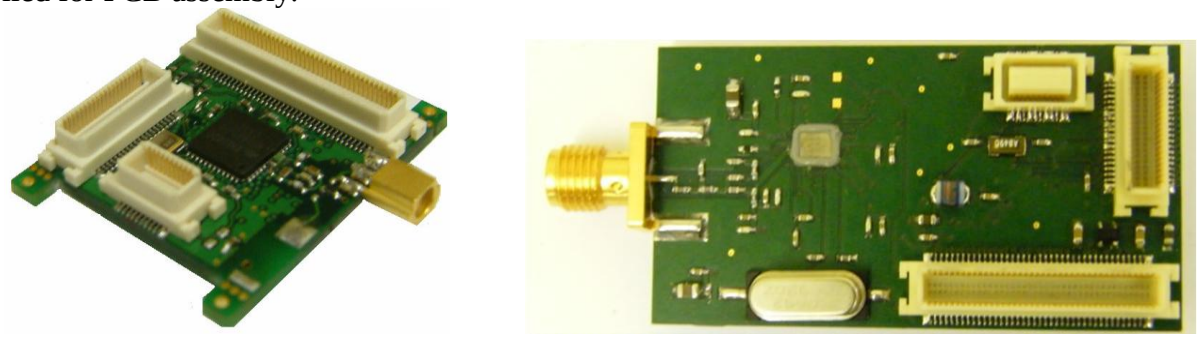

Fig. 9. Tyndall Zigbee mote (left) and ADF7020 flip chip mote (right)

Two WSN motes were optimized by the proposed methodology: left of Fig. 9 is the Tyndall Zigbee mote with QFN packaging [9], right of Fig. 9 is the Tyndall ADF7020 mote with flip chip packaging of the bare die [10]. The Zigbee mote was working at 2.4GHz, while the ADF7020 was at 433MHz.

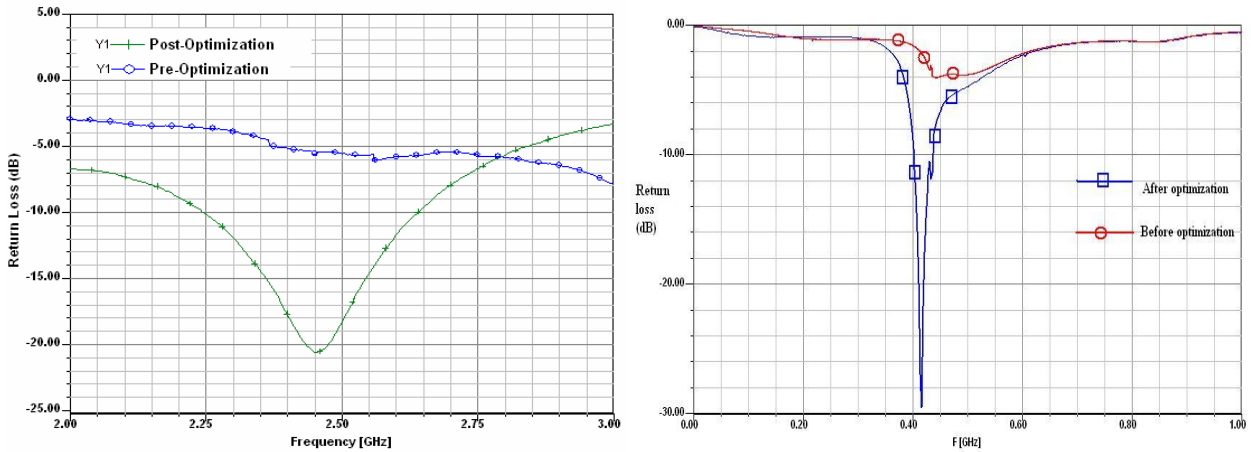

Fig. 10. Measurements of Zigbee mote (left) and ADF7020 mote (right)

Some measurements are given in Fig. 10: for the Zigbee mote, the return loss of the optimized board is significantly better than the un-optimized case, with a greater than 15dB improvement; for the ADF7020 mote, 20dB improvement of return loss is obtained by optimization. The measurements match the simulation and analysis well. The proposed methodology brought great improvement of return loss without any additional cost.

Summary

This paper presented a methodology to model variety of circuit components into passive network and to optimize the passive network's return loss to achieve large improvement in RF performance. The modeling of the RF circuit involved packaging interconnects parasitic extraction, PCB layout and substrate stack-up build-up and equivalent passive circuit construction. Measurements, compared by pre- and post- optimization, not only fit the simulation, but also showed a major improvement of the return loss of more than 15dB for two WSN nodes.

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