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AsH_3 gas-phase *ex situ* doping 3D silicon structures

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Dopant incorporation in Si can be done *in situ* during epitaxial growth, or *ex situ* for localised material modification from a variety of sources including ion, solid, liquid, or gas. Gas-phase doping has the advantage that it does not require a thin film deposition, it is more effective at entering tight spaces than a liquid, and it is less damaging and more conformal than a beam-line ion implant. In this work, we apply arsine (AsH_3) gas at approximately atmospheric pressures in order to n-type dope three-dimensional (3D) Si device structures. It was observed that the gas-phase doping can be either corrosive or gentle to thin-body Si depending on the process conditions. Initial doping processes caused damage to the Si due to etching, but after process optimisation, the structural integrity of the Si nanostructures could be maintained successfully. Moreover, it was noted that evaluating doping processes entirely on planar Si surfaces can be misleading: processes which appear promising initially may not be transferrable to non-planar thin-body structures like fins or nanowires, due to unwanted Si etching. Overall, we found that gas-phase doping with AsH_3 could provide $>10^{20}\,cm^{-3}$ electrically active As concentrations. This high As incorporation makes gas-phase doping very attractive for future gate-all-around devices, where the space between features will decline with continued transistor scaling. *Published by AIP Publishing.*
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I. INTRODUCTION

Impurity doping Si from a gas source is a promising alternative process method to the more standard techniques such as ion implantation, plasma-assisted doping, solid-source based in-diffusion, or liquid-source monolayer based in-diffusion. The motivation behind considering gas-source impurity doping processes stems from the architecture and design of current and future field-effect transistors (FETs), which are based on 3D Si features with decreasing dimensions.[1] Furthermore, and even more significantly, the spacing between the 3D Si structures is falling rapidly with each passing technology node and will continue to do so for the foreseeable future.[2] It is unknown at present whether many modern semiconductor processes can transfer to tight-pitch features where spaces and gaps are sub-10 nm. For example, any process that relies on conformal deposition of a film will be more challenging if the gap between features approaches twice the required film thickness. Likewise, liquid-based processes will struggle to deal with densely packed features due to limitations of wetting. The problems of ion implantation into thin-body structures are well documented[3] and will not diminish with scaled inter-nanowire gaps.

Gas-phase doping does not require a thin film deposition, is more effective at entering tight spaces than a liquid, and is less damaging and more conformal than a beam-line ion implant. Reports of gas-based doping of Si have been available for decades for common dopants but unfortunately this body of work is limited to planar substrates, which makes it impossible to evaluate their suitability for nanowire devices, where the physics may be fundamentally different due to the vastly different surface-to-volume ratios involved. With 3D structures, dopant diffusion depends on local surface orientations,[4] but more importantly in the context of in-diffusion-based doping, the physics of incorporation and dopant interaction with the surface becomes significantly more important with scaling. This means in essence that the surface barrier dominates, in terms of whether a dopant atom gets trapped or will incorporate into the semiconductor crystal. The problem of getting the dopant in becomes surface limited, unlike with ion implantation where one can project the dopant beyond the surface, so the surface is less influential.

Ransom *et al.* used arsine or tertiarybutylarsine in a helium carrier gas to gas-phase dope Si substrates with As,[5] observing higher As incorporation with a higher rapid-thermal-anneal (RTA) temperature and a higher As precursor concentration. The peak As concentration extracted by Secondary Ion Mass Spectrometry (SIMS) analysis was $>10^{20}\,cm^{-3}$. Song *et al.* also used arsine in their experiments but in a H_2 carrier gas.[6] They also achieved approximately $10^{20}\,cm^{-3}$ As concentrations using a 25 sccm AsH_3 flow rate injected into a

gas-source molecular beam epitaxy chamber at 500 °C. A drive in RTA at 1000–1075 °C was used in conjunction with a capping oxide for encapsulation.

In general, P incorporation from phosphine has produced lower dopant concentrations than As. Kalkofen *et al.* used phosphine in a two-step process involving surface adsorption followed by a drive-in RTA at 900–950 °C.[7] They commented that after discounting the surface peak, which is susceptible to SIMS artefacts, the impurity concentration was in the range of 10^{19} cm^{-3}. Kiyota *et al.* also used phosphine as their dopant source,[8,9] in H_2 carrier gas, similarly achieving a maximum P incorporation on the order of 10^{19} cm^{-3}. They did, however, show that higher phosphine flow rates produced more P incorporation. Zagozdzon-Wosik *et al.* showed very high P concentrations of $>10^{20}$ cm^{-3} by SIMS analysis when they used a solid source proximity doping technique,[10] whereby dopant atoms were evaporated from a donor wafer and diffused into a target wafer held in close proximity. Very recently Taheri *et al.* doped Si by gas-phase monolayer doping (MLD) using a diethyl 1-propylphosphonate precursor.[11] SIMS analysis was not available, but sheet resistance measurements demonstrated the success of the concept. There have been an equivalent number of p-type dopant studies using B_2H_6 as the dopant source, with some very high B incorporation reported.[12,13] Astrov *et al.* have reported in-diffusion into Si from gas-sources for the less-common dopants S and Se.[14,15] Finally, gas-phase n-type doping of Ge has been successfully demonstrated using tertiary-butyl-arsine, arsine, and phosphine in recent years.[16,17]

In summary, we chose to work with AsH_3 as a source of the common n-type dopant As as it was seen in the literature to produce higher n-type doping incorporation than phosphine. We apply several AsH_3 gas-phase doping processes to 3D Si structures with diameters ranging from 10 to 300 nm.

II. EXPERIMENTAL

This section is a summary of the nanowire test structure design and fabrication process. Extended details can be found in a recent publication.[18] A schematic representation of the process flow and variables considered in this work is shown in Fig. 1.

The nanowire devices under study to characterise the doping processes consist of multi-parallel nanowires that form a resistor structure. This is a simple two pad test structure where current versus voltage characteristics are measured to extract resistance. The nanowire width (W), length (L), and spacing (S) are all varied on the mask layout design. The metal contact pads consist of a 10 nm Ti adhesion layer with a thicker 150 nm Au layer on top.

Process step	Comment
Planar Si or nanowires patterned from SOI	
AsH_3 processing	AsH_3 flow rate (variable: 10, 50, or 250 sccm) Peak temperature : 850 °C Time at 850 °C (variable; 120, 300, or 900 s)
SiO_2 cap deposition (optional)	50 nm sputtered
RTA (optional)	1050 °C 5 s
SiO_2 cap removal (optional)	

FIG. 1. Summary of the AsH_3 process flow and variables considered in this work.

For the nanowire devices throughout this work, nominally undoped (100) SOI substrates were used, with a Si thickness of 66 nm and a buried SiO_2 thickness of 145 nm. The unpatterned substrates used for carrier profiling were standard (100) lowly doped p-type Si wafers. For nanowire processing, the SOI substrates were patterned using the Raith VOYAGER electron beam lithography (EBL) system with a beam energy of 50 keV, and the high resolution EBL resists hydrogen silsesquioxane (HSQ, XR1541, 2%) from Dow Corning. The samples were etched in an Oxford Instruments System 100 ICP etcher operating in Reactive Ion Etch (RIE) mode. The etch chemistry was a Cl_2/N_2 gas mixture at flows of 20 and 40 sccm, respectively, with a process pressure of 10 mTorr and an RF power of 80 W yielding a DC bias of 220 V. On all samples, prior to application of the AsH_3 process, samples were degreased, and native oxide was removed.

Gas-phase doping of all samples was carried out using a conventional metalorganic vapour phase epitaxy (MOVPE) rf-induction heated, horizontal reactor system, at a pressure of 700 Torr, with carrier gas Pd-diffuser purified hydrogen at a flow rate of 16 SLM. Highest purity commercially available AsH_3 gas was used as the dopant source. Samples were heated in the reactor from 20 °C to 850 °C for 800 s on a graphite susceptor under hydrogen. After 260 s, the sample reached a temperature of 600 °C at which point AsH_3 dopant gas was switched into the reactor at a controlled flow rate (10 sccm, 50 sccm or 250 sccm depending on process). Sample heating continued under these conditions up to the process temperature of 850 °C. The sample was then held at the process temperature for 120 s (10 sccm process), 300 s (50 sccm process), or 900 s (250 sccm process) before heating was switched off and the sample was allowed to cool. After 300 s, the sample reached a temperature of 600 °C at which point AsH_3 dopant gas was switched out of the reactor and the sample was allowed to cool to room temperature under hydrogen.

In some cases, samples were characterised immediately without further processing. Selected samples received a 50 nm sputtered SiO_2 capping layer, deposited prior to rapid-thermal-anneal (RTA) to prevent volatilisation of the dopant. Samples were then treated with a 1050 °C 5 s RTA in N_2. Afterwards, for capping layer removal, typically for 50 nm SiO_2 that had been annealed at 1050 °C, a 25:1 BOE solution was applied for 2 min. A UV lithography based process was used to pattern the Ti:Au (10:150 nm) metal contact pads, based on a lift off technique.

Electrochemical Capacitance Voltage (ECV) profiling was performed to determine the electrically active carrier concentration using dilute ammonium bifluoride as the electrolyte. Top-down scanning electron microscopy (SEM) was performed on an FEI 650 FEG SEM. Cross-sectional Transmission Electron Microscopy (XTEM) was carried out using the JEOL 2100 HRTEM operated at 200 kV. Cross-section samples were prepared by focused ion beam etching using a FEI's Dual Beam Helios Nanolab system. For current

versus voltage measurements, the KEITHLEY 37100 and KEITHLEY 2602 were used.

III. RESULTS AND DISCUSSION

A. Dopant chemical and carrier profiling

Figure 2 shows representative chemical and carrier profiles extracted after the 250 sccm AsH_3 process was applied to planar Si substrates. No post-RTA was applied to this sample set. Overall, this doping profile looks encouraging as the electrically active concentration is $>10^{20}\,cm^{-3}$, there is a steep tail and box-like shape to the profile, and the 30 nm of diffusion is relatively little and could be further optimised with a tailored thermal budget. The large difference in total and electrically active As in the 10 nm closest to the surface is likely to be as a result of electrically inactive immobile clustered As in this region.[19,20]

However, when this process flow was applied to nanowire devices fabricated from SOI substrates, it was seen in optical and scanning electron microscopes that the Si features had been severely attacked and in most cases had been entirely etched away. These data will be presented in Sec. III B. For this reason, we reduced the aggressive nature of the AsH_3 process in the next round of experiments by reducing both the AsH_3 flow rate and exposure time at process temperature. All other variables remained constant.

Figure 3 shows representative chemical and carrier profiles extracted after the 50 sccm AsH_3 process was applied to planar Si substrates. The blue curves show the SIMS and ECV profiles directly after the gas doping process, without a post-RTA. The As is confined to the top 10 nm of the Si substrate according to the SIMS profiling, and the ECV profile appears to show little As activation. However, this may be caused by the difficulty for ECV analysis in generating an active carrier profile for such a shallow junction. ECV is based on a CV measurement and must deplete the doped region of interest in order to calculate the active doping concentration. If the region is very shallow (e.g., 10 nm), it tends to fully deplete which makes the data extraction difficult.

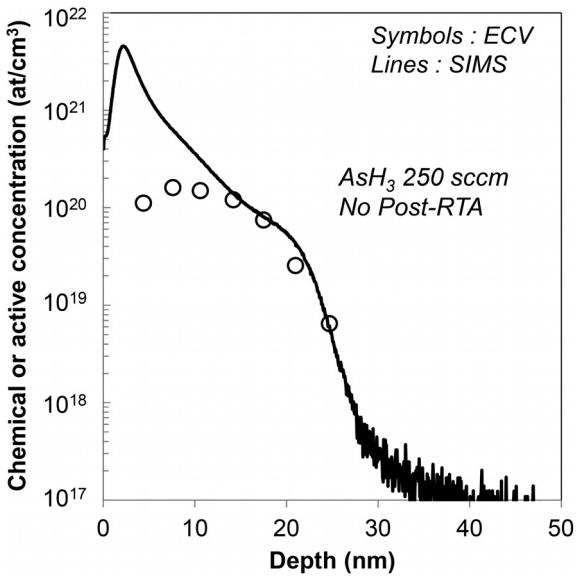

FIG. 2. Chemical and carrier concentration profiles versus depth into the Si determined by SIMS and ECV analysis, respectively, on bulk Si with a 250 sccm AsH_3 gas flow.

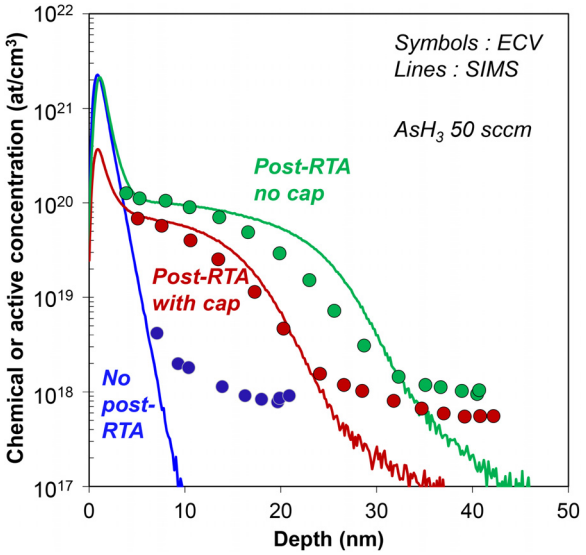

FIG. 3. Chemical and carrier concentration profiles versus depth into the Si determined by SIMS and ECV analysis, respectively, on bulk Si with a 50 sccm AsH_3 gas flow. Here, the application of a post-doping RTA at 1050 °C for 5 s has driven in As from near the surface. The best result was achieved doing this RTA without a capping oxide.

After the 1050 °C 5 s RTA, a significant amount of As has in-diffused from the near-surface region, as seen in the red and green curves in Fig. 3. The SIMS and ECV profiles match quite well for the most part, indicating that almost all incorporated As is electrically active and shows maximum As concentrations on the order of $10^{20}\,cm^{-3}$. This is a positive result for an in-diffusion based process. The difference in the SIMS versus ECV in the top 5 nm is related to electrically inactive As resident in the native oxide and immobile As clusters close to the surface. Furthermore, the differences in the tails of the profiles reflect the differences in noise levels of the two techniques. SIMS has a superior lower noise level, or better dynamic range in this case (P profiling in Si), while in this case the ECV detection limit is approximately $10^{18}\,cm^{-3}$. Finally, we have not applied any specific alignment to affect the depth scales. The good agreement on the depth scale for the 2 data sets was achieved without any post-processing of the data.

It was noticed that more As in-diffused in the case where no SiO_2 cap was present during the RTA. This is related to the segregation coefficient of As in the Si/SiO_2 system, where the As diffuses either preferentially into Si or preferentially into SiO_2. Evidentially, in this situation with a super-saturation of As at the surface, i.e., in the first monolayers, the SiO_2 cap causes the As to move away from the Si substrate.

Figure 4 shows carrier concentration profiles versus depth into the Si determined by ECV analysis, on bulk Si with a 10 sccm AsH_3 gas flow. This sample received a 1050 °C RTA to drive in the As. Three separate ECV measurements were done on the same sample, differentiated by different symbols, to demonstrate the reproducibility of the measurement technique. As in-diffusion is lower than that for 50 sccm and

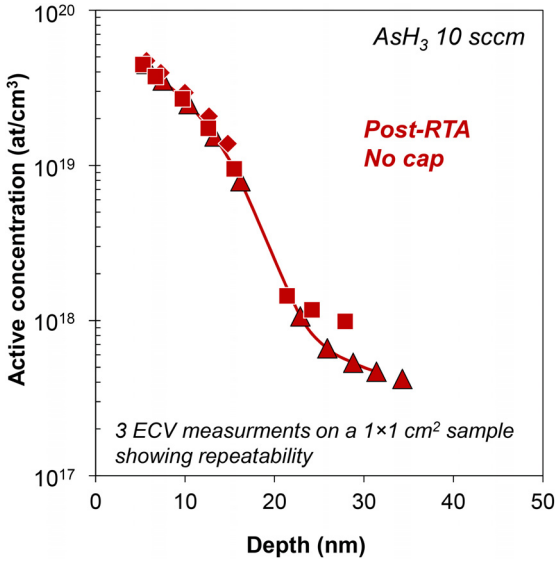

FIG. 4. Carrier concentration profiles versus depth into the Si determined by ECV analysis, on bulk Si with a 10 sccm AsH_3 gas flow. This carrier profile was after a 1050 °C RTA to drive in the As. Three separate ECV measurements were done on the same sample, differentiated by different symbols, to demonstrate the reproducibility of the measurement technique.

250 sccm processes which is expected due to the lower As concentration gradients present at the sample-gas interface. The maximum electrically active concentration is in the range of $6 \times 10^{19}\,cm^{-3}$, and the carrier profile is mostly confined to the top 25 nm of the Si.

B. Optical, SEM, and TEM inspection of 3D structures

By decreasing the AsH_3 gas flow rate and exposure time at the process temperature, the gas doping process was made less aggressive and the attack of the Si was reduced as a result. Nanowire devices survived and were imaged by SEM and TEM. Figure 5 shows the representative SEM images of the Si nanowire devices, fabricated from SOI substrates, after the AsH_3 processing with the flow rates of 250, 50, and 10 sccm, respectively. In Fig. 5(a) after the 250 sccm AsH_3 process, the Si has been etched away completely. The dark region in the image is the buried oxide of the SOI wafer, and the bright regions are the Ti/Au metal contact pads. In Fig. 5(b), the Si nanowires are clearly present after the 50 sccm AsH_3 process, as 4 nanowires can be seen, connecting larger Si regions on either side. However, it is also evident that two of the nanowires are damaged in Fig. 5(b). Several test structures were imaged in this way, and this type of visible damage was common, and seemingly randomly distributed throughout in terms of frequency and location. Finally in Fig. 5(c), the 10 sccm process was demonstrated to be the gentlest approach as there was no evidence in the SEM of structural damage to the Si regions or nanowires in this case.

Figure 6 shows a representative cross-sectional TEM image of a typical isolated Si nanowire directly after doping by the 50 sccm AsH_3 process. The sidewalls have been attacked and roughened by the process, apparently etched along specific crystal facets, which is undesirable. However, the inside of the nanowire is free of visible crystal defects, in contrast to what one would expect to observe after ion

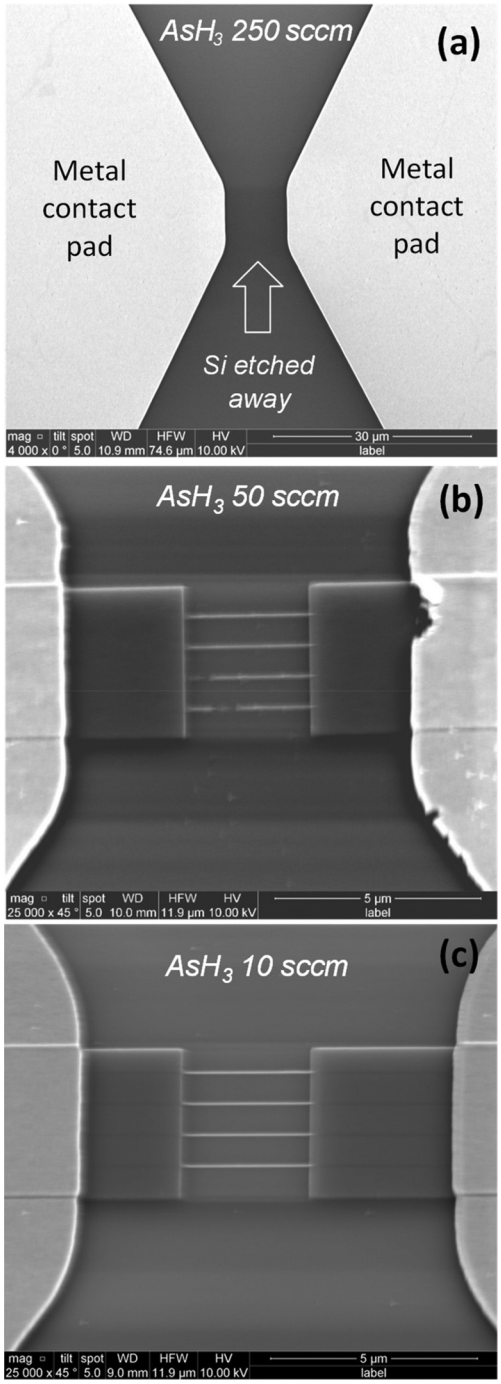

FIG. 5. Representative SEM images of Si nanowires directly after doping using a 250, 50, or 10 sccm AsH_3 gas flow, and contact metal pad patterning. Lowering the AsH_3 gas flow lowers the Si etching. For the 10 sccm process, the nanowires are not attacked, and even the long and narrow nanowires survive.

implantation of a thin-body Si structure.[21] This device conducted current and did not feature a broken nanowire which would lead to an open circuit. The inset of Fig. 6 shows a representative XTEM post-patterning and before doping. This is not the exact test structure as in the main part of Fig. 6, but is included to show the sidewall smoothness prior to doping.

Figure 7 shows a representative cross-sectional TEM image of four densely packed Si nanowires directly after doping by the 10 sccm AsH_3 process. Here, we show the

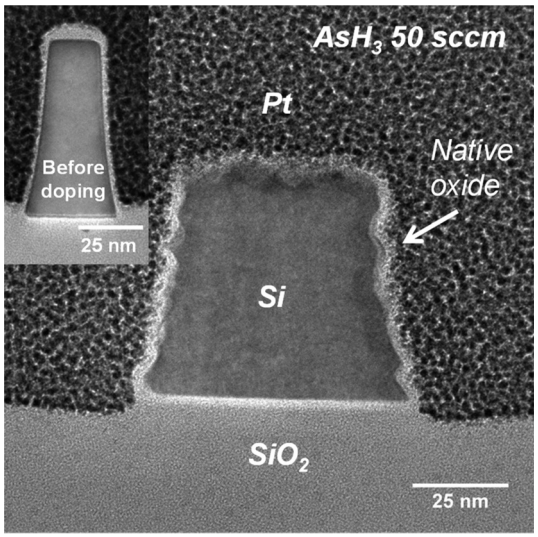

FIG. 6. Representative cross-sectional TEM image of a Si nanowire directly after doping using a 50 sccm AsH_3 gas flow. The sidewalls have been attacked and roughened by the process; however, the inside of the nanowire is free of visible crystal defects. The inset shows a representative XTEM post-patterning and before doping showing smooth sidewalls.

tightest pitch structure on the layout as there were a number of interesting observations. The nanowires are crystalline and are once again free of visible crystal defects such as {111} stacking faults or twin boundaries. The sidewalls appear smoother than in Fig. 6, which correlates with the SEM images shown in Fig. 5. There is approximately 1 nm of native oxide around the outside of the Si features, which we commonly see after these devices are exposed to ambient air for any period of time. Finally, it is interesting to note that the AsH_3 process had etched the oxide regions between the Si, in the trenches between the nanowires. This was not observed in XTEM of similar test structures that were doped by processes other than gas-phase doping and could be linked to the reaction of SiO_2 with atomic H from cracked AsH_3.[22]

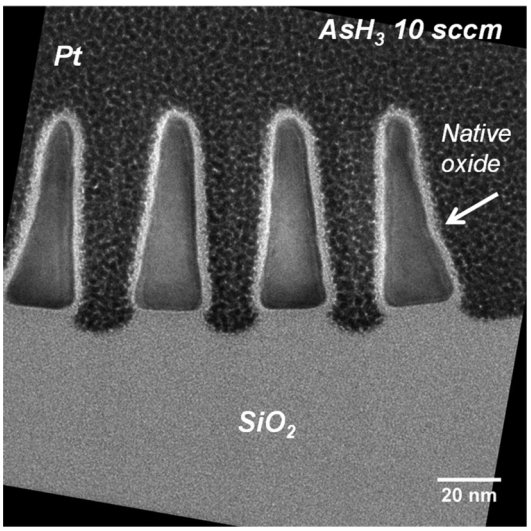

FIG. 7. Representative cross-sectional TEM image of Si nanowires directly after doping using a 10 sccm AsH_3 gas flow. The sidewalls appear smoother than in Fig. 6. The nanowire pitch is 40 nm.

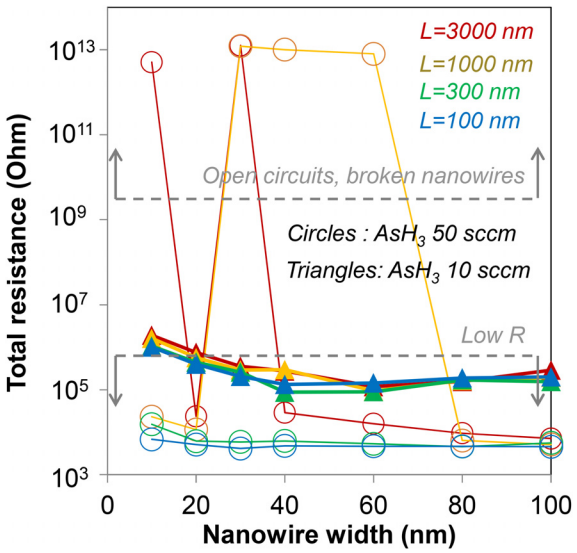

FIG. 8. Total resistance in the AsH_3 gas doped four finger nanowire test structure, 66 nm tall, as a function of W, with S fixed at 1000 nm. Despite a number of device failures where the high R values indicate open circuits or broken nanowires, several devices yield a low R value indicating high As activation levels.

C. Electrical characterisation

Figures 8 and 9 show the electrical data from the Si nanowire devices in this work. Figure 8 shows a representative set of data that contains the main conclusions. Figure 9 shows all the data collected.

Figure 8 shows the total resistance (R_{total}) versus W, for different L, comparing the 50 sccm process versus the 10 sccm process. The 10 sccm process has better device yield as the 50 sccm process had several device failures, characterised by extremely high R_{total}. Those are essentially open circuits, corresponding to broken nanowires. On the other hand, the 50 sccm process can reduce R_{total} to the lowest values seen in this work, namely, in a 10^3–10^4 Ohm range. It was noticed in general that device failures occurred in long

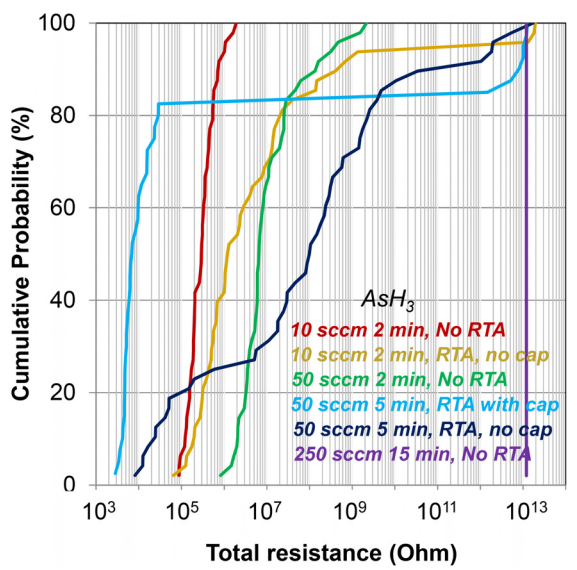

FIG. 9. Cumulative probability, in terms of percentage, of total nanowire resistance in AsH_3 doped nanowire devices.

and narrow nanowire devices, which is expected, as these are more fragile than the short large-diameter counterparts. Thus, it can be concluded that the dimension and shape of the 3D Si structure of interest could determine which process is best suited for it. In other words, the long narrow structures are fragile, so they need an extremely gentle process; here the 10 sccm AsH_3 process would be appropriate. For the short large-diameter structures, which are more robust and can withstand more corrosive processes, the 50 sccm AsH_3 process would be a better choice for lower electrical resistance.

Figure 9 shows the cumulative probability of all the R_{total} values collected in this work for six process variations, including the different AsH_3 flow rates and process times, the use of a post RTA or not, and the use of an SiO_2 cap during the RTA or not. To clarify, the first processes were AsH_3 10 sccm 120 s, 50 sccm 300 s, and 250 sccm 900 s. The data presented up to and including Fig. 8 refer to these conditions. In Fig. 9, we also have variations with time.

For the 250 sccm process, the analysis was straightforward, as there was 100% device failure. As already seen in Fig. 8, the 50 sccm process could reduce R_{total} to the lowest levels, at the cost of some device loss. The 10 sccm process had the fewest device failures, but the best median R_{total} value is 2 orders of magnitude higher than the best median R_{total} of the 50 sccm process. The 10 sccm 2 min no RTA process (red curve) shows a very tight distribution with almost 100% device yield. The non-zero device loss in the case of the 10 sccm processes is attributed to low level etching during the doping process, and some device loss due to the reactive-ion-etch and metal contact formation processes unrelated to the doping step. Two of the 50 sccm processes (blue curves) show some excellent low R_{total} values ($<10^5$ Ohm) but the yield has been compromised to a degree. The 50 sccm 5 min with RTA with a cap (light blue curve) shows approximately 82% of the devices with $R_{total} < 10^5$ Ohm.

The use of RTA, with or without the cap, produced more in-diffused doping profiles in the SIMS and ECV analysis, while in the electrical data there was a benefit to R_{total} but also made the yield worse. The use of a cap or not deserves closer evaluation in future work. Finally, it should be noted that the process time will be a factor in the dopant incorporation, but is a secondary factor compared to the variations of AsH_3 flow rate explored in our work to date. Like with ion implantation, time will affect the dose (linearly), so it must have an effect to some degree.

Following the parameter extraction routine described in Ref. 18, nanowire resistance and Si resistivity were then extracted, by first extracting and subtracting out contact resistance, according to the equation

$$R_{TOTAL} = 2R_{CONTACT} + \rho\frac{L}{t.W}. \quad (1)$$

Resistivity (ρ) is selected as the benchmark parameter to compare different doping processes with each other, which is extracted using

$$R_{NANOWIRE} = \rho\frac{L}{t.W}. \quad (2)$$

This was not possible for all processes here because of the poor yield for many devices in this work. A large sample set of working devices is needed to reliably extract contact resistance. This was possible for processes where the yield was acceptable, namely, the red curve in Fig. 9 (10 sccm 2 min no RTA) and the light blue curve in Fig. 9 (50 sccm 5 min, RTA with a cap) discounting the broken nanowires (open circuits). For the other processes, we are not confident of the extraction routine, i.e., too many non-working devices.

Figure 10 shows ρ versus nanowire width and nanowire spacing for the two AsH_3 processes mentioned above, as well as the P room-temperature ion implant and allyldiphenylphosphine (ADP) P monolayer doping (MLD) with an

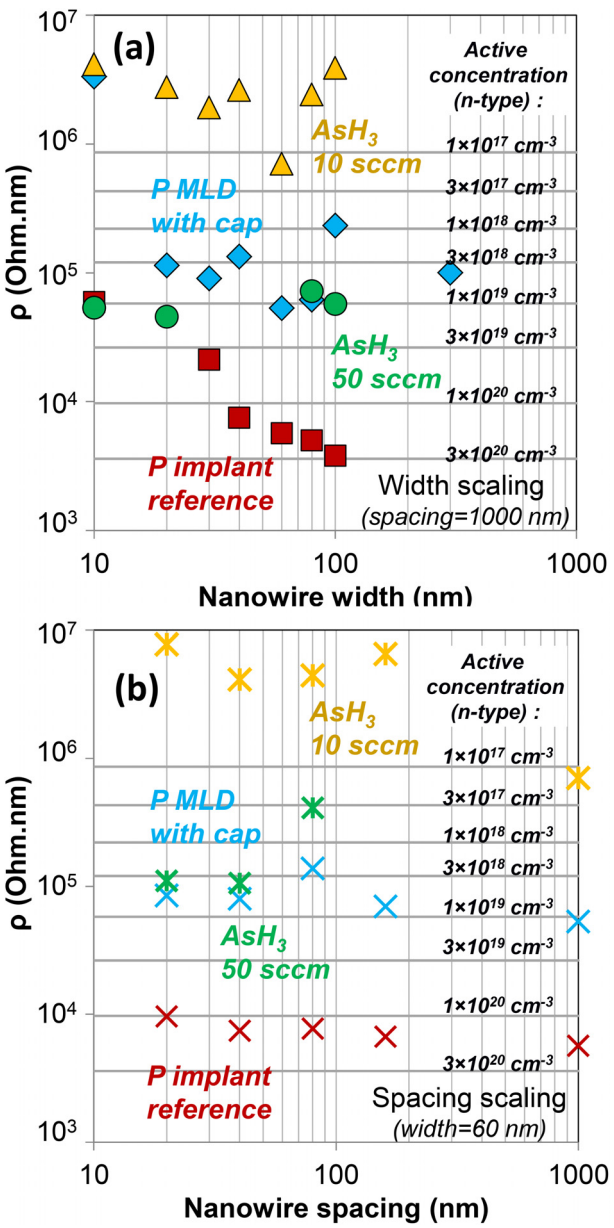

FIG. 10. (a) Resistivity (ρ) in four finger nanowire test structures doped by AsH_3 10 sccm 2 min with no RTA (yellow), AsH_3 50 sccm 5 min with a post-RTA with a cap (green), benchmarked with data from Ref. 18, namely, ADP P MLD (blue) and ion implanted P (red), as a function of W with S fixed, and (b) as a function of S with W fixed. The horizontal lines represent active concentration isolines associated with ρ, as calculated using Si mobility values assuming a uniformly doped nanowire, as described in Ref. 18.

SiO_2 cap from Ref. 18. These data support the conclusions that the higher AsH_3 flow rate yields better dopant incorporation, and that scaling the width has a relatively small impact on the ρ. This is consistent with the TEM that showed the core of the nanowire does not contain crystal damage, unlike the room-temperature ion implantation case where the defectivity (and hence ρ) versus W trend will be quite strong. The lower AsH_3 flow rates result in worse values of ρ, as expected. Benchmarking against other dopant techniques shows that the gas doping has potential in 3D structures at small W despite the surface attack during doping, under certain conditions, but the gas-based processes still require a certain amount of optimisation to challenge ion implantation.

D. Using AsH_3, the balance between doping and etching

The most significant variable in this work, in terms of dopant incorporation or Si etching, was the AsH_3 supply. Higher flow rates lead to greater As incorporation as expected, but also greater etching. Having the first one without the second is clearly the desired situation.

With greater As supply, there will be more in-diffusion. First, the As dose is increased by the AsH_3 flow rate, and also the diffusivity is enhanced. Arsenic exhibits significant dopant-enhanced diffusivity in Si. Nylandsted Larsen *et al.*[23] showed a 2 orders of magnitude increase in As diffusivity in going from donor concentrations of $10^{19}\,cm^{-3}$ to $3\times10^{20}\,cm^{-3}$. Thus, the greater concentration of As present will cause more diffusion. This explains why the 250 sccm process produced a 30 nm deep As profile directly after the AsH_3 processing at 850 °C, without the need for a 1050 °C RTA, while the other processes only showed junction depths of 30–40 nm after a 1050 °C 5 s RTA. Moreover, comparing Figs. 3 and 4, the diffusivity during RTA drops with AsH_3 supply.

In terms of the Si etch rate, this is also correlated with the AsH_3 supply, as this was the primary process variable. It is expected during processing that the AsH_3 disassociates into As + 3H, and it is this atomic H that combines with Si to form the volatile SiH_4 which evaporates as a gas. There have been numerous literature reports of Si etching in combination with atomic H.[24–26] It is not surprising that the higher AsH_3 supply produced greater Si etching although it has been reported that this etch rate is inversely proportional to temperature.[27] Furthermore, Miyagi *et al.* showed that there can be preferential etching of Si, in the presence of elemental H, according to the crystal facets such as (001) and (111).[28] The authors of that work commented that (111) facets terminated with H were more stable and thus etched less. In Fig. 6, we observed preferential etching along crystal facets, which is consistent with that work. Future gas-phase doping work should use gas sources with a lower active H content.

Further, future work in this area should include 2D and 3D profiling of the carriers and impurity doping, by techniques such as scanning spreading resistance microscopy and atomprobe tomography. This is important in order to determine the potential uniformity and conformality from gas-phase doping in 3D structures.

IV. CONCLUSIONS

Overall, in this work, we have demonstrated gas-phase doping to be a very attractive alternative doping methodology for future gate-all-around devices, with high active concentrations attainable with reasonably controlled diffusion lengths. We observed a trade-off between As activation and incorporation versus etching in 3D Si structures exposed to AsH_3. The AsH_3 flow rate had the greatest influence on the results. The 10 sccm process was the gentlest approach with almost 100% device yield but $<10^{20}\,cm^{-3}$ electrically active As concentration was achieved, making this more suited to long fragile nanowires with small diameters. The 50 sccm process showed promise with a $>10^{20}\,cm^{-3}$ active As concentration but there was some device loss, making this more suited to short large-diameter nanowires. Finally, the 250 sccm experiment looked ideal on planar Si, but entirely etched away the Si nanowires resulting in a 0% device yield. A post-process RTA and capping did not provide the same effect as in monolayer doping where they appear to be vital; here they provide some positive impact on the electrical performance while also leading to some device loss.

In conclusion, gas-phase doping processes provide a viable alternative to ion, liquid, or solid source doping approaches for 3D Si device structures.

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