Physics-based TCAD analysis of Border and Interface traps in Al_2O_3/InGaAs stacks using Multifrequency CV-curves

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Abstract- In this paper, we analyze the multi-frequency C-V curves of $In_{0.53}Ga_{0.47}As$ MOSCAPs by employing physics-based TCAD simulations including both border and interface traps. The calculations reproduce the experimental inversion and accumulation capacitance, and the general trend of the depletion capacitance. A study of the influence of the quantization model on the extraction of the trap distribution is also carried out.

1. Introduction

One of the major concerns for the implementation of high mobility III-V semiconductors as channel materials in CMOS technology, or for integration of RF and mm wave functions with silicon CMOS, is the large density of interface (IT) and border trap (BT) [1]. The reliable extraction of interface (D_{IT}) and border (D_{BT}) trap distribution is challenging and accurate simulation of multi-frequency C-V can be used to overcome this issue [2]. Analysis of BTs to date has been based on a distributed capacitor/resistor model [2,3]. In this work, we extend these studies simulating the AC response of BT and IT by employing a TCAD simulator [4] that solves the Poisson, drift-diffusion and charge conservation equations, taking into account the elastic band-to-trap tunneling model [5] for BTs.

An analysis of the model limitation and accuracy is carried out for a reliable extraction of D_{IT} and D_{BT}.

2. Device Fabrication and characterization

The n-type InGaAs MOSCAP fabrication starts with a n^+ InP (100) substrate. A 2 µm n-$In_{0.53}Ga_{0.47}As$ layer was grown by MOVPE using a nominal S doping concentration of $4 \cdot 10^{17}$ cm^{-3}. The Al_2O_3 dielectric with a thickness of 6 ± 0.3 nm (**Fig. 1**) was grown by ALD. Ni(70 nm)/Au(90 nm) was used as the metal gate and was formed by electron beam evaporation and a lift-off process. MOSCAPs were treated by post-metal FGA ($0.05H_2$,$0.95N_2$) at 450 °C. C-V characteristics have been measured between 1 kHz and 1 MHz using an E4980 LCR meter.

3. Results and Discussion

As the determination of the density and energy distribution of interface traps and border traps is based on the deviation of the experimental C-V response from the ideal case, it is instructive to first consider the multi-frequency C-V characteristics of the ideal InGaAs MOS structure (**Fig. 2**). For this value of T_{OX} it is important to include quantum effects [6] that can be taken into account using the modified local density approximation (MLDA) model. The corresponding experimental C-V response is shown in **Fig. 3**, where significant deviations from the ideal case are observed in accumulation due to BT, and in the transition to inversion due to IT and the possible contribution of BT aligned with the InGaAs valance band (VB). The oxide capacitance for the simulation is determined from the minimum capacitance in inversion (C_{min}) at high-frequency, under the assumption that traps do not affect it. The set of parameters founded are T_{OX}=6.3 nm and ε_{OX}=7, which are used in the rest of the work. The InGaAs minority carrier lifetime was calibrated to match the frequency position of the peaks in the G/ω and -ω·dC/dω curves [7] (**Fig. 4**). This calibration also captures the experimental inversion capacitance vs frequency (**Fig. 5**).

Using the D_{BT} shown in **Fig. 6**, the experimental capacitance can be reproduced fairly well (**Fig. 7**). It is worth noting that using the classical electrostatic model (w/o MLDA) a lower D_{BT} must be used to reproduce the experiments, underestimating the BT charge by ~32%. Moreover, since the classical model overestimates the capacitance (see Fig. 5), simulations cannot reproduce well the experimental data in the range $0.5<V_G<1$ V.

The IT model, however, is local and relies on the carrier concentration at the interface [4], thus the emission rates become unphysically small when the MLDA model is used. For this reason, in the subsequent figures, where we include IT, we show only results obtained w/o MLDA model.

Fig. 8 compares simulated and experimental capacitance in depletion and inversion including the D_{IT} and D_{BT} shown in **Fig. 9**. The general trend of the experimental curves can be reproduced by the simulations, but some parameters adjustments are still needed to achieve a better agreement.

4. Conclusion

In this paper, we used extensive TCAD simulations to analyze the effect of IT and BT on the C-V response for advanced InGaAs/Al_2O_3 MOSCAPs. The simulations yield the distribution of BT into the oxide and also highlight the importance of the physical models employed and their impact on the extraction of D_{BT} and D_{IT}.

References

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Acknowledgements: The research leading to these results has received funding from the European Commission FP7/2007-2013 under Grant Agreement III-V-MOS Project No. 619326 via the IUNET consortium and the H20202 INSIGHT project No 688784.

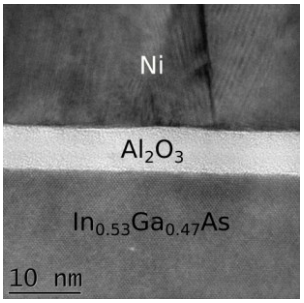


Fig.1: Cross-sectional TEM image shows an Al_2O_3 gate oxide thickness of 6 ± 0.3 nm.

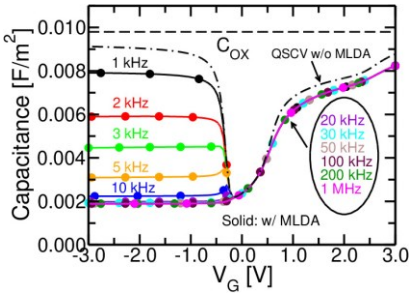


Fig.2: Simulated multifrequency C-V at 300K w/o including traps using the MLDA model (solid lines). The quasi-static C-V (QSCV) simulated w/o MLDA is reported with dash-dot line.

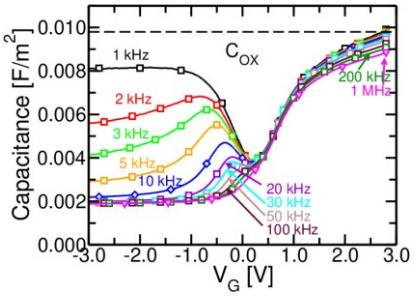


Fig.3: Experimental multifrequency C-V characteristics at 300 K. Negligible leakage current is observed during the measurements.

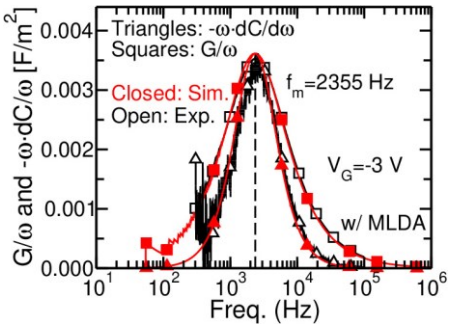


Fig.4: Experimental (open symbols) and simulated (closed symbols, w/o traps) curves of G/ω and -ω·dC/dω plotted vs. frequency (ω is the angular frequency). The transition frequency f_m is reproduced using a minority carrier generation life time of 92 ps

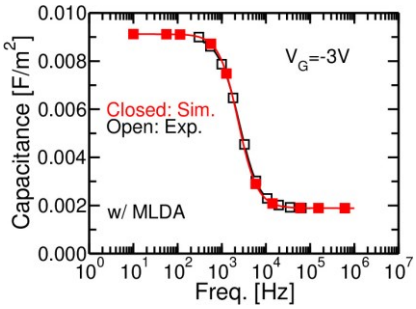


Fig.5: Experimental (open symbols) and simulated (closed symbols, w/o traps) inversion capacitance as a function of frequency.

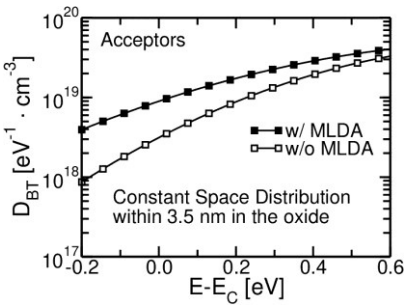


Fig.6: *Energy distribution of BT used in simulation w/ and w/o MLDA model to reproduce the experiments in Fig. 7. Space distribution is uniform within the first 3.5 nm of Al_2O_3. E_C is the InGaAs CB energy.*

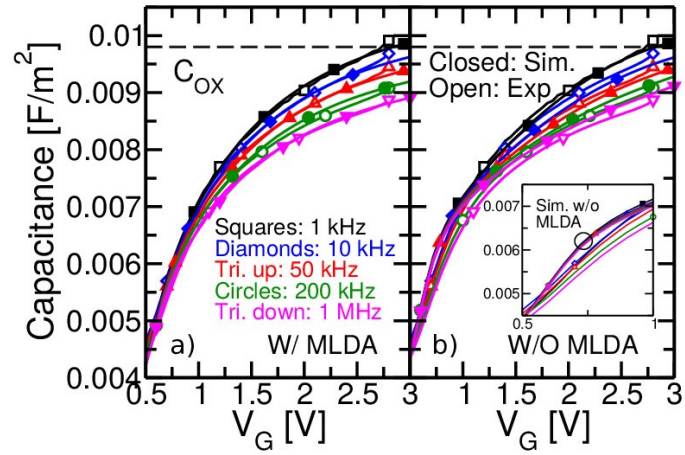


Fig.7: *CV characteristics measured (open symbols) and simulated (closed symbols) using the MLDA (a) or the classical electrostatic (b) model. Simulations include the border traps show in Fig. 6 with a trap volume Ω_T=1·10^{-24} cm^3. The inset zooms on plot b shows that the classical charge model overestimates the experimental capacitance.*

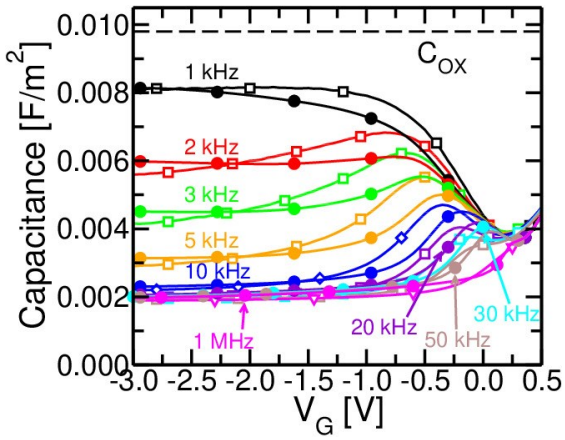
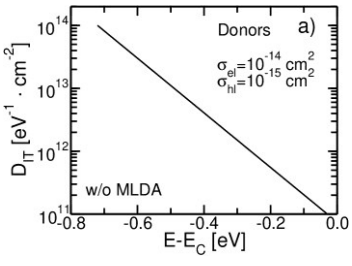


Fig.8: *CV characteristics measured (open symbols) and simulated (closed symbols) using the classic charge model. Simulations include the trap densities shown in Fig. 9 (note that BTs are distributed toward the lower bandgap and the valence band).*



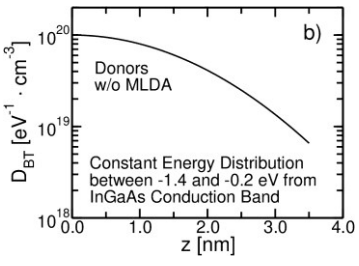


Fig.9: (a) *D_{IT} and (b) BT space distribution used in simulation w/o MLDA to reproduce the experimental capacitance in Fig. 8. The Energy distribution of BT is kept uniform in energy between -1.4 to -0.2 eV from the InGaAs conduction band. The capture cross section of IT for electron (σ_{el}) and holes (σ_{hl}) are set to 10^{-14} and 10^{-15} cm^2 respectively, while BTs have a trap volume Ω_T=1·10^{-24} cm^3. E_C is the InGaAs CB energy and z is the depth of BT in the Al_2O_3.*