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Physics-based modelling of MoS_2: the layered structure concept

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ABSTRACT

Recently, continuum-based Technology Computer Aided Design (TCAD) device models have been used to investigate the advantages and limitations of Transition Metal Dichalcogenides (TMDs), as one of the promising families of 2D-semicoductors. Nevertheless, a complete physics-based model is still missing. In this work, TCAD methodology is advanced for MoS_2 devices, as the material system is modelled considering a structure formed by layers of MoS_2 and Van-der Waals gaps, as opposed to a continuous semiconductor, The structure is benchmarked against previous experimental data and the behavior of thin and multilayer MoS_2 is studied. Then, the model is used to evaluate the electron distribution and current density in a MoS_2-based Field-Effect Transistor (FET). The analysis of the layered-structure provides additional understanding of the electrostatics and carrier transport in 2D semiconductors.

1. INTRODUCTION

2D-Semiconductors, and particularly TMDs, have been one of the most studied semiconductors to replace silicon in FETs applications. Their characteristics are attractive from an electron device perspective[1]. Due to their atomic structure, the channel thickness of FETs can be formed with a precision which is defined directly by the 2D atomic structure of the semiconductor. This allows an improved electrostatic control when compared to classic 3D semiconductors. In addition to electrostatic control, 2D semiconductors have the potential for reduced surface

roughness when compared to grown or etched 3D semiconductors. This is significant, as surface roughness limited mobility scales between t^6 and t^4, where t is the channel thickness[2,3]. Also, the surface is not typically characterized by unsaturated dangling bonds or dimers, as in other semiconductors, and therefore the interface traps could be lower in practice, as recently reported[4,5,6]. In addition, the wide range of bandgaps that they present, from semimetal to insulators, can be exploited in MOSFET and tunnel-FET applications.

The use of physics-based models can give a substantial improvement for the time and cost associated with the development of new materials and device architectures[7]. Recent publications have indeed shown how the use of a properly formulated TCAD model can help in the understanding of the physics of 2D-semiconductors[8,9,10,11,12] Nevertheless, a complete TCAD model accounting for the inherent 2D structure is still missing.

Previous publications investigating continuum-based modelling in MoS_2 have accounted for the 2-Dimensional structure based on highly asymmetric mobility in-plane and out-of-plane, while maintaining a homogenous structure[12]. In this work, instead of using a continuous slab of semiconductor, as previously reported, we introduce in a TCAD tool the "layered structure", which takes into account both in-plane drift and diffusion currents and a tunneling process through the Van-der-Waals gap (VdW-gap) between the layers of the 2D-semiconductor. This type of layered-modelling with a TCAD tool is still missing in the state of the art[13], even if the layered structure is a fundamental feature of TMDs or any other 2D-material and modelling might benefit from its introduction. For this study of transport in 2D-semiconductors we used the continuum-based Synopsys Sentaurus Device software[14].

The analysis is calibrated using previous experimental findings based on vertical transport through MoS_2. The results show that 2D-semiconductors can be modelled by a TCAD tool and the

layered structure can be particularly important when a few layers of material are considered, as the layered characteristics of the material have a greater impact with reducing 2D film thickness.

2. SIMULATION SETUP: THE LAYERED STRUCTURE

The electrical simulations are obtained solving the Poisson and drift diffusion equations using the Fermi-Dirac distribution. The carrier density and density of states for monolayer MoS_2[15], effective mass[16],[17] and carrier lifetime[18] are set considering previous experimental or theoretical studies.

Figure 1a shows a representative TEM image of 3-layers of MoS_2 taken in the channel region of a back-gated MoS_2 MOSFET, where it is possible to notice the characteristic layered structure of the semiconductor[8]. The structure is represented schematically in Figure 1b in order to emphasize the division between each MoS_2 layer. This same layered representation is used in the TCAD (Figure 1c) where the layers of semiconductors are alternated by VdW-gaps. The green stripes are the MoS_2 layers, while the light-blue layers are the VdW-gaps. The Van-der-Waals gaps are set between the layers of the MoS_2 only, and not between the MoS_2 and the oxide or the MoS_2 and the contact. These effects are outside the scope of this work which is the carrier transport in the MoS_2 layers. However, previous experimental reports pointed to a VdW gap of 0.3 nm (k=1) at the MoS_2-oxide interface[4].

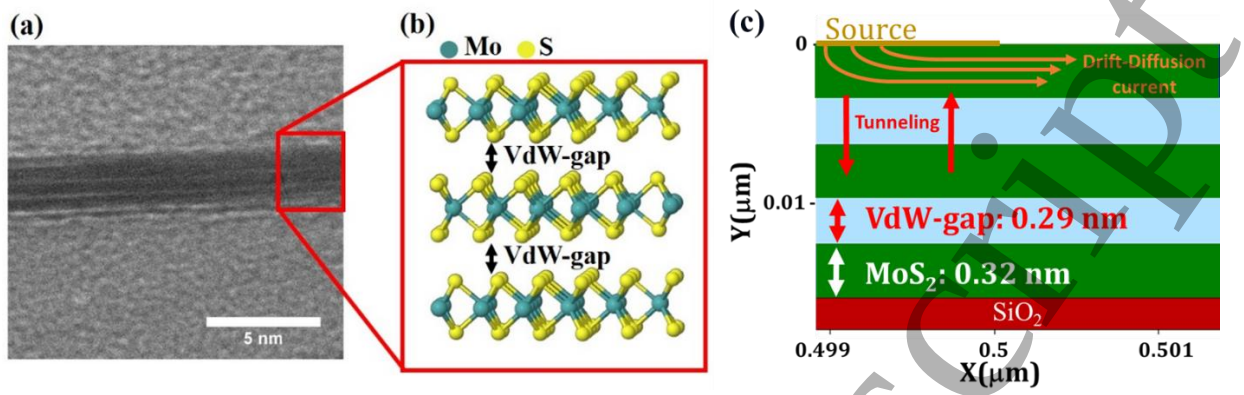

Figure 1: (a) Representative TEM image showing the layered structure of MoS_2. (b) Representation of the structure of MoS_2 showing the Van-der Waals gaps between the layers[19]. (c) Schematic of the layered structure implemented in the Sentaurus physics based device simulator.

The thickness of the MoS_2 and the gap layers in Figure 1c is set initially to 0.32 nm and 0.29 nm respectively, close to the values that are usually visible by TEM analysis or calculated by X-ray diffraction[20]. However, the effective electrical thicknesses might be different. Previous studies have shown that there exists an overlap of the wave functions and an exchange interaction between nearby MoS_2[21]. During the analysis the thickness of one layer of MoS_2 and one VdW-gap will be constant and equal to 0.61 nm, which is the known thickness of monolayer MoS_2. Nevertheless the effective electrical thickness of the two sub-components will change as it is a variable that needs to be benchmarked against experimental data.

In general there will be two kind of currents: (1) parallel current in the MoS_2 layers, which is modelled by the drift-diffusion equations, and (2) perpendicular transport in between layers due to direct tunneling through the gaps[22], which act as tunneling barriers.

Figure 2b shows the conduction band energy of 5 layers of MoS_2 considering a uniform (red) and a layered structure (black). For the layered structure, it is clear that, to have conduction from the top to the bottom of the device, tunneling through the VdW gaps is necessary. Note that the VdW-gaps are aligned with the vacuum level, while the workfunction of the MoS_2 layers are equal to 4eV at this thickness, as evaluated experimentally[23]. Similarly, Figure 2c shows the

electrostatic potential variation in 5 layers of MoS_2. Due to the presence of the VdW gaps, the variation for the layered structure is is not linear with distance, as in the uniform structure, but exhibits two distinct gradients of potential for the MoS_2 region and the VdW region, based on their respective dielectric constant.

The dielectric constant of each VdW gap was set to 1. The dielectric constant of MoS_2 was experimentally measured and the values for different thicknesses are known[24]. For samples thicker than 10 nm, which is the case of the experiments that will be considered in this work, the value is initially 10.5. Nevertheless, as will be later explained, it will be considered as a variable since for previous calculations MoS_2 was considered as a uniform semiconductor. Other basic parameters are set considering reported theoretical and experimental results[8].

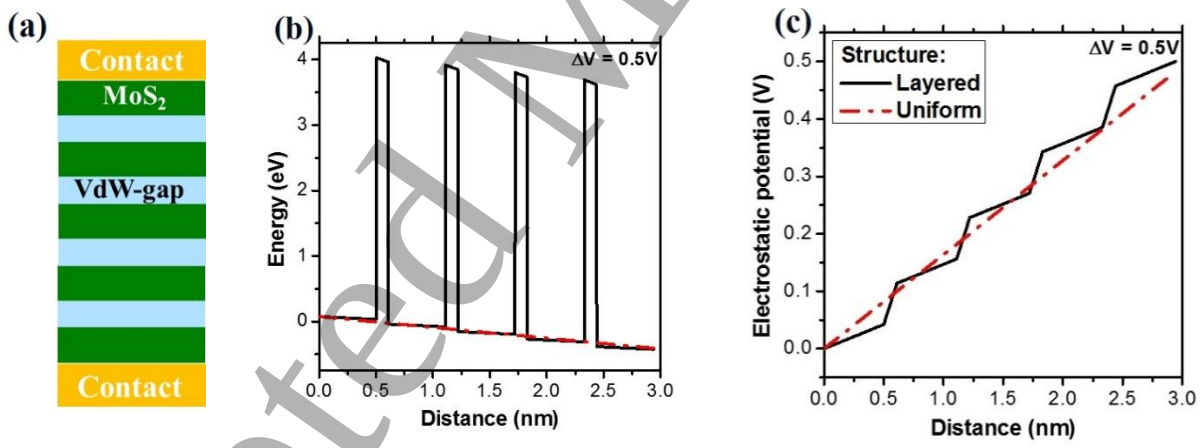

Figure 2: (a) Device structure considered. (b) Conduction band energy and (c) electrostatic potential variation in the layered and uniform structure, with a voltage of 0.5V applied across the device. For these simulations the VdW-gap is 0.11 nm and the MoS_2 thickness is 0.5 nm. The dielectric constant of MoS_2 is equal to 3.

3. METHODOLOGY DEVELOPMENT

The methodology adopted in this work is to first model the vertical transport through the layered MoS_2, and to use this to subsequently model transport of a back gated MoS_2 MOSFET structure. In relation to the Figure 2b, the vertical transport will be determined by direct tunneling

process through the VdW gaps[22]. The model implemented for direct tunneling in Sentaurus is determined by: the barrier height to tunneling (see Figure 2b), the tunneling effective mass of the electron in the VdW gap, and the potential difference between the two MoS_2 layers[22]. The potential difference between two consecutive layers will be determined by the vertical dielectric constant assumed for the single layer of MoS_2. As we assume the VdW gap is vacuum, the barrier to electron tunneling is set at 4eV. Consequently, the parameters to be determined are the dielectric constant of the MoS_2 and the effective electron mass during tunneling. To obtain these values we calibrate the model against published experimental data for vertical transport through MoS_2[25,26].

In the experimental works which will be used to calibrate the tunneling model, MoS_2 was exfoliated on a gold metal pad and SiO_2 or HSQ was patterned by lithography on top of the flake as an isolation layer[25,26]. The top metal was Ni/Au. In this way it was possible to consider only the perpendicular conduction in MoS_2. Based on an analysis of the experimental data assuming the MoS_2 as a homogeneous semiconductor a Schottky barrier of 0.3 eV at the contact was determined for the Au/MoS_2 contact, while the effective perpendicular mass was evaluated to be 0.18 m_0[25]. Both these values will be considered in our simulations as well.

The TCAD software solves the Drift-diffusion equations in both the parallel and perpendicular direction (along the x- and y-axis respectively of Figure 1c). The parallel mobility will be set according to experimental findings as we will explain in a later section. For the modelling of the perpendicular transport, the aim is that this conduction component is limited by tunneling through the VdW-gaps (see Figure S1). To achieve this, the perpendicular electron mobility is increased to a point where it no longer affects the conduction (see Figure S1).

Figure 3a reports the experimental and simulated perpendicular drain current at 3V as a function of the total thickness of the MoS_2. The figure shows 3 curves where the individual layer

thickness of the MoS_2 is varied (and the VdW-gap thickness accordingly). The results at 3V, with a MoS_2 individual layer thickness between 0.5 and 0.55 nm are in reasonable agreement with experiments. We also considered the data from Zhu et al. at 1V (see Figure S2), which show less agreement with the simulations. One reason might be the different top contact used for the devices, Ti instead of Ni, which is known to form a layer of TiO_2 at the MoS_2 interface.

Figure 3b shows the current density considering a variation of the Schottky barrier at the contact from 0.15eV to 0.45eV. The value of 0.3eV is the barrier height used for Figure 3a. A variation in the barrier causes the current density to move almost rigidly along the y-axis. At a voltage of 3V the barrier has little effect on the simulations, because the voltage is considerably higher than the Schottky barrier.

Figure 3c shows the variation in the current density when modifying the dielectric constant of MoS_2, from 3 to 20. The value of 10.5 is the one used initially. The variation in dielectric constant has a significant effect, and a reasonable fitting is obtained with a dielectric of 3, which is consistent with previous theoretical studies[30]. A variation in the dielectric constant will change the partition of the electric field in the device. A lower dielectric in the MoS_2 will increase the potential drop between consecutive MoS_2 layers, which increases the direct tunneling current (see Figure S3). Based on this analysis, while not fully optimized, the following section takes a perpendicular dielectric constant of the MoS_2 as 3, the thickness for the MoS_2 layer will be 0.5 nm, with a 0.11 nm VdW-gap.

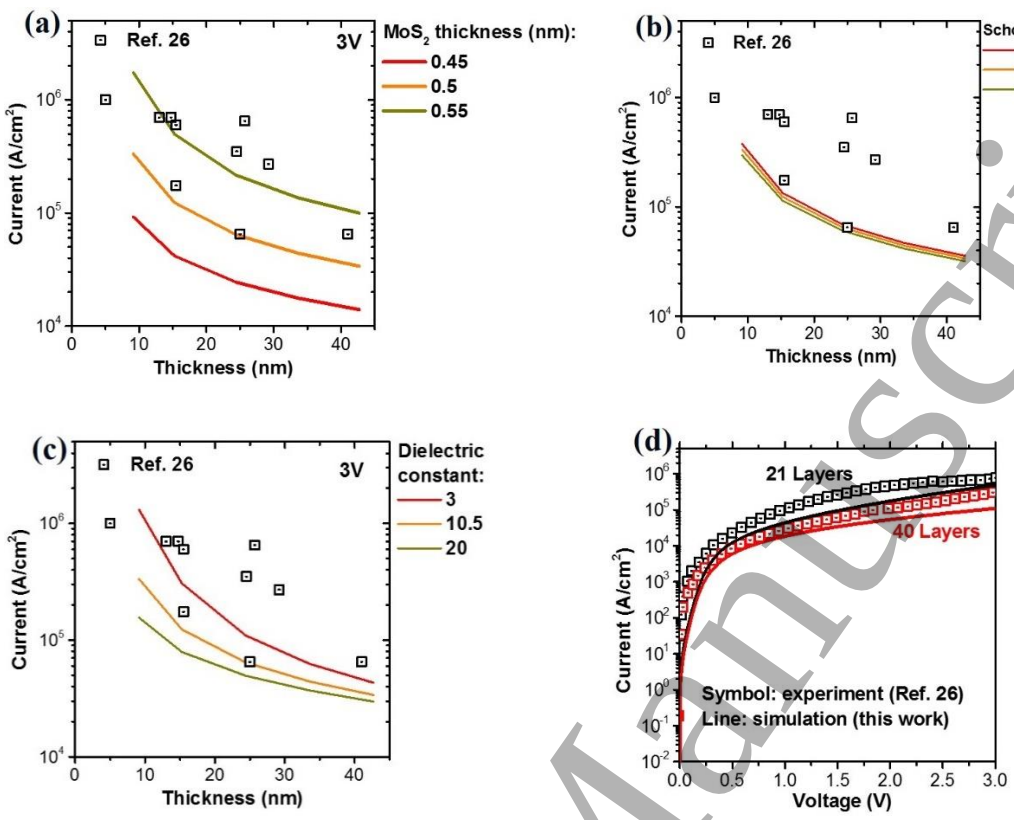

Figure 3: Current density at 3V for different thickness considering a variation of: (a) MoS_2 thickness, (b) Schottky barrier and (c) perpendicular dielectric constant of MoS_2. Unless specified, a dielectric constant of 10.5 and a thickness of 0.5 nm were used for the MoS_2, with a Schottky barrier of 0.3eV. (d) Comparison of the simulated and experimental vertical current for two different thicknesses reported by Zhang et al.[26].

Figure 3d shows the vertical current from two experimental devices with different layers of MoS_2, in comparison with the TCAD model. It is noted that while the parameter tuning process was performed at a fixed voltage (3V) there is a good agreement with the experimental data across the full voltage range and for the two value of MoS_2 thickness[26].

Generally, the differences between simulations and experiments can be related to the immaturity of the material itself, which can cause experimental error in the extraction of the Schottky barrier or the dielectric of MoS_2. The Schottky barrier can differ from the value of 0.3eV for different samples due to different thickness[27], impurities and defects, which are highly present in TMDs in general[28]. As reported by McDonnell et al.[29], a defect density of 0.3%, common in TMDs, can be sufficient to dominate the contact resistance and it can also cause device-to-device

variation. Furthermore, the dielectric constant of MoS_2 might differ from the experimental extracted value as it is not only dependent on the number of layers, but first-principle calculations showed a certain dependency on the perpendicular electric field as well[30].

It is also important to consider that if a uniform structure would be used, instead of a layered structure, the current density would increase or decrease according to the perpendicular mobility defined in the model. Nonetheless, a perpendicular mobility, even if thickness-dependent, does not have a physical meaning at low dimensions, as will be further clarified in the next section.

4. APPLICATION OF THE DEVELOPED MODEL: MoS_2 BACK-GATED FET

Using the parameters for the vertical MoS_2 transport obtained in section 3, the implications of the layered MoS_2 structure to the characteristics of a back-gated MoS_2 MOSFET are considered in this section. For the purpose of this study, which is comparative study between the homogeneous and the layered MoS_2 structure, additional effects such as interface traps or Schottky contacts are not considered. Also, we considered a planar MoS_2, although different directions[31,32] or structures (i.e.: nanotubes[33]) could be potentially considered in the model. The simulated device is discussed in Figure 4a, the channel length is equal to 0.5 µm, and the device is back-gated with 20 nm of SiO_2. The thickness of MoS_2 was chosen as 8 layers and a uniform *n*-type doping concentration of 10^{17} cm^{-3} was chosen[34]. A constant anisotropic mobility model is used (bias independent). The in-plane parallel mobility depends on previous experimental results[35] (Figure 4b), while the out-of-plane conduction is as described in the previous section. This back-gated structure is typical of many MoS_2 FET devices reported in literature.

The device characteristics are compared for the case of the layered structure, with the parameters derived from the previous sections, and for the case of a homogeneous MoS_2 film. While the parallel mobility will be the same between the two models, for the homogeneous MoS_2 case we take a perpendicular mobility of 0.5 $cm^2/V.s$. This is increased from the value of 0.2 $cm^2/V.s$ considered in a previous work[12]. The increase in the perpendicular mobility of 0.5 $cm^2/V.s$ was implemented so that the current level of the two structure is similar to facilitate a qualitative comparison.

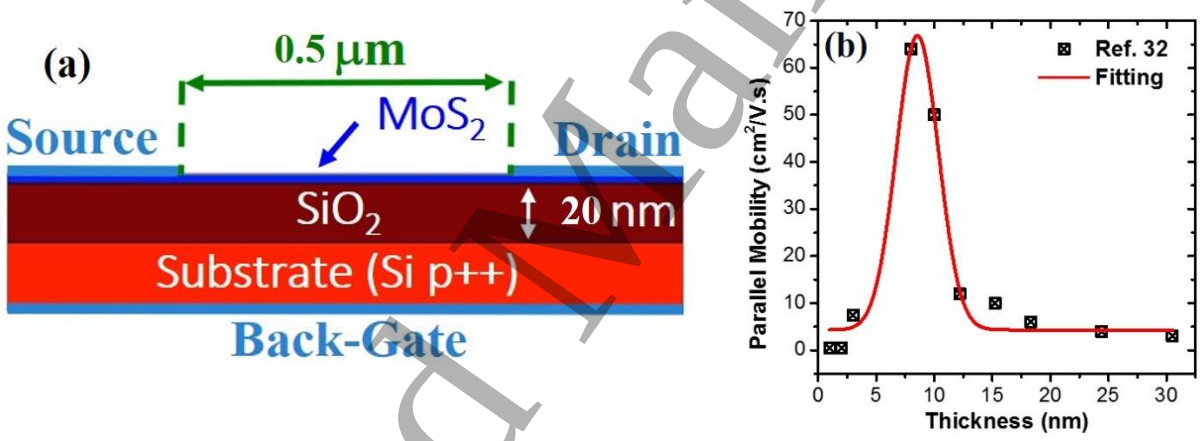

Figure 4: (a) Schematic of the device structure implemented in Sentaurus device. (b) Layer dependent parallel mobility used for both structures[35,35].

Figure 5a and 5b show the transfer characteristic varying drain voltage for the uniform and the layered structure respectively. The first obvious difference is the current density considering the same applied voltages. The layered structure shows a current almost an order of magnitude higher. Nevertheless, the transition from off to on in the layered structure is much gradual around 0.5-1.0 V. In order to clarify both these points Figure 5 c-h show the current density in the whole device, increasing the drain voltage from 0.5 to 3V at a back-gate voltage of 5V.

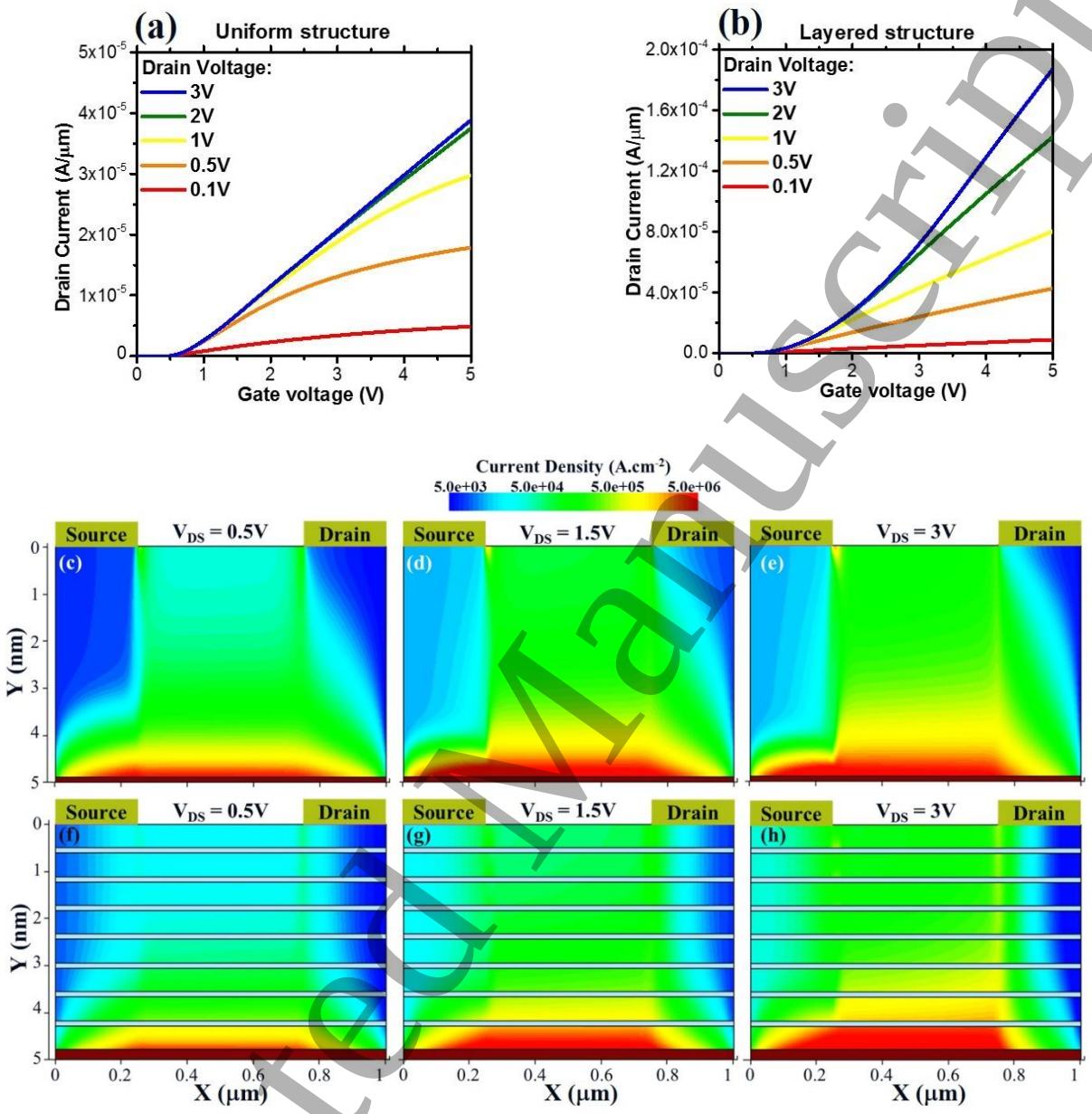

Figure 5: Transfer characteristic for the (a) uniform and (b) layered structure varying the drain voltage from 0.1 to 3V. Current density contour plot varying the drain voltage from 0.5 to 3V for the (c-e) uniform and (f-h) layered structure. Gate voltage is 5V (V_{GS}-V_T≅3V).

Considering first the variation of the current density at any fixed drain voltage it is clear that the current density is mostly limited to the bottom layers. When a drain voltage is applied the current density will increase closer to the drain contact, passing through the whole structure. This is true for both structures, and the increase in drain voltage creates a "path" from the bottom of the

semiconductor to the drain contact. From the contour plots at the highest drain voltage for both structures, Figure 5e and 5h, it is clear that below the tip of the drain contact the current density increases. Another important difference is related to the current density along the horizontal direction, where the variation of the current density with distance, particularly in the 1st MoS_2 layer, or the equivalent depth in the uniform structure, exhibit significant differences (See Fig. S6).

As a result, the difference between the two transfer characteristics is related to how the current vertically passes through the structure. The uniform structure depends on the perpendicular mobility, while for the layered one depends on direct tunneling through the VdW-gaps. Even if the first option might generate results that are in agreement with experimental data the transport process in a real MoS_2 is likely different. Due to a discrete structure formed by separate layers it is unlikely that the process can be simply described by a perpendicular mobility with a Drift-Diffusion transport model. Also, especially for thin devices the assumption of a perpendicular mobility does not have a physical meaning by definition, since the film thickness will be less than the mean free path between collisions. Therefore, the presence of the VdW-gaps provide a more accurate description of the transport in a real MoS_2 film, or 2D-semiconductor in general.

5. CONCLUSIONS

In conclusion, with a combination of experimental findings and theoretical results a physics-based layered structure model was developed for MoS_2. Considering previous reports on the perpendicular conduction in MoS_2 devices, a layered structure that considers both the semiconducting layers of MoS_2 and the Van-der-Waals gaps in between them was developed and optimized for the first time in a TCAD software. The model was then used to shed light on the current distribution in a back-gated MoS_2-based FET.

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