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Prediction of Phase Noise and Spurs in a Nonlinear Fractional- N Frequency Synthesizer

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Abstract—Integer boundary spurs appear in the passband of the loop response of fractional- N phase lock loops and are, therefore, a potentially significant component of the phase noise. In spite of measures guaranteeing spur-free modulator outputs, the interaction of the modulation noise from a divider controller with inevitable loop nonlinearities produces such spurs. This paper presents analytical predictions of the locations and amplitudes of the spurs and accompanying noise floor levels produced by interaction between a divider controller output and a PLL loop with a static nonlinearity. A key finding is that the spur locations and amplitudes can be estimated by using only the knowledge of the structure and pdf of the accumulated modulator noise and the nonlinearity. These predictions also offer new insights into why the spurs appear.

Index Terms—Fractional- N , PLL, spur, prediction, phase noise, nonlinearity, noise floor, spectrum.

I. INTRODUCTION

FRACTIONAL- N PLLs are widely used where the generation of precisely-defined frequency components is required [1]. This includes a huge number of modulation, demodulation and clock generation applications. The versatility and power of fractional- N PLLs has led to their ubiquity in microelectronic systems.

The key feature of the fractional- N architecture is noise-shaped modulation of the divide ratio (typically using a MASH modulator incorporating Digital Delta-Sigma Modulators (DDSMs) [2], although other modulator architectures have also been proposed [3]–[6]). The introduction of the modulator allows the PLL to maintain an effectively fractional input-output frequency ratio, but also brings its main drawback: since the loop feedback divide ratio is directly controlled by a modulation term, this introduces phase noise into the loop. Furthermore, this phase noise may induce strong spurious

periodic components [7]. Spurious components that are outside the passband of the synthesizer can be attenuated by filtering. Those inside the loop cannot be removed easily by filtering. These in-band components usually occur for small values of the fractional divide ratio and are called integer boundary spurs (IBS).

Previous work has attempted to reduce the amplitudes of these spurs by removing them at source, within the divider controller, thus making the spectrum of the latter spur-free [8]. Even if the spectrum of the modulator is itself spur-free, spur regrowth will occur in the loop when nonidealities are present [9], or when cross-coupling occurs within the loop [10]. Furthermore, techniques aimed at removing the phase noise from the loop are only able to achieve attenuation, but not removal, of these spurs [5], [7], [11]–[13]. In spite of techniques that offer improved charge pump linearity [14], the presence of loop nonlinearities is unfortunately inevitable. Progress on elucidating the features of nonlinearity-induced spurs has been slow [15], and only the *locations* of these spurs have so far been predicted, not their *amplitudes* [8], [21].

In this paper we present a semi-analytical technique for deriving a full prediction of the phase noise due to modulation of the nonlinearity—that is, the *locations and amplitudes* of the integer boundary spurs, and the density of the folded quantization noise component—given only knowledge of the modulator output noise and the nonlinear loop transfer function. We demonstrate that the phase noise is a function of the nonlinearity and the statistics of the modulator noise.

The paper is structured as follows. In Section II, we first present an overview of the problem and describe the main features of nonlinearity-induced phase noise and spurs. We then present in Section III a method for predicting the key features of this phase noise, via a signal we term the Periodic Nonlinearity Noise. Section IV demonstrates the reliability of these predictions using comparisons to simulations of four representative fractional- N PLLs from the literature. Finally, we summarize our conclusions in Section VI.

II. INTEGER BOUNDARY SPURS AND NONLINEARITY-INDUCED PHASE NOISE

The architecture of the fractional- N Phase Lock Loop we consider in this work is shown in Fig. 1. The fractional- N PLL modulates the instantaneous, integer feedback division ratio, $N[n]$, such that it approximates a desired nominal, fractional division ratio, N_{nom} [16]. This is done by the introduction of

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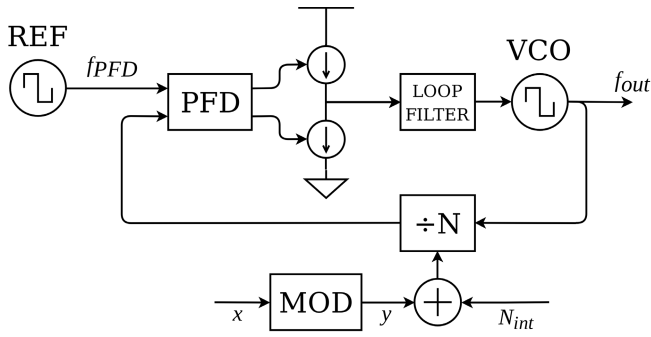


Fig. 1. Structure of a fractional- N PLL employing a DDSM as a divide ratio controller.

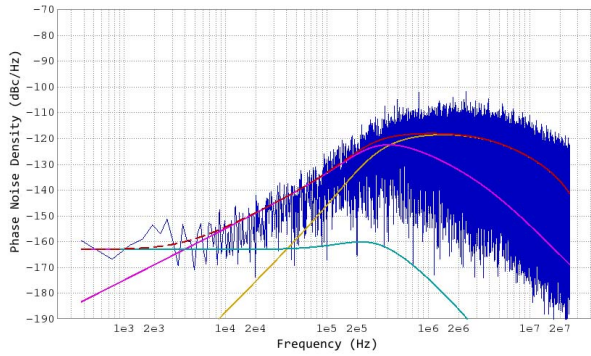


Fig. 2. Simulated contribution of the MASH to the output phase noise spectrum of a linear fractional- N PLL (dark blue). Colored smooth curves indicate theoretical estimates of the individual contributions due to MASH modulation noise [16] (yellow), first-order shaped dither [16] (cyan), noise due to non-uniform sampling [22] (purple) and the total noise envelope (red, dashed), assuming that the additive quantization noise in the MASH is white.

a modulation term, $y[n]$, with a fractional mean. Thus,

$$N[n] = N_{\text{int}} + y[n]; \quad N_{\text{nom}} = N_{\text{int}} + E\{y\}, \quad (1)$$

where $E\{\cdot\}$ denotes the expectation operator.¹

The primary rationale for the design of the DDSM is the desire to produce modulation noise that is pushed to higher frequencies, so that the bulk of this noise is filtered by the low-pass loop response. Fig. 2 shows the contributions to the output phase noise spectrum of a simulated linear PLL due to modulation noise, using a dithered MASH 1-1-1 modulator. The effective use of dithering can guarantee a spur-free modulator output [17]–[20]. The PLL parameters are given in Table I, where f_{PFD} is the loop PFD frequency, x is the input to the modulator, which we take as constant in this work, and M is the modulus of the MASH. $M = 2^B$, where B is the bit width of each DDSM accumulator in the MASH. Hence, $E\{y\} = x/M$.

In an actual system, the PLL loop will be nonideal, and typically nonlinear. The simulated contribution to the output

¹Throughout this paper, it is insinuated that y is a stochastic signal. Since the modulator is normally implemented as an entirely deterministic Finite State Machine (FSM), as in the case of a MASH modulator with or without pseudorandom dither, then y is deterministic. In this case, the Probability Mass Function of y , $P(y)$, is taken to equal the steady-state probabilities of the FSM output, while the expectation of y is defined as the population mean of y , as usual.

TABLE I
PLL DESIGN USED IN SECTION II

x	17
M	2^{16}
N_{FFT}	2^{17}
f_{PFD}	50 MHz
Bandwidth	550 kHz

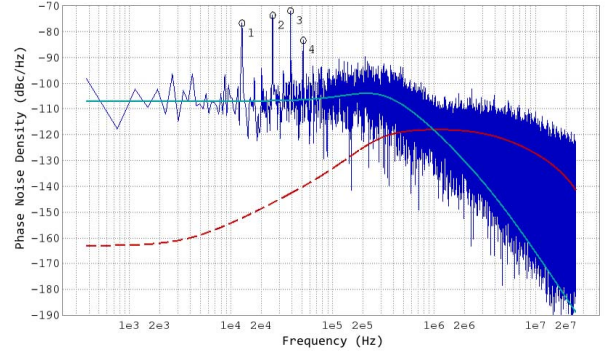


Fig. 3. Output phase noise spectrum of a simulated fractional- N PLL with a nonlinear loop transfer function, representing a nonideal loop. The cyan curve indicates the loop response. The (dark blue) phase noise spectrum shows a notable departure from the total noise envelope in Fig. 2 that assumes linear conditions (red, dashed).

phase noise spectrum in this case, shown in Fig. 3, is very different. We can divide this spectrum into three components:

- 1) The linear component of the high-pass modulation noise is still present, although it may be stronger or weaker because the gain of the loop transfer function from the feedback divider to the output will be modified by the linear component of the nonlinearity.
- 2) A white noise floor has appeared (in this example, at approximately -108 dB/Hz), which is also low-pass shaped by the loop response.
- 3) Strong integer boundary spurs appear (labeled 1, 2, 3 and 4 in the figure).

The latter two noise and spur components result from the interaction between the modulation noise and the nonlinearity; if either is removed, these components are not present.

It should be noted that the spurs lie at integer multiples of a fundamental frequency—the frequency of the lowest spur—which indicates that these spurs result from an underlying periodic phenomenon. We can offer the following empirical prediction for the fundamental frequency of this phenomenon:

$$f_{\text{spur}} = \frac{x}{M} f_{\text{PFD}}, \quad (2)$$

when $x/M \ll 1$.

Note that we are assuming a loop frequency of f_{PFD} . Therefore folding about $f_{\text{PFD}}/2$ must be applied to the result of Eq. (2) to determine the actual frequency offset from the carrier; it follows that inputs of x and $(M - x)$ will result in similar fractional spurs [21].

In order to predict fully the contribution to the PLL's output phase noise spectrum due to the modulation noise,

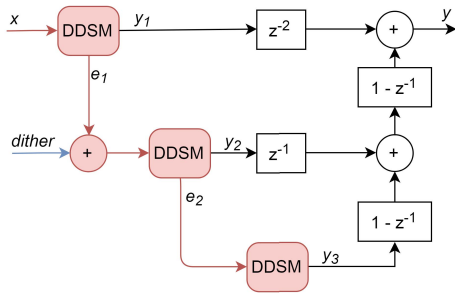


Fig. 4. MASH 1-1-1 modulator used as a divide ratio controller in this paper. Pseudorandom binary dither is used to ensure that the output is spur-free [18], [19].

TABLE II
MASH 1-1-1 MODULATOR USED IN SECTIONS III & IV

x	17
M	2^{16}
f_{PFD}	50 MHz
N_{sim}	2^{19}
N_{FFT}	2^{19}
Overlap	50%

we require four pieces of information: a) the gain of the loop transfer function from the feedback divider to the output, b) the positions of the integer boundary spurs, c) the amplitudes of the integer boundary spurs, and d) the level (power spectral density) of the noise floor. The first piece is easily identified from the linear component of the transfer function, while the second piece is given by Eq. (2). This leaves two unknowns: the amplitudes of the integer boundary spurs, and the level of the noise floor.

III. PREDICTION OF NONLINEARITY-INDUCED PHASE NOISE

Throughout this paper, we assume that the feedback divider is controlled by the dithered MASH 1-1-1 modulator shown in Fig. 4, with the parameters given in Table II. This method can be readily adapted to other architectures.

We begin by assuming the simplest case where the modulator input x is a small value relative to M , which ensures that fractional spurs are located in the passband. Our analysis will also apply to very large values of x , after applying necessary sign changes.² In general, in-band spurs will occur when x is very close to integer fractions of M ; an extension of this method to the general case is presented in the Appendix.

A. Modulation Noise

The required average divide ratio is $N_{\text{int}} + x/M$. This is approximated at time instant $t = n/f_{\text{PFD}}$ by dividing the output frequency by $N[n] = N_{\text{int}} + y[n]$, where f_{PFD} is the update frequency of the PFD.

²Observing that $(M - x) \equiv -x \pmod{M}$, the behavior with a modulator input of $(M - x)$ mimics that of x , but the signs are reversed, and hence Figs. 5 and 6 are mirrored across the $y = 0$ axis with the tracks ascending instead of descending.

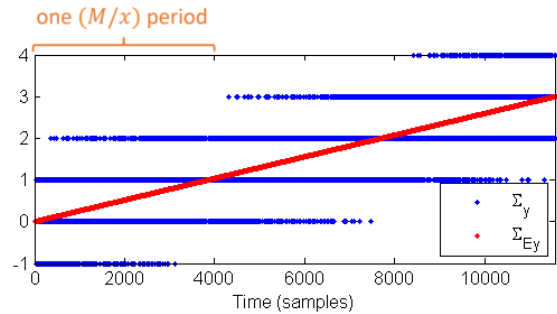


Fig. 5. Accumulated digital modulator output Σ_y (blue) and expected fractional output Σ_{E_y} (red).

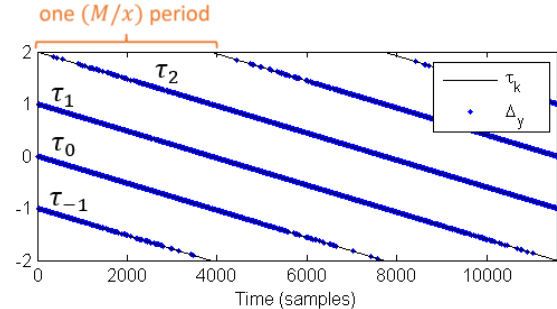


Fig. 6. Modulation noise signal Δ_y . Each (blue) sample of the signal $\Delta_y[n]$ lies on an underlying (black) line segment denoted τ_k .

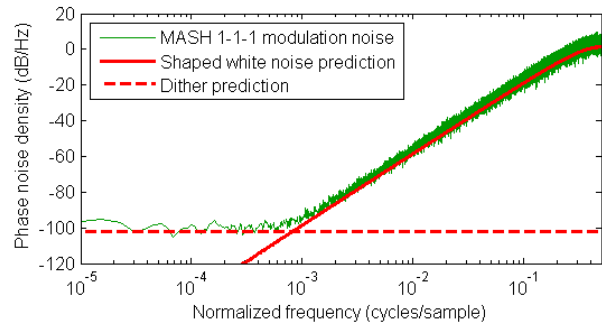


Fig. 7. Spectrum of modulation noise from the MASH 1-1-1 modulator, showing spur-free behavior in spite of the periodic pattern in Fig. 6.

Fig. 5 shows the desired accumulated output $\Sigma_{E_y}[n]$ (red) and the approximation $\Sigma_y[n]$ (blue), where

$$\Sigma_y[n] = \sum_{k=0}^n y[k] \quad (3)$$

and

$$\Sigma_{E_y}[n] = \sum_{k=0}^n \frac{x}{M}. \quad (4)$$

The difference between these two signals, shown blue in Fig. 6, is the quantization noise which we call *modulation noise* in this paper; it is defined by

$$\Delta_y[n] = \Sigma_y[n] - \Sigma_{E_y}[n]. \quad (5)$$

Fig. 7 shows the spectrum of Δ_y , demonstrating the lack of inherent spurs in the accumulated output. Welch's method is used throughout the paper to generate the spectrograms (unless otherwise stated).

Note that y is dimensionless; it denotes the instantaneous divide ratio of the loop. Hence, the modulation noise, Δ_y , is also dimensionless. It can be expressed as a phase error, which is called the *modulation phase noise*, using [16]:

$$\phi_{\text{mod}} = \frac{2\pi}{N_{\text{nom}}} \Delta_y, \quad (6)$$

or as a time offset from the reference clock edge, using [16]:

$$t_{\text{mod}} = \frac{1}{f_{\text{PFD}} N_{\text{nom}}} \Delta_y, \quad (7)$$

where N_{nom} is the nominal divide ratio. The error is referenced to the PFD input in each case.

The contribution of ϕ_{mod} to the PLL output phase noise spectrum can then be calculated using [16]:

$$S_{\phi_{\text{out, mod}}}(f) = \left(\frac{N_{\text{nom}}}{f_{\text{PFD}}} \right)^2 |G(f)|^2 S_{\phi_{\text{mod}}}(f), \quad (8)$$

where $S_{\phi_{\text{mod}}}$ and $S_{\phi_{\text{out, mod}}}$ are the spectra of the modulation phase noise referred to the PFD input and its contribution to the output phase noise, respectively, and $G(f)$ is the normalized frequency response of the PLL loop, as described in [16]. Note that $G(0) = 1$.

It is clear from Eqs. (6) and (8) that, in the passband of $G(f)$, the contribution of the modulation noise to the output phase noise spectrum is a scaled version of the spectrum of Δ_y . Since we are interested in predicting passband spurs and phase noise, we will study Δ_y directly in the remainder of this paper. It should be mentioned, however, that our prediction also holds outside of the passband, as long as the attenuation caused by the loop response $G(f)$ is taken into account.

B. Tracks and Probability Distribution

When x is constant, Eq. (5) becomes

$$\Delta_y[n] = \Sigma_y[n] - n \frac{x}{M}. \quad (9)$$

Since $y[n]$ is an integer-valued function, so is $\Sigma_y[n]$.

Define *tracks*

$$\tau_k(t) = k - t \frac{x}{M}, \quad (10)$$

$t \in \mathbb{R}$, where each track corresponds to a different value of k . Then, for every integer n ,

$$\Delta_y[n] = \tau_k(n) \quad (11)$$

for some $k \in \mathbb{Z}$.

The output y of the MASH 1-1-1 is bounded between -3 and $+4$. The modulation noise Δ_y is bounded between -2 and $+2$, as shown in Fig. 6. Therefore, for $0 \leq t < M/x$, each sample of Δ_y lies on one of four distinct tracks τ_k , $k \in \{-1, 0, 1, 2\}$ in this example.

In general, for $jM/x \leq t < (j+1)M/x$, $|\Delta_y| < A$ and samples of Δ_y lie on one of $2A$ tracks τ_k , $k \in \{j-A+1, j-A+2, \dots, j+A-1, j+A\}$. Since the choice of the time origin is arbitrary, we can map each interval of length M/x in Fig. 8(a) onto the interval $0 \leq t < M/x$, as shown in Fig. 8(b).

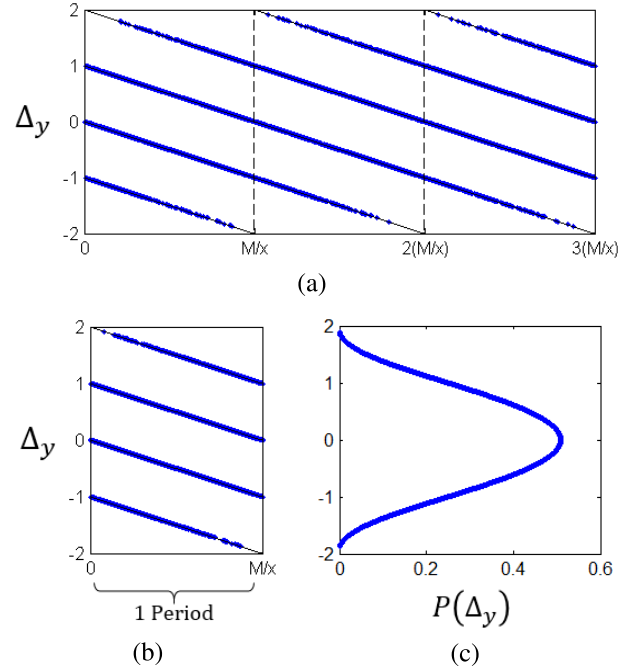


Fig. 8. (a) Samples of Δ_y (blue) are distributed over tracks τ_k (black); (b) Due to periodicity, all samples can be mapped onto a finite set of tracks (four in this example); (c) The distribution of samples of Δ_y defines the probability distribution $P(\Delta_y)$.

Note that the domain $[-2, +2]$ of Δ_y can be subdivided into four regions $[-1, -2)$, $[0, -1)$, $[+1, 0)$ and $[+2, +1)$ corresponding to the four tracks τ_k , $k = -1, 0, +1, +2$.

Next we determine the probability distribution of Δ_y . Consider N samples $\Delta_y[n]$, $n = 0, 1, 2, \dots, N$, where N is large. In the case of a MASH 1-1-1 modulator with modulus M , an odd initial condition, and first-order pseudorandom dithering with period L_d , the period of the signal y is $2ML_d$ [23]. For example, with $M = 2^{25}$ and a pseudorandom binary sequence generated by a 24-bit linear feedback shift register, $2ML_d \approx 10^{15}$.

Following (9), the N samples of $\Delta_y[n]$ can take on values in the discrete set $\{-A, -A + \frac{1}{M}, -A + \frac{2}{M}, \dots, +A - \frac{1}{M}, +A\}$. Define

$$P(\Delta_y = m) = \frac{\#\{n : \Delta_y[n] = m\}}{N}, \quad (12)$$

where $\#$ denotes cardinality. The probability distribution for this example is shown in Fig. 8(c).

At this juncture, it is worth pointing out that the only assumptions made so far are that the modulator is digital with a small output mean. Consequently, this analysis applies to *every digitally modulated fractional- N PLL*. Although we focus mainly on a MASH 1-1-1 divider controller in this work, the results apply to *all* digital divider controller structures, including, amongst others, successive quantizers [5].

C. Interactions Between the Modulator Output and the Loop Nonlinearity

A static nonlinearity can be treated as a mapping from the domain of the modulation noise to the co-domain of a new

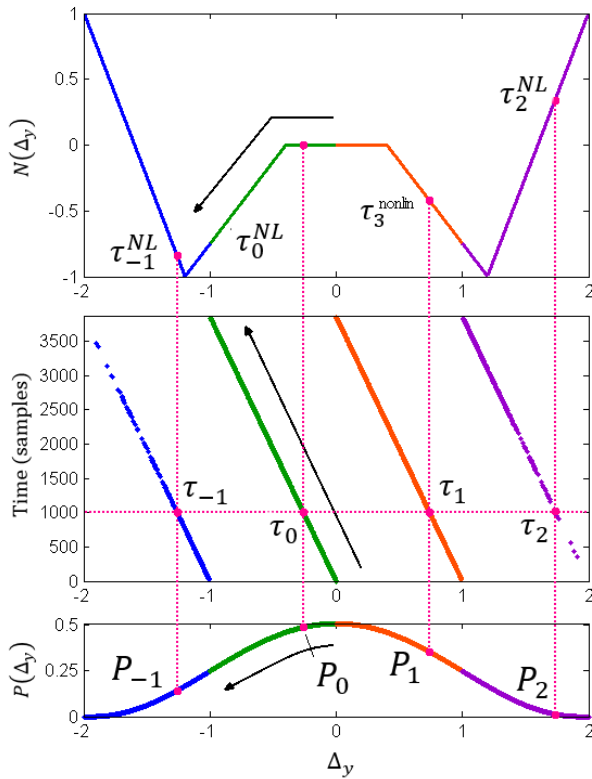


Fig. 9. Demonstration of how the modulation noise Δ_y (center) from Fig. 6 produces a nonlinearity noise signal, Δ_y^{NL} , by indexing the nonlinearity (top) according to the probability $P(\Delta_y)$ (bottom). The situation at $t = n_0 = 1000$ is highlighted. The arrow of time is indicated in black.

nonlinearity noise signal. For the purposes of illustration, in this subsection we will demonstrate the waveforms resulting from applying the modulation noise of the MASH 1-1-1, studied in the preceding sections, to a static nonlinear transfer function.

Fig. 9 shows an example nonlinear function³ (top), the rotated modulation noise waveform from Fig. 6 (middle) and the modulation noise Probability Mass Function (PMF, bottom), where each point has been colored by track, and the black arrows denote the passage of time. We restrict our analysis to the situation where the loop has settled into steady-state behavior and the loop nonlinearity can be described by a static nonlinearity transfer function.

We denote by Δ_y^{NL} the nonlinearly distorted modulation noise which arises from the interaction between Δ_y and the nonlinearity $\mathcal{N}(\cdot)$. Thus,

$$\Delta_y^{NL} = \mathcal{N}(\Delta_y). \quad (13)$$

Physically, Δ_y^{NL} , shown in Fig. 10, corresponds to the excess phase error introduced into the loop by the presence of the loop nonlinearity. The spectrum of this signal is shown in Fig. 11. Unlike the spectrum of the underlying modulation noise Δ_y in Fig. 7 which is spur-free and highpass filtered,

³This specific nonlinearity has no physical meaning. It is simply used for illustration purposes.

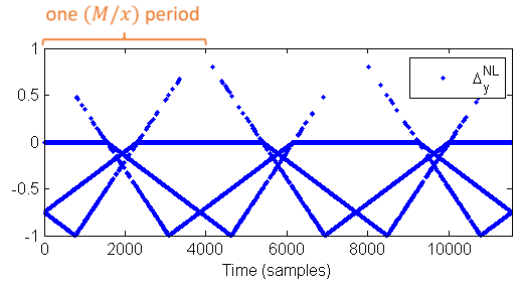


Fig. 10. Nonlinearly distorted modulation noise $\Delta_y^{NL}[n]$ in the time domain.

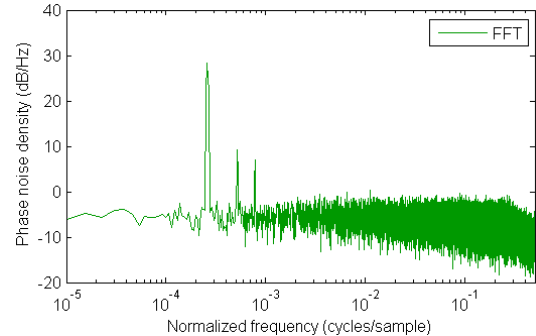


Fig. 11. Frequency spectrum of the nonlinearly distorted modulation noise Δ_y^{NL} .

this signal has an elevated flat noise floor and strong periodic components.

D. Periodic and Noiselike Components of the Nonlinearly Distorted Modulation Noise

An important step in predicting the spectrum of the nonlinearly distorted modulation noise is to consider separately the periodic and noise-like behaviors. Denote by τ_k^{NL} the image of the track τ_k under the mapping $\mathcal{N}(\cdot)$. We have that

$$\tau_k^{NL}(t) = \mathcal{N}(\tau_k(t)) \quad \forall k. \quad (14)$$

Fig. 12 shows nonlinearly distorted noise samples Δ_y^{NL} (blue, green, orange and purple) and tracks τ_k^{NL} (black) for the example in Fig. 9.

Referring first to Fig. 9, consider the time instant $t = n_0 = 1000$, indicated by the dashed red line in the central subplot. To simplify the notation, define

$$\begin{aligned} P(\Delta_y = \tau_{-1}(n_0)) &= P_{-1} \\ P(\Delta_y = \tau_0(n_0)) &= P_0 \\ P(\Delta_y = \tau_{+1}(n_0)) &= P_{+1} \\ P(\Delta_y = \tau_{+2}(n_0)) &= P_{+2}, \end{aligned}$$

as shown in the bottom subplot.

Note that

$$\Delta_y[n_0] = \begin{cases} \tau_{-1}(n_0) & \text{with probability } P_{-1} \\ \tau_0(n_0) & \text{with probability } P_0 \\ \tau_{+1}(n_0) & \text{with probability } P_{+1} \\ \tau_{+2}(n_0) & \text{with probability } P_{+2} \end{cases} \quad (15)$$

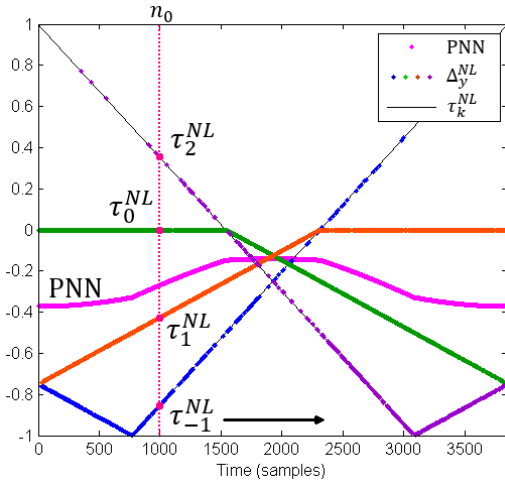


Fig. 12. Nonlinearity noise Δ_y^{NL} produced by the features illustrated in Fig. 9, shown with the corresponding tracks τ_k^{NL} (black). The instant $t = n_0 = 1000$ is highlighted dashed in red.

After the mapping $\mathcal{N}(\cdot)$, and referring to Fig. 12, we have that

$$\Delta_y^{\text{NL}}[n_0] = \begin{cases} \tau_{-1}^{\text{NL}}(n_0) & \text{with probability } P_{-1} \\ \tau_0^{\text{NL}}(n_0) & \text{with probability } P_0 \\ \tau_{+1}^{\text{NL}}(n_0) & \text{with probability } P_{+1} \\ \tau_{+2}^{\text{NL}}(n_0) & \text{with probability } P_{+2} \end{cases} \quad (16)$$

We call the average value of $\Delta_y^{\text{NL}}[n]$ the Periodic Nonlinearity Noise, denoted *PNN*, where:

$$PNN[m] = \sum_{k=-1}^{+2} \tau_k^{\text{NL}}(m) P(\tau_k(m)), \quad (17)$$

where $m \in \{0, 1/x, 2/x, \dots, (M-1)/x\}$.

The periodic extension of the *PNN* signal, shown in magenta in Fig. 12, is periodic with period M/x .

The complementary component of the phase noise describes the aperiodic behavior of the nonlinearly distorted modulation noise, i.e. the noise floor in Fig. 11. We call this component the Stochastic Nonlinearity Noise (*SNN*), defined by:

$$SNN[n] = \Delta_y^{\text{NL}}[n] - PNN[m], \quad (18)$$

where $m = n \bmod (M/x)$.

Fig. 13 shows the spectra of *PNN* and *SNN*, where it can be seen that these concepts separate the periodic and stochastic behavior of the nonlinearly distorted modulation noise, the entire spectrum of which is shown in Fig. 11.

Note that the *SNN* is entirely aperiodic, almost white noise. This is consistent with the common observation that the nonlinearity contributes a flat noise floor to the passband of the phase noise spectrum. An intuitive explanation for the typically flat frequency spectrum of the *SNN* requires considering the nonlinearity as a power series, and observing that odd and even powers of a sinusoid produce frequency components at respectively odd and even multiples of the sinusoid frequency. Sampling effects fold these frequency

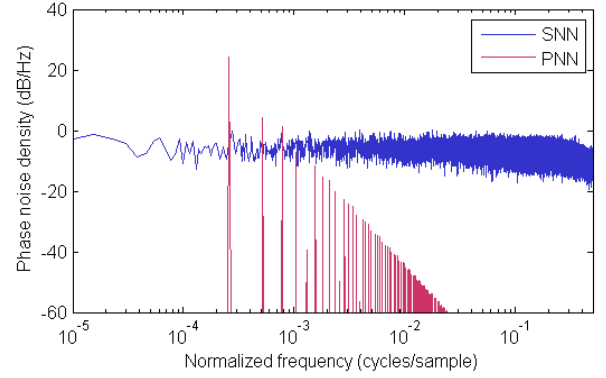


Fig. 13. Frequency spectrum of the *PNN* (magenta), consisting of harmonics of frequency $(x/M) \text{ rad s}^{-i/2+1}$, and the *SNN* (blue), which takes the form of white noise (with some rolloff near the Nyquist frequency). Welch's method is used for the *SNN*, while a traditional FFT is used to represent the *PNN* so as to clearly distinguish the spurs.

components, thus redistributing the noise power across the spectrum.⁴

E. Quantifying the Noise Floor and Spur Amplitudes

In Section II we stated that in order to predict the phase noise due to loop nonidealities accurately, we required two pieces of information: the locations and amplitudes of the spurs, and the level of the noise floor due to the nonlinearity. The spurs and noise floor are described by the *PNN* and *SNN* signals, respectively, and hence a prediction can be made.

Since the *PNN* contains only the spurious components of Δ_y^{NL} , the amplitudes of these spurs can be extracted using the DTFS. The variance of the *SNN* can be determined in a manner similar to Eq. (17), by calculating the variance of the difference between each track, τ_k^{NL} , and the *PNN*, weighted by the associated probability sequences $P(\tau_k)$:

$$\sigma_{SNN}[m] = \sum_k P(\tau_k(m)) \left(\tau_k^{\text{NL}}(m) - PNN[m] \right)^2. \quad (19)$$

where $m \in \{0, 1/x, 2/x, \dots, (M-1)/x\}$.

The level of the noise floor, where the *SNN* is assumed to take the form of white noise, is then given by:

$$S_{SNN} = 10 \log_{10} \left(\sigma_{SNN}^2 \right), \quad (20)$$

where N_{FFT} is the length of the spectrum.

In Fig. 14, these predictions are compared to the actual frequency spectrum of the nonlinearity noise. Note that the spur locations and amplitudes match for the three most significant spurs.

IV. SIMULATION

The method for predicting the phase noise arising from loop nonidealities will next be applied to four example nonlinearities from the literature:

⁴It is assumed that the aperiodic noise due to the nonlinearity is flat in the spectrum. While this is true in many practical cases, it does not necessarily hold generally and is treated here as a helpful approximation.

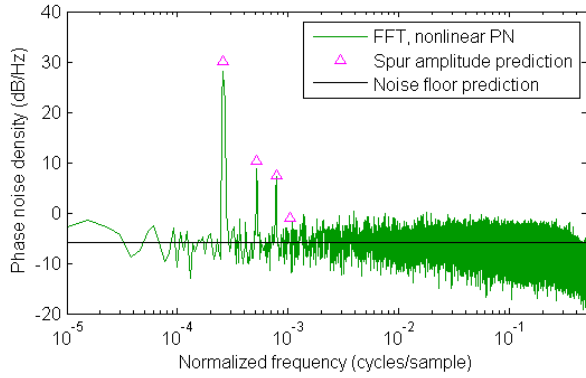


Fig. 14. Frequency spectrum of the nonlinearly distorted modulation noise, compared to the spur predictions offered by (17) (triangles) and the noise floor prediction offered by (20) (black).

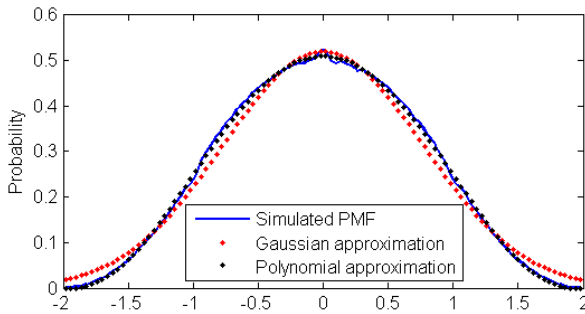


Fig. 15. PDF of modulation noise, Δ_y , of a simulated MASH 1-1-1 modulator, showing the poor Gaussian fit (red) and the more appropriate polynomial fit used in the following examples (black).

- A piecewise-linear function with a discontinuous derivative at $(\phi - \phi_0) = 0$,
- A piecewise-linear function with a discontinuous derivative at $(\phi - \phi_0) \neq 0$,
- A piecewise-exponential function with a discontinuous derivative at $(\phi - \phi_0) \neq 0$, and
- A simple polynomial function.

We make several simplifications when predicting the spur amplitudes and noise level. Firstly, instead of attempting to derive an analytical expression for the accumulated modulation noise PMF, we derive it numerically through simulation of the MASH 1-1-1 modulator. A Gaussian approximation was deemed inappropriate,⁵ as can be seen in Fig. 15, so the following polynomial approximation was used:

$$f(\Delta_y) \simeq \begin{cases} 0 & \Delta_y < -1.9 \\ -0.0006\Delta_y^8 + 0.0014\Delta_y^6 \\ + 0.0497\Delta_y^4 - 0.3111\Delta_y^2 \\ + 0.5095 & -1.9 \leq \Delta_y \leq 1.9 \\ 0 & \Delta_y > 1.9. \end{cases} \quad (21)$$

The nonlinearity could be instead referenced to the phase offset at the input of the PFD, as before, by applying $\Delta_y = (N_{\text{nom}}/2\pi)\phi$, where N_{nom} is the nominal PLL divide ratio [16].

⁵More correctly, Δ_y was found to be platykurtic as $\gamma_2 = -0.59$.

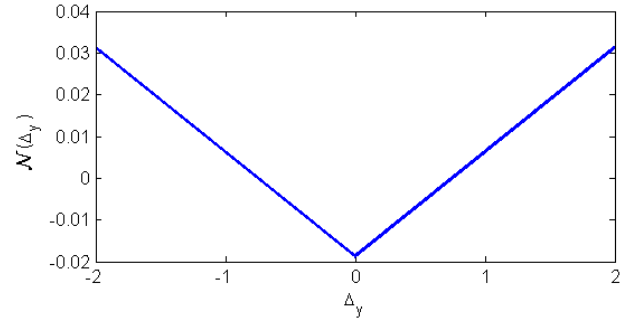


Fig. 16. A piecewise linear nonlinearity.

Secondly, unlike the example nonlinearity of Fig. 9 which was used up to this point, the PLL transfer functions considered below contain both linear and nonlinear components, and we are only interested in the latter. Extracting the linear component could be done by applying a linear fit to the nonlinearity in the region over which Δ_y spans. However, since the probability of Δ_y is not uniform, this will overemphasize the contribution of the extremities; hence, the linear component was estimated by applying a linear fit to the nonlinearity in the central 3/4 of the region over which Δ_y spans (i.e. in the range $[-1.5, +1.5]$), and this component was subtracted from the transfer function in order to estimate the nonlinear component.

We will continue to study the spectrum of the nonlinearly distorted modulation noise, Δ_y^{NL} , with the understanding that this is a good proxy for the contribution to the PLL output phase noise for the reasons detailed in Section III-A.

A. Piecewise-Linear Nonlinearity

The simplest nonlinearity studied in this paper consists of two linear sections with different slopes. This piecewise-linear nonlinearity is commonly used to model the situation where the charge pump has mismatched positive and negative currents, respectively [24], [25], although current mismatch also results in nonlinearity noise which is not centered on the discontinuity [26].

Neglecting the inevitable offset which occurs in practice, we have considered the case where the nonlinearity noise is centered on the discontinuity (i.e. the quiescent point is at the discontinuity), because this is the simplified situation most often studied in the literature.

We will consider the situation where there is a 5% mismatch between charge pump currents, which produces the nonlinearity shown in Fig. 16. Since the nonlinearity is piecewise-linear, and the nonlinearity noise is centered on the discontinuity, the tracks, τ_k^{NL} , consist of lines, shown black in Fig. 17(a). The spur amplitude and noise floor predictions, shown in Fig. 17, match the simulated nonlinearity noise reasonably well.

Razavi has derived a prediction for the ratio between the peak of the *overall* phase noise, given by $\Delta_y + \Delta_y^{\text{NL}}$, and the nonlinearity noise floor in the case of a specified charge pump mismatch, $\Delta I/I_{\text{CP}}$ [25]. For a given PLL and modulator, the amplitude of the peak is fixed and does not depend on the nonlinearity as the modulation noise dominates at high

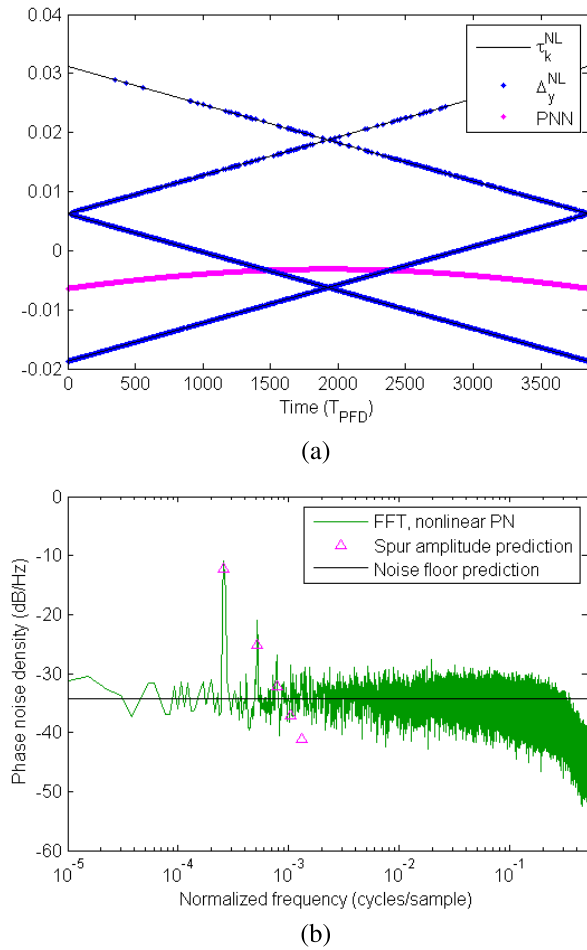


Fig. 17. Nonlinearity noise and PNN (a) and spectrum (b) of simulation incorporating the piecewise linear nonlinearity in Fig. 16.

frequencies. The level of the noise floor is predicted to be:

$$20 \log_{10} \left(\frac{\Delta I / I_{CP}}{4} \right), \quad (22)$$

relative to the peak [25].

This prediction is valid only for the case where the quiescent point is *exactly* at the discontinuity, as is the case with this nonlinearity, and only provides a prediction for the *relative* offset between the noise floor of the nonlinearity noise and the peak of the modulation noise. It makes no prediction about spur amplitudes. By contrast, our technique provides an absolute prediction for the amplitudes of the spurs.

Eq. (22) predicts that the noise floor will lie 38.1 dB and 32.0 dB below the peak when there is a mismatch of 5% and 10%, respectively, with the peak appearing at +4.26 dB/Hz in our example. Fig. 18 compares this and our predictions to the simulated phase noise.⁶

Razavi's prediction is found to match the simulated noise floor closely, while our prediction underestimates the noise floor by roughly 3 dB in each case. The reason for this is that

⁶The modulator input in Figs. 18 and 21 has been changed to $x = 137$, in order to show spurs at higher frequencies; all other parameters remain unchanged.

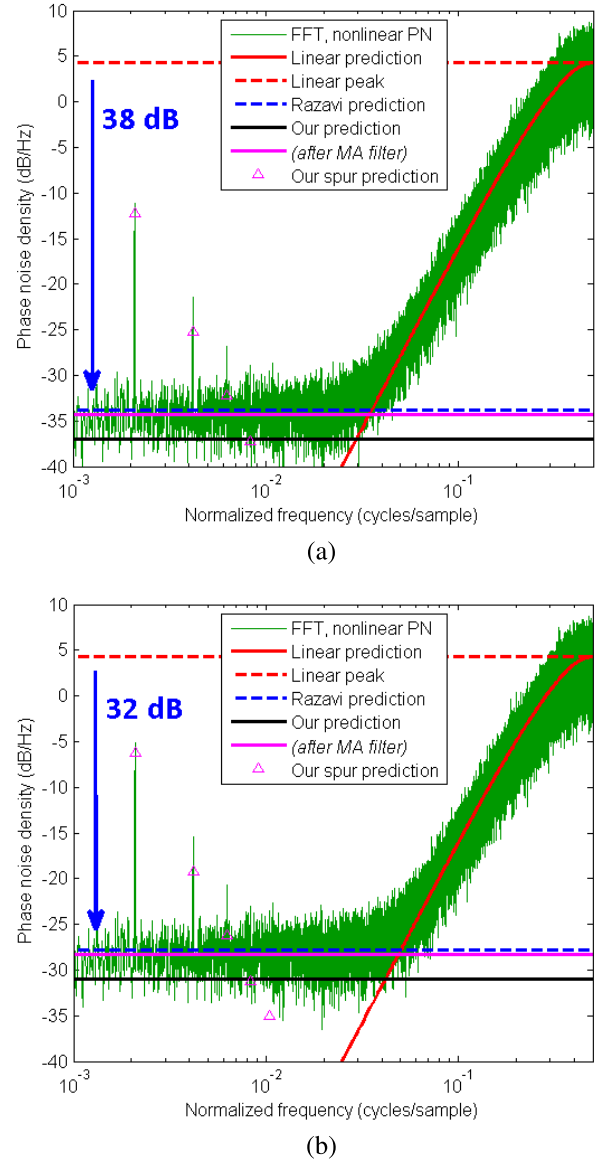


Fig. 18. Frequency spectrum of overall phase noise (modulation and nonlinearity noise) resulting from PWL nonlinearity corresponding to a charge pump mismatch of (a) 5% and (b) 10%, with the noise floor, spur and peak predictions shown.

the spectrum of the estimated SNN isn't flat, as can be seen in Fig. 17, which causes Eq. (20) to underestimate the low-frequency noise floor. This can be overcome by passing the estimated SNN through a low-pass filter, which removes the high-frequency roll-off, before applying Eq. (20). A 10-point moving-average filter was used in this case. The resulting corrected prediction, illustrated by the magenta line in Fig. 18, accurately predicts the noise floor. Additionally, our spur prediction accurately tracks the change in amplitude of the largest spur.

Arora *et al.* present a similar prediction for the corner frequency, which is the frequency at which the power density of the nonlinearity noise floor is equal to that of the linear modulation noise ($f_c = f$ such that $S_{y_{nonlin}}(f) = S_{y_{mod}}(f)$) [27]. By equating [16, Eq. (23)] (after making the substitution $T \equiv 1/f_{PFD}$) with our prediction and that given by Razavi,

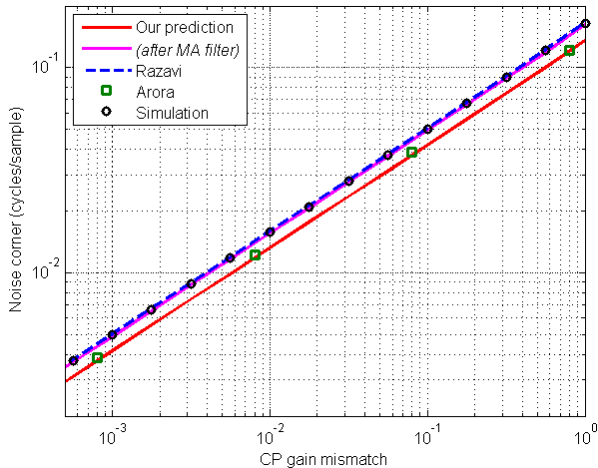


Fig. 19. Comparison of the corner frequencies given by each of the three predictions, with the corner frequency seen in simulation.

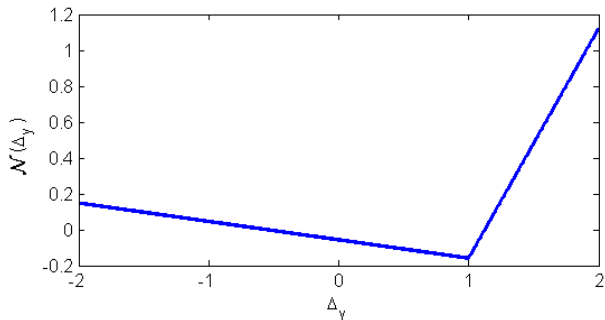


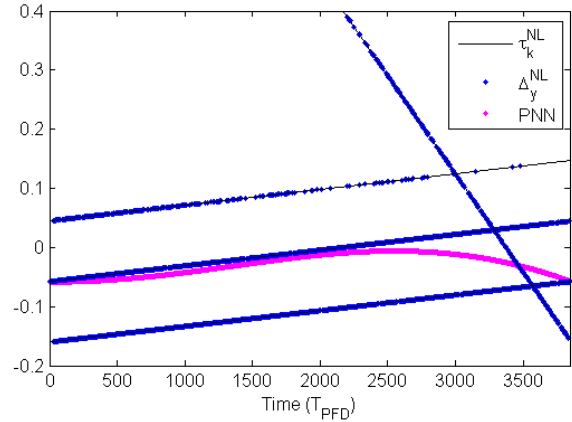
Fig. 20. A piecewise linear nonlinearity with the quiescent point at $\phi_0 \neq 0$.

respectively, we can determine the corner frequency in each case. These are shown graphically in Fig. 19. Our prediction, after removal of the high-frequency roll-off, and Razavi’s prediction both closely match the simulation for a wide range of mismatch values. Arora’s prediction slightly underestimates the corner frequency.

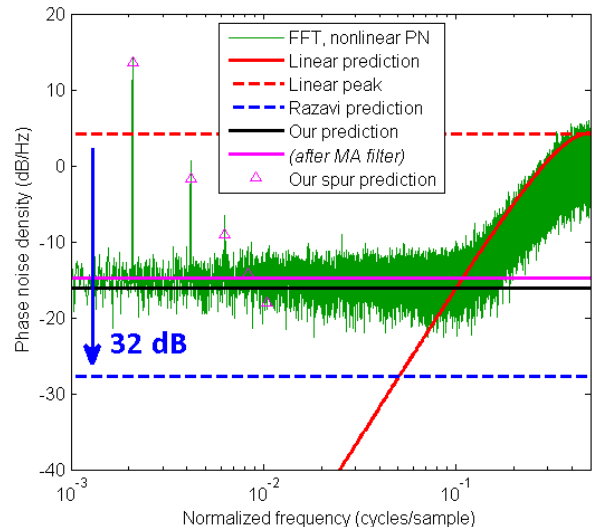
B. Piecewise-Linear Nonlinearity With Offset Quiescent Point

We have previously mentioned that Razavi’s estimate only applies to the case where the discontinuity lies *exactly* at the center of the nonlinearity. Fig. 20 shows the nonlinearity resulting from a 5% mismatch, as before, except that the quiescent point has been offset such that the discontinuity occurs at a point 1/4 the width of the region which Δ_y spans from the quiescent point (i.e. $\Delta_{y0} = -1$), to simulate the actual shift in quiescent point due to current mismatch [26].

Fig. 21(a) compares both predictions for this nonlinearity, while Fig. 21(b) compares both predictions for a 10% mismatch with the same quiescent point. It can be seen that the noise floor, which appears at -17.6 dB/Hz and -17.3 dB/Hz, respectively, no longer concurs with Razavi’s predictions of -36.8 dB/Hz and -30.8 dB/Hz, respectively. We predict a noise floor at -19.3 dB/Hz with a 5% mismatch and -19.0 dB/Hz with a 10% mismatch, which, after application of the moving average filter, increase to -18.1 dB/Hz and



(a)



(b)

Fig. 21. Frequency spectrum of overall phase noise (modulation and nonlinearity noise) resulting from PWL nonlinearity corresponding to a charge pump mismatch of (a) 5% and (b) 10% and an offset of $y_0 = -1$, with the noise floor, spur and peak predictions shown.

-17.8 dB/Hz respectively—within half a dB of the simulated noise floor. We also correctly predict the amplitudes of the largest three spurs to within 2 dB.

C. Piecewise-Exponential Nonlinearity

The piecewise-linear nonlinearity considered above is an oversimplification of the effects of charge pump nonidealities. Firstly, the charges delivered are different in the presence of positive and negative signals, respectively. However, the PLL loop dynamics ensure that the positive and negative charges will balance out. This results in a phase error with non-zero mean, which moves the quiescent phase difference, ϕ_0 , away from the discontinuity [26].

Furthermore, not only will the charge delivered by each polarity be mismatched, but so will the timing. This results in shorter or longer pulses, which alters the total charge delivered by each side of the charge pump [15], [27]. The resulting

TABLE III

PLL PARAMETERS USED TO DERIVE NONLINEARITY SHOWN IN FIG. 23

f_{ref}	100 MHz	t_r^{up}	0.3 ns
N_{nom}	20	t_r^{dn}	0.2 ns
t_d	1 ns	t_f^{up}	0.2 ns
t_0	0.33 ns	t_f^{dn}	0.3 ns

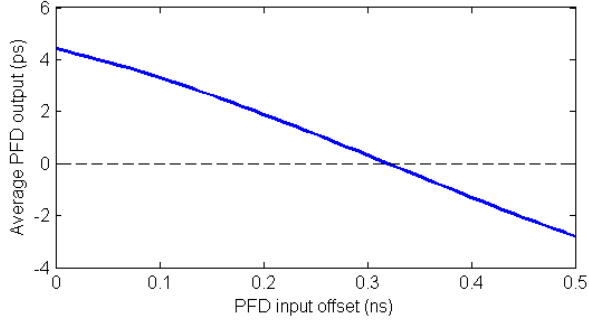


Fig. 22. Plot of average PFD output versus PFD input offset. A quiescent point is present at 0.33 ns.

nonlinearity will no longer be piecewise-linear, but piecewise-exponential.

Arora *et al.* offer an analysis of the dynamic behavior of the charge pump [27]. From this analysis, they have derived a prediction for the excess charge pump current produced as a result of mismatched charge pump timing delays. We have adapted their prediction to produce an expression for the corresponding nonlinearity, in units of time:

$$\begin{aligned} & \left(1 - e^{-(t_k - t_d)/t_r^{\text{up}}}\right) \left(t_f^{\text{up}} - t_r^{\text{up}}\right) \\ & - \left(1 - e^{-t_d/t_r^{\text{dn}}}\right) \left(t_f^{\text{dn}} - t_r^{\text{dn}}\right), \quad t_k \geq 0, \end{aligned} \quad (23)$$

$$\begin{aligned} & \left(1 - e^{-t_d/t_r^{\text{up}}}\right) \left(t_f^{\text{up}} - t_r^{\text{up}}\right) \\ & - \left(1 - e^{-(|t_k| - t_d)/t_r^{\text{dn}}}\right) \left(t_f^{\text{dn}} - t_r^{\text{dn}}\right), \quad t_k < 0, \end{aligned} \quad (24)$$

where t_r^{up} and t_f^{up} are the rise and fall times, respectively, of the “up” charge pump; t_r^{dn} and t_f^{dn} are the rise and fall times, respectively, of the “down” charge pump; t_d is the grouped propagation delay of the PFD; and t_k is the measured time offset between clock edges at the input of the PFD.

We study the example described in Table III, where we have applied the simplification that $t_r^{\text{up}} = t_f^{\text{dn}}$ and $t_r^{\text{dn}} = t_f^{\text{up}}$. The quiescent point, t_0 , was found numerically by applying the PDF of Δ_y to the PLL transfer function (given by $t + \mathcal{N}(t)$, where $\mathcal{N}(t)$ is the nonlinearity described by Eqs. (23) and (24)) and integrating the result to determine the average PFD output, shown in Fig. 22. It was found that the average PFD output reduced to 0, signifying steady-state operation, at an offset of $t_0 = 0.33$ ns. The corresponding nonlinearity is shown in Fig. 23.

The *PNN*, shown in Fig. 24(a), has a very sharp peak resulting from the discontinuous derivative in the nonlinearity. Its spectrum therefore contains a large number of harmonics, as can be seen in the prediction and corresponding simulated spectrum in Fig. 24(b).

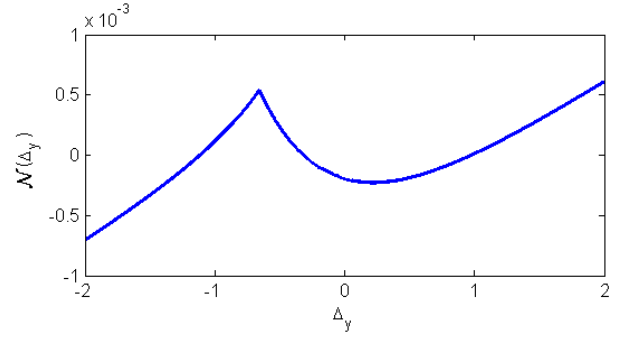
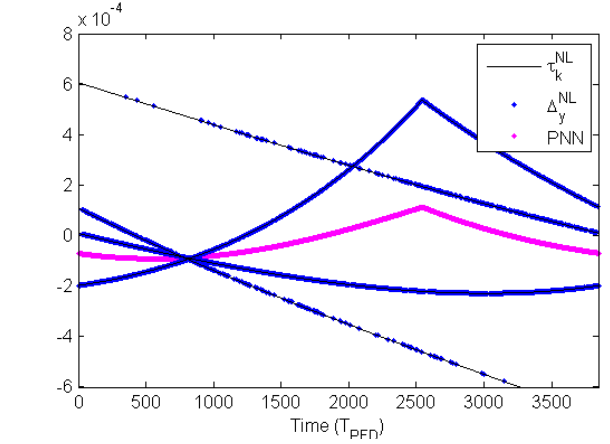
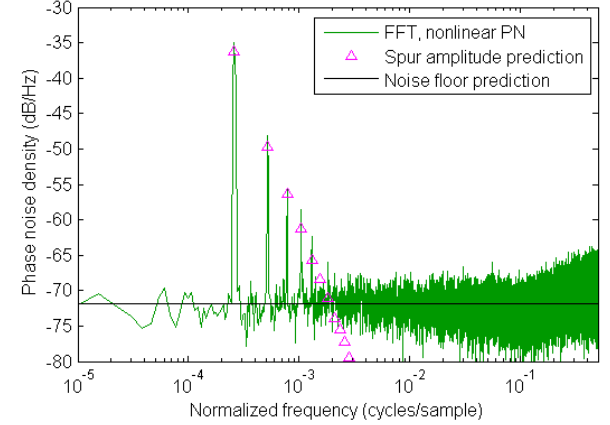


Fig. 23. A piecewise-exponential nonlinearity.



(a)



(b)

Fig. 24. Nonlinearity noise and *PNN* (a) and spectrum (b) of a simulation incorporating the piecewise-exponential nonlinearity in Fig. 23. Predictions for additional spurs are shown to account for the increase in the number of IBS spurs.

D. Simple Polynomial Nonlinearity

Both previous nonlinearities have been constructed by studying possible charge pump nonidealities. In practice, there are numerous other potential sources of nonlinearities in the loop, the combination of which will likely create a very complex transfer function. For this reason, it is instructive to consider the situation where charge pump mismatches do not dominate the loop transfer function.

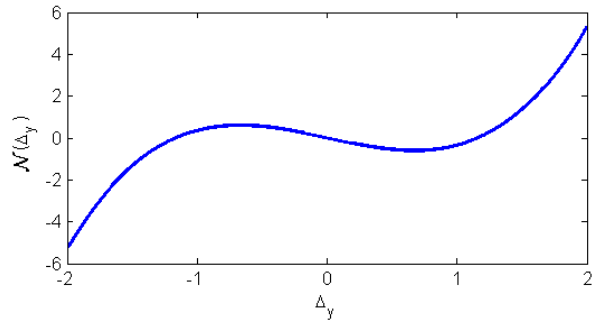
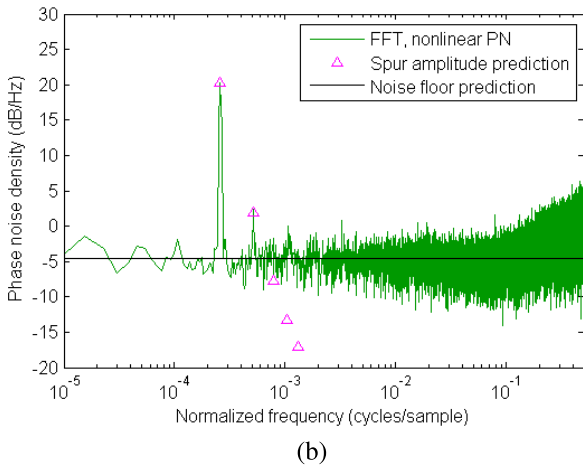
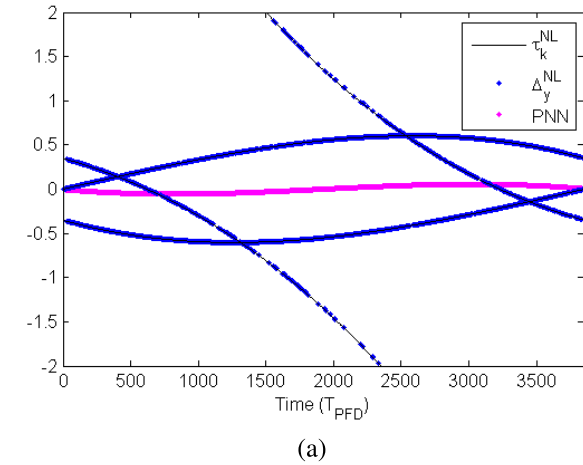


Fig. 25. A simple polynomial nonlinearity.


 Fig. 26. Nonlinearity noise and PNN (a) and spectrum (b) of a simulation incorporating the simple polynomial nonlinearity in Fig. 25.

To begin with, we will study the case where the nonlinearity is a simple polynomial function. Polynomial nonlinearities have previously been studied by Swaminathan *et al.* as a simplification of generalized nonlinearities [5]. The nonlinearity we will consider, shown after the removal of the linear component in Fig. 25, is $\mathcal{N}(\Delta_y) = \Delta_y^3$.

Since this is a relatively strong nonlinearity, the nonlinearity noise shown in Fig. 26 is much higher than in previous examples, and the spur amplitude and noise floor predictions match this. There is a small offset between the prediction and the simulation, which likely stems from inaccurate linearization

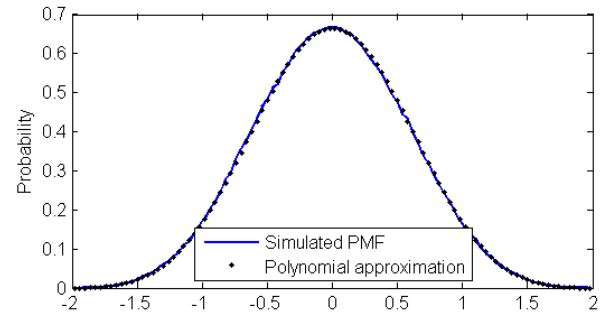
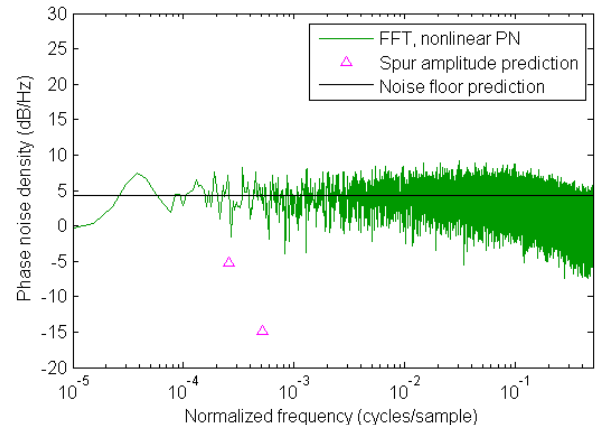


Fig. 27. PDF of the Successive Requantizer's accumulated output, and polynomial fit.


 Fig. 28. Spectrum of a simulation using Swaminathan *et al.*'s Successive Requantizer and incorporating the simple polynomial nonlinearity in Fig. 25. "Spur-free" operation can be observed.

of the nonlinearity, as some of the modulation noise is still present at higher frequencies.

E. Successive Requantizer

Swaminathan *et al.* and Familiar *et al.* have presented an alternative modulator, the *Successive Requantizer*, which is theoretically immune to polynomial nonlinearities of a given order [5], [6]. Consider the modulator described in [5],⁷ which is provably immune to polynomial nonlinearities of up to third order. The accumulated modulation noise PMF for this modulator can be approximated well by the following 12th-order polynomial, as shown in Fig. 27:

$$\begin{aligned} N(\Delta_y) \simeq & 0.0001\Delta_y^{12} - 0.0030\Delta_y^{10} + 0.0294\Delta_y^8 \\ & - 0.1557\Delta_y^6 + 0.4851\Delta_y^4 - 0.8537\Delta_y^2 + 0.6650. \end{aligned} \quad (25)$$

Fig. 28 shows the spur-free nonlinearity noise spectrum which results from the interaction of this modulation noise with the third-order nonlinearity. Spur-free operation has been achieved at the expense of an increased phase noise floor. The spur amplitude prediction correctly predicts that the spurs will be masked by the nonlinearity noise; the fact that the predicted

⁷Although Familiar and Galton have subsequently generalized the structure to higher orders [28], we will only study the first-order case here.

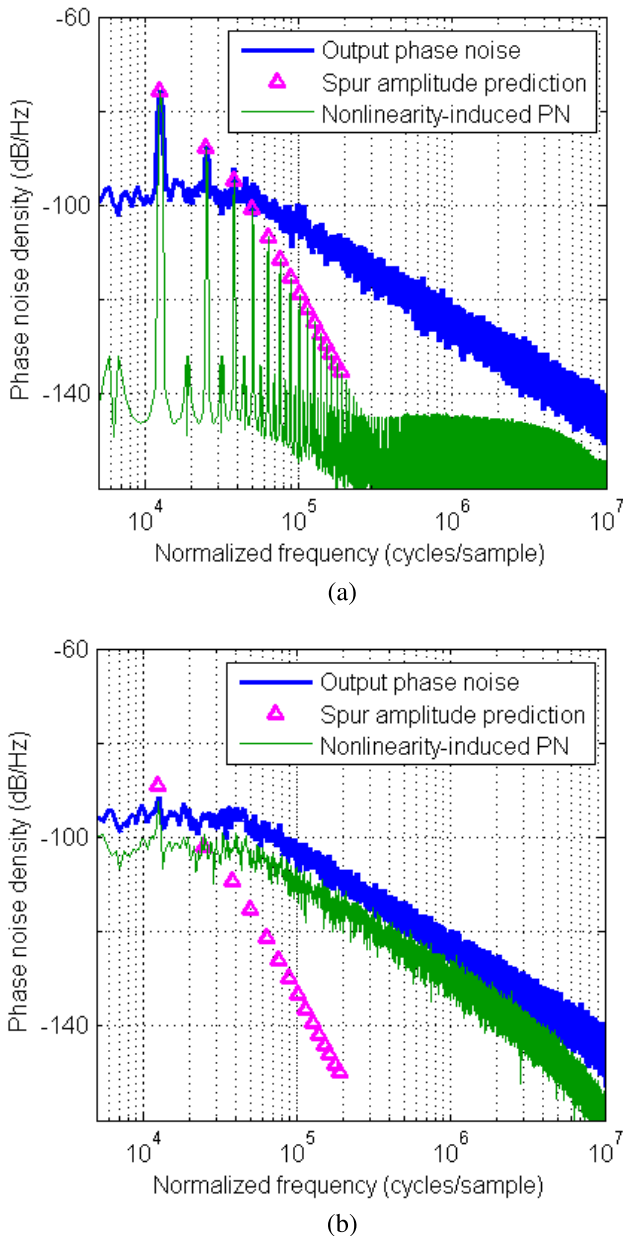


Fig. 29. Comparison of spur amplitude prediction and simulated output phase noise corresponding to the situation in [28, Fig. 9], using a (a) $\Sigma\Delta$ and (b) Successive Requantizer modulator. Both visible and hidden spur amplitudes are correctly predicted by the theory.

spur amplitudes are non-zero stems from the approximations mentioned at the start of this section.

It should be noted that for any modulator with a bounded accumulated output, $|\Delta_y| \leq A$, then for at least one p , $p \leq A$, the nonlinearity $\mathcal{N}(\Delta_y) = \Delta_y^p$ will produce spurs [29]. For this reason, while it is possible to approximate most practically encountered static nonlinearities with a polynomial of given order, the residual higher-order components will still produce spurs.

Familiar and Galton present output phase noise spectra of a simulated PLL with 1% charge pump mismatch employing a $\Sigma\Delta$ modulator and Successive Requantizer in [28, Fig. 9]. Fig. 29 shows a good agreement between the predicted and

simulated spur amplitudes. Our method accurately predicts spurs which are not visible in the output spectrum due to other noise sources, and demonstrates that all spurs are reduced in amplitude by the Successive Requantizer in this case.

V. CONCLUSION

In this paper, we have demonstrated how manipulation of the PLL loop nonlinearity, informed by the statistics of the modulation noise, can be used to derive predictions for the amplitudes of the spurs and the noise floor in the spectrum of the nonlinearity-induced noise. In doing so, we have demonstrated that the contribution of the nonlinearity to the output phase noise spectrum depends on the shape of the nonlinearity, the PMF of the modulation noise, and certain PLL parameters. Finally, we have verified, through simulation of a typical fractional- N synthesizer, that these predictions hold for a range of representative static nonlinearities.

The immediate application of the findings presented herein is that it demonstrates how the spectral behavior of a fractional- N PLL with a given nonlinearity and modulator design may be evaluated in a manner which allows separate calculation of the spurs and noise floor.

From a broader point of view, by redefining the modulation and nonlinearity noise in terms of a stochastic process which can be mapped to a pattern of tracks which is repeated periodically in time, we offer a new perspective into the contribution of loop nonlinearities to the phase noise spectrum. This perspective should both offer insight into the generation of phase noise and inform the design of novel PLL architectures and spur mitigation strategies.

APPENDIX

SPUR PREDICTION WITH LARGER VALUES OF x

The method presented in this paper assumes that the input to the modulator, x , is very small or very close to the modulator modulus: $|x| \ll M$. This appendix shows how the method can be extended to other modulator inputs which also produce in-band spurs.

In general, in-band spurs will occur when x approaches a rational multiple of the modulus. Their behavior can be determined by first expressing x in the following format:

$$x = \frac{aM}{b} + \bar{d} \quad a, b \in \mathbb{Z}, (a, b) \text{ coprime} \quad (26)$$

Using the above formulation, in-band spurs will occur when $|\bar{d}| \ll M$ for any a and b . These spurs will typically only be visible when b is small.

The example studied in the body of this paper, $|x| \ll M$, represents a special case corresponding to $b = 1$. As outlined in Section III-B above, in this special case, where the modulation noise Δ_y is bounded by $|\Delta_y| < A$, each sample of Δ_y lies on one of $2A$ distinct tracks.

In general, each sample of Δ_y lies on one of at most $2Ab$ tracks, where the minimum track separation is given by $1/b$. This results in the alternate formulation of Eq. (10),

$$\tau_k(t) = \frac{k}{b} - t \frac{x}{M}. \quad (27)$$

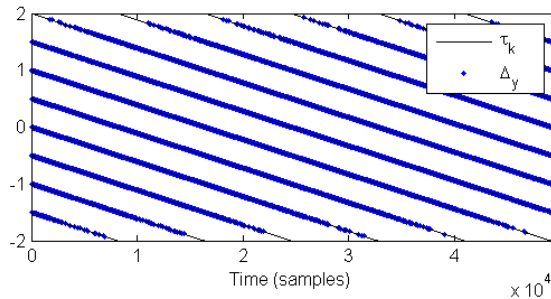


Fig. 30. Modulation noise tracks, τ_k (black) and simulated modulation noise (blue), showing reduced track spacing (0.5) and increased number of tracks (8).

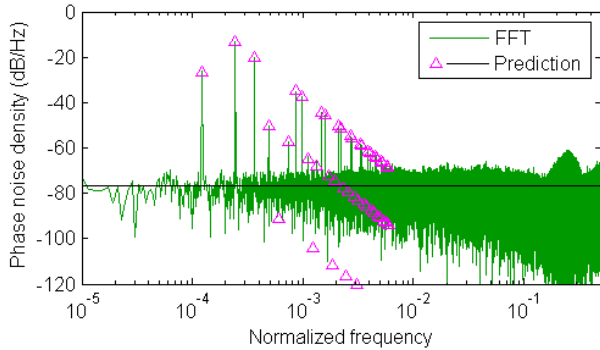


Fig. 31. Frequency spectrum of the nonlinearity noise, compared to spur predictions, demonstrating the application of the method to larger values of x producing in-band spurs.

Note that, as the number of tracks has increased and the spacing between tracks has been reduced, $k \in \{j - A + 1/b, j - A + 2/b, \dots, j + A - 1/b, j + A\}$ and Eq. (11) will now apply to *rational* values of k .

The spur prediction method can then be carried out as before, using a modified form of Eq. (17):

$$PNN[m] = \sum_{q=-Ab+1}^{+Ab} \tau_{q/b}^{NL}(m) P(\tau_{q/b}(m)), \quad (28)$$

and applying Eqs. (19) and (20), as before.

Fig. 30 shows the τ_k tracks for $x = 32772$, which corresponds to $a = 1$, $b = 2$ and $\bar{d} = 4$. There are 8 tracks, each separated by $1/2$ and described by Eq. (27). The resulting spur prediction, in the presence of the nonlinearity shown in Fig. 9, is illustrated in Fig. 31, demonstrating a good match between theory and simulation.

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REFERENCES

[1] B. Miller and B. Conley, "A multiple modulator fractional divider," in *Proc. 44th Annu. Symp. Freq. Control*, May 1990, pp. 559–568.

[2] T. A. D. Riley, M. A. Copeland, and T. A. Kwasniewski, "Delta-sigma modulation in fractional-N frequency synthesis," *IEEE J. Solid-State Circuits*, vol. 28, no. 5, pp. 553–559, May 1993.

[3] S. B. Sleiman, J. G. Atallah, S. Rodriguez, A. Rusu, and M. Ismail, "Optimal $\Sigma\Delta$ modulator architectures for fractional-N frequency synthesis," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 2, pp. 194–200, Feb. 2010.

[4] S. B. Sleiman and M. Ismail, "Multimode reconfigurable digital $\Sigma\Delta$ modulator architecture for fractional-N PLLs," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 57, no. 8, pp. 592–596, Aug. 2010.

[5] A. Swaminathan, A. Panigada, E. Masry, and I. Galton, "A digital requantizer with shaped requantization noise that remains well behaved after nonlinear distortion," *IEEE Trans. Signal Process.*, vol. 55, no. 11, pp. 5382–5394, Nov. 2007.

[6] E. Familier, C. Venerus, and I. Galton, "A class of quantizers with DC-free quantization noise and optimal immunity to nonlinearity-induced spurious tones," *IEEE Trans. Signal Process.*, vol. 61, no. 17, pp. 4270–4283, Sep. 2013.

[7] S. E. Meninger and M. H. Perrott, "A 1-MHz bandwidth 3.6-GHz 0.18- μm CMOS fractional-N synthesizer utilizing a hybrid PFD/DAC structure for reduced broadband phase noise," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 966–980, Apr. 2006.

[8] M. P. Kennedy, "Recent advances in the analysis, design and optimization of digital delta-sigma modulators," *Nonlinear Theory Its Appl.*, vol. 3, no. 3, pp. 258–286, Jul. 2012.

[9] B. De Muer and M. Steyaert, "A CMOS monolithic $\Delta\Sigma$ -controlled fractional-N frequency synthesizer for DCS-1800," *IEEE J. Solid-State Circuits*, vol. 37, no. 7, pp. 835–844, Jul. 2002.

[10] P. V. Brennan, H. Wang, D. Jiang, and P. M. Radmore, "A new mechanism producing discrete spurious components in fractional-N frequency synthesizers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 5, pp. 1279–1288, Jun. 2008.

[11] W. Rhee and A. Ali, "An on-chip phase compensation technique in fractional-N frequency synthesis," in *Proc. IEEE Int. Symp. Circuits Syst. VLSI (ISCAS)*, vol. 3, Jul. 1999, pp. 363–366.

[12] L. Zhang, X. Yu, Y. Sun, W. Rhee, D. Wang, Z. Wang, and H. Chen, "A hybrid spur compensation technique for finite-modulo fractional-N phase-locked loops," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2008, pp. 417–420.

[13] L. Zhang, X. Yu, Y. Sun, W. Rhee, D. Wang, Z. Wang, and H. Chen, "A hybrid spur compensation technique for finite-modulo fractional-N phase-locked loops," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 2922–2934, Nov. 2009.

[14] A. L. Lacaita, S. Levantino, and C. Samori, *Integrated Frequency Synthesizers for Wireless Systems*. Cambridge, U.K.: Cambridge Univ. Press, 2007, ch. 9–4, pp. 224–229.

[15] F. Bizzarri, A. M. Brambilla, and S. Callegari, "On the mechanisms governing spurious tone injection in fractional PLLs," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 64, no. 11, pp. 1267–1271, Nov. 2017.

[16] M. Perrott, M. Trott, and C. Sodini, "A modeling approach for $\Sigma\Delta$ fractional-N frequency synthesizers allowing straightforward noise analysis," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1028–1038, Aug. 2002.

[17] W. Chou and R. M. Gray, "Dithering and its effects on sigma-delta and multistage sigma-delta modulation," *IEEE Trans. Inf. Theory*, vol. 37, no. 3, pp. 500–513, May 1991.

[18] S. Pamarti and I. Galton, "LSB dithering in MASH delta-sigma D/A converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 4, pp. 779–790, Apr. 2007.

[19] V. R. Gonzalez-Diaz, M. A. Garcia-Andrade, G. E. Flores-Verdad, and F. Maloberti, "Efficient dithering in MASH sigma-delta modulators for fractional frequency synthesizers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 9, pp. 2394–2403, Sep. 2010.

[20] H. Mo and M. P. Kennedy, "Masked dithering of MASH digital delta-sigma modulators with constant inputs using multiple linear feedback shift registers," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 64, no. 6, pp. 1390–1399, Jun. 2017.

[21] D. Bannerjee, *PLL Performance, Simulation, and Design*. Indianapolis, IN, USA: Dog Ear, 2006.

[22] M. Cassia, P. Shah, and E. Bruun, "Analytical model and behavioral simulation approach for a Sigma-Delta fractional N synthesizer employing a sample-and-hold element," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 11, pp. 850–859, Nov. 2003.

- [23] H. Mo and M. P. Kennedy, "Influence of initial conditions on the fundamental periods of LFSR-dithered MASH digital delta-sigma modulators with constant inputs," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 64, no. 4, pp. 372–376, Apr. 2017.
- [24] E. Temporiti, G. Albasini, I. Bietti, R. Castello, and M. Colombo, "A 700-kHz bandwidth $\Sigma \Delta$ fractional synthesizer with spurs compensation and linearization techniques for WCDMA applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1446–1454, Sep. 2004.
- [25] B. Razavi, "An alternative analysis of noise folding in fractional-N synthesizers," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2018, pp. 1–4.
- [26] V. Sadeghi, H. Naimi, and M. Kennedy, "The role of charge pump mismatch in the generation of integer boundary spurs in fractional-N frequency synthesizers: Why worse can be better," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 60, no. 12, pp. 862–866, Dec. 2013.
- [27] H. Arora, N. Klemmer, J. C. Morizio, and P. D. Wolf, "Enhanced phase noise modeling of fractional-N frequency synthesizers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 2, pp. 379–395, Feb. 2005.
- [28] E. Familier and I. Galton, "Second and third-order noise shaping digital quantizers for low phase noise and nonlinearity-induced spurious tones in fractional-N PLLs," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 63, no. 6, pp. 836–847, Jun. 2016.
- [29] E. Familier and I. Galton, "A fundamental limitation of DC-free quantization noise with respect to nonlinearity-induced spurious tones," *IEEE Trans. Signal Process.*, vol. 61, no. 16, pp. 4172–4180, Aug. 2013.



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