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Multi-micron silicon photonics platform for highly manufacturable and versatile photonic integrated circuits

Aaron J. Zilkie, *Member, IEEE*, Pradeep Srinivasan, Andrea Trita, Thomas Schrans, *Member, IEEE*, Guomin Yu, *Member, IEEE*, Jerry Byrd, David A. Nelson, Karl Muth, Damiana Lerosé, Mazin Alalusi, *Member, IEEE*, Kevin Masuda, Melissa Ziebell, Hooman Abediasl, John Drake, Gerald Miller, Henri Nykanen, Evie Kho, Yangyang Liu, Hong Liang, Hua Yang, Frank Peters, *Member, IEEE*, Amit Nagra, and Andrew G. Rickman, *Member, IEEE*

Abstract—We describe and characterize a multi-micron silicon photonics platform that has been designed to combine performance, power efficiency, manufacturability and versatility for integrated photonic applications ranging from data communications to sensors. We outline the attributes needed for broad applicability, high-volume manufacturing, and large-scale deployment of silicon photonics, and describe how the platform is favorable with respect to these attributes. We present demonstrations of key technologies needed for the communications and sensing applications, including low-loss fiber attach, compact low-loss filters, efficient hybrid wavelength division multiplexed lasers, and high-speed electro-absorption modulators and integrated photodetectors.

Index Terms—Photonic integrated circuits, Integrated optics, silicon photonics, photonic integration, optical interconnects, optoelectronics, hybrid lasers, III-V hybrid integration

I. INTRODUCTION

SILICON photonics is now widely regarded as the key technology to bring planarized photonic integrated circuits to a wide range of photonic applications ranging from cost- and power-efficient optical transceivers, co-packaging of optics with high-speed ASICs, and compact sensing and 3D imaging solutions [1, 2, 3].

Over the past two decades, and in particular in the last few years, a multitude of silicon photonic companies have emerged, each having differences in their approach to making commercial products in silicon photonics and having waveguide heights ranging from 220 nm up to 4 μm [4–19]. But no one company has yet demonstrated large-scale deployment of silicon photonic integrated circuits across many applications achieving the large economies of scale similar to those attained

by Application Specific Integrated Circuits (ASICs) in microelectronics. Even in the communications market space alone, silicon photonics has yet to displace the established III-V-semiconductor micro-optic-packaged technologies [20].

Why hasn't silicon photonics yet realized the expectations of rapid growth across a wide range of applications? To scale up, silicon photonics still has to prove it is better in terms of device assembly process and manufacturing yields over conventional optical solutions while maintaining good or better performance and delivering on the promise of high levels of integration and significant size and cost reduction.

We suggest that a silicon photonics solution that achieves the goals of broad applicability and large-scale deployment should have all of the following attributes:

1. High-yield wafer processing with low device sensitivity to process variations
2. Integration of a large number of components
3. High integration densities
4. Low optical losses
5. Polarization independence
6. Efficient integration of III-V materials
7. Broad (> 300 nm) operating wavelength range
8. High power handling
9. High-speed, compact, and low-power modulator and detector technologies and interface electronics for ≥ 200 Gb/s/mm data throughput densities
10. Low-loss (≤ 1 dB) fiber coupling with simple high-yield high-throughput fiber assembly

The majority of Si photonics platforms today use a top silicon guide layer height of less than or equal to 0.3 μm [4–16, 21, 22] with the main established foundries converging on 220 nm. The choice of this waveguide dimension is mainly because of i) a push to have waveguides that cut-off higher order modes to

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A. J. Zilkie, P. Srinivasan, A. Trita, T. Schrans, G. Yu, J. Byrd, M. Alalusi, M. Ziebell, G. Miller, K. Masuda, H. Liang, D. Lerosé, H. Abediasl, and A. Nagra, are with Rockley Photonics, Inc, Pasadena CA 91104 USA (email: aaron.zilkie@rockleyphotonics.com).

H. Nykanen and E. Kho are with Rockley Photonics Oy, Espoo, Finland.

H. Yang is with Rockley Photonics Ireland Ltd, Cork, Ireland.

Frank Peters is with Rockley Photonics Ireland, Cork, Ireland and also with the Physics Department, University College Cork, Cork, Ireland and the Integrated Photonics Group, Tyndall National Institute, Cork, Ireland.

J. Drake is with Rockley Photonics Ltd, Newport, Wales, UK.

A. G. Rickman is with Rockley Photonics Ltd, Oxford, England, UK.

achieve “pure” single-mode behavior, ii) the perceived importance of using existing capital-intensive CMOS foundry infrastructures (which can not process multi-micron Si topographies), and iii) a reliance on Si pn-junction Mach-Zehnder structures or ring-resonators for high-speed modulators [1]. However, unlike CMOS electronics, losses do not go down in a photonics circuit when the size of the waveguide is shrunk. Indeed, it is somewhat the opposite: beyond a certain size, the losses go up in a photonic waveguide if the size is reduced. Multi-micron waveguides have losses 2-10 times lower than sub-micron waveguides [23, 24, 23, 25]. Also filter reproducibility and repeatability significantly drop for sub-micron photonics waveguides, because of a much larger effective index sensitivity at these dimensions. Furthermore, sub-micron silicon photonics platforms cannot achieve polarization dependence simultaneously with acceptable fabrication tolerances [21] [26], whereas multi-micron waveguides can. Lastly, as predicted in [27], it has proven to be challenging to this day to achieve low-loss (~ 1 dB or less) coupling from a 220 nm waveguide to standard single-mode fiber with a mode ~ 50 times larger, as state-of-the-art out-of-plane grating couplers are achieving at best 1.5-2.5 dB coupling loss to SMF fiber and also suffer from polarization dependence and limited optical bandwidth [7, 4, 6, 5]. Good progress has recently been made with broader-band polarization independent losses in the 1.5-2.0 dB range coupling from sub-micron waveguides directly to SMF fiber in commercial platforms using edge-coupling with sub-wavelength gratings and/or multi-level silicon nitride [28, 29, 30, 31], but the processes are somewhat complex and requiring small feature sizes in the lithography.

In this paper we will describe and demonstrate the Rockley Photonics multi-micron silicon photonics platform which is favorable for combining all of these attributes. It is therefore an attractive platform for realizing large-scale integrated and planarized photonics technologies for a wide range of applications and high-volume manufacturing.

II. MULTI-MICRON PLATFORM DESCRIPTION

A. Single-mode behavior

The multi-micron silicon-on-insulator (SOI) rib-waveguide that maintains mono-mode operation is based on the principles described in a seminal paper by Soref, Schmidtchen, and Petermann in 1991 [27]. The generic rib-waveguide cross-section in our platform and the basic parameter definitions are shown in Fig. 1. In our platform the height of the top silicon guide layer $h = 2b\lambda$ is chosen to be $\geq 1 \mu\text{m}$. The main advantages gained by using this multi-micron waveguide size is simultaneous achievement of polarization independence, low-loss coupling to standard single mode fiber (SMF) and III-V actives, very low propagation losses, and high tolerance to fabrication variations.

As discussed in [27] it is a misconception that a height less than $0.3 \mu\text{m}$ is required to have a single-mode rib waveguide. Indeed in [27] it is explained that for “large” silicon guide layer

thicknesses, higher order vertical modes do not propagate as long as $r > 0.5$ because they will leak into slab modes. Fig. 2 shows eigenmode expansion (EME) simulations (performed in Lumerical MODE solutions) of light propagation down a waveguide with $h = w = 3 \mu\text{m}$ and $e = 0.6h$ over a distance of $2000 \mu\text{m}$, excited by a circular fiber mode with $3 \mu\text{m}$ spot size, offset from the waveguide mode center by $1 \mu\text{m}$ in both the horizontal and vertical directions, for light at a wavelength of 1300 nm (as in [27]). This shows that, even though higher order modes exist immediately after off-center excitation, as the light propagates these modes leak into unguided slab modes and eventually only the fundamental mode propagates. Comparing the propagation in the $3 \mu\text{m}$ height to the $4 \mu\text{m}$ simulated in [27] we see that the $3 \mu\text{m}$ height waveguide is more tolerant to off-center excitation and less coupling to higher order slab modes occurs. It should be noted that losing light to slab modes would normally be undesirable as it would represent power loss from the waveguide, so it is also important to take care to only excite the fundamental mode when coupling into waveguides of this size to ensure power-efficient operation.

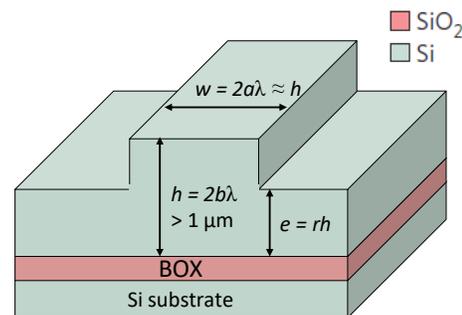


Fig. 1. Cross-section of the multi-micron SOI waveguide structures used in this paper. Parameter definitions follow those in [27].

B. Polarization independence

In this platform, to achieve polarization independence, the ratio of the rib width to silicon layer height simply needs to be chosen to be close to or greater than unity ($a/b \geq 1$ so that $w/h \approx 1$) to ensure the TE and TM fundamental modes have similar effective index values. The waveguide rib is formed by etching Si outside the rib area to a depth $e = rh$. Parameters a , b and r are as defined in [27]. Fig. 3 a) and b) show simulated TE and TM mode profiles for a waveguide with $h = w = 3 \mu\text{m}$ and $e = 0.6h$.

The mode profiles are indistinguishable from each other indicating near polarization degeneracy. Fig. 3 c) and d) show the mode size and shapes for a typical 220 nm sub-micron waveguide on the same scale as a) and b) for comparison. These modes are clearly highly polarization dependent, with the TM mode being cut-off and existing in the cladding layer. The small size of the modes in the 220 nm height waveguides in c) and d) compared to the multi-micron mode size in a) and b) also illustrates the magnitude of the size difference that must be overcome to couple to an SMF fiber mode, which is still significantly larger than the modes in a) and b).

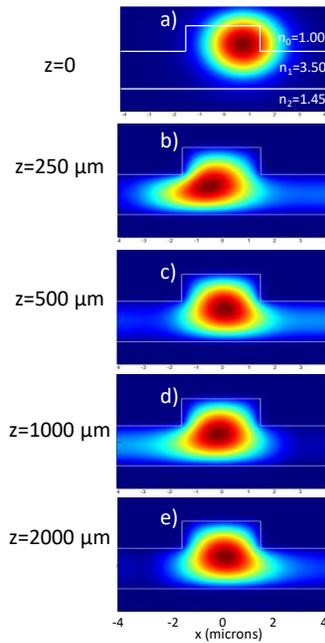


Fig. 2. (a-e) 2D mode profiles at varying propagation distances z after a $3 \mu\text{m}$ diameter circular excitation at a wavelength of 1300 nm off-center by $1 \mu\text{m}$ in both horizontal and vertical directions for rib waveguide height and width of $3 \mu\text{m}$, $e=0.6h$. $n = 3.5$ is used for the material index of bulk Si at 1300 nm .

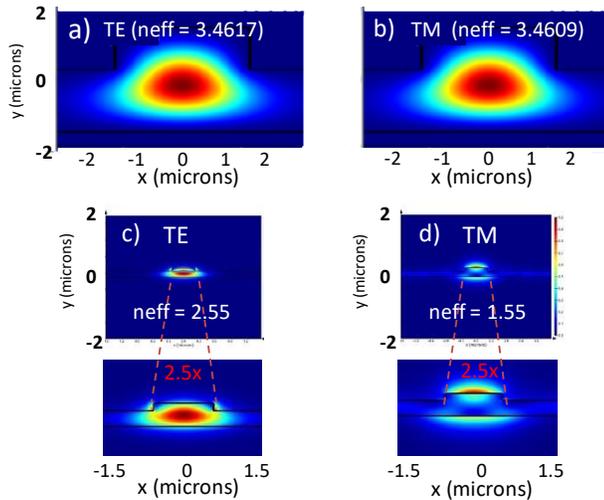


Fig. 3. a) TE and b) TM Mode shapes and effective indices in our multi-micron rib waveguide at a wavelength of 1550 nm ($h = w = 3 \mu\text{m}$, $r = 0.6$); c) TE and d) TM mode shapes for the common 220 nm height waveguide platform for comparison ($h = 220 \text{ nm}$, $w = 450 \text{ nm}$, $r = 0.6$).

C. Euler bends for tight bend radii

Another misconception associated with a multi-micron bend radius is that the bend radii need to be large to enable low loss bends and avoid mode leakage. However tight bend radii with bend losses comparable to those readily achieved in standard sub-micron platforms can be readily achieved in the multi-micron platform by converting to strip or wire waveguides ($r < 0.15$) for some portions in the circuit where a bend is needed and narrowing the waveguide width [32, 23]. Rib-to-strip converters have similarly been used in sub-micron waveguides to combine low-loss rib waveguides with tight bends [33]. In [32, 23] Cherchi *et al.* have reported Euler bend effective radii

as low as $1.3 \mu\text{m}$ with losses of 0.09 dB per 180° bend in a $4 \mu\text{m}$ waveguide platform, and lower losses of 0.02 dB per bend with larger bend radii. Larger bend radii can be chosen to minimize losses if ultra-tight bends are not needed. Fig. 4 shows transmission measurements of Euler bend test structures in our $3 \mu\text{m}$ height strip waveguides consisting of varying numbers of Euler L-bends with effective bend radius $R_{\text{eff}} = 86 \mu\text{m}$. The measurements show an average 0.018 dB per 90° bend for TE polarization and $< 0.01 \text{ dB}$ for TM polarization over full C-band wavelengths with little to no wavelength dependence confirming the excellent practicality of these bends for use in low-loss high density photonic integrated circuits in the multi-micron platform. Smaller bend radii can also be used if needed with a penalty of slightly higher losses [23].

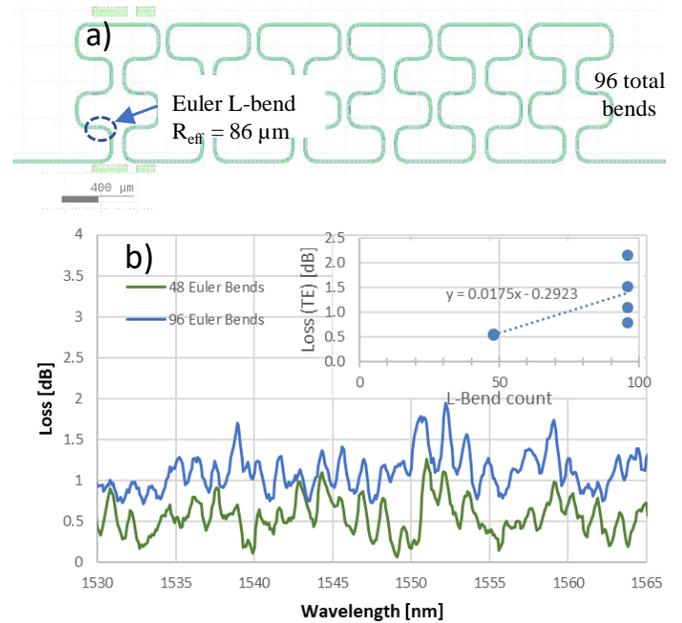


Fig. 4. a) Euler bend test circuit mask layout, and b) loss spectra and average transmission loss versus bend count (inset) of Euler bend test structures with 48 and 96 Euler bends in our $3 \mu\text{m}$ waveguides ($h=3 \mu\text{m}$). In the Euler bends the waveguide width was reduced to $w=1.5 \mu\text{m}$. Two chips from two different wafers were measured, each chip having one structure with 48 bends and two with 96 for a total of 6 data points.

D. Low propagation loss

Low propagation losses are critical in particular when making photonic integrated circuits integrating multiple components and functions together, which is a key need for making photonic integrated circuits applicable to a large range of applications, and to achieve high volumes. Many critical photonic elements involve lengthy passive regions and have performance benefits associated with low waveguide losses, for example arrayed-waveguide grating (AWG) filters [34], higher order tapped-delay-line filters and cascaded Mach-Zehnder filter arrays [35, 36, 37], and optical phased arrays [3]. Resonant devices requiring high quality factors and low roundtrip losses, such as ring-resonator filters and narrow linewidth external cavity lasers also have a critical dependence on loss. Many silicon photonics applications involve the use of these

components, and in some cases scaling to larger circuit sizes or scaling of the performance for future applications and use cases require pushing the losses as low as possible. The multi-micron waveguide platform is the platform of choice for lowest propagation losses in silicon. As propagation losses are dominated by the electromagnetic field scattering from side-wall roughness, decreasing modal overlap with the waveguide sidewalls leads to lowering of propagation losses. Larger waveguides lead to higher confinement and less field overlap with waveguide side walls. As seen in Fig. 2, both TE and TM modes are highly confined in a waveguide with $h = w = 3 \mu\text{m}$, as is evident by the mode effective index being very close to the refractive index of bulk silicon ($n_{\text{Si}} = 3.476$). For the sub-micron platforms the much lower effective indices of $n_{\text{effTE}} \approx 2.4$ indicates a much weaker confinement and intrinsically higher overlap with waveguide sidewalls.

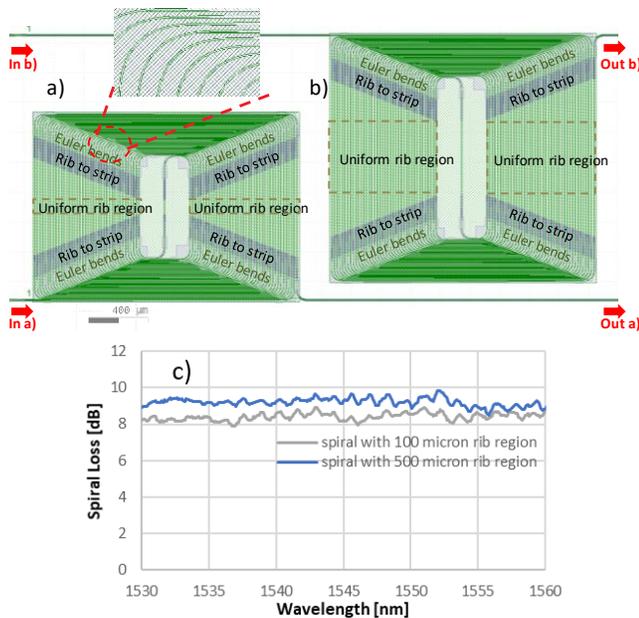


Fig. 5. a) 40-loop Spiral with and Euler bends and 100 μm long rib waveguides in the uniform rib region. b) 40-loop Spiral with and Euler bends and 500 μm rib waveguides in the uniform rib region, equivalent to 3.2 cm longer rib waveguide length; c) measured spiral loss spectra over C-band wavelengths.

Fig. 5 shows results of characterizations of waveguide spirals to assess losses of the rib waveguides, rib-to-strip converters, and strip waveguides necessary to combine low-loss waveguides with tight-radius Euler bends. The spirals have 40 loops with each loop having two regions of rib waveguides, four 150- μm -long rib-to-strip converters to convert to two strip waveguide regions and four Euler bend regions to make tight bends with $R_{\text{eff}} = 86 \mu\text{m}$ on each corner. Two spirals that have identical designs with only different lengths in the low-loss rib regions, the second spiral having 800 μm additional length of rib waveguide in each loop, are measured. The difference in losses between the two loops allows for an accurate measurement of the rib-waveguide loss. An additional spiral having only strip waveguides and Euler bends, with no rib waveguide regions and no rib-to-strip convertors, is used to determine the loss of the strip waveguide, by subtracting the

TABLE 1
LOSSES OF PASSIVE WAVEGUIDE BUILDING BLOCKS

Quantity	Value	Unit
Rib waveguide loss	0.18	dB / cm
Tight Bend loss	0.01	dB per 90° bend
Strip waveguide loss	0.31	dB / cm
Rib-to-strip convertor loss	0.01	dB

Euler bend loss for 160 bends using the known bend loss value determined in section C. Once the rib and strip waveguide losses are determined, the rib-to-strip convertor losses can approximately be determined by subtracting these losses from the total waveguide loss and dividing by the number of convertors.

The losses of the various passive building blocks in our platform are summarized in TABLE 1.

E. High power handling

The capacity of a photonic integrated circuit waveguide to handle high powers is an important topic not often discussed. For some PIC applications such as LiDAR, high output power translates to longer imaging ranges and faster frame rates, and high power handling in these applications can be important for PICs to compete against current free-space optics solutions, or to enable performance scaling for future needs and applications.

Silicon has a significant two-photon absorption (TPA) coefficient, and therefore silicon has non-linear absorption (i.e. absorption dependent on power per unit area in the waveguide) which results in self-heating which can limit the performance of silicon photonic integrated circuits in the presence of high power levels in the waveguide. This non-linear two-photon absorption leads to field-intensity-dependent free carrier generation, which not only causes absorption of light but also causes self-heating and a change in the phase of propagation by changing the refractive index.

According to [38, 39, 40], for a waveguide having effective mode area \bar{a} and material TPA absorption coefficient β_T , the absorption in a silicon waveguide in the presence of two-photon absorption is given by $\alpha = \alpha_s + \alpha_2 I^{(3)}$ where α_s is the linear absorption due to waveguide scattering, α_2 is the non-linear absorption coefficient and is related to β_T according to $\beta_T = \alpha_2 \hbar \omega_0 v_g$, and $I^{(3)}$ is the nonlinear intensity in the waveguide. In [38] the TPA coefficient was measured in a 4- μm -high silicon waveguide and has the value $\beta_T = 0.45 \text{ cm/GW}$ at a wavelength of 1550 nm. Using this simple formalism, we can calculate the field intensities at which the TPA-induced loss $\exp(-\alpha_2 I^{(3)})$ results in significant absorption as a function of different waveguide effective mode areas \bar{a} . For the 2 cm long chip in [38] which has $\bar{a} = 6.2 \mu\text{m}^2$ the input peak power threshold for a 1 dB TPA-induced loss is 18 W. For a 2 cm long chip in a 3 μm height platform which has $\bar{a} = 3.5 \mu\text{m}^2$ this corresponds to 10W, and in a 220 nm height platform ($\bar{a} \approx 0.1 \mu\text{m}^2$) the same threshold is 300 mW. Thus the 1-dB TPA loss threshold is 30 times lower for a 220 nm height waveguide, due a mode area that is 30 times smaller than in a 3 μm height waveguide. In LiDAR applications for example, high constant-wave powers above 100 mW are desired and the onset of TPA

at these power levels in sub-micron waveguides begins to degrade efficient laser operation.

F. Low phase errors and wavelength variations

Interferometric or resonant devices perform basic critical functions in photonic integrated circuits, such as filtering, modulation, beam steering (in optical phased arrays), and creating laser cavities. These devices rely on precise control of optical phase, and phase is determined by the refractive index seen by the light propagating of the waveguide, and the length of the propagation distance. Length can be precisely controlled in the patterning process during optical lithography, but the effective refractive index is determined not only by the dielectric constants of the materials inside and surrounding the waveguide, but more importantly the shape of the waveguide. In photonic integrated circuits, waveguide shape non-uniformities across a wafer translate to phase and therefore optical path length non-uniformities, which translate to variations in free-spectral ranges and therefore filter center wavelengths for filters and resonator-based modulators, lasing wavelengths for lasers, and loss of coherence in optical phased arrays.

Similar to scattering loss as discussed in section D, the higher the confinement of the light in the waveguide, the less sensitive it is to waveguide shape variations. Simulated and measured values of refractive index change and wavelength change due to percentage changes in waveguide height, width, and etch depth are given in TABLE 2. In our analysis we find it convenient to represent in % both index and wavelength changes due to relative waveguide dimension changes. Following from [21], waveguides in the 220 nm platform on 200 mm wafer sizes using 193 nm lithography, a $\pm 1.5\%$ change is representative of typical 3σ width variations, and $\pm 2.5\%$ is typical for 3σ height variations. Our results in this paper are based on work on 150 mm wafer sizes using 365 nm i-line lithography, and, conveniently, we find that our 3σ variations in width and height in our $h = w = 3 \mu\text{m}$ waveguides expressed in % are approximately the same as those mentioned above for the 220 nm platform in 193 nm lithography. Etch depth variations for these etch depths can range from $\pm 2.5\%$ to $\pm 5\%$, and in this analysis we assume they are $\pm 2.5\%$ (as above). Modelling of the effective index variations shows a 20-40x lower change in effective index in a $3 \mu\text{m}$ waveguide compared with that in the 220 nm waveguide, and there is a corresponding reduction in center wavelength variations in optical filters in the $3 \mu\text{m}$ waveguide platform. This result is confirmed by comparing measurements of the variation of AWG filters with 200 GHz and 400 GHz channel spacings around 1550 nm made in our platform to center wavelength variations of filters with similar channel spacings and operating wavelengths reported

from foundries running 220 nm waveguide processes. We find a $25\times$ lower 3σ wavelength variation of 0.3 nm amongst AWGs in our platform across multiple wafers and multiple sites per wafer, whereas a value of 7.8 nm 3σ variations for filters in the 220 nm platform has been reported [22]. Fig. 6 plots the simulated index changes and associated wavelength changes versus waveguide platform height, where the 220 nm height point corresponds to the standard $h = 220\text{nm}$ $w = 450 \text{ nm}$ waveguide dimension. The dotted line shows a curve fit to the data points and reveals the dependence of index sensitivity roughly fits a $x^{-1.5}$ relationship, verifying that there is a rapid increase in the index sensitivity and wavelength variability when the waveguide height goes below $1 \mu\text{m}$ assuming the waveguide width is $\leq 2h$. It should be noted that, as in [22], variability in filters can be compensated for by adding active tuning circuits that use for example thermal phase shifters but this adds significant complexity, additional electrical circuits and drives up the number of electrical interfaces to the photonics PIC.

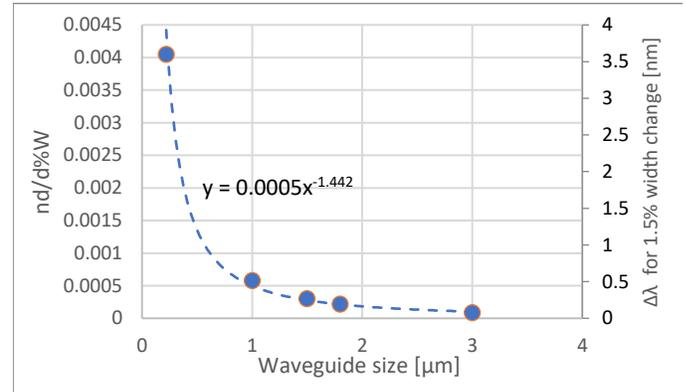


Fig. 6. Simulated change in effective index per percent change in waveguide width, and associated wavelength change for 1.5% change in waveguide width, as a function of waveguide width. Waveguide height of 220 nm assumes waveguide width of 450 nm.

G. III-V integration

A critical capability needed for versatile silicon photonics PICs is III-V integration. Lasers cannot efficiently be made in Si, and III-V semiconductor laser diodes provide the most efficient light sources. Existing III-V waveguide devices such as lasers and modulators optimized for performance and power efficiency naturally have a multi-micron mode size, thus power-efficient integration of III-V components is fundamentally well suited to our multi-micron platform. Various techniques for integration of III-V actives to Si photonic waveguides have been demonstrated, with the techniques generally falling into two categories, i) bonding unprocessed III-V materials placed above the Si waveguide with evanescent coupling between the

TABLE 2
COMPARISON OF VARIATIONS OF WAVEGUIDE DIMENSIONS AND WAVELENGTH VARIATIONS IN FILTERS IN THE DIFFERENT SI PHOTONIC PLATFORMS

Structure	$dn/d\% \Delta w$ (simulated)	$\Delta\lambda(\Delta w=1.5\%)$ [nm] (simulated)	$dn/d\% \Delta h$ (simulated)	$\Delta\lambda(\Delta h=2.5\%)$ [nm] (simulated)	$dn/d\% \Delta e$ (simulated)	$\Delta\lambda(\Delta e=2.5\%)$ [nm] (simulated)	$\Delta\lambda$ [nm] Measured (3σ)
3 μm rib ($h = w = 3 \mu\text{m}$, $r > 0.5$)	9.0E-05	0.06	2.5E-04	0.28	6.0E-05	0.07	0.3
3 μm strip ($h = w = 3 \mu\text{m}$)	1.8E-04	0.12	1.80E-04	0.12			
220 nm rib	3.9E-03	3.56	5.00E-03	7.61	3.0E-03	4.57	7.8 ^a

Values are for TE only and are all 3σ values consistent with [21]. Values for $3 \mu\text{m}$ waveguides are for 150 mm wafers and 365 nm i-line lithography.

^aFrom [22]

Si waveguide and III-V waveguide, and ii) attaching processed III-V devices in a recess in the Si waveguide layer and performing edge coupling.

The edge coupling scheme in the multi-micron silicon waveguide platform provides multiple advantages for high volume silicon photonic integrated circuits, namely i) direct compact coupling between III-V and Si (no evanescent tapers or spot-size converters needed), ii) active III-V device processing in existing III-V foundries, iii) ‘back-end’ integration of known good and reliable III-V devices (tested before integration), and iv) more favorable thermals owing to a direct thermal path to the Si substrate since the recess can be etched through the BOX layer. Manufacturable hybrid external-cavity lasers with good performance and narrow line-widths can be realized in the multi-micron platform by using a simple III-V flip-chip bonding process [41, 18].

Fig. 7 plots the coupling efficiency between a standard III-V multiple-quantum-well (MQW) device waveguide and a multi-micron silicon photonic waveguide with height ranging from $h = 1 \mu\text{m}$ to $h = 3 \mu\text{m}$ and width $w = 3 \mu\text{m}$. The coupling losses range from 0.2 – 2 dB for heights ranging from 1 to 3 μm , respectively, for waveguides as-is (without any mode conversion), and from 0.2-0.3 dB when a local spot-size converter is added to the SOI or III-V waveguide to optimize the mode height at the coupling interface, assuming ideal placement accuracy of the III-V element. Fig. 6 and Fig. 7 together show that efficient III-V coupling, compactness, and high manufacturing tolerances can be achieved simultaneously for any desired application by using multi-micron silicon waveguide heights in the 1 to 3 μm range. High performance hybrid integrated lasers and modulators made in this way in 3 μm waveguide heights are described further in section III.C and III.D.

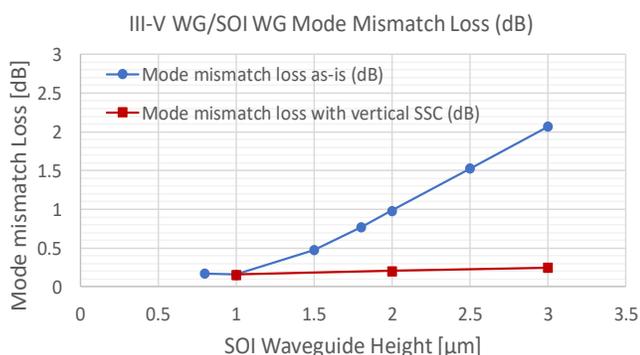


Fig. 7 Coupling loss between standard III-V active device waveguide and silicon waveguide with varying silicon waveguide height and fixed width $w = 3 \mu\text{m}$ (circles), and with local vertical spot-size convertor added to optimize height at coupling interface (squares), assuming ideal alignment.

III. PLATFORM TECHNOLOGIES

A. Fiber Attach

Many current and future applications of silicon photonics PICs involve interfacing to standard single-mode optical fiber (SMF). For these PICs to be used in high-volume applications, the attach to SMF must be simple, low loss, and the attach assembly process must be low-cost and easy to perform, ideally

without lengthy active alignment steps. The multi-micron platform is naturally well-suited to meet these requirements as the mode size in the waveguide is within one order of magnitude of the mode size in SMF fiber. Because of this a single-stage spot size convertor can be used to expand the mode to a $13 \times 13 \mu\text{m}$ large waveguide and facilitate mode-matching to SMF fiber. Anisotropic wet-etched V-grooves can also be formed in the silicon substrate at the ends of the expanded waveguides [24] to facilitate passive alignment of SMF fiber to the $13 \times 13 \mu\text{m}$ waveguide end. Since the angle of the V-groove is defined by the crystal planes of the silicon, the depth of the V-groove can be precisely controlled to lithographic tolerances by optimizing the V-groove width. When a stripped SMF fiber is placed in the V-groove, the center of the SMF fiber mode is aligned to the center of the $13 \times 13 \mu\text{m}$ waveguide mode. The theoretical coupling loss between the mode of the SMF fiber and the $13 \times 13 \mu\text{m}$ waveguide is only 0.15 dB, and when combined with the loss of the spot-size converter and additional loss tolerance for fiber dimension and V-groove etch variabilities, the theoretical loss of the fiber attach chain in high volume production can be < 1 dB per interface for both TE and TM polarizations.

We fabricated spot-size convertor (SSC) test chips that have $h = w = 13 \mu\text{m}$ high waveguides aligned to deep-etch V-grooves on either end of the chip coupled to a $h = w = 3 \mu\text{m}$ high waveguide in between using two single-adiabatic taper spot-size convertors which transition the mode between the two waveguide sizes. The chip schematic is shown in Fig. 8 a). An SEM picture of the V-groove structure is shown in Fig. 8 b). Fig. 8 c) shows the measured fiber-to-fiber optical transmission through the SSC chip, with the fiber coupling optimized. The measured total fiber-to-fiber loss is 1.8 dB, corresponding to 0.9 dB coupling per fiber interface.

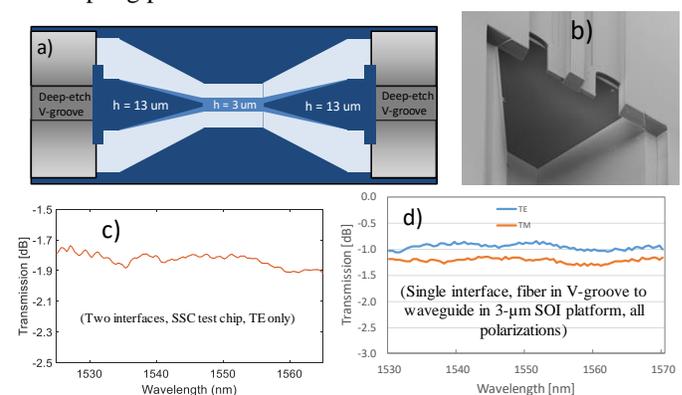


Fig. 8 a) Schematic of spot-size-convertor chip which converts $13 \times 13 \mu\text{m}$ waveguides aligned to deep-etched V-grooves at the edges to a $3 \times 3 \mu\text{m}$ waveguide in the middle; b) SEM picture of a fabricated V-groove aligned with a $13 \times 13 \mu\text{m}$ waveguide; c) measured fiber-to-fiber optical transmission spectrum of the chip over full C-band wavelengths (TE polarization only). d) measured fiber-to-waveguide optical transmission spectrum for buried SSC, TE and TM polarization. d) was measured as half the transmission through two SMF fibers placed passively in V-grooves coupled with on-chip buried SSCs to either end of a U-bend $w=h=3 \mu\text{m}$ rib waveguide.

The SSC chip in Fig. 8 was fabricated in a starting wafer having an $h = 13 \mu\text{m}$ top Si guide layer and etching down to the $h = 3 \mu\text{m}$ height to make the tapers. The spot size converters

and $13 \times 13 \mu\text{m}$ waveguides can also be inverted and integrated into an SOI wafer structure with $3\text{-}\mu\text{m}$ -high top Si layer, creating a buried SSC allowing for planar integration and seamless process integration with other elements in the platform, facilitating PICs with low-loss fiber attach structures at the chip edges and integrated with other platform elements as desired. We have achieved loss from passively aligned SMF fiber through buried SSCs to $w=h=3 \mu\text{m}$ waveguides in $3\text{-}\mu\text{m}$ SOI of nominally 1.1 dB with $\pm 0.2 \text{ dB}$ PDL as shown in Fig. 8 d).

B. AWG Filters

Filters are a key element for performing multiplexing and demultiplexing functions in PICs, for example for wavelength division multiplexing (WDM) in data communication systems or to make spectrometers, and are commonly implemented in silicon photonics using arrayed waveguide gratings (AWGs) [34, 24].

AWG filters are particularly well suited for the multi-micron silicon photonics platform. AWGs have been reported in thin (sub-micron) SOI platforms and have seen good performance and compact size [34], but they have not yet been deployed commercially because of the large sensitivity of the channel wavelengths to fabrication variations in this platform, and the large polarization dependence due to the large birefringence in these waveguides. The multi-micron SOI waveguides on the other hand have little to no birefringence, low phase errors due to waveguide fabrication variations, and low propagation loss as described in section II. For AWGs these properties enable high performance, high repeatability and high yields, even with relaxed manufacturing capabilities. Indeed, for these reasons AWGs in multi-micron SOI waveguides were deployed commercially already in the late 90s [24].

An historical issue with AWGs in a thick-silicon SOI platform is the fact that the bend radius of the waveguide is also large (typically few mms) and this results in a device with a large footprint, which is not compatible with the stringent size requirements of high-density optical I/O photonic chips. Also the lower waveguide dispersion in the multi-micron waveguides results in a further $\sim 2x$ relative increase in the waveguide array length compared to AWGs made in sub-micron waveguides. However, the use of the Euler bends discussed in section II.C now unlocks the possibility of still extremely compact and novel AWG layout schemes. **Error! Reference source not found.** shows rectangular-shaped AWGs implemented by using two 90-degree Euler bends on each waveguide in the waveguide array. Shallow-etched rib waveguides were used for the waveguides leading to the interface between the free-propagation-region and the waveguide array. Square deep etched slab waveguides were used to implement the actual delay sections in the array which have zero birefringence and allow polarization independent operation. In the Euler bend regions, the waveguide width was reduced to $1.5 \mu\text{m}$ to facilitate tight bend radii of $R_{\text{eff}} = 86$ as discussed in section II.C. Rib-to-strip converters were used inside the waveguide array to transition from one cross section to the other, and were optimized for minimal reflections and minimal excitation of higher order modes.

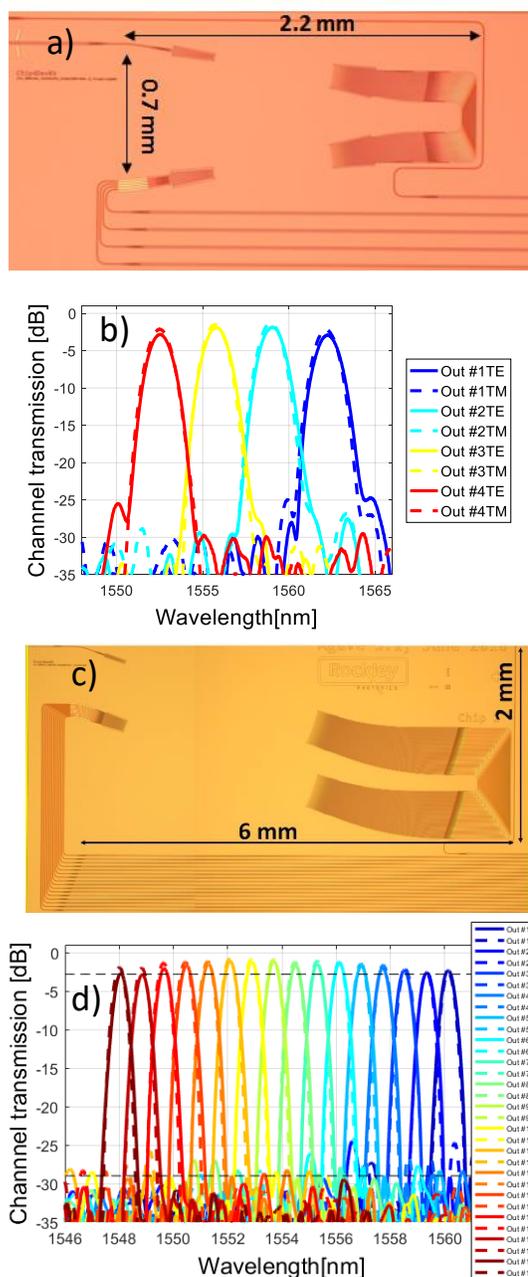


Fig. 9 Top-view chip micrographs a), c) and optical spectrum measurements b), d) for both TE and TM polarizations of Arrayed Waveguide Gratings (AWGs) fabricated in the Rockley Photonics multi-micron platform.

The devices in Fig. 9 were fabricated in SOI wafers having a $3 \mu\text{m}$ top Si guiding layer using an i-line wafer stepper (348 nm lithography linewidth) on 150 mm wafers. The devices were characterized using a broadband source in combination with an optical spectrum analyzer. Light was coupled directly to waveguides using a lensed optical fiber, and a polarization switch was used to control the input polarization state to both TE and TM states. Fig. 9 b) and d) show the spectral response for both polarizations of a 1×4 - 400GHz and 1×16 100GHz AWGs respectively. The losses are normalized to a reference straight waveguide measured with the same input and output lensed fibers to ensure equal coupling efficiencies to the devices and reference waveguides. The insertion loss across all

channels and both polarizations is < 3 dB. The crosstalk (defined as power from adjacent aggressor channel leaking into the center of the victim channel) is better than -25 dB across all channels for both polarization states. The polarization-dependent frequency shift (PDF) is below 10GHz and the PDL is below 0.5dB.

Thermal management of filters is also important in a silicon photonics platform as Si has a relatively large thermo-optic coefficient of $80 \text{ pm}/^\circ\text{C}$ and power-efficient thermo-optic phase shifters are desired. Thermal management and thermo-optic phase shifting can be performed by introducing localized heaters into the Si waveguides, and we have achieved efficient $\sim 1 \text{ mW}/\pi$ waveguide heaters with doped regions and undercuts similar to what has been shown in [42]. All-Si a-thermal AWGs with little/no channel wavelength drift versus temperature can also be made in our platform. Details of our efficient thermo-optic waveguide heater technologies and a-thermal AWGs will be published in future works.

Fig. 10 shows the AWG channel registration measured across multiple dies and wafers in a fabrication run. The wavelength variation is better than $\sigma = 0.1 \text{ nm}$. Waveguide variations are estimated to be $\Delta w_{3\sigma} = 54 \text{ nm}$, and height variations $\Delta h_{3\sigma} \pm 75 \text{ nm}$.

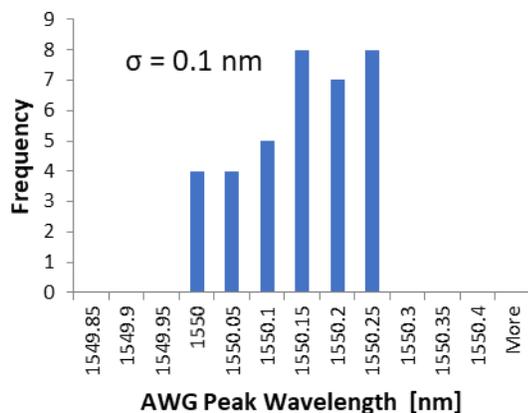


Fig. 10. AWG peak wavelengths for a single AWG design measured across multiple dies and 150 mm wafers.

C. Hybrid III-V lasers

As mentioned in section II.G we perform III-V integration using an edge coupling scheme to make hybrid lasers in our platform. Hybrid laser devices were made by fabricating InP-based RSOAs and DFB lasers in a standard III-V foundry and integrating them into $h = 3 \mu\text{m}$ silicon rib waveguides using well known flip-chip integration methodologies (see e.g. [18]) but using modern solder processes and commercial die-bonder tools with high alignment accuracy.

External cavity lasers were made with the RSOAs coupled to DBR gratings etched in the silicon rib waveguide, and a wall plug efficiency of 15% and output power exceeding 50 mW at 25°C was achieved, as shown in Fig. 11 a) through c). Anti-reflection coatings (composed of single-layer silicon nitride films) and angled waveguides at the output facets were used on both the Si and III-V sides to suppress facet reflections. Such lasers can have very narrow linewidths due to the fact that the hybrid edge-coupling scheme provides the ability to decouple the length of the gain region from the passive region in the

cavity, and therefore a significant portion of the cavity length can be composed of our low-loss silicon waveguides. Results from a linewidth measurement on one of our external cavity DBR lasers is shown in Fig. 11 d). Linewidths of $< 40 \text{ kHz}$ are obtained. Fig. 11 e) shows the spectrum of a 4-channel WDM laser PIC created with hybrid integration of an RSOA with an array of 4 waveguides coupled to an array of 4 waveguides having gratings of different pitches. An SEM micrograph of a similar 8-ch WDM laser PIC is shown in Fig. 11 b).

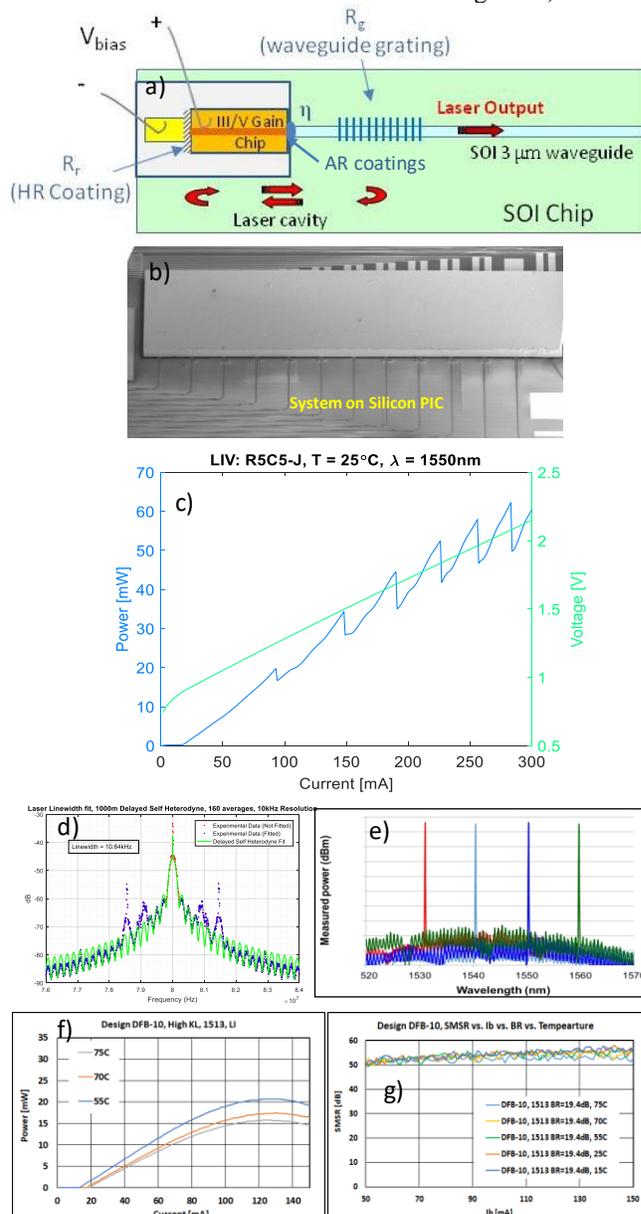


Fig. 11 Schematic drawing a), SEM micrograph b), and performance measurements c)-g) of our silicon photonic hybrid laser platform;

The performance of hybrid DFB structures fabricated in the platform is shown in Fig. 11 f) and g). Output powers greater than 15 mW over a full chip temperature range of $25^\circ\text{C} - 75^\circ\text{C}$ are obtained. These lasers have an SMSR > 50 dB and are tolerant to -20 dB of return loss at the laser facet. Tolerance to back-reflection at these levels is a key attribute for commercial silicon photonic lasers as the lasers need to maintain performance in the presence of multiple sources of scattering

and back reflection on the silicon chip and from the external link beyond the transmitter chip.

Owing to this hybrid scheme, our silicon photonic laser platform is capable of integration of III-V dies of different designs or material systems on the same PIC. By combining with multi-cavity wafer scale integration techniques, we can make many-channel laser PICs covering a broad range of wavelengths for ultra-broadband applications.

D. High speed modulators and detectors

III-V integration on silicon is a key technology enabler for silicon photonics. Several techniques have been used for integration of III-V on silicon for lasers and EAMs on sub-micron waveguide platforms. These typically require specialized processing techniques to be developed in a silicon fab and involve removal of large areas of the III-V material resulting in high costs. We have developed 1310 nm electro-absorption modulators fabricated in standard III-V foundries with excellent performance over temperature at 25Gbaud, and with performance that can scale to higher speeds for future generations, which are hybrid flip-chip integrated into the Si waveguides in the same way as the RSOAs and lasers as described in section C. The performance of these devices is shown in Fig. 12. The figure shows open eye-diagrams at 25C and 75C with low TDECQ penalties for 25 Gb/s NRZ and 50 Gb/s PAM-4 modulation. The DC extinction ratio of the devices show broadband performance at O-band wavelengths. Our EAM platform is also capable of good performance at 50 Gb/s NRZ and 100 Gb/s PAM-4 modulation rates, details of which will be published in future works.

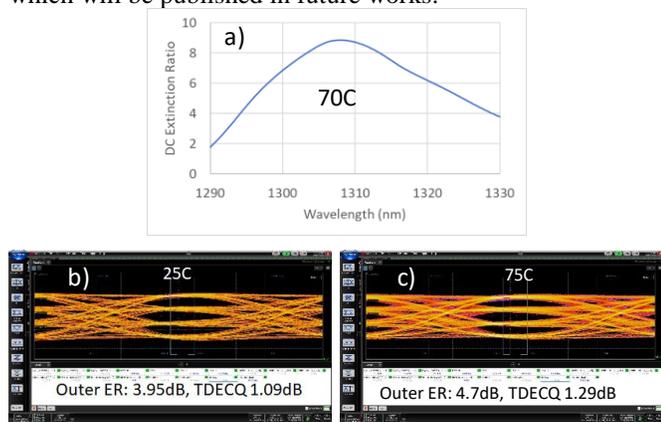


Fig. 12 a) DC Extinction ratio at 70C versus wavelength for our III-V EAMs with 2V peak-to-peak drive swing. EAM eye-diagram with 50 Gb/s PAM-4 signaling at b) 25C and c) 75C.

Polarization independent and broadband germanium waveguide photodetectors (PDs) were realized with monolithic Ge diode waveguides having monolithic integration of 3- μ m-thick Ge epitaxially grown inside our w=h=3 μ m Si waveguides. The performance of our Ge PDs is shown in Fig. 13. The devices show S21 bandwidths in excess of 40 GHz, sufficient for detection of 50 Gb/s PAM-4 signals, and high responsivities of >1 A/W and >0.85 A/W in the C-band and O-bands respectively. High-speed monolithic Ge PDs with similar performance in multi-micron SOI waveguides have been reported previously in [25].

PMD electronics for our high speed EAM and PDs are described in [2].

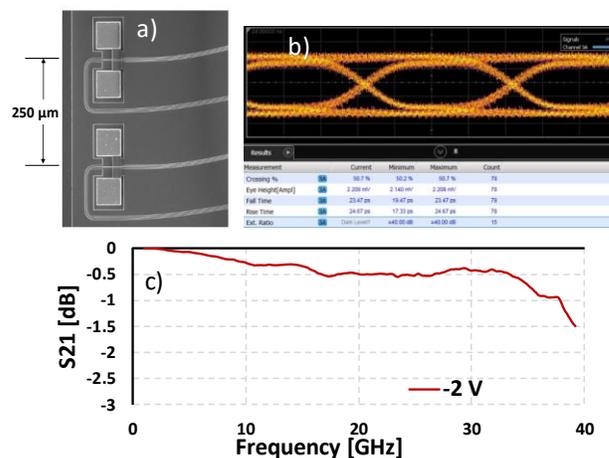


Fig. 13 a) SEM micrograph of Ge PDs PIC, with PDs integrated on a 250 μ m pitch with the help of Euler bends. b) eye diagram and c) S21 plot measured on one PD at 25 Gb/s at -2V bias.

IV. APPLICATIONS

Silicon-photonic PICs incorporating high-data-rate modulators and detectors can revolutionize optical I/O solutions for datacenters by co-packaging high-density I/O PICs with switch ASICs [2]. In these optoASIC applications there is a need for high (>200) Gb/s/mm integration densities in the PICs to allow edge integration with the ASIC. This drives the need for silicon photonics modulators and detectors that can be integrated with pitches of ≤ 300 μ m, data rates of 50 Gb/s per wavelength, integrating an increasing number of components per chip. Moreover, to be viable for this application the high speed modulators and detectors must have the ability to scale to smaller integration densities and high data rates that are needed to keep pace with the generational throughput increases of the switch ASICs. Our compact III-V-based EAM modulators and monolithic Ge PDs are well suited for these requirements, and transceiver Tx and Rx PICs made in our platform have sizes < 30 mm², planar fiber attach included, comparable to or smaller than most transceiver PICs made in sub-micron silicon photonics platforms.

Our multi-micron silicon photonics platform also has advantages for sensing applications and in particular 3D imaging and LiDAR. First, these applications can require large transmitted optical powers of at least +30 dBm in a single output waveguide, due to the $1/R^2$ dependence of the power received at a detector placed at a distance R up to a few hundred meters from the target, as well as fast steerable narrow beams to provide high spatial resolution at fast frame rates [3]. The much higher power handling capability of the multi-micron platform discussed in section II.E enables higher performance LiDAR systems that have longer range and/or higher received powers enabling faster frame rates. We have measured over 2 W of peak optical power handling without observable TPA saturation in our platform. Second, to achieve a large number of diffraction limited sampling spots with an optical phased array (OPA), a large number of single emitters is needed on a tight pitch for a large field of view. Placing single emitters on a

tight pitch requires very good confinement in the emitting silicon waveguides so that the emitters do not couple to each other. As the multi-micron waveguide platform has a mode with very high confinement for waveguide widths down to 0.5 μm , the platform is ideally suited for tight pitch emitters. Combined with the high manufacturing yields and reduced phase errors, this means large emitting arrays with wide field of view and shorter calibration times can be produced with good manufacturability. Third, to scan a far field with a large number of sampling points at a large frame rate, fast steering of an OPA is needed, with a steering speed $< 1\mu\text{s}$ per sample point desired. While thermo-optic phase shifters are commonly used to implement beam steering in many OPAs [43, 3], they are not fast enough for many applications. Fast phase shifters based on silicon p-i-n or p-n waveguide diodes, or more exotic materials, should ideally be used to achieve fast phase-based steering. Silicon p-i-n or p-n waveguide diodes capable of 1 to 10s of ns response time, lengths in the range 0.5-5 mm, and V_{π} L efficiencies (for p-n diodes) similar to sub-micron-waveguide high-speed phase modulators can also be made in the large waveguide platform. Fourth, the waveguides and fiber couplers have large optical bandwidth of operation, providing the capability to operate over a wide range of wavelengths. Finally, on the receive side, the platform is well suited to implement coherent receivers for Frequency-Modulated Continuous Wave (FMCW) LiDAR. Coherent receiver PICs can easily be made with 2x2 MMIs to mix the signal with the local oscillator and integrated waveguide photodiodes. The inherent polarization independence of the circuit will allow the receiver performance to be independent of the polarization state coming from the target. In addition, the wide wavelength range supported by the waveguides makes our platform very well suited for other sensing applications such as wideband spectroscopy.

V. CONCLUSION

We have described and characterized a multi-micron-size silicon photonic integrated circuit platform that has been designed to provide the maximum combination of performance, power efficiency, manufacturability and versatility. This has been achieved by developing a silicon photonics process that is separate from and unconstrained by CMOS processes. Instead, it has been optimized for photonic circuit performance and manufacturability. Specifically, compared to conventional sub-micron waveguide platform integrated circuits, our platform has 2-10 times lower waveguide losses, 25 times less variability of performance due to equivalent percent changes in waveguide dimensions, polarization independence for the key technology elements, and a monolithic fiber attach technology which has < 1 dB insertion loss and is ultra-broad-band.

Using this platform we have demonstrated i) compact AWGs up to 16 channels with insertion losses < 3 dB across all channels and polarizations and very low channel center wavelength variability, ii) hybrid DBR and DFB lasers providing high output powers of 15–50 mW, wall plug efficiencies of 15% at 25C, narrow linewidths of < 40 kHz, and WDM capability, and iii) high speed EAM modulators and Ge detectors that are compact, power efficient, and have good

performance for 50 Gb/s PAM-4 data modulation and detection.

The platform and demonstrated technologies pave the way for the deployment of planar photonic integrated circuits across a diverse range of applications ranging from data communications to sensors. This enables integrated photonics to begin to leverage the economies of scale for high volume manufacturing, which has been key to the success of the microelectronics industry.

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ALL BIOS ARE REQUIRED



Aaron J. Zilkie (S'99, M'08) (S'97) received his M.A.Sc. and Ph.D. degrees in electrical and computer engineering from the University of Toronto, Toronto, Canada in 2004 and 2008 respectively, and a B.Sc. degree in electrical engineering from the University of Manitoba, Winnipeg, Manitoba, Canada in 2001.

Aaron is Co-founder and VP of R&D at Rockley Photonics where he currently leads silicon photonics R&D developing next next-generation products and solutions for the company. Aaron has 15 years of

experience in research and development, IP development, and product development in optical datacom, optical communications, and photonics. Prior to Rockley Photonics he has held roles at Kotura Inc. where he developed the silicon photonic hybrid lasers and QSFP optical transceivers, and at Oclaro Technology Inc. and Nortel Networks where he developed optical communications system components and subsystem products. He has over 40 granted patents and patent applications, has authored or co-authored multiple journal articles in the field of photonics, and has presented at numerous international photonics and optical communications conferences.

Pradeep Srinivasan received his Ph.D. in Optics and Photonics from University of Central Florida, Orlando, FL, U.S.A. where he developed high power lasers and nanostructured all-dielectric metamaterials.

Pradeep is the Director of the silicon photonics development team at Rockley Photonics leading PIC development across multiple product verticals in datacom and sensor applications. Prior to Rockley, he was part of the pioneering team that launched Intel Corporation's first silicon photonics products.

Andrea Trita received his Ph.D. degree in electrical engineering from the University of Pavia, Italy, in 2009, where he worked on semiconductor lasers and nonlinear optics using silicon photonic waveguides.

Andrea joined Rockley Photonics in 2014. From 2011 to 2014, Andrea was with the Photonics Research Group of Ghent University, an associated lab of imec, as a Post-Doctoral Researcher working on integrated silicon photonic FBG interrogators. His current research interests include WDM components in silicon photonics.



Thomas Schrans has an MS in Electrical Engineering from the University of Gent, Belgium, and both an MS and PhD in Electrical Engineering from the California Institute of Technology, Pasadena, CA.

Thomas has been active in the fiberoptic and optical interconnect industry for over 25 years, most recently at Rockley Photonics Inc. which he joined in 2014 as Director of Product Development, spear-heading in package optics. Since December of 2017 he holds the position of Director of Advanced Technology where he leads the technology development for next generation products. Prior to joining Rockley Photonics he was VP of Technology and Advanced Product Development and co-founder at Kaiam Corporation, a private company pioneering and commercializing hybrid photonics integrated circuits as multi-wavelength high speed fiber optic transceivers. He has held positions at IBM, Ortel Corporation, Lucent Technologies, Agere Systems, Encore, Optical Communications Products and Santur Corporation, where he managed the development of the pioneering 10x10Gb/s CFP for 100G Ethernet. He has been an active participant in various industry standards organizations (IEEE802.3) and MSAs, holds several patents and has multiple publications. He is a member of the IEEE and the OSA, has been a member of the OFC organizing committee since 2016 and is sub-committee chair for the OFC2019 Active Devices Committee, and he has been member of the organizing committee for the IEEE OI conference since 2018.

Guomin Yu became a Senior Member of IEEE in 2011 and received his M. Eng. degree in Engineering Physics from McMaster University, Hamilton, ON, Canada in 2001.

Guomin joined Rockley Photonics in 2014 and his current focus is on design and development of high speed photonics devices.

Jerry Byrd holds a BSEE from UCLA, Los Angeles, CA, U.S.A. Jerry joined Rockley Photonics in 2015 where he is Manager of Packaging Engineering. Prior to joining Rockley, Jerry served as the Director of Product Development at OEwaves where he led the product development of a photonic microwave

oscillator, and numerous other research projects. He also served as a Technical Manager, for Xponent Photonics where he led the development of a surface mount laser, and low-cost packaging for FTTx transceivers. He was also responsible for developing numerous FTTx transceiver reference designs to support customer evaluations.

Jerry has over 20 years in the photonics industry, with contributions in packaging, electrical design, test and project management.

David A. Nelson received his MSEE degree from UCLA, Los Angeles, CA, U.S.A. in 1978 and a BS degree in Physics from Brigham Young University in 1975.

David is currently the Director of Integrated Circuit Design at Rockley Photonics. Prior to that Mr. Nelson was Principal Engineer within the Silicon Photonics Group at Intel where he helped develop photonics and electronic integrated circuits for Intel's first 100G silicon photonic based fiber optic communication modules.

David was the founder and CEO of Comlinear Corporation which pioneered high data rate devices in the 1990's. Mr. Nelson is the holder of over twenty patents.

Karl Muth became a member of the IEEE and the IEEE-SA in '93 and '08 respectively. He received a Dipl.-Ing. degree in electrical engineering (telecommunications engineering) from the Technical University Darmstadt, Germany in 1991.

Karl is currently Director of Communication Technology at Rockley Photonics, Pasadena, CA and is leading the architecture and design of terabit opto-ASICs. During his industry career he has worked at Bosch, Marconi, Texas Instruments, and Intel on the design of wireless and optical transceivers and numerous chipsets for RF and high speed optical communications as well as industry standardization of optical communication interfaces.

Karl has co-authored 4 journal and conference papers and holds more than 10 patents in the fields of RF and high speed optical communication systems. He is a member of the Optical Society of America.

Damiana Lerose holds a Ph.D. in Physics from the Martin Luther University, in cooperation with the Max-Planck-Institute for Microstructure Physics, both in Halle, Germany. Her Ph.D. research focused on designing, fabricating, and characterizing thin-film solar cell prototypes based on patterned silicon nanowires p-doped by aluminum crystallization. Prior to that, for her M. Sc., she joined research activities in photonics at the University of Trento, Italy, and St. Andrews, Scotland, UK, which included the design, fabrication, and characterization of optical devices.

Damiana is at Rockley Photonics where she leads the team responsible for the manufacturing of silicon photonics chips, process development, mask tooling, and ramp-up to production volumes. Before joining Rockley Photonics, Damiana worked at Trioptics, California, as the R&D manager for optical metrology equipment. Her tasks also included customer support and tool qualification. Prior to that, she worked in X-FAB Semiconductor Foundries in Erfurt, Germany, leading a multi-disciplinary development team for integrating optical devices within the existing CMOS manufacturing line, from new prototypes to their transfer to production volume. She worked closely with customers, partners, and sub-contractors across Europe and Asia.

Damiana has filed two patents based on her work in hyperspectral optical filters and published the results in peer-reviewed journals.

Mazin Alalusi holds an MSEE from the University Washington and a BSEE degree from the University of Southern California, Los Angeles, CA, U.S.A.

Mazin joined Rockley Photonics in 2015 and is currently Principal Semiconductor Laser Engineer. Prior to joining Rockley, as Senior Design Engineer at Redfern Integrated Optics, Mazin led the design, development, and transfer to production of sub-kHz, ultra-low phase noise, shot noise limited, ultra-stable semiconductor laser DBRs in 14-pin butterfly.

Mazin has over 25 years of experience in Photonics RF Design and Integration, Test and Instrumentation and Modeling Tools. He has held technical engineering roles at K2 Optronics, Maple Optical Systems, OptiMight Communications, Xtera Communications, Pacific Fiberoptics, DSC Communications, and C-COR Electronics.

Kevin Masuda received his B.Sc. degree in electrical engineering from University of California Los Angeles, Los Angeles, CA, U.S.A. in 2009. He joined Rockley Photonics in 2015 and his current focus is III-V process and integration.

Melissa Ziebell received her Ph.D. from the University of Paris-Sud, Orsay, France and M.S degree in physics from Delft University of Technology, Delft,

The Netherlands and École Polytechnique/Institut d'Optique Graduate School, Palaiseau, France.

Melissa is currently a Senior High Speed Semiconductor Engineer at Rockley Photonics, where she is a PIC Lead for 100G Chipsets and TRX. Previously, Melissa was as a CNRS Post-Doctoral Researcher at Institut d'Optique Graduate School, Palaiseau, France, where she worked in the Agence nationale de recherche (ANR) Quantum Cryptography on Silicon project, to demonstrate theoretically and experimentally the possibility to integrate a proprietary technology for Quantum Key Distribution (QKD) on a silicon photonics chip.

Hooman Abediasl holds a Ph.D. from the University of Southern California, Los Angeles, CA, U.S.A., and B.S. and M.S. degrees in electrical engineering from Sharif University of Technology. During his PhD, he was focused on design and implementation of integrated complex electro-optical systems targeting optical sensing and imaging applications.

Hooman is at Rockley Photonics where he was first responsible for designing high-speed photonic devices, and now leads the development of optical sensor products at Rockley Photonics. He is responsible for commercialization of optical sensor chipsets targeting a range of markets including autonomous vehicles and healthcare.

Hooman is a pioneer in the field of integrated optical phased arrays (OPA) introducing two generations of the world's first monolithic OPAs in CMOS process. He has recently won the Nokia Bell Labs first prize 2016 for his PhD research.

John Drake received his B.Sc. degree in Applied Physics & Microelectronics from University of Northumbria in 1994 and MBA from University of Bath in 2002 in the UK.

John joined Rockley Photonics in 2015 and is focused on process development and integration for the fabrication of optical circuits. He has over 20 years' experience in the fields of micromachining and silicon photonics processing.

Gerald Miller received his Ph.D. in Applied Physics from the California Institute of Technology, Pasadena, CA, U.S.A. in 2012. Gerald joined Rockley Photonics in 2018 and is currently working on semiconductor laser design for silicon photonic applications.

Henri Nykänen received his M.Sc. from Helsinki University of Technology (HUT) in 2008 and D.Sc. from Aalto University in 2013.

Henri has worked at Aalto University/HUT between 2008-2013, main research topic being GaN based blue/UV LED technology with 15 publications. Later moving to private sector, he has worked with Rockley Photonics since 2015, with leading expertise on SiP wafer processing.

Evie Kho received B.Eng. (Hons) in electronics and computer engineering from University Malaysia Sarawak in 2004. She had her internship with Intel Microelectronics Malaysia in 2003 and after graduation, worked in X-Fab Sarawak as Process Development Engineer.

Evie joined Rockley Photonics in 2015. She is currently a Senior Process Engineer in the company, responsible for Silicon Photonic process development.

Yangyang Liu will receive her PhD in electrical engineering from University of Colorado, Boulder in 2018. She joined Rockley Photonics (Pasadena, CA) as a Photonics Design Engineer in Nov 2017, and has been primarily working on passive silicon photonic device design.

Hong Liang received the B.Sc. degree in physical optics from Shandong University, Jinan, China, in 1984.

Hong is currently the Principal Engineer, Photonics Test Lab Manager at Rockley Photonics, where she leads photonics test planning, development and execution. Previously, Hong was the Principal Engineer, R&D Test Lab Manager Mellanox where she was for the characterization of silicon photonics devices including optical modulators, photodetectors, grating couplers, integrated WDM transmitters, and receivers. Previously, she has served for The Institute of Physical and Chemical Research, Wako, Japan.

Hua Yang became a member of IEEE in 2018. He received his M.Sc. degree in material science from Wuhan University of Technology in 2003, and Ph.D. degree in optoelectronics from Institute of Semiconductors, CAS, in 2006.

Hua is now at Rockley Photonics working on silicon photonics. Prior to Rockley, he worked as a research fellow in Nanyang Technological University, Singapore from 2006 to 2008 then he joined Tyndall National Institute, Ireland,

as a senior staff researcher till 2018. He has been focusing on research and development of the III-V semiconductor devices and integrated circuits.



Frank H. Peters (M'96) was born in Victoria, B.C. Canada. In 1988 he completed a B.Eng. in engineering physics at the Technical University of Nova Scotia, Canada. In 1991 he completed a Ph.D. from McMaster University, Canada.

From 1991-1993, he worked as a Research Engineer in the Electrical and Computer Engineering Department at the University of California, Santa Barbara. From 1993 until 2001 he worked as a Research Scientist at Optical Concepts, W. L. Gore and Associates and Agilent Technologies developing and integrating photonic devices into datacom and telecom applications. From 2001-2005 Frank worked at Infinera in Sunnyvale California in the development of high speed photonic integrated circuits, and then moved to Ireland in 2005. He is a professor in the physics department at University College Cork, and the head of the Integrated Photonics group at the Tyndall National Institute. He has authored more than 200 papers and holds over 40 patents all concerned with thermal, optical, electrical and systems issues relating to the design and use of photonic devices and high speed photonic integrated circuits.

Amit S. Nagra received his Ph.D. degree in electrical engineering from the University of California at Santa Barbara in 1999. He has worked at Rockley Photonics in Pasadena (USA) since 2015 as the COO and is responsible for leading the Photonics development, Supply chain, and Operations teams.



Andrew Rickman, OBE, holds a mechanical engineering degree from Imperial College, London, a PhD in silicon photonics from Surrey University, an MBA from Cranfield University and honorary doctorates from Surrey, Edinburgh, Napier and Kingston Universities.

Andrew is the Founder and Chief Executive Officer of Rockley Photonics. Andrew is a leading proponent of silicon photonics and has led innovation in many aspects of photonics technologies. He was previously founder, chief executive and chairman of Bookham Technology and grew the company to become a FTSE100 business. In 1988, Bookham, renamed Oclaro, became one of the world's largest fiber optics telecom component producers. Oclaro is now part of Lumentum. More recently, Andrew was chairman of Kotura Inc., a leader in the field of silicon photonics for fiber optic communications. He was instrumental in Kotura's development and its sale to Mellanox Technologies Ltd. in 2013.

Andrew is a chartered engineer and a Fellow of the Royal Academy of Engineering and the Institute of Physics. He was awarded an OBE in the Queen's Millennium Honours list for services to the telecommunications industry and is a winner of the prestigious Royal Academy of Engineering Silver medal for his outstanding contribution to British Engineering.