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The characterisation and passivation of fixed oxide charges and interface states in the Al_2O_3/InGaAs MOS system

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Abstract

In this paper we present and overview of experimental results examining charged defect components in the Al_2O_3/$In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor (MOS) system. For the analysis of fixed oxide charge and interface state density an approach is described where the flat band voltage for *n* and *p* type Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOS structures is used to separate and quantify the contributions of fixed oxide charge and interface state density. Based on an Al_2O_3 thickness series (2nm to 20nm) for the *n* and *p* type $In_{0.53}Ga_{0.47}As$ layers, the analysis reveals a positive fixed charge density (~$9x10^{18}$ cm^{-3}) distributed throughout the Al_2O_3 and a negative sheet charge density (-$8x10^{12}cm^{-2}$) located near the Al_2O_3/$In_{0.53}Ga_{0.47}As$ interface. The interface density integrated across the energy gap is ~ $1x10^{13}$ cm^{-2} and is a donor type (+/0) defect. The density of the fixed oxide charge components is significantly reduced by forming gas (5% H_2/95% N_2 ambient at 350ºC for 30 min) annealing. The interface state distribution obtained from multi-frequency capacitance-voltage and conductance-voltage measurements on either MOS structures or MOSFETs indicates a peak density located around the $In_{0.53}Ga_{0.47}As$ mid-gap

energy, with a sharp increase in the interface state density towards the valance band and evidence of interface state aligned with the $In_{0.53}Ga_{0.47}As$ conduction band. The integrated density obtained from multi-frequency capacitance-voltage and conductance-voltage analysis is in good agreement with the approach of comparing the flat band voltages in *n* and *p* type $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS structures. Finally, the paper reviews recent work based on an optimisation of the $In_{0.53}Ga_{0.47}As$ surface preparation using $(NH_4)_2S$, combined with minimising the transfer time to the atomic layer deposition reactor for the Al_2O_3, which indicates interface state reduction and genuine surface inversion for both *n* and *p* type $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS structures.

1. Introduction

The last fifty years have witnessed dramatic developments in computing power, information storage and digital communication technologies. A significant driving force behind these developments has been the on-going miniaturisation of metal oxide semiconductor field effect transistors (MOSFETs), which represent the fundamental switching elements of integrated circuits. The scaling of MOSFETs minimum device dimensions from values of around 10 μm in the early 1970's to values of around 65 nm in 2006 was performed to increase transistor density and switching speed and was achieved without any significant changes to the fundamental device concept or the basic SiO_2 and Si materials which constituted the device.

As the minimum dimensions of MOSFETs were reduced to values below around 50nm, transistor miniaturisation no longer remained as the single driving force behind the development of integrated circuits. In the recent technology generations there has been a concerted research effort to incorporated new materials into the device structure to reduce the power dissipation associated with individual MOSFETs and consequently to reduce the overall power dissipation associated with integrated circuits. The power dissipation of *n* and *p* channel MOSFETs in a Complementary MOS (CMOS) configuration is comprised of both static and dynamic components. A significant reduction in static power dissipation was achieved with the incorporation of an HfO_2 based high dielectric constant (high-*k*) material into the gate stack of MOSFETs to reduce gate current leakage at the 45nm technology node [1]. The dynamic power dissipation is proportional to the square of the supply voltage (V_{dd}), and as a consequence the use of semiconductor materials or device architectures which allow V_{dd} reduction are also being

investigated to reduce the dynamic power dissipation in CMOS inverters. One approach to reduce V_{dd} without reducing the drive current and the associated switching speed is through the use of high mobility materials, such as Ge and III-V compound semiconductors, to form the active channel region of the MOSFETs. A range of alternative semiconductors have been studied which exhibit high hole mobility (Ge [2], GaSb [3], InGaSb [4]) and high electron mobility (InGaAs [5-8], InAs [9], InSb [10]).

There are a range of challenges associated with the realisation of high channel mobility materials, which include: the understanding, control and passivation of electrically active defects at the interface between the high-*k* dielectric layer and the III-V or Ge surface, fixed oxide charges within the high-*k* oxide and traps within the oxide (border traps); the reduction of the overall source and drain contact resistance in III-V semiconductors; the integration of the high mobility materials onto a 300mm silicon platform; the control of the band to band tunnelling leakage in reduced band gap semiconductors (Ge=0.66eV, $In_{0.53}Ga_{0.47}As$ =0.75eV); and finding a suitable *p* channel device when using III-V materials for both the *p* and *n* channel MOSFET.

Considering the issue of the gate stack formation, the search to find suitable dielectrics and processes to form stable III-V MOS structures with acceptable levels of electrically active interface states is not a new pursuit, with publications on GaAs MOSFETs dating back to the mid-1960's [11]. Early work focussed on chemical, thermal, or anodic oxidation of the III-V surface (GaAs), as well as sputter deposition methods [12-14]. More recent work has focussed on the use of atomic layer deposition (ALD) for the formation of high-*k* oxides on III-V surfaces [15]. In the case of MOS systems formed on GaAs [16] and on $In_xGa_{1-x}As$ (x: 0.3 to 0.15) [17] surfaces the capacitance-voltage (C-V) response is generally dominated by a high level of dispersion of the capacitance with frequency consistent with a high ($>10^{13}$ $cm^{-2}eV^{-1}$) density of interface states (D_{it}) at the high-*k*/In_xGa_{1-x} As (x: 0, 0.15, 0.3) interface. Analysis of the C-V response at a reduced temperature of 77K [18] confirms that the Fermi level is strongly pinned at high-*k*/GaAs and high-*k*/$In_xGa_{1-x}As$ (x: 0.15 to 0.3) interfaces. A significant reduction of D_{it} and a genuine demonstration of surface inversion at the high-*k*/GaAs interface can be achieved through the use of gallium sub oxide (Ga_2O) deposition onto an oxide free GaAs surface using an ultra-high vacuum environment [19, 20]. Similar results can also be achieved using silicon

interlayers inserted between the GaAs surface and the oxide layer [21, 22]. However, these results demonstrating genuine surface accumulation and inversion have not been replicated to date using ALD to form the high-*k* gate oxide on GaAs.

When moving to MOS systems formed on $In_{0.53}Ga_{0.47}As$ surfaces, (which is a lattice matched indium concentration to InP), a range of publications demonstrate modulation of the surface Fermi level with the gate voltage and genuine surface accumulation in MOS capacitors formed on *n*-type $In_{0.53}Ga_{0.47}As$ [17, 23-25]. However, the multi-frequency C-V response of the $In_{0.53}Ga_{0.47}As$ MOS capacitors for a range of ambient temperatures still indicates the influence of an interface defect response, and interface state densities around the $In_{0.53}Ga_{0.47}As$ mid-gap energy are typically reported to be in the range mid-10^{12} to $2x10^{13}cm^{-2}eV^{-1}$ [26-29]. Analysis of C-V response of $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS structures also indicates the presence of fixed positive oxide charges [30, 31] within the oxide layer. In addition to fixed oxide charge and interface states, dispersion in the C-V response of $In_{0.53}Ga_{0.47}As$ MOS for samples biased in accumulation has been attributed to the effect and defects located within the oxide near the oxide/$In_{0.53}Ga_{0.47}As$ interface (sometimes referred to as border traps [32]), which can communicate with the conduction and valence bands of the $In_{0.53}Ga_{0.47}As$ by a tunnelling process [33, 34].

As charges in the bulk of the oxide and interface states affect MOSFET performance, stability and long term reliability, it is important to characterize and understand the various defect components. The objective of this paper is to provide an overview of charged defect quantification in the $In_{0.53}Ga_{0.47}As$ MOS system. The paper will firstly review a method to separate fixed oxide charges and interface states based on the determination of the flat band capacitance for *n* and *p* type $In_{0.53}Ga_{0.47}As$ MOS structures. Following this section, the paper will provide a summary of the interface state density distribution across the energy gap as determined from the analysis of MOS capacitors and MOSFETs. Finally, the paper will cover approaches which have been studied to reduce the interface state density in $In_{0.53}Ga_{0.47}As$ MOS system, and demonstrate that following an optimized $In_{0.53}Ga_{0.47}As$ surface preparation interface state densities can be reduced to a level which results in a C-V response consistent with genuine surface inversion for both *n* and *p* type $In_{0.53}Ga_{0.47}As$ MOS structures.

The paper will focus on the case of the $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS system, as experimental results [23, 24], supported by theoretical calculations [35] indicate that Al_2O_3 reduces the concentration of electrically active states at the oxide/$In_{0.53}Ga_{0.47}As$ interface. Moreover, the process of forming Al_2O_3 on the $In_{0.53}Ga_{0.47}As$ surface using trimethylaluminum (TMA) [$Al(CH_3)_3$] and H_2O results in a reduction of the native oxides on the $In_{0.53}Ga_{0.47}As$ surface [15] through a process of ligand exchange [36]. As a consequence, the use of Al_2O_3 deposited by ALD is representative of the best interfacial properties reported to date for the oxide/$In_{0.53}Ga_{0.47}As$ MOS system. While Al_2O_3 exhibits a relatively low *k* value (8 to 8.6), the equivalent oxide thickness (E_{OT}) of the gate stack can be reduced by utilizing a bi-layer oxide approach where the Al_2O_3 is used as an interfacial control layer and an oxide with a higher *k* value (e.g., HfO_2) is subsequently deposited to achieve a scaled E_{OT} [37, 38].

2. Experimental Sample Details

The experimental results and analysis presented in this paper are based on both $Al_2O_3/In_{0.53}Ga_{0.47}As$/InP MOS capacitors and *n*-channel $In_{0.53}Ga_{0.47}As$ MOSETs. For the case of the MOS capacitor samples $In_{0.53}Ga_{0.47}As$ epitaxial layers of 2μm in thickness were grown by metal organic vapour phase epitaxy (MOVPE) on InP (100) substrates. For the case of the *n* type samples the $In_{0.53}Ga_{0.47}As$ layers were doped with sulphur to ~ $4x10^{17}cm^{-3}$ on heavily *n*-doped (S at ~$2x10^{18}cm^{-3}$) InP substrates. For the corresponding *p* type samples the $In_{0.53}Ga_{0.47}As$ layers were doped with zinc to ~ $4x10^{17}cm^{-3}$ on heavily *p*-doped (Zn at ~$2x10^{18}cm^{-3}$) InP substrates. Experimental results are reported for samples with and without chemical treatments of the $In_{0.53}Ga_{0.47}As$ surface prior to the atomic layer deposition of the Al_2O_3 layer. For the samples with chemical treatment prior to oxide deposition, the $In_{0.53}Ga_{0.47}As$ surfaces were initially degreased by sequentially rinsing for 1 min each in acetone, methanol, and isopropanol. Before the Al_2O_3 deposition, the samples were immersed in $(NH_4)_2S$ solutions (10% in deionized H_2O) for 20 min at room temperature (~295K). The 10% $(NH_4)_2S$ surface preparation approach for 20 minutes and room temperature was found to be the optimum to suppress the formation of $In_{0.53}Ga_{0.47}As$ native oxides and to reduce the high-*k*/$In_{0.53}Ga_{0.47}As$ interface state density [39, 40]. The optimum of 10% $(NH_4)_2S$ was subsequently confirmed to yield improvements in fully fabricated planar and 3D $In_{0.53}Ga_{0.47}As$ MOSFETs [41]. Following the

10% $(NH_4)_2S$ surface preparation the samples were introduced to the atomic layer deposition (ALD) chamber. Results are presented where the transfer time from the aqueous $(NH_4)_2S$ solution to the ALD chamber varied between 3 and 30 minutes. The Al_2O_3 dielectric was deposited by ALD at temperatures in the range 270 to 300°C using TMA and H_2O. The TMA pulse was the first pulse in the ALD process. A range of Al_2O_3 thickness values from 5 nm to 20 nm were fabricated. Results are presented for samples with Ni(60nm)/Au(40nm) metal gates formed by electron beam evaporation and a lift-off process [24, 39], and for samples with a Pt gate (75nm) formed by electron beam evaporation through a shadow mask [31].

For the analysis based on surface-channel MOSFETs, the devices were fabricated on a 2-µm-thick Zn-doped (4×10^{17} /cm^3) *p*-$In_{0.53}Ga_{0.47}As$ layer grown on *p*+ InP (100) wafer by metal-organic vapor phase epitaxy (MOVPE). The $In_{0.53}Ga_{0.47}As$ surface passivation prior to gate oxide deposition was an immersion in 10% $(NH_4)_2S$ at room temperature for 20 min (transfer time < 5 minutes). A 10-nm-thick Al_2O_3 gate oxide film was formed by ALD using alternating pulses of TMA and H_2O precursors at 250°C. The source and drain (S/D) regions were selectively implanted with a Si dose of 1×10^{14} cm^{-2} at 80 keV and 1×10^{14} cm^{-2} at 30 keV. Implant activation was achieved by rapid thermal anneal (RTA) at 600°C for 15 s in a N_2 atmosphere [42]. A 200-nm-thick Pd gate was defined by electron beam evaporation and lift-off. Non-self-aligned ohmic contacts were defined by selective wet etching of the Al_2O_3 in dilute HF and electron beam evaporation of an Au (14 nm)/Ge (14 nm)/Au (14 nm)/Ni (11 nm)/Au (200 nm) metal stack. It is noted that MOS capacitors were also included in the MOSFET fabrication process flow. Further details can be found in [43].

The C-V and conductance-voltage (G-V) measurements were recorded using either an HP4284A, CV enabled B1500, or an E4980 Agilent LCR meter. The measurements, from -50°C to 25°C, were performed on-wafer in a microchamber probe station (Cascade Microtech, model Summit 12971B) in a dry air, dark environment (dew point < -65°C).

3. Charge Separation and Quantification at the Flat Band Voltage (V_{fb})

The results in Figures 1 (a) and 1 (b) provide representative multi-frequency C-V responses (100 Hz to100 kHz) for Au/Ni/Al_2O_3(8nm)/$In_{0.53}Ga_{0.47}As$/InP MOS capacitors for *p*-type and *n*-type $In_{0.53}Ga_{0.47}As$ layers, respectively. The samples received a 10% $(NH_4)_2S$ surface preparation for

20 minutes and room temperature, with a 7 minute transfer time to the ALD system. The C-V responses demonstrate a range of features which are generally representative of $In_{0.53}Ga_{0.47}As$ MOS structures. Considering the case of the *n*-type $In_{0.53}Ga_{0.47}As$ MOS structure as shown in Figure 1 (b). In the nominally accumulated region of the C-V (V > 0.5 V) the sample exhibits a relatively low level of frequency dispersion (1.0 % per decade). The black horizontal line represents the theoretical maximum low frequency capacitance calculated using a Poisson-Schrodinger C-V simulation based on the $In_{0.53}Ga_{0.47}As$ Γ Valley only [44]. Upon cooling the sample down to 77K the capacitance (V > 0.5 V) exhibits very little change (for example see [18]), and this observation is consistent with genuine surface accumulation of electrons at the Al_2O_3(8nm)/*n*-$In_{0.53}Ga_{0.47}As$ interface as opposed to capacitance dominated by an interface defect response. It is noted that the measured capacitance exceeds the theoretical maximum low frequency capacitance, which will be discussed further in section 4.

In the gate voltage region from -0.5V to -2 V the C-V exhibits a frequency dependent distortion, where the capacitance moves through a peak value and subsequently decreases with increasing negative gate voltage. This observation is typical of *n*-type $In_{0.53}Ga_{0.47}As$ MOS structures and has been observed for a range of oxides, including: Al_2O_3 [45], SiO_2 [46], HfO_2 [17], $LaAlO_3$ [47], Si_3N_4 [48] and $SrTaO_6$ [49]. This type of C-V response is characteristic of an interface state distribution which exhibits a peak density at a specific energy level in the $In_{0.53}Ga_{0.47}As$ band gap [50], and is discussed further in section 4 of the paper. It is noted that when higher D_{it} levels are present and/or thicker oxides are used, the effect is to stretch out the D_{it} response along the gate voltage axis, and a clear peak in the C-V may not be observed in this case [51].

The C-V behaviour of the MOS structure is influenced by fixed oxide charges, interface states and defects within the oxide (border traps). The conventional approach to determine the interface state density and the fixed oxide charge density is to determine the two quantities separately from multi-frequency C-V and G-V responses and the flat band voltage (V_{fb}) respectively. In this section we will review an approach reported in [31], where the fixed oxide charge and the integrated interface state density across the energy gap (in units [cm^{-2}]) can be separated and quantified based on the experimental flat band voltage for *n* and *p* type $Al_2O_3/In_{0.53}Ga_{0.47}As$/InP MOS structures.

The concept behind the approach is illustrated in Figures 2 (a) and 2 (b), where the flat band condition is represented on a schematic energy band diagram for *p* and *n* type $In_{0.53}Ga_{0.47}As$ structures respectively. For the sake of illustration, it is assumed in Figure 2 that the interface states are donor (0/+) type. Considering first the fixed oxide charge (Q_{fixed}) component, it is reasonable to assume that the fixed oxide charge density and distribution in the high-*k* layer (Al_2O_3 in this case), will not depend on the dopant type of the InGaAs, as the dopant concentration of $4x10^{17}$ cm^{-3} represents one dopant atom for approximately every 10^5 In, Ga or As substrate atoms. The charge associated with the interface state density at the flat band condition, however, will depend on the nature and density of the interface states. The position of the Fermi level (E_F) at the flat band condition relative to the conduction band edge (E_C) or valence band edge (E_V) is set by the semiconductor doping concentration. For $In_{0.53}Ga_{0.47}As$ with a doping concentration of $4x10^{17}$ cm^{-3}, as presented in this work, the Fermi level (E_F) at flat band condition is close to the band edges, with E_C-E_F ~ 0.04 eV and E_F-E_V~0.04 eV for the *n* and *p* type $In_{0.53}Ga_{0.47}As$, respectively. Consequently, the Fermi level position at the Al_2O_3/$In_{0.53}Ga_{0.47}As$ interface, at the flat band voltage (V_{fb}), in *n* and *p* doped $In_{0.53}Ga_{0.47}As$ MOS structures ($4x10^{17}$ cm^{-3}), spans the majority of the $In_{0.53}Ga_{0.47}As$ energy gap. Consequently, the interface states are primarily unoccupied for a *p*-type substrate and primarily occupied for the *n*-type substrate. The corresponding equations for the flat band voltages are shown in Figures 2(a) and 2(b).

This provides an approach to quantify and separate the fixed oxide charge and interface state density contributions. From the equations for the respective flat band voltages for the *p* (V_{fbp}) and *n* (V_{fbn}) samples, as shown in Figures 2 (a) and 2 (b), by subtraction of V_{fbn} and V_{fbp}, the fixed oxide charge term and the metal work function in contact with the oxide are eliminated, and the resulting equation is below,

$$V_{fbN} - V_{fbP} = \left(\phi_{sp} - \phi_{sn}\right) + \frac{qD_{it}}{C_{ox}} \tag{1}$$

Consequently, the magnitude of the difference between V_{fbn} and V_{fbp} represents the magnitude of D_{it} integrated across the energy gap in units of [cm^{-2}]. The sign of $\left(V_{fbN} - V_{fbP}\right) - \left(\phi_{sp} - \phi_{sn}\right)$ indicates if the interface states are net donor or net acceptor type. Once D_{it} is evaluated it can be substituted back into the individual equation for V_{fbp} and V_{fbn} in Figures 2(a) and 2(b).

Alternatively, if a value for the work function of the metal on the oxide is known or assumed, the total charge density at the flat band voltage (Q_{fixed} + qD_{it}) can be determined in each case and the difference in the calculated values yields the interface state density (qD_{it}).

For this approach, it is necessary to perform the electrical measurements under conditions which minimise the capacitance contribution of the interface states (C_{it}) and/or border traps (C_{bt}) to the overall measured capacitance, allowing a determination of the flat band capacitance and corresponding flat band voltage. In order to approximate to the true high frequency response, measurements were performed at a temperature of -50°C and an *ac* signal frequency of 1 MHz. Under such measurement conditions, interface traps are manifest primarily as a stretch out of the depletion part of the C-V characteristic along the gate voltage axis. The temperature of -50°C and the frequency of 1 MHz were selected for practical reasons. The temperature of -50°C represents the lowest temperature available for the probe station used. Frequencies higher than 1 MHz can be affected by series resistance contributions.

Figure 3 illustrates the C-V response at -50°C and 1 MHz of *n* and *p* type Au/Ni/Al_2O_3(8nm)/$In_{0.53}Ga_{0.47}As$/InP MOS capacitors. These are the same samples for which the multiple frequency C-V results were presented in Figure 1. Based on the doping concentration ($4x10^{17}cm^{-3}$), the Al_2O_3 thickness of 7.8 nm (from transmission electron microscopy), a dielectric constant of 8.6 for the Al_2O_3 [43], the flat band capacitance is determined as 0.006 F/m^2 and the corresponding V_{fbn} and V_{fbp} values are shown in Figure 3. The values of ϕ_{sn} and ϕ_{sp} are set by the $In_{0.53}Ga_{0.47}As$ electron affinity (4.9eV) and the $In_{0.53}Ga_{0.47}As$ doping concentrations and are also shown in Figure 3. Using equation (1) the integrated interface state density across the $In_{0.53}Ga_{0.47}As$ energy gap is $2.7x10^{12}$ cm^{-2}. The sign of $\left(V_{fbN} - V_{fbP}\right) - \left(\phi_{sp} - \phi_{sn}\right)$ is positive, which indicates the interface states are net donor type, in agreement with Brammertz et al. [52] and Varghese et al. [53][1]. Based on an assumed value for the 5eV for the Ni work function of in the Au/Ni gate stack, the fixed oxide charge density can be determined and is ~$3x10^{12}$ cm^{-2}. For the single oxide thickness value presented in Figure 3, it is not possible to determine if the fixed charge is located in a plane or distributed throughout the

[1] It is noted that it is possible for both donor and acceptor states to exist within the energy gap at the oxide/InGaAs interface, and in this case, the technique yields the density of donors minus the density of acceptors and not the magnitude of the donor plus acceptor concentrations. That is, the method determines the net charge associated with the D_{it} in the energy gap, and not the net density.

oxide layer. In addition, it is possible that both positive and negative fixed oxide charge exist in the oxide layer. For this analysis it is necessary to examine an Al_2O_3 thickness series, which is considered next.

Figure 4 shows the results obtained from an Al_2O_3 thickness series experiment. The samples are Pt gate $Al_2O_3/In_{0.53}Ga_{0.47}As$/InP MOS capacitors over *n* and *p* type ($4x10^{17}$ cm^{-3}) $In_{0.53}Ga_{0.47}As$. The $In_{0.53}Ga_{0.47}As$ surface received no surface preparation prior to the ALD alumina process. The thickness series included samples with no annealing following the oxide deposition and metal gate formation (referred to as "no FGA"), and a corresponding series with a forming gas anneal (FGA) in a 5% H_2/95% N_2 ambient at 350^{o}C for 30 min. From the flat band voltage determined at -50^{o}C and 1 MHz, the total charge (Q_{tot}) was determined based on an assumed Pt work function of 5.4eV [54]. For more details see [31]. Q_{tot} represents the sum of the fixed oxide charge (Q_{fixed}) and the *charged* interface state component at the flat band condition, and is the equivalent charge density (in units [cm^{-2}]) located at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface. The results are presented for Al_2O_3 thickness values from 11nm to 20nm, for samples with and without FGA.

The Figure contains a number of significant features relating to the charge components in the $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS structure. Firstly, the total charge Q_{tot} at V_{fb} for both the *n* and the *p* type $In_{0.53}Ga_{0.47}As$ MOS structures prior to FGA is positive and increase linearly with the Al_2O_3 thickness, indicating that the fixed oxide charge in the Al_2O_3 is distributed uniformly throughout the oxide layer. From the slope of Q_{tot} versus the Al_2O_3 thickness (t_{ox}), for either the *n* or *p* type MOS samples, the volume density of positive charge is ~ $7x10^{18}$ cm^{-3} to $1.1x10^{19}$ cm^{-3}. Secondly, the magnitude of Q_{tot} is higher for the *p* than the *n* type $In_{0.53}Ga_{0.47}As$ MOS structures by a constant amount. This corresponds to the value of D_{it} integrated across the $In_{0.53}Ga_{0.47}As$ energy gap and has a density of $1.1x10^{13}$ cm^{-2}. The magnitude of Q_{tot} is higher for *p* than *n* type $In_{0.53}Ga_{0.47}As$, again indicating that the net D_{it} across the energy gap is donor type, in agreement with the results in Figure 3 and [52, 53]. The integrated D_{it} in Figure 4 (pre FGA) is higher than the value obtained for the samples in Figure 3 ($2.7x10^{12}$ cm^{-2}). The samples in Figure 3, however, experienced an $(NH_4)_2S$ surface preparation (10% in deionized H_2O) for 20 min at room temperature, prior to the ALD oxide deposition, confirming the efficacy of the $(NH_4)_2S$ surface preparation in D_{it} reduction for the $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS system. A third

observation from Figure 4 relates to the total charge density extrapolated to zero Al_2O_3 thickness for the pre-FGA samples. As discussed previously, the interface defects within the energy gap are donor type, as a consequence for an *n* type $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS capacitor at V_{fb} the interface defects are occupied and neutral, and the charge at V_{fb} is only influenced by the fixed oxide charge component. If the Al_2O_3 layer contained only uniformly distributed positive charges, then the extrapolated Q_{tot} for this sample should intercept the origin in Figure 4. However, extrapolation of this curve yields a value of $-7.6x10^{12}$ cm^{-2}, indicating a negative fixed oxide charge component present at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface. Hence, Q_{tot} is comprised of a positive charge density on the oxide Q_{ox} and a negative sheet charge at the interface (Q_{int}). Finally, from Figure 4, the fixed oxide charge components (both positive and negative) in the Al_2O_3 are both significantly reduced by the forming gas annealing process.

Based on the results presented in Figure 4, the picture which emerges for the charge type and distribution for the $Al_2O_3/In_{0.53}Ga_{0.47}As$ is illustrated in the TEM image in Figure 5. The distribution of positive charge throughout the Al_2O_3 and the negative charge located close to the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface is in agreement with the analysis in [30]. The same charge distribution in the oxide was also obtained for the Al_2O_3/GaSb MOS system [55]. The density of the positive and negative charge are reduced significantly following forming gas annealing 5% H_2/95% N_2 ambient at 350^{o}C for 30 min, and the results are summarized in Table 1[2].

Based upon first principles calculations and x-ray photoelectron spectroscopy results it has been proposed that the bulk positive fixed charge can be attributed to aluminium dangling bonds and the negative fixed charge near the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface to oxygen dangling bonds in the Al_2O_3 layer [30]. The observation that the positive and negative charge densities can be significantly reduced following a FGA is consistent with this observation as atomic hydrogen resulting from the forming gas anneal process is known to passivate dangling bond centres, with

[2] The interface state density is also reduced by the FGA. However, for the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface in the full MOSFET process, which experienced a 600°C for 15 s in a N_2 to activate the source and drain silicon doping implantation, the FGA has no influence on the interface state density [71]. As a consequence, the reduction in D_{it} recorded in Table 1 is most probably a result of a structural rearrangement of the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface due to the temperature of the FGA process (350^{o}C), which is higher than the Al_2O_3 growth temperature (270^{o}C), and not a result of hydrogen passivation of interface states.

the Pt gate electrode assisting in the dissociation of molecular hydrogen into atomic hydrogen [56].

4. The D_{it} Energy Distribution at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ Interface

The technique of charge separation at the flat band voltage, as described in section 3, provides the integrated density of the defects across the band gap and identifies if the defects are primarily donor or acceptor type. However, the technique does not contain information relating to the energy distribution of the interface defects. The energy distribution can be contained from analysis of the multi-frequency C-V or G-V responses, using the well-established high-low frequency C-V method [57], the Terman Method [58] or via conductance analysis [59].

To provide insight into the D_{it} distribution which can yield the C-V behavior exhibited by the $In_{0.53}Ga_{0.47}As$ MOS samples in Figures 1 (a) and 1 (b) it is instructive to consider the multi-frequency C-V responses reported for $Si(100)/SiO_2$ and $Si(100)/SiO_x$/high-*k* MOS structures where a high density of silicon dangling bonds (P_{bo} and P_{b1}) are present at the $Si(100)/SiO_2$ interface. The silicon dangling bonds (P_{bo} and P_{b1}) are amphoteric defects and have specific peak energies in the silicon band gap, which are reported to be around 0.3eV and 0.85eV above E_V in silicon based on electrical [60-65] and biased electron spin resonance methods [66]. These defects are electrically active following the dissociation of hydrogen from the dangling bonds. This can be achieved by vacuum annealing (T> 700^{o}C) [62], a rapid pull from an oxidation furnace [60] or through a process of rapid thermal annealing (RTA) in a N_2 ambient [63], where the cooling from the maximum RTA temperature is too rapid to allow passivation during the cooling process. Analysis of the high-*k*/Si MOS system by electron spin resonance [67, 68] and C-V analysis [69, 70] indicates that the dominant interface defects are also P_b centres, as the interface region between the silicon and the high-*k* film (either intentionally or via the high-*k* growth process) is an SiO_x layer.

An example C-V response is shown for a $TiN/HfSi_xO_yHfO_2/SiO_x/Si(100)$ MOS capacitor in Figure 6 (a) [69], where the sample experienced no final forming gas annealing and un-passivated P_b centres are present. The corresponding interface state profile in the upper gap region is shown in Figure 6 (b). There are clear similarities between the C-V response of P_b

centres in the TiN/$HfSi_xO_y$/HfO_2/SiO_x/Si(100) MOS structures in Figure 6 (a), and interface defect response for the Al_2O_3(8nm)/$In_{0.53}Ga_{0.47}As$/InP MOS capacitor in Figure 1 (b). Both indicate a frequency-dependent C-V distortion, with the capacitance moving through a peak and subsequently reducing. In addition, the peak capacitance occurs at a bias closer to the accumulation region with increasing ac signal frequency. The C-V response, in both cases, is consistent with an interface state density which has a peak density at a specific energy in the band gap. This is also supported by first principles C-V simulations by Masson et al [50]. The similarities between C-V response for the TiN/$HfSi_xO_y$/HfO_2/SiO_x/Si(100) and the Al_2O_3(8nm)/$In_{0.53}Ga_{0.47}As$/InP MOS capacitors, provides a platform for interpreting the typical InGaAs C-V responses, and also strong evidence that the D_{it} at the Al_2O_3/$In_{0.53}Ga_{0.47}As$ exhibits a peak density at a specific energy in the $In_{0.53}Ga_{0.47}As$ energy gap.

Figure 7 (a) presents the interface state density versus gate voltage obtained for the high-low C-V approach (high=1MHz and low=200Hz) and the conductance approach (200Hz) for the Al_2O_3(8nm)/*n*-$In_{0.53}Ga_{0.47}As$/InP MOS capacitor shown in Figure 1 (b). The equivalent parallel conductance, G_p, was converted to a peak interface state density using the assumption of zero deviation in surface potential band bending. It is observed that the conductance and the high-low approach are in reasonable agreement. For more details see [39]. Translating the gate voltage to the energy position was achieved by assuming that the 1 MHz C-V represents a true high frequency response, and the resulting D_{it} distribution is shown in Figure 7 (b). The interface state distribution exhibits a peak density of $1.5x10^{13}$ $cm^{-2}eV^{-1}$ at 0.35eV above the valence band edge. The interface density in units of [cm^{-2}] is obtained through the integral of the curve. The integrated density from 0.26eV to 0.61eV yields a value of $2.9x10^{12}$ cm^{-2}. The approach of using V_{fbn} and V_{fbp}, as shown in Figure 3, on the same sample set, yielded $2.7x10^{12}$ cm^{-2} demonstrating the consistency of the two separate approaches for the calculation of the integrated interface state density.

An alternative approach to profile the energy distribution of interface states for the Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOS system based on analysis of the full gate capacitance of the surface *n*-channel $In_{0.53}Ga_{0.47}As$ MOS transistors has recently been reported [71]. In this approach, the experimental capacitance, recorded at -50^oC and 1 MHz to approximate a high frequency response, is compared to the theoretical C-V response to evaluate the interface state distribution

across the $In_{0.53}Ga_{0.47}As$ energy gap. This approach has the advantage of profiling the interface state density distribution using a single device structure. The resulting interface state distribution is shown in Figure 8.

In agreement with the C-V and G-V analysis in Figure 7 (b), the analysis of the full MOSFET gate capacitance reveals a peak D_{it} density around the mid gap energy (E_v+ 0.36eV). The observation of a peak density near the $In_{0.53}Ga_{0.47}As$ mid-gap energy has also been reported in other works, for different high-*k* oxides, including: $LaAlO_3$ [72], $SrTa_2O_6$ [49] and an Al_2O_3/HfO_2 bi-layer [26]. The density and energy at the peak are compared in table 2. The similarity in the energy associated with the peak D_{it} for the different high-*k* oxides suggest that the interfacial defects are related to the $In_{0.53}Ga_{0.47}As$ surface and not to the oxide layer. This indicates options such as dangling bonds or dimers of As, Ga or In and anti-site defects, such as the AsGa anti-site. The energy at the peak density and charge transition type (donor) are consistent with As_{Ga} anti-site defects based on hybrid density functional calculations of point defects in III–V compounds [73]. It is noted, however, that not all groups report a peak in the interface state density within the band gap, and a number of publications indicate a monotonic increase in the interface state density from the $In_{0.53}Ga_{0.47}As$ conduction band to the $In_{0.53}Ga_{0.47}As$ valence band edge [52, 74, 75]. The determination of the precise energy distribution of D_{it}, and in particular whether or not a peak density occurs within the energy gap, is an area where further research is needed in the high-*k*/$In_{0.53}Ga_{0.47}As$ MOS field.

From Figure 8, it is also observed that the interface state density is low around the $In_{0.53}Ga_{0.47}As$ conduction band edge, and increases sharply into the conduction band. Including a D_{it} component at energies > E_c is required as the experimental values of capacitance exceed the predicted maximum theoretical values when the Fermi level enters the $In_{0.53}Ga_{0.47}As$ conduction band. The interface states aligned with the conduction band are acceptor like, and the results in Figure 8 are in agreement with other publications [74, 76]. The observation of interface states aligned with the $In_{0.53}Ga_{0.47}As$ conduction band is also consistent with C-V measurements on GaAs MOS and $In_xGa_{1-x}As$ MOS capacitors ($x \leq 0.3$). For *n*-GaAs MOS [16] and *n*-$In_xGa_{1-x}As$ MOS capacitors ($x \leq 0.3$) [17, 18] the C-V response is not consistent with genuine surface accumulation, and analysis indicatives a high density of acceptor like interface states in the upper region of the energy gap. The *n*-$In_{0.53}Ga_{0.47}As$ MOS samples do exhibit genuine surface

accumulation of electrons. The energy gap reduction from GaAs to $In_{0.53}Ga_{0.47}As$ is primarily due to a reduction in the energy of the conduction band minima (i.e., an increase in electron affinity). In this case, the interface defects which prevent surface accumulation in *n*-$In_xGa_{1-x}As$ MOS capacitors ($x \leq 0.3$) are located in the conduction band for $In_{0.53}Ga_{0.47}As$ MOS structures. Consequently, the C-V observations and analysis for *n*-$In_xGa_{1-x}As$ MOS capacitors ($x \leq 0.3$) are consistent with the inferred presence of interface states with energies aligned with the conduction band for the case of $In_{0.53}Ga_{0.47}As$ MOS structures.

Finally, it is noted that there is also a sharp increase in D_{it} towards the valence band edge, which is in agreement with most publications on the interface state density in the oxide/$In_{0.53}Ga_{0.47}As$ system [52, 74, 75]. Based on the experimental approach used in this work, it is not possible to discriminate between the contributions of border traps or interface states for D_{it} close to the valence band or for D_{it} aligned with the conduction band.

5. Reduction of D_{it} and Surface Inversion for $In_{0.53}Ga_{0.47}As$ MOS devices

A wide range of techniques have been explored to reduce or passivate electrically active interface states at the oxide/ $In_{0.53}Ga_{0.47}As$ interface. The techniques reported have included; the deposition of Ga sub-oxides on an As de-capped $In_{0.53}Ga_{0.47}As$ surface [77], nitridation of the $In_{0.53}Ga_{0.47}As$ surface [46], the use of As capping layers desorbed in the ALD reactor [78], the use of undoped InP capping layers [5], and the use of thin ALD oxide interface control layers [37].

The use of inorganic sulphides has been established as an approach to improve the electronic properties of III-V surfaces, and $(NH_4)_2S$ has been reported to improve surface recombination velocity for GaAs [79]. The approach has been extended to the chemical preparation of $In_{0.53}Ga_{0.47}As$ surface prior to oxide deposition and studies have been performed to identify the optimum conditions for $(NH_4)_2S$ surface preparation [39, 40]. Based on analysis using atomic force microscopy, x-ray photoelectron spectroscopy and C-V analysis, the optimum was found to be 10% $(NH_4)_2S$, at room temperature for 20 minutes. The exposure time between the removal from the $(NH_4)_2S$, solution and entry to the ALD system has been established to be a factor which influences the resulting D_{it} values [24].

The C-V results (20 Hz to 100 kHz) shown in Figures 9 (a-c) illustrate the influence of the air exposure time between the optimum $(NH_4)_2S$ surface preparation and entry of the sample into the ALD reactor for 8 nm Al_2O_3 deposition on *n*-InGaAs surfaces. The transfer times shown are 30 minutes, 7 minutes and 3 minutes. The three multi-frequency C-V responses illustrate the progressive reduction of the interface state concentration with the reduction of the transfer time from 30 minutes to 3 minutes. In Figure 9 (a), which is typical of C-V responses for an *n*-$In_{0.53}Ga_{0.47}As$ MOS structure, the full interface state response is outside the gate bias window on the measurement. The capacitance corresponding to the expected theoretical minimum capacitance (C_{min}) based on the doping concentration of $4x10^{17}$ cm^{-3} is also marked on the figure. The minimum experimental capacitance at 100 kHz does not reach the theoretical minimum indicating the surface is not inverted within the gate bias range examined. Figure 9 (b) is for the reduced exposure time of 7 minutes. In this case, the interface defect feature in depletion (highlighted by a red oval) is reduced in magnitude, and the experimental capacitance is closer to the theoretical minimum. Both of these observations are consistent with a reduction in the interface state concentration. Figure 9 (c), is for the case of a 3 minutes transfer time. The interface state response is significantly reduced in this case and the capacitance value at high frequency reaches the expected theoretical minimum value. While not clearly evident in the C-V response, the interface state defect response is still present in the range -0.5 to -1 V (highlighted by the red oval). The interface states in this region are still evident in the conductance response [24]. However, the interface state density concentration is clearly reduced significantly for this sample, and in the gate bias range < -2 V, the capacitance for a given *ac* signal frequency acquires an almost constant value with applied gate voltage. The constant capacitance in this region increases with decreasing frequency up to the maximum value set by the oxide capacitance. This is the characteristic *ac* response of an MOS system in inversion [80]. Detailed analysis of the capacitance and conductance of this sample with *ac* signal frequency and temperature confirms surface inversion for both *n* and *p* doped $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS structures [24]. This characteristic behaviour of surface inversion has also been reported for Al_2O_3/n- $In_{0.53}Ga_{0.47}As$ [23] and Al_2O_3/p- $In_{0.53}Ga_{0.47}As$ [81] MOS capacitors, and for HfO_2/p-$In_{0.53}Ga_{0.47}As$ [25].

The C-V response for the corresponding Al_2O_3/*p*- $In_{0.53}Ga_{0.47}As$ /*p*+InP MOS capacitor with the optimised $(NH_4)_2S$ surface preparation and the 3 minutes transfer time is shown in Figure 10 (a). Again, the characteristic inversion behaviour is evident for $V_g > 1$ V, and analysis of the frequency and temperature dependence in the bias region $V_g>1$ V is consistent with surface inversion [24]. The minimum experimental capacitance at 1 MHz is in agreement with the theoretical value based on the Zn doping concentration ($4x10^{17}$ cm^{-3}). Analysis of the conductance around the region of the peak interface state density response ($V_g \sim -0.6$ V) yields a mid-gap D_{it} in the range 6 to $9x10^{11}$ $cm^{-2}eV^{-1}$. The significant reduction in the mid-gap D_{it} , when compared to the results in Figure 7 (b) and Figure 8, allows the Fermi level to be moved through the energy gap at the Al_2O_3/ $In_{0.53}Ga_{0.47}As$ interface within the applied bias range, resulting in the observed inversion behaviour for both the *n* and *p* type $In_{0.53}Ga_{0.47}As$ MOS structures.

Significantly, further support that the *ac* capacitance behaviour in Figures 10 (a) ($V_g> 1V$) and 9 (c) (Vg < -2 V), represent genuine surface inversion can be obtained from the Al_2O_3/*p*-$In_{0.53}Ga_{0.47}As$ MOS capacitors formed in a full surface-channel $In_{0.53}Ga_{0.47}As$ MOSFETs process [42]. The availability of the full MOSFET allows an accurate determination of the threshold voltage, which can be identified on the neighbouring Al_2O_3/*p*-$In_{0.53}Ga_{0.47}As$ MOS capacitor. An example is presented in Figure 10 (b) for the C-V response from 100 Hz to 100 kHz of an Al_2O_3 (10nm)/*p*-$In_{0.53}Ga_{0.47}As$/*p*+InP capacitor formed in a full $In_{0.53}Ga_{0.47}As$ MOSFET process described in section 2 of the paper. The threshold voltage (V_T) of the neighbouring MOSFET was 0.43 V and is identified on the Figure (dotted line). The V_T of the MOSFET relates to the condition of strong inversion at the Al_2O_3/*p*-$In_{0.53}Ga_{0.47}As$ interface, and consequently the multi-frequency C-V behaviour for $V_g > 0.43$ V in Figure 10 (b) corresponds to the C-V response of an inverted surface. This provides further support that the *ac* C-V response as shown in Figure 10 (a) does correspond to the condition of surface inversion.[3]

[3] It is noted that the "shoulder" in the capacitance at intermediate frequencies in the region corresponding to strong inversion (~ 0.5 V in Figure 10(a) and ~ 0.3 V in Figure 10 (b)) is not due to an interface state response. This behaviour is also evident in the simulated ideal multi-frequency C-V with no interface states, fixed charge or border traps. This is beyond the scope of this work and will be covered in a future publication.

6. Conclusions

The performance, stability and long term reliability of InGaAs MOSFETs will be affected by fixed oxide charges in the gate oxide and interface defects, so it is important to characterize and understand the various charged defect components within the InGaAs MOS system, and to explore ways to intrinsically remove or passivate the defect sites. In this work we have presented an overview of capacitance-voltage and conductance-voltage based analysis of fixed oxide charges and interface states in the $Al_2O_3/In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor (MOS) system, where the Al_2O_3 layer is deposited by atomic layer deposition.

Based on an analysis of the flat band voltage obtained from the high frequency (-50^{o}C, 1 MHz) CV responses of *n* and *p* type $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS structures, an approach has been described to determine the density of interface states (D_{it}) integrated across the $In_{0.53}Ga_{0.47}As$ energy and the total fixed charge in the oxide. Using this technique for an Al_2O_3 thickness series (2nm to 20nm), for samples with no initial $In_{0.53}Ga_{0.47}As$ surface preparation and no forming gas annealing, the analysis indicates a fixed positive oxide charge distributed through the Al_2O_3 layer (~$8x10^{19}$ cm^{-3}) and a negative sheet charge (~ -$8x10^{12}$ cm^{-2}) located near the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface. This charge distribution has been obtained for different ALD systems and for Al_2O_3/GaSb structures by other groups, indicating the charge density and distribution is related uniquely to the Al_2O_3 layer. The interface state density integrated across the energy gap (E_v+0.04eV to Ev+ 0.67eV) for samples prior to forming gas annealing (5% H_2/95% N_2 ambient at 350^{o}C for 30 min) is ~ $1x10^{13}$ cm^{-2} donor type defects (+/0). Following forming gas annealing the positive and negative oxide charge density is reduced significantly, consistent with the fixed charges being related to dangling bonds type defects in the Al_2O_3.

The interface state distribution determined from $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS structures and surface channel Al_2O_3 gate $In_{0.53}Ga_{0.47}As$ MOSFETs, yields a peak interface state density centred at 0.36 eV above the $In_{0.53}Ga_{0.47}As$ valence band edge, with a density ~ $1.5x10^{13}$ $cm^{-2}eV^{-1}$ for samples where the surface preparation and transfer time to the ALD system are not optimised. The interface state density increases sharply towards the valence band edge. The interface state density exhibits a minimum value near the $In_{0.53}Ga_{0.47}As$ conduction band edge, and then increases sharply into the $In_{0.53}Ga_{0.47}As$ conduction band, where the defects aligned with the conduction band are acceptor-like (0/-). Following an optimisation of the $In_{0.53}Ga_{0.47}As$

surface preparation in $(NH_4)_2S$ and minimising the transfer time to the ALD reactor, the mid gap interface state density is reduced to around 6-9x10^{11} $cm^{-2}eV^{-1}$, and the multi-frequency C-V and G-V responses are consistent with genuine surface inversion for both *n* and *p* type $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS structures.

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References

[1] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi,G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks , R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, K. Zawadzki,"*Tech. Dig. - Int. Electron Devices Meet*. 247, (2007)

[2] Choong Hyun Lee, Tomonori Nishimura, Kosuke Nagashio, Koji Kita and Akira Toriumi, *IEEE Elec. Dev. Letters* 58, 1295 (2011)

[3] A. Ali, H. S. Madan, A. P. Kirk, D. A. Zhao, D. A. Mourey, M. K. Hudait, R. M. Wallace, T. N. Jackson, B. R. Bennett, J. B. Boos, and S. Datta, *Appl. Phys. Lett.*, 97, 143502 (2010)

[4] Kuniharu Takei, Morten Madsen, Hui Fang, Rehan Kapadia, Steven Chuang, Ha Sul Kim, Chin-Hung Liu, E. Plis, Junghyo Nah, Sanjay Krishna, Yu-Lun Chueh, Jing Guo, and Ali Javey, *Nano Lett.* 12, 2060−2066 (2012)

[5] M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. K. Hudait, J. M. Fastenau,J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah,and Robert Chau *Tech. Dig. - Int. Electron Devices Meet.* 319, (2009)

[6] Steven J. Bentley, Martin Holland, Xu Li, Gary W. Paterson, Haiping Zhou, Olesya, Ignatova, Douglas Macintyre, Stephen Thoms, Asen Asenov, Byungha Shin, Jaesoo Ahn, Paul C. McIntyre and Iain G. Thayne, *IEEE Electron Device Letters,* 32 (4). pp. 494-496 (2011)

[7] Masafumi Yokoyama, Ryo Iida, Sanghyeon Kim, Noriyuki Taoka, Yuji Urabe, Hideki Takagi, Tetsuji Yasuda, Hisashi Yamada, Noboru Fukuhara, Masahiko Hata, Masakazu Sugiyama, Yoshiaki Nakano, Mitsuru Takenaka, and Shinichi Takagi, *IEEE Elec. Dev. Lett.*, VOL. 32, 1281 (2011)

[8] Mengwei Si, Jiangjiang J. Gu, Xinwei Wang, Jiayi Shao, Xuefei Li, Michael J. Manfra, Roy G. Gordon, and Peide D. Ye, *Appl. Phys. Lett.* 102, 093505 (2013)

[9] Anil W. Dey, Claes Thelander, Erik Lind, Kimberly A. Dick, B. Mattias Borg, Magnus Borgström, Peter Nilsson, and Lars-Erik Wernersson, *IEEE Electron Device Letters* , 33, 791 (2012)

[10] Robert Chau, Justin Brask, Suman Datta, Gilbert Dewey, Mark Doczy, Brian Doyle, Jack Kavalieros, Ben Jin, Matthew Metz, Amlan Majumdar, and Marko Radosavljevic, *Microelectronic Engineering* 80, 1-6, (2005)

[11] H. Becke, R, Hall, J. White, *Solid State Electronics,* 8 (10), 813 (1965)

[12] Physics and Chemistry of III-V Compound Semiconductor Interfaces, edited by C. Wilmsen, (Plenum, New York, 1985).

[13] H.H. Wieder, “Dielectric/semiconductor interfaces”, *J. Vac. Sci. Technol.* B11, 1331 (1993); and references therein.

[14] W.F. Croydon, E.H.C. Parker, *Dielectric Films on Gallium Arsenide* (Gordon and Breach, Scientific Publishers: New York, 1981)

[15] Robert M. Wallace, Paul C. McIntyre, Jiyoung Kim, and Yoshio Nishi, *MRS Bulletin*, 34, 493 (2009)

[16] G. Brammertz, H. C. Lin, K. Martens, D. Mercier, C. Merckling, J. Penaud, C. Adelmann, S. Sioncke, W. E. Wang, M. Caymax, M. Meuris, and M. Heyns, *J. Electrochem. Soc*. 155, H945 (2008)

[17] É. O'Connor, S. Monaghan, R. D. Long, A. O'Mahony, I. M. Povey, K. Cherkaoui, M. E. Pemble, G. Brammertz, M. Heyns, S. B. Newcomb, V. V. Afanas'ev, and P. K. Hurley, *Appl. Phys. Lett.* 94, 102902 (2009)

[18] P.K. Hurley, É. O’Connor, S. Monaghan, R. D. Long, A. O’Mahony, I. M. Povey, K.Cherkaoui, J. MacHale, A.J. Quinn, G. Brammertz, M. Heyns, S. B. Newcomb, V. V. Afanas’ev,, A. M. Sonnet, R. V. Galatage, M. N. Jivani, E. M. Vogel, R. M. Wallace and M. E. Pemble, *ECS Transactions*, 25 (6) 113-127 (2009)

[19] A. Callegari, P.D. Hoh, D.A. Buchanan and D. Lacey, *Appl. Phys. Lett.*, 54, 332 (1989)

[20] M. Passlack, M.Hong and J.P. Mannaertz, *Appl. Phys. Lett.*, 68, 1099 (1996)

[21] C. L. Hinkle, M. Milojevic, B. Brennan, A. M. Sonnet, F. S. Aguirre-Tostado, G. J. Hughes, E. M. Vogel, and R. M. Wallace, *Appl. Phys. Lett.*, 94, 162101 (2009)

[22] M. El Kazzi, L. Czornomaz, D. J. Webb, C. Rossel, D. Caimi, H. Siegwart, J. Fompeyrine,and C. Marchiori, *Appl. Phys. Lett.*, 99, 052102 (2011)

[23] H. D. Trinh, E. Y. Chang, P. W. Wu, Y. Y. Wong, C. T. Chang, Y. F. Hsieh, C. C. Yu, H. Q. Nguyen, Y. C. Lin, K. L. Lin, and M. K. Hudait, *Appl. Phys. Lett*. 97, 042903 (2010).

[24] É. O’Connor, S. Monaghan, K. Cherkaoui, I. M. Povey, and P. K. Hurley, *Appl. Phys Lett* 99, 212901 (2011)

[25] T. D. Lin Y. H. Chang C. A. Lin, M. L. Huang, W. C. Lee J. Kwo and M. Hong, *Appl. Phys. Lett*, 100, 172110 (2012)

[26] L. K. Chu, C. Merckling, A. Alian, J. Dekoster, J. Kwo, M. Hong, M. Caymax,and M. Heyns, “ *Appl. Phys. Lett.*, 99, 042908 (2011)

[27] G. Brammertz, H. C. Lin, K. Martens, D. Mercier, C. Merckling, J. Penaud, C. Adelmann, S. Sioncke, W. E. Wang, M. Caymax, M. Meuris, and M. Heyns, *J. Electrochem. Soc.* 155, H945 (2008)

[28] Yoontae Hwang, Roman Engel-Herbert, Nicholas G. Rudawski, and Susanne Stemmer, *Appl. Phys. Lett*. 96, 102910 (2010)

[29] Roman Engel-Herbert, Yoontae Hwang, and Susanne Stemmer, *Journal of Applied Physics*, 108, 124101 (2010)

[30] B. Shin, J.R. Weber, R.D. Long, P. K. Hurley, C.G. Van de Walle, G. Chris, P. C. McIntyre, *Appl. Phys. Lett*. 96, 152908 (2010)

[31] R. D. Long, B. Shin, S. Monaghan, K. Cherkaoui, J. Cagnon, S. Stemmer, P. C. McIntyre, and P. K. Hurley, *Journal of The Electrochemical Society*, 158 (5) G103-G107 (2011)

[32] D. M. Fleetwood, *IEEE Trans. on Nuclear Science*, 39, 269 (1992)

[33] Guy Brammertz, Alireza Alian, Dennis Han-Chung Lin, Marc Meuris, Matty Caymax, and W.-E. Wang, *IEEE Trans. on Elec. Dev*., 58, 3890 (2011)

[34] Yu Yuan, Bo Yu, Jaesoo Ahn, Paul C. McIntyre, Peter M. Asbeck, Mark J. W. Rodwell, and Yuan Taur, *IEEE Trans. On Elec. Dev*, 59, 2100, (2012)

[35] J. Robertson and L. Lin *Appl. Phys. Lett*. 99, 222906 (2011).

[36] S. Klejna and S. D. Elliott, *J. Phys. Chem*. C 116, 643-654 (2012).

[37] A. O'Mahony, S. Monaghan G. Provenzano, I.M. Povey, M.G. Nolan, E. O'Connor, K. Cherkaoui, S.B. Newcomb, F. Crupi, P. K. Hurley and M.E. Pemble, *Appl. Phys. Lett*. 97, 052904 (2010)

[38] R. Suzuki, N. Taoka, M. Yokoyama, S. Lee, S. H. Kim, T. Hoshii, T. Yasuda, W. Jevasuwan, T. Maeda, O. Ichikawa, N. Fukuhara, M. Hata, M. Takenaka, and S. Takagi, *Appl. Phys. Lett*. 100, 132906 (2012)

[39] É. O'Connor, B. Brennan, V. Djara, K. Cherkaoui, S. Monaghan, S. B. Newcomb, R. Contreras, M. Milojevic, G. Hughes, M. E. Pemble, R. M. Wallace, and P. K. Hurley, *Journal of Applied Physics*, 109, 024101 (2011)

[40] B. Brennan, M. Milojevic, C. L. Hinkle, F. S. Aguirre-Tostado, G. Hughes, and R. M. Wallace *Appl. Surf. Sci.* 257 (9), 4082, (2011)

[41] J. J. Gu, A. T. Neal, and P. D. Ye, *J. Appl. Phys.*, 99, 152113 (2011)

[42] V Djara, K Cherkaoui, S B Newcomb, K Thomas, E Pelucchi, D O'Connell, L Floyd, V Dimastrodonato, L O Mereni and P K Hurley, *Semicond. Sci. Technol.* 27 082001 (2012)

[43] V. Djara, K. Cherkaoui, M. Schmidt, S. Monaghan, É. O'Connor, I. M. Povey, D. O'Connell, M. E. Pemble, and P. K. Hurley, *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1084 - 1090, (2012).

[44] T.P. O'Regan, P.K. Hurley, B. Soree, M.V. Fischetti, *Appl. Phys. Lett*. 96, 213514 (2010)

[45] Eun Ji Kim, Lingquan Wang, Peter M. Asbeck, Krishna C. Saraswat, and Paul C. McIntyre, *Appl. Phys. Lett*. 96, 012906 (2010)

[46] T. Hoshii, M. Yokoyama, H. Yamada, M. Hata, T. Yasuda, M. Takenaka, and S. Takagi, *Appl. Phys. Lett.* 97, 132102 (2010)

[47] N. Goel, P. Majhi, W. Tsai, M. Warusawithana, D. G. Schlom, M. B. Santos, J. S. Harris and Y. Nishi, *Appl. Phys. Lett*. 91, 093509 (2007)

[48] Igor Krylov, Arkady Gavrilov, Dan Ritter, and Moshe Eizenberg, *Appl. Phys. Lett*. 99, 203504 (2011)

[49] Zhang P.F., Nagle R.E., Deepak N., Povey I.M., Gomeniuk Y.Y., O'Connor E., Petkov N., Schmidt M., O'Regan T.P., Cherkaoui K., Pemble M.E., Hurley P.K., Whatmore R.W. *Microelectronic Engineering*, 88, 7, 1054-1057 (2011)

[50] P. Masson, J. L. Autran, M. Houssa, X. Garros and C. Leroux, *Appl. Phys. Lett.,* 81 (18), 3392 (2002).

[51] E. O'Connor, Djara V., Monaghan S., Hurley P.K., Cherkaoui K. *ECS Transactions*, 35, 3 415-430 (2011)

[52] G. Brammertz, H.C. Lin, K. Martens, A. Alian, C. Merckling, J. Penaud, D. Kohen, W.-E Wang, S. Sioncke, A. Delabie, M. Meuris, M. Caymax, M. Heyns, *ECS Transactions*, 19 (5) 375-386 (2009)

[53] D. Varghese, Y. Xuan, Y. Q. Wu, T. Shen, P. D. Ye, and M. A. Alam, *Tech. Dig. - Int. Electron Devices Meet. p. 379 (*2008)

[54] Y.-C. Yeo, T.-J. King and C. Hu, *J. Appl. Phys.*, 92, 7266 (2002).

[55] Aneesh Nainani, Toshifumi Irisawa, Ze Yuan, Brian R. Bennett, J. Brad Boos, Yoshio Nishi, and Krishna C. Saraswat,, *IEEE Trans on Elec Dev*. 58, 3407 (2011)

[56] Scholten, J. J. F.; Pijpers, A. P.; Hustings, A. M. L. *Catal. Rev-Sci. Eng*. 1985, 27, 151-206.

[57] R. Castagne and A. Vapaille, *Surface Sci.*, 28, 557 (1971)

[58] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology,* Wiley, New York, 1982, p. 325.

[59] E. H. Nicollian and A. Goetzberger, *Bell Syst. Tech. J*. 46, 1055 (1967).

[60] E. H. Poindexter, G. J. Gerardi, M. Rueckel, and P. J. Caplan, *J. Appl. Phys.* 56, 2844 (1984)

[61] M. J. Uren, J. H. Stathis, and E. Cartier, *J. Appl. Phys.* 80, 3915 (1996)

[62] M. J. Uren, K. M. Brunson, J. H. Stathis, and E. Cartier, *Microelectron. Eng.* 36, 219 (1997)

[63] BJ O'Sullivan, PK Hurley, C Leveugle C, JH Das, *Journal of Applied Physics*, 89, 7, (2001), p3811.

[64] P.K.Hurley, B.J.O'Sullivan, F.N. Cubaynes, P.A. Stolk, F.P. Widdershoven and J.H.Das , *Journal of the Electrochemical Society*, 149, pp. 194-197 (2002)

[65] N.H. Thoan, K. Keunen, V.V. Afanas'ev and A. Stesmans, *J. Appl. Phys,* 109, 013710 (2011)

[66] G. J. Gerardi, E. H. Poindexter, M. E. Rueckel, and P. J. Caplan, *Appl. Phys. Lett*. 49, 348 (1986).

[67] A. Stesmans and V.V. Afanas'ev, *Appl. Phys. Lett.*, 80, 1957 (2002).

[68] Y.G. Fedorenko L. Truong, V.V. Afanas'ev, and A. Stesmans, *Applied Physics Letters,* 84, 4771 (2004).

[69] P.K. Hurley, K. Cherkaoui, S. McDonnell, G. Hughes and A.W. Groenland, *Microelectronics Reliability*, 47, (2007), 1195-1201

[70] P.K. Hurley, K. Cherkaoui, E. O'Connor, M.C. Lemme, H. D.B. Gottlob, M. Schmidt , S. Hall, Y. Lu, O. Buiu, B. Raeissi, J. Piscator, O. Engstrom and S.B. Newcomb, Journal of the Electrochemical Society, 155 (2) G13-G20 (2008)

[71] V. Djara, T.P. O'Regan, K. Cherkaoui, M. Schmidt, S. Monaghan, É. O'Connor, I.M. Povey, D. O'Connell, M.E. Pemble, P.K. Hurley, *Microelectronic Engineering* 109 182–188 (2013)

[72] Ali, A. ; Madan, H.; Koveshnikov, S.; Oktyabrsky, S.; Kambhampati, R.; Heeg, T.; Schlom, D.; Datta, S. *IEEE Trans. Electron Devices,* vol. 57, no. 4, pp. 742-748, Apr. 2010.

[73] H-P Komsa and A. Pasquarello *Microelectronic Engineering* 88 (2011) 1436–1439

[74] G. Brammertz, H.C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, *Appl Phys Lett.*, 95, 202109 (2009)

[75] Han-Ping Chen, Yu Yuan, Bo Yu, Jaesoo Ahn, Paul C. McIntyre, Peter M. Asbeck, Mark J. W. Rodwell, and Yuan Taur, *IEEE Transactions on Electron Devices* , 59, No. 9, 2383 (2012)

[76] N. Taoka, M. Yokoyama, S.H. Kim, R. Suzuki, R. Iida, S. Lee, T. Hoshii, W. Jevasuwan, T. Maeda, T. Yasuda, O. Ichikawa, N. Fukuhara, M. Hata, M.Takenaka and S.Takagi, *Proceedings of the IEEE International Electron Devices Meeting – IEDM*, p. 610 (2011)

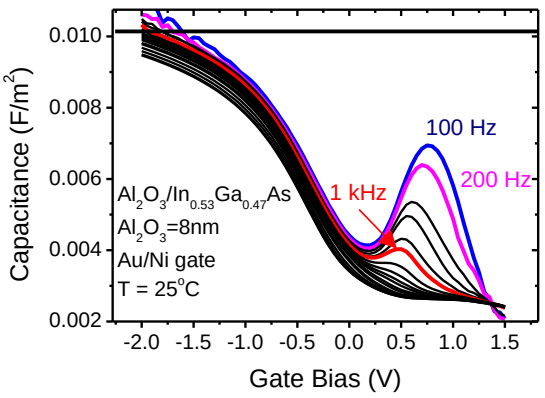
[77] M. Milojevic, R. Contreras-Guerrero, E. O'Connor, B. Brennan, P. K. Hurley, J. Kim, C. L. Hinkle and R. M. Wallace, *Appl. Phys. Lett.*, 99, 042904 (2011)

[78] E.J. Kim, E. Chagarov, J. Cagnon, Y. Yuan, A.C. Kummel, P.M. Asbeck, S. Stemmer, K.C. Saraswat, and P.C. McIntyre, *J. Appl. Phys.* 106, 124508-1-8 (2009).

[79] E. Yablonovitch, Bhat R, Harbison JP, Logan RA. *Appl. Phys. Lett.*, 51, 439 (1987)

[80] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*, Wiley, New York, 1982, p.145.

[81] H. C. Lin, W-E. Wang, G. Brammertz, M. Meuris, and M. Heyns, *Microelectron. Eng.* 86, 1554 (2009).



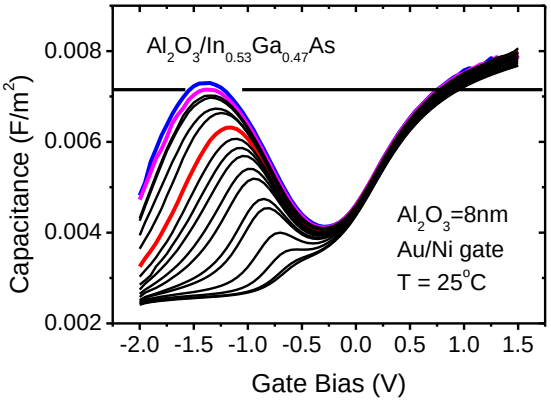
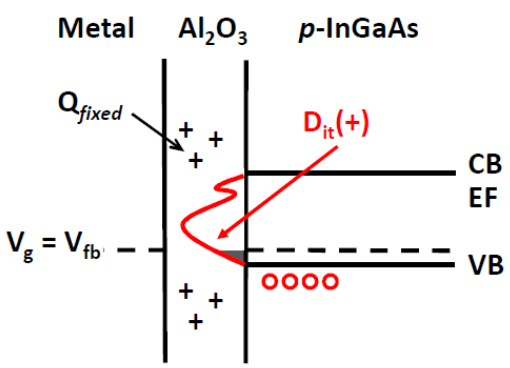
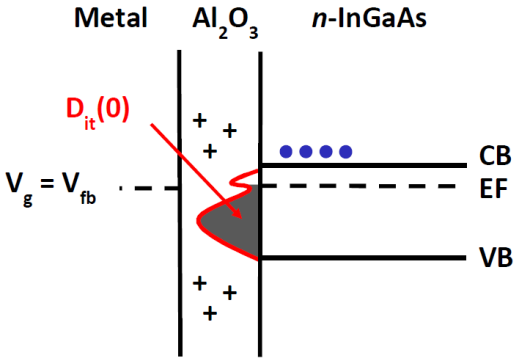


Figure 1 (a) Room temperature multi-frequency C-V (100 Hz to 100 kHz) for an Au/Ni/8nmAl_2O_3/n-$In_{0.53}Ga_{0.47}As$/InP MOS structure. The $In_{0.53}Ga_{0.47}As$ surface experienced a 10% $(NH_4)_2S$ surface preparation approach for 20 minutes and room temperature. The transfer time from the $(NH_4)_2S$ to the ALD reactor was 7 minutes. The black horizontal line represents the theoretical maximum low frequency capacitance calculated using a Poisson-Schrodinger C-V simulation based on the $In_{0.53}Ga_{0.47}As$ Γ Valley only.	Figure 1 (b) Room temperature multi-frequency C-V (100 Hz to 100 kHz) for the corresponding Au/Ni/8nmAl_2O_3/p-$In_{0.53}Ga_{0.47}As$/InP MOS structure. Surface preparation and transfer time as in Figure 1 (b). The black horizontal line represents the theoretical maximum low frequency capacitance calculated using a Poisson-Schrodinger C-V simulation based on the $In_{0.53}Ga_{0.47}As$ Γ Valley only.



$$V_{fbP} = (\phi_m - \phi_{sp}) - \frac{Q_{fixed}}{C_{ox}} - \frac{qD_{it}}{C_{ox}}$$



$$V_{fbN} = (\phi_m - \phi_{sn}) - \frac{Q_{fixed}}{C_{ox}}$$

Figure 2 (a) Schematic representation of the energy band diagram for the Al_2O_3/p-$In_{0.53}Ga_{0.47}As$ MOS structure at the flat band condition. The interface states are assumed donor type, and are predominantly unoccupied, and positively charged. The corresponding flat band voltage (V_{fbP}) for the structure is shown below the Figure, where ϕ_m is the work function of the metal gate, ϕ_{sp} is the work function of the *p*- type $In_{0.53}Ga_{0.47}As$, Q_{fixed} [cm^{-3}] is the positive fixed charge density in the Al_2O_3 , C_{ox} is the oxide capacitance per unit area [F/m^2] and D_{it} is the interface state distribution.

Figure 2 (b) Schematic representation of the energy band diagram for the Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOS structure at the flat band condition. The interface states are assumed donor type, and are predominantly occupied, and neutral. The corresponding flat band voltage (V_{fbN}) for the structure is shown below the Figure. ϕ_{sn} is the work function of the *n*-type $In_{0.53}Ga_{0.47}As$, and all other terms are as defined in Figure 2(a).

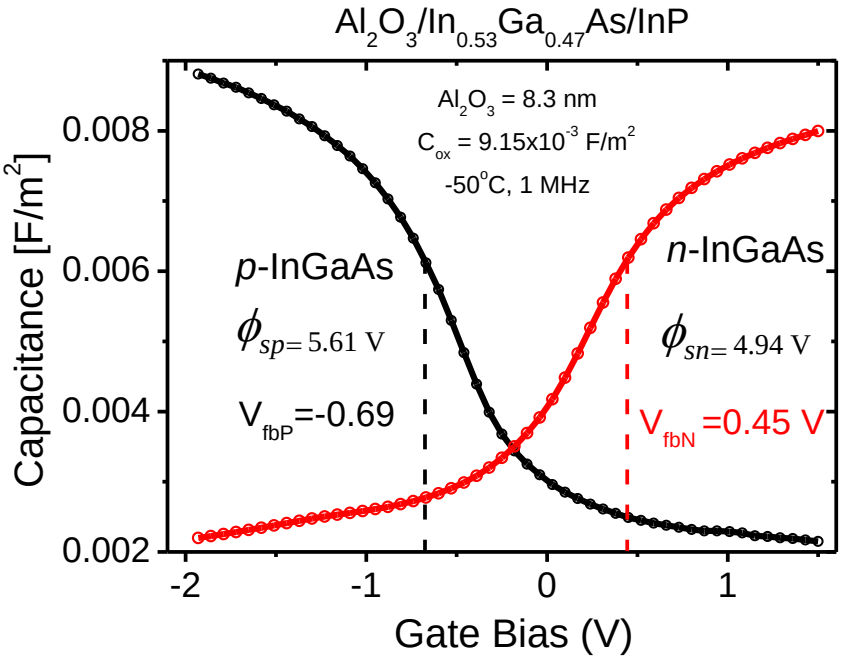


Figure 3. The C-V responses for the *n* and *p* type $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS structure recorded at 1 MHz and -50ºC to approximate to a high frequency C-V response (Note: these are the same sample as in Figures 2 (a) and 2 (b)). The flat band voltages for the *n* and *p* type $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS structures are shown in the figure. The difference in the flat band voltages relates to the integrated D_{it} across the $In_{0.53}Ga_{0.47}As$ energy gap, as indicated in equation (1), and yields a value of $2.7x10^{12}$ cm^{-2}.

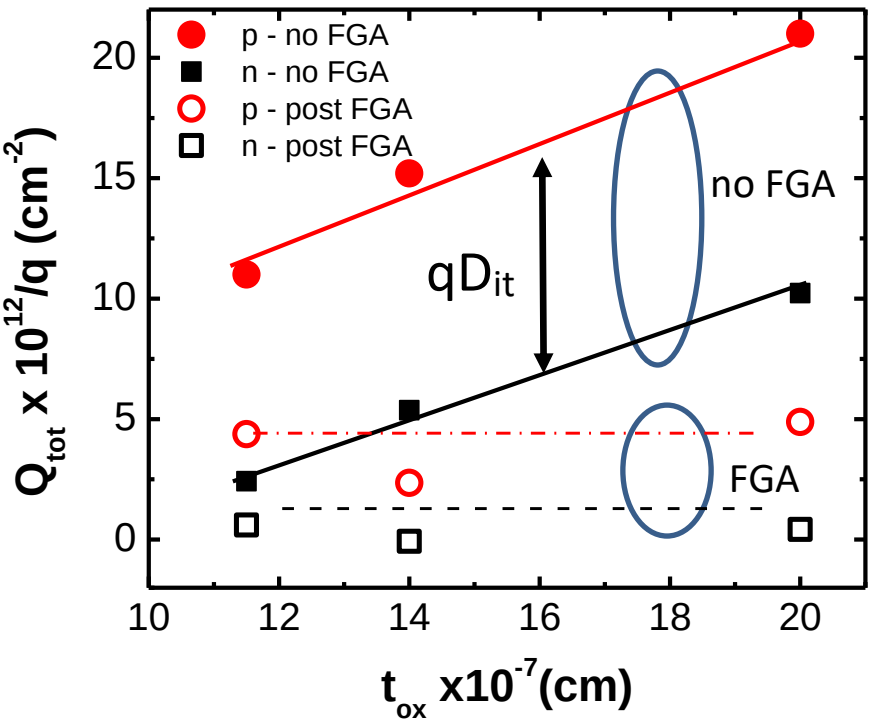


Figure 4. The total charge density as a function of Al_2O_3 thickness (11 nm to 20nm) determined for the flat band voltages of the *n* and *p* type Pt/Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOS structure recorded at 1 MHz and -50^{o}C. The results are shown prior to the 350^{o}C for 30 min. FGA (filled symbols) and post FGA (open symbols) for the *p*-type (red) and *n*-type (black) $In_{0.53}Ga_{0.47}As$ MOS samples. The difference between the total charge for the *p* and *n* type $In_{0.53}Ga_{0.47}As$ MOS is the integrated D_{it}, and the results indicate net donor type interface states.

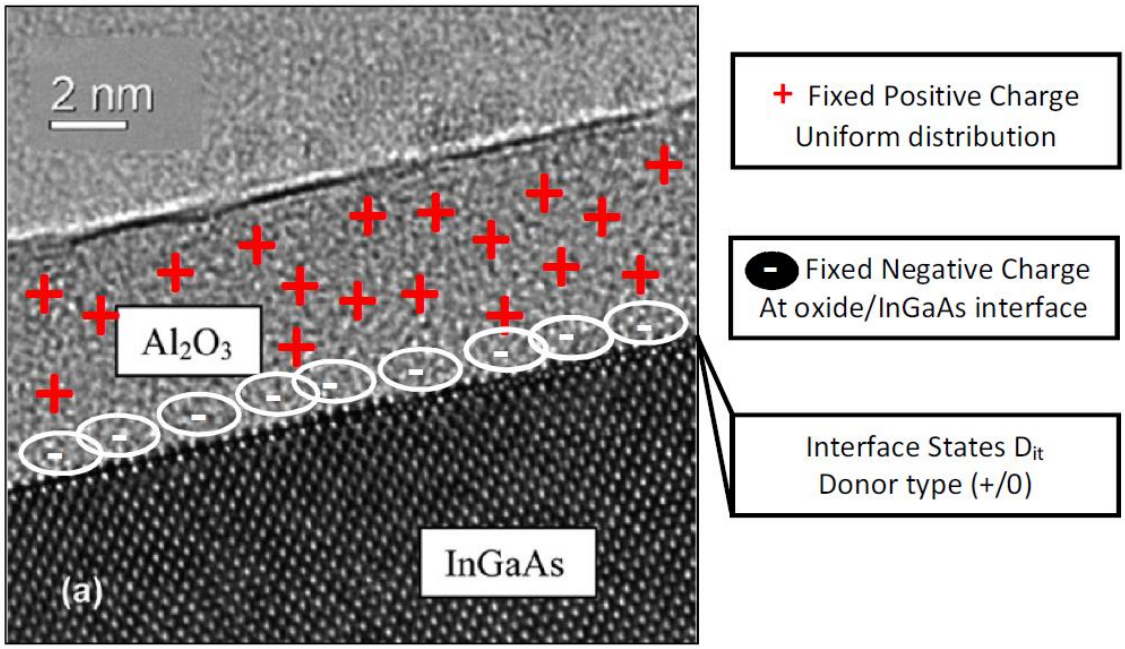
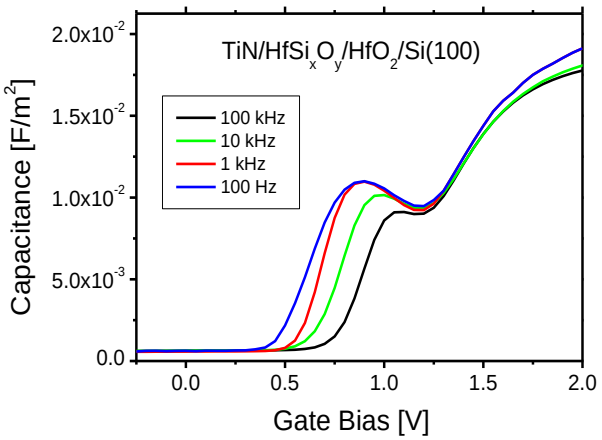


Figure 5. Transmission electron micrograph image of an $Al_2O_3/In_{0.53}Ga_{0.47}As$ structure illustrating the picture which emerges from the C-V analysis for fixed oxide charges and interface states.

Charge Component	Q_{ox}/q (cm^{-3})	Q_{int}/q (cm^{-2})	D_{it} (cm^{-2})
Pre FGA	9×10^{18}	-8×10^{12}	1×10^{13}
Post FGA	$<4 \times 10^{18}$	-7×10^{11}	5×10^{12}

Table 1. The values of the positive oxide charge (Q_{ox}) distributed through the Al_2O_3, the negative fixed charge near the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface (Q_{int}), and the interface state density (D_{it}) before and after the forming gas annealing process. Note: The Q_{fixed} in Figure 2 is comprised of the two terms Q_{ox} and Q_{int}. The term Q_{tot} in Figure 4 is the sum of Q_{fixed} and qD_{it}.



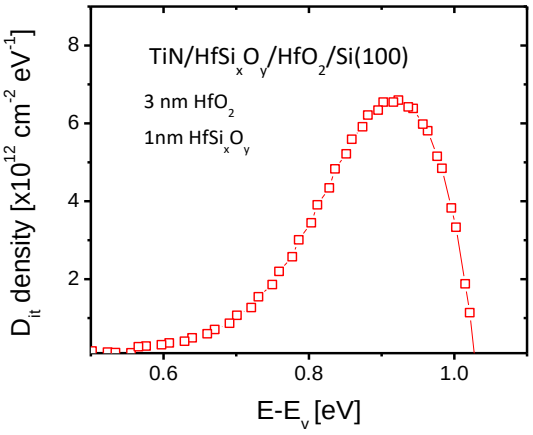
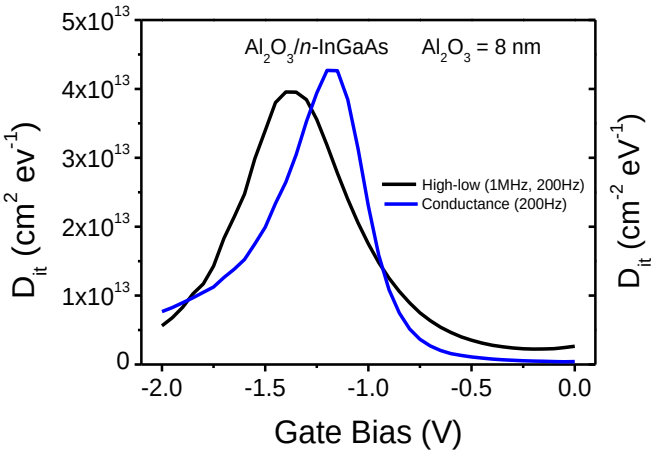


Figure 6 (a) Example multi-frequency (100Hz to 100 KHz) C-V response obtained for a (100)Si/SiO_x/HfO_2/$HfSi_xO_y$/TiN gate stack over n-type silicon. HfO_2 films by MOCVD. Measurements at 22^{o}C [69]. The samples experienced no final forming gas anneal, and have non-passivated silicon dangling bond defects (P_{b0}, P_{b1}).	Figure 6 (b) The corresponding interface state density profile determined in the upper half of the silicon energy gap. The energy (E) is with respect to the highest energy in the valence band, E_v.



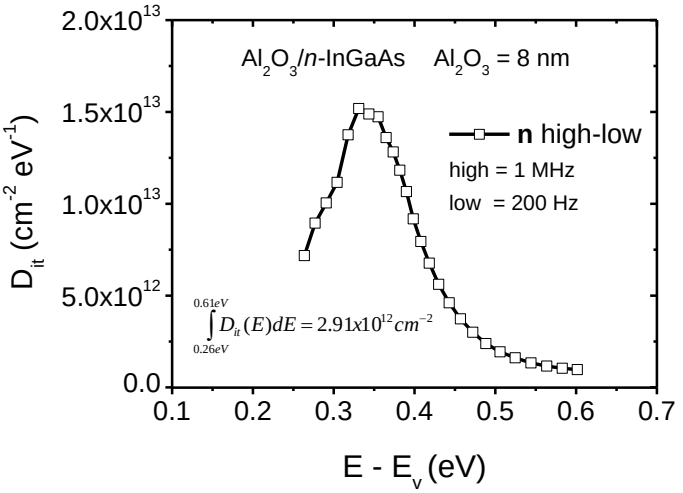


Figure 7 (a) Interface state density as a function of gate voltage obtained from the high-low C-V (1MHz, 200Hz) and conductance (200HZ) method, obtained from analysis of the Au/Ni/8nmAl_2O_3/p-$In_{0.53}Ga_{0.47}As$/InP MOS structure shown in Figure 1 (b). Note, the good agreement between the two separate approaches.	Figure 7 (b) The corresponding interface state density profile determined across the $In_{0.53}Ga_{0.47}As$ energy gap. The energy (E) is with respect to the highest energy in the valence band, E_v. The interface state distribution exhibits a peak density of $1.5x10^{13}$ $cm^{-2}eV^{-1}$ at 0.35eV above the valence band edge. The interface density in units of [cm^{-2}] is obtained through the integral of the curve. The integrated density from 0.26eV to 0.61eV yields a value of $2.9x10^{12}$ cm^{-2}. Note, this integrated density is in good agreement with the value of $2.7x10^{12}$ cm^{-2} obtained from the same samples using the charge separation approach at V_{fb}, as shown in Figure 3.

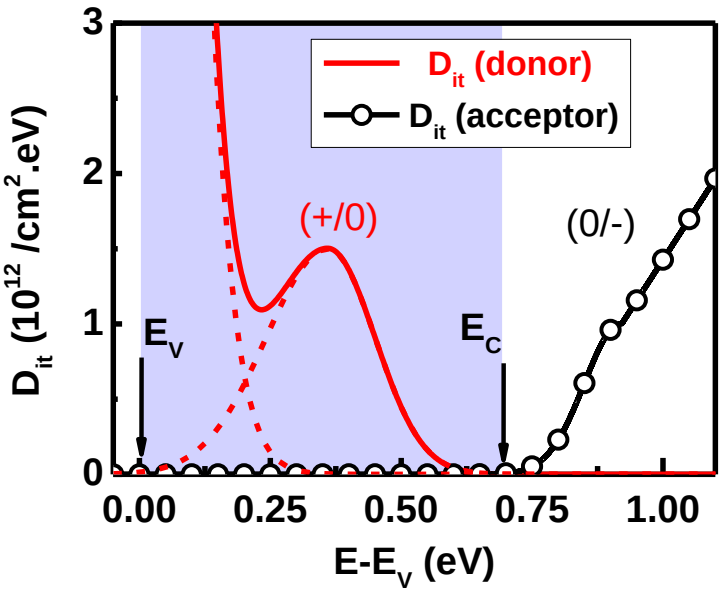


Figure 8. The energy distribution of interface states for the $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS system based on analysis of the full gate capacitance of the surface *n*-channel $In_{0.53}Ga_{0.47}As$ MOS transistors in conjunction with Poisson-Schrodinger C-V simulation.

High-*k* Oxide	Peak D_{it} ($cm^{-2}eV^{-1}$)	Energy of Peak D_{it} (eV)	Reference
$LaAlO_3$	4×10^{13}	E_v+0.45	[73]
$SrTa_2O_6$	2.5×10^{13}	E_v+0.30	[48]
Al_2O_3/HfO_2	6×10^{12}	E_v+0.40	[26]
Al_2O_3	1.5×10^{13}	E_v+0.36	[this work, & 72]

Table 2 The peak interface state density, and the energy of the peak density with reference to $E_{V,}$ reported for various high-*k* oxides on $In_{0.53}Ga_{0.47}As$.

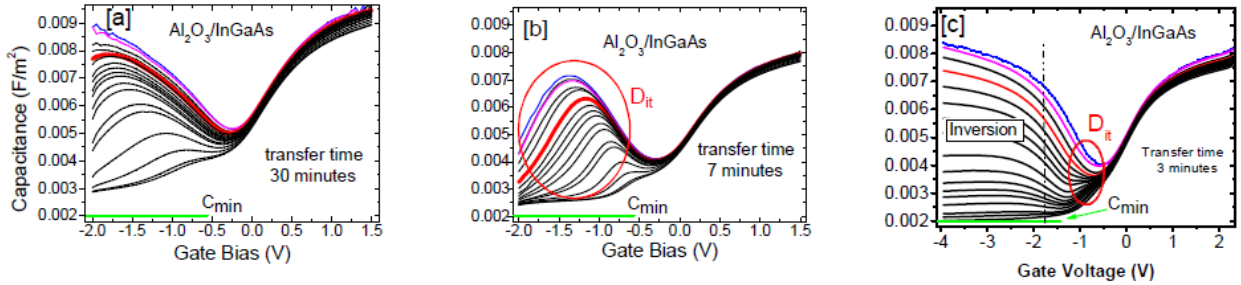
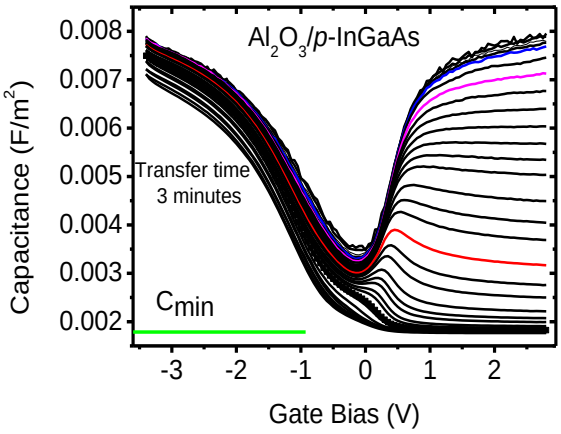


Figure 9 Room temperature multi-frequency C-V responses (from 100 Hz to 100 kHz) for Al_2O_3(8nm)/n-$In_{0.53}Ga_{0.47}As$/InP MOS structures with Au/Ni gates. The $In_{0.53}Ga_{0.47}As$ surface experienced a 10% $(NH_4)_2S$ surface preparation approach for 20 minutes and room temperature. Results are shown for varying transfer times from the 10% $(NH_4)_2S$ solution to the ALD reactor of (a) 30 minutes, (b) 7 minutes and (c) 3 minutes. The samples illustrate the effect of a progressive reduction of D_{it} and the emergence of surface inversion for the case of the 3 minute transfer time in Figure 9 (c).



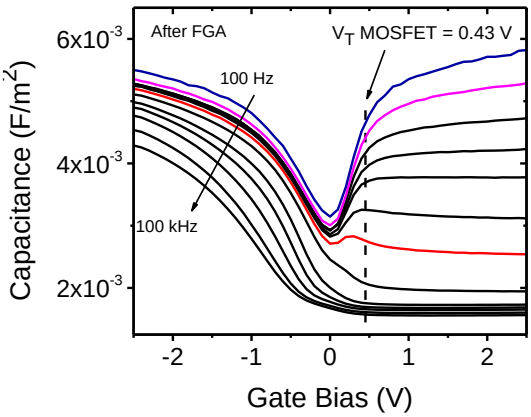


Figure 10 (a) Room temperature multi-frequency C-V responses (from 20 Hz to 100 kHz) for Al_2O_3(8nm)/p-$In_{0.53}Ga_{0.47}As$/InP MOS structures with Au/Ni gates. The $In_{0.53}Ga_{0.47}As$ surface experienced a 10% $(NH_4)_2S$ surface preparation approach for 20 minutes and room temperature. Transfer time = 3 minutes. This is the p-$In_{0.53}Ga_{0.47}As$ sample corresponding to the p-$In_{0.53}Ga_{0.47}As$ sample in Figure 9 (c).

Figure 10 (b) Room temperature C-V responses (from 100 Hz to 100 kHz) for an Al_2O_3(8nm)/p-$In_{0.53}Ga_{0.47}As$/InP MOS capacitor from the full surface channel $In_{0.53}Ga_{0.47}As$ MOSFET process. The threshold voltage of the neighboring MOSFET (0.43 V) is shown in the Figure. The CV response for a gate bias > 0.43 V is the C-V response for the Al_2O_3/p-$In_{0.53}Ga_{0.47}As$ interface in inversion.