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## Structural and electrical analysis of the atomic layer deposition of $HfO_2/n-In_{0.53}Ga_{0.47}As$ capacitors with and without an $Al_2O_3$ interface control layer

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## Structural and electrical analysis of the atomic layer deposition of $HfO_2/n-In_{0.53}Ga_{0.47}As$ capacitors with and without an $Al_2O_3$ interface control layer

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High mobility III-V substrates with high-*k* oxides are required for device scaling without loss of channel mobility. Interest has focused on the *self-cleaning* effect on selected III-V substrates during atomic layer deposition of Al<sub>2</sub>O<sub>3</sub>. A thin (~1 nm) Al<sub>2</sub>O<sub>3</sub> interface control layer is deposited on In<sub>0.53</sub>Ga<sub>0.47</sub>As prior to HfO<sub>2</sub> growth, providing the benefit of *self-cleaning* and improving the interface quality by reducing interface state defect densities by ~50% while maintaining scaling trends. Significant reductions in leakage current density and increased breakdown voltage are found, indicative of a band structure improvement due to the reduction/removal of the In<sub>0.53</sub>Ga<sub>0.47</sub>As native oxides. © *2010 American Institute of Physics*. [doi:10.1063/1.3473773]

A critical technological challenge in the integration of high k-dielectrics on III-V channels is the control of the high-k/III-V interface. Although the interfacial chemistry of the high-k/Si system is similar to the SiO<sub>2</sub>/Si system,<sup>1</sup> the high-k/III-V system is more complex, due to competition between the various native oxide species at the interface,<sup>2</sup> resulting in growth of a poor quality interfacial layer.<sup>3–6</sup> In recent work,<sup>3</sup> reductions in interface state defect densities  $(D_{it})$  were achieved by pre-treatment of the In<sub>0.53</sub>Ga<sub>0.47</sub>As surface prior to atomic layer deposition (ALD) of HfO<sub>2</sub>  $[k \sim 16-25$ , band gap  $(E_o) \sim 5.8-6.0$  eV].<sup>7-9</sup> The native oxides of In<sub>0.53</sub>Ga<sub>0.47</sub>As (Ga<sub>2</sub>O<sub>3</sub>, In<sub>2</sub>O<sub>3</sub>, and As<sub>2</sub>O<sub>3</sub>) have low band gaps (3.6-4.8 eV) (Refs. 2 and 9) and k-values of 8-10 when relating the reported<sup>9,10</sup> k-value for  $Ga_2O_3$  and  $In_2O_3$ with the approximate refractive indices  $(n \sim 1.9 \text{ for all})^2$ through the equation  $n^2 \propto k$  and the Moss Inverse Law<sup>11</sup> for the refractive index, k-value and energy band gap. They are detrimental to the band structure of high-k/III-V devices by increasing the leakage current and creating potential wells in the native oxide layer between the high-k oxide and the substrate. The self-cleaning Al<sub>2</sub>O<sub>3</sub> ALD process is reported to reduce or remove the III-V native oxides.<sup>12-15</sup> However, devices employing Al<sub>2</sub>O<sub>3</sub> ( $k \sim 8.6-11.6, E_{o} \sim 8.8 \text{ eV}$ ) (Refs. 8, 9, and 12) as the gate oxide are limited for scaling due to its low k-value.

In this work, the structural and electrical properties of Pd/HfO<sub>2</sub>/*n*-In<sub>0.53</sub>Ga<sub>0.47</sub>As devices (HfO<sub>2</sub>: nominal thickness  $\sim$ 3,  $\sim$ 4, and  $\sim$ 5 nm) with/without an  $\sim$ 1 nm Al<sub>2</sub>O<sub>3</sub> interface control layer (ICL), are examined using high resolution transmission electron microscopy (HR-TEM) and current/capacitance/conductance versus voltage measurements (JV, CV, and GV, respectively). The devices are labeled: *s*1\_3, *s*1\_4, *s*1\_5 (e.g., sample,  $\sim$ 1 nm Al<sub>2</sub>O<sub>3</sub>,  $\sim$ 5 nm HfO<sub>2</sub> is labeled *s*1\_5). As a control, devices were fabricated without the Al<sub>2</sub>O<sub>3</sub> ICL [nominal  $\sim$ 5 nm HfO<sub>2</sub> only (label:

 $s0_5$ ]. The motivation for this work is: (i) to detect any improvement in the quality and structure of the interface using the bilayer approach; (ii) to investigate if an Al<sub>2</sub>O<sub>3</sub> ICL improves the electrical performance of devices by modifying the metal-oxide-semiconductor (MOS) band structure; (iii) to determine if scaling is possible with an Al<sub>2</sub>O<sub>3</sub> ICL using reducing thicknesses of HfO<sub>2</sub>.

The  $\sim 2 \ \mu m \ n$ -type (S:  $\sim 4 \times 10^{17} \ cm^{-3}$ ) In<sub>0.53</sub>Ga<sub>0.47</sub>As channels had a  $\sim 0.1 \ \mu m$  InP buffer layer (S:  $\sim 2$  $\times 10^{18}$  cm<sup>-3</sup>) on a ~350  $\mu$ m InP substrate (S:3-8  $\times 10^{18}$  cm<sup>-3</sup>). All In<sub>0.53</sub>Ga<sub>0.47</sub>As layers were grown by MOVPE. An ex situ three-stage surface pre-treatment process [HCl, NH<sub>4</sub>OH, and  $(NH_4)_2S$ ] was performed on the n-In<sub>0.53</sub>Ga<sub>0.47</sub>As/InP substrates which has previously been shown to be beneficial to device performance.<sup>3</sup> The  $Al_2O_3$ and HfO<sub>2</sub> layers were deposited in a Cambridge NanoTech Fiji F200LLC ALD system, at 250 °C. The ALD of Al<sub>2</sub>O<sub>3</sub> and HfO<sub>2</sub> employed alternating pulses of TMA  $[Al(CH_3)_3]/H_2O$  and tetrakis(ethylmethylamino)hafnium (TEMAH) {Hf[N( $C_2H_5$ )(CH<sub>3</sub>)]<sub>4</sub>}/H<sub>2</sub>O, respectively. MOS structures were completed by vacuum evaporation of  $\sim$ 200 nm of Pd at a deposition rate of 2.5 Å/s using a lift-off process. No ohmic back contacts were formed.

Figures 1(a) and 1(b) present cross-sectional HR-TEM micrographs of  $s1_5$  and  $s0_5$ , confirming the physical oxide and nominal thicknesses are in close agreement:  $s1_5$  [Fig. 1(a)] has a ~5.3 nm HfO<sub>2</sub> layer, and a ~1.2 nm Al<sub>2</sub>O<sub>3</sub> layer.  $s0_5$  [Fig. 1(b)], has a ~4.9 nm HfO<sub>2</sub> layer. All oxide layers are amorphous. Comparison between Figs. 1(a) and 1(b) shows a ~0.7 nm native oxide layer at the high-k/n-In<sub>0.53</sub>Ga<sub>0.47</sub>As interface when no Al<sub>2</sub>O<sub>3</sub> ICL is deposited, which is indicative of an Al<sub>2</sub>O<sub>3</sub> self-cleaning effect on the native oxide, for sample  $s1_5$ .

Figure 2(a) presents a cross-sectional HR-TEM micrograph of  $s1_3$ . The physical thicknesses of HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> are ~3.2 nm and ~1.2 nm, respectively. Figure 2(b), a plan-view HR-TEM micrograph for sample  $s1_5$ , reveals the epitaxial 2  $\mu$ m n-In<sub>0.53</sub>Ga<sub>0.47</sub>As layer to be defect-free,

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FIG. 1. Cross-sectional HR-TEM micrographs of (a)  $s1_5$ , with ~5.3 nm HfO<sub>2</sub> and ~1.1 nm Al<sub>2</sub>O<sub>3</sub> and (b)  $s0_5$ , with ~4.9 nm HfO<sub>2</sub> and a ~0.7 nm native oxide layer.

with an associated negligible root mean square (rms) surface roughness of <1 nm.

Figure 3 shows (a) JV responses and (b) the measured 1 kHz CV responses, along with the simulated<sup>16</sup> CV curves for all samples. The inset to Fig. 3(a) shows the capacitance equivalent thickness (CET) versus HR-TEM extracted HfO<sub>2</sub> physical thickness plot for the bilayer sample set  $(s1_3, s1_4, s1_5)$ , with a linear fit. Figure 3(a), when assessing the bilayer sample set only, shows that leakage current density increases with reducing HfO<sub>2</sub> thickness, and the dielectric breakdown voltage increases with increasing HfO2 thickness. This is expected for a dominant quantummechanical (QM) tunneling leakage mechanism with similar energy barrier height and shape, and for a dominant electrically-controlled oxide breakdown process.<sup>17</sup> However, the leakage current density response for sample s0 5 is substantially higher (approximately three orders of magnitude at 3 V) than for sample  $s1_5$ , showing that the absence of an Al<sub>2</sub>O<sub>3</sub> ICL changes the tunneling barrier height/shape to conduction beyond a thickness-dependency regime only and introduces an additional, highly temperature-dependent (not shown), trap-assisted conduction mechanism that adds magnitude and fluctuation to the response.<sup>18</sup> Figure 3(b) shows that the accumulation maximum capacitance at 2 V scales correctly with oxide thickness for the bilayer sample set. The simulated curves confirm that surface accumulation is achieved at 2 V for all samples.<sup>3</sup> The accumulation maximum capacitance is greater for the measured data compared to the simulated data, showing the existence of a QM correction factor. This difference could be due to additional states inside the conduction band at the oxide/ $n-In_{0.53}Ga_{0.47}As$ 



FIG. 2. HR-TEM micrographs of (a)  $s_{1_3}$  (cross-sectional), with  $\sim 3.2$  nm HfO<sub>2</sub> and  $\sim 1.2$  nm Al<sub>2</sub>O<sub>3</sub>; (b)  $s_{1_5}$  (plan-view) shows a defect free n-In<sub>0.53</sub>Ga<sub>0.47</sub>As substrate layer.



FIG. 3. (Color online) (a) JV responses for all samples, with significantly lower leakage for the  $s1_5$  (Al<sub>2</sub>O<sub>3</sub> ICL) devices, compared to  $s0_5$  devices. (b) Measured and simulated (from the 1D Poisson–Schrödinger solver) 1 kHz CV responses for all samples. Inset to (a) shows the CET vs physical thickness with a linear fit.

interface,<sup>19</sup> and/or charge quantization leading to X and L satellite valley occupation in the conduction band.<sup>20</sup> We see a similar maximum accumulation capacitance for the  $\sim 5$  nm HfO<sub>2</sub> samples with/without Al<sub>2</sub>O<sub>3</sub> (s1\_5 and s0\_5, respectively), showing that the overall equivalent oxide thickness of these oxide stacks are similar. The observed variation in the maximum accumulation capacitance ( $\sim 0.003 \text{ F/m}^2$ ) for sample s0\_5 is likely due to native oxide layer thickness variation not observable by HR-TEM. Given the large difference in leakage current density between these samples  $(s1_5$ and  $s0_5$ , it is evident that the Al<sub>2</sub>O<sub>3</sub> ICL substantially reduces the native oxide layer thickness while increasing the barrier height to electron tunneling from the In<sub>0.53</sub>Ga<sub>0.47</sub>As conduction band. The linear fit of the inset to Fig. 3(a) shows that the reduction in HfO<sub>2</sub> thickness for the bilayer structures produces the required scaling trend. This linear fit can be used to extract an intercept CET value, which has contributions from Al<sub>2</sub>O<sub>3</sub>, any underlying native oxide layer (if present), and the QM correction contribution from the *n*-In<sub>0.53</sub>Ga<sub>0.47</sub>As accumulation layer. HR-TEM [Figs. 1(a), 1(b), and 2(a)], in combination with the electrical results [Figs. 3(a), 3(b), 4(a), and 4(b)], indicate that no substantive underlying native oxide layer is present for the bilayer sample set. Assuming this is the case and since we can extract the contributions from  $Al_2O_3$ , we can thereby determine a QM correction factor of  $\sim 0.7$  nm. From the slope of the linear fit we can estimate the HfO<sub>2</sub> k-value to be  $\sim$ 20, which is within the reported range.<sup>7</sup> Reasonable assumptions used were: (i) the k-value of both  $Al_2O_3$  and any native oxide<sup>2,10,12</sup> layer is  $\sim 9$  and (ii) the physical thicknesses used for sample s1\_4 are nominal thicknesses proportionally corrected using HR-TEM/nominal-thickness ratios and ALD cycle ratios for other samples. The absence of an underlying native oxide



FIG. 4. (Color online) (a) and (b) show CV responses (20 frequencies; 1 kHz–1 MHz) for samples  $s0_5$  and  $s1_5$ , respectively. The insets to (a) and (b) show the corresponding GV responses.

layer, evidenced by HR-TEM in combination with the electrical results, indicates that the  $Al_2O_3$  is likely to be removing the native oxides via the *self-cleaning* process.

Figures 4(a) and 4(b) show the multifrequency CV responses for samples  $s0_5$  and  $s1_5$ , respectively. The insets to Figs. 4(a) and 4(b) show the corresponding GV responses. We observe an increased D<sub>it</sub> response in both the CV and GV profiles for sample s0 5 when compared to the equivalent response for sample s1\_5, which includes (over the entire voltage range) an increased CV and GV stretch-out and frequency dispersion. In the voltage range -1 to 0.25 V, the absence of minority carriers is assumed, corresponding to the depletion regime. An approximation to the Conductance Method<sup>21</sup> indicates that samples  $s0_5$  and  $s1_5$  have estimated  $D_{it}$  values of  $\sim 8 \times 10^{12}$  cm<sup>-2</sup> eV<sup>-1</sup> and  $\sim 4 \times 10^{12}$  cm<sup>-2</sup> eV<sup>-1</sup>, respectively. Due to the absence of distinct equivalent parallel conductance  $(G_p/\omega)$  peaks as observed in SiO<sub>2</sub>/Si systems, this is derived assuming zero standard deviation in band bending using values of  $G_p/\omega$  at -1 V and taken at 30 kHz. While it is noted that the  $G_p/\omega$ magnitudes may be affected by the approximation conditions, and any possible minority carrier contribution, the relative difference provides a valid estimate. There is approximately a 50% reduction in  $D_{it}$  when including an  $Al_2O_3$ ICL.

In summary, it is found that the inclusion of a thin  $Al_2O_3$  ICL (~1 nm) at the  $HfO_2/In_{0.53}Ga_{0.47}As$  interface improves the structural and electrical properties of Pd/HfO<sub>2</sub>/*n*-In<sub>0.53</sub>Ga<sub>0.47</sub>As devices. The inclusion of the  $Al_2O_3$  ICL improves the breakdown voltage and reduces leakage current densities by approximately three orders of

magnitude at 3 V by increasing the barrier height to tunneling from the  $In_{0.53}Ga_{0.47}As$  conduction band into the oxide. No apparent native oxide layer is observed at the high- $k/In_{0.53}Ga_{0.47}As$  interface when using an  $Al_2O_3$  ICL, suggesting that the  $Al_2O_3$  ALD process is *self-cleaning* the  $In_{0.53}Ga_{0.47}As$  native oxides. Comparing the electrical performance for the bilayer samples with different HfO<sub>2</sub> thicknesses we find that device scaling trends can be achieved. Combining the structural and electrical results we find a QM correction factor of ~0.7 nm. The inclusion of an ICL causes an approximate 50% reduction in  $D_{it}$ , thereby improving the quality of the interface.

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