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Two mm-Wave Vector Modulator Active Phase Shifters With Novel IQ Generator in 28 nm FDSOI CMOS

Domenico Pepe, *Member, IEEE*, and Domenico Zito, *Senior Member, IEEE*

***Abstract*— This paper presents two 4-bit (16-phase) mm-wave vector modulator phase shifters exploiting a novel in-phase and quadrature signal generator that consists of a single-input double-output cascode amplifier incorporating a lumped-element coupled-line quadrature coupler. The two circuit implementations have been designed and fabricated in a 28 nm fully depleted silicon-on-insulator CMOS. The first (PS1) achieves a higher gain and the second (PS2) has a more compact area (reduced to about 50%). Each consumes 18 mA from a 1.2 V supply. PS1 exhibits an average gain of 2.3 dB at 87.4 GHz and B_{3dB} from 78.8 to 92.8 GHz; rms gain error of 1.68 dB at 87.4 GHz and <2 dB in the B_{3dB}; rms phase error of 9.4° at 87.4 GHz and <11.9° in B_{3dB}; $S_{11} < -10.5$ dB in B_{3dB}; average P_{1dB} of −7 dBm; and average noise figure (NF) equal to 10.8 dB at 87 GHz. PS2 exhibits an average gain of 0.83 dB at 89.2 GHz and B_{3dB} from 80.2 to 96.8 GHz; rms gain error of 1.46 dB at 89.2 GHz and <2 dB in B_{3dB}; rms phase error of 11.2° at 89.2 GHz and <11.9° in B_{3dB}; $S_{11} < -11.5$ dB in B_{3dB}; average P_{1dB} of −6 dBm; and average NF of 11.9 dB at 89 GHz.**

***Index Terms*— 28 nm fully depleted silicon-on-insulator (FDSOI) CMOS, phase shifter, phased array, quadrature coupler, vector modulator, *W*-band.**

I. Introduction

PHASED array systems will be crucial in future wireless communication and sensing applications [1]–[11]. They are employed in communication systems to obtain steerable directional antenna patterns in order to improve the link budget and in radars and imagers to electronically scan a targeted surface.

Beamforming can be performed at different sections of the receiver and transmitter chains: 1) in the radio frequency (RF) path [12], [13]; 2) in the local oscillator path [14], [15]; 3) in the baseband [16], [17]; and 4) in the digital domain [18]. One of the most promising phase shifting techniques for mm-waves is phase shifting in the RF path, since with respect to 2), it allows a wider operating bandwidth, and with respect to 3) and 4), it allows sharing all building blocks after the phase shifters, leading to considerable power and area savings. Moreover, in the RF path the reactive elements (inductors and capacitors) are smaller than they would be at the intermediate frequency or baseband, enabling a more compact design.

Phase shifters can be passive or active. Passive phase shifters, such as switched *LC*-networks [19], reflective-type phase shifters [20], and loaded line phase shifters [1], [21], typically exhibit high linearity performance but also high losses, high noise figure (NF), and large area on chip. Active phase shifters, such as vector modulators [22], typically exhibit higher gain compared with passive counterparts, smaller area on chip, and higher phase shift resolution, at the expense of lower linearity performance [23].

This paper presents two vector modulator active phase shifters with a novel in-phase/quadrature (IQ) signal generator, enabling higher gain, lower NF, and a more compact design with respect to the state of the art, to be used in a *W*-band phased array passive imager. For this specific application linearity is not a stringent requirement, but gain and NF are critical in order to have a good system resolution [4].

The idea and proof of concept have been presented recently [24]. In this paper, we extend the previous conference paper by: 1) reporting additional results; 2) addressing the circuit analysis and design; 3) detailing the experimental setups and measurement steps; and 4) presenting a second and new test-chip implementation for a more compact design enabling the effective integration of large arrays. The two phase shifters have been designed and implemented in a 28 nm fully depleted silicon-on-insulator (FDSOI) CMOS technology by STMicroelectronics, and characterized experimentally by means of direct on-chip measurements.

This paper is organized as follows. In Section II, the proposed IQ signal generator is presented and its operating principle is explained and analyzed in detail. In Section III, the design of the two mm-wave active phase shifters is addressed. In Section IV, the results of their experimental characterizations are reported. In Section V, the conclusions are drawn. The noise analysis is given in the Appendix.

II. Proposed IQ Generator for Active Phase Shifters

Fig. 1(a) shows the block diagram of a vector modulator active phase shifter. The vector modulator phase shifter is based on an IQ signal generator and two variable gain amplifiers (VGAs).

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D. Pepe is with the Dipartimento di Scienze e Metodi dell'Ingegneria, Università di Modena e Reggio Emilia, 42122 Reggio Emilia, Italy and also with the Tyndall National Institute, T12 R5CP Cork, Ireland (e-mail: domenico.pepe@ieee.org).

D. Zito was with the University College Cork, College Road, T1 YN60 Cork, Ireland, and also with the Tyndall National Institute, T12 R5CP Cork, Ireland. He is now with the Department of Engineering, Aarhus University, Finlandsgade 22, 8200 Aarhus N, Denmark (e-mail: domenico.zito@eng.au.dk).

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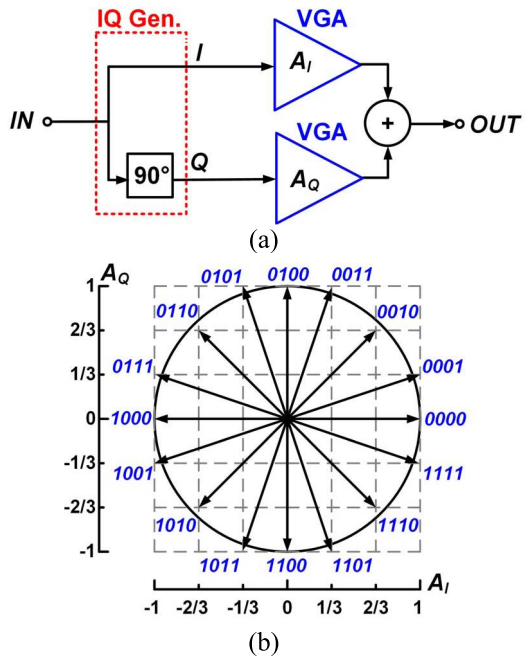


Fig. 1. (a) Block diagram of a vector modulator phase shifter. (b) Phase selection diagram as a function of the DGS input bits.

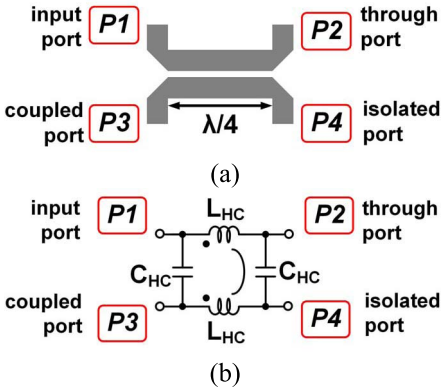


Fig. 2. (a) Coupled line quadrature coupler. (b) Lumped implementation.

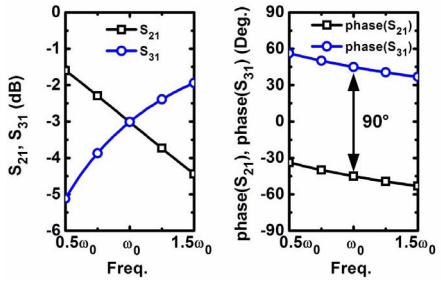


Fig. 3. Simulated absolute value and phase of S_{21} and S_{31} of the circuit in Fig. 2(b).

The I and Q components of the input signal are weighted by algebraic coefficients by properly choosing the gains A_I and A_Q of the two VGAs in order to have the desired phase shift. The polar diagram of the output phase is shown in Fig. 1(b), for the case of a 16-phase full-360° phase shifter. By properly choosing the normalized gains A_I and A_Q equal to -1, $-2/3$, $-1/3$, 0, 1, 1/3, 2/3, 1 it is possible to select any phase shift from 0° to 360° with a 22.5° resolution.

The IQ signal generator is a crucial building block of the vector modulator. The most widespread methods to obtain a 90° shift are the use of delay lines [1], [21], polyphase filters [25], or quadrature couplers [26], [27]. All-pass polyphase filters and quadrature couplers usually exhibit relevant losses, which impair the NF of the receiver. Delay lines generally introduce lower losses, but the attenuation in the delayed path can lead to imbalance between I and Q channels. For particular applications, for example, passive imaging [4], [5], minimizing losses, and NF contribution in the receiver chain, usually at the expense of reduced linearity performance, is very often an imperative requirement.

The IQ generator combines signal amplification and quadrature phase shifting by embedding a lumped-element coupled-line quadrature coupler (LECLQC) into a single-input double-output cascode amplifier, i.e., it consists of a cascode amplifier with one input (in) and two outputs (I and Q), with an interstage LECLQC between the input common-source (CS) transistor and the output common-gate transistors. Compared with passive IQ generator, it allows better coupler port isolation, lower losses, and lower NF.

In order to explain the operating principle, first we consider the coupled line quadrature coupler shown in Fig. 2(a). When the mutual coupling between the lines approaches unity, and all the ports are terminated with the line characteristic impedance Z_0, if an excitation is applied to the input port (P1), then the signal splits into two signals that are 90° apart in phase at the through (P2) and coupled (P3) ports. No power flows through the isolated port (P4).

Fig. 2(b) shows the lumped element implementation of the LECLQC [28]–[32], where

$$L_{\mathrm{HC}} = \frac{Z_0}{\omega_0} \tag{1}$$

$$C_{\mathrm{HC}} = \frac{1}{2 \cdot Z_0 \cdot \omega_0} \tag{2}$$

and ω_0 is the operating angular frequency in rad/s. Fig. 3 gives the S_{21} and S_{31} parameters (magnitude and phase) of the circuit of Fig. 2(b). Note that at ω_0, the signal power splits equally into the through and coupled ports and the phase difference is 90°.

Fig. 4 shows the schematic of the proposed IQ signal generator. The input signal is amplified by M_1. The isolated port of the LECLQC is connected to the drain of M_2. M_2 also allows the correct dc biasing of the Q branch (M_4). The coupled and through ports of the LECLQC are connected to the sources of M_3 and M_4. The impedances seen toward the drain of M_1 and M_2 and the source of M_4 and M_3 can be adjusted by varying the transistor sizes and bias currents.

Fig. 5 shows the small-signal equivalent circuit for noise and signal analyses of the IQ signal generator, where the gate-drain capacitance C_{GD} and the gate resistance R_G of M_1 have been neglected in the interests of simplicity. Z_S is the impedance seen toward the source of M_3 and M_4, whereas Z_D is the impedance seen toward the drain of M_1 and M_2.

In order to show the impact of the transistor size and bias current on Z_D and Z_S, circuit simulations have been carried out in a 28 nm FDSOI CMOS. Fig. 6(a)–(d) shows how Z_D and Z_S vary with the transistor size and bias current

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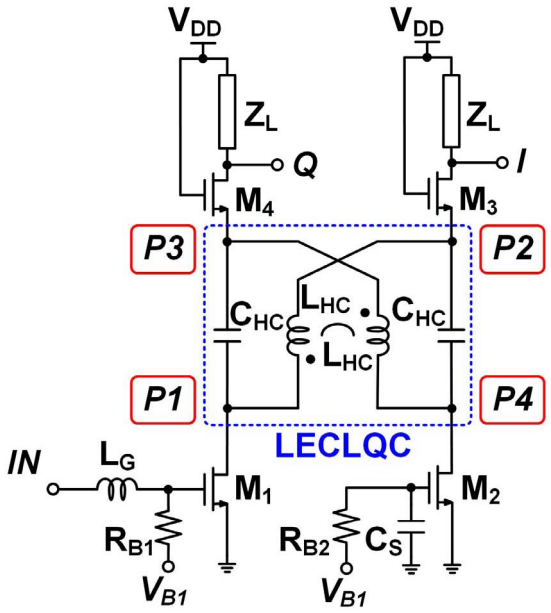


Fig. 4. Schematic of the IQ signal generator, exploiting the LECLQC (in the dotted box) to generate in-phase and quadrature signals.

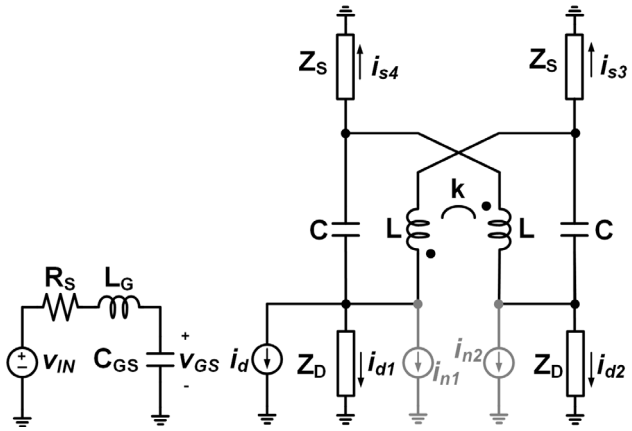


Fig. 5. Small-signal equivalent circuit of the IQ signal generator for circuit and noise analyses. $i_d = g_m v_{GS}$. The channel noise sources i_{n1} and i_{n2} are in gray.

density, at the operating frequency. $\mathrm{Re}\{Z_S\}$ and $\mathrm{Re}\{Z_D\}$ are inversely proportional to the channel width (W), and have a peak for a drain current density (I_D/W) of 0.015 mA/μm. $\mathrm{Im}\{Z_S\}$ and $\mathrm{Im}\{Z_D\}$ are also inversely proportional to W, and decrease with I_D/W. While for higher I_D/W and larger W, $\mathrm{Im}\{Z_D\}$ decreases with a steeper slope than $\mathrm{Re}\{Z_D\}$, but it is still not negligible, $\mathrm{Im}\{Z_S\}$ approaches $j0\ \Omega$ and is negligible compared with $\mathrm{Re}\{Z_S\}$.

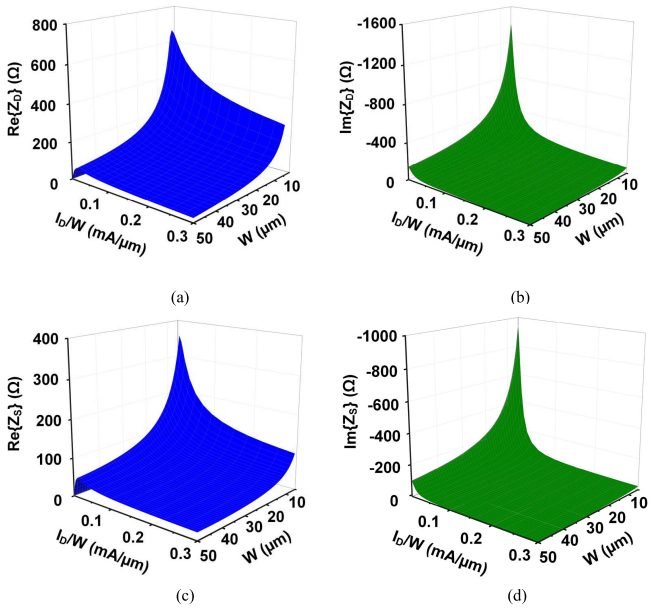


Fig. 6. (a) Real part of Z_D; (b) imaginary part of Z_D; (c) real part of Z_S; (d) imaginary part of Z_S; versus I_D/W and W, from schematic simulations in a 28 nm FDSOI CMOS.

Fig. 7(a) and (b) shows the IQ amplitude imbalance and phase difference imbalance of the LECLQC when $\mathrm{Re}\{Z_S\} = Z_0$, versus $\mathrm{Re}\{Z_D\}$, $\mathrm{Im}\{Z_D\}$, and $\mathrm{Im}\{Z_S\}$. It is to be noted that, if Z_S is real, then the IQ amplitude imbalance and phase difference imbalance remain equal to zero for any Z_D, although for $Z_D \neq Z_S$ a reduction of $|S_{21}|$ and $|S_{31}|$ occurs, as shown in Fig. 7(c), as a consequence of the input port impedance mismatch, as shown in Fig. 7(d).

Transistors M_1 and M_2 can be sized and biased in order to have the highest gain or the minimum NF [33], and M_3 and M_4 (together with their drain loads) can be sized to have Z_S close to Z_D, confident that as long as the imaginary part of Z_S is negligible, the circuit remains sufficiently robust to large Z_S and Z_D mismatches.

Moreover, Z_D and Z_S mismatches can be compensated by choosing L_{HC} and C_{HC} that deviate by a certain amount from the ideal values obtained by (1) and (2), and an appropriate coupling coefficient (k) between the spirals of the transformer. The analysis of the circuit in Fig. 5 allows deriving the transfer functions between the currents in the loads and the current i_d, namely, i_{s3}/i_d, i_{s4}/i_d, i_{d4}/i_d, and i_{d1}/i_d, where $i_d = g_m v_{GS}$, which are expressed as (3)–(6), shown at the bottom of this page.

$$\frac{i_{s3}}{i_d} = \frac{2C^2LZ_D^2Z_S(k-1)s^3+CLZ_D(Z_D+Z_S)(k-1)s^2-Z_D(2CZ_DZ_S-L)s-Z_D(Z_D+Z_S)}{C^2L^2(Z_D+Z_S)^2(k^2-1)s^4+2CL(k-1)[2CZ_DZ_S+L(k-1)]s^3+L\left[k^2-1-2CL\left(Z_D^2+Z_S^2\right)+4CLZ_SZ_D(k-2)\right]s^2-2(Z_D+Z_S)(CZ_DZ_S+L)s-(Z_D+Z_S)^2} \tag{3}$$

$$\frac{i_{s4}}{i_d} = \frac{C^2L^2Z_D(Z_D+Z_S)(k^2-1)s^4+CLZ_D[2CZ_SZ_D(k-1)+L(k^2-1)]s^3-CLZ_D(k+1)(Z_D+Z_S)s^2-Z_D(2CZ_SZ_D+Lk)s}{C^2L^2(Z_D+Z_S)^2(k^2-1)s^4+2CL(k-1)[2CZ_DZ_S+L(k-1)]s^3+L\left[k^2-1-2CL\left(Z_D^2+Z_S^2\right)+4CLZ_SZ_D(k-2)\right]s^2-2(Z_D+Z_S)(CZ_DZ_S+L)s-(Z_D+Z_S)^2} \tag{4}$$

$$\frac{i_{d4}}{i_d} = \frac{C^2L^2Z_S(Z_D+Z_S)(k^2-1)s^4+CL[2CZ_SZ_D(k-1)+L(Z_D+2Z_S)(k^2-1)]s^3-[L^2(k^2-1)+2CLZ_S(Z_Dk-2Z_D-Z_S)]s^2-(2CZ_DZ_S^2+LZ_D+2LZ_S)s-Z_S(Z_D+Z_S)}{C^2L^2(Z_D+Z_S)^2(k^2-1)s^4+2CL(k-1)[2CZ_DZ_S+L(k-1)]s^3+L\left[k^2-1-2CL\left(Z_D^2+Z_S^2\right)+4CLZ_SZ_D(k-2)\right]s^2-2(Z_D+Z_S)(CZ_DZ_S+L)s-(Z_D+Z_S)^2} \tag{5}$$

$$\frac{i_{d1}}{i_d} = \frac{2C^2LZ_DZ_S^2(k-1)s^3+2CLZ_DZ_S(k-1)s^2+Z_D(Lk-2CZ_S^2)s}{C^2L^2(Z_D+Z_S)^2(k^2-1)s^4+2CL(k-1)[2CZ_DZ_S+L(k-1)]s^3+L\left[k^2-1-2CL\left(Z_D^2+Z_S^2\right)+4CLZ_SZ_D(k-2)\right]s^2-2(Z_D+Z_S)(CZ_DZ_S+L)s-(Z_D+Z_S)^2} \tag{6}$$

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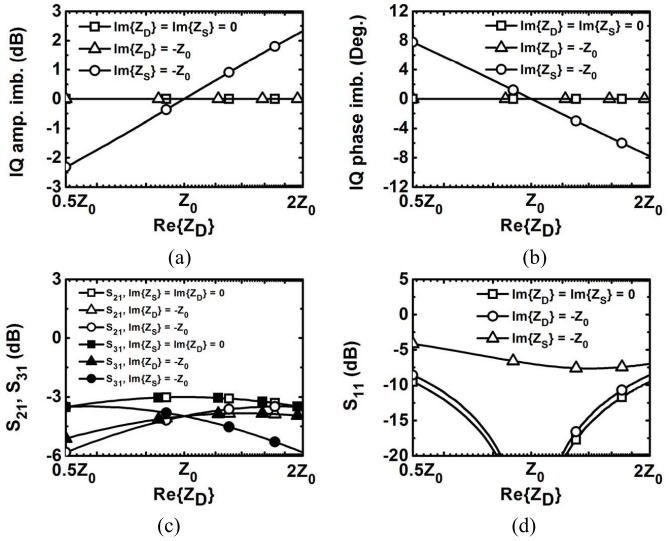


Fig. 7. (a) IQ amplitude imbalance, (b) IQ phase difference imbalance, (c) S_{21} and S_{31}, and (d) S_{11} of the LECLQC in Fig. 2(b) versus Re$\{Z_D\}$, Im$\{Z_D\}$, and Im$\{Z_S\}$.

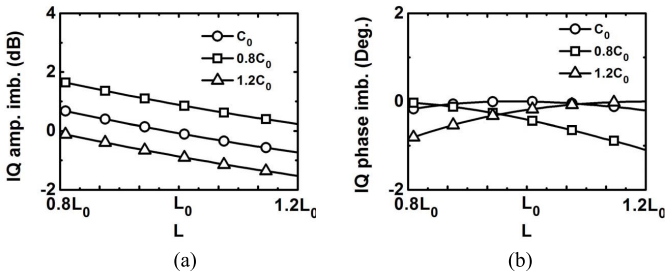


Fig. 8. (a) IQ amplitude imbalance and (b) IQ phase difference imbalance when L and C vary by ±20% of their nominal values.

In order to achieve the desired behavior, L, C, and k have to be chosen such that the currents i_{s4} and i_{s3} are equal in magnitude and have a phase difference of 90°, and the current i_{d2} has to be close to zero, at ω_0. These can be summarized by the following design conditions:

$$|i_{s4}|_{\omega_0}/|i_{s3}|_{\omega_0} = 1 \tag{7}$$

$$\angle i_{s4}|_{\omega_0} - \angle i_{s3}|_{\omega_0} = 90^\circ \tag{8}$$

$$|i_{d2}|_{\omega_0} = 0. \tag{9}$$

Thus, once the transistors have been sized and Z_S and Z_D are known, L, C, and k can be found by solving the system of design equations (7)–(9).

Following a more practical approach, we used the circuit simulator to find the values of L, C, and k, as will be shown in Section III-A, related to the design in a 28 nm FDSOI CMOS.

Fig. 8(a) and (b) shows the IQ amplitude imbalance and phase difference imbalance errors when L and C vary by ±20% of their nominal values. These errors are within 2 dB and 1°, respectively, confirming the robustness also to hybrid coupler component variations.

III. Phase Shifters Design

Two 4-bit (16 phases) mm-wave vector modulator active phase shifters exploiting the IQ signal generator presented

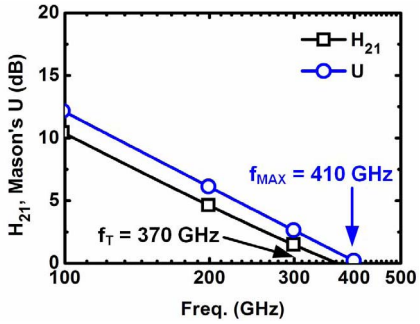


Fig. 9. Simulated current gain (H_{21}) and Mason's unilateral gain (U) for a minimum channel length transistor with width equal to 0.6 μm, biased with $V_{GS} = 0.7$ V and $V_{DS} = 1$ V.

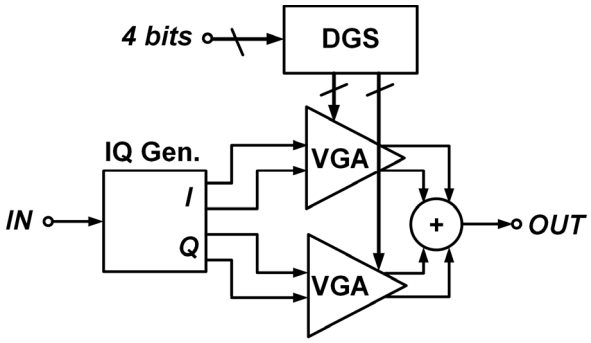


Fig. 10. Block diagram of the two mm-wave active phase shifters in a 28 nm FDSOI CMOS.

in Section II have been implemented in a 28 nm FDSOI CMOS technology by STMicroelectronics. The first solution exhibits a higher gain and the second solution has a more compact area. The main difference between the two different test-chip solutions lies in the VGA design, as will be explained hereinafter in Section III-A.

The transistors available within the 28 nm FDSOI CMOS technology by STMicroelectronics have simulated peak f_T and f_{MAX} of 370 and 410 GHz, respectively (see Fig. 9). Compared with bulk CMOS, transistors have the potential to be up to about 30% faster and more power efficient [34], making this technology attractive for mm-wave applications.

Fig. 10 shows the block diagram of the active phase shifters. The design of the IQ signal generator is common to the two circuit implementations, and is presented hereinafter in Section III-A. The design of the VGAs is presented hereinafter in Section III-B and the difference between the two circuit solutions is highlighted therein.

A. IQ Signal Generator

Fig. 11 shows the schematic of the IQ signal generator. The sizing of the transistor and passive components of the IQ generator is summarized in Table I. Fig. 12(a) and (b) shows the actual layout of the transistors and their most relevant layout parasitic components [35], respectively.

Fig. 13(a) and (b) shows the ratio of the amplitude of the I and Q outputs of the IQ signal generator [mag(I)/mag(Q)], and their phase difference [phase(I)-phase(Q)], as a function of L_{HC}, C_{HC}, and k, obtained by means of SpectreRF simula-

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TABLE I
DEVICE SIZING

PS1			PS2		
Transistors	**W/L**		**Transistors**	**W/L**	
$M_{1\text{-}8}$	14µm/28nm		$M_{1\text{-}8}$	14µm/28nm	
M_{PGS}	5µm/28nm		M_{PGS}	5µm/28nm	
Capacitors	**C(fF)**	**n/L(µm)/s(µm)**	**Capacitors**	**C(fF)**	**n/L(µm)/s(µm)**
C_{HC}	11	20/7/0.36	C_{HC}	11	20/7/0.36
C_{OUT}	57	24/16/0.36	C_{OUT}	57	24/16/0.36
Inductors	**L(pH)**	**n/D_{OUT}(µm)/w(µm)/s(µm)**	**Inductors**	**L(pH)**	**n/D_{OUT}(µm)/w(µm)/s(µm)**
L_G	136	2.5/20/1.8/1.8	L_G	136	2.5/20/1.8/1.8
$L_{m1\text{-}4}$	197	2.5/24/1.8/1.8	**Transformers**	**L(pH)/k**	**n/D_{OUT}(µm)/w(µm)/s(µm)**
Transformers	**L(pH)/k**	**n/D_{OUT}(µm)/w(µm)/s(µm)**	L_{HC}	241/0.55	1.5/38/1.8/0.45
L_{HC}	241/0.55	1.5/38/1.8/0.45	$B_{I\text{-}Q}$	100/0.73	1/36/3.6/-
$B_{I\text{-}Q}$	100/0.73	1/36/3.6/-	B_{OUT}	75/0.71	1/33/6.4/-
B_{OUT}	75/0.71	1/33/6.4/-	$T_{I\text{-}Q}$	140/0.2	1.5/33/1.8/1.8

Capacitors: n is the number of fingers; L is the finger length; s is the finger spacing.
Inductors/Transformers: n is the number of turns; D_{OUT} is the outer diameter; w is the trace width; s is the trace spacing.

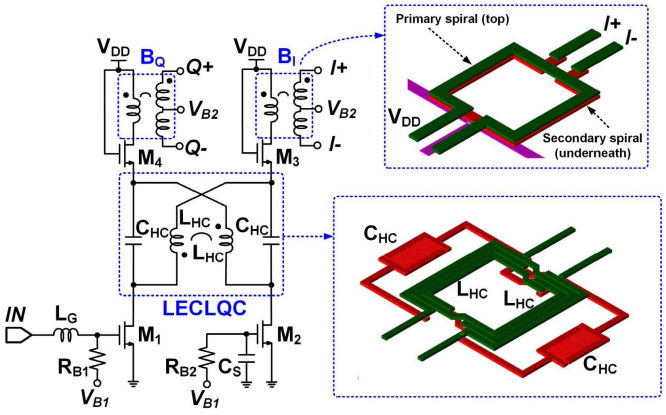
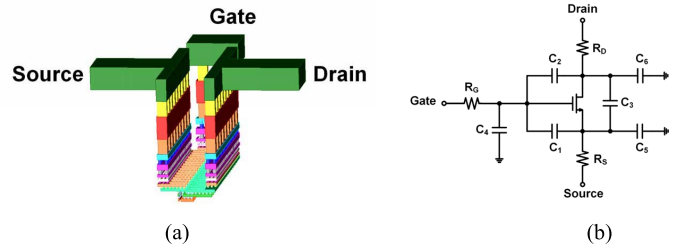


Fig. 11. Schematic of IQ signal generator and 3-D view of the LECLQC and the integrated baluns (B_I and B_Q).



(a) (b)

Fig. 12. (a) Transistor layout. (b) Transistor and layout parasitics [35].

tions, including the transistor layout parasitics. On inspection, it can be noted that for L_{HC}, C_{HC}, and k equal to about 240 pH, 8 fF and 0.55 [mag(I)/mag(Q)] and [phase(I)-phase (Q)] are close to 0 dB and $-90°$, respectively.

The loads of I and Q branches consist of two 1:1 transformers as baluns (B_I and B_Q), which also provide the single-ended to differential conversion required for properly driving the subsequent differential VGAs. The secondary spirals have a central tap for the dc biasing of the CS transistors of the VGAs. The inductor L_G improves the input impedance matching to a 50 Ω source resistance.

All the passive components have been designed and simulated by means of the FEM simulator element in ADS by Keysight Technologies (full wave 3-D FEM electromagnetic simulator, formerly known as EMDS).

B. Variable Gain Amplifiers

Fig. 14 shows the schematics of the VGAs. In particular, Fig. 14(a) reports the VGAs designed for the first phase shifter (namely, PS1) anticipated and partially reported in [24], whereas Fig. 14(b) reports the VGAs CS stages of the second phase shifter (namely, PS2).

Differential cascode amplifiers have been adopted in order to provide both negative and positive amplification coefficients, hence achieving full-360° phase shifting. The gain selection is operated by the common-gate programmable gain stage (PGS) and made according to the principle shown in [1]. The common-gate PGS of each VGA is implemented by a matrix of 18 transistors (two 3 × 3 matrixes, one for each branch). By properly switching ON and OFF these transistors (this is obtained by connecting to V_{DD} or grounding their gates), it is possible to set the normalized gain (-1, $-2/3$, $-1/3$, 0, 1, 1/3, 2/3, 1) by choosing the fraction of current that flows in the output load, while the current flowing in the CS transistors of the VGA remains constant.

A common-gate programmable gain stage has been employed, instead of programmable current sinks, in order to achieve the following.

1) Keep as low as possible the variations of the impedance seen at the I and Q inputs of the VGA for all the gain settings, and hence reducing the influence on the IQ generator performances.
2) Reduce the number of stacked transistors from V_{DD} to ground, for adequate gain at lower V_{DD} and so a lower average power consumption, despite the reduced efficiency for lower gain settings.

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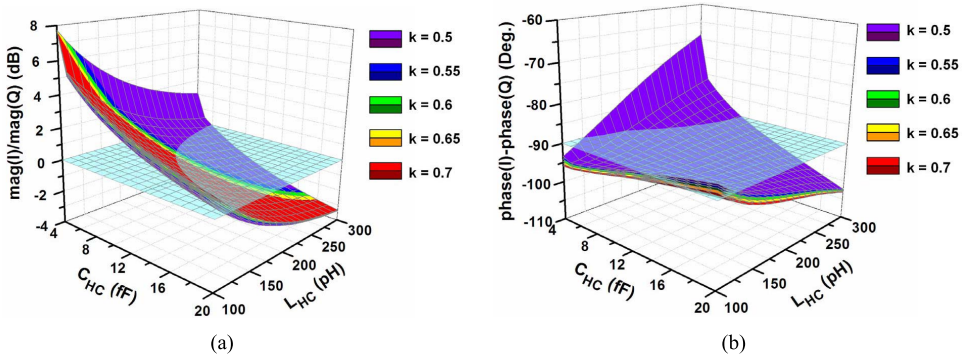


Fig. 13. Simulation results for the IQ signal generator in Fig. 9(a) including transistor layout parasitics, versus L_{HC}, C_{HC}, and k. (a) Amplitude ratio in decibel between I and Q output signals; note the intersection with the 0 dB reference plane. (b) Phase difference between I and Qoutputs in degrees; note the intersection with the 90° reference plane.

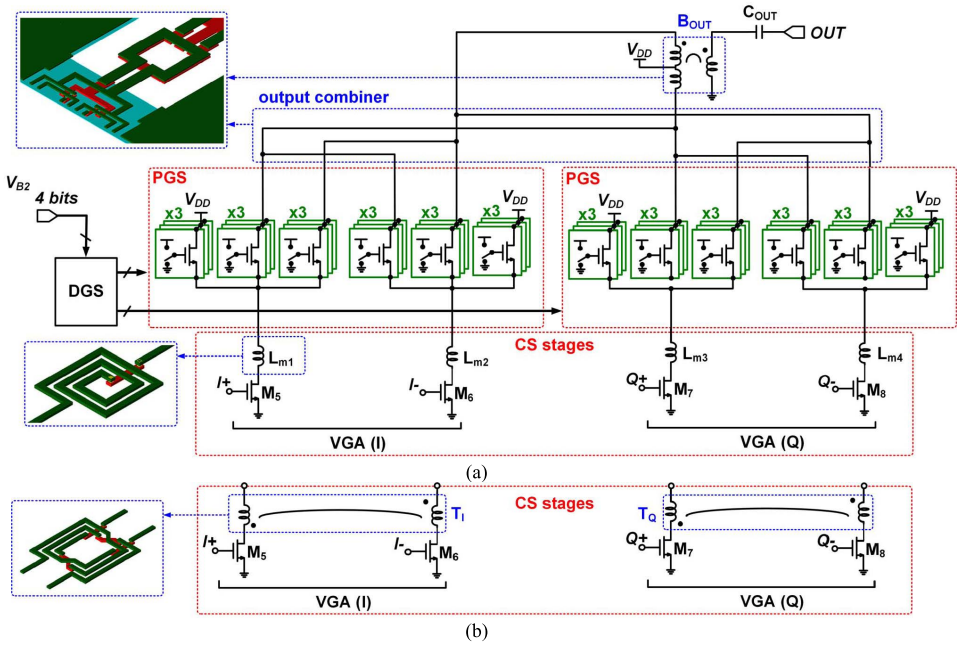


Fig. 14. (a) Schematic of the two VGAs (I and Q paths) with programmable gain stage (PGS), combiner, and output load balun (B_{OUT}) of the first test-chip (PS1). (b) Schematic of the CS stages of the two VGAs with integrated transformers T_I and T_Q of PS2. PGSs and B_{OUT} in PS2 are the same as in PS1.

The digital gain selector [DGS in Fig. 14(b)] consists of a combinatory logic (or-and) digital circuit, with input and output buffers, which provides the proper voltages to the gates of the PGS transistors according to a 4-bit input digital word. This entire circuit network consists of 728 transistors, including buffers.

In the VGAs of Fig. 14(a), i.e., related to PS1, the inductors L_{m1-4} resonate with the capacitances at the drain of M_{5-8} and the source terminals of the matrixes of common-gate transistors of the PGS in order to increase the gain of the VGAs [33], [36].

In PS2, the four inductors L_{m1-4} have been replaced with two transformers T_I and T_Q. The use of a transformer instead of two independent inductors allows area saving, as the two spirals lie within the same area and the total inductance values are increased by mutual coupling, and hence permitting the design of smaller spirals. This aspect is particularly critical in the design of large arrays where a large number of receivers or transmitters lie on the same silicon die. Thereby, PS2 allows a more compact design with respect to PS1, hence being very beneficial for large arrays envisaged for the future networks and communications, e.g., up to 256 elements [37].

Lastly, the output combiner of the VGAs was designed in order to minimize the length difference between each drain of the PGS stage and the output balun (B_{OUT}).

IV. Experimental Results

Fig. 15 shows the micrographs of the two test-chip implementations (PS1 and PS2). The overall area of the two test-chip implementations including IQ signal generator, VGAs, and DGS, is about 0.54×0.31 mm^2 for PS1, and 0.54×0.28 mm^2 for PS2. If we consider the core area only, (IQ signal generator plus VGAs), the core area of PS1 amounts

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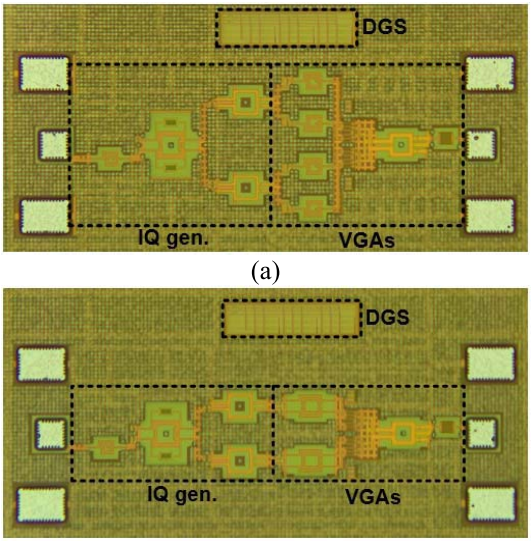


Fig. 15. Micrographs of the two test-chips. (a) PS1. (b) PS2. The core (IQ signal generator plus VGAs) area of PS1 is equal to 0.54×0.22 mm^2. The core area of PS2 is equal to 0.54×0.12 mm^2 (approximately half the PS1 core area).

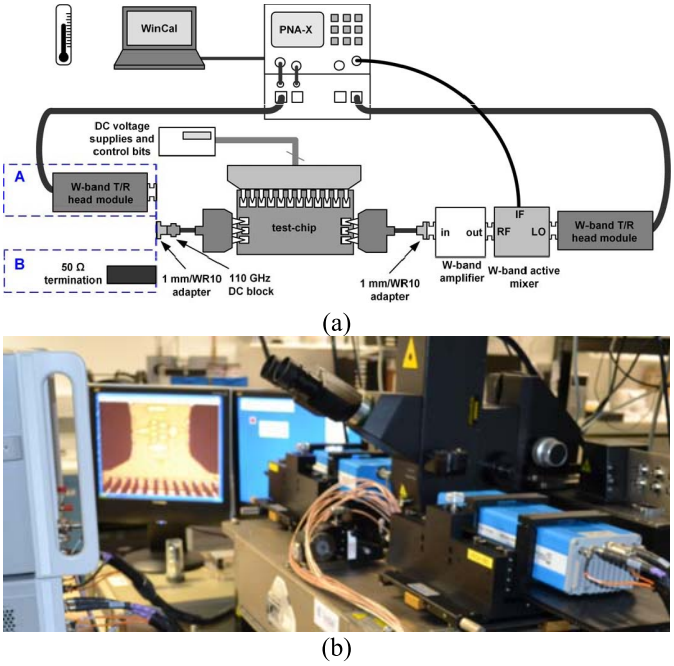


Fig. 16. S-parameter measurement setup. (a) Block diagram. (b) Photograph.

to 0.54×0.22 mm^2, whereas the core area of PS2 amounts to 0.54×0.12 mm^2, i.e., approximately half of the core area of PS1, making this latter more suitable for an effective integration of large arrays.

Fig. 16(a) and (b) shows the block diagram and photograph of the measurement setup for the S-parameters. The test-chips have been measured by means of the Agilent PNA-X N5244A with Agilent N5262A mm-wave test set controller and Agilent N5256AW10 W-band mm-wave T/R head modules. On-chip measurements have been carried out by means of 100 μm pitch 110 GHz GSG Cascade i110 probes. A 110 GHz

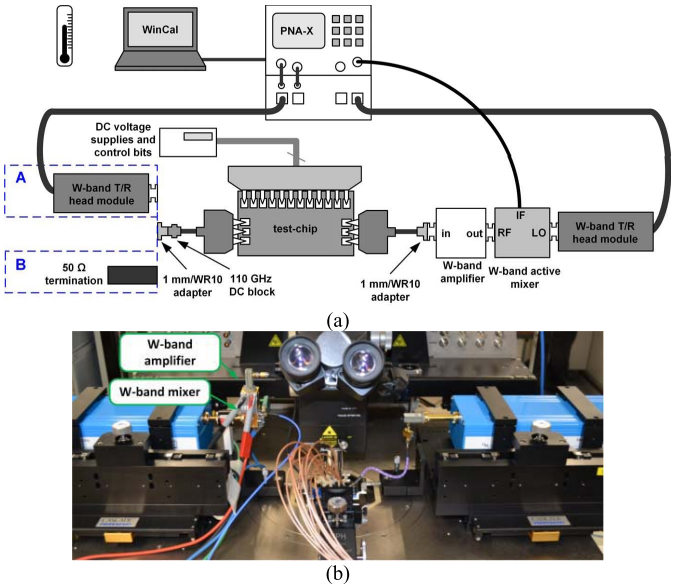


Fig. 17. (a) NF measurement setup for the phase shifter plus downconverter. First, the input probe is connected to the W-band head module (A) for gain measurement of the test-chip plus downconverter. Then, the input probe is connected to a W-band 50 Ω termination (B), and the output noise power density of test-chip plus downconverter is measured. (b) NF measurement setup (A) photograph.

DC block has been used on the PNA-X Port 1 for bias decoupling.

SOLT calibration with switch terms was performed by means of a Cascade 104-783A W-band GSG substrate and WinCal XE. Power calibration of the PNA-X was performed by means of the Agilent W8486A W-band power sensor and Agilent N1914A power meter.

The NF measurements were carried out with the cold-source method [38], [39]. This method consists of measuring the S-parameters of the test-chip, and the output noise power density (ONPD) of the test-chip when its input is terminated on 50 Ω (with the PNA-X low noise receiver, Option H29) [38]. The output of the phase shifter is downconverted to 1 GHz by means of a W-band lowloss active mixer (Millitech MB1-10 [40]). A W-band LNA (Millitech LNA-10-02130 [41]) is used to amplify the phase shifter output in order to mitigate the measure uncertainty.

Fig. 17(a) and (b) shows the block diagram and photograph of the experimental setup for the NF measurement. The NF measurements have been carried out based on the following steps.

1) The gain (G) of the downconverter (i.e., the cascade W-band LNA plus W-band mixer) is measured according to the setup A in Fig. 17(a). The input noise power density (INPD) is measured according to the setup B in Fig. 17(a). Then its NF is computed as follows:

$$F = \frac{\mathrm{SNR}_i}{\mathrm{SNR}_o} = \frac{1}{G} \cdot \frac{\mathrm{ONPD}}{\mathrm{INPD}} \tag{10}$$

where INPD $= k_B \times T_0$, k_B is the Boltzmann constant and T_0 is the reference source temperature.

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TABLE II
SUMMARY OF PERFORMANCES AND COMPARISON WITH THE STATE-OF-THE-ART CMOS AND BICMOS ACTIVE PHASE SHIFTERS

	[3]	[6]	[45]	[45]	[46]	This work PS1	This work PS2
Technology	SiGe BiCMOS	SiGe BiCMOS	SiGe BiCMOS	65nm CMOS	28nm FDSOI CMOS	28nm FDSOI CMOS	28nm FDSOI CMOS
Topology	Vector modulator	Vector modulator	Vector modulator	Vector modulator	Vector modulator	Vector modulator	Vector modulator
Central freq. (f_0) (GHz)	~ 81	~ 86	74	90	~105	87.4	89.2
B_{3dB} (GHz)	~ 74-92	~ 77-97	70-77	80-94	~97-110	78.8-92.8	80.2-96.8
Average gain at f_0 (G_{AV}) (dB)	~ -4	~ -4	~ -6*	~ -4.2 dB**	~0	2.3	0.83
RMS gain err. at f_0 (dB)	~ 1.5	~ 1	~ 0.6	~ 1.4	1.5	1.68	1.46
RMS gain err. in B_{3dB} (dB)	< 1.5	< 1	~ 0.6	~ 1.4	< 1.5	< 2	< 2
RMS phase err. at f_0 (Deg.)	~ 8	~ 6	~ 2	~ 2	13	9.4	11.2
RMS phase err. in B_{3dB} (Deg.)	< 11	< 12	< 4	< 5	> 20	< 11.9	< 11.9
S_{11} (dB)	-	-	-	< -11	< -22	< -10.5	< -11.5
IP_{1dB} (dBm)	~ 5 ± 2 (sim.)	-4 ± 2	-	-	-	-8 : -5 (avg. -7)	-7 : -5 (avg. -6)
Noise Figure (dB)	14-17 @ 80GHz (sim.)	-	26***	-	-	9-14 (avg. 10.8) @ 87GHz	8.9-15 (avg. 11.9) @ 89GHz
Resolution (bits)	5	4	4	4	2	4	4
Voltage supply (V)	2	2	2.5	1.2	1	1.2	1.2
Power consumption (mW)	28	-	67.5	43	122.9	21.6	21.6
FOM1	186.8	181.3	113.3	277.6	96.6	440.7	380.2
FOM2	0.61	-	-	-	-	0.37	0.31
Area (mm^2)	-	-	-	-	0.565	0.12 (core)	0.06 (core)

*~16 dB (LNA+phase shifter) – 22 dB (LNA stand-alone) = -6 dB
** ~1.8 dB (phase shifter +PA) – 7 dB (PA stand-alone) = -4.2 dB
*** Applying Friis formula: LNA gain and NF are 22 dB and 4 dB, NF of LNA+phase shifter is 7 dB

$$FOM1 = \frac{f_0(\text{GHz}) \cdot G_{AV}(\text{abs}) \cdot B_{3dB}(\text{GHz}) \cdot \text{Resolution (bits)}}{\text{RMS phase error in } B_{3dB}(\text{deg.}) \cdot \text{ RMS gain error in } B_{3dB}(\text{lin.})}$$

$$FOM2 = \frac{f_0(\text{GHz}) \cdot G_{AV}(\text{abs}) \cdot B_{3dB}(\text{GHz}) \cdot IP_{1dB}(\text{mW}) \cdot \text{Resolution (bits)}}{\text{RMS phase error in } B_{3dB}(\text{deg.}) \cdot \text{ RMS gain error in } B_{3dB}(\text{lin.}) \cdot P_C(\text{mW}) \cdot (NF(\text{lin.}) - 1)}$$

2) The gain and ONPD of the test-chip followed by the downconverter are measured, and the NF of test-chip plus downconverter is computed.
3) The NF of the test-chip is derived from the NF of the downconverter alone and the NF of the phase shifter plus downconverter using the Friis equation [42].

Section IV-A reports the measured results for the first test-chip (PS1). Section IV-B reports the measured results for the second test-chip (PS2).

The details of the measured performance and comparison with the state-of-the-art CMOS and BiCMOS full-360° phase shifters operating in W-band are given in Table II. It is worth noting that the presented solutions exhibit a lower NF up to 3 dB improvement, and a higher average peak gain up to 2 dB improvement, with respect to the state-of-the-art solutions of CMOS and SiGe BiCMOS full-360° phase shifters operating in W-band.

Two figures of merit, FOM1 and FOM2, have been defined for comparison with other works. FOM1 is based on the performances available for all the phase shifters in Table II. PS1 and PS2 exhibit the highest FOM1 among those in Table II. FOM2 also takes into account linearity, power consumption (P_C), and NF performances for a more extensive comparison. Note that PS1 and PS2 exhibit a FOM2 close to the best FOM2 exhibited by [3].

A. PS1 Experimental Results

The phase shifter consumes 18 mA from a 1.2 V supply.

The measured gain for the 16 phase states and the average gain are shown in Fig. 18. At 87.4 GHz, the circuit exhibits an average gain of 2.3 dB, and $B_{3\text{dB}}$ from 78.8 to 92.8 GHz.

Figs. 19 and 20 show the measured phase shift and relative phase shift to the reference state 0.

The measured rms phase and gain errors [43], [44] are shown in Fig. 21. The rms phase error is equal to 9.4° at the central frequency of the average gain ($f_0 = 87.4$ GHz), and lower than 11.9° in the $B_{3\text{dB}}$. The rms gain error amounts to 1.68 dB at 87.4 GHz and it is lower than 2 dB in the $B_{3\text{dB}}$.

Fig. 22 shows the measured S_{11} and S_{22} parameters. S_{11} parameter is lower than -10.5 dB in the $B_{3\text{dB}}$.

The measured gain of the phase shifter for the 16 phase states and the average phase shifter gain versus input power, at 87.4 GHz, are shown in Fig. 23. The input-referred 1 dB compression point ($IP_{1\text{dB}}$) varies from -8 to -5 dBm for the 16 phase states. The average $\text{IP}_{1\text{dB}}$ is equal to -7 dBm.

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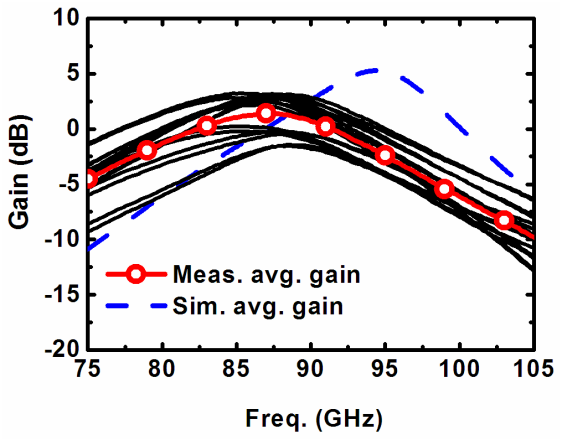


Fig. 18. PS1: measured gain (S_{21}) for the 16 phase states (black curves), and measured and simulated average gains.

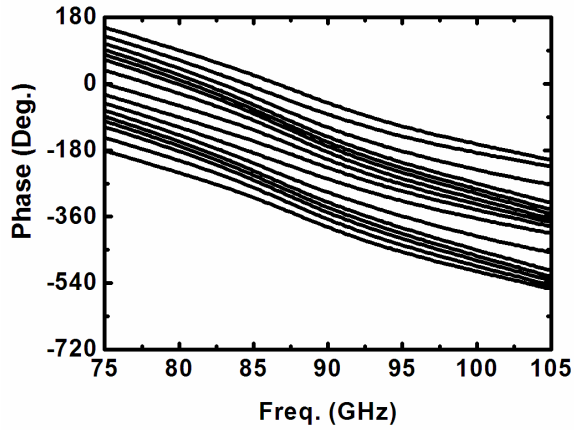


Fig. 19. PS1: measured phase shift for the 16 phase states.

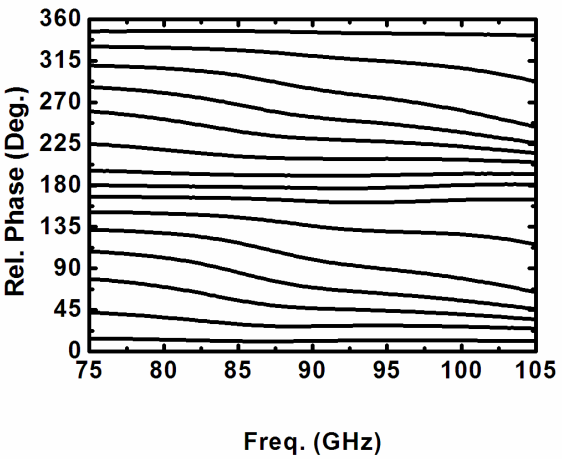


Fig. 20. PS1: measured relative phase shift with respect to the reference phase state 0.

The measured relative phase shifting for the 16 phase states versus input power, at 87.4 GHz, are shown in Fig. 24. The phase shifting is almost constant with the input power, with a deviation at the IP_{1dB} contained between 2° and 5° with respect to the phase for low values of input power, for the 16 phase states.

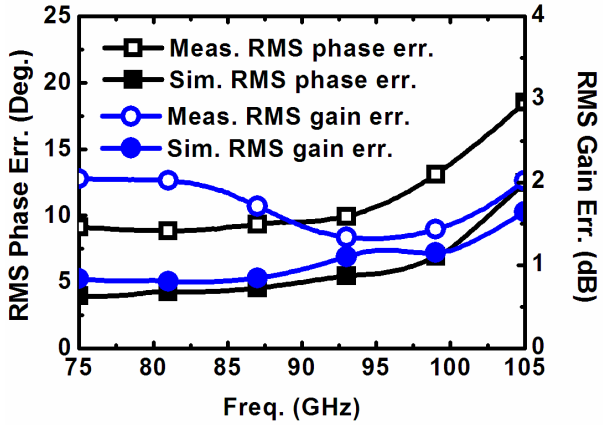


Fig. 21. PS1: measured and simulated rms phase error and rms gain error.

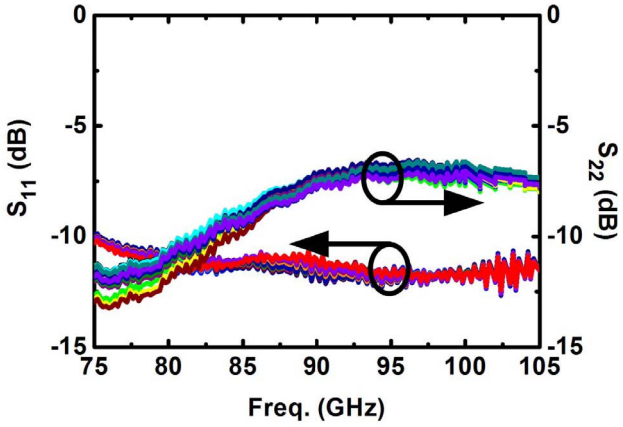


Fig. 22. PS1: measured S_{11} and S_{22} parameters for the 16 phase states.

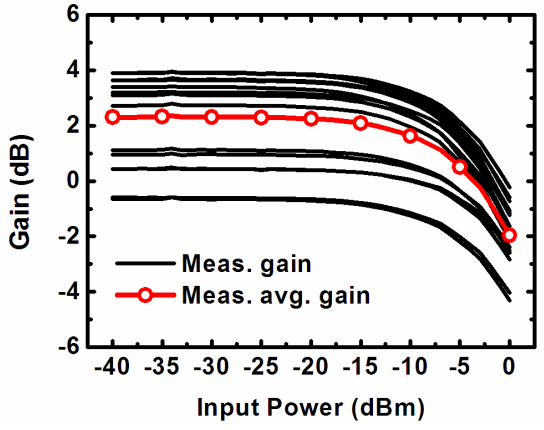


Fig. 23. PS1: measured gain versus input power, at $f_0 = 87.4$ GHz.

The rms phase error, measured at f_0 and $f_0 \pm 5$ GHz, versus input power is shown in Fig. 25. The rms error deviates by less than 3° in the range of input power between −40 and 0 dBm.

Fig. 26 shows the measured NF from 82 to 92 GHz (the bandwidth is limited to 10 GHz by the active W-band mixer) for the 16 phase states, and measured and simulated average NF. The NF is comprised between 9 and 14 dB at 87 GHz, and the average NF is equal to 10.8 dB at 87 GHz.

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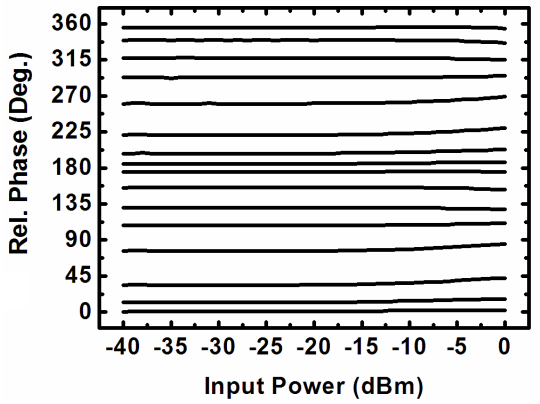


Fig. 24. PS1: measured relative phase versus input power, at $f_0 = 87.4$ GHz.

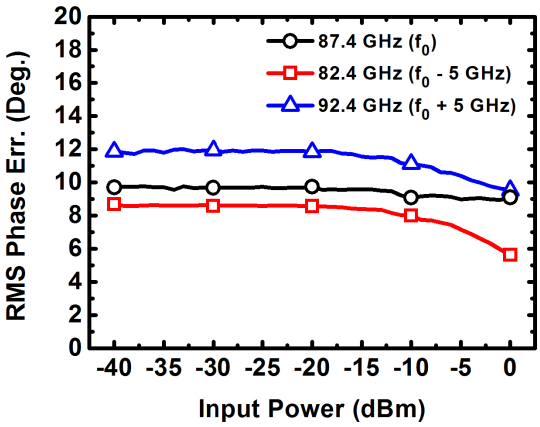


Fig. 25. PS1: measured rms phase error versus input power, at $f_0 = 87.4$, 82.4, and 92.4 GHz.

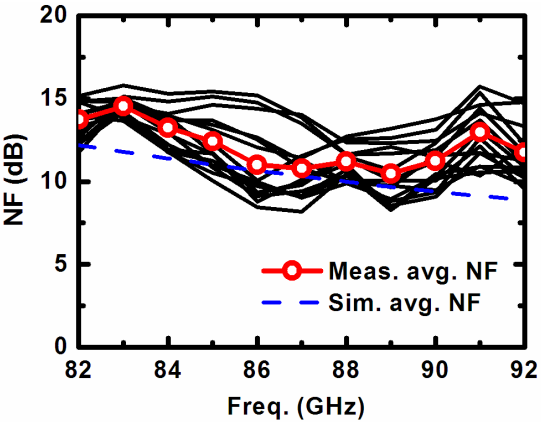


Fig. 26. PS1: measured NF for the 16 phase states (black curves), and measured and simulated average NF.

B. PS2 Experimental Results

The phase shifter consumes 18 mA from a 1.2 V supply.

The measured gain for the 16 phase states and the average gain are shown in Fig. 27. The circuit exhibits an average gain of 0.83 dB at $f_0 = 89.2$ GHz and $B_{3\text{dB}}$ from 80.2 to 96.8 GHz.

Figs. 28 and 29 show the measured phase shift and relative phase shift to the reference state 0, respectively.

The measured rms phase and gain errors are shown in Fig. 30. The rms phase error is equal to 11.2° at 89.4 GHz and is lower than 11.9° in the $B_{3\text{dB}}$. The rms gain error

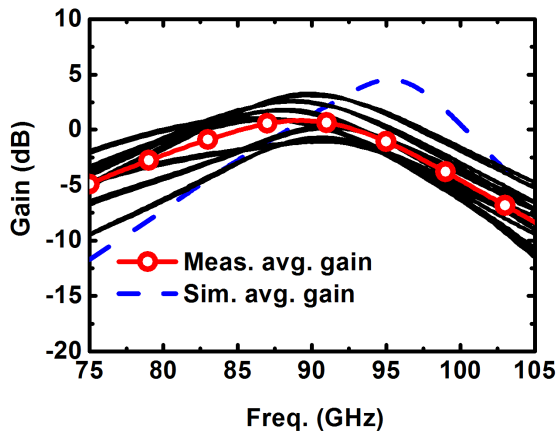


Fig. 27. PS2: measured gain (S_{21}) for the 16 phase states (black curves), and measured and simulated average gains.

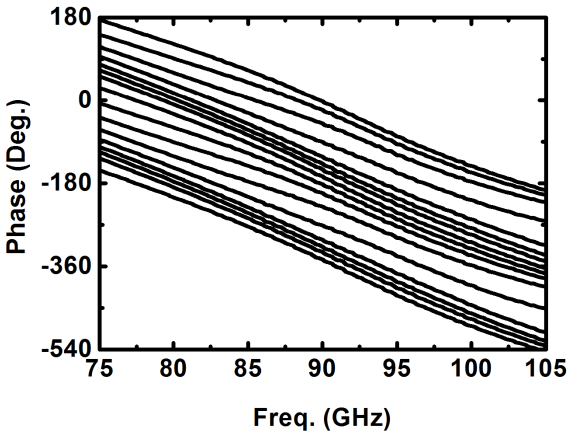


Fig. 28. PS2: measured phase shift for the 16 phase states.

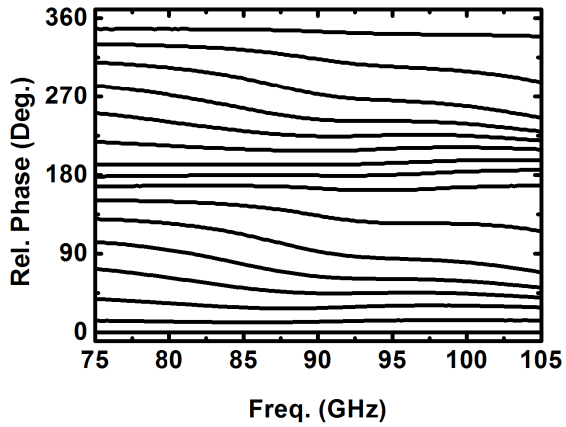


Fig. 29. PS2: measured relative phase shift with respect to the reference phase state 0.

amounts to 1.46 dB at 89.2 GHz and is lower than 2 dB in the $B_{3\text{dB}}$.

The measured S_{11} and S_{22} parameters are shown in Fig. 31. S_{11} is lower than −11.5 dB in the $B_{3\text{dB}}$.

Fig. 32 shows the gains versus input power, measured at 89.4 GHz, for the 16 phase states, and the average gain. The average $P_{1\text{dB}}$ is equal to −6 dBm, and is comprised between −7 and −5 dBm for the 16 phase states.

The measured relative phase shifting for the 16 phase states versus input power, at 89.2 GHz, are shown in Fig. 33.

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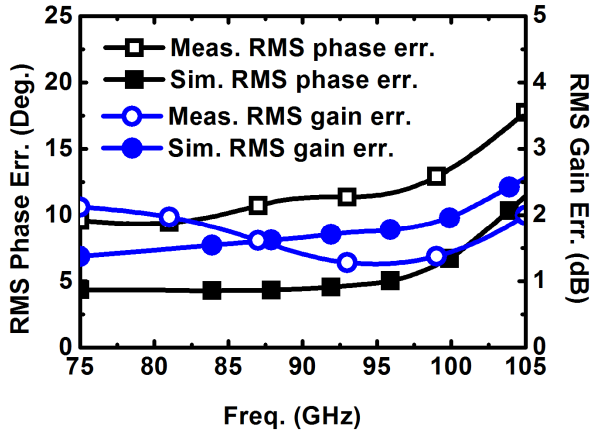


Fig. 30. PS2: measured and simulated rms phase error and rms gain error.

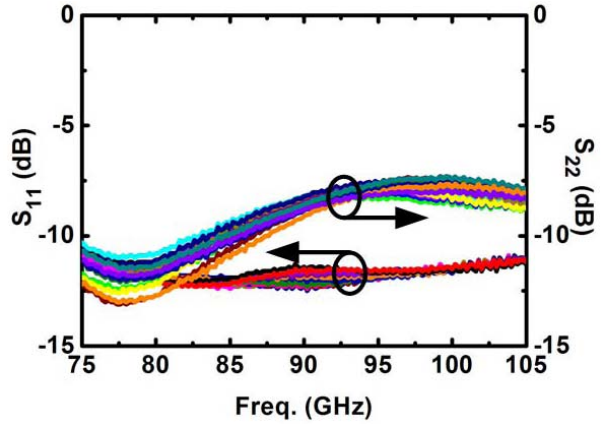


Fig. 31. PS2: measured S_{11} and S_{22} parameters for the 16 phase states.

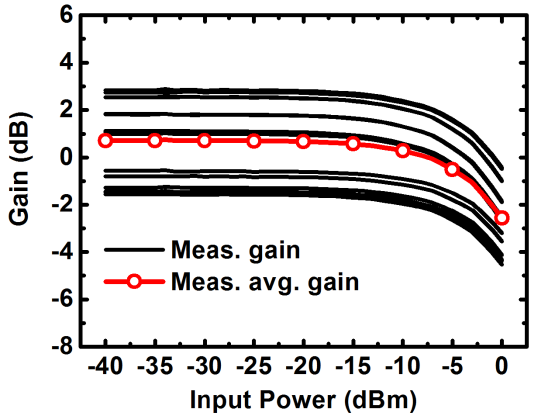


Fig. 32. PS2: measured gain versus input power, at $f_0 = 89.2$ GHz.

As for PS1, the phase shifting is almost constant with the input power, with a deviation at the $P_{1\text{dB}}$ bounded between 2° and 5° with respect to the phase for low values of input power, for the 16 phase states.

The rms phase error, measured at f_0 and $f_0 \pm 5$ GHz, versus the input power are shown in Fig. 34. The rms error deviates by less than 2° in the range of input power between −40 and 0 dBm.

Fig. 35 shows the measured NF from 84 to 94 GHz for the 16 phase states, and the measured and simulated average NF. The NF is between 8.9 and 15 dB at 87 GHz, and the average NF is equal to 11.9 dB at 87 GHz.

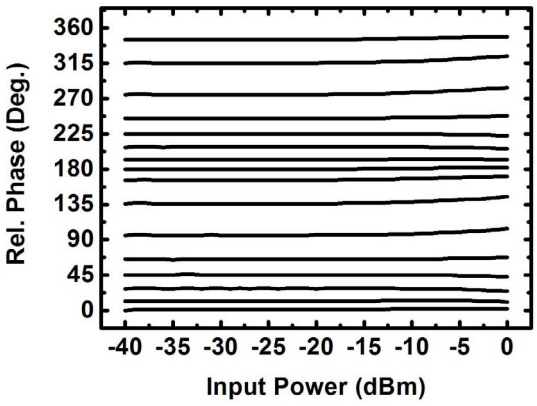


Fig. 33. PS2: measured relative phase versus input power, at $f_0 = 89.2$ GHz.

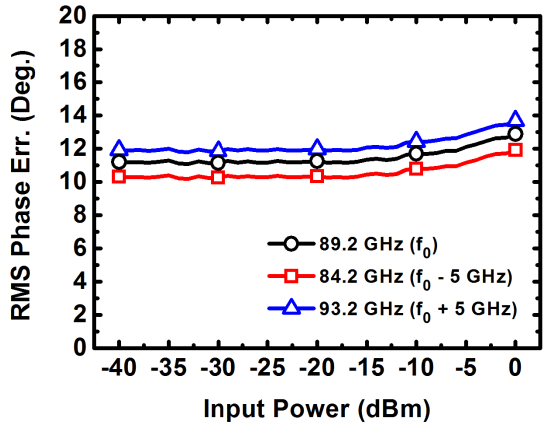


Fig. 34. PS2: measured rms phase error versus input power, at $f_0 = 89.2$, 84.2, and 93.2 GHz.

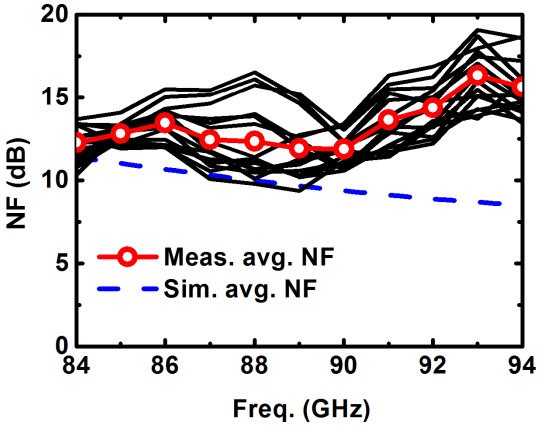


Fig. 35. PS2: measured NF for the 16 phase states (black curves), and measured and simulated average NF.

V. Conclusion

We reported two mm-wave vector modulator active phase shifters exploiting a novel in-phase (I) and quadrature (Q) signal generator that consists of a single-input double-output cascode amplifier incorporating an LECLQC.

The two different 4-bit (16 phases) test-chip implementations have been realized in a 28 nm FDSOI CMOS by STMicroelectronics and characterized experimentally. The first exhibits a higher gain and the second has a more compact

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area, i.e., reduced to about 50%, and is thereby more suitable for implementation of large arrays envisaged for massive multiple input multiple output systems. The two proposed solutions exhibit a lower NF up to 3 dB improvement, and a higher gain up to 2 dB improvement, with respect to the state-of-the-art CMOS and BiCMOS full-360° phase shifters operating in W-band.

APPENDIX

The NF of the IQ generator can be computed by analyzing the circuit in Fig. 5, where i_{n1} and i_{n2} are the channel noise sources of transistors M_1 and M_2, respectively. The effects of $C_{\rm GD}$, R_G, and contributions of the common-gate transistors are neglected in the interest of simplicity [47], [48].

To evaluate the I output noise due to the source resistance R_S, we first evaluate the transconductance $G_{\rm mI}$

$$G_{\rm mI} = \frac{i_{s3}}{v_{\rm IN}} = \frac{g_m}{s^2 C_{\rm GS} L_G + s C_{\rm GS} R_S + 1} \left(\frac{i_{s3}}{i_d}\right) \tag{11}$$

where $i_d = g_m v_{\rm GS}$ and (i_{s3}/i_d) is expressed as in (5).

The output noise due to R_S is equal to

$$\left.\overline{\frac{i^2_{n,\rm OUT}}{\Delta f}}\right|_{\rm RS} = \overline{\frac{v^2_{n.Rs}}{\Delta f}} |G_{\rm mI}|^2 = 4kTR_S \left|\frac{g_m}{s^2 C_{\rm GS} L_G + s C_{\rm GS} R_S + 1}\right|^2 \left|\frac{i_{s3}}{i_d}\right|^2. \tag{12}$$

The output noise due to M_1 amounts to

$$\left.\overline{\frac{i^2_{n,\rm OUT}}{\Delta f}}\right|_{M1} = \overline{\frac{i^2_{n.M1}}{\Delta f}} \left|\frac{i_{s3}}{i_d}\right|^2 = 4kT\gamma g_{d0} \left|\frac{i_{s3}}{i_d}\right|^2 \tag{13}$$

where γ is the channel thermal noise coefficient, g_{d0} is the zero-bias drain conductance, and (i_{s3}/i_d) is expressed as in (3).

For symmetry, the I output noise due to M_2 is equal to

$$\left.\overline{\frac{i^2_{n,\rm OUT}}{\Delta f}}\right|_{M2} = \overline{\frac{i^2_{n.M2}}{\Delta f}} \left|\frac{i_{s4}}{i_d}\right|^2 = 4kT\gamma g_{d0} \left|\frac{i_{s4}}{i_d}\right|^2 \tag{14}$$

where (i_{s4}/i_d) is expressed as in (4). If L, C, and k are chosen for proper quadrature operation, $i_{s4} = j i_{s3}$, $|i_{s4}| = |i_{s3}|$, the output noise due to M_2 is equal to that due to M_1. Then, the NF is calculated as the ratio between the total output noise and the output noise due to R_S

$$\begin{aligned} \rm NF &= 1 + \frac{\left.\overline{\frac{i^2_{n,\rm OUT}}{\Delta f}}\right|_{M1} + \left.\overline{\frac{i^2_{n,\rm OUT}}{\Delta f}}\right|_{M2}}{\left.\overline{\frac{i^2_{n,\rm OUT}}{\Delta f}}\right|_{\rm RS}} \\ &= 1 + 2\left|\frac{s^2 C_{\rm GS} L_G + s C_{\rm GS} R_S + 1}{g_m}\right|^2 \frac{\gamma g_{d0}}{R_S}. \end{aligned} \tag{15}$$

The NF in (15) also applies for the Q output port, being $|i_{s4}| = |i_{s3}|$.

At the operating frequency ω_0, under the hypotheses that L_G is equal to $1/(\omega_0^2 C_{\rm GS})$ to compensate for the imaginary part of the input impedance, and $\omega_T \approx g_m/C_{\rm GS}$, NF is

$$\rm NF \approx 1 + 2R_S \gamma g_{d0} \left(\frac{\omega_0}{\omega_T}\right)^2. \tag{16}$$

For simplicity, we consider the VGAs of the phase shifter in Fig. 10 as ideal amplifiers with programmable gains A_I and A_Q from -1 to 1, as in Fig. 1(b). The output of the phase shifter is $i_{\rm OUT} = A_I i_{s3} + A_Q i_{s4}$. Since $i_{s4} = j i_{s3}$, then $i_{\rm OUT} = (A_I + j A_Q) i_{s3}$. As shown in Fig. 1(b), $|A_I + j A_Q| \approx 1$ for the 16 phases, and then $|i_{\rm OUT}| = |i_{s3}|$. Thus, the NF of the phase shifter is expressed by (15) and (16), as for the IQ generator alone.

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Domenico Pepe (S'08–M'09) received the B.Sc. and M.Sc. degrees in electronic engineering from the University of Pisa, Pisa, Italy, in 2002 and 2005, respectively, and the Ph.D. degree in electronic engineering from the University of Pisa and the University of Bordeaux 1, Bordeaux, France, in 2009.

He is a Senior Researcher at the University of Modena and Reggio Emilia, Reggio Emilia, Italy. Since 2009, he has been with the Tyndall National Institute, Cork, Ireland. He has co-authored over 90 technical journals and conference papers, and book chapters. His current research interests include RF, UWB, and mm-wave IC design in nanoscale CMOS and BiCMOS technologies.



Domenico Zito (S'00–M'04–SM'14) received the M.Sc. degree in electronic engineering and the Ph.D. degree in information engineering from the University of Pisa, Pisa, Italy, in 2000 and 2004, respectively.

He is a Full Professor at the Department of Engineering, Aarhus University, Denmark. He was a Visiting Researcher at STMicroelectronics, Catania, Italy, in 2001, and Austriamicrosystems, Graz, Austria, in 2002. Since 2005, he has been with the University of Pisa, Italy. Since 2009, he has been with the University College Cork and Tyndall National Institute, Cork, Ireland. He has authored over 150 papers in peer-reviewed international journals and conference proceedings (over 20 invited papers), seven chapters of a book, and two books (one book edited), and holds three patents. His current research interests include the design of system-on-chip radiofrequency (microwave and mm-wave) front-ends in nanoscale CMOS and BiCMOS technologies for emerging wireless applications (data communication and contactless sensing).

Dr. Zito has been a member of the Editorial Board of peer-reviewed international journals and the Technical Program Committee of international conferences. He was a recipient of the First Prize at the European Wireless Business Idea Competition "Mario Boella" (VP URSI) in 2005 for the Best Practice in Research and Innovation in Wireless Technology. He was a recipient of three best paper awards at the IEEE conferences. He serves as a TPC member of the European Solid-State Circuits Conference, the TPC Chair of the IEEE International Conference on Electronics, Circuits and Systems 2016, and an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS.