Pattern compensation in SOA-based gates

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Abstract: We propose a novel scheme employing complementary data inputs to overcome the patterning normally associated with semiconductor optical amplifier based gates and demonstrate the scheme experimentally at 42.6Gb/s. The scheme not only avoids introducing patterning during switching, but also compensates for much of the patterning present on the input data. A novel gate was developed for the experiment to provide the complementary signals required for the scheme.

OCIS codes : (200.3760) Logic-based optical processing; (200.6015) Signal regeneration, (250.3140) Integrated optoelectronic circuits..

References and links

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1. Introduction

Interferometers incorporating semiconductor optical amplifiers (SOAs) are widely regarded as the most practical form of all-optical gate for telecommunications applications, offering what many consider to be the best combination of speed, size and power consumption. Differential or "push-pull" operation allows switching by return-to-zero (RZ) signals at rates beyond the limitation of the SOA recovery time [1], but although switching windows of a few

picoseconds duration can be precisely defined in time, the size of the phase difference created in the interferometer still varies from pulse to pulse. Because SOAs cannot fully recover between consecutive pulses, the first pulse in a train induces a larger phase difference than do subsequent pulses and consequently switches a larger proportion of the probe power, resulting in the familiar "patterned" output characteristic of SOA-based gates operating at rates of 40Gb/s and above.

One approach to the problem is to increase the effective speed of the gate with an ensuing component, which may be either an offset filter after the interferometer [2] or an additional SOA in the "Turboswitch" configuration [3]. Here, however, as first reported in [4], we make use of an inverted input signal in order to present both SOAs in a Mach-Zehnder gate with near constant input energy in every bit period, thus removing the initial cause of patterning. A complementary pair of signals was generated by a modified form of Mach-Zehnder gate developed for the purpose and, with these signals, the pattern compensation scheme was implemented in a second gate. The probe to the first gate can be either a stream of pulses, in which case the two complementary signals both have an RZ format, or a CW input, in which case the inverted signal has a varying level and resembles the modulated holding beam used in a previously reported pattern compensation scheme [5].

Another scheme, applicable to XOR gates, that employed complementary input signals to reduce patterning has achieved 86.4Gb/s operation [6]. A regenerator based on two stages of cross-gain modulation has also made use of complementary signals to avoid patterning by ensuring that the power in the second stage remained constant [7]. However, by removing the power variations within each bit period, this system also cancels the phase changes that would be needed in an interferometer-based gate.

The scheme described here uses the inverted signal to provide pattern compensation without switching the gate. As a result, it is applicable to a variety of gates exploiting the cross-phase modulation induced by an RZ signal in a Mach-Zehnder interferometer (MZI). In this paper, we present numerical simulations that elucidate the operating mechanism together with new experimental results.

2. Principle

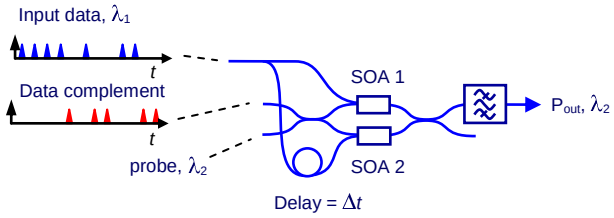

Fig. 1. Pattern compensation scheme applied to an SOA-MZI gate.

2.1 Pattern compensation

Patterning arises in an SOA-MZI gate because the SOAs do not receive the same input energy in each bit period when they are being switched by an arbitrary data signal. However, if the logical complement of the data is also applied to each SOA, then the total input energy per bit period can be made constant. The data complement must be prevented from also switching the device and this may be achieved by applying it to both SOAs simultaneously, e.g. through an input to the interferometer (Fig. 1). When the input data is a 1, the first SOA receives a "push" pulse and the second SOA receives a "pull" pulse after a short delay, causing the device to switch for the inter-pulse interval in the normal way. When the input data is a 0, both SOAs receive a pulse simultaneously and no switching occurs (Fig. 2). Thus both SOAs receive the same pulse energy in every bit period with just a small variation in arrival time. The SOA gains are therefore close to the same values at every pulse arrival and patterning is

substantially reduced. Push-pull operation is a necessary part of the compensation scheme and so the input data must have an RZ format.

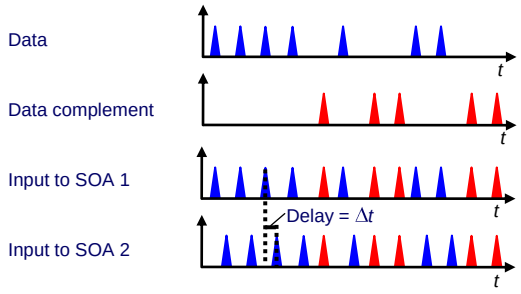

Fig. 2. Inputs received by SOA 1 and SOA 2.

An anticipated additional benefit of this scheme is that it will become less important to minimise the recovery time of the SOAs by operating them at high bias currents, which offers the prospect of SOA-based gates with lower power consumption.

2.2 Derivation of complementary signals

A prerequisite for the implementation of this scheme is a complementary pair of input signals and there are various means by which these may be obtained. The inverted signal could be generated from the data using cross-gain modulation in an SOA [5]. Alternatively, complementary signals may be available from the device preceding the gate in the system. For example, when differential phase-shift keyed (DPSK) signals are received, they are decoded with the aid of an interferometer which generates complementary amplitude-modulated signals at its two outputs. Logic gates employing interferometers can also produce complementary outputs. We have designed a novel form of the SOA-MZI gate that allows independent optimisation of the data and data complement outputs (Fig. 3).

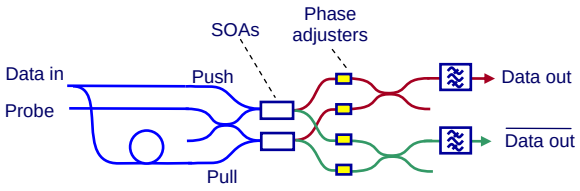

Fig. 3. SOA-MZI gate with independently optimised outputs.

Comparison with the conventional form of the gate (as in Fig. 1), shows that the modified gate has a second MZI partly overlaid on the first. The phase differences between the arms in the two interferometers can be adjusted separately to obtain the best extinction ratios for the data and its complement. Proper complementary outputs can only be obtained from a single interferometer when the phase difference induced during switching is exactly π radians for every data pulse.

3. Numerical simulation

In order to illustrate the operation of the compensation scheme, a simulation was carried out using a rate-equation based SOA model similar to that presented in [8]. First the gate was simulated without pattern compensation. A short sequence of 40Gb/s data consisting of 3ps pulses with mean power 3.5dBm served as the input data and a -10dBm CW probe was used. The split of the input power between SOA 1 and 2 and the phase difference between the arms of the interferometer were adjusted to give an output with good extinction ratio and minimum

patterning. The delay between the push and pull inputs was set to 6ps. Both SOAs were biased at 300mA.

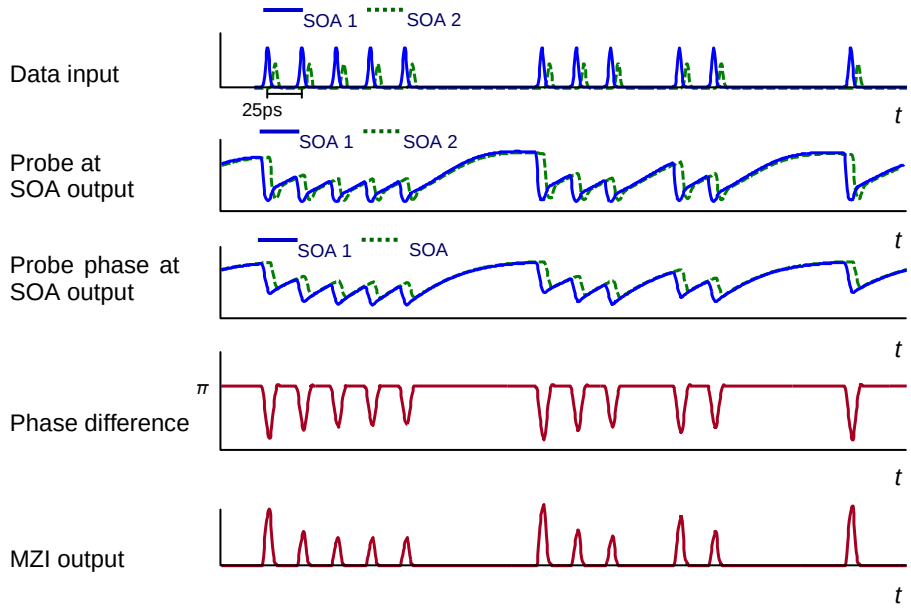

Fig. 4. Simulation of a conventional SOA-MZI gate showing patterned SOA responses and output.

The amplitudes and phases of the amplified probe signals at the outputs of SOA 1 and 2 are shown in Fig. 4. From these the phase difference and the resultant signal at the MZI output were calculated. At this bit rate, the probe amplitude and phase could only recover to steady-state levels when there were three or more consecutive zeros, so the response to a data pulse depended on the values of the previous few bits. In particular, a large phase change was induced by the first bit in a train of pulses but the subsequent phase changes became progressively smaller. The phase difference created between the MZI arms during each switching window therefore varied, despite the good cancellation between switching windows. Consequently the output pulse heights showed significant patterning.

The simulation was repeated with a 3dBm mean power data complement signal, also comprising 3ps pulses, split equally between the two SOA inputs (Fig. 5). The SOAs now received a pulse in every bit period and as a result underwent almost the same gain and phase excursions in every period. During a 1, the push-pull delay resulted in a phase difference between the two SOA outputs for the duration of the switching window, but the phase changes during a 0 were simultaneous. Now the phase differences created by the data pulses in each switching window were almost identical, yet the phase variations induced by the data complement pulses were accurately cancelled. As a result, the output of the MZI showed negligible patterning.

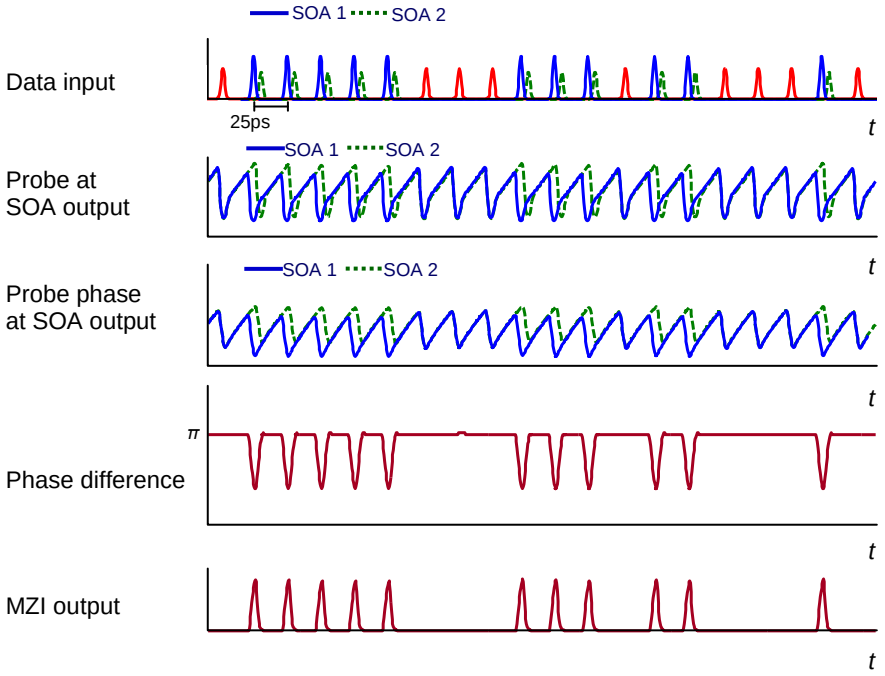

Fig. 5. Simulation of an SOA-MZI gate with pattern compensation.
(Data complement shown in red with data inputs.)

4. Experimental system

4.1 Return-to-zero compensation signal

A pair of SOA-MZI gates having the configuration described in Section 2.2 was fabricated by CIP Technologies using their hybrid-integration process [9]. The first gate provided complementary output signals with which pattern compensation was implemented in the second gate (Fig. 6). The inputs to the first gate were obtained from a 2^7-1 pseudo-random bit stream (PRBS) of 3ps pulses at 42.6Gb/s, which was divided into push and pull inputs. A pair of optical attenuators at the input together with the integrated phase adjusters enabled the output signal to be optimised [10]. Signal powers and wavelengths are shown in Table 1. The probe input was a train of 2ps clock pulses at 42.6GHz. The currents for the SOAs in the push and pull arms were 400mA and 360mA respectively. One of the interferometers in the first gate was phase-biased to give a non-inverted output which was amplified and split to provide push and pull inputs for the second gate.

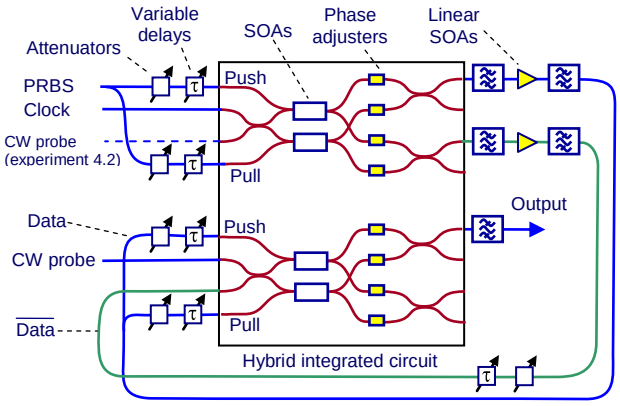

Fig. 6. Experimental system.

The second interferometer of the first gate was biased to produce an inverted data output to act as the compensation signal. Being composed of switched clock pulses, it was an RZ signal like the non-inverted data output. This signal was also amplified and connected to the second gate through an interferometer input to ensure that it reached both SOAs simultaneously.

The delay between the push and pull pulses in the second gate was 10ps and the compensation signal was synchronised with the centre of this interval. A CW source was used as the probe. Both SOA currents were set to 400mA and their 1/*e* recovery times were estimated at 40ps under the experimental conditions. The final output was taken from one of the interferometers in the second gate, which was biased to give a non-inverted signal with a mean power of -6.0dBm.

Table 1: Signal powers and wavelengths for RZ compensation signal experiment.

Gate 1	Wavelength (nm)	Power (dBm)	**Gate 2**	Wavelength (nm)	Power (dBm)
Push input	1553	-1.8	Push input	1565	-0.8
Pull input	"	-4.0	Pull input	"	-3.5
Clock	1565	-2.5	Compensation input	"	-0.6
Data out	"	0.3	CW probe	1553	-0.2
Data complement	"	0	Data out	"	-6.0

4.2 Return-to-on compensation signal

In the experiment just described, the compensation signal had an RZ format only because the probe in the first gate consisted of a train of clock pulses, but it is often more convenient to use a CW probe. In that case, although the data output from the first gate would remain in the RZ format, the inverted output would take the form of a "return-to-on" signal. That is, its output power would be nulled during the switching window and have a varying on-level between switching windows as the SOA gains recovered.

Accordingly, a second experiment was performed in order to establish whether such a signal could act as a compensation signal. A CW probe was applied to the second interferometer input of the first gate, in addition to the clock probe already connected (Fig. 6). Two probes were used in order to generate the data and compensation signals at different wavelengths, thus preventing interference in the second gate in the event of incomplete extinction of either signal. (Both probes could have been CW inputs, but it was

experimentally expedient to retain the clock.) The filters at the inverting output of gate 1 were retuned to the CW wavelength (1553nm) and thus passed the return-to-on output to gate 2 as the compensation signal. The filters at the non-inverting output were left unchanged and continued to pass the switched clock pulses as before. The signal powers and wavelengths employed in this experiment are listed in Table 2.

Table 2: Signal powers and wavelengths for return-to-on compensation signal experiment.

Gate 1	Wavelength (nm)	Power (dBm)	**Gate 2**	Wavelength (nm)	Power (dBm)
Push input	1553	-6.2	Push input	1565	-5.0
Pull input	"	-6.7	Pull input	"	-3.8
Clock	1565	-2.5	Compensation input	1548	1.6
CW probe	1548	0.8	CW probe	1553	-0.2
Data out	1565	-4.9	Data out	"	-10.4

5. Results

5.1 Return-to-zero compensation signal

The output of gate 2 was recorded with both an optical sampling oscilloscope and with a 70GHz electronic oscilloscope (Fig. 7). Before the compensation signal was connected, the output showed a variation between the maximum and minimum pulse amplitudes of 3.2dB, a degree of patterning that might be expected after the passage of the signal through two successive gates. Connecting the compensation signal reduced the variation to 1.0dB.

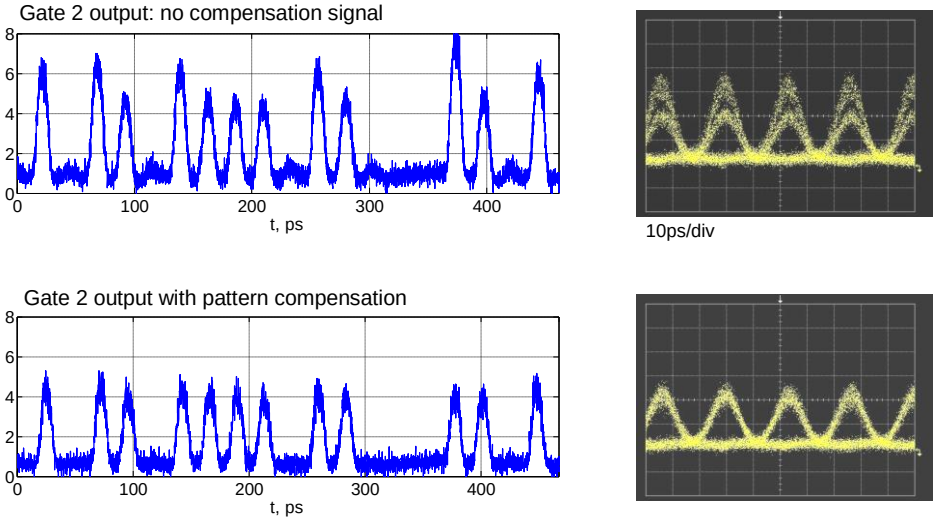

Fig. 7. Waveforms (optical sampling oscilloscope) and eye diagrams (electronic oscilloscope) with no compensation and with an RZ compensation signal.

5.2 Return-to-on compensation signal

For this experiment, the outputs of both gates were recorded (Fig. 8). The variation in pulse amplitude after gate 1 was 2.4dB. Without compensation, this was little changed by passing

through gate 2, but it is noticeable that the pulse amplitude then fell to its minimum value even for the second pulse in a train.

The compensation signal produced by gate 1 shows clear nulls during the switching windows, but a widely varying power level between windows. Nevertheless, when connected to gate 2 it caused a substantial reduction in the output patterning. Although the variation in pulse amplitude was still 1.7dB, it was less than that on the output from the first gate.

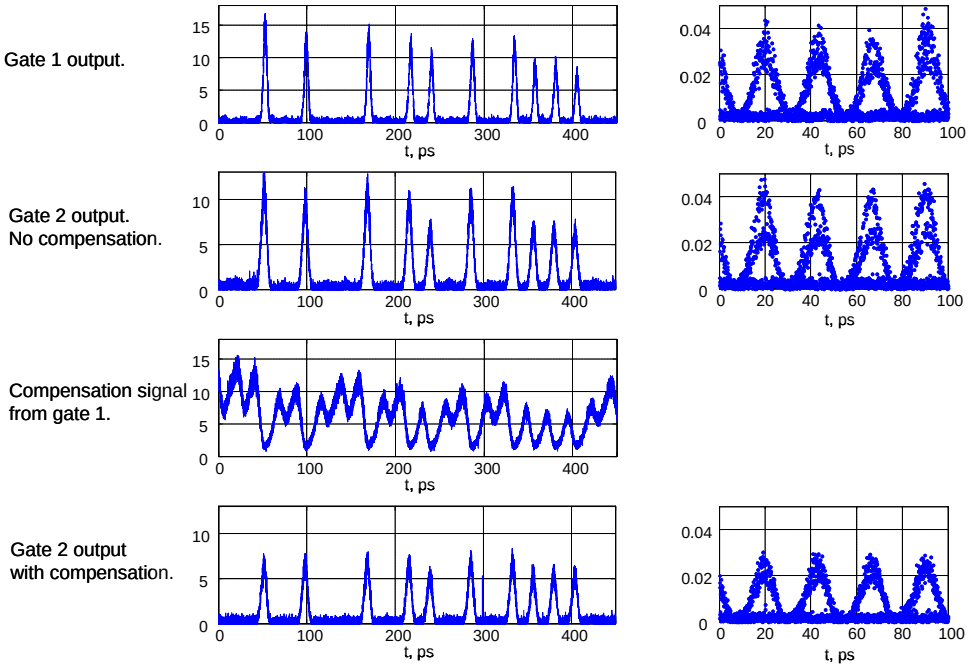

Fig. 8. Waveforms (optical sampling oscilloscope) and eye diagrams (electronic oscilloscope) with no compensation and with a return-to-on compensation signal.

6. Conclusions

We have proposed a novel scheme for preventing the output patterning that normally occurs in SOA-based gates. It is applicable to the widely used SOA-MZI configuration and makes use of the complement of the input data to equalise the pulse energies received by SOAs in each bit period without causing unwanted switching. Nothing in the scheme reduces the operating speed of the gate and it should therefore be applicable at the highest speeds of which this type of gate is capable.

The scheme has been experimentally demonstrated at 42.6Gb/s with both RZ and return-to-on compensation signals that were obtained from a preceding gate with a novel structure designed for the purpose. The RZ compensation signal gave the better performance, but in both cases, a substantial reduction in patterning was observed when the compensation signal was connected. Patterning was reduced to a level below that on the signal received from the uncompensated first gate, showing that the scheme not only prevented the second gate from causing additional patterning, but also compensated for the patterning already introduced.

Acknowledgement

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