Investigation and Design of Key Circuit Blocks in a 10 bit SAR ADC at 100 MS/s

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by

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Abstract

The work in this thesis is based on the investigation and design of key circuit blocks in a high speed, high resolution SAR ADC in TSMC's 28nm technology. The research carried out analyses the circuit limitations of the switched capacitor DAC and the settling problems of the reference voltage associated with a switched capacitor scheme.

The switched capacitor DAC is a critical block for overall ADC performance and various trade-offs are weighed up before discussing the layout of the split capacitor DAC implemented in the project, from unit capacitor up to top level routing. It also investigates the main sources of error using this topology and implements effective ways of mitigating these errors. The schematic design of DAC switches is also carried out and the results section discusses the top level linearity performance of the DAC.

This work also focuses on detailed analysis and implementation of a reference buffer circuit solution that is capable of supplying a reference voltage that is highly accurate and can settle in enough time for the high speed and high resolution specifications required by the SAR ADC. Various solutions were comprehensively investigated for this problem and the design of the chosen flipped voltage follower topology was implemented in schematic and layout. It was subsequently simulated at schematic and extracted parasitics level to verify its functionality and determine its overall performance. Finally, the work done in each block is verified in the context of the whole ADC by top level schematic and extracted layout simulation.

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Declaration

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Name: Gerald O' Sullivan

Date: July 2018

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Acronyms

ADC	Analogue to Digital Converter
BBM	Break-Before-Make
CDAC	Capacitive DAC
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital to Analogue Converter
DEM	Dynamic Element Matching
DNL	Differential Non-Linearity
ENOB	Effective Number of Bits
INL	Integral Non-Linearity
MIM	Metal-Insulator-Metal
MOM	Metal-Oxide-Metal
NMOS	N-type Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor
SAR	Successive Approximation Register

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1 Introduction

The purpose of this thesis is to investigate the various challenges faced in the design of a Successive Approximation Register (SAR) Analogue to Digital Converter (ADC). The work done on this project was carried out as a part of a high resolution noise-shaping ADC on 28 nm silicon. The objective of this project was to achieve at least 15 bit resolution for a 1 MHz input signal at a sampling rate of 70 MS/s. Using a lower resolution DAC (Digital to Analogue Converter), the noise shaping circuits shape or High Pass filter the quantization noise of the DAC and the comparator noise to obtain a higher resolution than the resolution of the SAR core.

There are many challenges faced in the design of a SAR ADC due to the complexity of the design and the tight design constraints that are necessary to ensure optimum performance. Various trade-offs, such as resolution, speed, power and area must be made in order to meet these specifications and this adds to the challenge of choosing the right solution to each problem faced over the course of the design. This Masters project involved designing the Capacitor DAC, corresponding switches and the provision of a stable reference voltage in order to help achieve the defined specifications of the overall SAR ADC. These challenges and their corresponding solutions will be discussed in depth throughout this thesis.

The main target specifications of the ADC are summarized in Table 1.1 below:

Table 1.1 ADC Target Specifications

Specification	Target Value
Technology	TSMC 28nm
Resolution without shaping (ENOB)	10 bits
SAR clock rate (synchronous)	1.5 GS/s
Sample Rate	100 MS/s
Input Signal Bandwidth	1 MHz
SNDR @100kHz	90 dB
Supply Voltage	0.9 V
Resolution with shaping (ENOB)	>15 bits
Power without ref. buffer (mW)	5
Power with ref. buffer (mW)	15

The performance of a SAR ADC is defined by its static (low frequency) and dynamic (high frequency) behaviour:

- **Differential Non-Linearity (DNL):** In an ADC, it is the difference between an actual step width and the ideal LSB width.

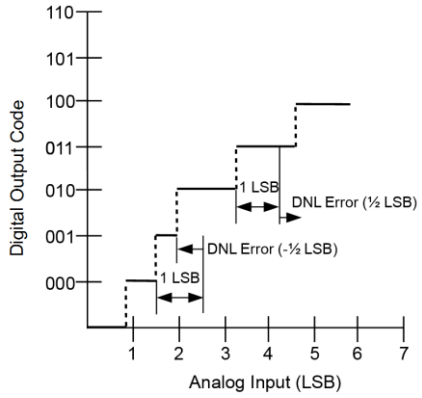

Figure 1.1 DNL Error of an ADC

- **Integral Non-Linearity (INL):** In an ADC, it is the deviation of the values of the actual transfer function from a straight line. This straight line is either the line of best fit or from the first and last point in the ramp, with offset and gain removed.

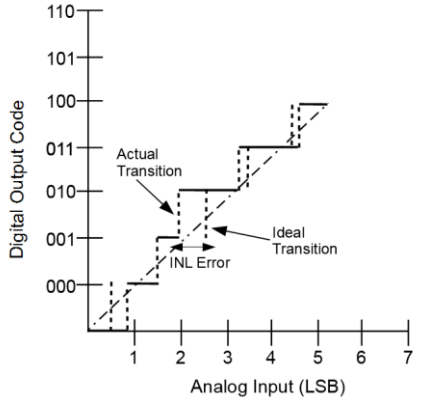

Figure 1.2 INL Error of an ADC

- **Signal to Noise Ratio (SNR):** It is the ratio of the amplitude of the desired signal to the amplitude of all the noise signals. In a low power ADC it is usually dominated by thermal noise. It is calculated from the frequency spectrum of the ADC output for a coherent tone input.

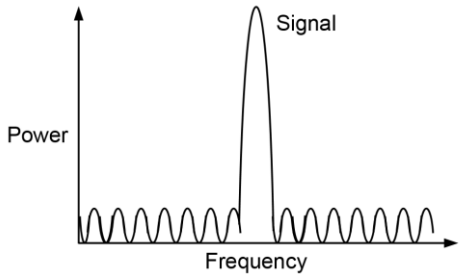

Figure 1.3 Signal to Noise Ratio Illustration

- **Signal to Noise and Distortion (SINAD):** This is a measure of the ratio of the RMS value of the sinewave to the RMS value of all the noise signals plus distortion.

- **Spurious Free Dynamic Range (SFDR):** It is the ratio of the RMS amplitude of the required signal to the RMS value of the next largest spurious component.

- **Effective Number of Bits (ENOB):** The resolution of the ADC denotes the number of bits used to represent the analog value, while the ENOB denotes the resolution of an ideal ADC that would give the same effective resolution. It is dependent on the total noise and distortion present in the ADC [1].

$$ENOB = \frac{SINAD - 1.76}{6.02} \tag{1.1}$$

1.1 SAR ADC Background

An ADC is one of the most important electronic devices in modern technology, in that it provides an interface between continuous signals in the real world and digital data storage and processing in the digital world. It does this by converting a continuous input voltage into a number of discrete steps, which are each assigned a digital code. The first step is sampling, where the signal is taken at periodic time intervals but still has continuous time amplitudes. The second step is quantization, where the signal is converted to discrete voltage levels [2]. Sampling involves switching an analogue signal onto a capacitor at a discrete time step. Quantization converts a discrete time analogue voltage signal into a discrete time, discrete voltage signal by successively comparing it to DAC digital outputs. This digital data can now be easily processed by micro-controllers and important information can be garnered and utilized for a wide range of applications.

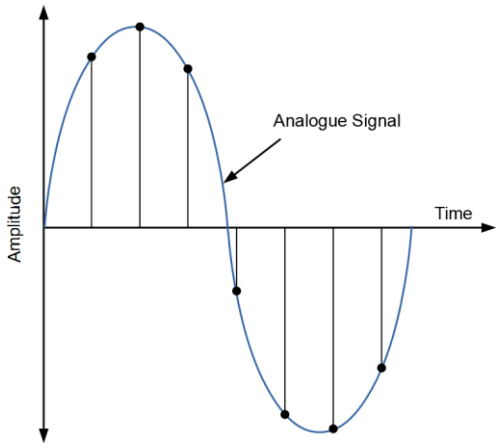

Figure 1.4 Sampled Signal

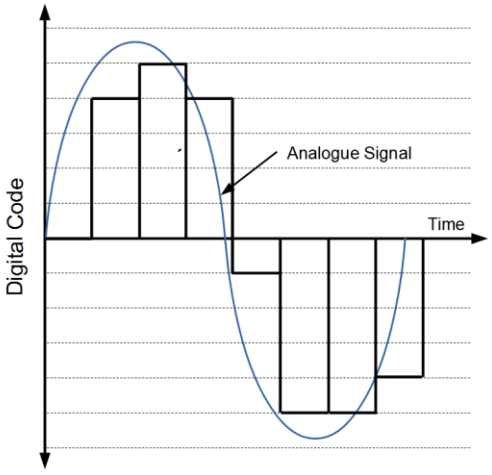

Figure 1.5 Quantised Signal

The table below compares the State of the Art for high precision ADCs converting 1 MHz signals. Most of them use Sigma Delta architectures, either Continuous Time (SDCT) or Switched Capacitor (SDSC). The novel architecture used in this project implements a SAR core ADC to achieve state of the art precision at equal sampling speed.

Table 1.2 Comparison of recent State of the Art High Precision ADCs

Reference	**Ho** [3] 2015	**Brewer** [4] 2005	**Silva** [5] 2006	**Bannon** [6] 2014	**Bandyopadhyay** [7] 2014
Architecture	SDCT	SDSC	SDCT, Complex	Pipeline, SAR	SDCT
Fs (MHz)	140	20	41.7	5	57.5
Fin (MHz)	2.2	1	0.2	0.001	0.6
OSR	32	10	104	1	48
SNDR (dB)	90.4		90	98.6	
SNR (dB)		100		99	97.3
Power (mW)	4.5	475	210	30.5	21
Walden FOM (pJ/con step)	37.8	2905.2	20310.5	87.7	678.2
Schreier FOM (dB/J)	177.3	163.2	149.8	177.7	164.6
Technology (nm)	55	250	180	180	180
Area (mm^2)	0.09	20.21	6	5.74	0.99

In the last ten years, SAR architecture has become a major design involved in advancing the state of the art in analog-to-digital conversion. One of the major reasons for this is that SAR ADCs rely on MOS switches and latches, which have greatly benefitted from technology scaling [8]. They also use switched capacitor DACs, which benefit from good matching and no static power consumption. SAR ADCs are frequently chosen as a viable architecture for medium to high resolution applications with sample rates under 5 MS/s. The resolution of these devices commonly range between 8-16 bits, with comparatively low power consumption as well as a small form factor [9]. Due to their sequential nature, the best performing SAR ADCs have around 10 bit resolution

Compared to other architectures, SAR ADCs are very power efficient for medium accuracies. This benefits from their simple design which can allow lower supply voltages to be used [10]. These obvious advantages and the flexibility they provide make this architecture very popular for a wide array of applications.

A SAR ADC consists of a sample and hold circuit, which samples the input voltage onto a capacitor, using switches. This allows a constant input voltage sample to be maintained during the conversion [2]. This is then followed by a comparator which compares an input signal with a reference voltage [11]. In this way, it generates the bits by successive approximation [2]. This comparator output is fed to the Successive Approximation Register, which functions to perform the binary search algorithm to sequentially determine the value of each bit based on the output of the comparator and supply the DAC with a digital approximation voltage. It takes N clock cycles to obtain all N bits of the

digital code [12]. This is shown below in Figure 1.6 and the successive approximation of a 5 bit SAR ADC is illustrated in the timing diagram in Figure 1.7.

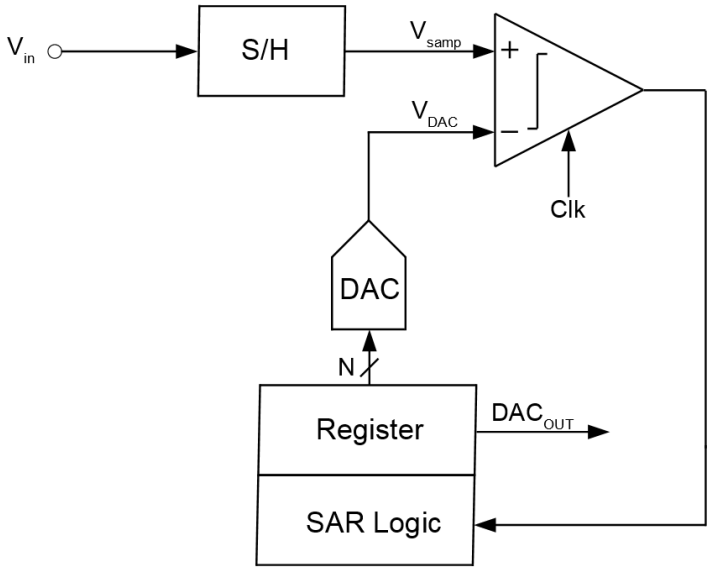

Figure 1.6 SAR ADC Functional Diagram **[9]**

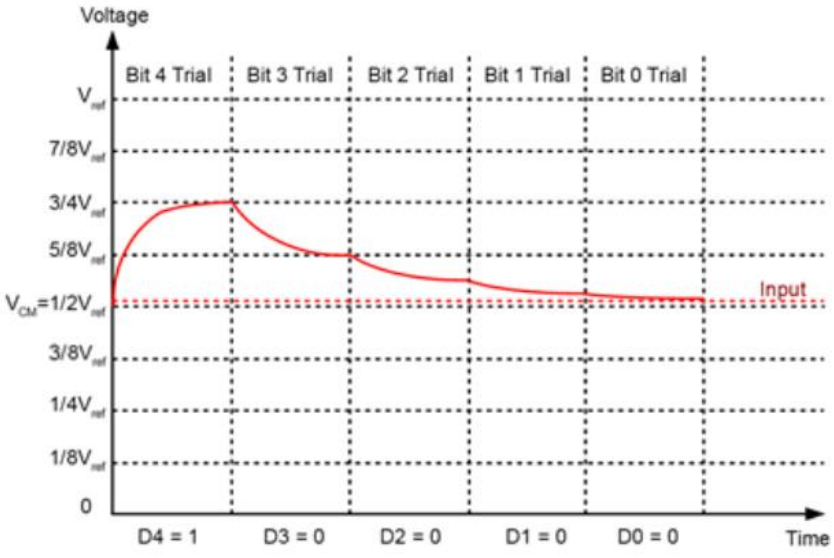

Figure 1.7 SAR ADC Successive Approximation Timing Diagram (5 bits**)**

1.2 Capacitive DAC

A DAC is an integral part of a switched capacitor SAR ADC. It converts the digital code generated by the comparator to an analogue signal and this signal is compared with the analogue input signal during bit cycling to successively approximate the correct digital code. As a result, the accuracy of the overall ADC is very dependent on the accuracy of the DAC. The DAC can be implemented as a capacitor based, switched current or R-2R ladder DAC. The reasons for choosing the capacitive DAC were the zero quiescent current and better matching capabilities of capacitors over resistors [13]. Charge redistribution DACs set an output voltage proportional to the ratio of the capacitance switched to Vrefp and the total capacitance. Another advantage of using a capacitive charge redistribution DAC is that the input signal can be sampled onto the capacitive DAC, taking away the need for having a separate sample and hold circuit, saving area on chip [14].

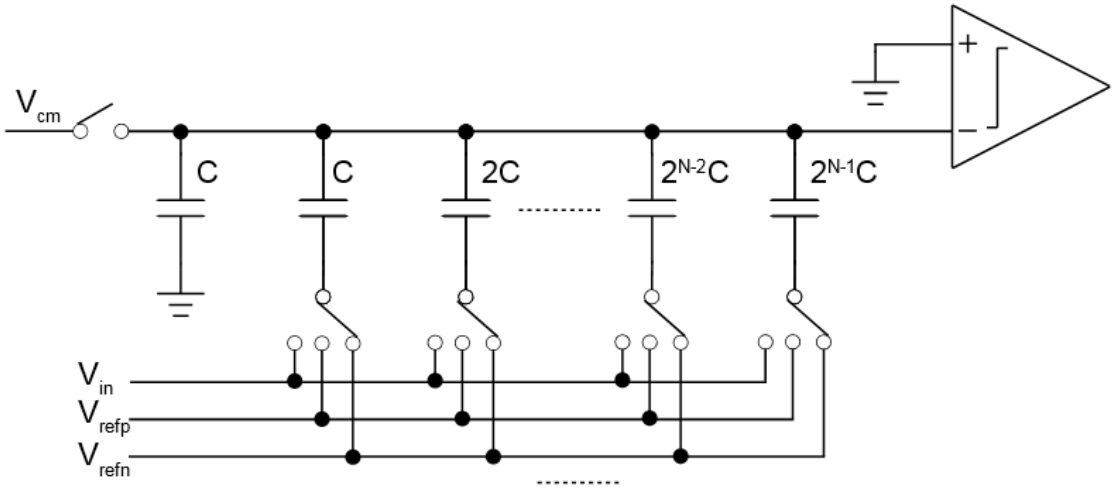

Figure 1.8 Charge Redistribution DAC Architecture

1.3 Sources of Error on Capacitor DACs

Error sources appear in two different forms on a DAC. These can be described as static error sources and dynamic error sources. Static errors determine the accuracy of the DAC and dynamic errors affect how consistent the DAC conversions will be. The impact of these errors is that an inaccurate charge distribution can occur during the conversion stage on the DAC and an incorrect analogue output voltage will be fed to the comparator.

1.3.1 Static Errors

- *Offset Error:* This error can be defined in a DAC as the step value at the output when the digital input is zero. It is a linear error, so all codes are affected equally [15]. Offset errors manifest in a SAR from offsets in the comparator or reference voltage DC offsets.

- *Gain Error:* It is defined as the difference between the nominal and actual gain points on the transfer function after the offset error has been corrected to zero [15]. It has the same percentage error on each step. It can be caused by top plate parasitic capacitances to ground.

- *DNL:* Static error sources can manifest themselves as non-linearities in the output of the DAC. A common measurement of the linearity performance in a DAC is Differential Non-Linearity (DNL). DNL measures the deviation of each step from an ideal LSB [16]. It is defined mathematically in Equation 1.2:

$$DNL(i) = \frac{V_{out(i+1)} - V_{out(i)}}{V_{LSB\_IDEAL}} - 1, where\ 0 < i < 2^{N-2} \qquad (1.2)$$

$V_{out(i)}$ is the DAC output code corresponding to the digital code input i, N is the number of bits of the DAC and V_{LSB_IDEAL} is the ideal step size between two adjacent analogue outputs [17]. A DAC is monotonic if the analog output always increases as the DAC code increases. A negative DNL causes non-monotonicity in a DAC [1]. The impact of non-monotonicity in a DAC is missing codes in the output of the SAR ADC. DNL in the DAC output codes results in noise in the ADC, reducing the overall SNR [18].

- *INL:* Another metric for non-linearity in a data converter is integral non-linearity. It is a measure of the deviation between the actual output value of the DAC and the ideal output value, essentially measuring the accumulation of errors in all the preceding codes. INL manifests itself as harmonic distortion in the SAR ADC output reducing the Spurious Free Dynamic Range (SFDR) [18]. INL is defined mathematically in Equation 1.3:

$$INL(i) = \sum_{j=0}^{i} DNL_j \, , where \; 0 < i < 2^{N-2} \qquad (1.3)$$

1.3.2 Dynamic Error Sources

Measuring static errors allows a designer to quantify the level of performance in their circuit under an ideal, fully settled, noise free environment. In reality dynamic errors, in the form of partially settled conversions and thermal noise, will limit the overall performance of a DAC. The dynamic performance of a DAC is quantified using the three metrics: Signal to Noise Ratio (SNR), Signal to Noise plus Distortion Ratio (SNDR) and Effective Number of Bits (ENOB).

- *Thermal Noise*: Thermal noise is a fundamental limitation of any analogue circuit design. Along with matching requirements, it sets the unit capacitor size of the DAC. It is a white random process, meaning that it is flat across the spectrum, giving it a random voltage signal, independent of frequency [19]. In any electrical conductor, the electrons present will experience random velocity fluctuations, caused by the thermal energy in the conductor. This will cause voltage variations across the conductor (resistor) [20]. This thermal noise power is defined mathematically as:

$$\overline{V_n^2} = 4kTR \cdot \Delta f \ \ V^2/Hz \tag{1.4}$$

Where *k* is Boltzmann constant, *T* is temperature in Kelvin, *R* is the resistance of the conductor and Δf is the bandwidth of the ADC system. The output thermal noise voltage of an RC circuit can then be defined as [20]:

$$\overline{v_n^2} = \frac{kT}{C} \ V^2 \tag{1.5}$$

- *RC Settling*: The conversion period of the DAC will set the maximum RC settling time for each conversion. Conversion time is set by the comparator decision time, logic processing time and DAC settling time. DAC settling time sets the switch sizes for the DAC. Conversion time, along with power, area and resolution considerations will dictate the capacitor sizes and the architecture used in the design. Incomplete settling during the sampling stage will produce errors in the output and effect the accuracy of the overall ADC. The finite settling time constraints are defined by the sampling capacitance, the voltage difference and the total series switch resistance. Larger capacitors are more beneficial for matching requirements and thermal noise but increasing the RC settling time constant of the circuit [21]. The figure below illustrates the incomplete settling of an RC switched capacitor circuit.

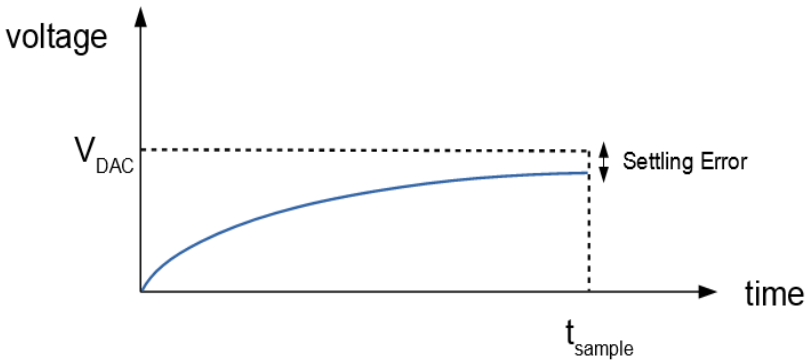

Figure 1.9 RC Settling Time Error

1.4 Voltage Reference Buffer

A stable reference voltage is one of the major requirements for an accurate SAR ADC. The reference voltage is a very precise voltage at which the input to an ADC is compared against or the output of a DAC is generated from. For a stable and repeatable data conversion it is necessary to have a non-varying reference voltage at the end of each sampling instance. This becomes an even greater requirement for higher resolution data converters, with ever smaller LSB step sizes requiring more precise reference voltages [22]. The absolute value of the reference is important for some applications where precise voltages need to be measured. For other applications the relative magnitude of different input signals is sufficient.

The biggest challenge of maintaining a stable reference voltage is the charge draw onto the capacitor after each switching instant, during conversion. This charge draw causes the reference voltage to drop and necessitates a finite time to allow the reference voltage to return to the stable and repeatable level. If an off-chip reference is supplied to the DAC, the settling is worsened due to parasitic inductances in the bond wires. The large current drawn by the capacitor array after a switching instant through this parasitic inductance causes ringing in the reference voltage which, in turn, provides an unstable reference voltage to the DAC and inconsistent output codes [23].

Decoupling capacitors are commonly used to dampen the oscillations on the reference voltage and short high frequency signals to ground. Large capacitors act as charge reservoirs for transient current and, therefore, effectively filter low frequency noise [24]. However, in order to provide a stable reference adequate for high resolution and high

speed applications, the area/power demands of the capacitor become too great due to the capacitance needed to rectify the ringing problem. Possible solutions for this problem are reservoir capacitors used in [25] and sampling the reference as described in [26].

In the following two chapters the design process of the project will be discussed. Chapter 2 details the design and optimization of the capacitive DAC and Chapter 3 describes the design and optimization of the reference buffer. In Chapter 4 the results of the projects are illustrated and discussed and, finally, chapter 5 discusses the conclusions of the work and any future work that could be based off this project.

2 Switched Capacitor DAC Design

Although advanced CMOS processes are created to build highly complex digital circuits with millions of transistors, a benefit of these technologies with their fine wire spacing is that they can achieve good capacitor densities and raw (untrimmed/calibrated) matching greater than 10 bit [27]. They also make good switches for the switched CDAC because parasitic capacitance of switches reduces with scaling, helping to improve linearity [28]. Due to these reason CMOS SARs became very popular in the 2000s [29]. The Capacitive DAC is a very important element of a switched capacitor SAR ADC. It allows sampling to be carried out before conversion, without requiring an additional capacitor. It impacts directly on the resolution of the ADC and must be designed with sampling speed, thermal noise figure, area and power in mind.

2.1 DAC Topology

Figure 2.1 shows the type of DAC implemented in the overall SAR ADC.

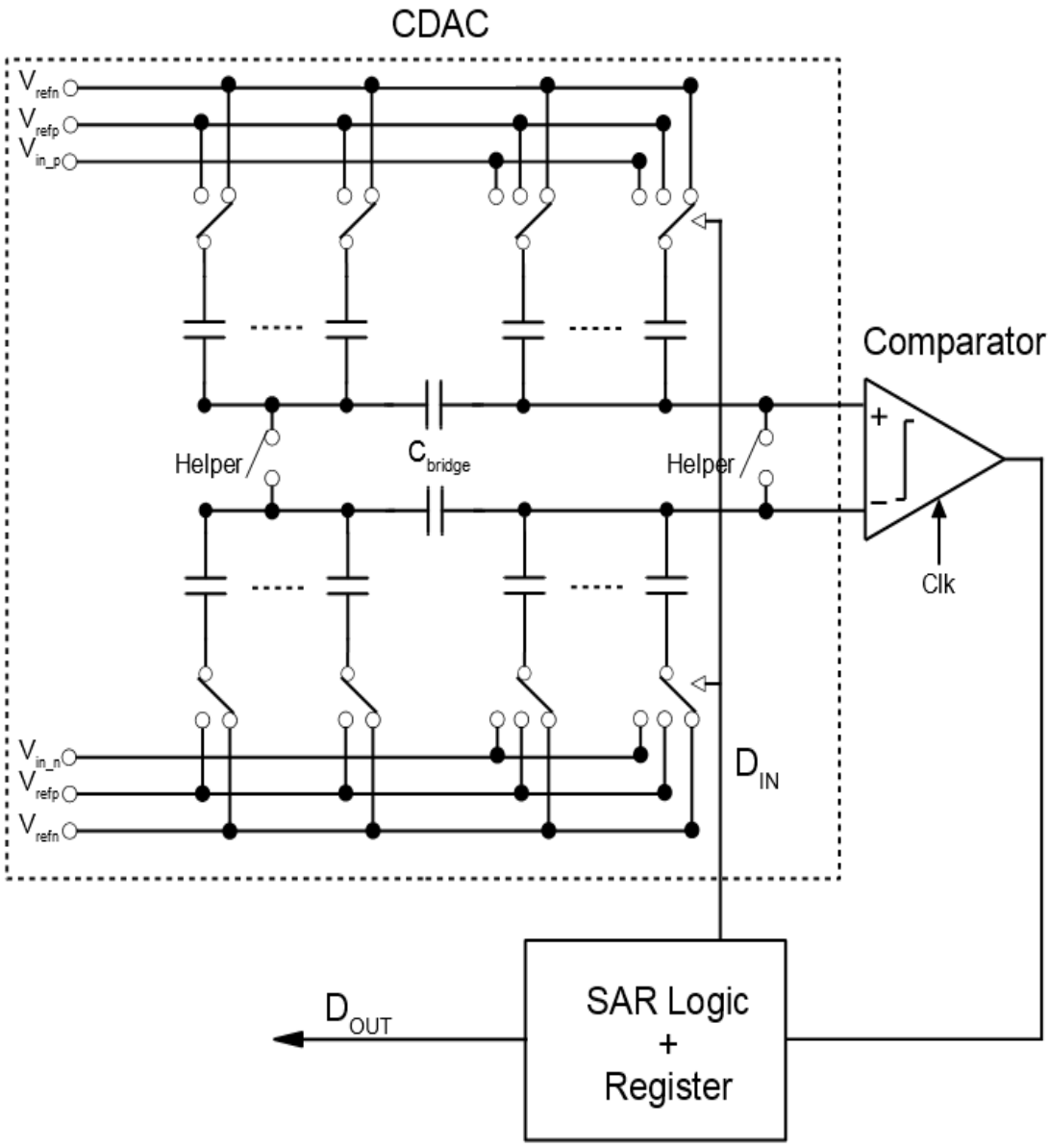

Figure 2.1 Differential CDAC & Switches

2.2 Causes of Static Errors in a DAC

- Systematic Offset: A systematic offset in the capacitor array will manifest itself as a gain error or as a DNL or INL error. The sources of systematic mismatches have the same effect on every device. Top plate parasitic capacitance to the substrate can cause a gain error or a linearity error if on the LSB side of a split capacitor array. This is explained further with diagrams in Section 2.5. If the layout of the device is precise with equal area on each capacitor and low level parasitic capacitance between each node, this problem can be mitigated with each device seeing the same percentage difference [30]. Systematic offset can also be caused by process gradients which affect each device differently and cause a mismatch between individual devices. This problem can be alleviated by ensuring that devices are close together or follow a common centroid layout so that each capacitor is affected proportionally by the process gradient [31]. The effect of systematic offsets can be largely eliminated by correct layout design procedures, minimizing inherent offsets in capacitances, bias currents, DC voltages, etc.

- Random Mismatch: This phenomenon occurs from random process variations, such as non-uniform dielectric thickness, edge variations and different doping concentrations on a device to device basis. It is a harder problem to deal with than systematic offset because they cannot be predicted before the chip has

been built. The effect of random mismatch is dependent on the device size and can be minimized by using larger devices [32].

$$\boldsymbol{\sigma\left(\frac{\Delta C}{C}\right) \propto \frac{1}{A_C}} \tag{2.1}$$

Where A_C is capacitor area, ΔC is the random variation of the unit capacitor (C) and the standard deviation of the unit capacitor mismatch is denoted as $\sigma(\Delta C/C)$ [33].

This, of course, poses its own disadvantages by increasing area, power and, potentially, settling time requirements. Random mismatch causes linearity errors and reduces the ADC ENOB. Switch capacitors are the main error sources for smaller capacitors, with wiring and switches causing more fixed errors for larger capacitor values.

2.3 DAC Capacitor Sizing

One of the biggest considerations to be made when designing a switched capacitor DAC for a SAR ADC is the sampled thermal noise. This sets the lower noise limit in the ADC. The total capacitance in the DAC determines the sampled thermal noise in the ADC as shown in the following equation:

$$V_{noise} = \sqrt{\frac{kT}{C_{DAC}}} \tag{2.2}$$

The limit of sampled thermal noise is determined as follows:

$$\sqrt{\frac{kT}{C_{DAC}}} = \frac{1}{2}\text{LSB} \tag{2.3}$$

To achieve 10 bit resolution in the DAC with V_{ref} = 0.9 V, thermal noise must be limited to:

$$\sqrt{\frac{kT}{C_{DAC}}} = 440\ \mu\text{V} \tag{2.4}$$

Solving for C_{DAC} in the previous equation (at room temperature) gives:

$$C_{DAC} = 0.02\ \text{pF} \tag{2.5}$$

A DAC capacitance of 2 pF was ultimately used, meaning that it was not limited by thermal noise. Mismatch became the limiting factor, so the unit capacitor was sized at 15 fF to ensure static performance wasn't degraded by capacitor mismatch.

2.4 Unit Capacitor Design

The sizing of the unit capacitor is one of the most critical specifications for the CDAC because it determines the level of thermal noise and mismatch in the DAC as well as area and power consumption [34]. The area of the capacitor is also important with mismatch determined by Pelgrom's inverse-area mismatch model [35]. There are two main types of Capacitors that are used in the design of CDACs. These are Metal-Insulator-Metal (MIM) capacitors and Metal-Oxide-Metal (MOM) capacitors.

MIM capacitors have comparatively good area efficiency. They do suffer from strict layout rules, however, which limit the minimum MIM capacitance to several femtofarads or tens of femtofarads. They also require special dedicated metal layers and process steps. As a result they are not supported by all process technologies [33].

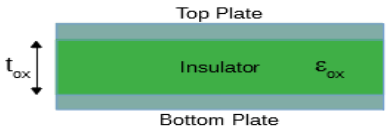

Figure 2.2 MIM Capacitor Structure

The equation below shows how the capacitance of a MIM capacitor relates to the permittivity of the dielectric, the oxide thickness and the area of each metal plate. Due to a thin, high permittivity dielectric used in MIM devices their area can be vastly reduced. As seen in the MIM model above, the capacitance is vertically between two metal layers, with the top plate protected by the bottom plate from the substrate, reducing top plate parasitic capacitance [36].

$$C = \frac{\varepsilon A}{t_{ox}} \tag{2.6}$$

MOM capacitors, in contrast, are built using standard metal interconnect layers. As a result they can be utilised in any CMOS process. They can also be custom made as parasitic elements in the layout, while only being limited in size by the metal width and metal spacing design rules of the interconnect layers [33].

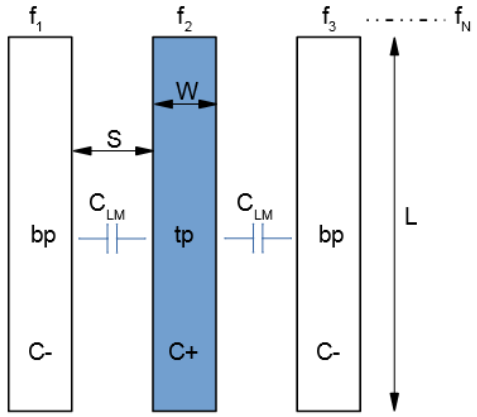

Figure 2.3 Plan View of MOM Capacitor Structure

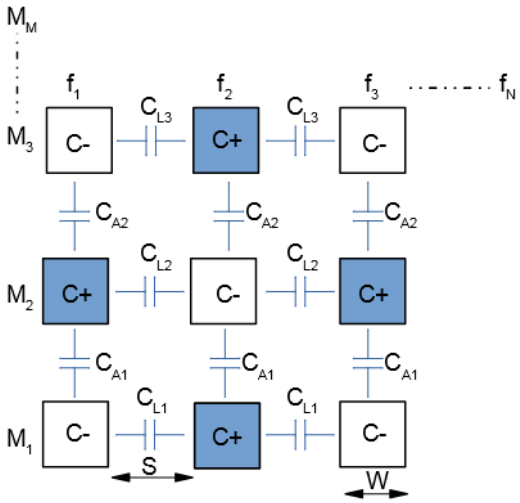

Figure 2.4 Cross-Section of MOM Capacitor Structure

The two figures above show the mechanism by which capacitance is created in a MOM capacitor with most of the capacitance between the interdigitated fingers on each metal layer and a lesser amount vertically between the layers. A smaller spacing gives higher capacitance per unit area but increases mismatch according to Pelgrom's law and is also limited by design rule lower spacing limits. The total capacitance can also be increased by increasing the number of fingers, length of fingers or number of metal layers in the MOM capacitor. Using BSIM4 models for the MOM capacitor it was decided to use a finger spacing of 0.07 µm and finger width of 0.08 µm. These were chosen as a balance between lower mismatch and lower parasitic capacitance from the area of the device.

MOM capacitors were chosen as the unit capacitor design for the CDAC in this project because it was required to build the ADC with standard (digital) CMOS, without any extra process steps being required. It was decided against using MIM capacitors because of the dedicated metal layers required and the lower size limits imposed on them, with the intention of creating a 15 fF unit capacitor. Initially, a full custom MOM capacitor design was used because of the obvious advantages of having reduced sizing limitations. However, this was later changed to a TSMC supported MOM unit capacitor (layers 3-5) with customized outer layers because of matching concerns and less design complexity, with the advantage of being able to separate the capacitance of the MOM layers from the parasitic capacitance of the extra metal layers and the routing when running parasitic extractions. The MOM capacitor used metal 3, 4 & 5 with an interdigitated structure. Four MOM capacitors were instantiated in parallel to create the unit capacitor.

The model below shows the parasitic capacitance and resistance between the bottom and top plates to the substrate. The top plate is the sensitive node because the parasitic capacitance causes a gain error, while the bottom plate parasitic capacitance merely adds extra loading to the reference signal. It is, therefore, a priority to protect the top plate from the substrate to reduce top plate parasitic capacitance.

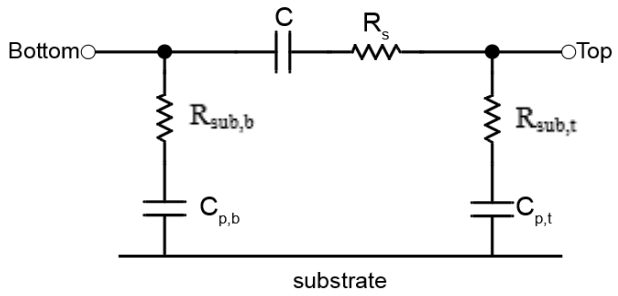

Figure 2.5 MOM Capacitor Parasitic Model

The figure below shows the interdigitated design of the unit capacitor for each metal layer with both plates of the capacitor clearly illustrated.

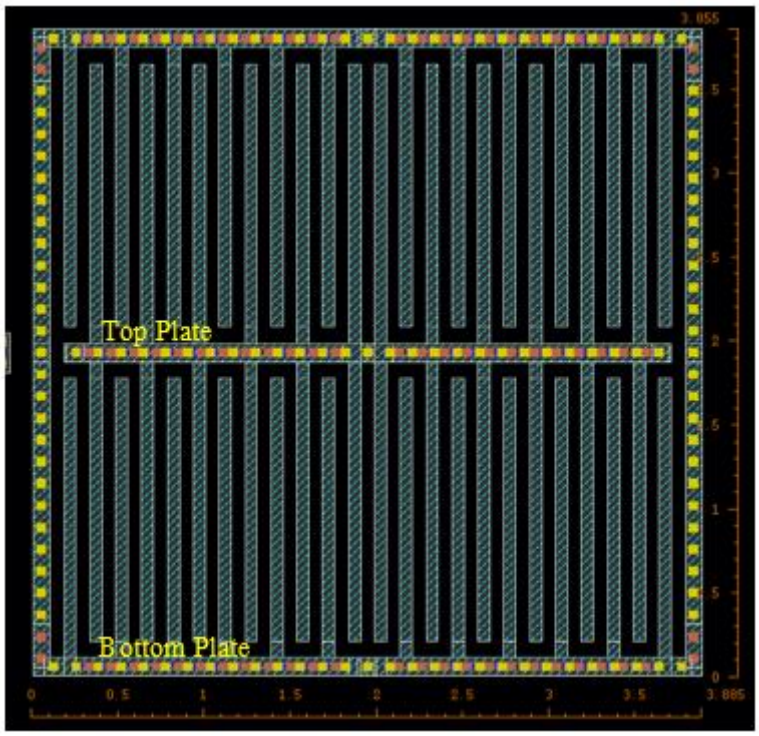

Figure 2.6 Unit Capacitor

The vias between the three MOM layers in the unit capacitors can clearly be seen as coloured boxes in the figure above. Having a large amount of them around the perimeter of the capacitor helps shield the charge on the capacitor by acting as a Faraday cage and decreases the inter-layer resistance by having multiple parallel conductive paths. Each MOM capacitor has 12 fingers, giving 24 fingers on the top and bottom half of the unit capacitor. The top plate runs along the middle of the unit capacitor, with fingers running vertically up and down. These interlink with the vertical fingers coming from the bottom plate, which surrounds the unit capacitor. In this configuration the top plate is protected

from all sides by the bottom plate and top plate parasitic capacitance is reduced. A solid metal 2 layer, connected to the bottom plate also shields the top plate of the capacitor from the substrate to minimize the parasitic capacitance between the top plate and the substrate.

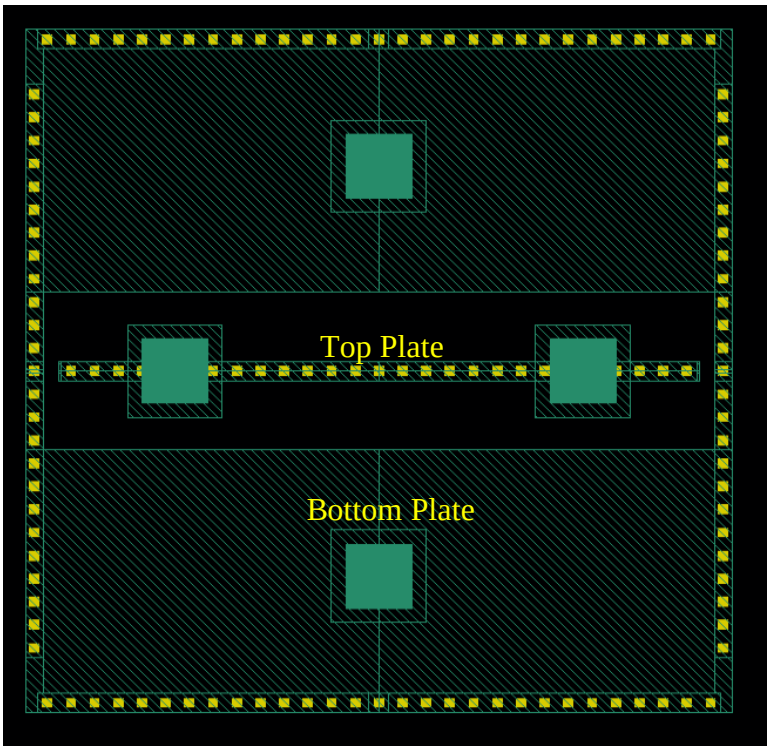

Figure 2.7 Metal 6 Layer in Unit Capacitor

The metal 6 layer was added to the unit capacitor to provide additional layer-layer capacitance and, more importantly, to shield the top of the capacitor in the same way as the vias shield the sides. The top and bottom plates are brought up from metal 5 by the yellow vias in the figure above and the turquoise vias bring the top and bottom plates up to the metal 7 routing, which will be discussed in the following section.

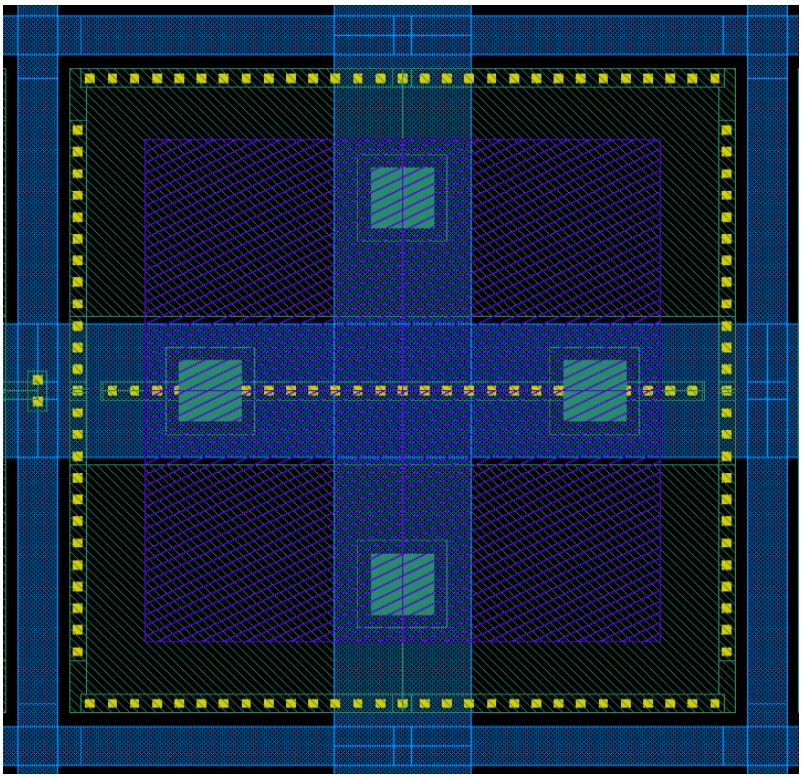

Figure 2.8 Unit Capacitor Showing Metal 6, Metal 1 & Metal 8

The blue cross in the figure above is metal 1 and is placed in the unit capacitor for density purposes. A purple metal 8 square is placed on top of the capacitor for metal density purposes and as a shield to prevent coupling to the PCB (printed circuit board) in this flip-chip design. It is disconnected electrically from the unit capacitor. Metal 8 couldn't be included in the unit capacitor because the minimum size is too big to use as a capacitor and it is placed too close to potential coupling sources to risk connecting to the capacitors. Metal 3-5, the MOM layers are hidden from this figure for clarity, as is the metal 2 layer. The metal 2 layer is the same shape as the M3-M5 layer, with the same interdigitated fingers but it is all connected together on the bottom plate node, which feeds up to metal 3 bottom plate using multiple vias. M6 and M7 are low resistance, thick metals which make them suitable for routing purposes.

2.5 Bridge Capacitor

A bridge capacitor carries out a very important function in a capacitive DAC. A capacitive array with a bridge capacitor is also known as a split capacitor array, due to the array being split into two parts. This design allows for larger unit capacitors, which improves matching. It increases speed, and has similar INL and decreased DNL in comparison to a regular binary-weighted capacitor array [37]. Implementing a split capacitor array has the benefit of decreasing the area and power consumption of the CDAC, while keeping the number of bits the same. This is implemented by using the same unit capacitor on each side of the bridge capacitor and doubling in size with each successive bit. Depending on where the bridge capacitor is located, the area can be vastly reduced, in an exponential relationship going from one end of the array to the middle of the array.

Ultimately, the size of the MSB capacitor can be decreased massively without having to have an LSB so small that it suffers from mismatch [32] and thermal noise. For higher resolution DACs, this gives a great balance between greater accuracy, with lower power consumption and area. The bridge capacitor is also known as an attenuation capacitor because it attenuates the voltage from every capacitor on the LSB side of the CDAC. This is because it is in series with the LSB capacitors [38]. I was decided to incorporate a split capacitor DAC in this design because a non-split capacitor 10-bit DAC would not have been able to satisfy the area limitation of the chip, while providing adequate accuracy.

The equivalent charge model of the split capacitor DAC is shown below with the mathematical derivations showing the relationship between the output voltage on the DAC and the individual capacitor values.

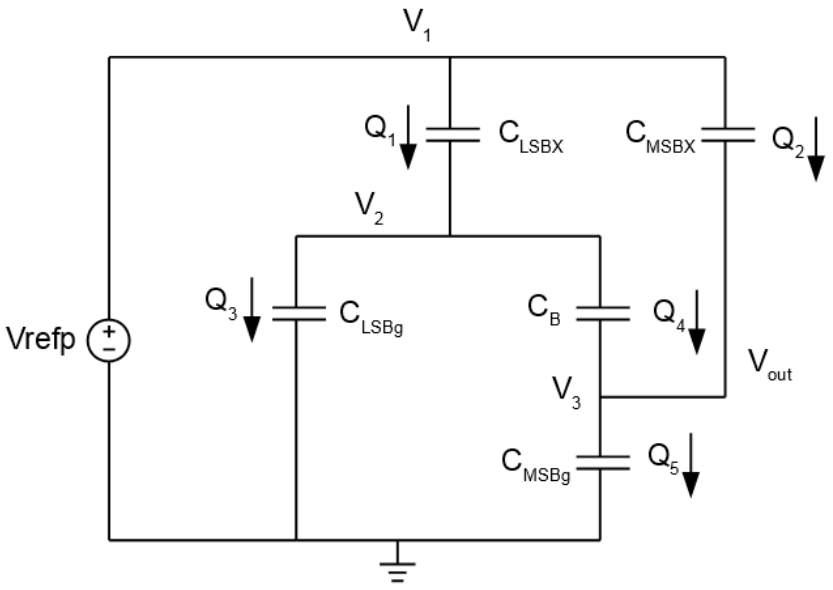

Figure 2.9 Equivalent charge flow diagram of Split Capacitor DAC

Note $C_{LSBx} + C_{LSBg} = C_{LSB}$ and $C_{MSBx} + C_{MSBg} = C_{MSB}$

$$v_{out} = \frac{V_{refp}\left(C_{MSBx} + \frac{C_{LSBx}C_B}{C_{LSB} + C_B}\right)}{C_{MSB} + \frac{C_B C_{LSB}}{C_{LSB} + C_B}}, \qquad assuming\ V_{refn} = 0\ V \tag{2.7}$$

This general formula provides a useful way of modeling the effect of a badly sized bridge capacitor on MATLAB® and the effect of top plate parasitic capacitance to ground on both the LSB and MSB arrays. It enabled the decision to orientate the bridge capacitor with the bottom plate connected to the LSB side of the CDAC because the higher parasitic capacitance to the substrate on the bottom plate has less of an effect on the output voltage. This is due to the bridge capacitor attenuating the LSB gain error. See Appendix A, section 6.1 for the full mathematical derivation of the formula.

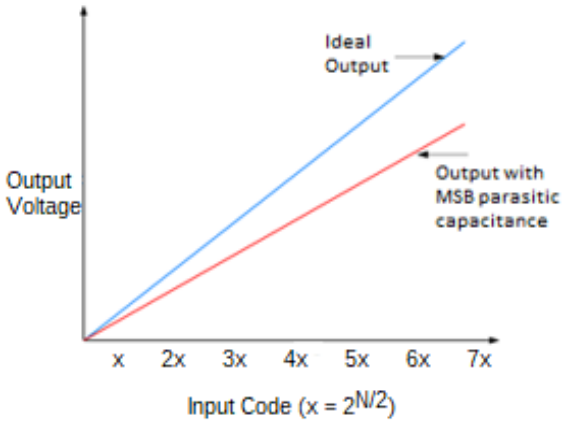

Figure 2.10 Effect of MSB parasitics on V_{out}

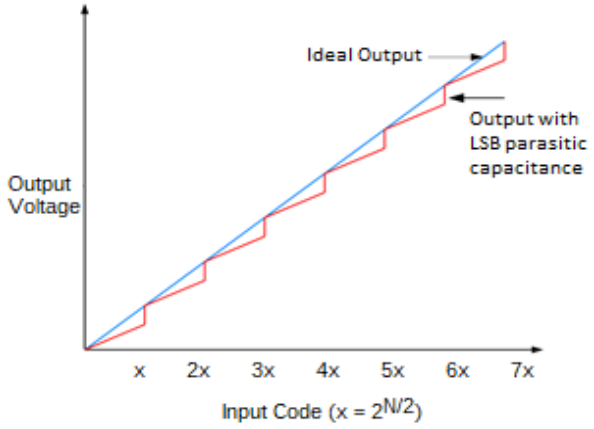

Figure 2.11 Effect of LSB parasitics on V_{out}

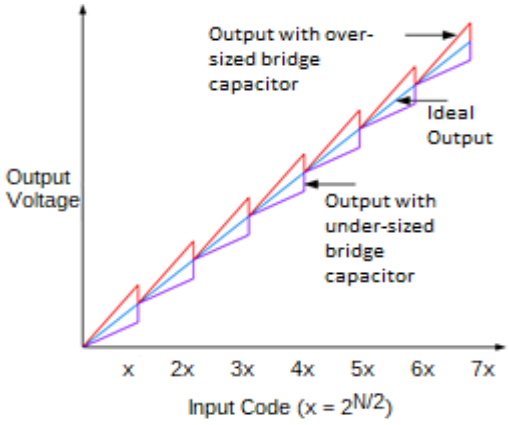

Figure 2.12 Effect of Bridge Capacitor Offset on V_{out}

As seen on figure 2.10, MSB parasitic capacitance simply causes a gain error to the output voltage. However, as seen on figure 2.11 and 2.12 above, a common problem associated with the split capacitor design is that the top plate parasitic capacitance on the LSB side of the capacitor array and the fractional value of the bridge capacitor both add uncertainty

in the output voltage of the LSB array, which limits the overall accuracy of the CDAC [39]. It is therefore very important to minimize LSB top plate parasitic capacitance to ground and bridge capacitor offset. Initially a 12 bit split 6:6 capacitor DAC was implemented but it was later reduced to 10 bit with an 8:2 split. Having the two bits on the LSB side of the bridge capacitors minimized the effects described above. Interesting resolutions to the matching problem of the fractional bridge capacitors were described by Agnes et al. in [40] who replace the fractional bridge capacitor with a unit bridge capacitor (which suffers from constant gain error) and Chen et al. in [41] who pick a bridge capacitor that is slightly larger than the required value. This can then be compensated for by a tunable ballast capacitor on the LSB array. For layout matching purposes, it was decided to use a $2*C_{unit}$ bridge capacitor. This didn't add a gain error because of the extra redundancy on the LSB array, which will be explained in the next section.

2.6 Redundancy

Redundancy provides an alternative way of mitigating the impact of settling errors in a capacitive DAC [42]. The SAR algorithm uses the overlapping steps due to redundancy to allow comparison decision errors to be digitally corrected [43]. The sampling rate imposes strict time constraints on the settling time of the DAC designed in this project and redundancy aided in alleviating the settling requirements in the bit cycling up to the redundant capacitor present in the capacitive array. This is important because the redundancy was most effective for the larger capacitors which required the most time to settle and this factored in the decision to place a 16C redundant capacitor in the MSB array. The redundancy in the LSB array helped with the bit decisions for the smallest capacitors, which were critical decisions to the final accuracy of the CDAC. Without

redundancy MSB capacitors before the redundant capacitor would have to settle to 10 bit accuracy but with redundancy they only have to settle to 6 bit accuracy, while maintaining the same overall accuracy in the SAR ADC. This relaxes the buffer settling specifications discussed in section 3.4.

The time trellis diagrams for a SAR with and without redundancy shown below describe how redundancy accommodates for incomplete settling during the bit trials in a 5 bit DAC. Without redundancy, if the settled value is below its actual value an incorrect comparison will be made that cannot be resolved in later trials. The first diagram shows that there is no margin for settling errors without redundancy but the second diagram shows that subsequent cycles can correct for errors in previous cycles, due to overlap in later cycles [29].

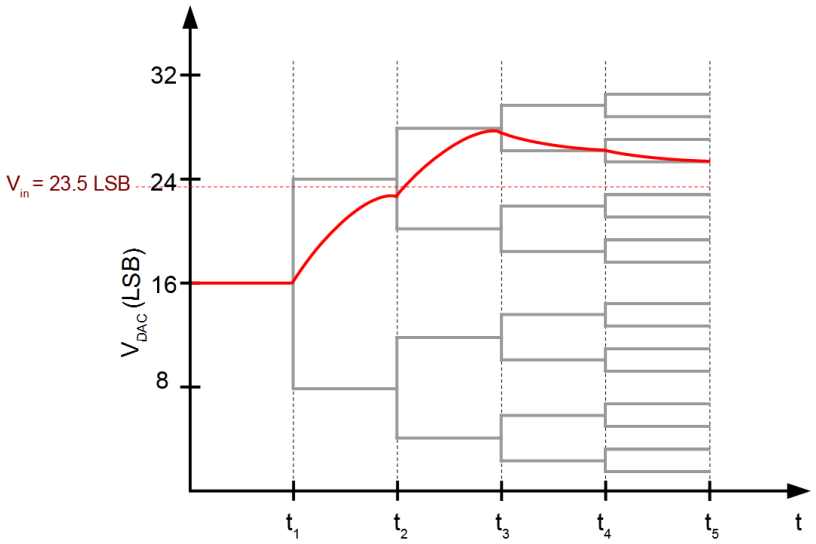

Figure 2.13 Time Trellis of Bit Trials without Redundancy

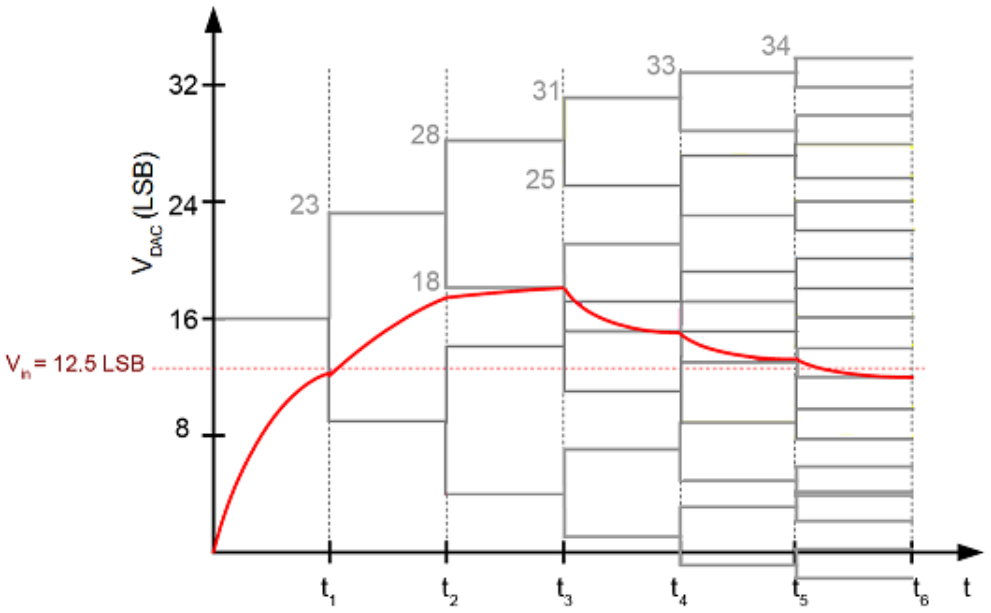

Figure 2.14 Time Trellis of Bit Trials with Redundancy

An additional comparison cycle is required for redundancy compared to the number of bits in the ADC but, crucially, absorbs errors introduced in previous decisions by allowing multiple trajectories to arrive at the final decision, as shown in Figure 2.13 and 2.14. This will be critical in this design to help correct for incomplete settling in initial bit decisions, even with the extra time taken from an additional comparison cycle.

2.7 Capacitor Routing

The top plate and bottom plate routing was a critical design challenge, impacting crucially on the matching of the individual capacitors in the DAC. Routing between individual capacitor arrays was all done on metal 7. Initially, the top plate was routed through metal 8 but this ran the risk of coupling to the substrate, affecting the linearity of the DAC. The final routing layout on metal 7 is illustrated in the figure 2.15. One vertical strip runs down

the middle, connecting the bottom plate of every unit capacitor in a column to the reference switches below the DAC. The top plate routing runs down every active capacitor in each column in two vertical strips. They are placed at either side of the bottom plate routing in order to connect each column horizontally as shown. Having a uniform routing network, with every capacitor having the same horizontal routing, minimized mismatch in the capacitor array.

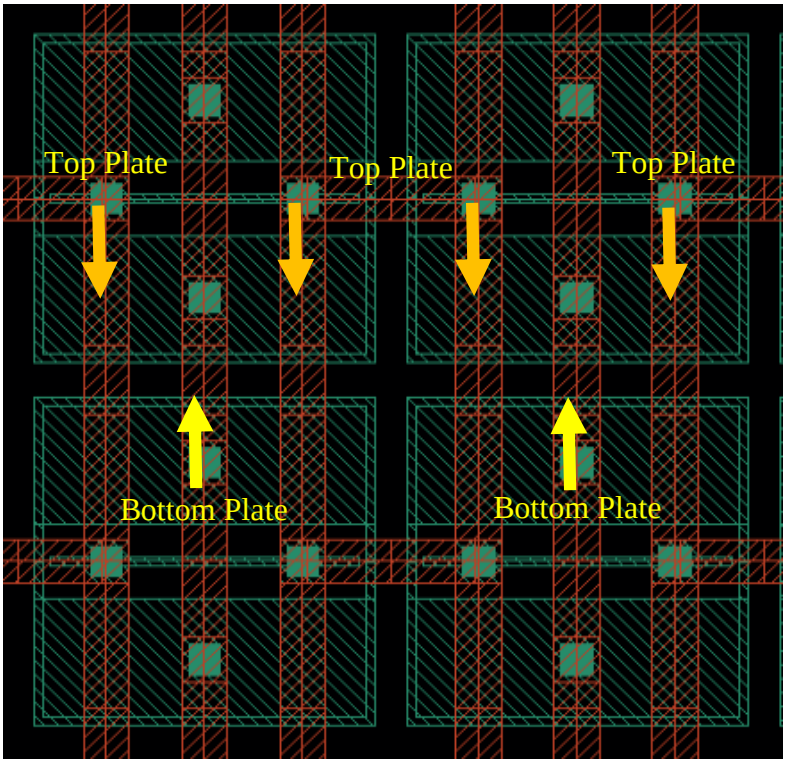

Figure 2.15 Top plate and Bottom plate routing

The placement and routing of the bridge capacitor was very important to ensure good matching and minimize gain errors due to parasitic capacitance. It was implemented as two unit capacitors with bottom plates connected in parallel to the top plate of LSB array and the top plate connected in parallel to the top plate of MSB array as shown in figure

2.16. It was placed above the 1C capacitors in both arrays to minimize extra parasitic capacitance and keep the matching at its optimum.

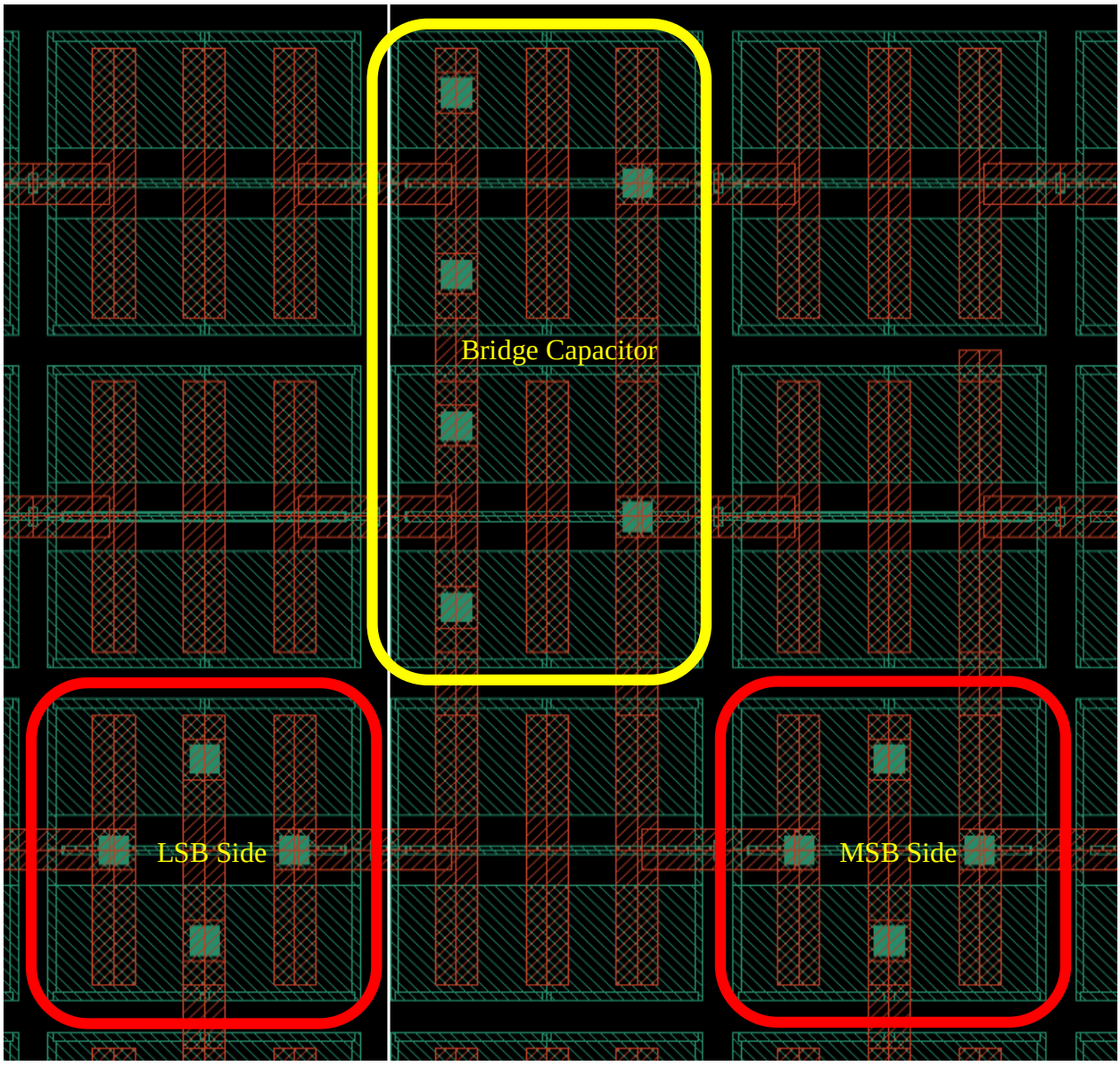

Figure 2.16 Bridge Capacitor Routing

2.8 DAC Schematic

The specific design of the CDAC is then shown in a single ended format, for ease of explanation, in the following figure. The bridge capacitor used in the DAC and its exact placement in the array had a big effect on the overall performance of the DAC and had to be carefully placed to achieve the required specifications. Redundancy was used in this capacitive DAC array and implemented in the LSB side of the array as a 2C column and in the MSB side as an extra 16C column. This allowed a more relaxed settling requirement in the larger MSB decisions. The layout structure is explained in the next section, with emphasis on achieving optimum matching between individual capacitors in the capacitor array, to achieve the schematic implantation shown in the figure below. The signal is first sampled onto the capacitor bottom plates and then transferred to the top plate. Half of the capacitors are switched to V_{refp} and half are switched to V_{refn} to transfer this charge. After this the capacitors switch to V_{refp} or V_{refn} depending on the comparator decisions. By only having the top plate switch active during Reset mode to connect V_{cm} to the top plate and then connecting the bottom plate to V_{in} during sampling, noise from V_{cm} is eliminated.

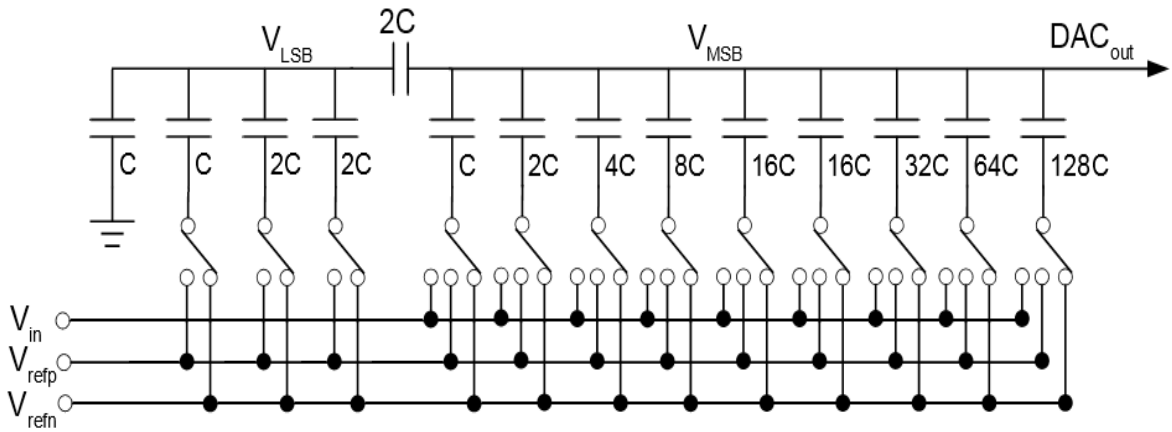

Figure 2.17 Single Ended CDAC Implemented in SAR ADC

2.9 DAC Layout Structure

The layout structure is a very important consideration for capacitive matching and for routing logistics. The MSB capacitor was split into 8 16C columns for easier routing and to allow Dynamic Element Matching (DEM) [44] to be added. The Common Centroid is a popular approach used to mitigate systematic offsets due to process gradients [31]. This approach was trialed but didn't suit the particular design because the matching in the 16 columns of 16C capacitors was best when the devices were together in a block. Splitting them caused more 16C columns to experience less parasitic coupling capacitance due to being exposed to more dummy capacitance. In addition, the smaller capacitor columns, which were placed in the middle of the 16C columns, now had a disproportionate amount of extra coupling capacitance, increasing mismatch between the devices. The asymmetric split capacitor design also made it unsuited to a common centroid approach. The capacitor columns were all placed flat at the bottom to reduce mismatch caused by the coupling capacitance of the extra routing. Three layers of dummy capacitors were placed around the perimeter of the array to provide uniformity and reduce systematic mismatch.

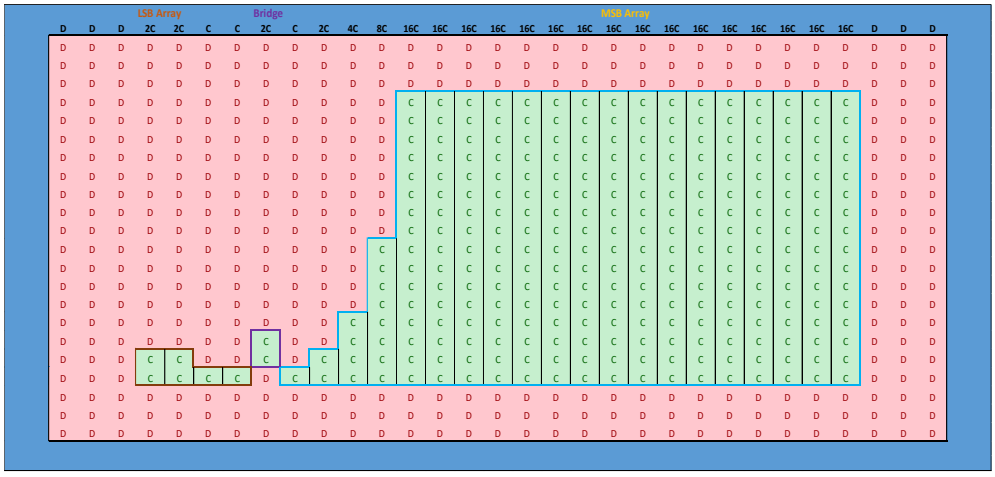

Figure 2.18 Illustration of CDAC Layout Structure

2.10 Top Level DAC Layout

The figure below shows the top level layout of the DAC capacitive array.

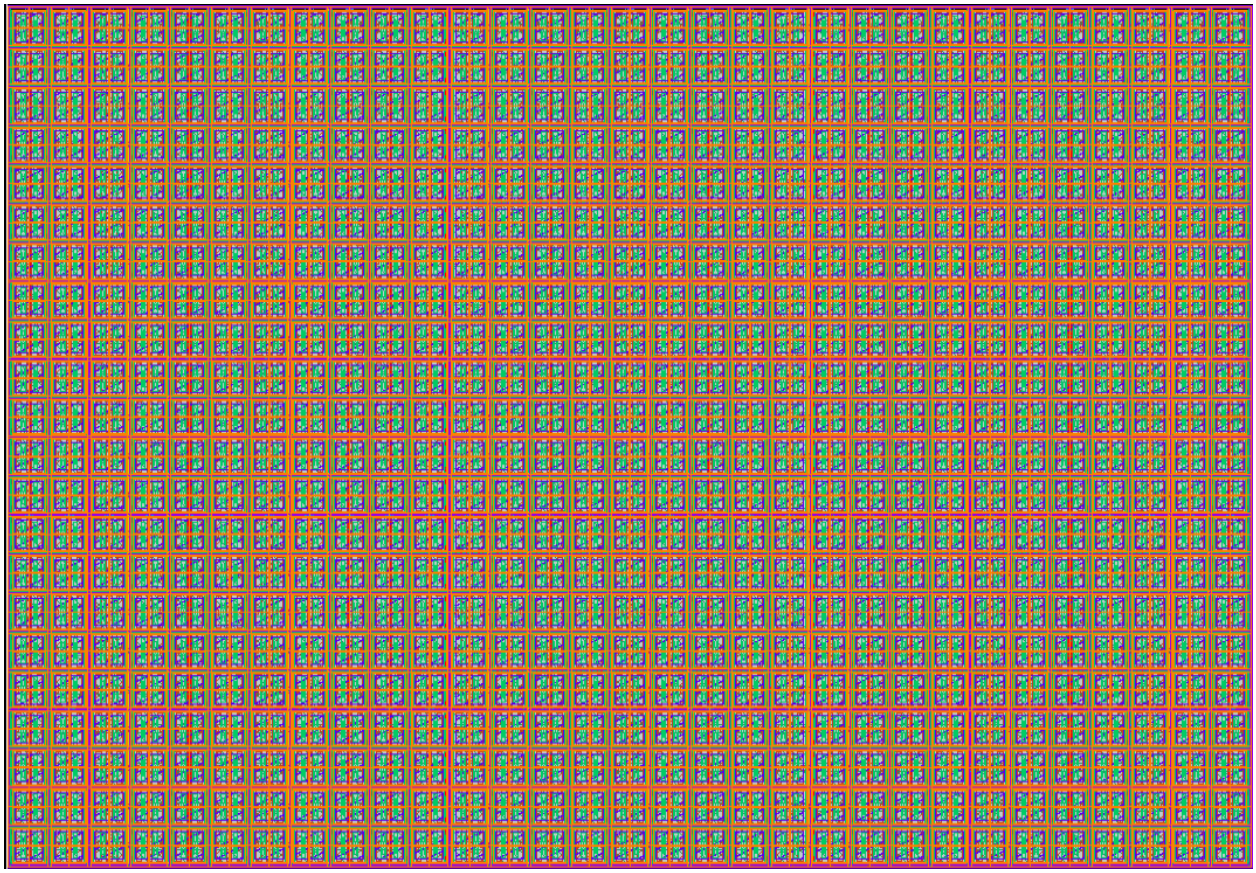

Figure 2.19 Top Level Layout of CDAC

2.11 Break Before Make (BBM) Circuit

A BBM circuit is used when it is necessary to switch a signal path between two different sources. It enables the original signal path to be opened before closing the signal path of the new source. This prevents the signal sources from short circuiting across to each other. In the design of the CDAC it carries out an important function, preventing the positive and negative reference voltages, vrefn and vrefp respectively, from being connected to the bottom plate of the capacitors at the same time. If the positive and negative references happened to short circuit together the current spikes caused would increase the reference settling time. The figure below illustrates the function of the BBM for creating a delay between the switching of the positive and negative references.

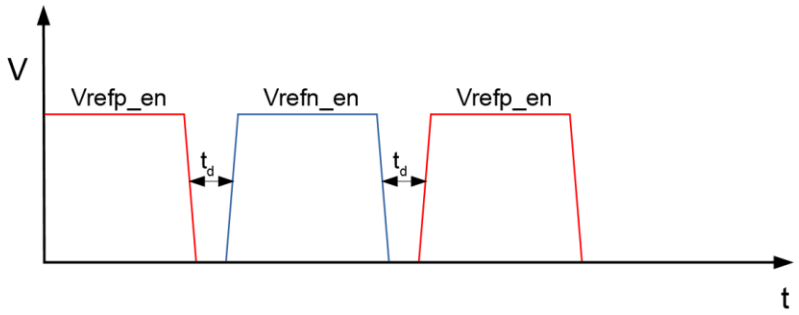

Figure 2.20 BBM Timing Diagram

Figure 2.21 shows the BBM and switches circuit that is used for the MSB capacitors where sampling occurs. Due to the fact that the bottom plate of each capacitor column in the CDAC array is switched separately to the positive and negative references, this requires a separate BBM circuit for each column. No BBM is added to the input signals at the SAR controller ensuring that the DAC reference switches are open when this switch is closed.

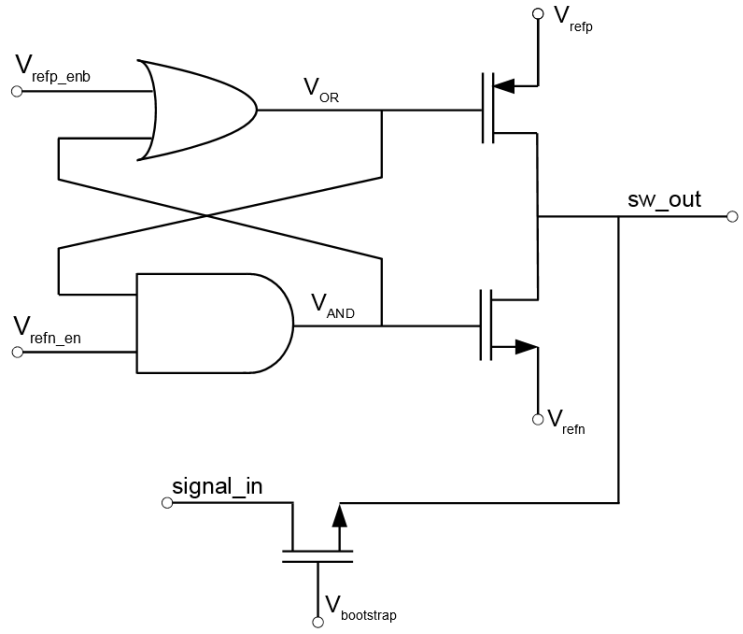

Figure 2.21 BBM circuit for MSB columns

The BBM for the LSB capacitors in Figure 2.22 is similar but doesn't connect the input signal to the output of the switches because sampling doesn't take place on those capacitors.

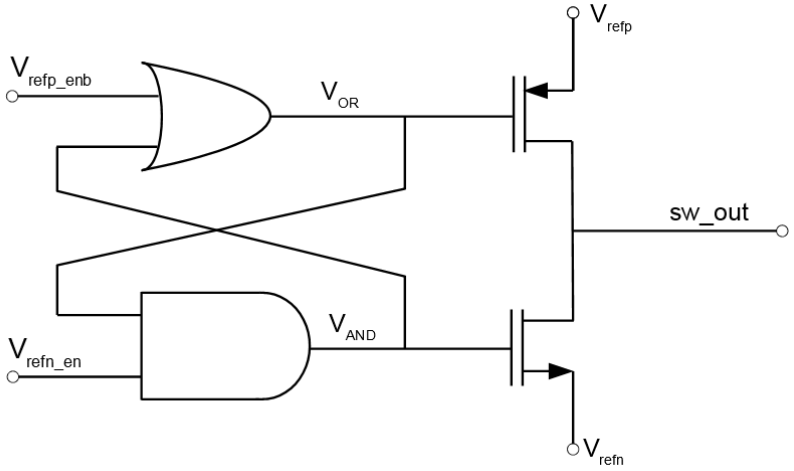

Figure 2.22 BBM circuit for LSB columns

The BBM circuit was implemented using CMOS NAND and NOR gates in series with inverters to create the AND and OR gates shown above [45]. The output switches shown above are PMOS and NMOS switches, with the minimum possible length and width sized to have a maximum time constant of 50ps across all corners. This is because it takes 4 time constants to fully charge an RC load. With a sampling time of 200ps and a capacitance of about 250 fF on each of the biggest columns the ON resistance of each switch is calculated as follows:

$$R = \frac{\tau}{C} = \frac{50 \times 10^{-12}}{250 \times 10^{-15}} = 200\ \Omega \tag{2.8}$$

The layout for the break before make circuit and switches is shown below in Figure 2.23:

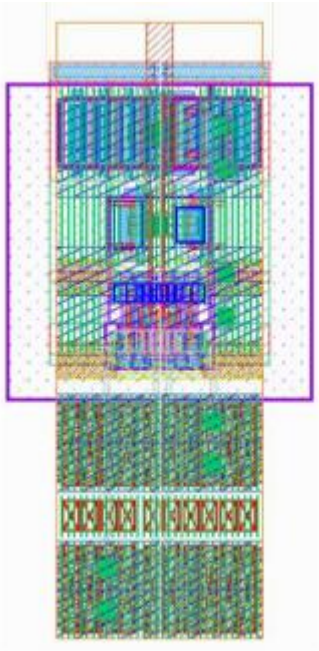

Figure 2.23 Layout of BBM and Switches

2.12 Summary

This chapter discussed the 10-bit split capacitive DAC structure chosen for this design. It also addressed the issue of offset and mismatch and how it would be mitigated in this design. The decision to choose a MOM capacitor design and the unit capacitor sizing and design methodology was described, followed by the overall array with routing and the impact it had on capacitive mismatch. The benefits of redundancy were discussed for this particular design with its sampling time limits. Finally, the final schematic and layout designs were illustrated and the break before make circuits that interface with the DAC.

3 Reference Buffer Design

The role of the reference buffer is crucial in maintaining the accuracy of the SAR ADC. It is designed to provide a stable and repeatable voltage reference for the CDAC during conversion. The reference voltage is required to be 0.9 V $\pm$ 1%, with low noise levels.

3.1 Voltage Reference Loading

The switched capacitors in the DAC provide a dynamic load to the voltage reference, requiring the reference to handle time varying (transient) currents and to settle to a steady state value between each switching instant, during conversion. During sampling, the CDAC is connected to the input of the ADC, and a charge proportional to the voltage input is held on its capacitors. The DAC is disconnected from the input before conversion starts and the conversion algorithm then successively switches each bit to the voltage reference or ground. This switching causes current to be sourced from or sunk by the reference. The charge required, and therefore the current, is proportional to the size of the capacitor being switched in the array [46]. A decoupling capacitor is often placed before the DAC to source and sink the current during the conversion stage and to filter out any noise as well as the ripple of the reference voltage [47].

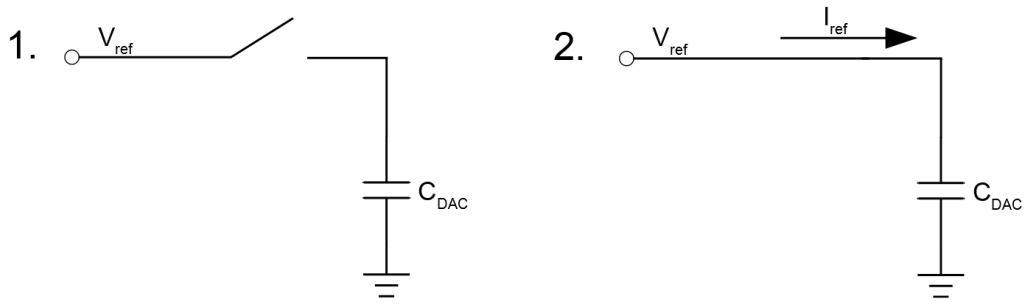

Figure 3.1 DAC Switching Induced Reference Currents

Top plate sampling is used in the SAR ADC in this project. The diagram below illustrates the circuit used to implement this design structure. It is drawn as a single ended circuit for illustration purposes but is mirrored in the real circuit to create a fully differential sampling network with a positive and negative reference voltage.

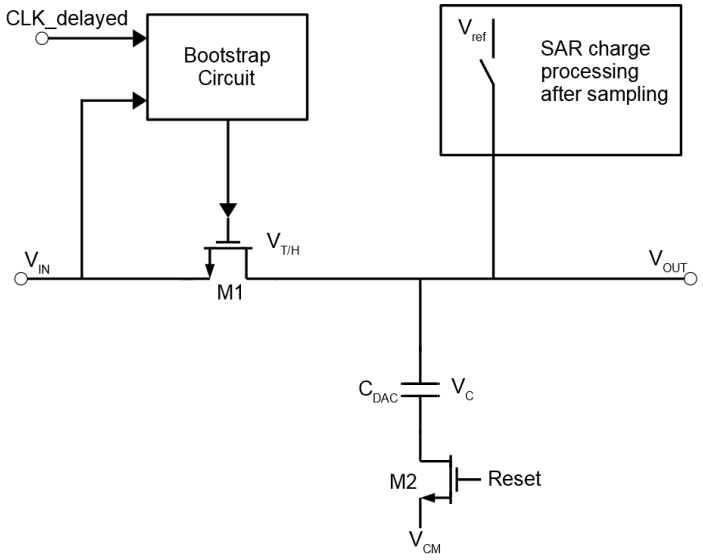

Figure 3.2 SAR Sampling Network

Initially the capacitors are reset, the top-plate is set to V_{cm} and, on the bottom plate, half of the total capacitance set to V_{refp} and the other half set to V_{refn}. Then the DAC switches open and the sampling switch closes. The signal is sampled onto the DAC top plates. Then the top plate switch opens so no more charge can be added to the capacitors as their top plate is floating. Finally, the bottom plates are set back to V_{cm}. Half the total capacitance is once again set to V_{refp} and the other half is set to V_{refn}. The largest current spike from the reference occurs when half the total capacitance is set to V_{refp} and half is set to V_{refn}. Figure3.3 below illustrates the timing of the switches.

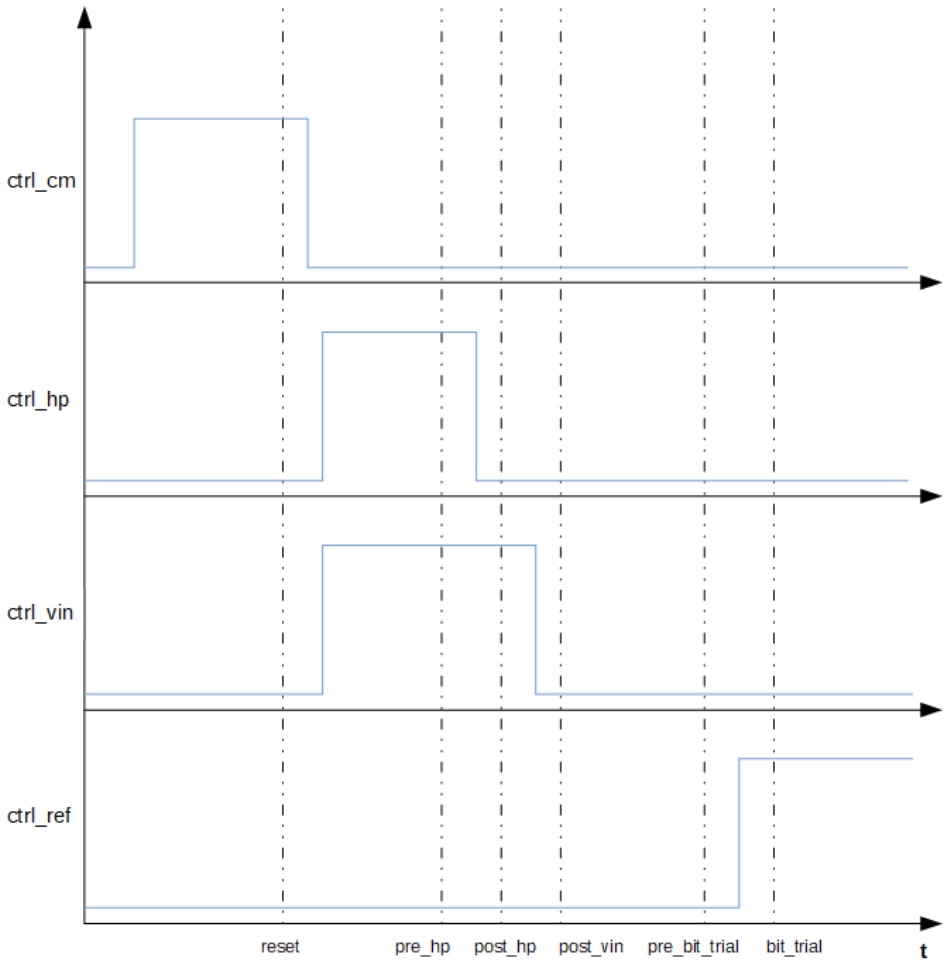

Figure 3.3 Timing diagram for switch circuit

Figure 3.3 shows the timing off switching states in switches for the DAC. The first stage is the reset stage, where all of the switches are inactive other than the top-plate switch (ctrl_cm). The second stage is the sampling stage, where the helper switch (ctrl_hp) and bottom plate v_{in} switch (ctrl_vin) are active. After this, we see the MSB bit trial stage, where only the v_{ref} switch is active (ctrl_ref).

3.2 Reference Ringing Problem

Finite settling limitations of the reference voltage caused by the switching transients of the DAC capacitance could be simply mitigated by having a low impedance from the reference supplies to the input of the DAC with a decoupling capacitor to filter high frequency noise. However another, larger problem is found by using an off-chip (external reference) to drive the DAC. The inherent inductance on the chip package bond wires causes ringing of the reference voltage in response to a current step. Due to the possible oscillations caused by the bond wire inductance, a large external capacitor is not a good solution to this problem [48]. Another option is to use a large on-chip capacitor, at the cost of a lot of area. A flip-chip design was used in this project, which reduced parasitic inductance in the bond wires but not enough to cater for the high levels of accuracy demanded by the project. The board to chip RLC model, which was used for modelling and simulation estimates, is shown in the figure below.

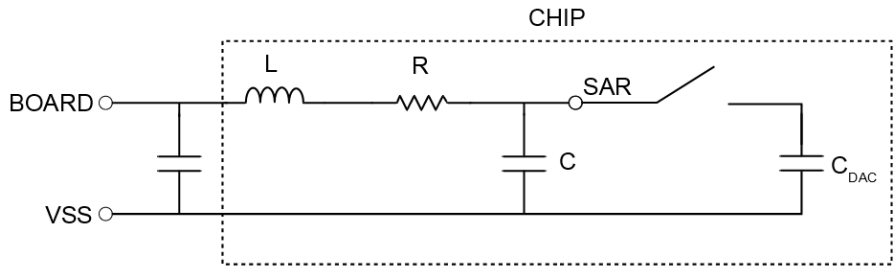

Figure 3.4 Flip Chip Package Model

Using the model in Figure 3.4, the current response over time for the reference was derived in order to characterize the reference response to a voltage step due to switching at the DAC. The voltage response was then found and this derivation allowed the effect of different model parameters on the step response to be determine on MATLAB.

Using Kirchoff's Voltage Law: $$V_{ref,in} - V_L - V_C - V_R = 0 \quad (3.1)$$

Assuming $V_{ref,in}$ is constant in time, $$V_{ref,in} - L\frac{dI}{dt} - IR - \frac{1}{C}\int Idt = 0 \quad (3.2)$$

Differentiate with respect to time: $$-L\frac{d^2I}{dt^2} - R\frac{dI}{dt} - \frac{I}{C} = 0 \quad (3.3)$$

$$\frac{d^2I}{dt^2} + \frac{R}{L}\frac{dI}{dt} + \frac{I}{LC} = 0 \quad (3.4)$$

Assuming a solution in the form, $$\alpha^2 + \frac{R}{L}\alpha + \frac{1}{LC} = 0 \quad (3.5)$$

$I = I_0 e^{\alpha t}$:

Therefore: $$\alpha = -\frac{R}{2L} \pm \frac{1}{2}\sqrt{\frac{R^2}{L^2} - \frac{4}{LC}} \quad (3.6)$$

But time constant, $$\tau = \frac{L}{R} \quad (3.7$$

And natural frequency, $$\omega_0 = \frac{1}{\sqrt{LC}} \quad (3.8)$$

Therefore: $$\alpha = -\frac{1}{2\tau} \pm i\omega \quad (3.9)$$

Where, $$\omega = \sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}} \quad (3.10)$$

The solution of the differential equation is then: $$I(t) = I_0 e^{-\frac{t}{2}\tau} \sin(\omega t) \quad (3.11)$$

But, $$V_{ref}(t) = V_{ref0} + \Delta V_{ref}(t) \quad (3.12)$$

And initial current step is: $$I_0 = \Delta V_{ref}(t)(\frac{1}{\omega C}) \quad (3.13)$$

The transient voltage at the DAC input can be defined as: $$\Delta V_{ref}(t) = I(t)(\frac{1}{\omega C}) \quad (3.14)$$

Therefore: $$V_{ref}(t) = V_{ref0} + I(t)(\frac{1}{\omega C}) \quad (3.15)$$

This equation shows the damped step response of the reference current in the RLC circuit, with initial current I_0, time constant τ and damped frequency ω. It shows an exponential decay with a sinusoidal oscillation to a step in the current, caused by capacitor switching. The reactive components in the circuit determine the damping coefficient, causing it to either be under-damped, critically damped or over-damped. The MATLAB plots below show the different solutions to this model, given an initial reference voltage of 0.9 V at the input to the DAC and a reference voltage step of 450 mV.

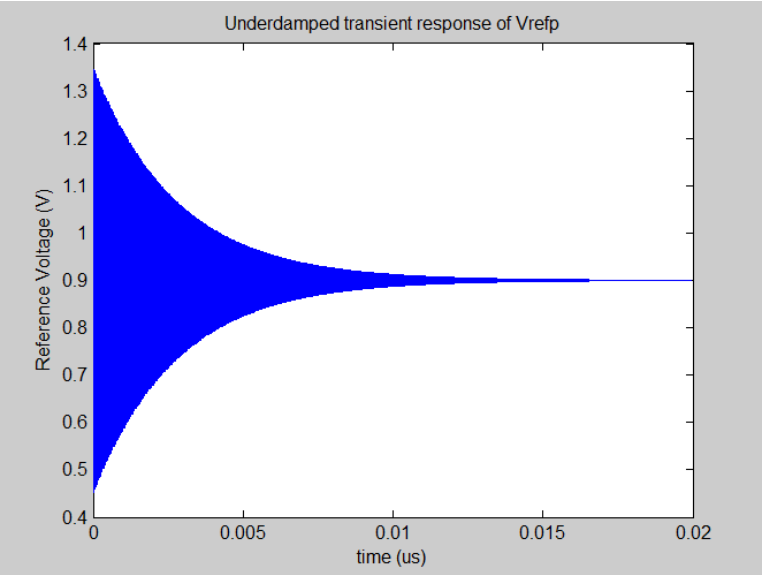

Figure 3.5 RLC Reference Voltage Response with Bond Wire Resistance of 5mΩ

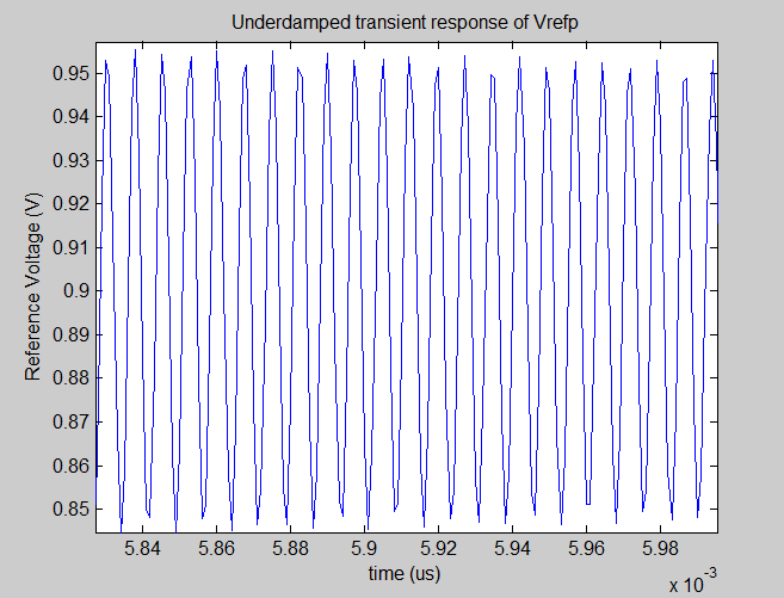

Figure 3.6 Zoomed in graph of Figure 3.4 showing decaying sinusoidal response

The figures above show the expected underdamped response of the reference current to a step on the flip-chip package, with expected parasitic inductance of 70 pH, parasitic resistance of 5 mΩ and internal decoupling capacitance of 2 pF.

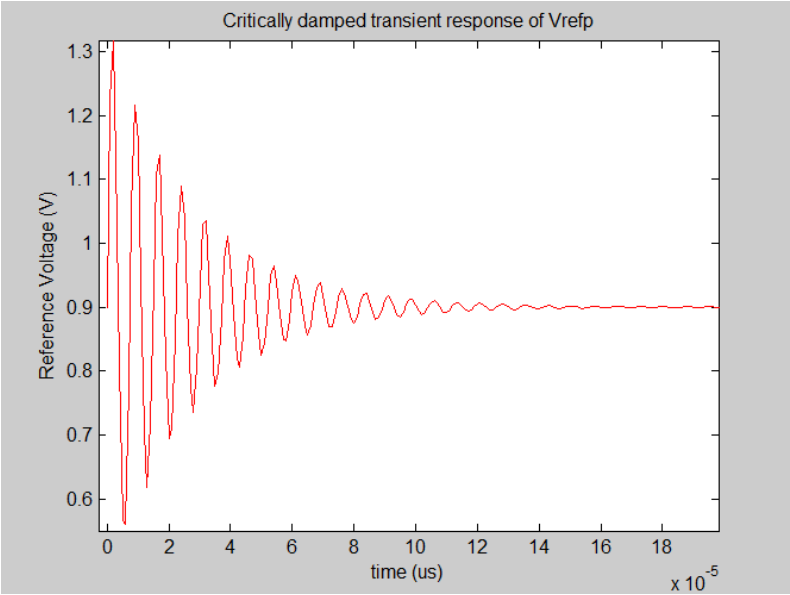

Figure 3.7 RLC Reference Voltage Response with Bond Wire Resistance of 0.5Ω

The plot above shows the expected response of the reference current to a step if the bond wire resistance was increased by 2 orders of magnitude, to 0.5 Ω. It shows a much higher rate of decay. This illustrates the impact of a low Q, lossy bond wire inductance on the degradation of the reference voltage due to switching induced ringing.

3.3 Reference Buffer Solution

Given the impracticality of designing an on-chip capacitance large enough to shunt the low frequency ringing to ground, and the fact that capacitors are not capable of bypassing both low and high frequencies because of the internal resonances in the capacitors themselves [49], it became apparent that a more robust solution was required. These internal resonances occur at high frequency due to the parasitic inductance becoming dominant. Large capacitors have been used as a solution but the charge taken from the

capacitor is dependent on the SAR code [26]. A unity gain voltage buffer was chosen to resolve the reference ringing. In principle, it would receive a reference input voltage, and match that DC voltage level at the output. A high input impedance would block any transient signals arriving at the input and a low output impedance would allow a quick response to a switching transient at the output.

Two popular unity gain buffer topologies are compared below:

Table 3.1 Source Follower vs. Flipped Voltage Follower

Design Metric	**NMOS Source Follower Buffer (Figure 3.8)**	**Flipped Voltage Follower (FVF) Buffer (Figure 3.9)**
Output Impedance	Higher	Lower
Bandwidth	Lower	Higher
Current Sourcing	High	Higher
Current Sinking	Limited	Limited
Voltage Gain	Less than unity	Unity
Complexity	Simple	Complex
Voltage Headroom	$V_{DD}=V_{OUT}+V_{GS}$	$V_{DD}=V_{OUT}+V_{DS}$
Power Consumption	Higher	Lower

The NMOS source follower follows the input with a dc level shift and is able to source a large amount of current from the load. It is limited in its current sinking capabilities, however, by the biasing current mirror because a current mirror has fixed current and cannot adapt to a changing load. The PMOS source follower, however can sink a lot of current but its current sourcing is limited. The PMOS source follower is capable of a higher output voltage, while the NMOS source follower can set a lower output voltage at the same supply voltage. The FVF topology can source a large amount of current but its current sinking capabilities are limited by its biasing current source [50].

Two of the most important metrics in a voltage buffer are the input and output impedance. The input impedance needs to be as high as possible to block any perturbations at the buffer output, disturbing the reference input to the CDAC from feeding through, and a low output impedance is required to respond quickly to a load. Flipped voltage followers have a lower output impedance than regular source followers due to its shunt feedback dynamically reacting to the output load [51]. A basic source follower requires bigger devices to achieve the same output impedance as an FVF buffer because the output impedance is inversely related to the trans-conductance of the MOSFET and the aspect ratio and bias current must be increased more than the equivalent FVF design to achieve the necessary output impedance value [52].

The non-linearity in the basic source-follower is also worse than the corresponding FVF [51]. Power is directly proportional to supply voltage and an NMOS source follower needs a higher supply voltage than a PMOS source follower or an FVF to achieve the same output voltage.

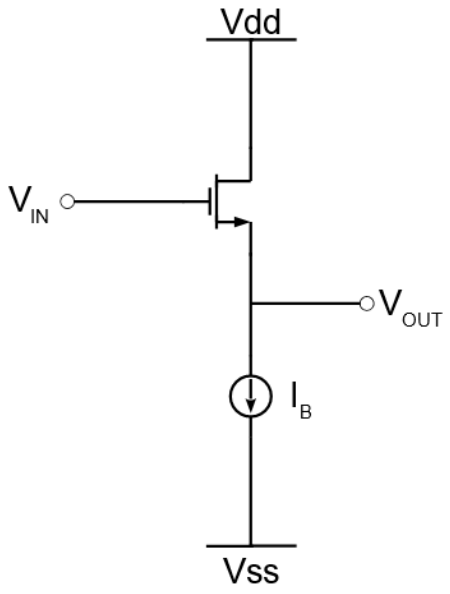

Figure 3.8 NMOS Source Follower Schematic

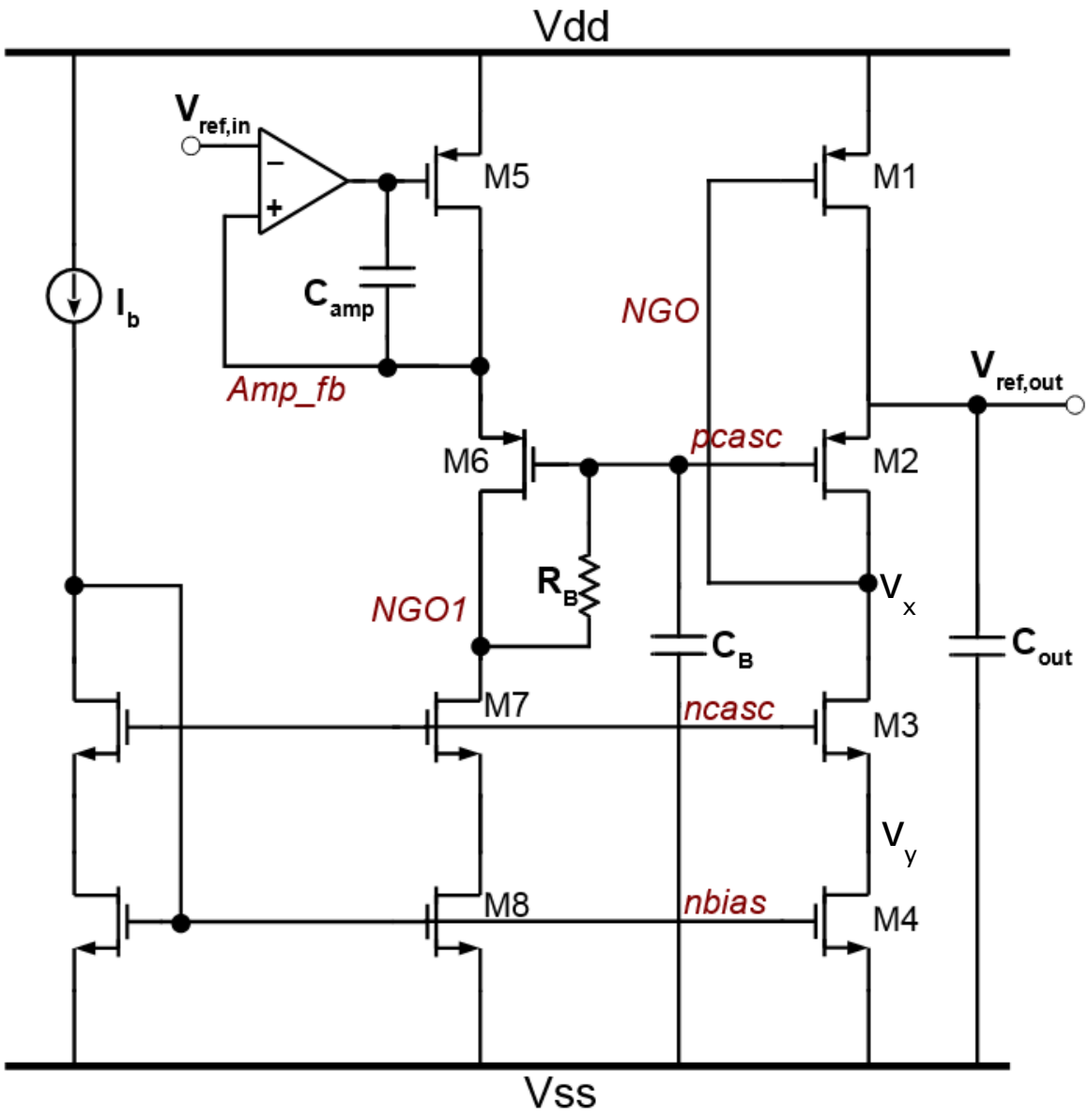

Figure 3.9 Flipped Voltage Follower Schematic

The FVF architecture was chosen because of its very low output impedance, compared to a regular source follower buffer as shown on the next page. The amplifier shown in Figure 3.9 is described in Section 3.5.

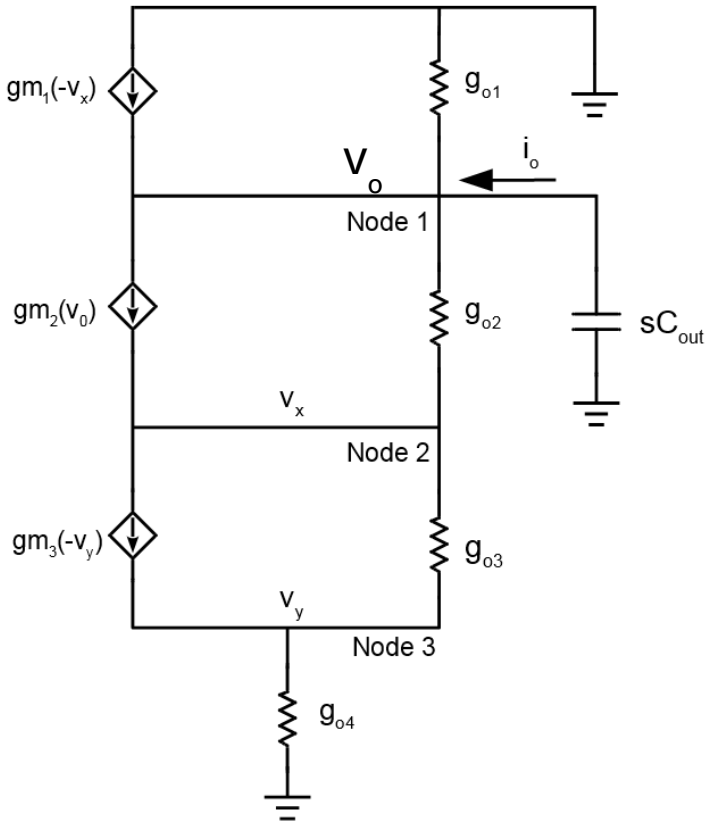

Figure 3.10 FVF Small Signal Equivalent Circuit for Rout

Small Signal Analysis of FVF output Stage to find output impedance:

At node 1: $$i_o = v_o g_{o1} + (v_o - v_x) g_{o2} + g_{m1} v_x + g_{m2} v_o \quad (3.16)$$

At node 2: $$(v_x - v_y) g_{o3} - v_y g_{m3} - v_o g_{m2} + (v_x - v_o) g_{o2} = 0 \quad (3.17)$$

At node 3: $$v_y g_{o4} + v_y g_{m3} + (v_y - v_x) g_{o3} = 0 \quad (3.18)$$

Rearranging for v_y: $$v_y = \frac{v_x g_{03}}{g_{o3} + g_{o4} + g_{m3}} \quad (3.19)$$

But $g_o << g_m$: $$v_y \cong \frac{v_x g_{o3}}{g_{m3}} \quad (3.20)$$

Subbing for v_y in (3.17) and rearranging:

$$v_x \cong \frac{v_o(g_{m2} + g_{o2})}{g_{o2}} \tag{3.21}$$

But $g_o << g_m$: $$v_x \cong \frac{v_o g_{m2}}{g_{o2}} \tag{3.22}$$

Subbing for v_x in (3.16):

$$i_o = v_o g_{o1} + \left(v_o - \frac{v_o(g_{m2})}{g_{o2}}\right) g_{o2} + g_{m1}\left(\frac{v_o(g_{m2})}{g_{o2}}\right) + g_{m2} v_o \tag{3.23}$$

$$i_o = v_o(g_{o1} + g_{m2} + g_{o2} - \frac{g_{o2}(g_{m2})}{g_{o2}} + \frac{g_{m1}(g_{m2})}{g_{o2}} \tag{3.24}$$

Finding r_{out} $$r_{out} = \frac{v_o}{i_o} = \frac{1}{g_{o1} + g_{o2} + g_{m2} - \frac{g_{o2}(g_{m2})}{g_{o2}} + \frac{g_{m1}(g_{m2})}{g_{o2}}} \tag{3.25}$$

$$r_{out} = \frac{g_{o2}}{(g_{o2})(g_{o1} + g_{o2} + g_{m2}) + g_{m2}(g_{m1} - g_{o2})} \tag{3.26}$$

But $g_o << g_m$: $$r_{out} = \frac{g_{o2}}{g_{m2} g_{m1}} \tag{3.27}$$

The derivation above shows how the output impedance of the FVF buffer is inversely proportional to the trans-conductance of the first PMOS multiplied by the intrinsic gain of the second PMOS.

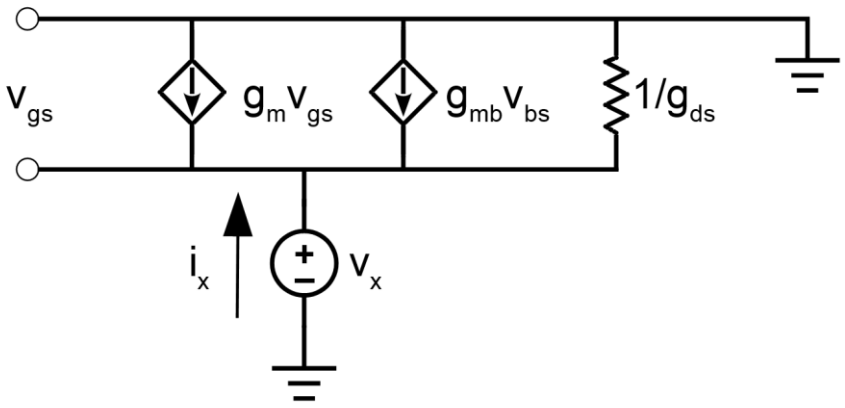

Figure 3.11 Source Follower Small Signal Equivalent Circuit for Rout

The diagram above illustrates the small signal equivalent circuit of a source follower buffer. The output impedance can be derived as shown below.

$$i_x = g_m v_x + g_{mb} v_x + g_{ds} v_x \tag{3.28}$$

Where, $$v_{gs} = -v_x \quad \& \quad v_{bs} = -v_x \tag{3.29}$$

Therefore: $$r_o = \frac{v_x}{i_x} = \frac{1}{g_m + g_{mb} + g_{ds}} \cong \frac{1}{g_m} \tag{3.30}$$

It is clear that a significantly lower output impedance can be achieved using the FVF topology instead of the regular source follower. The next step is to derive the specifications for output impedance of the FVF and the capacitance at the output of the buffer for charge sharing at switching instants.

3.4 Settling Requirements Specifications

The worst case step in reference voltage is when the MSB Capacitor is switched. For a 10 bit single ended DAC it is required to find the exponential error for a step voltage, V_x, to settle to less than half an LSB:

$$\Delta_{wc} e^{-\frac{t_c}{\tau}} < \frac{1}{2} \times \frac{V_{ref}}{2^{10}} \tag{3.31}$$

The MSB capacitor is initially charged to common mode or $V_{refp}/2$ and is switched to V_{refp}. The charge required to set the MSB capacitor to is V_{refp}:

$$Q_{wc} = \frac{C_{MSB} V_{ref}}{2} \tag{3.32}$$

Q=CV, The MSB charge is drawn from the reference capacitor C_{ref}:

$$\Delta_{wc} = \frac{C_{MSB} V_{ref}}{2C_{ref}} \tag{3.33}$$

Therefore:

$$\begin{aligned} \frac{C_{MSB} V_{ref}}{2C_{ref}} e^{-\frac{t_c}{\tau}} &< \frac{1}{2} \times \frac{V_{ref}}{2^{10}} e^{-\frac{t_c}{\tau}} \\ &< \frac{C_{ref}}{C_{MSB}} \times 2^{-10} \end{aligned} \tag{3.34}$$

Rearranging in terms of settling time:

$$t_c > -\ln\left(\frac{C_{ref}}{C_{MSB}} \times 2^{-10}\right)\tau \tag{3.35}$$

But: $$\tau = R_{out}(C_{ref} + C_{dac}) \quad (3.36)$$

Therefore: $$t_c = -\ln(\frac{C_{ref}}{C_{MSB}} \times 2^{-10})(R_{out})(C_{ref} + C_{dac}) \quad (3.37)$$

R_{out} requirements for this worst case settling time are therefore:

$$R_{out} = \frac{t_c}{-\ln(\frac{C_{ref}}{C_{MSB}} \times 2^{-10})(C_{ref} + C_{dac})} \quad (3.38)$$

This equation determines the R_{out} specification for the buffer for a given settling time t_c, with a DAC capacitance C_{dac} and a reference capacitance at the output of the buffer, C_{ref}. Plotting this on MATLAB for different C_{ref}/C_{dac} ratios yields:

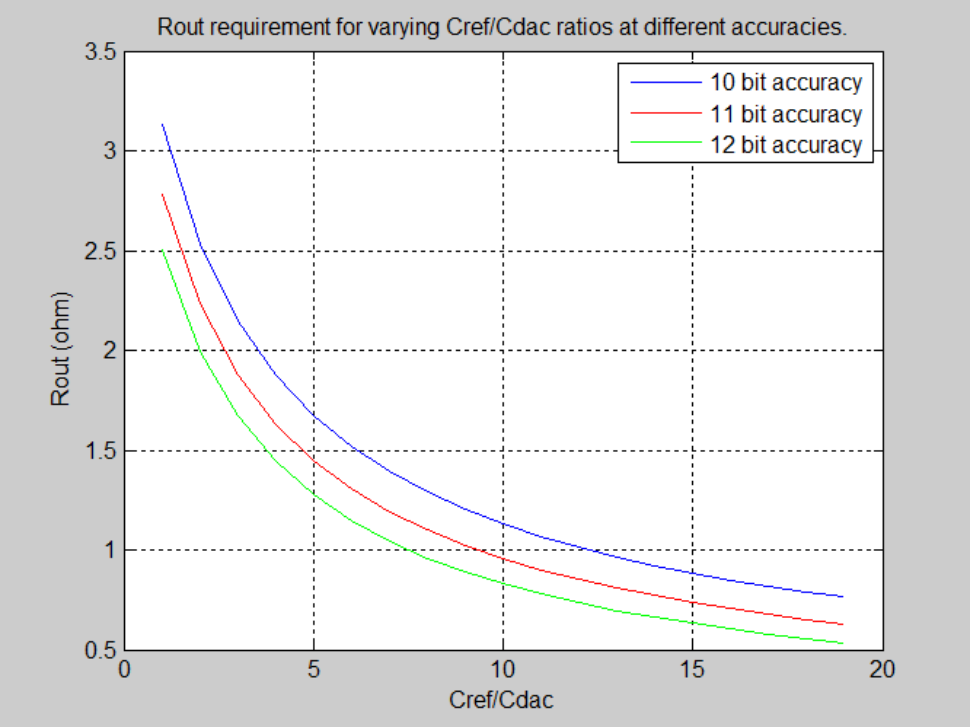

Figure 3.12 Rout Buffer Specifications for Different Capacitance Ratios

3.5 Buffer Amplifier Design

The amplifier plays a critical role in keeping a constant voltage at the input of the CDAC. The reference input is applied to v_{ip} as shown in the schematic below and the output is applied to the gate of a PMOS in the first stage of the FVF, with the drain of the amplifier fed back into v_{in}. A capacitor C_c is placed between the v_{out} and v_{in} nodes and sized to provide adequate phase margin in the feedback loop to prevent instability. The gain, A, of the amplifier defines how well v_{in} will match v_{ip} as shown in the following equation.

$$v_{ip} = \frac{Av_{in}}{1 + A} \tag{3.39}$$

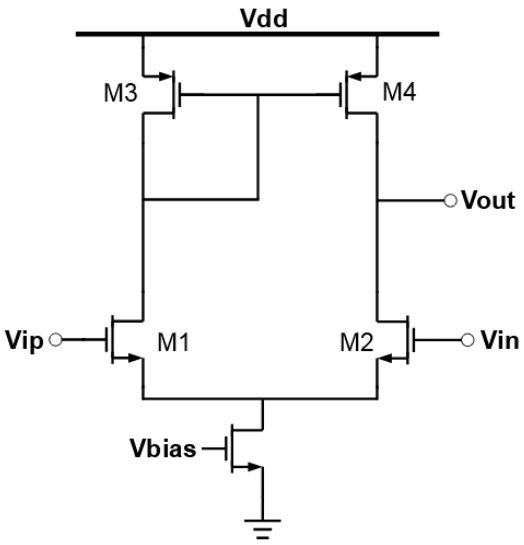

Figure 3.13 Amplifier Circuit Schematic

The gain of the amplifier is found by breaking the amplifier into its left and right hand side components and solving the small signal equivalent circuits as below. Analysis is for differential inputs with common source node of M1 and M2 assumed to be virtual ground.

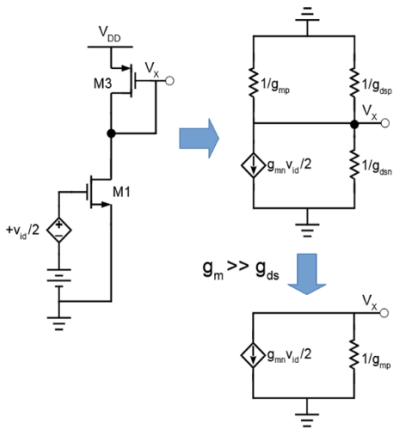

Figure 3.14 LHS Amplifier Gain Derivation

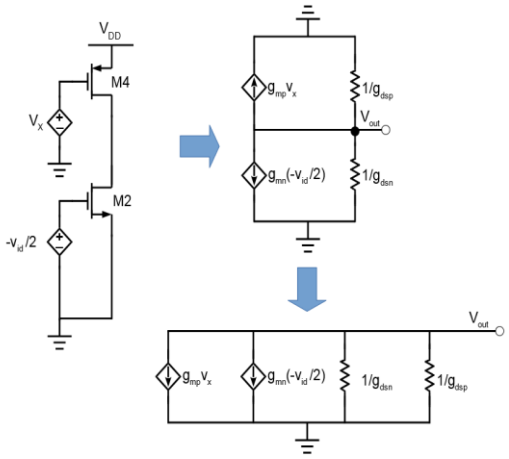

Figure 3.15 RHS Amplifier Gain Derivation

Taking the left and right hand side simplified small signal circuits, the gain can now be calculated. Assume that the g_{mp} and g_{dsp} of both PMOS devices are equal and the g_{mn} and g_{dsn} of both NMOS devices are equal. These devices are matched, with equal current flowing in both legs, i.e. half the bias current flowing in the bottom NMOS device.

LHS:
$$v_x = -\frac{g_{mn}\frac{v_{id}}{2}}{g_{mp}} \tag{3.40}$$

RHS:
$$v_{out} = -\frac{g_{mp}v_x - g_{mn}\frac{v_{id}}{2}}{g_{dsn} + g_{dsp}} \tag{3.41}$$

Substitute for V_x:
$$v_{out} = -\frac{g_{mp}(\frac{-g_{mn}}{g_{mp}}\frac{v_{id}}{2}) - g_{mn}\frac{v_{id}}{2}}{g_{dsn} + g_{dsp}} \tag{3.42}$$

$$v_{out} = \frac{g_{mn}v_{id}}{g_{dsn} + g_{dsp}} \tag{3.43}$$

Therefore,
$$A = \frac{v_{out}}{v_{id}} = \frac{g_{mn}}{g_{dsn} + g_{dsp}} \tag{3.44}$$

3.6 Buffer DC Bias Design

The basic current mirror biasing circuit was designed first but it was decided that supply, process & temperature variations would create a varying bias current for the FVF circuit. It was therefore decided to use a self-biasing circuit designed to have a current output of 50µA, independent of changes in supply voltage as shown in the equations below.

$$(\frac{W}{L})_4 = (\frac{W}{L})_3 \qquad (\frac{W}{L})_2 = k(\frac{W}{L})_1$$

Assume $I_3 = I_4$ & $V_{Th1}=V_{Th2}$

$$\sqrt{\frac{2I_{ref}}{\mu_n C_{ox}(\frac{W}{L})_N}} = \sqrt{\frac{2I_{out}}{\mu_n C_{ox}(\frac{W}{L})_N}} \text{ [53]} \tag{3.45}$$

$$I_{ref} = I_{out} \tag{3.46}$$

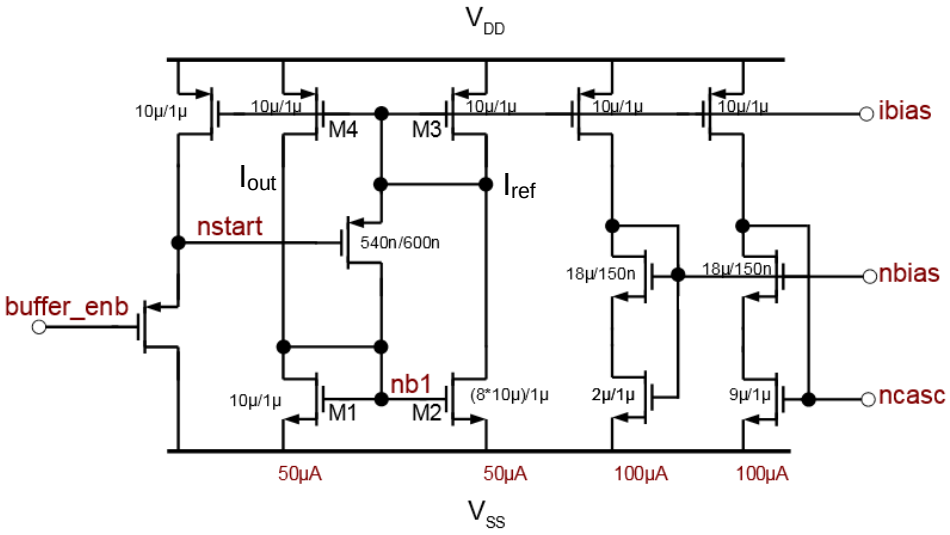

Figure 3.16 FVF Current Biasing Circuit

A start-up function is also included in the biasing design to cause bias current to flow when required. The 50µA bias current is mirrored along the PMOS devices until they are

scaled up to a 100µA current which biases the amplifier circuit and the NMOS current mirrors that provide the bias current to set the nbias and ncasc voltage nodes. An NMOS in triode region is included in the previous stage to set the nbias voltage at an increased DC value. This works by having a gate voltage set by the NMOS current mirror and a constant current set by the PMOS current mirror. This drops a voltage over the channel resistance, proportional to L/W of the channel. The drain voltage is maintained below the gate voltage by the NMOS previous current source, keeping it in triode region.

The following schematic shows how two NMOS and PMOS current mirrors are used to provide a constant, supply insensitive voltage difference between pcasc and NGO1. It achieves this by supplying equal and opposite currents to the pcasc and NGO nodes, with a nominal 100 µA current differential creating an IR drop across the resistor. This ensures that there is a similar voltage difference between pcasc and NGO1 and ultimately sets the buffer output to the reference voltage supplied to the first stage by the amplifier, with both bias currents being proportional to each other in each stage, with a 10X scaling. This proportionality factor is important in preventing offsets from manifesting in the circuit.

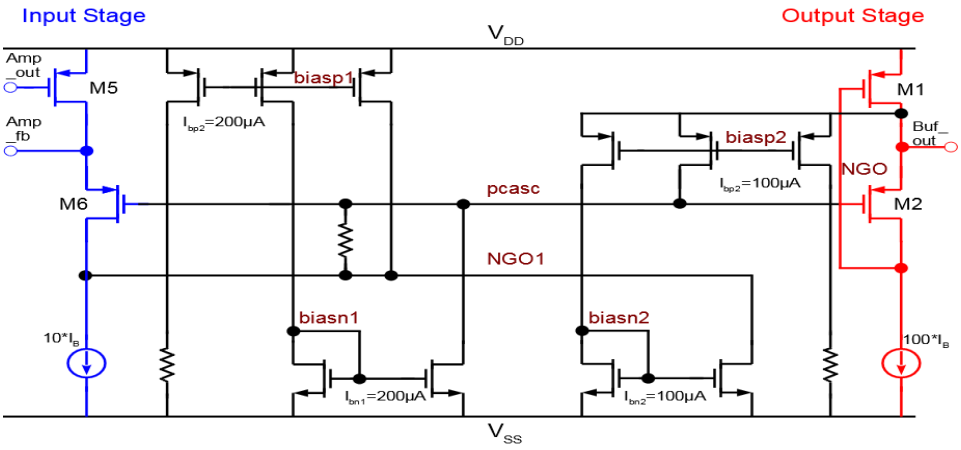

Figure 3.17 NGO1 and pcasc Voltage Drop Biasing Circuit

3.7 Loop-gain Stability Analysis

Loop gain analysis is very important in a closed loop feedback system. Under certain conditions of gain and phase of the feedback signal instability can occur because of the transfer function of the feedback loop going to infinity and creating an oscillator. This would pose serious problems for an amplifier loop or for the FVF output loop and it is necessary to ensure these situations don't arise in the design. The amplifier loop and its closed loop transfer function is derived below, showing the conditions necessary for stability in the feedback loop.

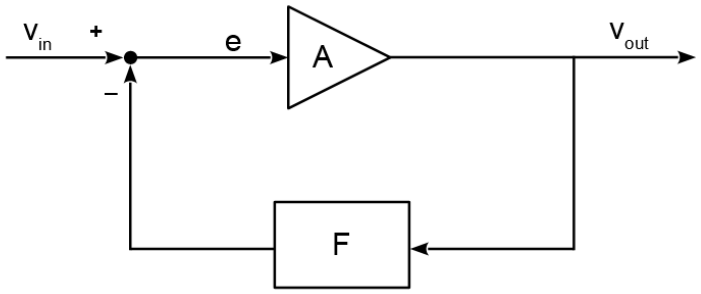

Figure 3.18 Amplifier Closed Loop Gain

- V_{in} is the input signal; V_{out} is the output signal; e is the error signal.
- A is the forward or open loop system.
- F is the feedback system.

From the figure above:

$$v_{out} = Ae, \qquad e = v_{in} - Fv_{out} \tag{3.47}$$

But,

$$v_{out} = Gv_{in} \tag{3.48}$$

Subbing Equation 3.48 into both equations in 3.47 and putting in terms of e:

$$e = \frac{G}{A} v_{in}, \qquad e = v_{in} - FGv_{in} \tag{3.49}$$

Equating both equations in 3.49 and putting in terms of G(s) gives:

$$G(s) = \frac{A(s)}{1 + A(s)F(s)} \tag{3.50}$$

For the loop to be stable, the denominator of the gain expression must not approach zero because that would cause to transfer function to tend to infinity. These terms are frequency dependent. The two criteria that cause this to happen are (they must occur at the same frequency):

$$|AF| \neq 1 \ \& \ \angle AF \ \neq -180° \tag{3.51}$$

The two safety margins for avoiding instability are the gain and phase margins. To find the gain margin of a loop, find the frequency where the phase is -180 degrees and measure the gain at the same frequency. Conversely, to find the phase margin of a loop, find the frequency where the gain is 0 dB and measure the phase at this frequency. Adding 180 degrees to this value gives the phase margin of the loop [54].

Loop gain analysis measures both the gain and phase and is carried out on both the amplifier feedback loop and the NGO output feedback loop of the buffer. Any instability in either of these loops will cause oscillations in the output of the buffer, making it impossible to have a stable, accurate reference voltage.

The MATLAB plot below illustrates how to find the phase margin from loop gain and phase, with a phase margin greater than 60° ensuring loop stability.

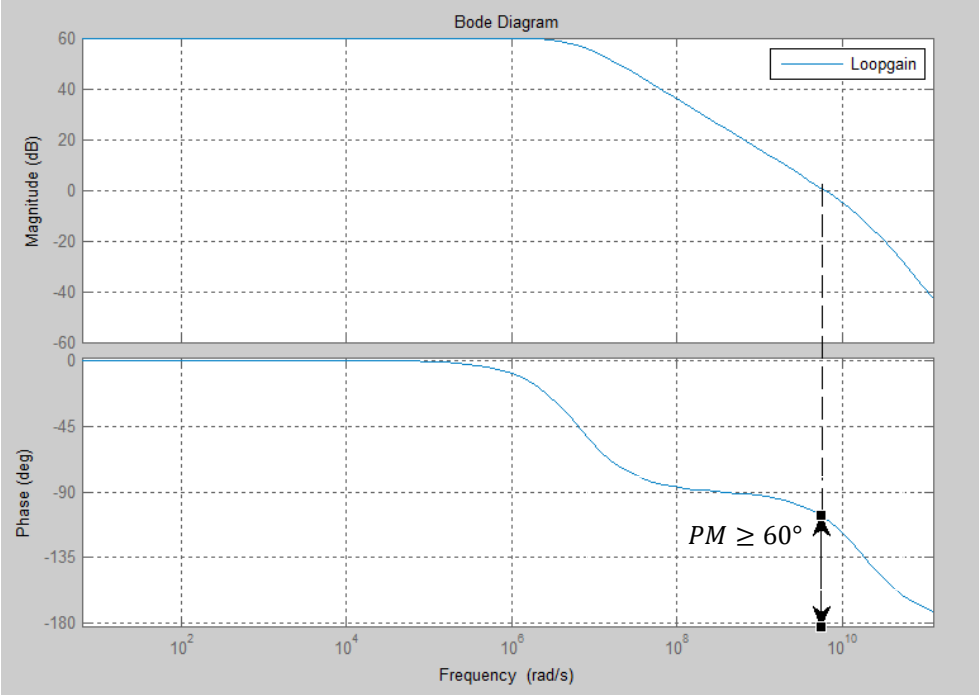

Figure 3.19 Amplifier Loop-gain plots for finding stability margins

3.8 Buffer Output Stage

The buffer output stage is subject to a multitude of factors that can create an unacceptable output reference voltage. As mentioned previously, the settling time is proportional to the output impedance of the output stage and if this is too low incomplete settling will occur. If the bias currents are not properly mirrored or there are DC voltages at important nodes not at the correct level a DC offset can manifest itself at the buffer output. Instability in the amplifier loop or the NGO feedback loop can cause oscillations in the output voltage, giving a time varying reference voltage. The phase and gain margins of both loop must

be known to ensure this does not occur. The following section discusses the test modes created to debug any problems with the output reference voltage.

3.9 Buffer Test & Simulation Modes

There are output pins included on the reference buffer block for testing and debug purposes. These can be utilized on a test bench if a problem is observed with the buffer.

- Bias Current test mode – There is a pin that allows a test current to be taken off chip from the reference buffer. This utilizes test gates, which could switch between a PMOS current mirror and the current drawn by the NMOS ncasc and nbias current mirrors.

- Loop-gain Analysis – The amplifier and NGO loops are both broken with two pins provided for each loop in order to perform loop gain analysis on each loop. This provides the option to assess the stability of both loops on simulations, while having the loops closed for normal operations.

3.10 Buffer Switching Logic

A buffer switching logic circuit was designed to switch the reference for the DAC between the buffer output and a bypass reference with minimum delay and IR drop. This enables the buffer to be bypassed for smaller bit sampling when it's not required. The switches are PMOS devices designed with minimum length and an effective width of 16 µm to achieve a negligible IR drop between source and drain. The logic circuit controls the gate of the switches based on the inputs ref_buf_en, ref_buf_bypass and ctrl_ref_sel. This is illustrated in the truth table, showing the control signals and resultant outputs. This logic

circuit was then implemented using De Morgan's theorem [55] to find the simplest configuration of NAND gates and inverters as shown in the schematic drawing below. Parallel devices are used to increase he width and, thus the output current and speed of the circuit. The inverters are cascaded in increasing width to decrease the input capacitance, while increasing their drive strength. These measures are to ensure the speed of the switching circuit is adequate for bypassing the buffer when it's not required.

Table 3.2 Truth Table for Switching Logic Circuit

Input			Output	
ref_buf_en	ref_buf_bypass	ctrl_ref_sel	Buffer	Bypass
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	0

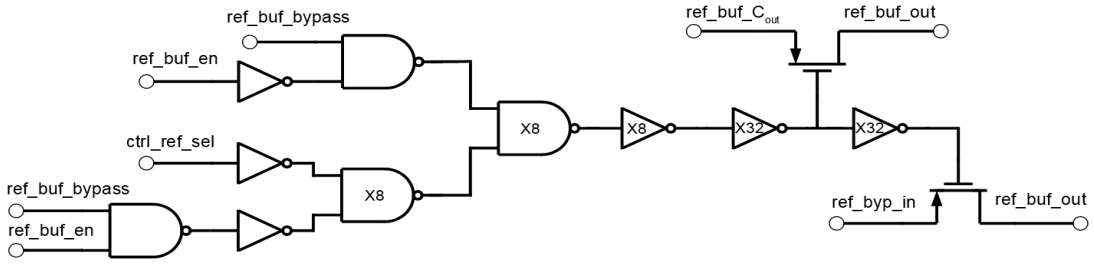

Figure 3.20 Buffer Switching Logic Circuit

3.11 Reference Buffer Schematic

The figure below shoes the final version of the reference buffer schematic for this project.

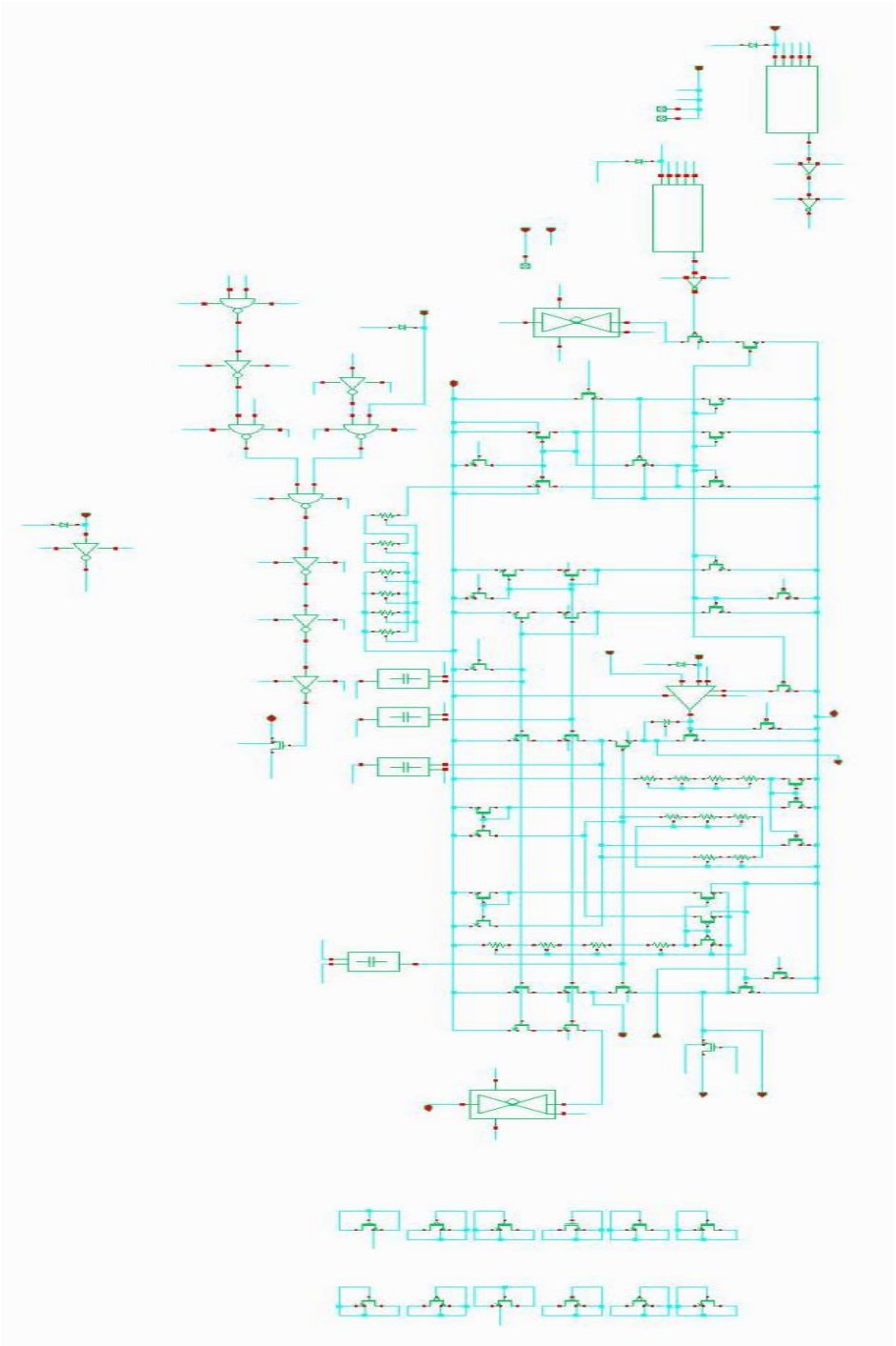

Figure 3.21 Reference Buffer Schematic

3.12 Reference Buffer Layout

The figure below shows the final layout for the reference buffer design in this project. An important consideration for the layout was mitigating the IR drop in the supply and ground routing, caused by the large currents in the buffer.

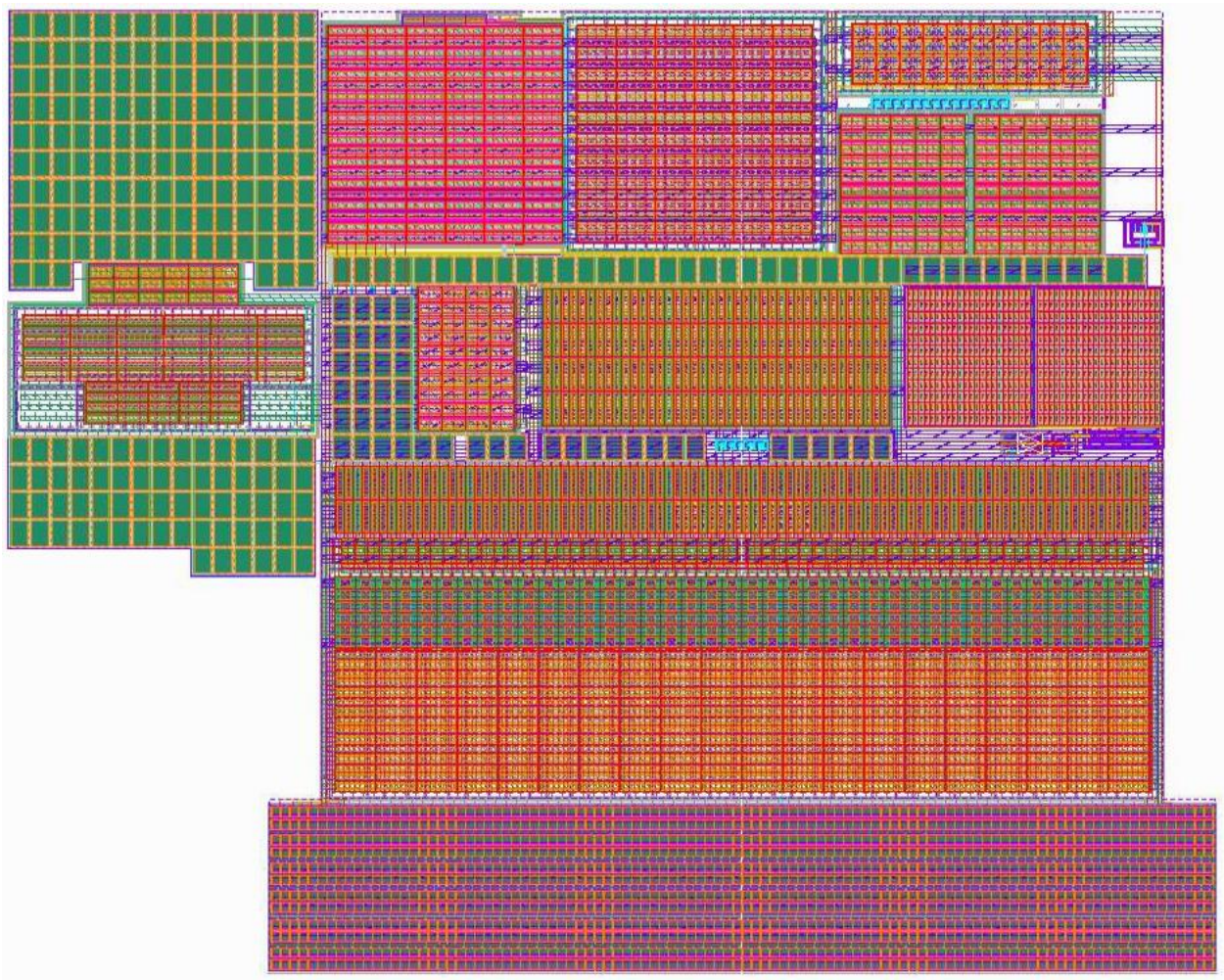

Figure 3.22 Reference Buffer Layout

3.13 Summary

This chapter discussed the reasons for choosing a reference buffer as a part of the design and the steps required to design a robust enough buffer to match the accuracy specifications and provide adequate stability needed by this design. An FVF and regular source follower were compared and it was shown why an FVF would be superior for the requirements of this project. The design of the amplifier was described and its importance for keeping a constant stable voltage at the input of the CDAC. The buffer DC current bias design was shown as well as the loop gain analysis to test the stability of the design. The buffer test modes and buffer logic circuits were shown. Finally, the schematic and layout designs of the buffer were illustrated.

The next chapter discusses the results of the project.

4 Results

4.1 Capacitive DAC Results

4.1.1 Introduction

This section presents simulation results for the capacitive DAC. Firstly, the capacitive matching of the CDAC is covered in section 4.1.2, with the corresponding DNL and INL results presented. Finally, a Monte Carlo analysis is presented to show the random mismatch that the individual capacitors may be exposed to and its effect on DNL and INL.

4.1.2 Capacitive Matching

Table 4.1 shows the matching performance of the Capacitive array from full parasitic extractions of the array, with the capacitor values corresponding to the capacitors labelled in Figure 4.1.

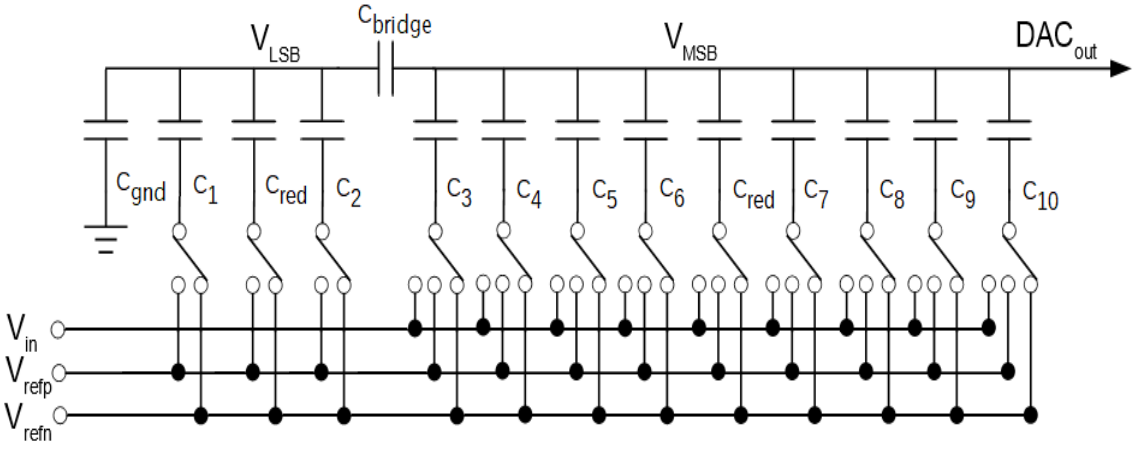

Figure 4.1 Schematic of Capacitive Array

Table 4.1 Capacitive Matching

Capacitor	Nominal (fF)	Additional (fF)	Total (fF)	Multiple of Average C_{unit}	Offset from target value (%)
MSB side of Capacitive Array					
C10	1873.782	152.243	2026.025	128.251	0.197
C9	936.891	77.206	1014.097	64.194	0.304
C8	468.445	37.811	506.256	32.047	0.147
C7	234.223	18.529	252.752	15.999	-0.002
Cred	234.223	18.563	252.785	16.002	0.011
C6	117.111	9.828	126.939	8.036	0.444
C5	58.556	4.854	63.410	4.014	0.350
C4	29.278	2.373	31.650	2.004	0.177
C3	14.639	1.214	15.853	1.004	0.354
LSB side of Capacitive Array					
C2	29.278	2.196	31.474	1.992	-0.380
Cred	29.278	2.199	31.478	1.993	-0.370
C1	14.639	1.212	15.851	1.003	0.337
Cgnd	14.639	1.045	15.684	0.993	-0.717
Bridge Capacitor					
Cbridge	29.278	0.929	30.207	1.912	-4.392

The careful layout considerations outlined in Chapter 2 ensured that the individual capacitors matched as well as possible. However, the matching was still limited due to

asymmetries in the layout such as routing, bridge capacitor placement, layout structure, and even how many active capacitors or dummy capacitors that each column was exposed to. As discussed in Chapter 2, a common centroid layout structure exhibited much worse matching than what is shown above. This degradation in matching outweighed the potential improvements from cancelling out process gradients.

4.1.3 DNL

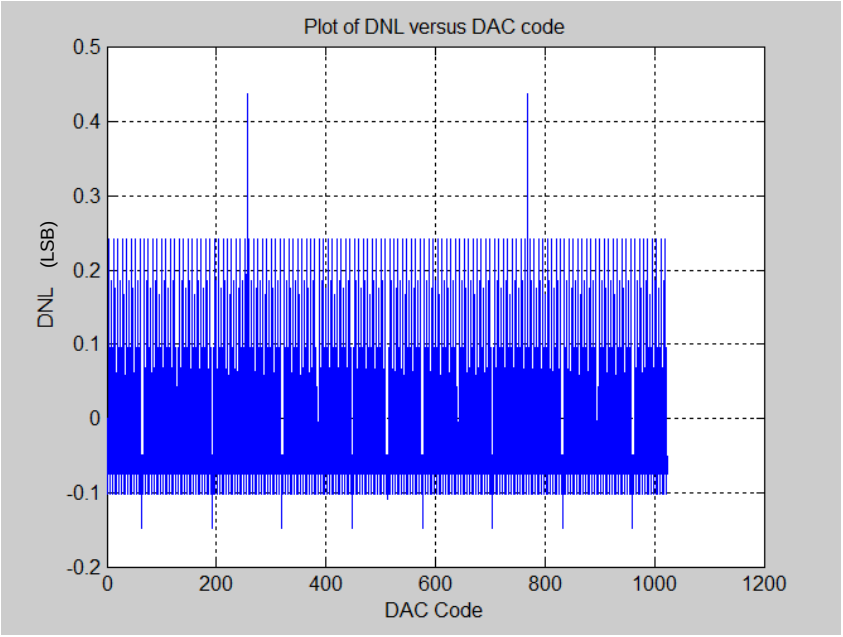

Figure 4.2 Capacitive DAC DNL

The DNL plot shows a maximum DNL of 0.44 LSB at code 256 and 768 because of the redundant 16C capacitor between C6 and C7. The actual DNL has a maximum of 0.24 LSB for an input ramp from 0V to 0.9V.

4.1.4 INL

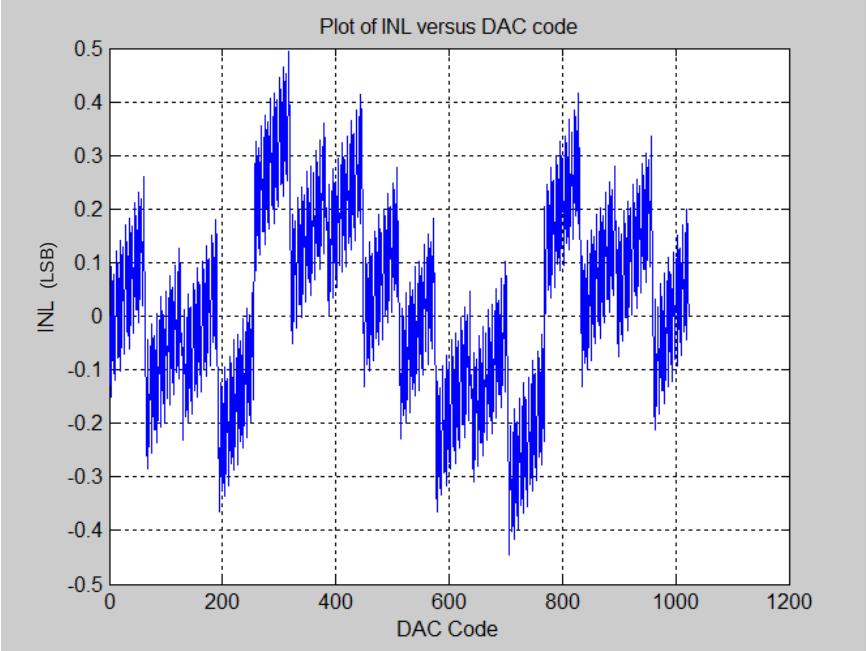

Figure 4.3 Capacitive DAC INL

The plot of the INL for the DAC ramp above shows a maximum INL of 0.5. However, this is increased due to the large DNL error caused by the redundant capacitor at code 256 and code 768.

4.1.5 Monte Carlo Analysis

A ramp test was applied to the DAC schematic containing the TSMC MOM capacitors but this time it was ran 100 times over global process corners and local device mismatch. The maximum DNL and INL error from each ramp was found and then plotted in two histograms to find the mean and standard deviation for each maximum INL and DNL. The 16C redundant capacitor column caused increased INL and DNL errors but the standard deviation showed how much variance can be expected due to capacitor mismatch.

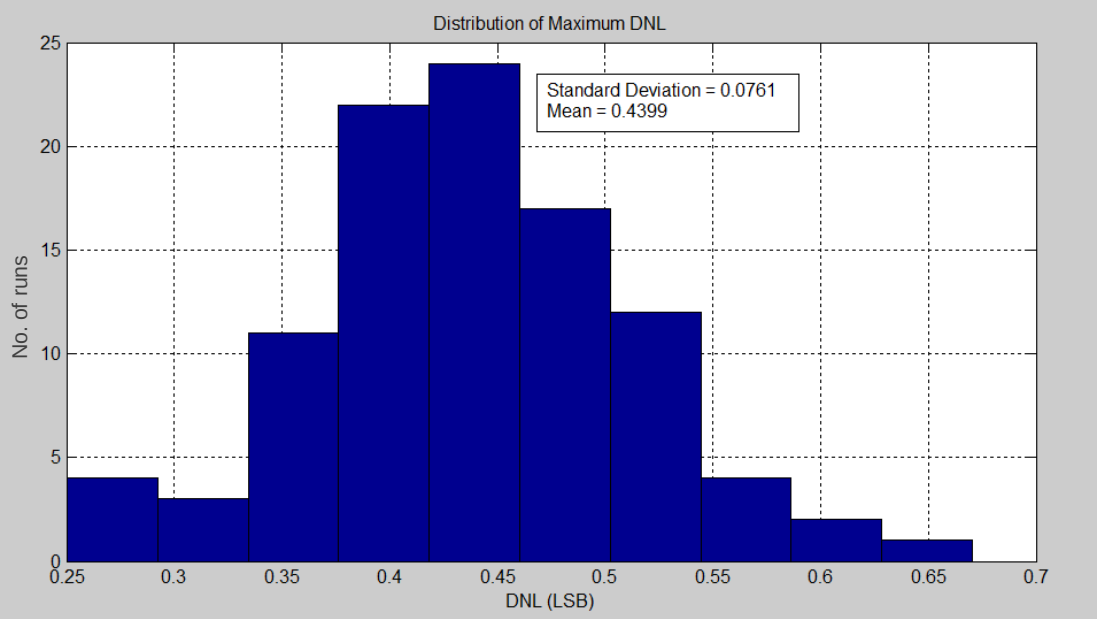

Figure 4.4 Monte Carlo Distribution of Max. DNL for 100 ramp tests

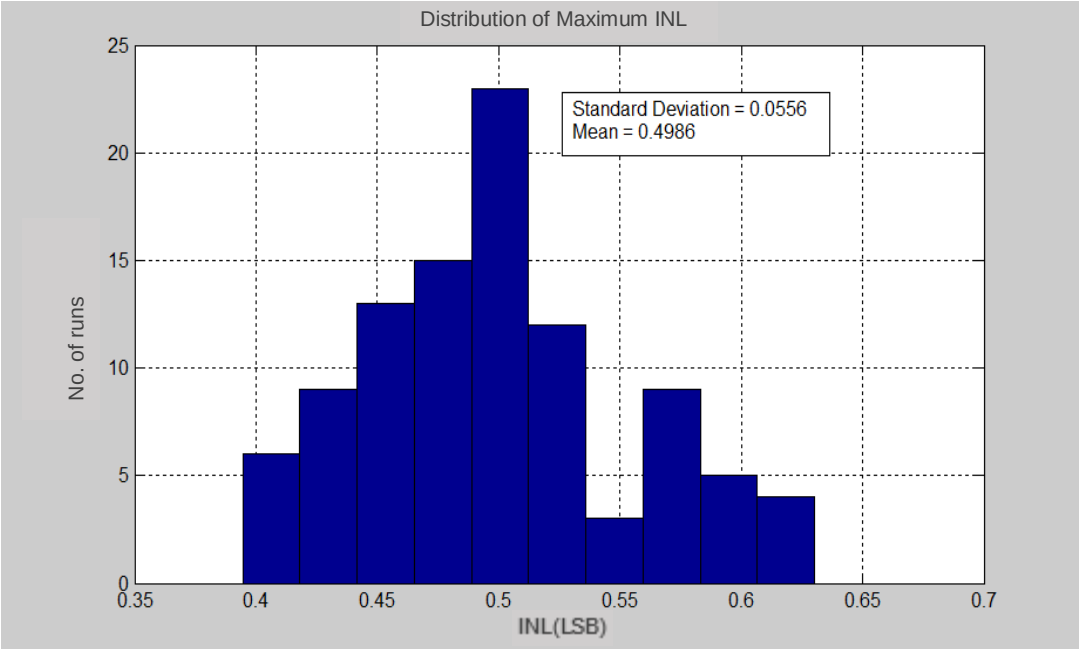

Figure 4.5 Monte Carlo Distribution of Max. INL for 100 ramp tests

4.2 Reference Buffer Results

4.2.1 Introduction

This section presents simulation results for the reference buffer design. These results include DC Monte Carlo analysis, DAC step settling, Loop Gain analysis, AC analysis, PSRR, Power consumption, Supply current transients, Transient Noise and Output Integrated Noise. They then cover enable/disable and power up/power down simulations. This section concludes with a summary table of the primary simulation results.

4.2.2 Buffer Specifications

Table 4.2 Reference Buffer Specifications

Parameter	Min	Typ	Max	Units
Resolution		16		Bits
Conversion Rate		1.5		GSPS
Settling Time		0.2		ns
Analog				
Input Signal Amplitude	0.895	0.9	0.905	V
Output Voltage	0.89	0.9	0.91	V
Load Capacitance		4		pF
Noise				
Output Integrated Noise		8		$nV^2/\sqrt{Hz}$
Dynamic Performance				
Maximum Load Step			0.45	V
Settling Accuracy (LSBs)		12		Bits
Start-up Time		20		µs
Power Supply				
Operating Voltage	1.1	1.2	1.3	V
Power Consumption		10		mW
Process 28nm HPC	ss	tt	ff	
Operating Temperature (Junction)	0	27	85	°C

4.2.3 DC Analysis

The DC output voltages of the Amplifier and Reference Buffer were measured and a Global Monte Carlo Analysis (across process) was carried out on the schematic to show the DC levels and the variance across corners and device mismatch.

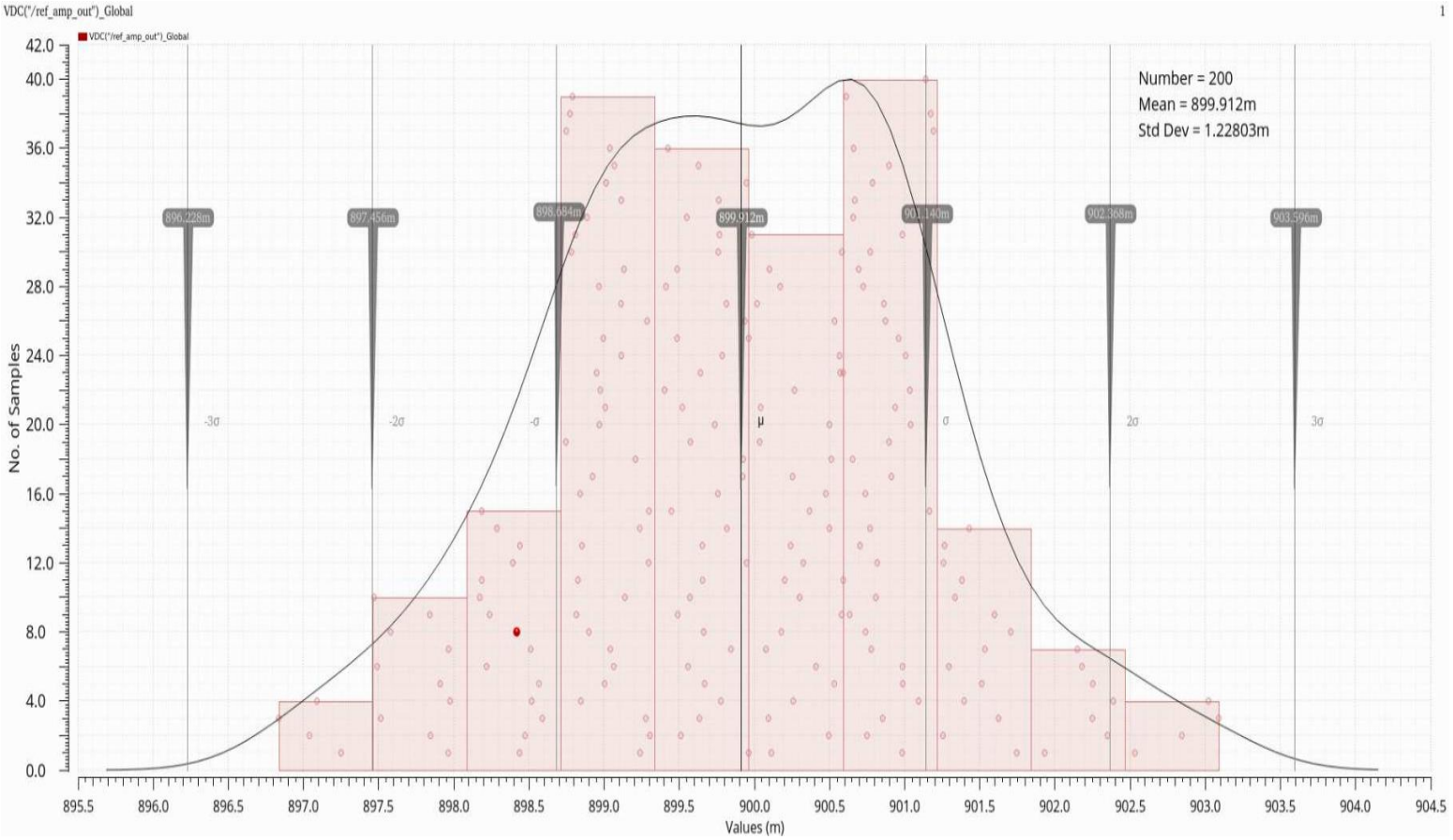

Figure 4.6 Monte Carlo DC Analysis of Amplifier Output Voltage

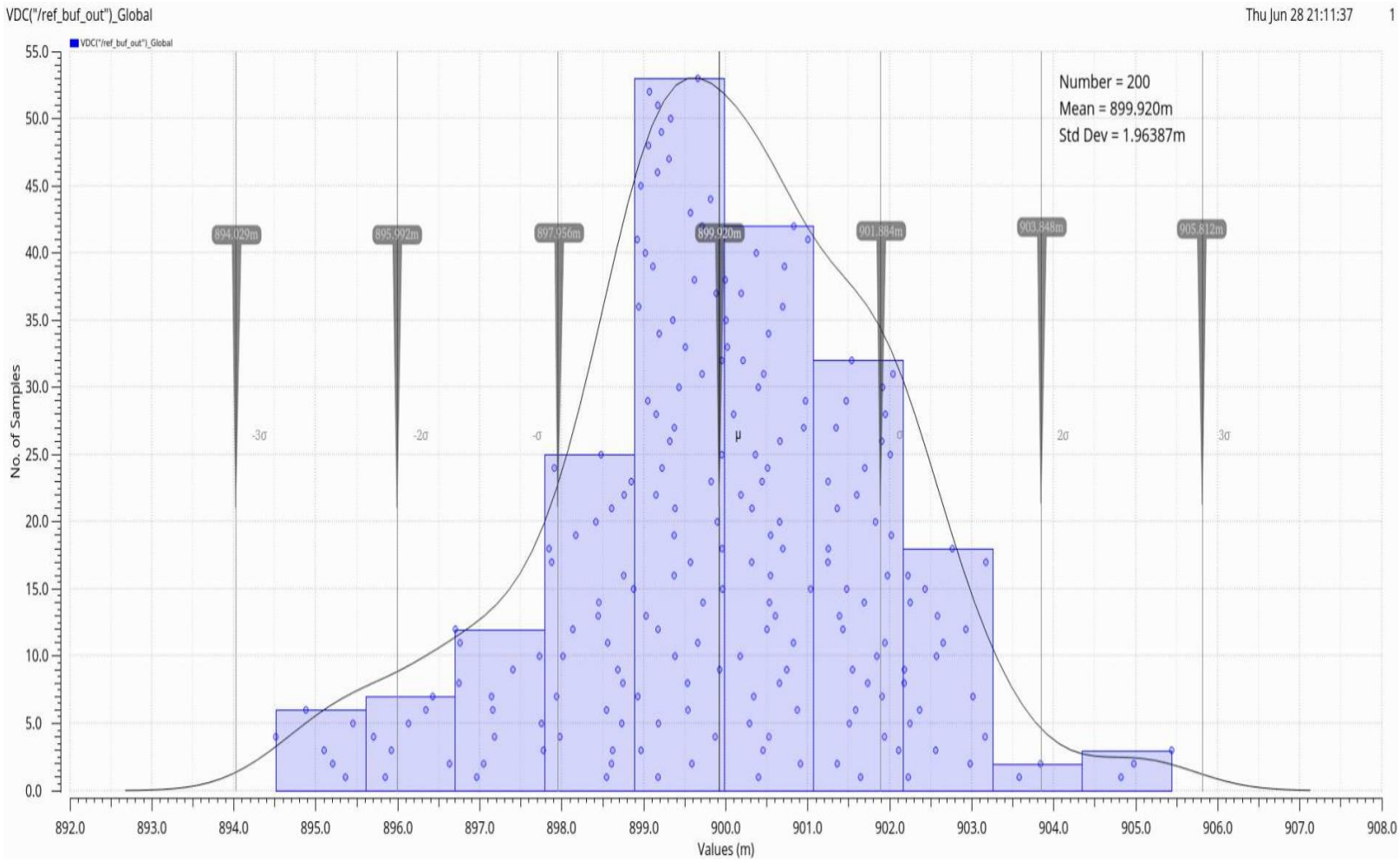

Figure 4.7 Monte Carlo DC Analysis of Buffer Output Voltage

4.2.4 DAC Step Settling

The DAC settling test bench was used to show the buffer's response to the DAC switching load during the bit trials. Setting the top plate to V_{CM} is the biggest switching load on the reference buffer. The plot below shows the buffer schematic response to the DAC steps in blue and the difference between this response and an ideal reference response in red. It demonstrates good settling, arriving within specification of 1% of the final settled value in 200ps. The purple plot shows the transient current response of the DAC reference to the switching loads.

Figure 4.8 DAC step settling and difference between settling with ideal reference and buffer reference

4.2.1 Supply Current Transient

The DAC step settling test involves large current transients from the supply voltage consuming a large amount of transient power.

Figure 4.9 shows the transient currents drawn during the bit cycling in the DAC. It illustrates the quiescent current of 12.7 mA and then the peak current of 19.5 mA after the switching instant of the MSB capacitor in the DAC. This is when the buffer is at its biggest load and most power is being consumed to settle the reference voltage.

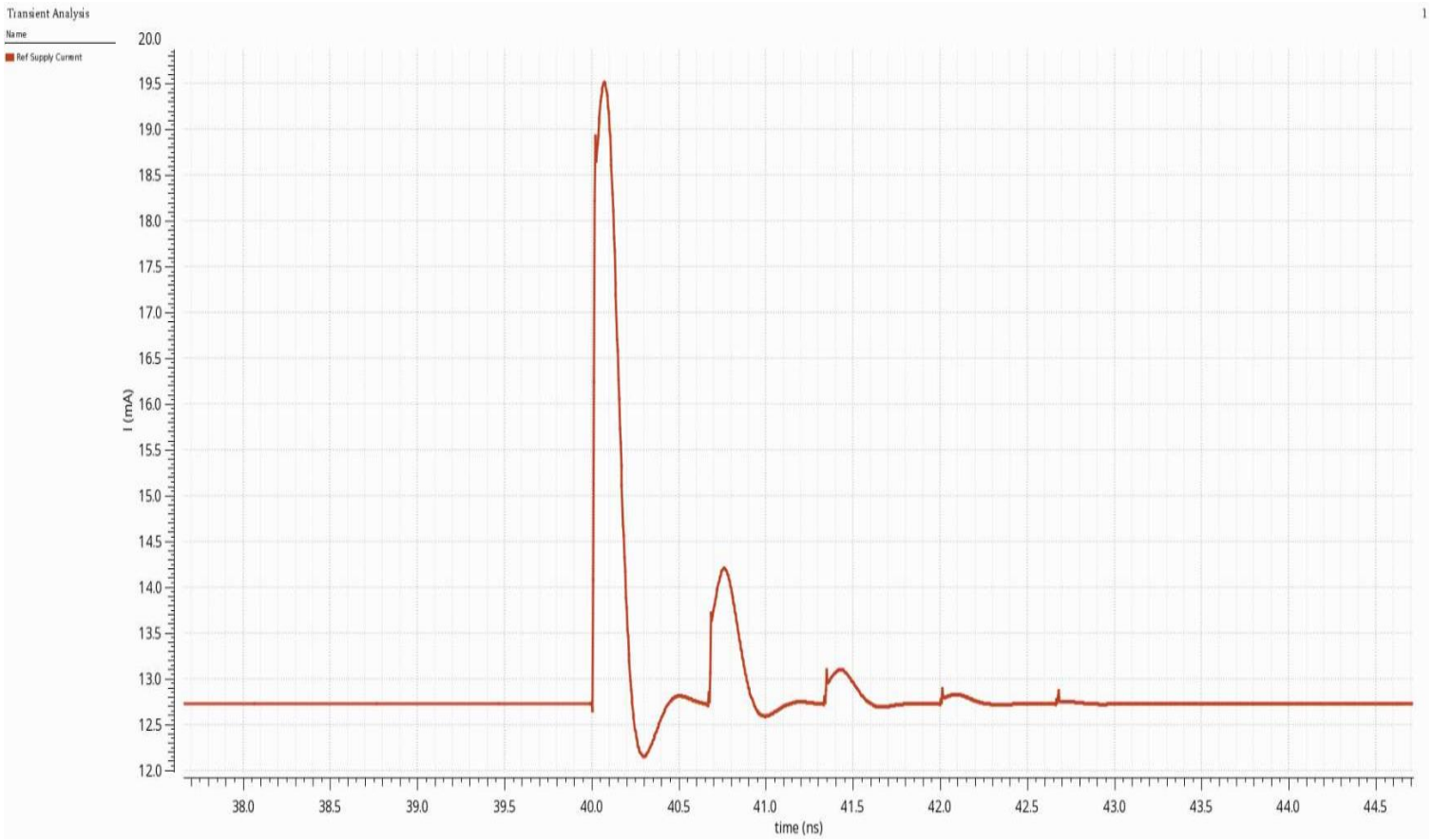

Figure 4.9 Buffer Supply Current Transient

4.2.2 Loop-gain Analysis

The plot of phase and gain of the amplifier schematic is shown below with a table showing the gain and phase margins for the amplifier and buffer schematic and extracted views.

Table 4.3 Loop-gain Analysis

Circuit Loop	Amplifier Schematic	Amplifier Extraction	Buffer Schematic (NGO loop)	Buffer Extraction (NGO loop)
Phase Margin	79.53°	78.48°	51.26°	39.1°
Gain Margin	31.85 dB	36.27 dB	19.84 dB	17.51 dB

The amplifier loop has adequate margin in both the schematic and extracted views. The NGO output loop of the buffer has adequate margin in the schematic view but could be preferably increased in the extracted view. The sudden change in the phase response on Figure 4.10 suggest possible instabilities in the circuit from non-dominant pole-zeroes in the circuit. However, the stability margins are adequate for the application.

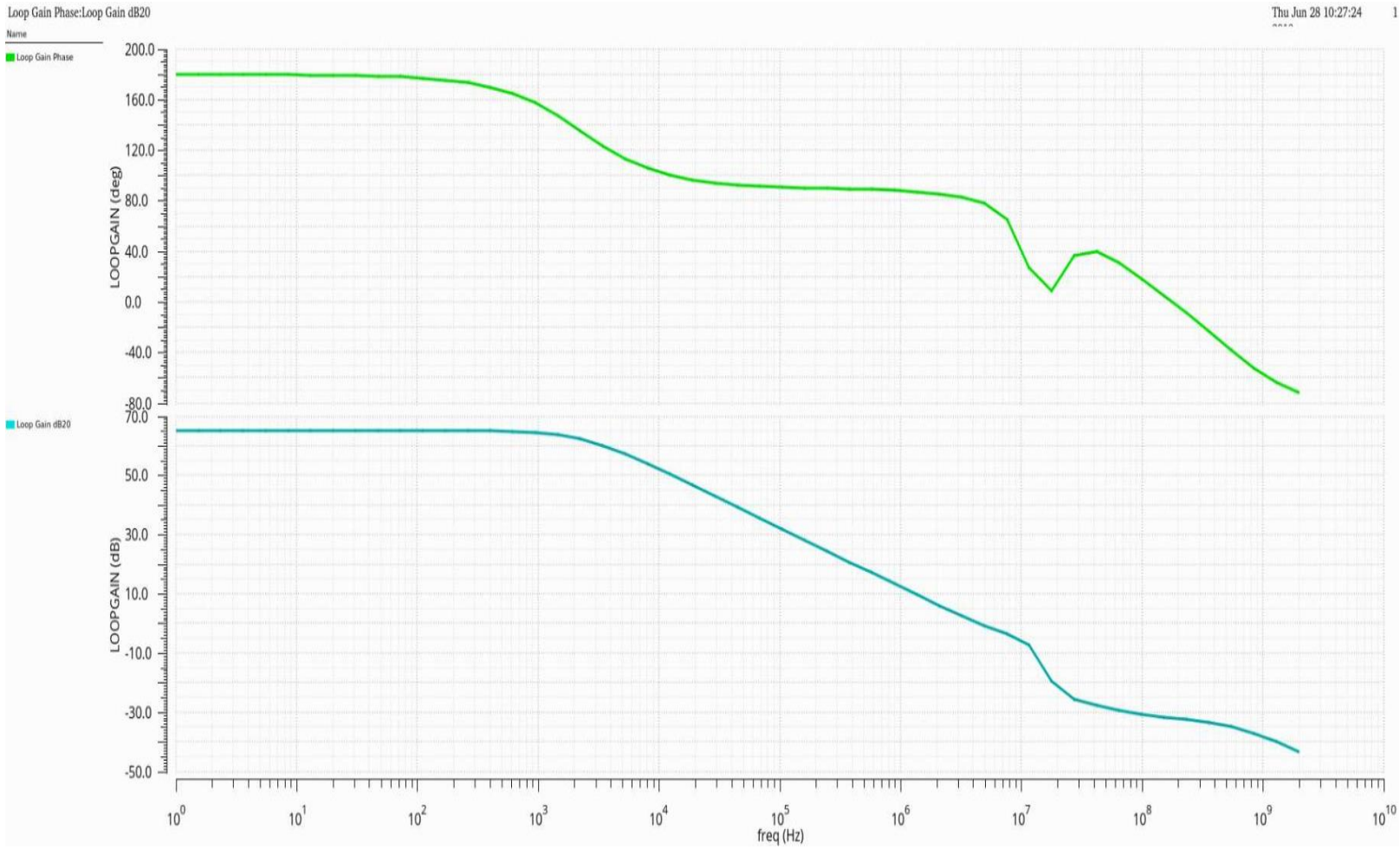

Figure 4.10 Loop-gain Analysis for Amplifier Schematic

4.2.3 AC Analysis

It was important to characterize the response at the output of the buffer to an ac signal at its input to determine its bandwidth and, ultimately its ability to filter input noise.

Figure 4.11 shows that the 3dB frequency of the buffer is 11.5 MHz, meaning that noise below this frequency will be allowed through. It is important, therefore, to have a large enough decoupling capacitor at the input to short the lower frequency noise to ground.

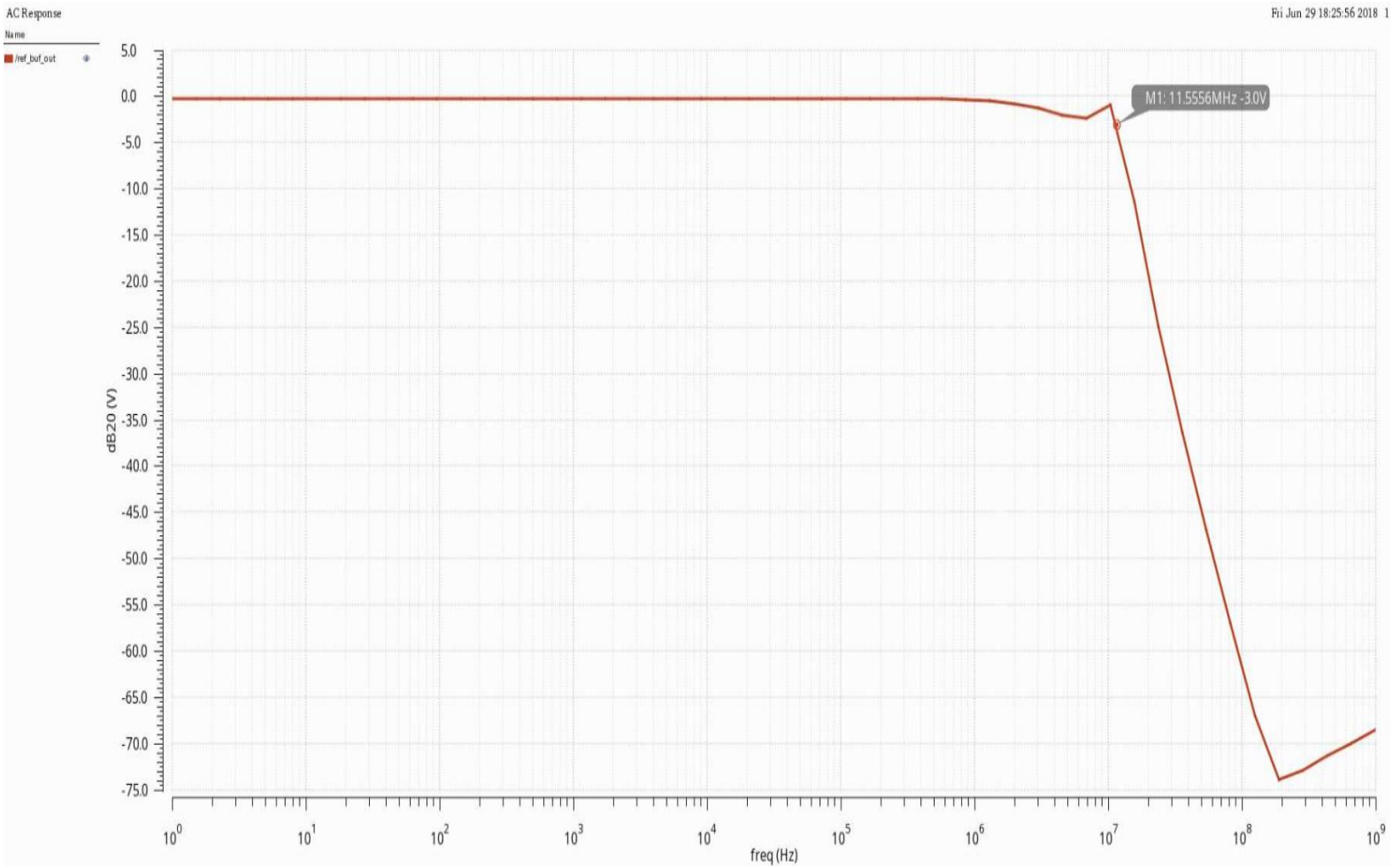

Figure 4.11 AC Response of Buffer

4.2.4 PSRR

The Power Supply Rejection Ratio is a measure of the ability of a circuit to suppress or reject perturbations or noise from coupling to the output node from the power supply.

It is defined mathematically as:

$$PSRR = 20\log_{10}\left(\frac{v_{out}}{v_{in,supply}}\right) \tag{4.1}$$

This test is carried out on the Buffer schematic by applying an AC input of 1V to the supply and measuring the AC response at the output. The PSRR is then found over frequency by obtaining a logarithmic plot of the output response.

The PSRR results in Figure 4.12 show suppression of low frequency noise coupling from the power supply to the output of the buffer, with noise above 10 MHz allowed through.

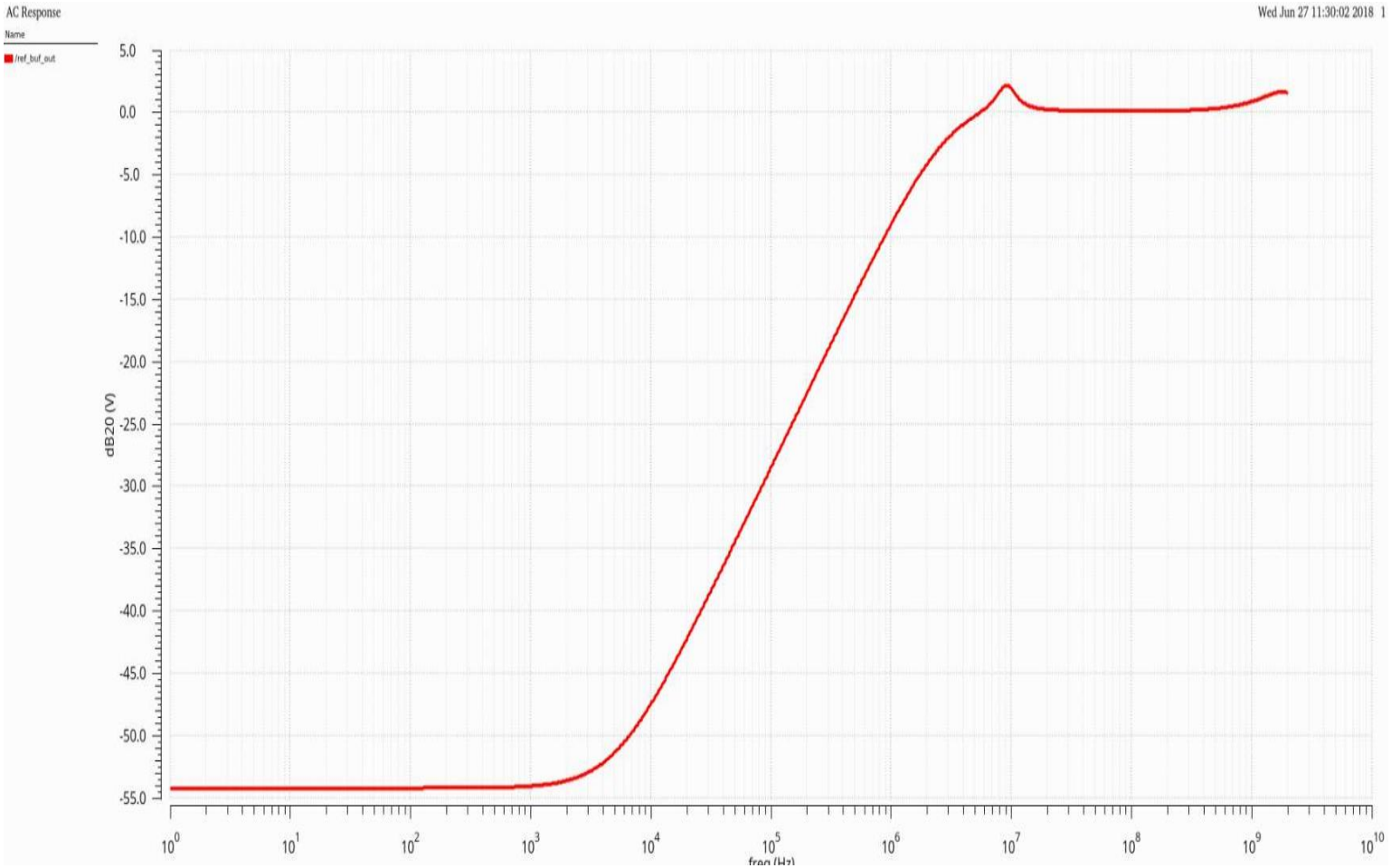

Figure 4.12 Buffer Schematic PSRR

4.2.5 Power Consumption

The reference buffer essentially operates under two distinct power dissipation modes. These are when the buffer is enabled or when the buffer is disabled. The power dissipated can be calculated by measuring the quiescent current drawn from the buffer supply, ref_buf_avdd. This is shown in the table below with more than 10 times a power saving in the buffer disabled mode.

Table 4.4 Power Consumption

Operation Mode	Current From avdd_1p2	Power
Buffer Enabled (schematic)	12.72 mA	15.264 mW
Buffer Disabled (schematic)	962.8 µA	1.16 mW
Buffer Enabled (extracted)	11.58 mA	13.89 mW
Buffer Disabled (extracted)	912.1 µA	1.09 mW

4.2.6 Transient Noise

Transient noise simulations were carried out on the buffer and amplifier with 100 runs, giving a good average for the outputs of both circuits. The simulation was set up to transition from buffer mode to bypass mode at 100 µs as shown in the figure below. It can be observed that the transient noise in the bypass mode is much reduced. The following figure shows the standard deviation for each iteration of the buffer and amplifier in buffer mode.

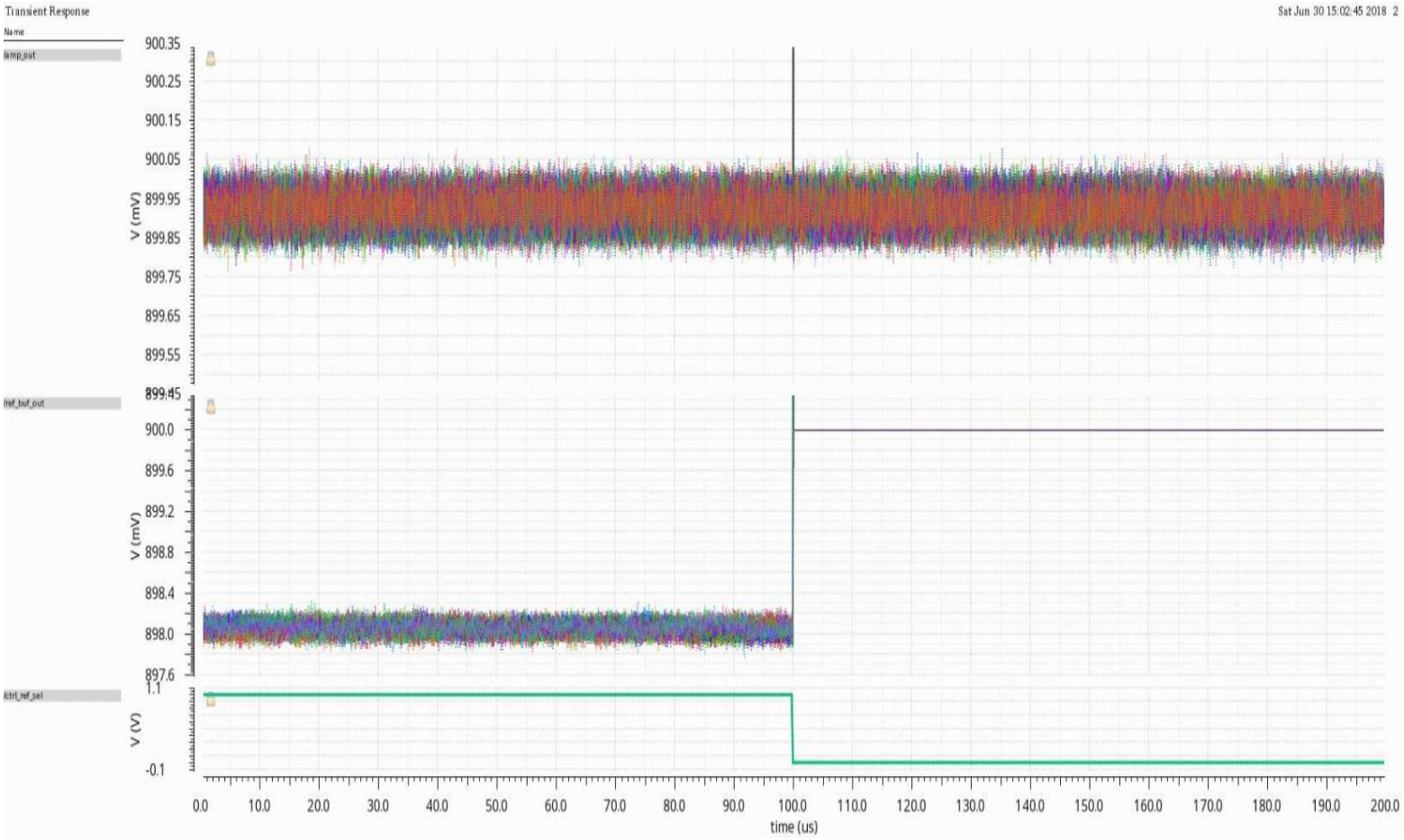

Figure 4.13 Transient Noise of Amplifier & Buffer Non-Bypass -- Bypass Mode

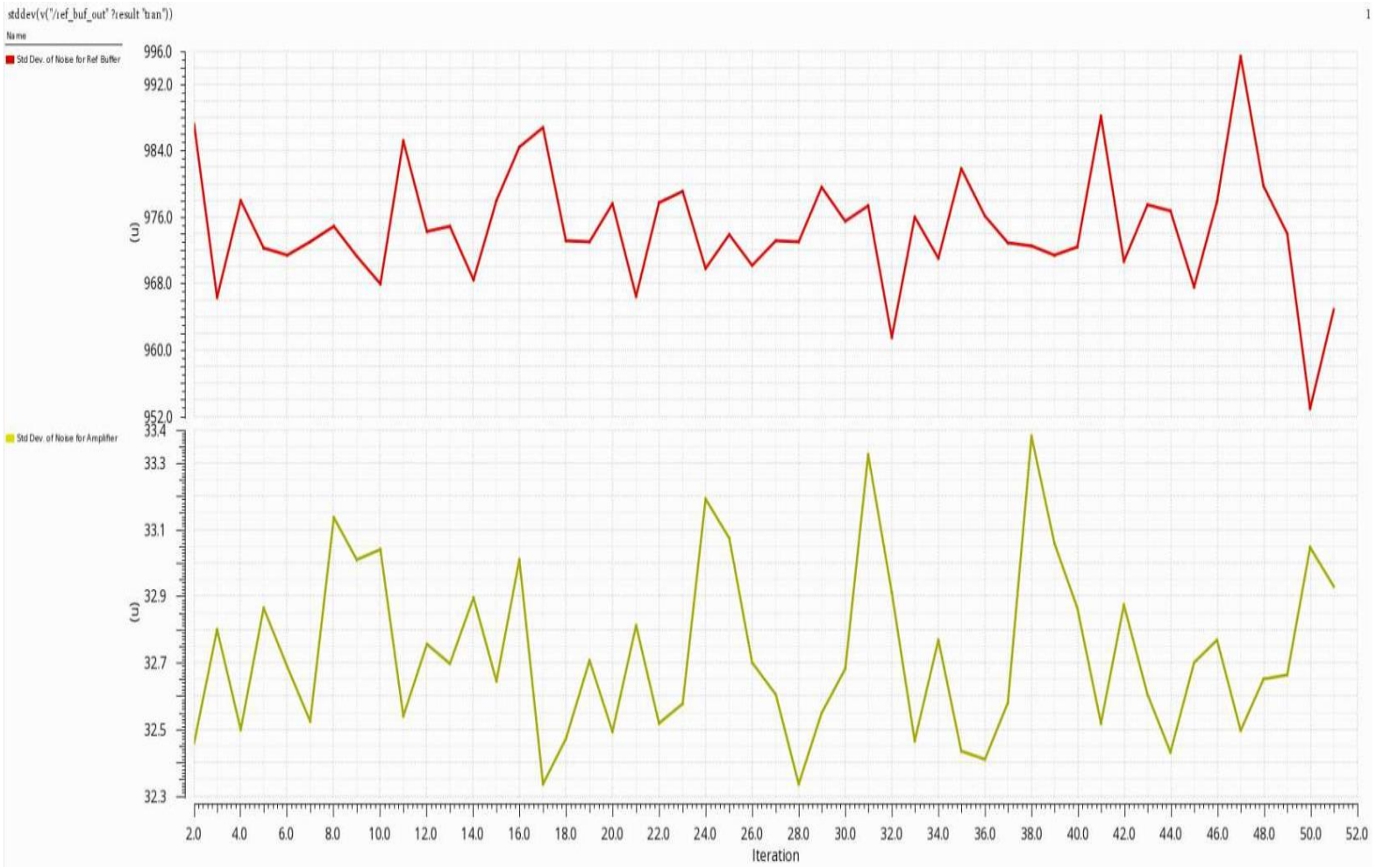

Figure 4.14 Standard Deviation of Amplifier and Buffer Noise across 100 Iterations

4.2.7 Output Integrated Noise

Table 4.5 Top 20 Noise Sources in the Reference Buffer

Device	Parameter	Noise Contribution	% Of Total
M70	id	1.3685 nV	16.24
MN4	id	0.7362 nV	8.74
MN3	id	0.6571 nV	7.80
MP5	id	0.6083 nV	7.22
MP8	id	0.46472 nV	5.52
MP4	id	0.3903 nV	4.63
M68	id	0.3717 nV	4.41
MN3	fn	0.3068 nV	3.64
MN4	fn	0.3057 nV	3.63
MP9	id	0.2686 nV	3.19
M37	id	0.2293 nV	2.72
M44	id	0.2282 nV	2.71
M74	id	0.1988 nV	2.36
M63	id	0.1919 nV	2.28
I57/M1	id	0.1358 nV	1.61
I57/M2	id	0.1351	1.60
I57/M3	id	0.1189 nV	1.41
/I57/M4	id	0.1117 nV	1.33

M43	id	0.0753 nV	0.89
M44	fn	0.06946 nV	0.82

Integrated Noise Summary in V^2 sorted by Noise Contributors.

- Total Summarized Noise = 8.42569 nV^2
- Total Input Referred Noise = 0.00330905 V^2

Signal to Noise ratio could be calculated from the integrated noise:

$$\text{Signal Power } = \frac{1}{2} v_{in}^2 \tag{4.2}$$

$v_{in} = 0.9,$

$Integrated\ Noise = 8.426 \times 10^{-9}$

$OSR = 32$

$$SNR = 10 \log_{10} \frac{P_{sig}}{\frac{P_{noise}}{OSR}} \tag{4.3}$$

$$SNR = 10 \log_{10} \left(\frac{(0.9)^2}{\frac{8.42569 \times 10^{-9}}{32}} \right)$$

$SNR = 94.88$ dB

The noise was reduced internally in the buffer by hanging 10 pF capacitors off the pcasc and NGO1 nodes and 5 pF capacitors off the ncasc and nbias nodes. This helped prevent noise from feeding through to the output by shunting it to the supply in the case of the PMOS nodes and to ground in the case of the NMOS nodes.

4.2.8 Buffer Enable/Disable Test

The control register ref_buf_en allows the user to enable or disable the buffer. In enable mode the buffer is operational with bias current flowing as required and the option to switch the output of the buffer in as a reference voltage. When the buffer is disabled, all the PMOS devices source connected to the supply have their gates pulled up to supply and all of the NMOS devices source connected to ground have their gates pulled to ground. This prevents the bias current from flowing in the buffer and effectively disables it in a low power mode, preventing it from being used as a voltage reference.

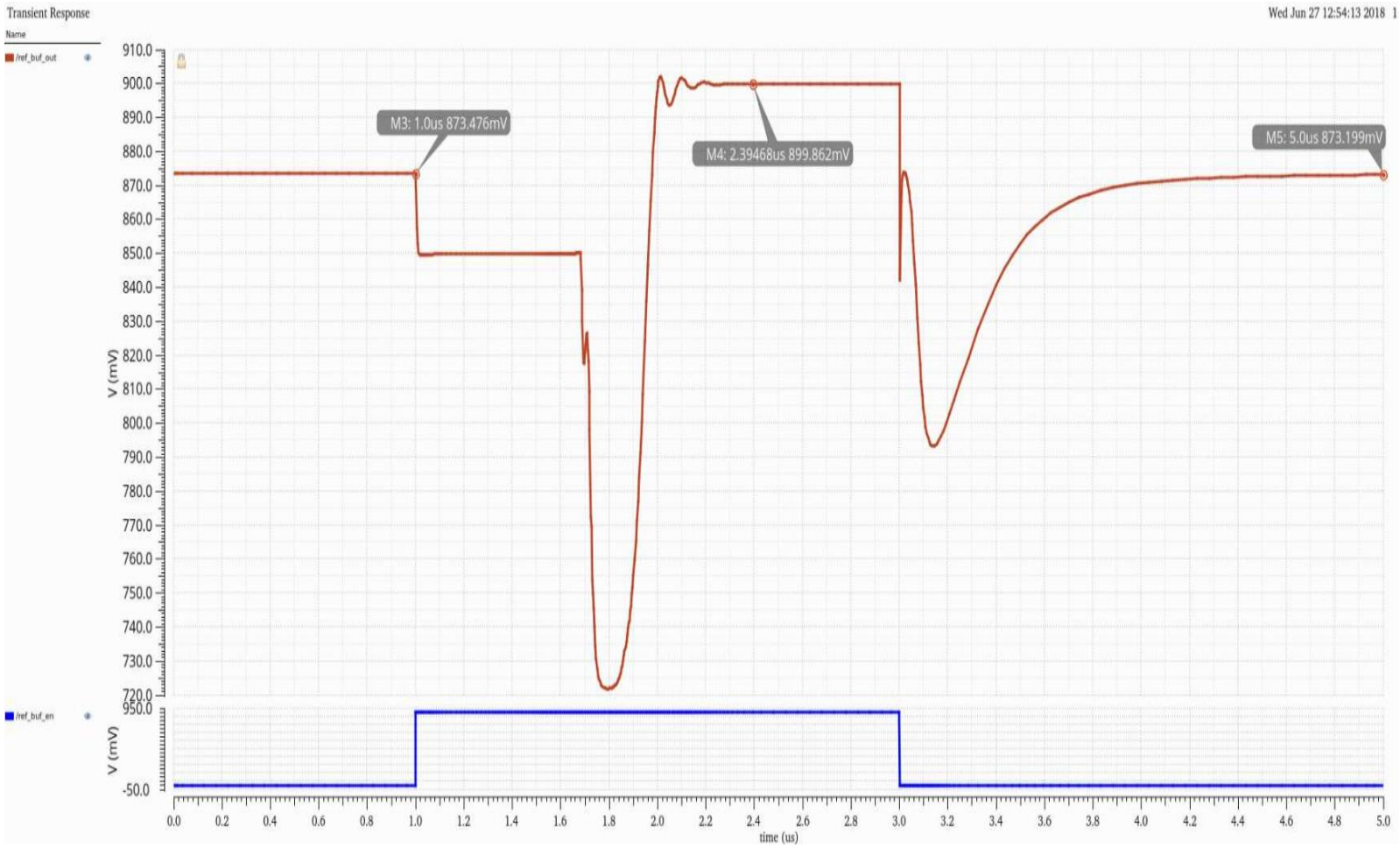

Figure 4.15 Buffer Disabled - Enabled - Disabled

4.2.9 Buffer Power Up/Down Supply Voltages

The digital supply voltage was ramped up to 0.9 V over 100 µs, it was allowed to settle for 100 µs and then the analogue supply voltage was ramped up to 1.2 V in 100 µs. The output was then allowed to settle to its DC value of 0.9 V for 100 µs and then the analogue and digital supplies were ramped off sequentially with a 100 µs gap in between. The digital supply was always on before the analog was turned on and remained on while the analog supply was turned off in order to retain control of the circuit. The plot below illustrates the response of the buffer output voltage and analogue supply current to this.

Figure 4.16 Power up/down of Analog & Digital Supplies

4.2.10 Summary of Buffer Results

Table 4.6 Reference Buffer Schematic Results Summary

Parameter	Conditions	Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
Settling % at 200ps	@typical conditions			0.71	%
-3dB small signal BW	@typical conditions		11.55		MHz
NOISE PERFORMANCE					
Output Integrated Noise	@typical conditions		8.43		nV^2/Hz
DC PERFORMANCE					
Offset Voltage	Process, temperature & supply voltage corners		0.09	1.9	mV
OUTPUT CHARACTERISTICS					
Output Current	MSB Load Step			11.36	mA
Loop Phase Margin	Process, temperature & supply voltage corners	50.28	51.23	70.06	Degree
Loop Gain Margin	Process, temperature & supply voltage corners	19.97	20.08	20.30	dB
POWER SUPPLY					
Quiescent Current	Bypass mode, buffer mode	0.96	12.72		mA
PSRR	<10 GHz		54		dB

4.3 ADC Top Level Results

4.3.1 Introduction

The top level simulations of the overall ADC are shown in this section. It shows the performance of the SAR + reference buffer to a ramp input and a sinewave input. The top level simulations invoked parasitic extracted models for the capacitor DAC and reference buffer and used a VerilogA model for the comparator. The model operates that on the clock rising edge if vinp > vinn the output is 1 and vinn > vinp the output is 0.

4.3.2 SAR + Reference Buffer Performance

The DNL of the SAR ADC with the reference buffer and redundancy enabled is shown below. It shows great performance with only the first and last code missing.

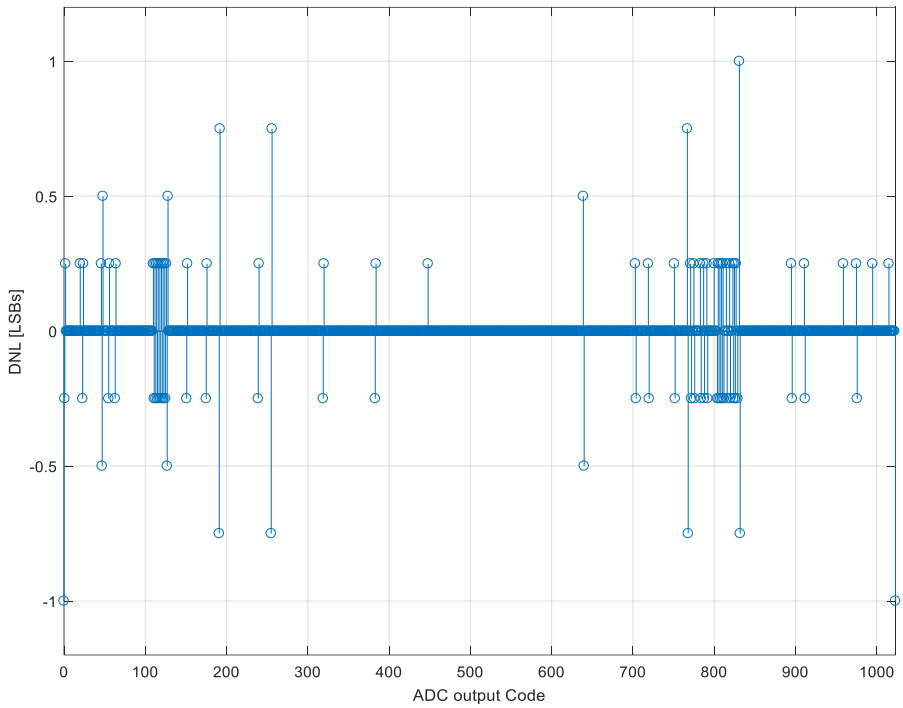

Figure 4.17 DNL for Top Level SAR with Reference Buffer and Redundancy Enabled

The plot below shows the INL plot for an input ramp with the reference buffer and redundancy enabled.

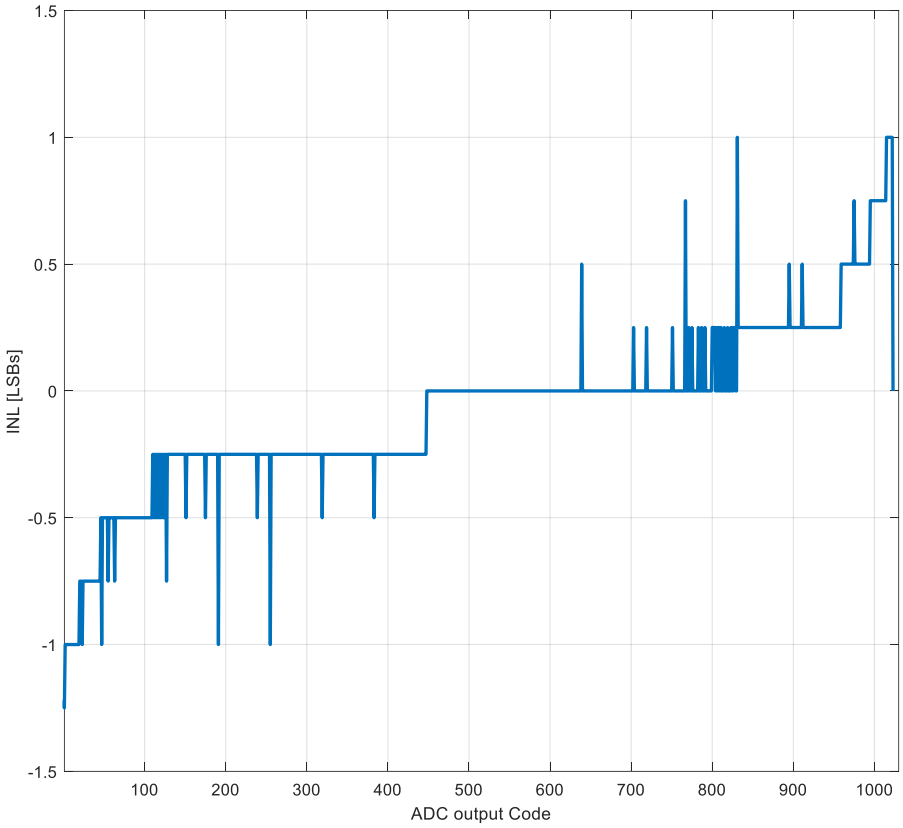

Figure 4.18 INL for Top Level SAR with Reference Buffer and Redundancy Enabled

The power spectral density plot below shows the performance of the top level SAR, without redundancy enabled, using the reference buffer and noise shaping circuits enabled to an input sinewave. It displays an SNR of 109.4 dB, which is better than all of the state of the art designs in Table 1.2. Likewise, the ENOB of 17.9 bits presented in Figure 4.19 achieves the target value of >15 bits in Table 1.1. Transient noise is only turned on for the reference buffer and is turned off for all other blocks.

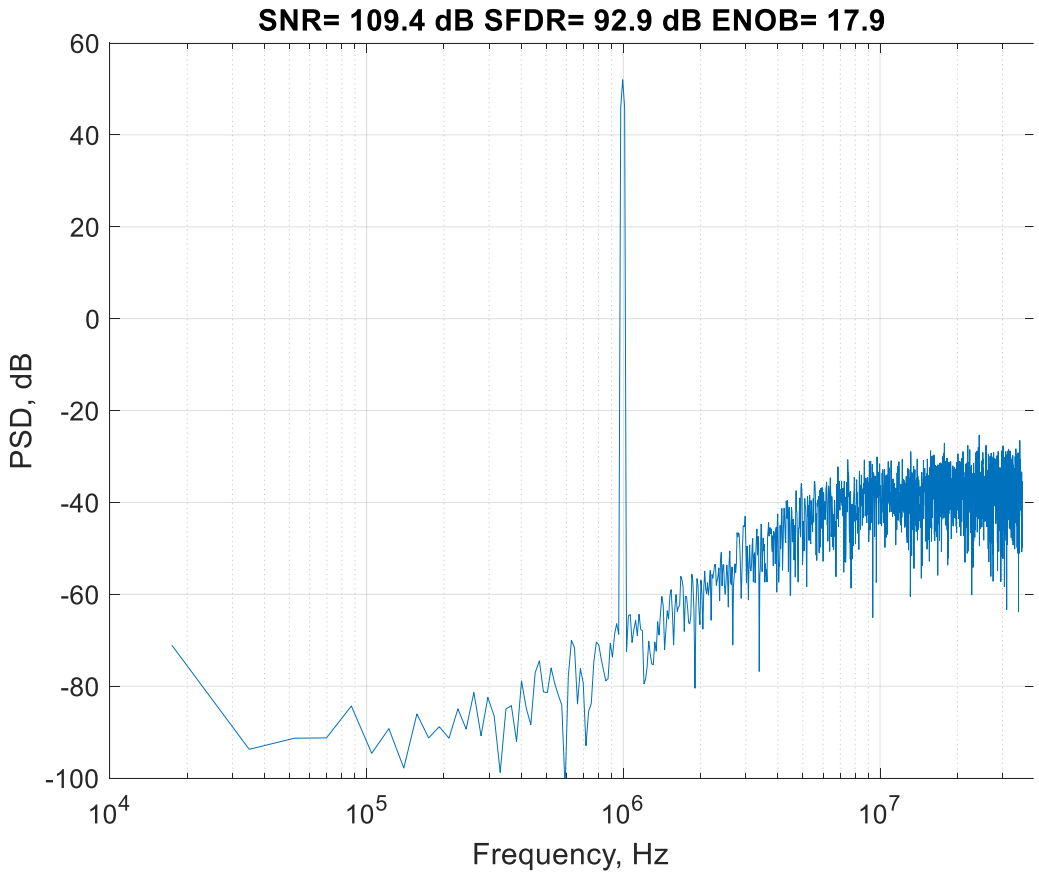

Figure 4.19 Power Spectral Density using Sine Wave Input with Non-Redundancy SAR & Reference Buffer (trnoise) with NS

The final plot below shows the results of the same simulation carried out in Figure 4.19 but without noise-shaping enabled. It shows an SNR of 60.7 dB and an ENOB of 9.8 bits, which was just below the targeted ENOB of 10 bits without noise shaping.

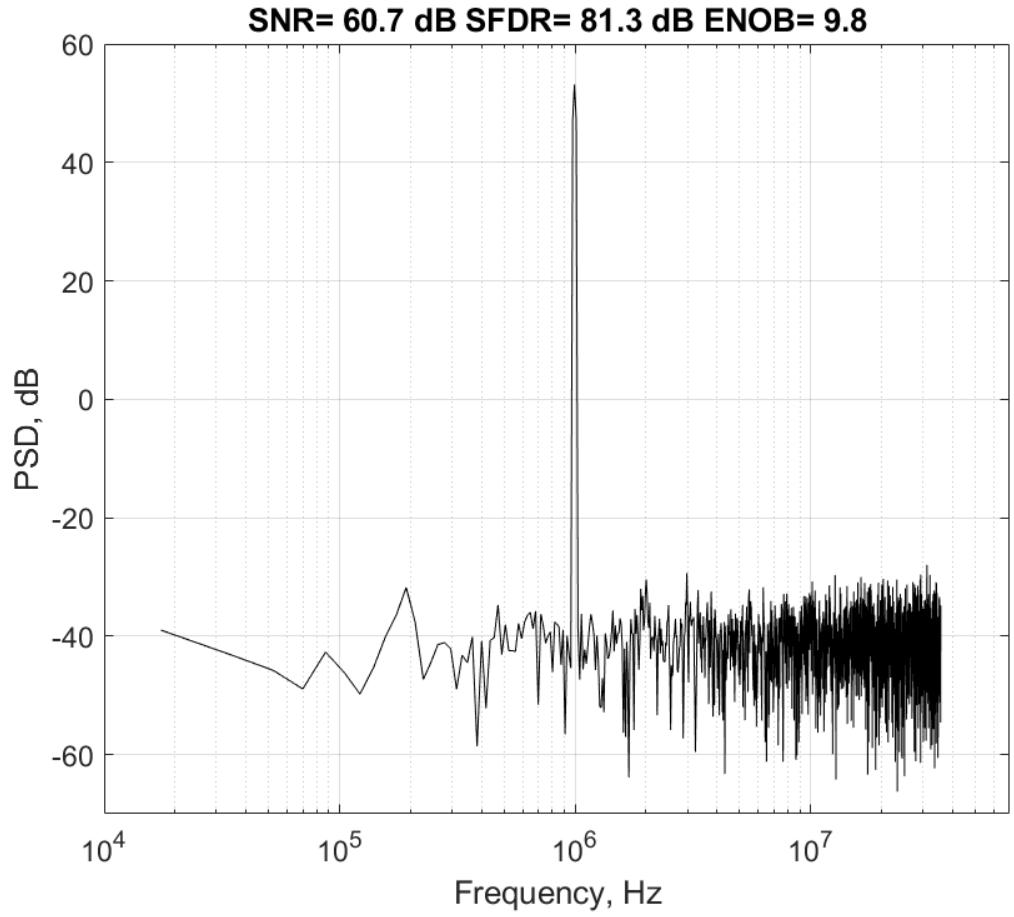

Figure 4.20 Power Spectral Density using Sine Wave Input with Non-Redundancy SAR & Reference Buffer (trnoise) without NS

4.4 Summary

This chapter showed the results obtained from this project. These results include DC Monte Carlo analysis, DAC step settling, Loop Gain analysis, AC analysis, PSRR, Power consumption, Supply current transients, Transient Noise and Output Integrated Noise. Some functional simulations showing the enable/disable and power up/power down functions are also shown. The end of the chapter illustrates the top level simulations and compares then to the targets set out at the beginning of the thesis.

5 Conclusions

5.1 Discussion

The objective of the work presented in this thesis was to design key blocks for a 10 bit, 100 MS/s SAR ADC. SAR ADCs perform well when operating at high speed, low resolution or low speed, high resolution. However, they struggle to perform at high speed, high resolution because of the nature of the successive approximation technique inherent in their design. They require sufficient settling time or smaller capacitors to settle in the required timeframe. This trade-off is analysed, with solutions proposed to relax the settling requirements, while increasing the speed and accuracy at which settling occurs.

A high resolution SAR ADC is limited by the resolution of the DAC. A switched capacitor DAC is implemented because it removes the requirement for an extra sampling capacitor and provides better matching than other topologies. A 10-bit split capacitor DAC was implemented to allow for larger unit capacitors and, thus, better matching, without increasing the overall size of the array excessively and increasing the demands on the settling. DNL and INL were kept to less than half an LSB and the layout was optimized to reduce mismatch between the individual capacitors and capacitor columns. Redundancy was added to relax the settling criteria and account for previous settling errors in the bit trials.

A Flipped Voltage Follower was chosen as a solution to the reference settling problem observed in the ADC. It was used because of its high current sourcing ability, zero voltage

offset and its dynamic feedback loop which enabled quicker settling to a transient voltage step.

The top level ADC simulations using parasitic extractions show that this design beats the target specifications on resolution using noise shaping at 17.9 bits, compared to the target of > 15 bits. It achieved an SNR of 109.4 dB, which was better than all of the state of the art designs shown in Table 1.2. With noise shaping turned off (noise shaping wasn't within the scope of this thesis), the ENOB of the ADC was 9.8 bits, just short of its target of 10 bits. The Capacitive DAC and buffer designs ensured the linear performance of the ADC was good with a maximum DNL and INL of 1 bit. The target power consumption of the buffer block was 10 mW but the actual consumption in simulations on parasitic extractions was 13.89 mW.

5.2 Future Work

5.2.1 Reference Error Calibration

The implemented reference buffer design required a large amount of current and, as a result, consumed a significant amount of power to settle the reference voltage in the required timeframe. In future work it would be of major benefit to deliver a less power hungry solution with the same levels of accuracy. This could be achieved by using reference error calibration to relax the tight constraints on the reference generation as achieved by Chi-Hang Chan et al. in [56] who differentiated the error outputs from the signal dependent switching transients and performed a subtraction in the digital domain.

5.2.2 Dynamic Element Matching

One of the main limiting factors for the resolution of the switched capacitor DAC and the overall ADC was the mismatch between the individual unit capacitors in the DAC introduced during circuit fabrication, resulting in non-linear distortion. DEM works by randomizing the usage of the individual capacitors causing the error created from the mismatches to be uncorrelated, pseudorandom noise rather than signal dependent distortion. Mismatch-scrambling DEM DACs create white noise and are used in Nyquist rate applications, while Mismatch-shaping DEM DACs is spectrally shaped and used in oversampling applications. This is discussed in depth by Ian Galton in [57]. In future work research would be carried out on mismatch-shaping DEM to mitigate the inevitable mismatch problems in the DAC and reduce the overall matching requirements.

5.2.3 DAC Digital Calibration

The accuracy of the output voltage of a DAC is dependent on gain and offset error in the DAC and from other components, such as switches. Digital calibration takes these errors into account and modifies the digital inputs sent to the DAC to remove the effect of these errors. This is an effective way of increasing DAC performance without requiring component trimming or off-chip solutions. It would be worth future research to further improve the performance of the DAC.

5.2.4 Switching Schemes

The switching schemes implemented in the SAR ADC has a major effect on overall power consumption. The conventional switching scheme implemented in most switched capacitor DACs is energy inefficient because the average energy consumed by the charging/discharging of the capacitors determines the switching efficiency. A merged capacitor switching scheme consumes significantly less energy than the conventional or split capacitor switching scheme as described in [58]. Future work on this project would benefit from researching and implementing a more power efficient switching scheme that benefits from good linearity and dynamic performance.

5.2.5 Asynchronous Timing

Asynchronous timing would benefit future work on the design because it would allow the SAR to switch faster as a result of shorter comparator time. Alternatively, it could relax the reference settling timing constraints for the same sampling speed. A full comparison on Synchronous and Asynchronous ADCs is given in [59].

Appendix A

A.1 Derivation of CDAC Equivalent Voltage Model

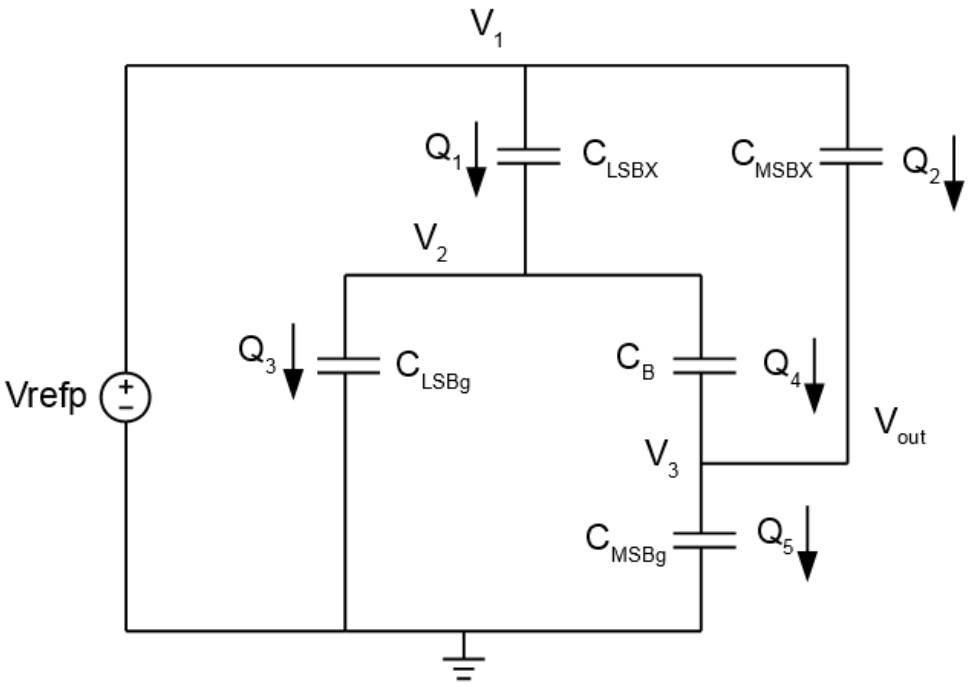

Figure A.1 Equivalent charge flow diagram of Split Capacitor DAC

1. Calculate the charge flowing in and out of each node in the circuit.

$$Q_1 = (v_1 - v_2)C_{LSBx} = (V_{refp} - v_2)C_{LSBx} \quad \text{(A.1)}$$

$$Q_2 = (v_1 - v_3)C_{MSBx} = (V_{refp} - v_{out})C_{MSBx} \quad \text{(A.2)}$$

$$Q_3 = (v_2 - 0)C_{LSBg} = v_2 C_{LSBg} \quad \text{(A.3)}$$

$$Q_4 = (v_2 - v_3)C_B = (v_2 - v_{out})C_B \quad \text{(A.4)}$$

$$Q_5 = (v_3 - 0)C_{MSBg} = v_{out} C_{MSBg} \quad \text{(A.5)}$$

2. The charge flowing into a node is equal to the charge flowing out of a node:

$$Q_1 = Q_3 + Q_4 \tag{A.6}$$

$$Q_5 = Q_2 + Q_4 \tag{A.7}$$

3. Two unknowns; v_2 and V_{out}. Must find equation (A.6) in terms of v_2:

$$(V_{refp} - v_2)C_{LSBx} = v_2 C_{LSBg} + (v_2 - v_{out})C_B \tag{A.8}$$

$$v_2(C_{LSBg} + C_{LSBx} + C_B) = V_{refp}C_{LSBx} + V_{out}C_B \tag{A.9}$$

But, $$C_{LSB} = C_{LSBx} + C_{LSBg} \tag{A.10}$$

$$v_2 = \frac{V_{refp}C_{LSBx} + v_{out}C_B}{C_{LSB} + C_B} \tag{A.11}$$

4. This can now be subbed into equation (A.7) to find V_{out}:

$$v_{out}C_{MSBg} = (V_{refp} - v_{out})C_{MSBx} + (v_2 - v_{out})C_B \tag{A.12}$$

$$v_{out}C_{MSBg} = (V_{refp} - v_{out})C_{MSBx} + (\frac{V_{refp}C_{LSBx} + v_{out}C_B}{C_{LSB} + C_B} - v_{out})C_B \tag{A.13}$$

$$v_{out}\left(C_{MSBg} + C_{MSBx} + C_B - \frac{C_B^2}{C_{LSB} + C_B}\right) = V_{refp}\left(C_{MSBx} + \frac{C_{LSBx}C_B}{C_{LSB} + C_B}\right) \tag{A.14}$$

But, $$C_{MSB} = C_{MSBx} + C_{MSBg} \tag{A.15}$$

$$v_{out} = \frac{V_{refp}\left(C_{MSBx} + \frac{C_{LSBx}C_B}{C_{LSB} + C_B}\right)}{C_{MSB} + \frac{C_B C_{LSB}}{C_{LSB} + C_B}} \tag{A.16}$$

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