High Frequency Point-of-Load (POL) DC-DC Converters Employing CMOS or GaN HEMT Switches

By Eoin Walsh.

Submission for MEngSc. University College Cork.

Supervisors

Mr. Séamus O'Driscoll

Dr. Terence O'Donnell

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Abstract

This thesis compares 2-level and 3-level buck converters, for use in very high frequency Point-of-Load (POL) DC-DC conversion. The nominal conversion is from 5 V to 1.8 V, at a 1 A output current, as is appropriate for use in a battery powered device. Today's typical commercial POL solution for this challenge employs a monolithic CMOS power switcher operating at 2-3 MHz and uses a discrete surface mountable (SMT) ferrite chip inductor. This work investigates the performance achievable over the 20-40 MHz range with the use of a new specially designed and fabricated Tyndall thin-film magnetics-on-silicon (tf-MoS) inductor component.

Two different power switching bridge types, CMOS and GaN, are investigated by both analytic loss modelling and by SPICE simulation. The CMOS bridge assumes a PMOS and NMOS combination using device models from a 180 nm CMOS process and the GaN bridge is based on commercially available discrete enhancement mode GaN HEMT switches. A behavioural model for a state-of-the-art commercial driver is developed. Measurements are initially made on a prototype 2-level GaN bridge circuit with open-circuit switch-node to allow for determination of load independent silicon losses. These measurements are used to validate both the switch with driver models and the circuit loss analyses.

Inductor loss is one of the key practical limitations towards achieving very high frequency switching. Both modelling and measurement techniques are used to investigate the performance of the custom thin-film inductor. An ultimate reference case, low-loss air-core inductor was wound and used to measure the lowest achievable complete converter loss over the 20-40 MHz range. Two SMT ferrite chip inductor options were selected based on datasheets review and fitted in the prototype to achieve the best performance with currently available commercial components. These three inductors and a new custom Tyndall thin film inductor are all simulated and tested in combination with the 2-level GaN switching bridge.

The measured overall efficiencies with loss breakdowns are presented for the various combinations of switch components and inductor technologies in 2-level converter. These measurements validate the models and simulations so that simulations for an extension to the 3-level converter and its performance comparison versus the 2-level converter may be made.

1. Introduction

1.1 Introduction to Buck Converters

In this thesis, Point-of-Load (POL) voltage regulation, using the DC-DC buck (step-down) converter is investigated. The focus is on the low power, mobile application. The battery voltage will vary, depending on factors such as state-of-charge, temperature, and load current, whereas the components being powered (for instance the CPU or transceivers), will be designed for a specific well-regulated input voltage. The POL converter provides the tightly regulated voltage with the high bandwidth necessary to support a rapidly changing load. For such a converter, in mobile applications, it is highly desirable to reduce the size, height and weight of the components involved. This thesis investigates the possibility of increasing the switching frequency (or effective switching frequency) to reduce size of the passive components (inductor and capacitors). The implication of the increased switching frequency and smaller passive component sizes and values on converter efficiency is considered.

The multi-level topology [10] multiplies the effective switching frequency of the inductor (for given switch frequency), reduces the voltages across the transistors and reduces the applied inductor volt-seconds. The multi-level technique can be utilised to reduce the inductor value or to increase efficiency. The drawback of the multi-level topology is that it adds additional switches, drivers, control complexity and capacitors to the circuit. This thesis compares the 2-level buck converter with a 3-level version of a multi-level buck converter.

The inductor filters the switch-node voltage and delivers smooth current into the output. Typically, the inductor is the largest component in the converter and hence this thesis focuses on all factors which influence its size. A larger inductance provides lower current ripple but at the expense of larger sizes because inductor volume is proportional to inductance value. The inductance value influences the operating mode of the converter and for instance; its value may be chosen to allow its current to go slightly negative (boundary conduction mode, BCM) before the high-side switch turn-on to create zero voltage switching (ZVS) on the high side switch. This thesis will also examine the inductor losses and size for a variety of inductor device formats and materials.

By increasing the switching frequency, a smaller inductor can be used to achieve the same amount of output ripple. This increases the losses in the switches, and switches that are capable of very high switching frequencies will generally handle lower voltages. The choice of switches is very important to achieve high efficiency at high frequency. High frequency allows lower switching ripple and small component sizes, for inductors and capacitors.

The switch, inductor, and topology trade-offs are explored by simulation and experiment for 2-level and 3-level buck converters in the 20-40 MHz range.

This chapter provides an overview of how the 2-level and 3-level buck converters operate. The challenges of operating inductors and switches at high switching frequencies and the loss mechanisms with each are also explored.

1.2 Step Down Converter Topologies

For step-down DC-DC voltage conversion there are several popular topologies, with their own benefits and drawbacks. Voltage dividers or linear regulators are simple but by their very nature their efficiencies are dictated by conversion ratio. Converters such as the forward or flyback which use transformers may be unnecessarily bulky for low power applications, they are better suited for higher voltages or when isolation is required. Switched-Capacitor (SC) converters can have very small footprints while delivering very high

efficiency at a fixed conversion ratio. The SC and buck converters may be merged to create a hybrid converter which boast smaller footprint and high efficiency with dynamic voltage regulation. SC converters and their hybrids work best at lower powers and with larger step-down ratios.

1.2.1 Buck Converter

The ideal topology diagram for the basic (2-level) synchronous buck converter is shown in Figure 1.1(a). The core concept behind the buck converter, is that two switches are used to chop a DC voltage into a pulsed waveform with smaller average voltage than the input DC voltage. The high-side switch is referred to as Sw_{HS} and the low-side switch as Sw_{LS}. When one switch is on the other is always off, to avoid short-circuiting or "shoot-through". When Sw_{HS} is on $V_{sn} = V_{in}$, and when Sw_{LS} is on $V_{sn} = 0$ V. Thus, the pulse width is Sw_{HS} on-time (t_{on}) and the pulse goes from ground to V_{in}. The ratio of t_{on} and the switching period (T_{sw}), is referred to as the duty cycle ($D = t_{on}/T_{sw}$). This pulse is then applied to an LC filter to create a smooth DC output voltage, with low ripple. In a lossless converter, the output voltage (V_{out}) is:

$$V_{out} = DV_{in}. \quad (1.1)$$

When Sw_{HS} is on the inductor (L) sees a positive voltage ($V_L = V_{in} - V_{out}$), hence it has a positive current ramp. When Sw_{HS} is off, the inductor sees a negative voltage ($V_L = -V_{out}$), and discharges through Sw_{LS} and the output. The converters in this thesis are operated with mostly positive inductor current. For the synchronous buck converter, the inductor current may be positive or negative during continuous conduction mode (CCM). The output capacitor (C_o) absorbs AC inductor current ripple and provides steady output voltage.

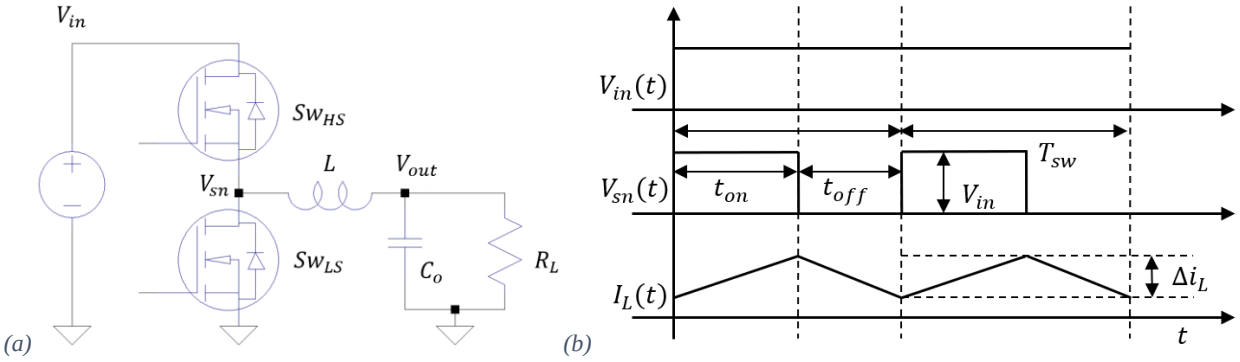


Figure 1.1. Ideal buck converter: (a) circuit diagram, (b) input voltage, switch-node voltage, and inductor current waveforms.

For (CCM) the equations used to determine the minimum output capacitance (C_{min}) and the minimum inductance (L_{min}) required are:

$$C_{min} > \frac{\Delta i_L}{8 * f_{sw} * \Delta v_{out}} \quad (1.2)$$

and

$$L_{min} > \frac{V_{out}(1 - D_{min})}{f_{sw} * \Delta i_{L(max)}} \quad (1.3)$$

where Δi_L is the inductor current ripple; Δv_{out} is the output voltage ripple; D_{min} is the minimum duty cycle (maximum possible input voltage); and $\Delta i_{L(\max)}$ is the maximum ripple current (maximum possible input voltage). The capacitance and inductance are both inversely proportional to the switching frequency. Typically, the larger the capacitance and the larger the inductance the larger the physical sizes of the

capacitor and inductor required. Increasing switching frequency, can be used to decrease inductors and capacitors size, but their losses may increase. Reducing the sizes of the switches will reduce their parasitic capacitances but will cause greater on-resistances and hence large conduction losses.

1.2.2 3-Level Buck Converter

The circuit diagram for the 3-level buck converter is shown in Figure 1.2(a). The 3-level has a similar structure to the 2-level buck converter, with the addition of two more switches and a flying capacitor (C_{fly}). The flying capacitor voltage ($V_{C_{fly}}$) is charged to nominally $V_{in}/2$.

The switching waveforms for the 3-level topology are shown in Figure 1.2(b). This topology has three possible switch-node voltage levels: V_{in}, $V_{in}/2$, and ground. By managing these at the switch-node, this allows for an output voltage range from ground to V_{in}. The operation mode in this thesis is for $0 < V_{out} < V_{in}/2$. Each period can be broken into four stages.

Stage 1: Sw_{HS1} and Sw_{LS2} are on. The inductor voltage is positive ($V_L = V_{C_{fly}} - V_{out}$). Note C_{fly} is applied at the switch-node to charge the inductor. This stage's duration is determined by Sw_{HS1} on-time ($t_{on(HS1)}$). For this thesis, both high-side switches have the same on-time ($t_{on(HS)}$).

Stage 2 and Stage 4: Sw_{LS1} and Sw_{LS2} are on. The inductor voltage is negative ($V_L = -V_{out}$), it discharges through the low-side switches and the output.

Stage 3: Sw_{HS2} and Sw_{LS1} are on. V_{in} is connected in series with C_{fly} and the inductor, both of which are charged. The inductor voltage is positive ($V_L = V_{in} - V_{C_{fly}} - V_{out}$); it is being charged.

For linear charging of the inductor, C_{fly} is chosen so that there is negligible voltage ripple on the flying capacitor ($\Delta v_{C_{fly}}$ << Vin). The duty cycle is defined as $t_{on(HS)}/T_{sw}$.

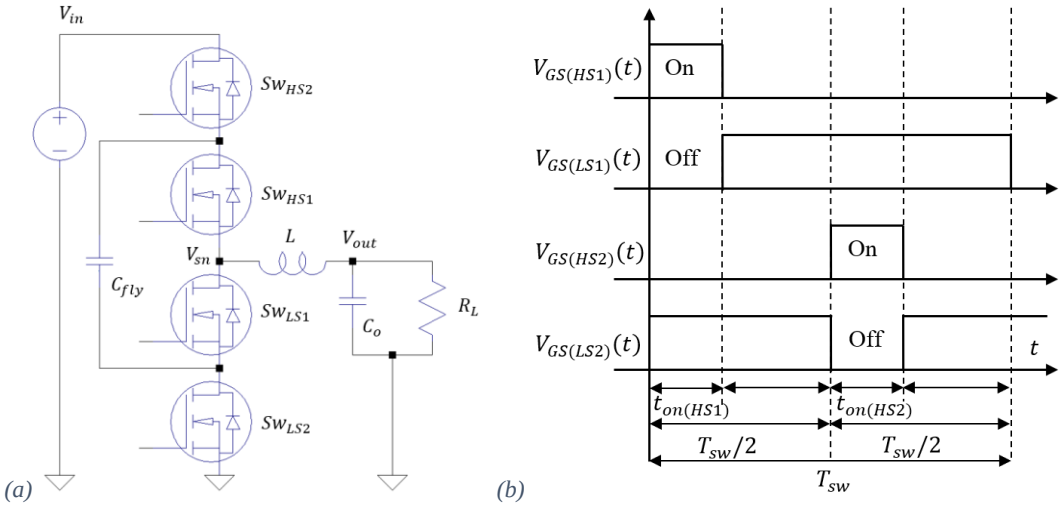


Figure 1.2. The ideal 3-level buck converter: (a) circuit diagram, (b) switches' gate-source voltage waveforms.

There are three benefits to this topology, firstly in the 2-level buck converter the switches must block the entirety of V_{in}; in the 3-level they only have to be able to block $V_{in}/2$. The smaller switch voltage rating allows for reduction in losses and smaller switch size and enables operation at higher f_{sw}. Secondly, (assuming that $\Delta v_{C_{fly}}$ is negligible) the voltage that the inductor has to step-down halves from V_{in} to $V_{in}/2$,

and thus D is doubled so that L_{min} can be reduced per Equation (1.3). The nominal D for the 2-level converter in this thesis is 0.36, thus L_{min} is approximately halved. Thirdly, the inductor is charged and discharged twice per period, doubling its effective frequency (f_{eff}). As per Equation (1.3) this means that L_{min} is halved of the equivalent 2-level. Combining the second and third benefits, L_{min} can be reduced to approximately a quarter (for D=0.36) for same switch switching frequency. The drawbacks to the 3-level are the additions of extra capacitors, switches and drivers with their associated footprints and losses. The circumstances where the 3-level buck converter is a viable alternative is an overall focus for this thesis.

1.3 Inductor Considerations

In the typical POL converter, the inductor takes the largest amount of space. It is shown from the inductance equation, that inductance is proportional to area:

$$L = N_{turns}{}^2 * A_{cross} * \mu / l_{core} \qquad (1.4)$$

where N_{turns} is the number of turns, A_{cross} is the cross-sectional area of the inner core material, μ is the magnetic permeability of the core, and l_{core} is the mean core length. Thus, for a larger inductance a larger core is needed or more turns, hence larger inductor size.

A lumped inductor model is shown in Figure 1.3. It has an inductance value L_{var} which is frequency dependent, due to the amplitude permeability ($\mu_A(f)$) characteristic. C models the inductor's self-capacitance, and R_1 is determined at the devices' resonant impedance. R_2 represents the DC resistance loss. The frequency dependent variable resistors, R_{var1} models the skin and proximity effects. R_{var2} models the core loss.

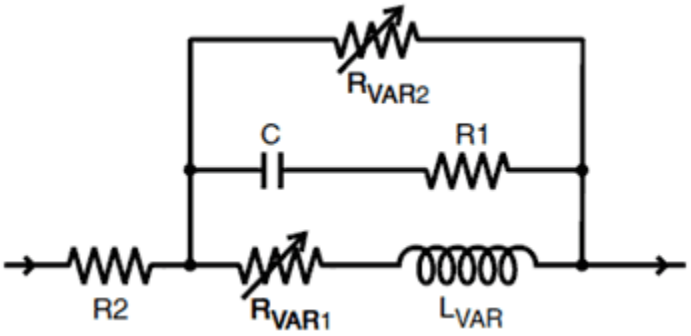


Figure 1.3. The equivalent circuit model for an inductor. Image from Coilcraft (website).

The basic layout of an inductor is a wire coiled around a highly magnetic core. As current is passed through the turns, energy is stored in an electromagnetic field. A changing current creates an induced EMF which will be in a direction to try oppose the change in current. The direct current resistance (DCR) or winding resistance, is the resistance through the length of the wire that is coiled around the core [1]. The self-capacitance passes the high frequency displacement current flowing across the winding as each winding turn creates a small capacitor with its neighbouring turn.

The skin effect in a conductor causes higher resistance at higher frequency because of the tendency for high frequency current to flow at the surface due to the decrease in the magnetic field penetrating the conductor [2]. The proximity effect causes a higher resistance at higher frequency due to circular or eddy currents caused by the ac magnetic fields created by the currents in nearby conductors. Both skin and proximity effects are frequency dependent [3].

Some of the core loss is due to eddy currents in the core magnetic material [1], as eddy currents produce their own magnetic fields to oppose the field that caused them [3]. Hysteresis loss is the other component of core loss.

When the converter switching frequency is increased, skin, proximity and core losses will be increased. If the increase of frequency results in lower inductance needed, this can mean that a smaller inductor could be used. A smaller inductor would have fewer winding turns, hence lower DCR, increased self-capacitance, proximity, and skin effects. There is a balance to be found.

This thesis will compare the Tyndall National Institute thin-film Magnetics-on-Silicon (TF MoS "*MagPwr*" MS2) inductor [4], with commercially available discrete surface-mounted (SMT) inductors, and a baseline low loss air-core inductor.

1.4 Switch Losses

The simplified structure of an n-type metal-oxide-semiconductor field-effect transistor (NMOS) is shown in Figure 1.4(a). For an ideal enhancement mode device, no current will flow between drain and source terminals until the gate voltage, (V_{GS}), exceeds a threshold voltage, V_{th}, when an inversion (n-type) layer is formed under the insulator beneath the gate contact. This layer forms a connection between the drain and source and allows current to flow from drain to source (I_{DS}) with low resistance. The device is a field controlled device and the gate insulator prevents DC current flow through the gate but due to its capacitance, there will be a displacement gate current flows which cause energy losses during device turn on and off.

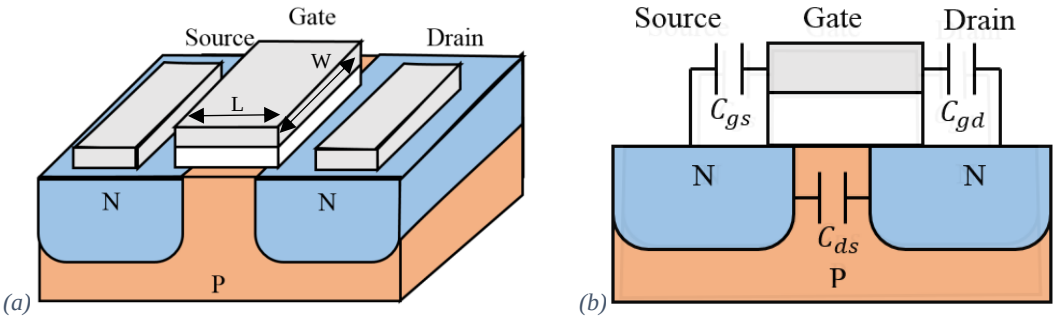


Figure 1.4. (a) Cross-section of an NMOS, (b) with effective capacitances.

A smaller sized switch results in an R_{DS} increase and smaller gate capacitance. Smaller switches (lower width, W) can turn-on and turn-off quicker, hence have lower switching losses, making them more suitable for higher switching frequencies. Ideally when a MOSFET is off, there is unlimited blocking between the drain and source. With sufficient V_{DS} or a small enough gate length, eventually a connection would be made, this is referred to as breakdown. Reducing L reduces the breakdown voltage, so smaller switches typically have lower breakdown voltage.

Another relationship is between the width to length (W/L) ratio of the channel and the on-resistance of the switch (r_{on}). In general, the larger the W/L ratio the smaller the on-resistance (larger drift currents). With a larger W/L ratio there is a larger cross-sectional area or smaller distance to travel. This is shown in the equation for resistance:

$$R = \rho l_{path}/A_{cross} \qquad (1.5)$$

where R is the resistance, ρ is the resistivity, l_{path} is the length to travel, A_{cross} is the cross-sectional area. L is generally fixed according to the voltage rating required for the device.

In Figure 1.4(b), the cross-section of an NMOS with its effective capacitances is shown. There are effective lumped capacitances between: the drain-source (C_{ds}), the gate-source (C_{gs}), and the gate-drain (C_{gd}). At high frequency, these capacitances are significant, due to the capacitance current being proportional to frequency. The small signal input capacitance (C_{iss}), the small signal output capacitance (C_{oss}), and the small signal reverse transfer capacitance (C_{rss}), are defined as:

$$C_{iss} = C_{gd} + C_{gs}, \quad (1.6)$$

$$C_{oss} = C_{gd} + C_{ds}, \quad (1.7)$$

and

$$C_{rss} = C_{gd}. \quad (1.8)$$

These capacitances vary with DC operating point.

There have been some several methods used to adapt and redesign the CMOS such as multi-finger MOSFETs, VDMOS, LDMOS [5-7]. These methods can be reduce the switch size or to reduce switching losses. For example, the multi-finger devices have drain and source regions shared between parallel devices and hence have lower gate-drain and gate-source capacitances.

Dead-times (t_d) are inserted between a Sw_{HS} turning off, and its Sw_{LS} compliment turning on and vice versa. Real switches cannot turn-on or turn-off instantaneously. If there is an overlap where both are on, there is a shorting of the input voltage to ground, with only the switches in the path. This is referred to as shoot-through, which leads to massive losses and possible switch destruction. There are two dead-times the fall dead-time ($t_{d(H-L)}$) and the rise dead-time ($t_{d(L-H)}$). $t_{d(H-L)}$ is defined as the time between the Sw_{HS} turning off and Sw_{LS} turning on. $t_{d(L-H)}$ is defined as the time between Sw_{LS} turning off and Sw_{HS} turning on.

As the inductor cannot have a sudden interruption in current, during the dead-time the inductor current as shown in Figure 1.1(b) flows though the body diode of Sw_{LS}. It can be optimal for a freewheeling diode to be connected in parallel with the switch to improve performance. The diode loss can be broken down into diode conduction (during dead-time) and diode reverse recovery loss (QRR) (3rd quadrant conduction and recovery for GaN switches). These are explored in greater detail in Chapter 2.4.2 on page - 26 -.

There are also gate losses associated with turning on/off the switch and keeping the switch on or off for GaN HEMT which has gate leakage current.

All of the significant switch loss components are examined in this thesis: Sw_{HS} turn-on power loss ($P_{on(HS)}$), Sw_{HS} turn-off power loss ($P_{off(HS)}$), Sw_{HS} QRR power loss ($P_{QRR(HS)}$), Sw_{HS} conduction power loss ($P_{con(HS)}$), Sw_{HS} gate power loss ($P_{gate(HS)}$), Sw_{LS} fall dead-time power loss ($P_{t_{d(H-L)}}$), Sw_{LS} rise dead-time power loss ($P_{t_{d(L-H)}}$), Sw_{LS} conduction power loss ($P_{con(LS)}$), and Sw_{LS} gate power loss ($P_{gate(LS)}$).

2. Literature Review and Background Theory

2.1 Converter Topologies

This section of the literature review investigates traditional switched-inductor based voltage regulators (such as the buck), step-down switched-capacitor (SC) converters, SC-buck hybrid converters, and multi-level flying-capacitor converters. The efficiencies, sizes, and optimal operating conditions of the topologies are discussed.

2.1.1 Buck Converter

Two effective ways of miniaturizing the buck converter are to increase the switching frequency or to use multi-phasing. The benefits and drawbacks of increasing the frequency is discussed in the introduction, this section convers the multi-phasing approach.

In a multi-phase converter, the inductor current is split into N smaller parallel buck converters. The switch-node voltage of each parallel converter is out of phase with the others by 360˚/N, hence each inductor current is out of phase with the others. This reduces the current ripple and allows for a smaller input and output capacitances. The total inductance is typically the same and there may be a separate one for each phase or there may be a coupled arrangement. As the current is split into parallel paths, the heat losses are spread over a larger area, reducing power loss density. One disadvantage is that there are more switches, increasing the total switch size. Another disadvantage is that current balancing requires more advanced control.

One example of the use of both multi-phasing and high frequency in buck design is [8]. The circuit diagram is shown in Figure 2.1. In this example, 16 phases are connected in parallel. In Figure 2.1, the error detector and pulse-width modulator (PWM) are shown in simplified form and the red dashed box is added to highlight the DC-DC converter power path.

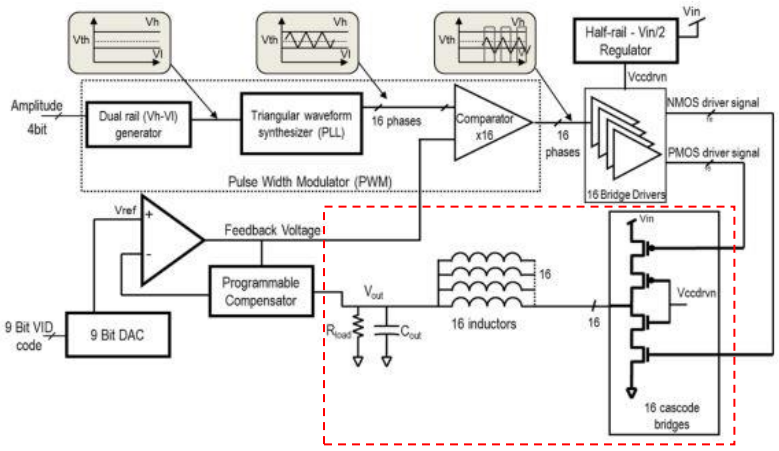


Figure 2.1. Simplified circuit diagram for Intel's FIVR (16-phase buck regulator). Image from [8].

A noteworthy technique to allow advanced CMOS geometry node integration may be seen in Figure 2.1; the switches are arranged in cascode bridges. In an NMOS-PMOS cascode bridge, there are four switches per phase instead of two (one high-side and one low-side). The bridge drivers are controlled through high-voltage level shifters and support soft-switching operations, zero-voltage switching (ZVS) and zero-current switching (ZCS); soft switching can greatly reduce switching losses and hence allow for high efficiency in high switching frequency converters [9]. The gates of the cascode devices are connected to the "half-rail"

(V_{ccdrvn}), which is regulated to $V_{in}/2$. This is the negative supply of the PMOS bridge driver, as well as the positive supply of the NMOS bridge driver. Due to this arrangement, 22 nm logic devices can be used while still handling voltages up to 1.8 V DC (0.9 V per switch). As CMOS technology nodes are scaled successively, while high frequency handling capabilities increase, this also leads to lower voltage handling capabilities.

This converter steps input voltages in the range of 12 V to 20 V down to an output voltage of 1.8 V. The high switching frequency of 140 MHz allows the components to be reduced in size enough to fit into existing unused space on the die. The high switching frequency allows each phase inductor to have a very small inductance value so that it can be realised with air-core alone. There is no magnetic material, which would be too lossy at 140 MHz. The effective current density of the FIVR is 31 A/mm, and an efficiency of up to 90% is achieved. The total I_{out} is in the range of 1 A to 15 A. The measured output voltage ripple is less than 4 mV, comfortably under 1% of the output voltage. This is achieved by using air-core inductors well under 2 mm^2 in area. The measured speed of response of the control is under 30 ns for the majority of the spike, with a total time of 100 ns to return to DC. This allows a peak spike of approximately 50 mV. The turn-on and turn-off time of the FIVR is approximately 0.6 µs.

This design demonstrates the very high level of integration that can occur in a DC-DC converter operating at a very high switching frequency and with multiple phases, it also utilizes cascode bridges and soft switching, these techniques allow for reduction in power losses and component size

2.1.2 Multi-Level Buck Converter

A highly integrated multi-level converter is described in [10]. This paper compares a 2-level buck, a 4-level buck, and a novel modified 4-level buck. The converter is designed using 28 nm fully depleted silicon-on-insulator (FDSOI) 1.5 V CMOS transistors and pulse frequency modulation (PFM) and operates in discontinuous conduction mode (DCM). The converter has a V_{in} range of 2.8 V to 4.2 V, a V_{out} range of 0.6 V to 1.2 V, a P_{out} range of 10 µW to 40 mW, a peak efficiency of 78%, and a maximum f_{sw} of 200 MHz. Its total footprint is 1.5 mm^2, excluding a pair of 5 nF flying capacitors and a 3 nH inductor.

The switches are stacked to distribute the voltage stress. The high-density capacitors in the scaled CMOS process have low voltage ratings (1.4 V for 28 nm) and must be stacked; stacking increases area and decreases power density. SC converters can achieve high efficiency and power densities, but only for fixed voltage ratios.

Multi-level converters enable a wide range of input and output voltages. They achieve higher overall efficiency by merging the benefits of inductive and capacitive converters. The flying capacitors reduce the switch-node voltage swing, thus reducing the voltage across the inductor. This means that the switching frequency may be reduced for the same ripple, to improve overall efficiency. The inductor may be used in a resonant mode to allow soft charge/discharge the capacitors, as another way to improved efficiency and power density.

For a 2-level (standard) buck, at least three stacked 28 nm transistors (1.5 V) would be required to block 4.2 V, shown in Figure 2.2(a) [10]. The 2-level offers no “voltage-breaking” advantage. The large effective series resistance (ESR) results in high conduction losses. A small on-chip inductor requires an increase in switching frequency to 100 MHz, resulting in high switching losses. There is no the frequency multiplication advantage. The switching frequency of a 2-level converter operating in discontinuous conduction mode (DCM) or in boundary conduction mode BCM) is given by:

$$f_{SW-2L} = \frac{2I_{out}V_{in}D(1-D)}{LI_{pk}^2} \quad (2.1)$$

where I_{pk} is the peak inductor current.

For a 4-level buck, the internal nodes between the stacked transistors are exploited by adding flying capacitors. As the switch-node voltage is reduced by a factor of three, the DCM switching frequency is given by:

$$f_{SW-4L} = \begin{cases} \frac{2I_{out}V_{in}D(1/3-D)}{LI_{pk}^2} & 0 < D < \frac{1}{3}\ (mode\ 1); \\ \frac{2I_{out}V_{in}(D-1/3)(2/3-D)}{LI_{pk}^2} & \frac{1}{3} < D < \frac{2}{3}\ (mode\ 2); \\ \frac{2I_{out}V_{in}(D-2/3)(1-D)}{LI_{pk}^2} & \frac{2}{3} < D < 1\ (mode\ 3). \end{cases} \qquad (2.2), (2.3), and (2.4)$$

Figure 2.2(d) shows that the equivalent switching frequency (for any of the three modes) of the 4-level converter is less than 20% of that of the 2-level converter. The figure shows that for the same inductance value, the normalised switching frequency can be reduced by a factor up to 23, and citing a 33% improvement in efficiency. The drain-source voltages of the 4-level converter's switches never exceed $V_{in}/3$. Alternatively the extra levels may be used to reduce the volt-seconds burden on the inductor so that smaller inductance values can be used. Modes 1-3 refer to PWM modes and the order in which the input source and ground is alternatively switched through the various multi-level capacitors.

The diagrams in Figure 2.2(a-c) show the circuit topologies.

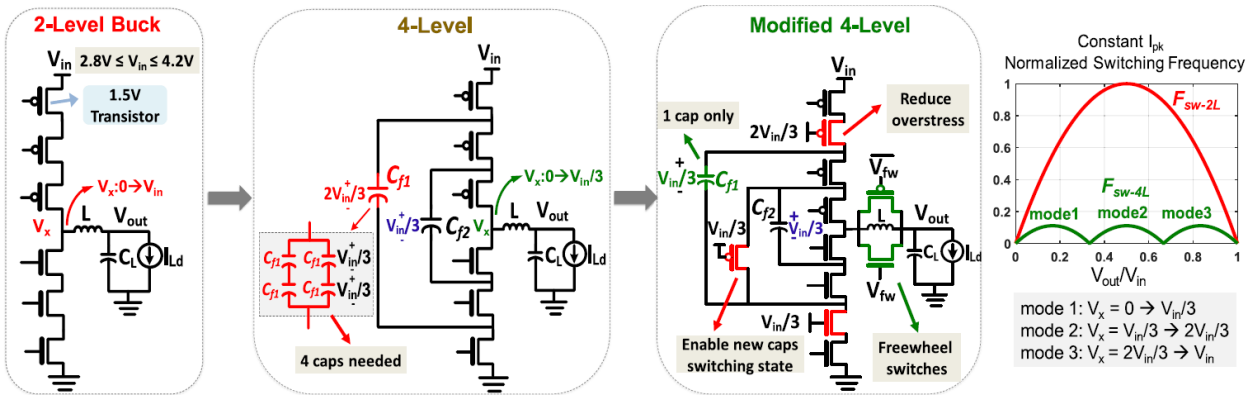


Figure 2.2. Topologies for: (a) the 2-level buck, (b) the 4-level buck, and (c) the modified 4-level buck converter. (d) Normalized switching frequency versus conversion ratio for the 2-level buck and the 4-level buck converter, operating in DCM with constant peak current I_{pk}. From [10].

2.2 High Frequency Magnetics

Paper [11] reviews the impact of inductors in high frequency DC-DC converters. Inductor size in portable applications is examined, specifically the Tyndall micro-fabricated magnetics-on-silicon inductor, which has a relatively large inductance per area, given its high frequency capability. There is also some analysis of the performance of SC-buck hybrid topologies.

Figure 2.3, extracted from [11], clearly shows that smaller inductor values, for a given area, are more efficient. The efficiency of an inductor can be calculated using the losses associated with its operation or from direct measurement. The equation for loss can be approximated by:

$$P_L = r_L * i_{L(rms)}{}^2 \qquad (2.5)$$

where r_L is the ESR of the inductor (representing all AC losses (copper and core) for the inductor) and $i_{L(rms)}$ is the root mean square current through the inductor.

Inductor efficiency is calculated using:

$$Efficiency = \frac{ConverterOutputPower}{ConverterOutputPower + InductorLoss}. \quad (2.6)$$

In the model used, eddy currents, hysteresis, DC, and AC (six harmonics) losses were all included. The result is shown in Figure 2.3. The buck converter is operated at 10 MHz, 20 MHz, 50 MHz, and 100 MHz. Using Equation (1.3) it is clear that inductance is inversely proportional to switching frequency. For each frequency, inductor efficiency is compared to the physical area taken up by the inductor. This work demonstrates how increasing the switching frequency of a buck converter can be utilized to reduce inductor size and loss.

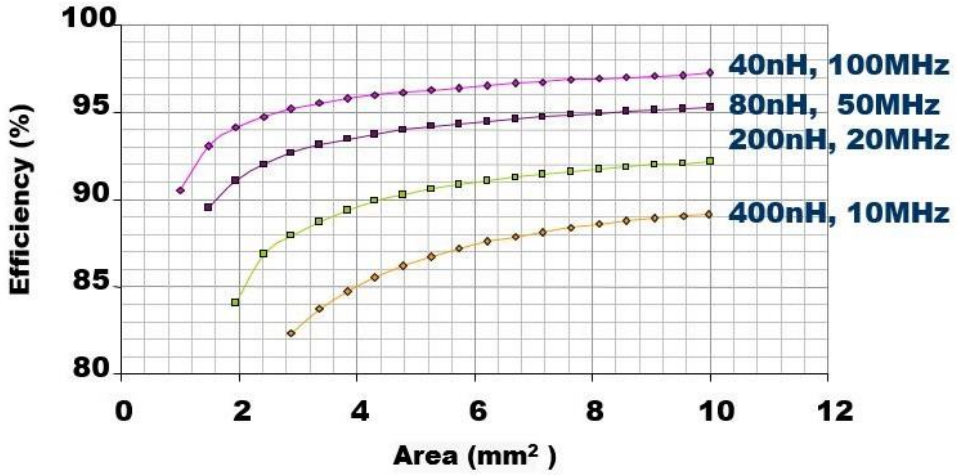


Figure 2.3. Area vs. efficiency for inductors at various frequencies. From [11].

2.3 High Frequency Switch Layout

2.3.1 Multi-Finger MOSFET

The multi-finger MOSFET (MFM) is discussed in this section, including its layout, operation, advantages, and disadvantages. The typical layout of a MOSFET is shown in Figure 2.4(a). By combining the MOSFET in parallel with two identical MOSFETs, as shown in Figure 2.4(b), the width is essentially tripled. This reduces the on-resistance, resulting in lower conduction losses, but increasing equivalent capacitances (C_{gs}, C_{gd} and C_{ds}), which can increase drive and switching losses. The three-finger MOSFET shown in Figure 2.4(c) has the same on-resistance as the device in Figure 2.4(b), as it also has triple the width of the single-finger device. The advantage of the three-finger MOSFET is that the MFM has lower overall C_{gs} and C_{gd} capacitances than the multiple MOSFETs connected in parallel.

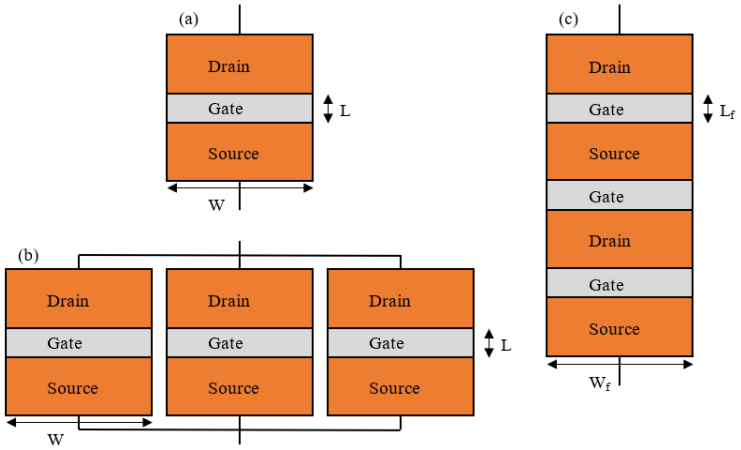


Figure 2.4. Top view of MOSFET configurations: (a) single-finger MOSFET, (b) three single-finger MOSFETs connected in parallel, and (c) three-finger MOSFET.

Figure 2.5 shows the cross-section of a four-finger MOSFET [12]. The four-finger MOSFET shown includes the bulk and shallow trench isolation (STI), and also has lightly doped drains (LDDs). LDDs improve MOSFET reliability at the expense of current drive [13].

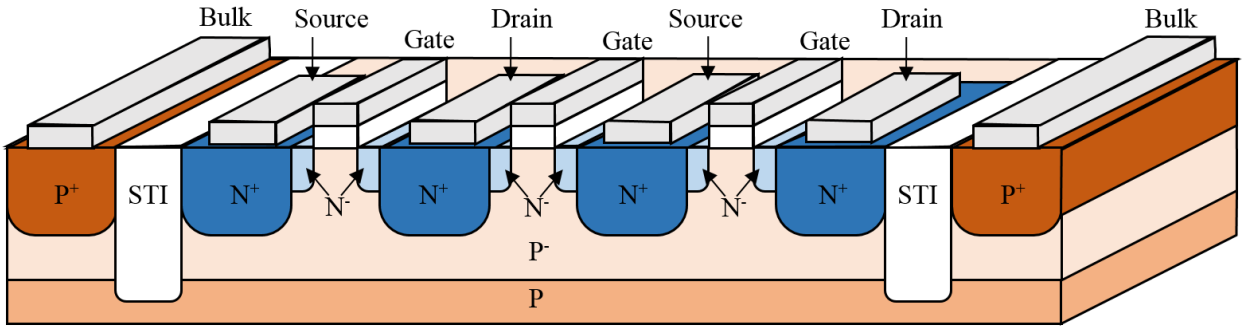


Figure 2.5. Cross-section of a four-finger n-type MOSFET. Based on [12].

As the number of gate fingers (N_f) increases, there is lower drain and source resistance, thus total resistance is reduced, leading to an increase in drain current. As more gates are connected in parallel, gate resistance is also reduced [14]. This reduction is limited, so that eventually, increasing the number of fingers does not significantly change the series parasitic resistance. The equation below gives the relationship between the total width (W_{total}) and N_f and W_f:

$$W_{total} = N_f * W_f. \quad (2.7)$$

In general, the drain-body and source-body capacitances (C_{db} and C_{sb}) decrease with the number of fingers (up to a point). The exception is C_{db} with an even number of fingers, in which case C_{db} gradually increases as the number of fingers increases.

The gate resistance, R_{gate}, is given by:

$$R_{gate} = R_{sch} \frac{W}{3*M*L*N_f^2} \quad (2.8)$$

where R_{sch} is the resistance of poly layer (gate layer) and M is a unitless coefficient. M depends on how the gate is accessed [15]. As R_{gate} is inversely proportional to N_f^2, the resistance is reduced by using the

multi-finger technique. Multi-fingering was used with the CMOS designed in this thesis switches to reduce on-resistance.

2.3.2 Bulk 180 nm NMOS and PMOS

This thesis deals with simulating converters that use multi-finger bulk CMOS switches. Models for the 5 V *ne5* (NMOS) and *pe5* (PMOS) bulk 180 nm CMOS devices of the XP018 series from X-FAB [16] are used. Figure 2.6 shows their cross-section. For the NMOS, there is p+ contact to the body. The body is connected to the n+ source and will form a body diode between source/body and the drain. The polysilicon gate regions are shown over the channels n+ poly for the NMOS and p+ poly for the PMOS.

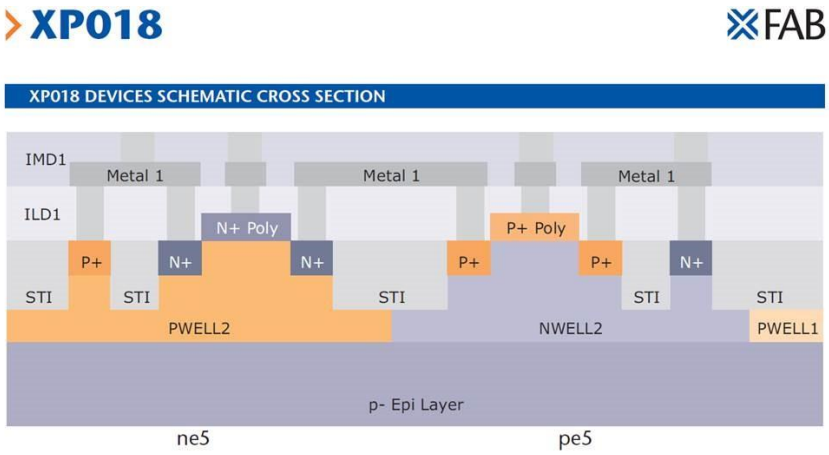


Figure 2.6. Cross-section of a 5 V ne5 and pe5 180 nm CMOS.

2.3.3 Gallium Nitride High-Electron-Mobility Transistors

The converter tested in this thesis uses 15 V EPC2040 [16] enhancement mode GaN switches manufactured by EPC. These 15V devices give somewhat similar performance to the *ne5* and *pe5* 5V CMOS devices designed. This section reviews that switch technology. The operation, advantages and disadvantages of gallium-nitride (GaN) high-electron-mobility transistors (HEMTs) is reviewed, with reference to [17-23].

In terms of material properties, GaN naturally has a wider band gap (3.4 eV) than Si (1.1 eV). This means that it has a higher critical electric field and shorter drift region for the same breakdown voltage (VB). Thus, a GaN transistor can have a much shorter length for the same blocking voltage, resulting in a smaller area. It has extremely low intrinsic carrier concentration, 1.9×10^{-10} cm^{-3} (Si is 1.5×10^{10} cm^{-3}), hence a lower leakage current. It has a piezo-polarization nature, meaning that it can have a high channel concentration without intentional doping, hence high electron mobility. Ga is a group three element and N is group five. When the two elements are combined, the structure has spontaneous polarization. This means that the bonds are polar, and because the structure is non-centrosymmetric, this polarization is intrinsic. GaN can also be grown on Si, making it cheaper than, for example, SiC or diamond.

GaN can form a heterojunction with AlGaN. A heterojunction is when an interface is formed between two different semiconductors with dissimilar bandgaps. In the formation of heterojunctions, it is beneficial to have large differences in bandgaps (AlGaN is 6.2 eV) and to have a small lattice mismatch so that there is no dislocation. The lattice mismatch between GaN and AlGaN causes a strain between the two layers, which produces the piezoelectric polarization. If there is a gradient in polarization, there is an induced positive charge. This charge attracts electrons, which form the two-dimensional electron gas (2DEG) [18]. The electrons are confined in a quantum well. The cross-section of a GaN switch is shown in Figure 2.7.

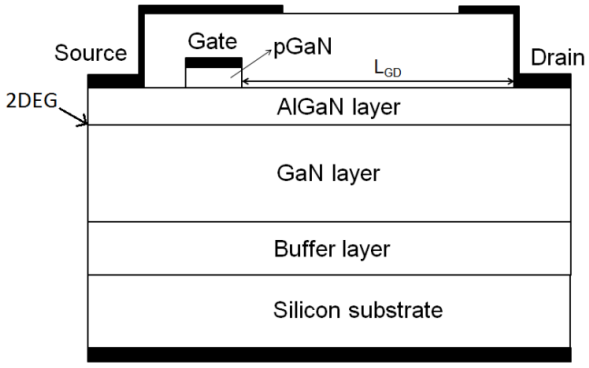


Figure 2.7. Cross-section of a GaN HEMT, E-mode p-GaN gate. Image from [17].

All the drain-source current flows in the 2DEG quantum well. There is a, associated trade-off when designing the AlGaN layer: a thicker AlGaN layer has lower leakage current, but this results in the 2DEG layer having a higher on-resistance. Injection or removal of carriers in the depletion region is not necessary, allowing for very fast switching and resulting in high-electron mobility. Fast switching allows the switch to operate at higher frequencies, so the converter can have smaller passive components. High-electron mobility causes low r_{on}, hence low conduction loss and higher efficiency.

The GaN HEMT has some disadvantages. Two significant ones are potentially limited performance due to blocking mode leakage current, and a current degradation mechanism known as current collapse. Current collapse occurs after high voltage stress: the drain current decreases even under the same gate and drain voltages, effectively increasing the on-resistance. This is also known as dynamic on-resistance.

2.4 High Frequency Switch Losses

2.4.1 Turn-On and Turn-Off Switching Losses

A high frequency switching loss analyses for a 2-level buck converter can be found in [24]. With an ideal switch, turn-on and turn-off would be instantaneous. The switch would go from blocking the full circuit voltage and allowing no current through to passing the full circuit current, with zero voltage drop, in zero time.

2.4.1.1 Turn-On Switching Loss

For this analysis, both switches are assumed to be NMOS. The high-side switch, Sw_{HS}, waveforms during turn-on, I_{DS}, V_{DS}, and V_{GS}, are shown in Figure 2.8. This is a simplified diagram of waveform behaviour. When V_{GS} reaches V_{th}, the inductor current starts to flow through the switch. When the switch is off, the current through it is zero. Before turn on, due to the mechanisms of the channel formation, it takes time before it can fully conduct $I_{DS(on)}$. Before the switch turns on, the inductor current is at its minimum, and thus $I_{DS(on)} = I_{L(min)} = I_{out} - \Delta I_{out}/2$. During I_{DS} rise interval, V_{DS} remains at its off-value ($V_{DS(off)}$), which is equal to V_{in}. Only after I_{DS} reaches $I_{L(min)}$ does V_{DS} start to drop. C_{oss} is then discharged until the switch voltage reaches its on-value ($V_{DS(on)} = r_{on} I_{DS(on)}$). The switches for this thesis are chosen to have very low r_{on} so that $V_{DS(on)}$ is negligible. Thus, for a short amount of time, the switch has both a high voltage and a current flowing through it to give the turn-on switching loss:

$$P_{sw(on)} = V_{in} f_{sw} I_{L(min)} t_r / 2 \qquad (2.9)$$

where t_r is the time from when I_{DS} starts to rise to when V_{DS} has completed its fall (to $V_{DS(on)}$).

An important consideration is the Miller plateau, also known as the gate-drain charge period. Approximately all the charge applied to the gate during this period charges the gate-drain capacitance (Q_{GD}), so that V_{GS} does not change. The voltage at which this occurs is referred to as the plateau voltage V_{PL}. During the time V_{GS} rises to V_{th}, the gate charge increases by Q_{GS1}. During the time that V_{GS} rises from V_{th} to V_{PL}, the increase in gate charge is Q_{GS2}, and I_{DS} rises from 0 A to I_L. The switch turn-on charge (Q_{sw}) is the sum of Q_{GS2} and Q_{GD}.

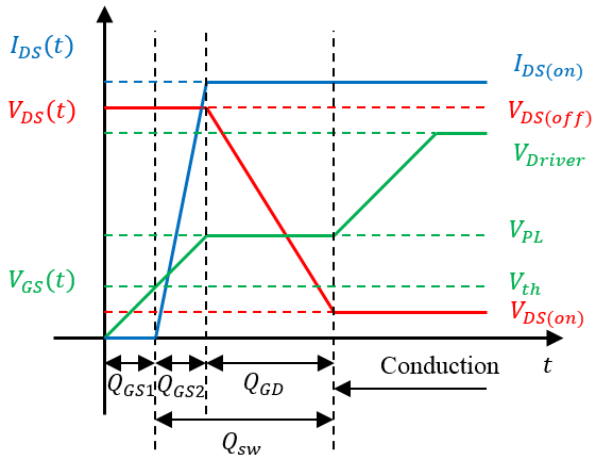


Figure 2.8. Example of the high-side switch waveforms during turn-on with Miller plateau.

Equation 2.10) is an improved version of Equation (2.9), where the rise time is defined as the charge at the gate required to turn-on the switch (Q_{sw}) divided by the gate current (I_g):

$$P_{sw(on)} = V_{in} f_{sw} I_{L(min)} Q_{sw} / 2 I_g. \qquad (2.10)$$

The gate current is defined by Ohm's law:

$$I_g = (V_{Driver} - V_{PL}) / (R_g + R_{Driver}). \qquad (2.11)$$

The voltage at the gate (V_g) is the difference between the driver voltage (V_{Driver}) and V_{GS} (which is equal to V_{PL}). The resistance between the driver and the gate is the sum of the gate resistance (R_g) and the driver resistance (R_{Driver}).

Another important consideration, especially at high frequency, is the common source inductance (L_{CSI}). In reality, due to device package interconnects and PCB traces, there will be an inductance between the switch's source and its driver reference, as shown in Figure 2.9. This inductance will slow down both turn-on and turn-off, and hence increase the switching losses.

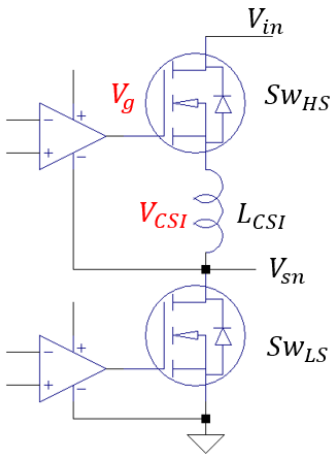


Figure 2.9. Switches with common source inductance (shown for high-side switch only).

As I_{DS} increases, this generates a voltage across L_{CSI}. This means that the effective V_{GS} now becomes:

$$V_{gs(eff)} = V_g - L_{csi}\frac{dI_{DS}}{dt} - V_{sn}\ . \qquad (2.12)$$

The following equation for Sw_{HS} switching loss accounts for the Miller plateau and the common source inductance:

$$P_{sw(on(HS))} = V_{in}f_{sw}(I_{out} - \Delta I_{out}/2)\left(\frac{Q_{gs2(HS)}}{2I_{g1(on)}} + \frac{Q_{gd(HS)}}{2I_{g2(on)}}\right). \qquad (2.13)$$

The gate current equations for the two parts of the turn-on are defined by the following equations:

$$I_{g2(on)} = \frac{V_{Driver} - V_{PL(HS)}}{R_{g(HS)} + R_{Driver} + L_{csi}\left(\frac{I_{out} - \Delta I_{out}/2}{dt1}\right)}, \qquad (2.14)$$

and

$$I_{g2(on)} = \frac{-b + \sqrt{b^2 - 4ac}}{2a}, \qquad (2.15)$$

where $dt1$ refers to Q_{GS2} interval. The values a, b, and c are:

$$a = \frac{L_{csi}Q_{oss(LS)}}{Q_{gd(HS)}^2}, \qquad (2.16)$$

$$b = \left(R_{g(HS)} + R_{Driver}\right), \qquad (2.17)$$

and

$$c = -\left(V_{Driver} - V_{PL(HS)}\right). \qquad (2.18)$$

2.4.1.2 Turn-Off Switching Loss

The mechanism of switch turn-off is essentially the reverse of the turn-on. The waveforms are shown in Figure 2.10. Before the switch turns off, it is fully conducting the inductor current, which is at its maximum, $I_{DS(on)} = I_{L(max)} = I_{out} + \Delta I_{out}/2$, and $V_{DS} = V_{DS(on)}$, again regarded as negligible. Once V_{GS} drops from V_{Driver} to V_{PL}, I_{DS} remains high and V_{DS} starts to rise. When C_{GD} is finally discharged, I_{DS} finally

starts to drop, V_{GS} begins to drop from the Miller plateau, and V_{DS} has reached its peak. I_{DS} does not reach zero until V_{GS} drops below V_{th}.

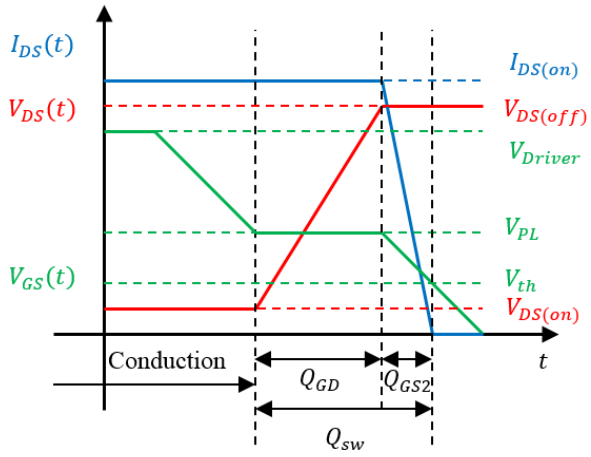


Figure 2.10. Example of the high-side switch waveforms during turn-off with Miller plateau.

The equation for Sw_{HS} turn-off loss with Miller plateau is:

$$P_{sw(off(HS))} = V_{in} f_{sw} (I_{out} + \Delta I_{out}/2) \left(\frac{Q_{gs2(HS)}}{2I_{g1(off)}} + \frac{Q_{gd(HS)}}{2I_{g2(off)}} \right). \quad (2.19)$$

The gate current equations for the two sections of the turn-off are defined by the following equations:

$$I_{g1(off)} = \frac{V_{PL(HS)}}{R_{g(HS)} + R_{Driver} + L_{csi} \left(\frac{I_{out} + \Delta I_{out}/2}{Q_{gs2(HS)}} \right)} \quad (2.20)$$

and

$$I_{g2(off)} = \frac{-b + \sqrt{b^2 - 4ac}}{2a}, \quad (2.21)$$

where a, b, and c are defined as:

$$a = \frac{L_{csi} Q_{oss(LS)}}{Q_{gd(HS)}^2}, \quad (2.22)$$

$$b = \left(R_{g(HS)} + R_{Driver} \right), \quad (2.23)$$

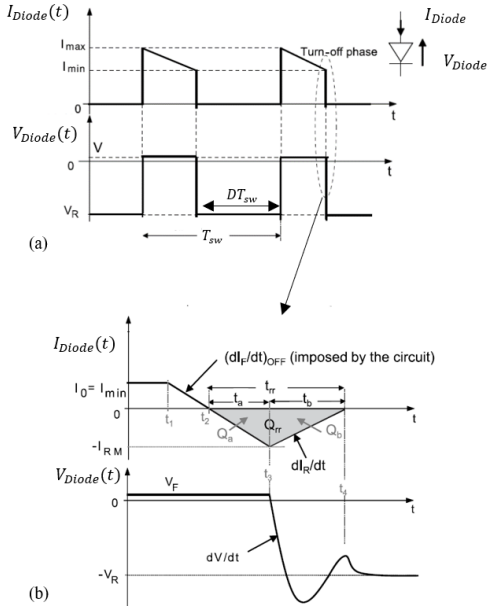
and

$$c = -V_{PL(HS)}. \quad (2.24)$$

2.4.2 Diode Reverse Recovery Loss

This thesis uses the theory from [25] to explore MOSFET body diode recovery loss, as this thesis is investigating the buck converter with both CMOS devices and GaN switches. The topology used in [25] is a diode-based buck converter, meaning that instead of a low-side synchronous switch there is a diode that conducts when the high-side switch is off. This thesis does not assume diode based buck converters, as the forward voltage of a diode would be comparable to the output voltage, but the analysis of the diode recovery

loss is useful regardless, because we may have some body-diode conduction loss. Figure 2.11 shows the diode current and voltage waveforms for (a) a full period, and (b) a close-up of the diode turn-off.



f_{sw} : Switching frequency

T_{sw} : Switching period

D : Duty Cycle

I_{max} : Maximum forward current

I_{min} : Minimum forward current

I_{RM} : Maximum reverse current

V_F : Forward voltage

V_R : Reverse voltage

I_{Diode} : Diode Current

V_{Diode} : Diode Voltage

$t_0 = t_2 - t_1$

$t_a = t_3 - t_2$

$t_b = t_4 - t_3$

Figure 2.11. Asynchronous buck converter's diode current and voltage waveforms for (a) a full period, and (b) a close up of the diode turn-off. Image from [25].

At time t_1, the diode starts to turn off. The current decreases with a slope of dI_F/dt, which is determined by the circuit. The diode voltage remains at the forward voltage (neglecting parasitic inductor effect).

At time t_2, the diode current reaches zero. The excess injected charges stored during the conduction phase begin to recombine. The diode voltage remains at the forward voltage.

At time t_3, the diode current reaches I_{RM}. The diode voltage starts to decrease as the minority carriers are evacuating. The current increases to zero at a rate of dI_R/dt, which is dependent on the diode technology and the circuit. The voltage drops and oscillates around the reverse voltage before stabilizing.

At time t_4, the diode can be considered completely off.

The total change in charge in the diode during the reverse recovery (Q_{rr}) can be broken down into the two regions Q_a and Q_b. The change in charge Q_a occurs between t_2 and t_3, and Q_b occurs between t_3 and t_4. The relationship between charge and current in the diode is thus:

$$Q_{rr} = Q_a + Q_b = \int_{t_2}^{t_3} I_{Diode}(t)dt + \int_{t_3}^{t_4} I_{Diode}(t)dt. \quad (2.25)$$

The time periods relating to these three charge values are:

$$t_{rr} = t_a + t_b. \quad (2.26)$$

The ratio between the two regions of time is referred to the softness factor S:

$$S = t_b/t_a = \frac{dI_F/dt}{dI_{RM}/dt}. \quad (2.27)$$

Using the following relationships:

$$t_a = \frac{I_{RM}}{dI_F/dt}, \quad (2.28)$$

and

$$t_b = S * t_a \, . \quad (2.29)$$

Equation (2.27) can be rearranged to:

$$t_{rr} = \frac{I_{RM}}{dI_F/dt}\,(1+s). \quad (2.30)$$

The energy lost due to the charge Q_{rr} is the diode reverse recovery loss.

2.4.3 MOSFET Conduction Losses

The conduction loss in a switch is calculated by multiplying the on-resistance by the square of the RMS current [24]. The typical current waveforms for the inductor, the high-side switch, and the low-side switch are shown in Figure 2.12, for the synchronous buck converter. The turn-on time, turn-off time and dead-times are not included in this image.

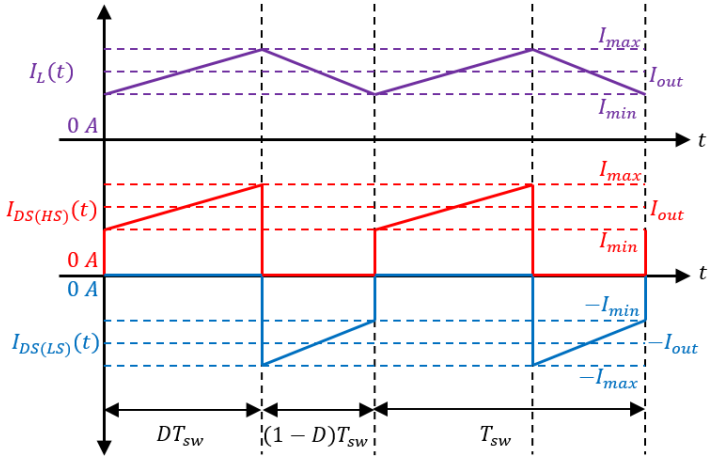


Figure 2.12. Synchronous buck converter current waveforms for the inductor, the high-side switch, and the low-side switch [24].

As noted in the introduction, transistors do not have resistances in the same way that metals do. An effective on-resistance ($R_{DS(on)}$) can be calculated using $V_{DS(on)}$ and $I_{DS(on)}$ or based on the transistor's W/L ratio. The RMS current (R_{rms}) can be approximated using trapezoidal RMS of the current waveform. Thus, the conduction loss is:

$$P_{con} = R_{DS(on)} I_{rms}^2 \quad . \quad [24](2.31)$$

The high-side switch and low-side switch conductions losses are:

$$P_{con(HS)} = r_{on(HS)} D(I_{out}^2 + \Delta I_{out}^2/12) \quad [24]\ (2.32)$$

and

$$P_{con(LS)} = r_{on(LS)}(1-D)(I_{out}^2 + \Delta I_{out}^2/12). \quad [24](2.33)$$

2.4.4 Dead-time Losses

Dead-time is added between the converter's gate drives to prevent the input being shorted to ground through the switches. For a small amount of time, both switches are off, but as the inductor must have a continuous current, complete disconnection is not possible. When both switches are off, the inductor can pull current through ground via the low-side switch body diode. The inductor and diode current waveforms are shown in Figure 2.13, along with the high-side and low-side gate-source voltage waveforms.

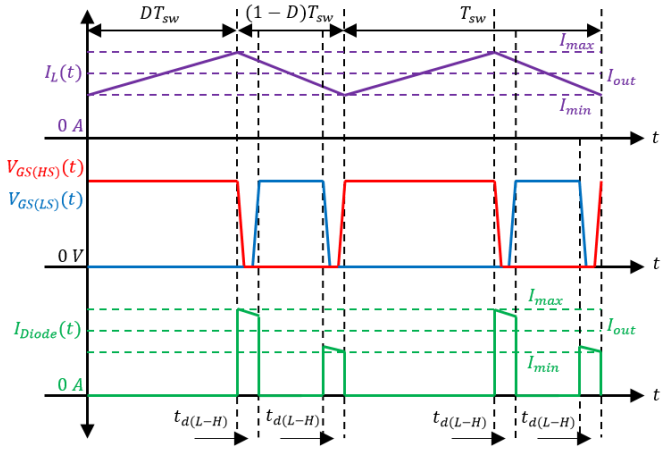


Figure 2.13. Synchronous buck converter waveforms, inductor current, high-side gate-source voltage, low-side gate-source voltage, and diode current [24].

The body diode loss is calculated by multiplying the voltage across the diode by the current through it during the time it is on [24]. The voltage across the diode is oriented in the opposite direction to the switch, thus it is equal to $V_{SD(LS)}$. The time between Sw_{LS} turn-off and Sw_{HS} turn-on is referred to the rise dead-time ($t_{d(L-H)}$). The time between Sw_{HS} turn-off and Sw_{LS} turn-on is referred to as the fall dead-time ($t_{d(H-L)}$). The current for the rise dead-time can be approximated as the minimum inductor current ($I_{out} - \Delta I_{out}/2$) and for the fall time as the maximum inductor current ($I_{out} + \Delta I_{out}/2$). The dead-time loss equation is:

$$P_{t_d} = V_{SD(LS)}\left[(I_{out} - \Delta I_{out}/2)t_{d(H-L)} + (I_{out} + \Delta I_{out}/2)t_{d(L-H)}\right]f_{sw}. \qquad [24](2.34)$$

2.4.5 Gate Driving Losses

The gate losses are calculated as the product of the total charge in the gate (Q_g) during one period multiplied by the driver voltage (V_{Driver}) and the switching frequency:

$$P_{gate} = P_{gate(HS)} + P_{gate(LS)} = \left(Q_{g(HS)} + Q_{g(LS)}\right)V_{Driver}f_{sw}. \qquad [24](2.35)$$

3. Simulations for 2 and 3-Level Buck Converters

This section details how LTSpice and MATLAB are used to simulate the converter topologies to compute the losses, under different conditions. The lumped circuit models for the drivers and inductors are included. Simulation models for the *ne5* (5 V NMOS switch in 180 nm bulk process) and EPC2040 switches are also included.

3.1 LTSpice and MATLAB

LTSpice, Linear Technology's version of SPICE, is a widely used circuit simulator, with a broad variety of applications. In this thesis, LTSpice is used to perform transient analyses of the converters. MATLAB code is written to invoke batch sets of simulations in LTSpice, allowing the simulation and component parameter variables to be defined in MATLAB. In LTSpice it is possible to define measurement commands for example finding the average, peak-to-peak, or RMS value of a waveform, this is a quick and convenient method to extract higher-level data from the simulations. MATLAB code is written to extract these measurements from each simulation as well as all the current and voltage waveforms, to perform analyses.

The first step for preparing the simulations is to create the LTSpice netlist for the two and three level converter schematics.. Parameters and variables are given unique variable names, for example ValVin (input voltage), ValL (inductance), and ValC (capacitance). The MATLAB code finds these placeholders and overwrites them with the desired values, this allows for all the values in the LTSpice file to be defined by the MATLAB code. The simulation data is in ASCII configuration as opposed to the default binary, to enable MATLAB to extract it. The waveforms are extracted from LTSpice using the function LTSPICE2MATLAB written by Paul Wagner [26].

A full cycle loss breakdown obtained from LTSpice, using the measurement command is used for the power loss. LTSpice is directed to return the value of the numeric integration of the product of the voltage across and current through a component, for the duration a switching period. The waveforms for the switches are extracted from LTSpice, the MATLAB code finds key timing points to further break down the losses, into sub-cycle switching intervals such as for turn-on loss.

Cadence PDK *ne5* (180 nm CMOS process design kit) Spectre models are converted into LTSpice format models. The conversion process was pre-validated, by switching simulations performed on extracted LTSpice MOSFET models of a specific width, W, in LTSpice and then in Cadence and ensuring match up.

3.2 Drivers and Bootstrap Capacitors Models

The bootstrap capacitor, maintains a steady supply voltage for a "flying" high-side driver, where its ground reference is switching, shown in Figure 3.1. The high-side driver ground reference node is marked with a red circle for clarity. The bootstrap capacitor (C_{Boot}) is set to 100 nF.

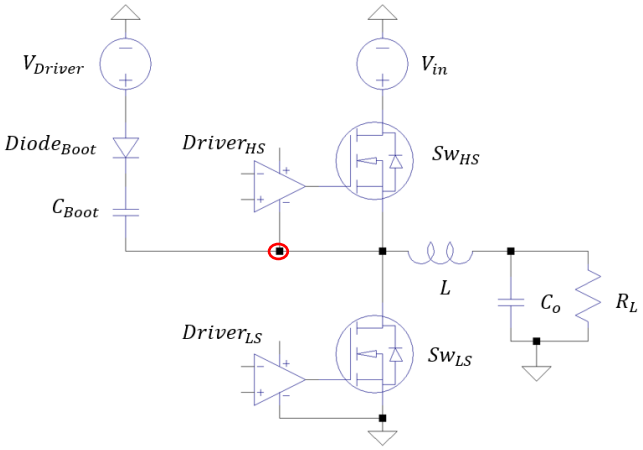


Figure 3.1. Simplified 2-level buck converter, with drivers and bootstrap diode and capacitor.

This arrangement is modified for the 3-level buck. A solution is to connect each of the three drivers, which are not referencing ground, to its own driver voltage as in Figure 3.1. The paper [28] proposes a novel strategy for multi-level bootstrapping. The paper reports a higher efficiency and power density, by using a cascaded bootstrap technique. The simplified version of this configuration is employed in this thesis as shown in Figure 3.2.

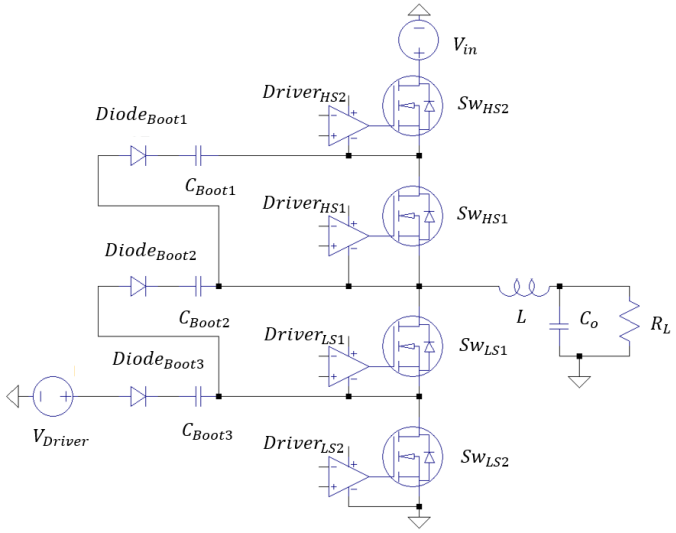


Figure 3.2. Simplified 3-level buck converter, with drivers and cascaded bootstrap diodes and capacitors.

For the bootstrap diode ($Diode_{Boot}$) the BAT46WH [27] is selected, with a lumped equivalent circuit model shown in Figure 3.3. Examining the data sheet it is determined that the forward voltage (V_F) is 0.175 V, the diode parallel capacitance (C_{Diode}) is 0.21 pF and the diode series resistance (R_{Diode}) is 5 Ω. The ideal diode ($Diode_{ideal1}$) is modelled to have a 0 Ω on-resistance, a 1 MΩ off-resistance, a 100 V reverse breakdown voltage, and includes the forward voltage.

For the drivers, the Peregrine Semiconductor PE29102 [29] is selected. The created lumped equivalent circuit model is shown in Figure 3.3. It has a pull-up resistance (R_{PU}) is 1.9 Ω and the pull-down resistance (R_{PD}) is 1.3 Ω. Ideal diodes were connected in series with these resistances to ensure that only pull-up is conducting when the driver is high, and only the pull down is conducting when the driver is low. The ideal

diode ($Diode_{ideal2}$) is modelled to have a forward voltage of 0 V, a 0 Ω on-resistance, a 1 MΩ off-resistance, and a 100 V reverse breakdown voltage. The pulse generators are set to have a 0.6 ns rise and fall time as per the PE29102 datasheet.

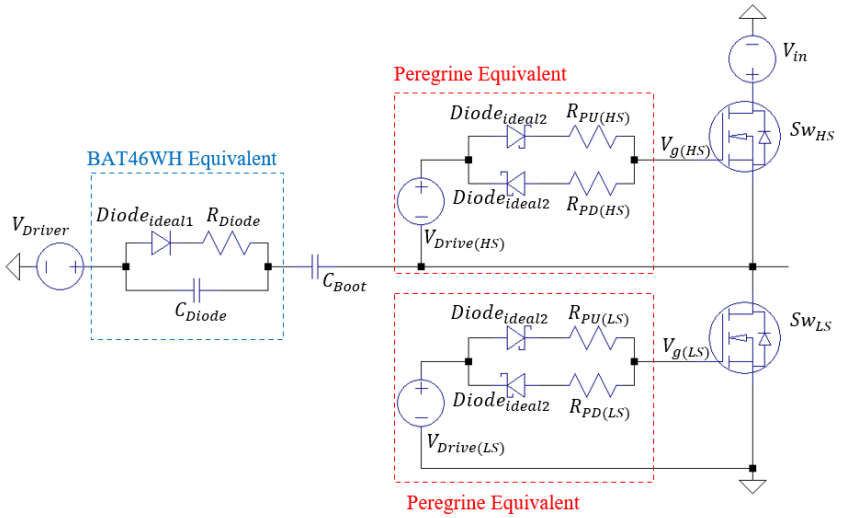


Figure 3.3. Lumped circuit models for bootstrap capacitor, its BAT46WH diode, and Peregrine drivers.

It is acknowledged here that AC bootstrap charge/discharge energies only are being modelled in the circuit shown above.

3.3 Output Capacitor Model

The circuit board uses two capacitors connected in parallel for the output capacitor. The capacitor used is the Taiyo Yuden low ESL 0306 AWK107C6475MV-T capacitor [30]. It has a capacitance of 4.7 µF, an ESL of 200 pH, and an ESR of 3 mΩ, at its self-resonance-frequency of 5 MHz, as shown in Figure 3.4. Thus, for two capacitors connected in parallel the capacitance is 9.4 µF, an ESL of 100 pH, and an ESR of 1.5 mΩ.

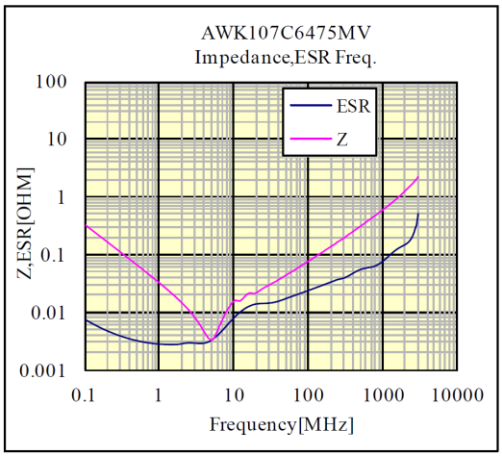


Figure 3.4. Impedance vs. Frequency for AWK107C6475MV capacitor.

3.4 Inductor Models

3.4.1 Introduction

This section examines the output inductor, it is theory, measurements, and how it is modelled in simulation. This thesis uses Tyndall National Institute's thin-film inductor in the power converters and discrete surface-mounted (SMT) chip inductors were also used for comparison. Discrete SMT inductors with similar inductance values are selected for a good comparison, the desired characteristics are shown in Table 3.1. The converter is operated in the range of 20 – 40 MHz. For the 3-level converter this means an effective inductor frequency up to 80 MHz, so that the inductance is required to hold to approximately 100 MHz.

Property	Value
Inductance	Approximately 50 nH
Direct-Current Resistance (DCR)	Less than 100 mΩ
Footprint	2 mm by 2 mm
Operating Frequency	Up to 100 MHz
Saturation Current	Approximately 1 A

Table 3.1 Desired specifications for discrete surface-mounted inductors.

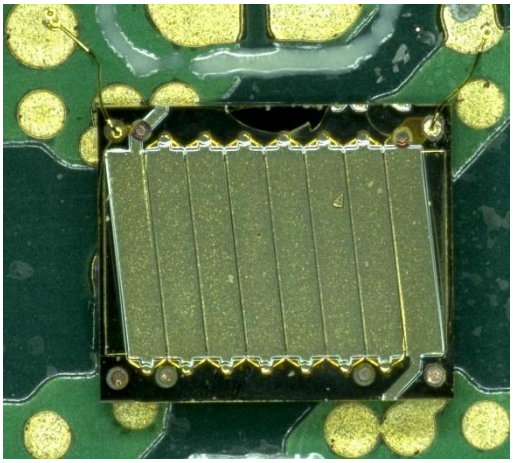


Figure 3.5. Tyndall's "MagPwr" thin-film inductor.

3.4.2 Commercial Surface-Mounted Chip Inductors Considered

To select the discrete SMT inductors by datasheet review, the following companies' catalogues are examined: Coilcraft, Bourns, Murata, and TDK. The properties of the shortlisted inductors are shown in Table 3.2.

In general inductors with larger area have smaller the DCR. The SLC Coilcraft series have the lowest DCR values, less than 0.21 mΩ. These are significantly lower than others considered, but they have the largest areas, over 50 mm^2. The smaller the sized inductors tend to have much larger DCR values, for example the LQG series from Murata have an approximate area of 0.5 mm^2 and DCR above 700 mΩ. The Murata LQW series are an exception to this, one of which has an area of 0.6 mm^2 and a DCR of only 60 mΩ. Wirewound chip inductors tend to have lower DCR than ones with plated conductors.

In general inductors with larger inductance have higher DCR, for given case size. The TDK inductors have inductance values (47 - 56 nH) close to the desired value but their DCR values are 100 mΩ or larger. The Bourns SRN series inductors have larger inductance values (220 - 470 nH) and have DCR values less than 100 mΩ, going as low as 7 mΩ.

Inductor Type	Inductance	Test fsw	Area	Height	DCR	Frequency L Changes	ISAT
	(nH)	(MHz)	(mm^2)	(mm)	(mΩ)	(MHz)	(A)
Coilcraft							
PFL1005	60	7.9	1.14x0.635	0.71	42	~100	1.3
PFL1609	470	7.9	2	<1	83	~100	0.76
PFL2010	470	7.9	3.2	1	60	~100	1.2
PFL2015	560	7.9			60	~100	1.3
SLC7530	50	0.1	7.5x6.7	3	0.123	<20	50
	50	0.1	7.5x6.7	3	0.209	<20	50
SLC7649	50	0.1	60		0.17	~50	84
XEL3515	71	1	3.5x1.5	1.5	2.85	~80	7
XFL2005	150	1	2x2	0.5	85	~100	0.6
XEL3520	70	1	3.2x3.5	2	2.45	~200	9.7
Bourns							
CW161009A-51NJ	51		1.65x1.15		240		0.6
CW105550A-51NJ	51		1x0.55		820		0.21
SRN2010TA	470	1	2x1.6	1	44		2.7
SRN2508A	470		2.5x2	0.8	80		2.5
SRP2510A	220	1	2.5x2	1	9		5.9
SRP2512	470	1	2.5x2	1.2	25		5.3
SRP4020	220		4x4	2	7		7
muRata							
LQG15HH47NG02#	47	100	1x0.5		720	~500	0.3
LQG15WH47NG02#	47	100	1x0.6		1600	~1000	0.19
LQW15CN48NJ00#	48	100	1x0.55	0.5	78	~400	1.1
LQW15CN53NJ10#	53	100	1x0.6	0.5	60	~300	1.3
LQW18CN55NJ00#	55	10	1.6x0.8	0.8	45	~300	1.5
TDK							
SIMID 0805-F	47	200	2x1.25	1.4	130		0.6
	56	200	2x1.25	1.4	140		0.6
MLF1608	47	50	1.6x0.8	0.95	200	~100	0.2
MLF2012	47	50	2x1.25	0.85	100	~100	0.3

Table 3.2. SMT inductors investigated by datasheet review .

3.4.3 Candidate Inductors

The inductors from Table 3.2, were short-listed to the candidate inductors shown in Table 3.3.

Inductor Type	Inductance (nH)	Test fsw (MHz)	Area (mm^2)	Height (mm)	DCR (mΩ)	ISAT (A)
PFL1005 [31]	60	7.9	1.14x0.635	0.71	42	1.3
LQW15CN55NJ00# [32]	55	10	1.6x0.8	0.5	78	1.1
MLF2012 [37]	47	50	2x1.25	0.85	100	0.3
SIMID 0805-F [36]	47	200	2x1.25	1.4	130	0.6
CW161009A-51NJ [34]	51		1.65x1.15		240	0.6
XFL2005 [33]	150	1	2x2	0.5	85	0.6
SRP2510A [35]	220	1	2.5x2	1	9	5.9

Table 3.3. The information on the candidate inductors.

Additional properties of the inductors are listed below. A shielded inductor contains most of the magnetic field within the inductor. As a shielded inductor emits low magnetic field outside of its package, there is lower coupling and fewer adverse effects on the rest of the circuit. It may therefore have a higher overall power efficiency. An important figure of merit (FOM) for an inductor is the DCR per unit inductance. A FOM can be used to quickly compare the DCR and inductance of various inductors.

PFL1005, has magnetic shielding and is a composite. FOM = 0.7 mΩ/nH.
LQW18CN55NJ00#, is unshielded and wirewound. FOM = 0.818 mΩ/nH.
MLF2012, is a monolithic multilayer. FOM = 2.128 mΩ/nH.
SIMID 0805-F, is ceramic and ferrite, and an open wound solenoid. FOM = 2.766 mΩ/nH.
CW161009A-51NJ, is unshielded and is ceramic. FOM = 0=4.706 mΩ/nH.
XFL2005, has magnetic shielding and is a composite. FOM = 0.567 mΩ/nH.
SRP2510A, is wirewound, shielded, and a metal alloy powder. FOM = 0.0409 mΩ/nH.

The two inductors selected for simulation and measurement are the PFL1005 and the LQW15CN55NJ00#. Of the inductors with inductance values close to the desired 50 nH, these two had the best FOMs, and smallest inductor areas.

3.4.4 Coilcraft Inductor Model

Coilcraft provides a lumped circuit model for their inductors, for use in LTSpice as shown in Figure 3.6. The lumped circuit model has six components:

R_1- A resistor in series with the self-capacitance, used to limit impedance resonance.
R_2- A resistor to model the DC loss.
R_{VAR1}- A variable series resistor to model skin and proximity effects.
R_{VAR2} – A variable series resistor to model the frequency dependent Core Loss.
C - The self-capacitance connected in parallel to the inductor.
L_{VAR}- The frequency dependent inductance.

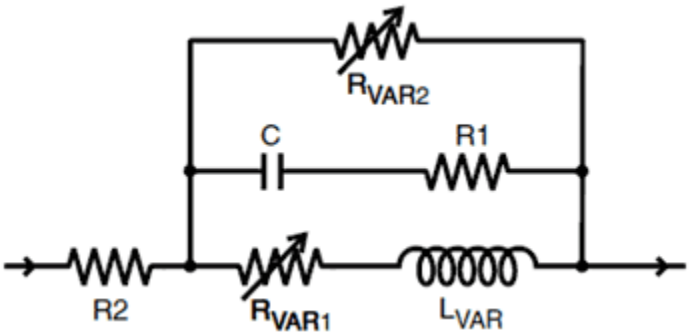


Figure 3.6. The LTSpice inductor model for the PFL1005. From Coilcraft.

The PFL1005 series is model is valid between 0.1 MHz to 100 MHz.

The variable components are modelled as follows:

$$R_{VAR1} = k1 * \sqrt{f}, \quad (3.1)$$

$$R_{VAR2} = k2 * \sqrt{f}, \quad (3.2)$$

and

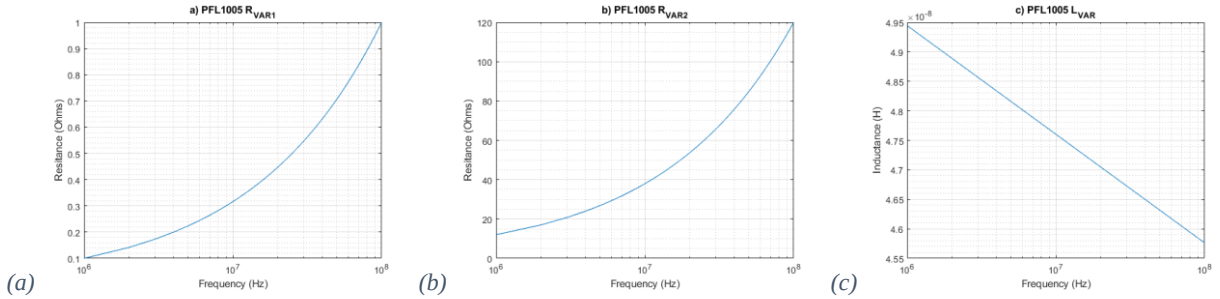
$$L_{VAR} = (k3 - k4 * \ln(k5 * f)) * 1e - 6 \quad (3.3)$$

where the k values are the measured coefficients for each inductor in the frequency range. The constant values for the two models are shown in Table 3.4.

Part #	R_1 (Ω)	R_2 (Ω)	C (pF)	k1	k2	k3	k4	k5
PFL1005-36N	200	0.034	0.05	1.00E-04	0.012	0.012	8.00E-04	2.00E-06

Table 3.4. Component values for PFL inductor. From Coilcraft.

The variable component values are compared with logarithmic frequency in Figure 3.7 for the PFL1005-36N. The three component values shown are (a) R_{VAR1}, (b) R_{VAR1}, and (c) L_{VAR}. The frequency range is from 1 MHz to 100 MHz. The resistances are proportional to the square root of the frequency. The inductance ramps down logarithmically against frequency, it starts at 49.5 nH at 1 MHz and goes to 45.8 nH at 100 MHz



(a) *(b)* *(c)*

Figure 3.7. The variable component values for the PFL1005-36N and logarithmic frequency (a) RVAR1, (b) RVAR2, and (c) LVAR.

3.4.5 Bourns Inductor Model

Various manufacturer model formats are examined to assess a good option for modelling the Tyndall inductor. The model provided by Bourns for the SRP2510A-R22M is shown in Figure 3.8. The frequency dependent core loss $R_p = 413\ \Omega$, the inductance $L = 220$ nH, the skin, proximity and DCR losses are combined in $R_{ser} = 0.009\ \Omega$, and the self-capacitance is $C_p = 6.753$ pF.

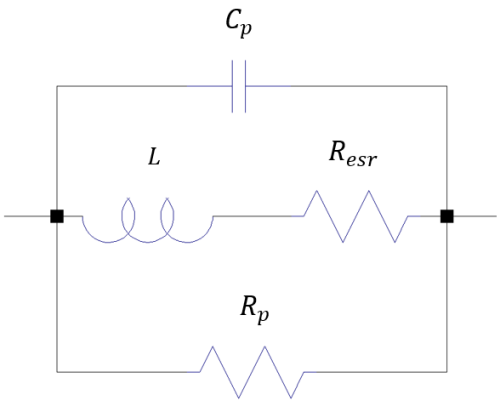


Figure 3.8. LTSpice model for SRP2510A-R22M inductor. From Bourns.

3.4.6 Murata Inductor Model

For the LQW18CN55NJ00# inductor, Murata provides a LTSpice netlist which is interpreted in the circuit diagram shown in Figure 3.9. The self-capacitance $C_1 = 36.2$ fF, the skin, proximity and DCR losses are modelled by $R_2 = 0261\ \Omega$, the inductance of the inductor $L_2 = 54.1$ nH, $R_4 = 267\ \Omega$ is the core loss , and the inductance $L_4 = 1.06$ µH is used to make R_4 frequency dependent.

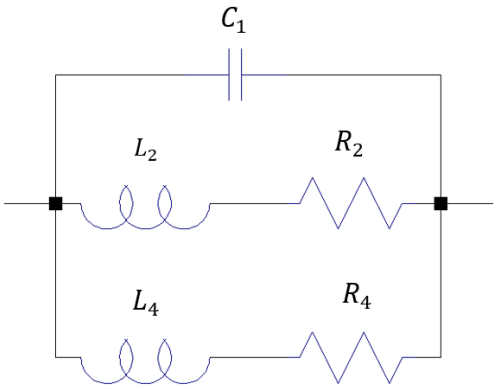


Figure 3.9. LQW18CN55NJ00# equivalent circuit diagram. From Murata.

3.4.7 TDK Inductor Model

The TDK SIMID 0805-F inductor model is added directly into the LTSpice library as a single component and not a sub-circuit which makes separating the various inductor loss components more difficult. The 47 nH version has the code B82498B3560J000.

The MLF2012 inductor series' equivalent circuit is shown in Figure 3.10, for the MLF2012D47NMT000 (the 47 nH version) the inductance $L_1 = 47$ nH, the resistance $R_1 = 230\ \Omega$ to model core loss, the self-capacitance $C_1 = 1.1$ pF, and the DCR $R_2 = 0.05\ \Omega$.

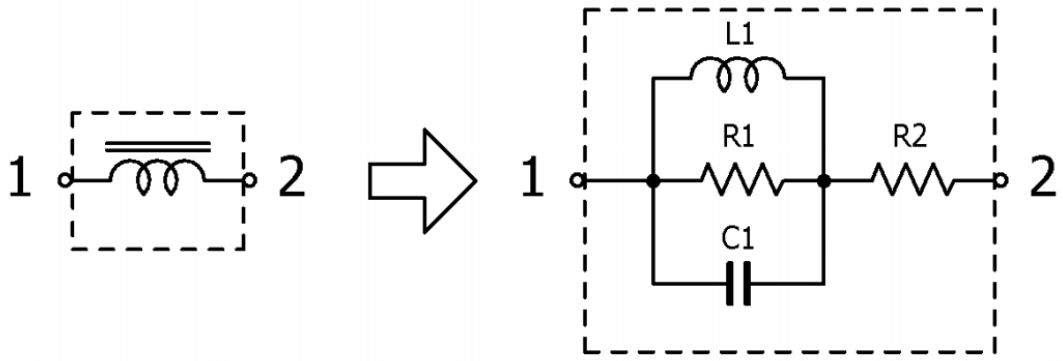


Figure 3.10. MLF2012 inductor series equivalent circuit diagram. From TDK.

3.4.8 Tindall's Inductor and Reference Low Loss *Air-core* Inductor Models

Tyndall's thin-film Magnetics-on-Silicon inductor is referred to as tf-MoS "*MagPwr*" MS2, and this thesis will refer to it as *MagPwr* from here on.

The *MagPwr* and *air-core* inductor are given a new format model as shown in Figure 3.11. The resistor R_{DC} models the DC resistance and is connected in series with the inductor L. The resistor R_{AC} conducts the ripple current and models the AC losses (core and high frequency copper). The AC current is supplied by a VCCS with a gain $G = 10{,}000$, the VCCS measures the voltage across a negligible resistor $R_1 = 10$ μΩ, R_1 is connected in series with the output capacitor.

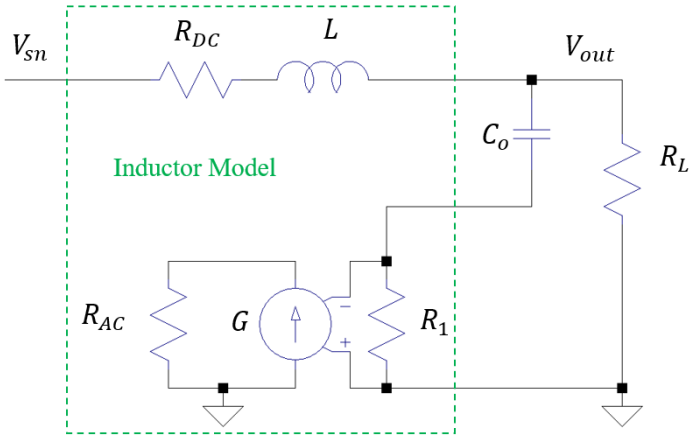


Figure 3.11.Lumped circuit model for MagPwr and air-core inductors.

For the *MagPwr* inductor R_{DC} was measured to be 150 mΩ.

The large signal quality factor, $Q_{LS} \approx 10$, when measured at 30 MHz. As

$$Q_{LS} = \omega L/R \text{ and } \omega = 2\pi f_{sw}$$

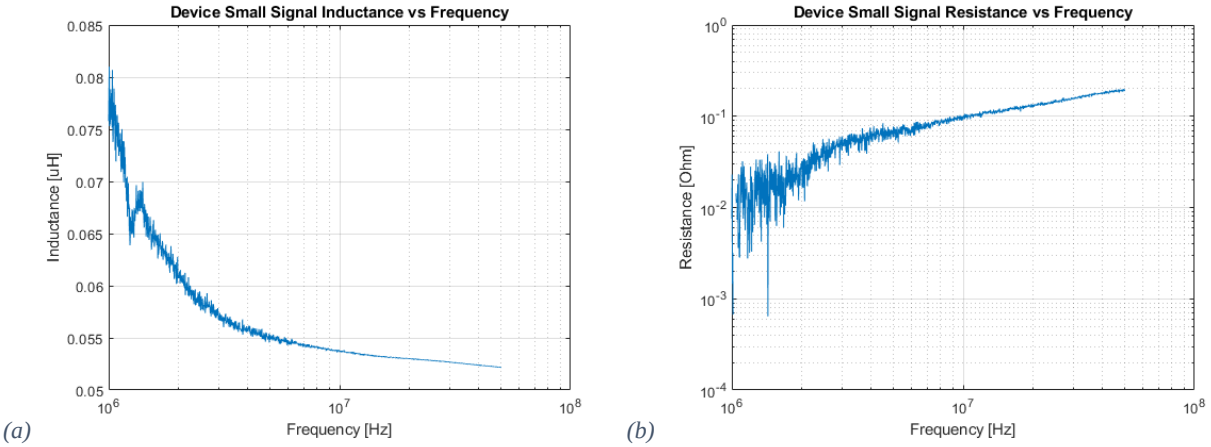
for a 50 nH inductor at 30 MHz, the total resistance is 942 mΩ, thus R_{AC} is 792 mΩ.

Note that further validation work is required on this modelling technique. The advantage is that there is the possibility of perfectly separating out the DC and AC components of loss. The difficulty is that R_{AC} conventionally represents the loss resistance at a given frequency for the case of DC and AC current flowing through it.

The *air-core* inductor was designed and built to have a very low DC resistance and with no core material to have very low AC loss, compared with the other inductors, to act as a benchmark for negligible inductor loss. The *air-core* was measured to have $R_{DC} \approx 5$ mΩ and $L \approx 50$ nH. It is shown in Figure 3.12, it has 9 turns, it is made in a solenoid pattern, and it is made with nine twisted strands of 35 SWG.

Figure 3.12. 50 nH air-core inductor.

For the *air-core* its parameters are measured with Agilent E5071C 300 kHz – 20 GHz network analyser, Figure 3.13(a) shows the inductance for the frequency of interest, Figure 3.13(b) shows the resistance for the frequency of interest. Table 3.5 shows the values of R_{DC}, R_{AC}, and L for the frequencies of interest.



(a) *(b)*

Figure 3.13. The air-core inductor's (a) inductance and (b) resistance response to frequency (logarithmic scale).

Frequency	**(MHz)**	**0**	**20**	**25**	**30**	**35**	**40**
Total Resistance	**(mΩ)**	R_{DC} = 6	126.2	146.6	157.5	161.7	177.1
AC Resistance (R_{AC})	**(mΩ)**	0	120.2	140.6	151.5	155.7	171.1
Inductance (L)	**(nH)**	N/A	53	52.8	52.66	52.52	52.39

Table 3.5. The values of R_{DC}, R_{AC}, and L for the air-core inductor for various frequencies.

3.5 Switching Behaviour

3.5.1 Diode Reverse Recovery and 3rd Quadrant Reverse Conduction

This section reviews and discusses body-diode reverse recovery (DRR) in CMOS switches (*ne5*), and 3rd quadrant reverse conduction (QRR) in GaN switches (EPC2040) applied in synchronous buck converters and focusing on the impact of the dead time. In this section all dead-times in a converter are assumed to be equal, only 2-level buck converters are considered and the drivers are assumed to behave like ideal voltage sources. The dead-time is defined as the time between $V_{GS(HS)}$ falling below V_{th} and $V_{GS(LS)}$ rising above V_{th}.

3.5.1.1 ne5 Diode Reverse Recovery

The test circuit shown in Figure 3.14(a), is designed to have $I_{out} = 1$ A and small Δi_L (≈ 0.06 A). For the ne5 switch, $V_{th} \approx 0.72$ V, the gate rise and fall times are 1 ns and the driver open-circuit levels are 0 V and 5 V. Combining these three factors, if $t_{on} = 23.2$ ns then $V_{GS(HS)}$ and $V_{GS(LS)}$ reach V_{th} at approximately the same time. Thus, the dead time for this particular on-time is defined as $t_d \approx 0$ ns. To illustrate, if $t_{on} = 22.2$ ns then $t_d \approx 1$ ns, and if $t_{on} = 24.2$ ns then $t_d \approx -1$ ns. The waveforms $I_L, V_{GS(HS)}$ and $V_{GS(LS)}$ for $t_d \approx 1$ ns, are shown in Figure 3.14(b). The following sections detail negative t_d (shoot-through), small positive t_d (partial body diode conduction), and larger positive t_d (full body diode conduction), and their effects on the diode reverse recovery.

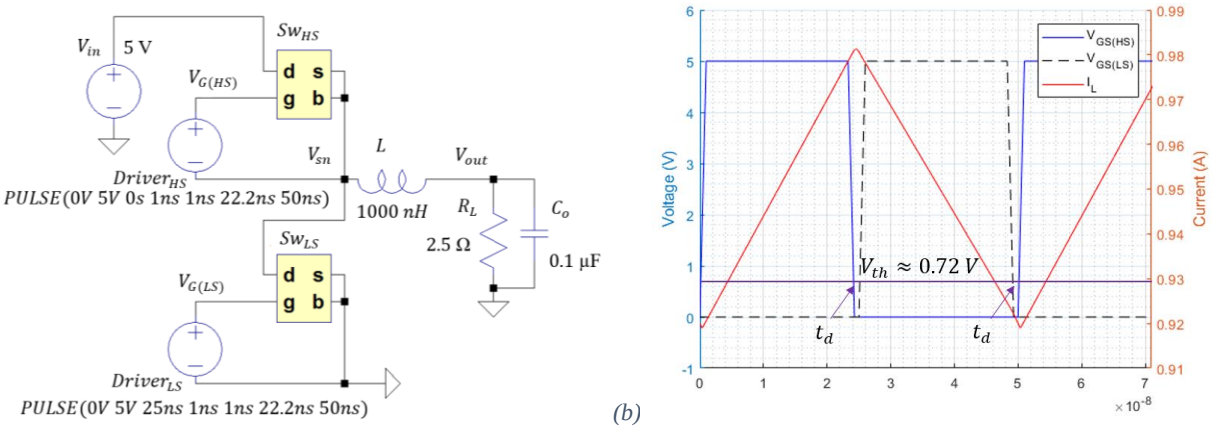


Figure 3.14. (a) Circuit diagram, and (b) inductor current and gate voltages, when t_d = 1 ns with ne5 switches.

Negative Dead Time

In this section the switch which is turning on, does so before the other has finished fully turning off, so that the converter has negative dead time. t_{on} ranges from 23.2 ns to 24.2 ns and thus t_d ranges from 0 ns to -1 ns. The switch waveforms when $t_d = 0$ ns, are shown in Figure 3.15 for a full period. Figure 3.16(a) shows the switch waveforms when $t_d = 0$ ns for Sw_{HS} turn-on. Figure 3.16(b) shows, the switch waveforms when $t_d = -1$ ns for Sw_{HS} turn-on. The two figures begin with $V_{GS(HS)}$ rise from 0 V. There is a large difference in the current waveforms in the two figures due to the duration of shoot-through. When $t_d = 0$ ns, ns the peak current I_{pk} is approximately 4.4 A, it peaks at approximately 0.4 ns. When $t_d = -1$ ns, I_{pk} is greater than 20 A, it peaks at approximately 0.65 ns.

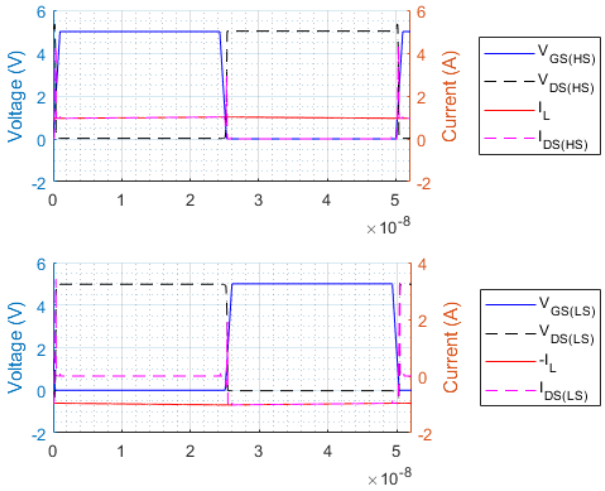


Figure 3.15. The ne5 switch waveforms when t_d = 0 ns, for one period.

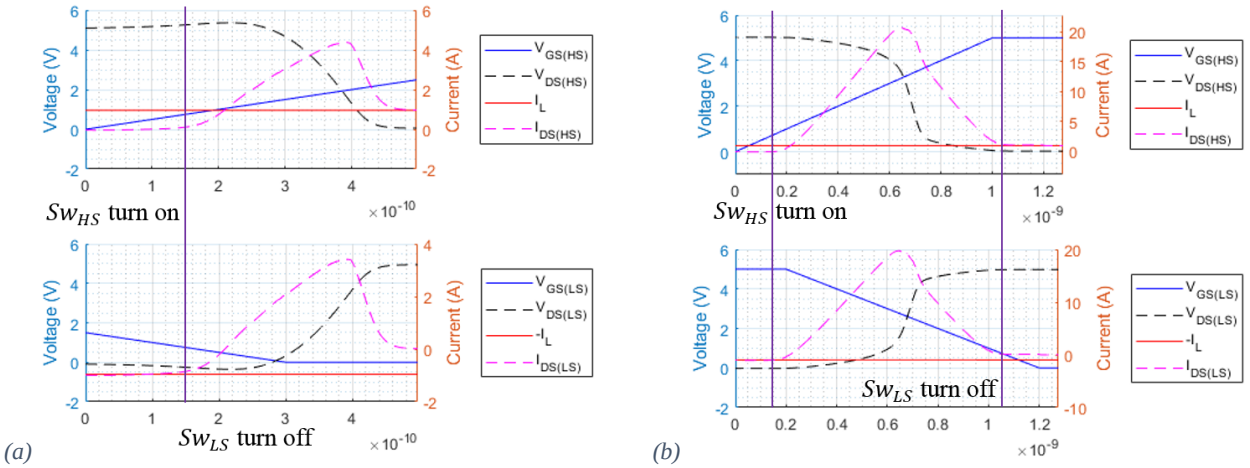


Figure 3.16. The ne5 switch waveforms when (a) t_d = 0 ns, and (b) t_d = -1 ns, at Sw_{HS} turn-on.

Figure 3.17(a) shows $I_{DS(HS)}$ waveforms at Sw_{HS} turn-on for a range of negative t_d. As value of t_d becomes more negative, I_{pk} gets larger and the peaks occur later, due to Sw_{LS} turning off later. The current waveforms for $t_d = 0$ ns to $t_d = -0.3$ ns are very similar indicating that they do not have shoot-through. Note that the final value of $I_{DS(HS)} = I_L = 1$ A.

Figure 3.17(b) shows $V_{DS(LS)}$ waveforms at Sw_{HS} turn-on for a range of negative t_d. The voltage waveforms for $t_d = 0$ ns to $t_d = -0.3$ ns, initially go negative and this indicates that for these values of t_d that the diode is partially conducting, I_L doesn't entirely go through Sw_{LS} channel. When t_d has a value of -0.4 ns and below, there is no negative voltage, as Sw_{HS} is on before Sw_{LS} starts to turn-off.

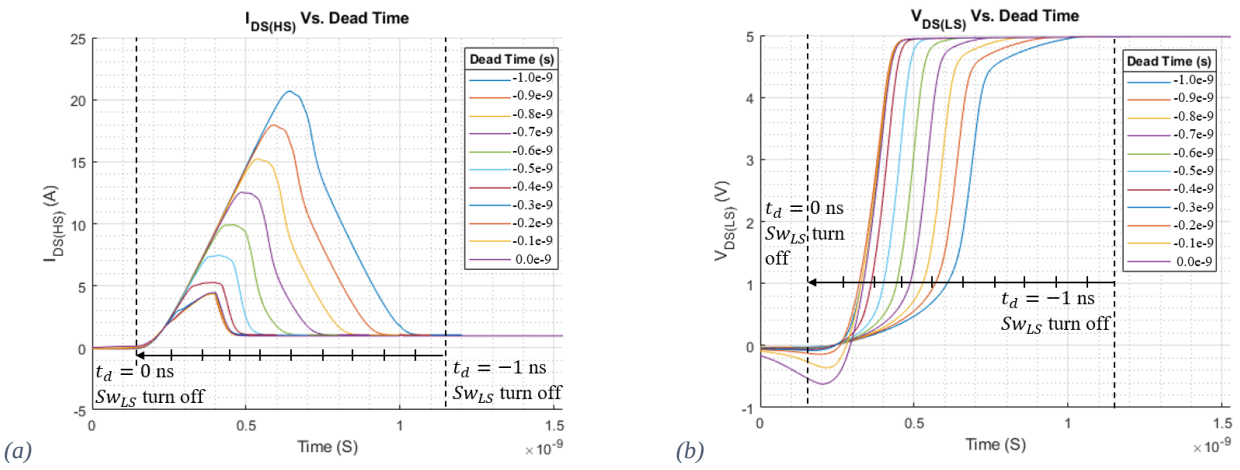


Figure 3.17. (a) $I_{DS(HS)}$ and (b) $V_{DS(LS)}$ waveforms, at Sw_{HS} turn-on, for negative t_d with ne5 switches.

Small Positive Dead Time

Figure 3.18(a) shows, the switch waveforms at Sw_{HS} turn-on, when $t_d = -0.25$ ns ($t_{on} = 23.45$ ns). Figure 3.18(b) shows, the switch waveforms at Sw_{HS} turn-on for $t_d = 0.15$ ns ($t_{on} = 23.05$ ns). When $t_d = 0.15$ ns, $I_{pk(LS)} \approx 4.4$ A, at approximately 0.4 ns, the values are similar to for $t_d = -0.25$ ns. Between these two dead times, Sw_{LS} is conducting but its body diode has not fully turned on yet, thus the channel of Sw_{LS} is conducting too.

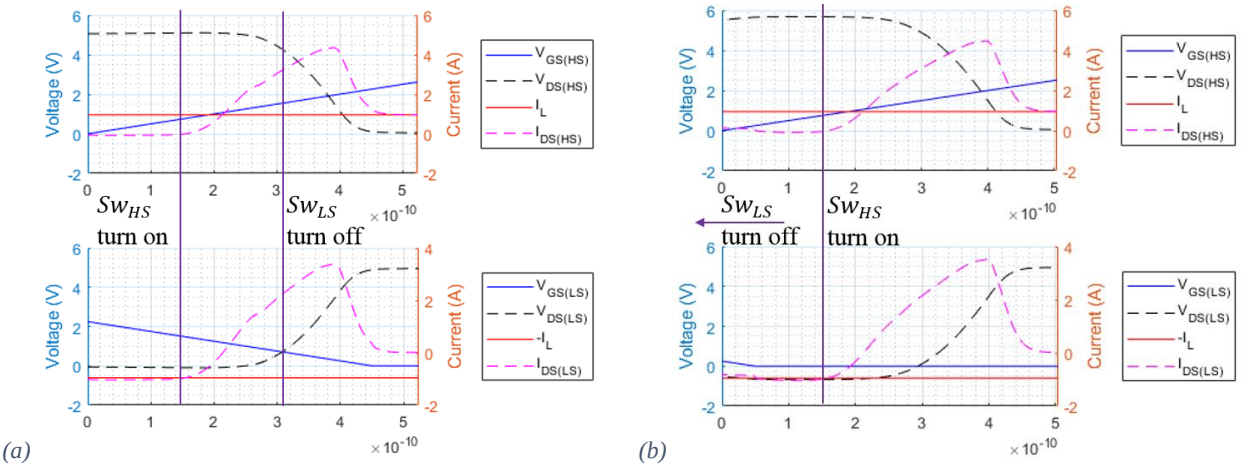


Figure 3.18. The ne5 switch waveforms when (a) t_d = -0.25 ns, and (b) t_d = 0.15 ns, at Sw_{HS} turn-on.

Figure 3.19(a) shows $I_{DS(HS)}$ waveforms for small positive t_d, at Sw_{HS} turn-on. I_{pk} only gets slightly larger with greater t_d and it also peaks slightly later. $I_{pk(HS)}$ increases from ≈ 4.32 A to ≈ 4.45 A as t_d increases from -0.25 ns to 0.15 ns.

Figure 3.19(b) shows, $V_{DS(LS)}$ waveforms for small positive t_d, at Sw_{HS} turn-on. As t_d increases, Sw_{LS} has to conduct I_L for a larger amount of time between being turned off, and Sw_{HS} turning on. When t_d is large enough the channel of Sw_{LS} is completely closed, and its body diode conducts all of I_L. The more current the body diode conducts, the more negative $V_{DS(LS)}$ is during the dead time. When $t_d = 0.05$ ns, $V_{DS(LS)}$ flattens at approximately -0.67 V, for larger values of t_d $V_{DS(LS)}$ continues to flatten at this value, this is the forward voltage of the body diode as it is conducting almost all of the current going through Sw_{LS}.

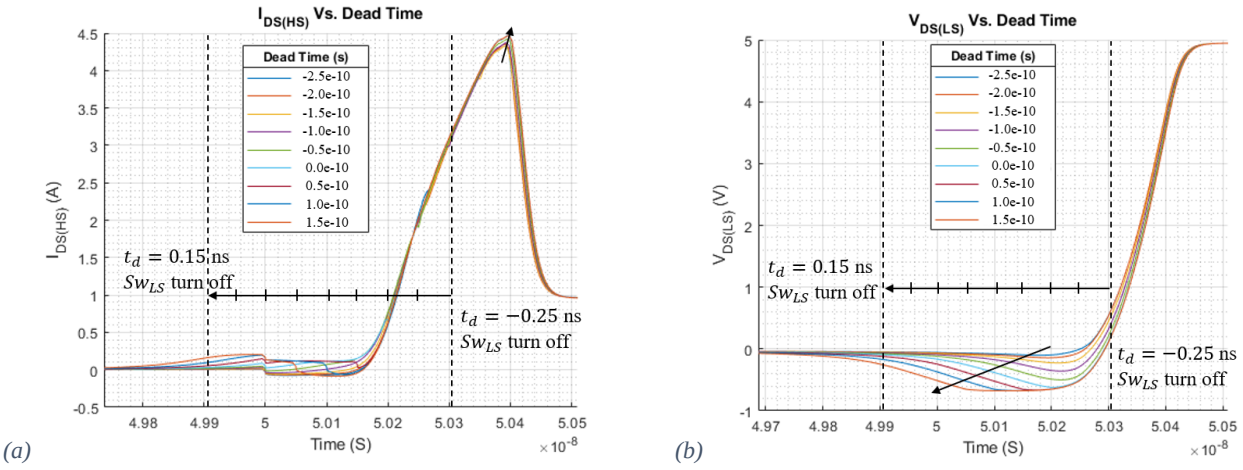


Figure 3.19. (a) $I_{DS(HS)}$ and (b) $V_{DS(LS)}$ waveforms, at Sw_{HS} turn-on, for small t_d with ne5 switches.

Large Positive Dead Time

Figure 3.20 shows, the switch waveforms for the circuit with $t_d = 1.16$ ns ($t_{on} = 21.04$ ns), at Sw_{HS} turn-on. Here the minimum value of $V_{DS(LS)} \approx -0.67$ V, which is the body diode forward voltage (V_F). I_{pk} is approximately 4.4 A and is approximately the same as when $t_d = 0.15$ ns in the previous sub-section. Sw_{LS} body diode is fully conducting Sw_{LS} current during the dead time, and the current spike is due to diode reverse recovery.

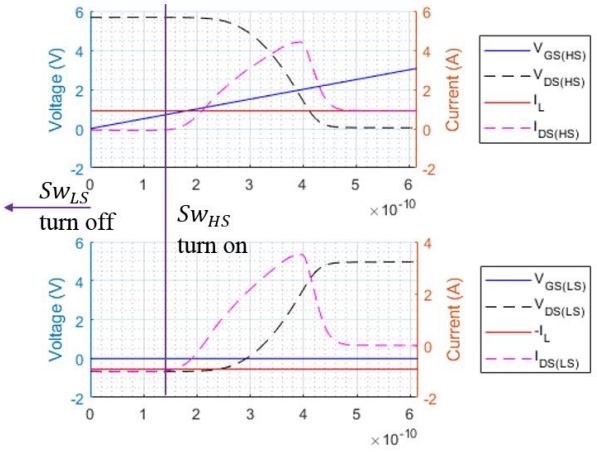


Figure 3.20. The ne5 switch waveforms when $t_d = 1.16$ ns, at Sw_{HS} turn-on.

Figure 3.21(a) shows, $I_{DS(HS)}$ waveforms for large positive t_d, at Sw_{HS} turn-on. There are very negligible differences in I_{pk} between various t_d. There is a change in current after Sw_{LS} turns off, that lasts approximately 0.2 ns, where the current rises to approximately 0.2 A and plateaus for approximately 0.1 ns, then returns to zero. This change in current occurs because, at the start of Sw_{LS} turn-off, and before $V_{DS(LS)}$ falls to V_F, $I_{C_{GD(LS)}}$ will flow through Sw_{HS}.

Figure 3.21(b) shows, $V_{DS(LS)}$ waveforms for large positive t_d, at Sw_{HS} turn-on . The minimum value of $V_{DS(LS)}$ is approximately -0.67 V, for any t_d value.

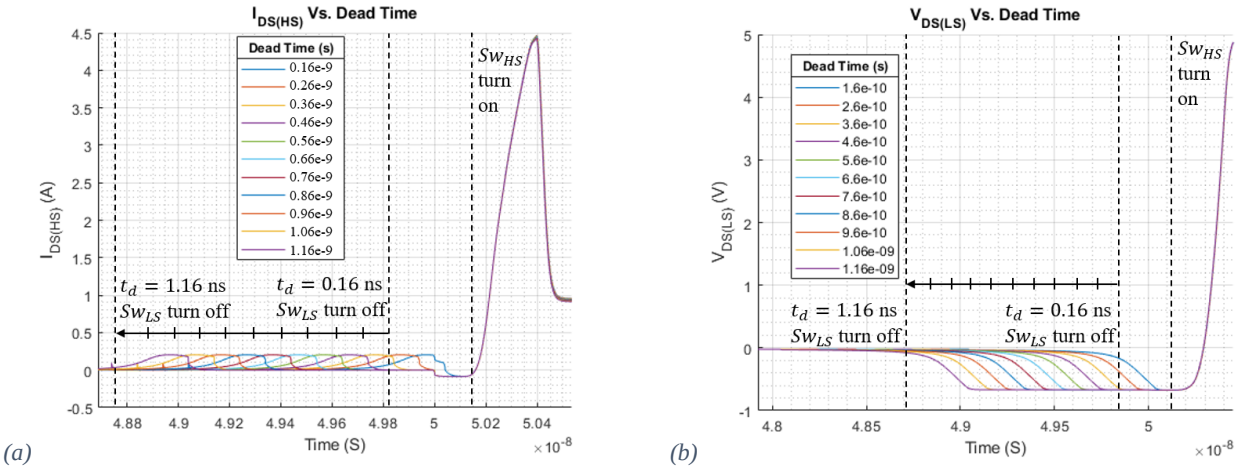


Figure 3.21. (a) $I_{DS(HS)}$ and (b) $V_{DS(LS)}$ waveforms at Sw_{HS} turn-on, for large t_d with ne5 switches.

3.5.1.2 EPC2040 3rd Quadrant (Reverse) Conduction Recovery

The test circuit shown in Figure 3.22, is designed to have $I_{out} = 1$ A, and small $\Delta i_L (\approx 0.06$ A). For the EPC 2040$V_{th} \approx 2$ V, the gate rise and fall times are 1 ns and the driver levels are 0 V and 5 V. Combining these three factors, if $t_{on} = 23.8$ ns, $V_{GS(HS)}$ and $V_{GS(LS)}$ reach V_{th} at nearly the same time. Thus, the dead time for this particular on-time is defined as $t_d \approx 0$ ns. Thus, if $t_{on} = 22.8$ ns then $t_d \approx 1$ ns, and if $t_{on} = 24.8$ ns then $t_d \approx -1$ ns. The waveforms I_L, $V_{GS(HS)}$ and $V_{GS(LS)}$ when $t_d \approx 0$ ns, are shown in Figure 3.22(b). The following sections will detail negative t_d (shoot-through), small positive t_d (before 3rd Quadrant conduction), and larger positive t_d (3rd Quadrant conduction), and their effect on the 3rd quadrant conduction recovery.

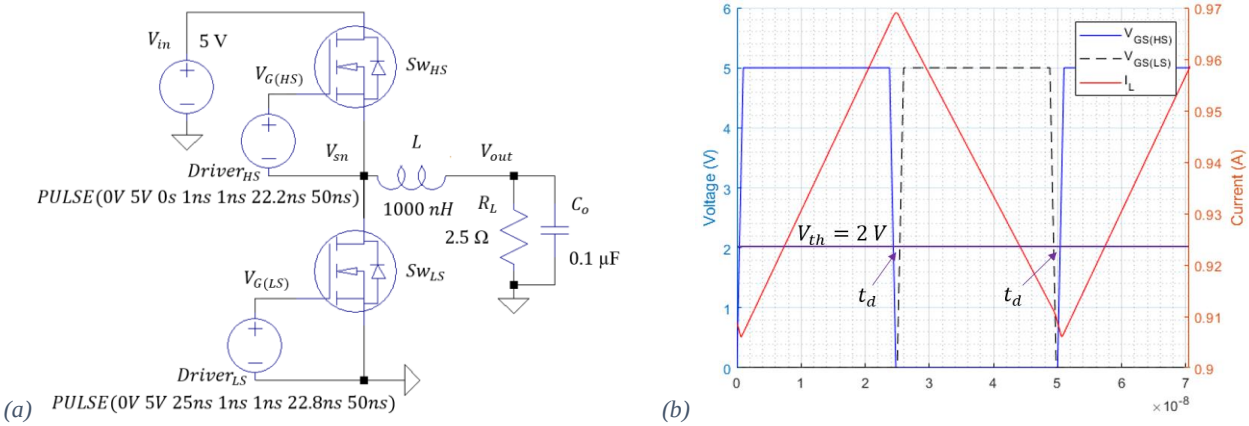


Figure 3.22. The (a) circuit Diagram, and (b) inductor current and gate voltages, when t_d = 1 ns, with EPC2040 switches.

Negative Dead Time

In this section each switch is allowed to start turning on before the other has finished fully turning off. The t_{on} ranges from 23.8 ns to 24.8 and ns, t_d ranges from 0 ns to -1 ns. The switch waveforms when $t_d = 0$ ns, are shown in Figure 3.23 for a full period. Figure 3.24(a) shows, a closer look at Sw_{HS} turn-on when $t_d = 0$ ns. Figure 3.24(b) shows, the switch waveforms when $t_d = -1$ ns at Sw_{HS} turn-on. There is a large difference in current waveforms for the two figures due to shoot-through. When $t_d = -1$ ns, I_{pk} is greater than 45 A at approximately 1 ns, when $t_d = 0$ ns, $I_{pk(LS)} =$ 2.4 A at ~0.65 ns.

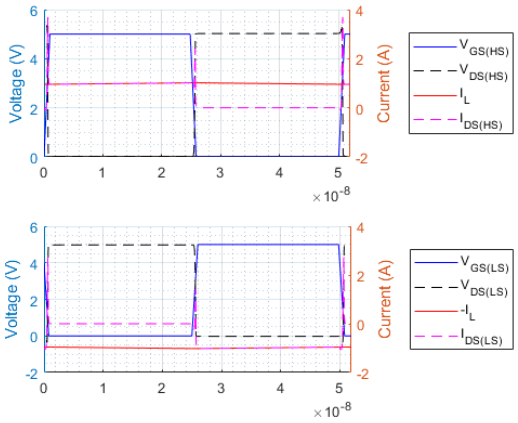


Figure 3.23. The EPC2040 switch waveforms when t_d = 0 ns, for one period.

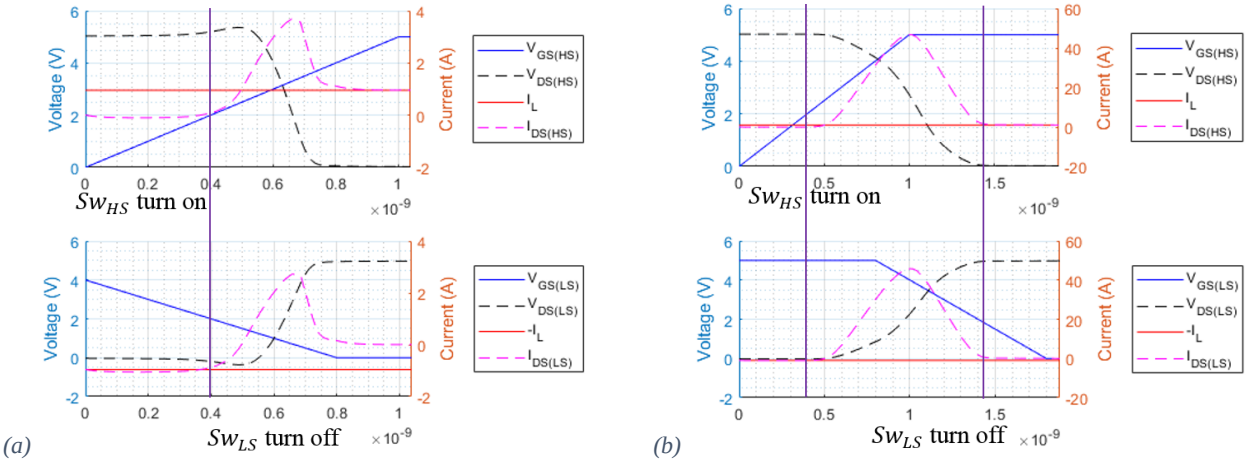


Figure 3.24. The EPC2040 switch waveforms when (a) t_d = 0 ns, and (b) t_d = -1 ns, at Sw_{HS} turn-on.

Figure 3.25(a) shows, $I_{DS(HS)}$ waveforms at Sw_{HS} turn-on, for negative t_d. As t_d becomes more negative, I_{pk} gets larger and occurs later due to Sw_{LS} turning off later. The current waveforms when $t_d = 0$ ns and $t_d = -0.1$ ns are very similar indicating neither has shoot-through.

Figure 3.25(b) shows, $V_{DS(LS)}$ waveforms at Sw_{HS} turn-on, for negative t_d. When $t_d = 0$ ns and $t_d = -0.1$ ns, the voltage initially goes negative to indicates that there is still some small t_d, during which I_L flows through Sw_{LS}, but the switch doesn't fully conduct. Other values for t_d, create no negative voltage, as Sw_{HS} is on before Sw_{LS} starts to turn-off.

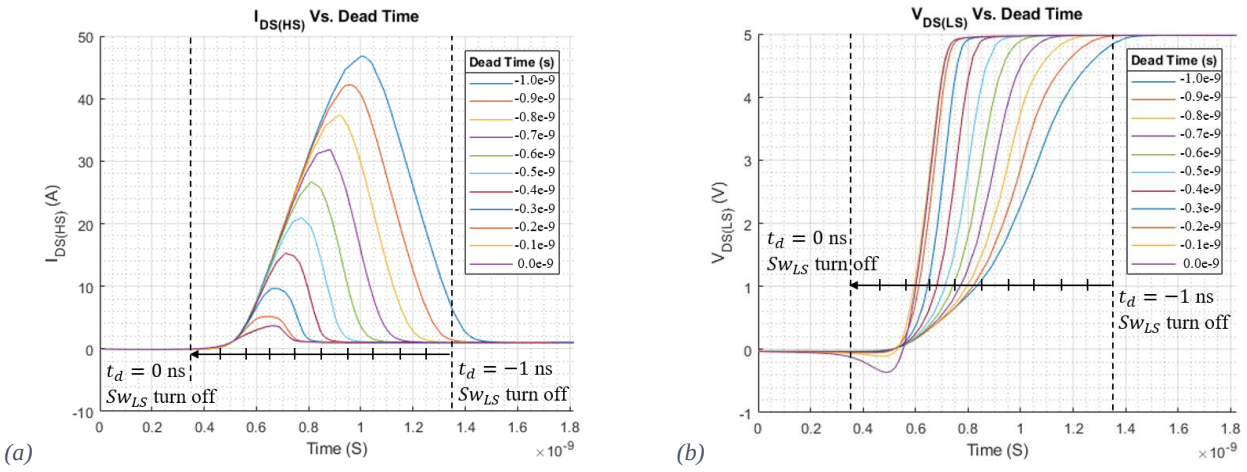


Figure 3.25. (a) $I_{DS(HS)}$ and (b) $V_{DS(LS)}$ waveforms, at Sw_{HS} turn-on, for negative t_d with EPC2040 switches.

Small Positive Dead Time

Figure 3.26 shows, the switch waveforms for the circuit with $t_d = 0.4$ ns ($t_{on} = 23.4$ ns), at Sw_{HS} turn-on. With this t_d, $V_{DS(LS)}$ almost goes to the reverse conduction forward voltage ($V_F \approx 2.2$ V) and $I_{pk(LS)} \approx 3$ A at ≈ 0.7 ns. Sw_{LS}, is conducting but has not entered the 3rd Quadrant conduction.

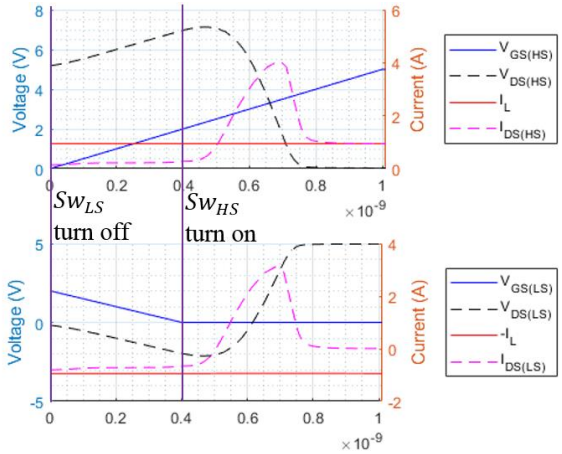


Figure 3.26. The EPC 2040 switch waveforms when $t_d = 0.4$ns, at Sw_{HS} turn-on.

Figure 3.27(a) shows, $I_{DS(HS)}$ waveforms for small positive t_d, at Sw_{HS} turn-on. I_{pk} is larger with greater t_d and it also peaks slightly later. Note that when $t_d \geq 0.32$ ns the current does not go negative. I_{pk} increases from ≈ 3.7 A to ≈ 4.1 A, when t_d increases from 0 ns to 0.4 ns.

Figure 3.27(b) shows, $V_{DS(LS)}$ for small positive t_d, at Sw_{HS} turn-on. As t_d increases, $V_{DS(LS)}$ gets progressively more negative, due to Sw_{LS} having to conduct I_L for a larger amount of time between being turned off and Sw_{HS} turning on.

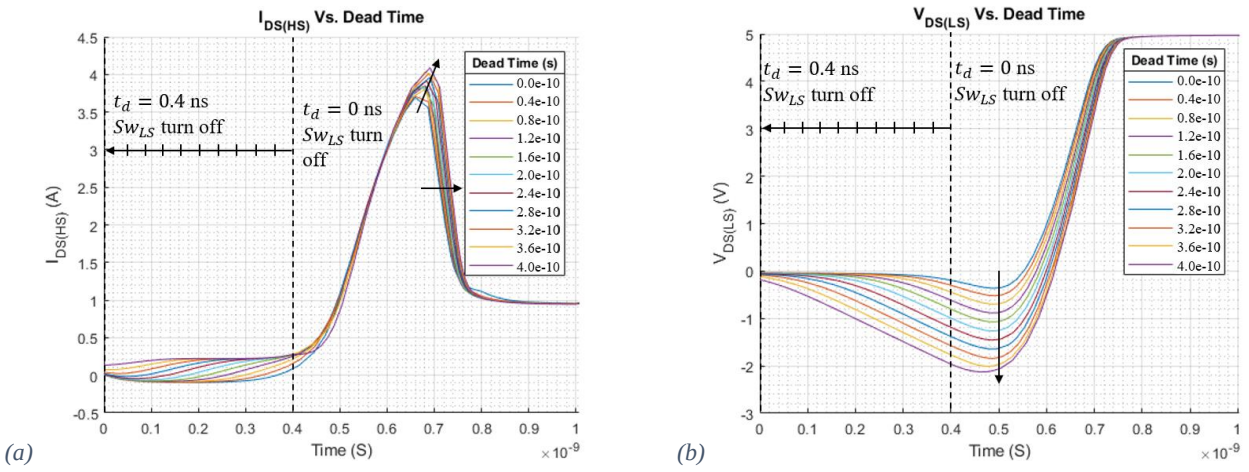


Figure 3.27. (a) $I_{DS(HS)}$ and (b) $V_{DS(LS)}$ waveforms, at Sw_{HS} turn-on, for small t_d with EPC2040 switches.

Large Positive Dead Time

Figure 3.28 shows, the switch waveforms for the circuit when $t_d = 1.4$ ns ($t_{on} = 22.4$ ns), at Sw_{HS} turn-on. The minimum value of $V_{DS(LS)} \approx -2.2$ V, which is assumed to be V_F. I_{pk} is very similar to the value when $t_d = 0.4$ ns. Sw_{LS}, has entered 3rd Quadrant conduction.

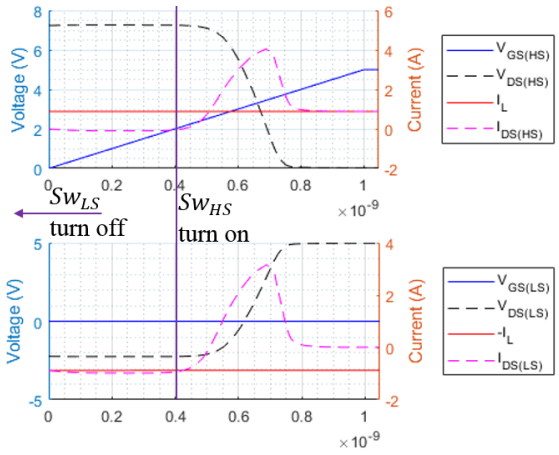


Figure 3.28. The EPC2040 switch waveforms when $t_d = 1.4$ ns, at Sw_{HS} turn-on.

Figure 3.29(a) shows, $I_{DS(HS)}$ waveforms for large positive t_d, at Sw_{HS} turn-on. There is very little difference in I_{pk} between the various t_d. After Sw_{LS} turns off, there is a change in $I_{DS(HS)}$, the current rises for approximately 0.5 ns, to a value of approximately 0.3 A and plateaus for approximately 3 ns, then returns to zero (with the exception of $t_d = 0.4$ ns). This occurs when the value of $V_{DS(LS)}$ has not reached V_F and Sw_{LS} starts to turn-off, resulting in $I_{C_{GD(LS)}}$ flowing through Sw_{HS}.

Figure 3.29(b) shows, $V_{DS(LS)}$ waveforms for large positive t_d, at Sw_{HS} turn-on. $V_{DS(LS)}$ drops to approximately -2.2 V (except for $t_d = 0.4$ ns) besides the time they reach V_F the waveforms appear identical.

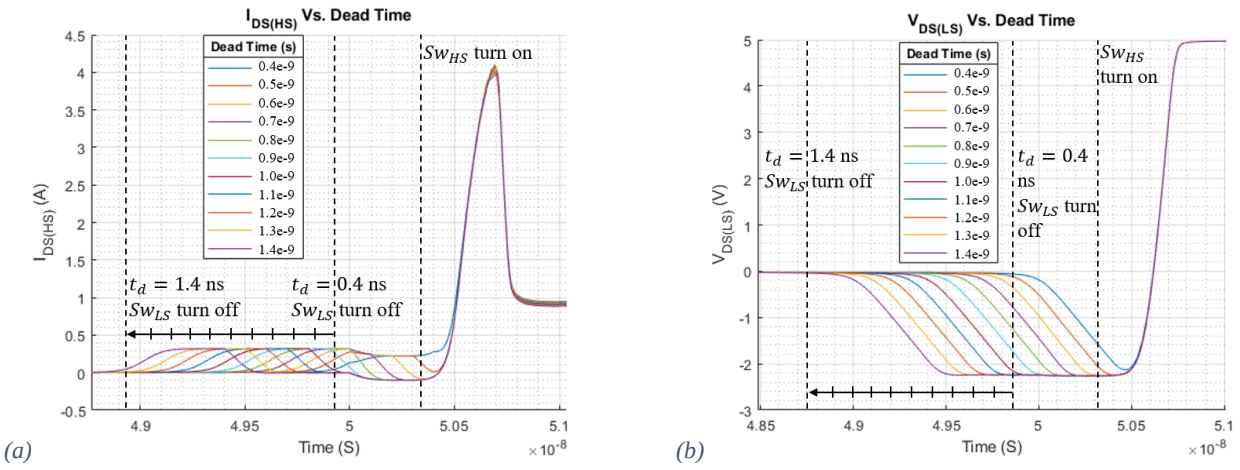


Figure 3.29. (a) $I_{DS(HS)}$ and (b) $V_{DS(LS)}$ waveforms, at Sw_{HS} turn-on, for large t_d with EPC2040 switches.

3.5.1.3 Analysis and Comparison of ne5 and EPC2040, with Varying Dead Times

The comparisons between the *ne5* and EPC2040, waveforms show a lot of similarities and they follow the same general patterns, but there are some slight differences.

When t_d is negative, there are large shoot-through currents, it is important that t_d is large enough to avoid this, as a shoot-through for nanoseconds can result in currents over 40 A. The EPC switches have a larger peak shoot-though current than the *ne5* switches for the same amount of time, this is due to them having less capacitance. For both switches, if t_d is negative but relatively small, Sw_{LS} turns off before shoot-through occurs. $V_{DS(LS)}$ does not go negative, because Sw_{LS} does not need to conduct I_L, while remaining off.

When t_d is positive and relatively small, the general trend of $I_{DS(HS)}$ is that the current goes slightly negative, and then ramps up to I_{pk}, which is slightly larger with larger t_d. For the ne5 switches there is some unusual behavior before the peak, which is due to both switches being on at the same time. The ne5 switches have a larger I_{pk}, indicating that their diode reverse recovery is larger than the EPC switches' 3rd Quadrant conduction recovery. Note for the ne5 switches I_{pk} occurs at approximately 0.4 ns whereas for the EPC switches I_{pk} is at approximately 0.7 ns, due to *ne5's* lower V_{th}. $V_{DS(LS)}$ of both switches get progressively more negative as t_d increases until they reach their V_F. For the body diode conduction with the *ne5* $V_F \approx 0.67$ V, and for the reverse conduction for the EPC2040 $V_F \approx 2.2$ V. The ne5 and EPC2040 reach this point for a similar value of t_d about 0.4 ns.

Using the changes in voltage and the currents in the capacitor equation:

$$i = C\frac{dV}{dt} \qquad (3.4)$$

the capacitance can be found.

When t_d is positive and larger, as Sw_{LS} turns off b$V_{DS(LS)}$ goes from 0 V to V_F. This change in voltage across the drain-source causes $I_{C_{GD(LS)}}$ to flow, this current must flow though Sw_{HS}, the current returns to zero when $V_{DS(LS)} = V_F$. For the *ne5*, its $I_{C_{GD(LS)}} \approx 0.3$ A, and its $V_{DS(LS)}$ goes from 0 V to -0.67 V in approximately 0.25 ns, thus its rate of change is 2.68 V/ns, indicating a capacitance of approximately 0.11 nF. For the EPC, its $I_{C_{GD(LS)}} \approx 0.4$ A and its $V_{DS(LS)}$ goes from 0 V to -2.2 V in approximately 0.5 ns, thus

its rate of change is 4.4 V/ns, indicating a capacitance of approximately 0.09 nF using equation . This shows a similar $C_{GD(LS)}$ for both switches (for this particular circumstance), with the *ne5's* being larger as indicated in other chapters. Otherwise I_{pk} for both switches is affected by t_d slightly enough to be negligible.

3.5.1.4 Calculating Losses for Sw_{HS} Turn-On in Simulation

Figure 3.30 shows, Sw_{LS} and Sw_{HS} waveforms, when $t_d = 0.6$ ns with EPC2040 switches. The upper graph shows Sw_{HS} and the lower shows Sw_{LS} waveforms. This demonstrates how the turn-on loss is differentiated from the QRR loss, by finding key time points (tA-tE as labelled in MATLAB code). Using the guide from [25], the method for determining the QRR loss is explained below.

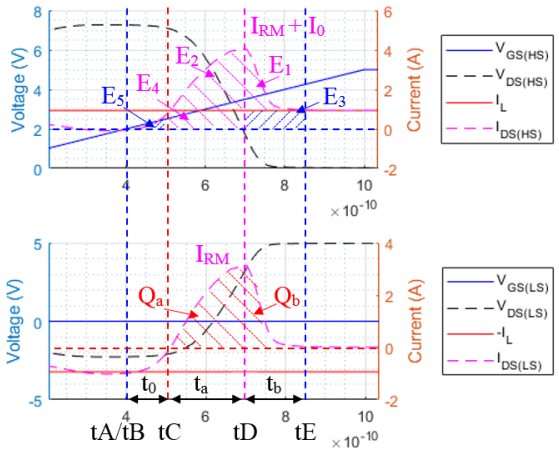


Figure 3.30. Sw_{HS} and Sw_{LS} waveforms, t_d = 0.6 ns and with EPC2040 switches at Sw_{HS} turn on. Example of 3rd Quadrant conduction recovery.

Timing Point Label	Condition
tA	$V_{GS(HS)}$ rises to V_{th}
tB	$I_{DS(HS)}$ rises to zero*
tC	$I_{DS(LS)}$ rises to zero
tD	Peak of $I_{DS(HS)}$ current spike
tE	$I_{DS(HS)}$ is the same as I_L

Table 3.6. Timing points for separating QRR and turn-on losses for EPC 2040 switches (DRR for ne5).

*In this case tA = tB, if I_L is less than $I_{DS(LS)}$, then $I_{DS(HS)}$ will be below 0 A before tA. If $I_{DS(LS)}$ is negative at tA there is no shoot-through. Assuming that the dead time is positive, whether $I_{DS(HS)}$ will be negative or not depends on how long the dead time is, and how close to 0 A I_L is at tA.

By finding the numeric integral of V_{DS} and I_{DS} during the time interval tB and tE the total turn-on energy loss in Sw_{HS} can be calculated:

$$E_{on(HS)tot} = \int_{tB}^{tE} V_{DS(HS)}(t) I_{DS(HS)}(t)\, dt. \qquad (3.5)$$

The energy loss during the interval of tB to tC is independent of the recovery:

$$E_5 = \int_{tB}^{tC} V_{DS(HS)}(t) I_{DS(HS)}(t)\, dt, \qquad (3.6)$$

as is the energy due to the inductor current during the interval of tD to tE:

$$E_3 = \int_{tD}^{tE} V_{DS(HS)}(t) I_L(t)\, dt. \qquad (3.7)$$

Thus, the reverse recovery loss can be calculated as:

$$E_{QRR(HS)} = E_{on(HS)tot} - E_5 - E_3. \qquad (3.8)$$

3.5.2 Switch Output Capacitance

To measure the equivalent energy output capacitance ($C_{oss(Eq)}$) for the EPC2040 or *ne5* switch, a voltage ramp across the drain-source of 0 V to 5 V is applied. The voltage ramp is simulated using a pulse generator. The ramp is designed to be similar to conditions in the synchronous EPC buck's V_{sn}, at Sw_{LS} turn-off and Sw_{HS} turn-on, when $t_d = 0$ ns, and $I_L \approx 1$ A. This voltage ramp is shown in Figure 3.31.

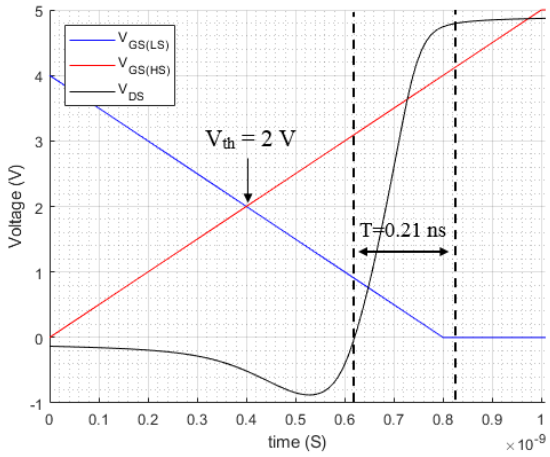


Figure 3.31. V_{DS}, $V_{GS(HS)}$ and $V_{GS(LS)}$ waveform for synchronous EPC2040 buck converter.

The test circuits are shown in Figure 3.32 (a) for the EPC2040 and Figure 3.32 (b) for the *ne5*. The voltage source V_{gate} ensures $V_{GS} = 0$ V, thus there is no I_{GS}. The body diode (or equivalent) is never allowed to turn-on so there is no forward current or reverse recovery. The voltage source V_{DD}, applies a linear voltage ramp similar to the change in the V_{DS}, as shown in Figure 3.31 V_{DS} ramps from 0 V to 5 V in approximately 0.21 ns. The resistors R_D, R_G, and R_S are added to make the current direction and value more convenient to measure in LTSpice, they have a value of 1 nΩ so as to be negligible.

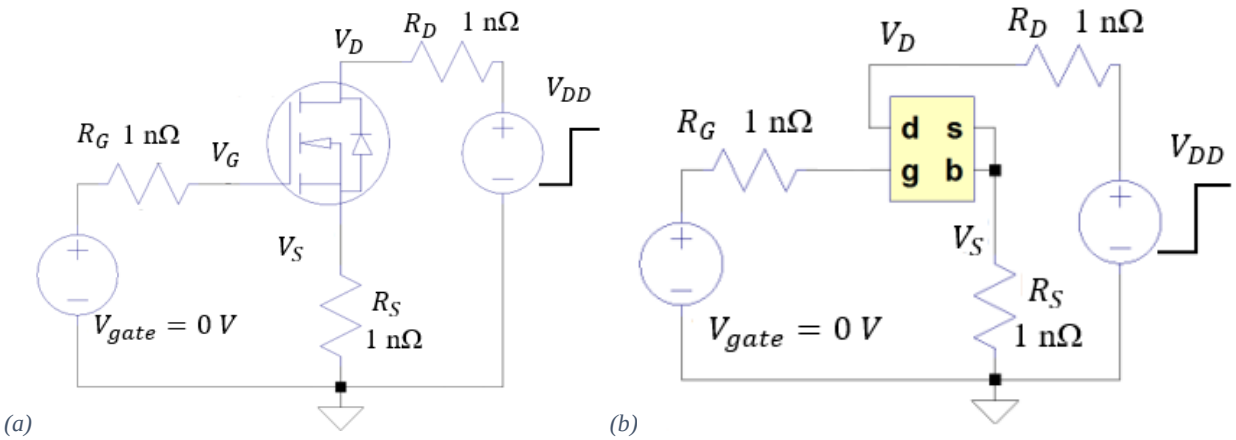


Figure 3.32. Circuit diagram for testing the equivalent energy capacitances for, (a) EPC2040 and (b) ne5 switches.

To ensure an equivalent test between the two switches, the W/L ratio of the *ne5* was set so that its r_{on}, matches the r_{on} of the EPC2040. r_{on} of the EPC2040 was measured with the circuit set up as in Figure 3.22(a) with $t_d = 0$ ns, $r_{on} = 24.17$ mΩ. The ne5 needs a width of 125 mm and a length 0.5 um to give $r_{on} = 24.55$ mΩ, in the conditions as in Figure 3.14(b).

An equivalent circuit for the switch is shown in Figure 3.33. As the switch does not turn-on, the diode never conducts (or the switch never enters 3rd quadrant conduction) and as $V_{GS} = 0$ V, there is no current flow in any of the paths indicated with green arrows. In LTSpice the current paths I_{DG} and I_{DS} cannot be measured directly, but the currents I_d, I_g and I_s can. The current that flows out of I_g flows entirely through C_{gd} and the current that flows out of I_s flows entirely through C_{ds}. These currents can be measured by the addition of the resistors R_G, and R_S shown in Figure 3.32.

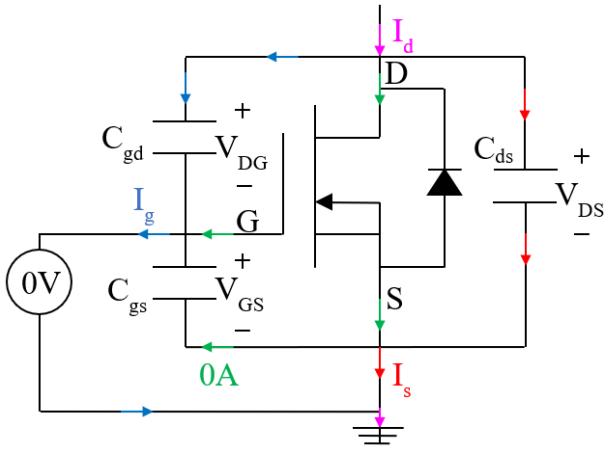


Figure 3.33. Equivalent Switch Circuit for bulk CMOS device with body shorted to source.

Drain, Source and Gate Current Waveforms, for Drain-Source Voltage Ramp

The voltage and current waveforms for the EPC2040 and *ne5* switches are shown in Figure 3.34. Capacitance in switches generally decreases as the voltage across them increases [16], which is why the currents are varying.

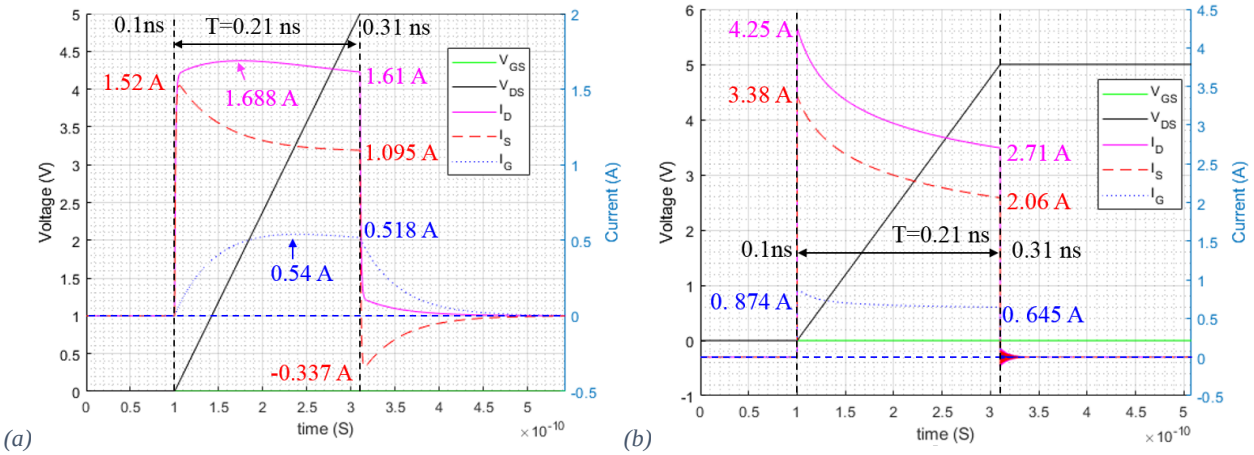


Figure 3.34. Current and Voltage Waveforms for (a) EPC2040 and (b) ne5, for equivalent energy capacitance determination.

The graphs in Figure 3.35 were obtained using the capacitor equation:

$$i(t) = C(t)\frac{dV}{dt}. \qquad (3.9)$$

As the gate is kept at zero volts, $V_{DS} = V_{DG}$. The voltage increases from 0 V to 5 V in 0.21 ns:

$$dV/dt = V_{DS}/dt \;=\; V_{DG}/dt \;= 2.38 \times 10^{10}\ V/s,$$

thus:

$$C(t) = i(t)/(2.38 \times 10^{10}).$$

Taking the respective current waveforms and dividing by 2.38×10^{10} V/s gives the relationships between the switch capacitances and respective voltage as shown in Figure 3.35.

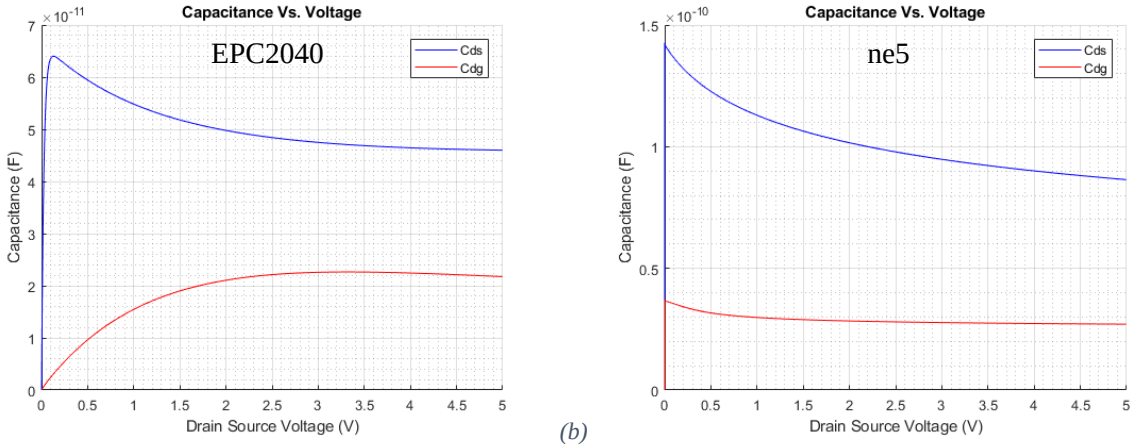


Figure 3.35. C_{dg} (blue) and C_{ds} (red) vs. V_{DS}, for (a) the EPC2040 switch and (b) the ne5 switch.

As the capacitances in a switch change with different voltage levels, an equivalent capacitance must be calculated, the methodology used is discussed in the next sub-chapter.

Mathematical Analysis of Equivalent Storage Energy Capacitance

The method used is the equivalent energy capacitance, which finds the equivalent linear capacitance needed to store the same amount of energy used for the corresponding change in voltage. This can be summarized by the following equation:

$$E = \int_{t_1}^{t_2} V(t)I(t)dt = \frac{1}{2}C_{Eq}V^2 \quad (3.10)$$

which can be rearranged as:

$$\Rightarrow C_{Eq} = \frac{2}{V^2}\int_{t_1}^{t_2} V(t)I(t)dt \quad (3.11)$$

where E is the energy in the capacitor, t_1 is the initial time the drain voltage starts to rise, t_2 is when the drain voltage reaches 5 V, $V(t)$ and $I(t)$ are the capacitor's voltage and current waveforms respectively, C_{Eq} is the equivalent energy capacitance, and V is the voltage difference (5 V).

The waveforms in MATLAB are in vector format, thus numeric integration is needed:

$$C_{Eq} = \frac{2}{V^2}\sum_{n=1}^{N}\frac{V(n)+V(n+1)}{2}\frac{I(n)+I(n+1)}{2}(t(n+1)-t(n)). \quad (3.12)$$

The equivalent output capacitance obtained by using (1.7), thus:

$$C_{oss(Eq)} = C_{gd(Eq)} + C_{ds(Eq)}. \quad (3.13)$$

Combining $C_{oss(Eq)}$ with the nominal on-resistance of the two switches gives a Figure of Merit (FOM):

$$FOM = C_{oss(Eq)}r_{on} \quad (3.14)$$

where r_{on} is the nominal on-resistance with the following voltage rating: $V_{DS} = 5\,V,\ V_{GS} = 5\,V$. As noted earlier for the EPC2040 this value is 24.17 mΩ, and for the *ne5* it is 24.55 mΩ, for $W = 125\,mm,\ L = 0.5\,um$. A comparison of these values is shown in Table 3.7.

	EPC2040	***ne5***
$C_{ds(Eq)}$ **(pF)**	47.928	94.517
$C_{dg(Eq)}$ **(pF)**	21.434	27.777
$C_{oss(Eq)}$ **(pF)**	69.362	122.294
$FOM\ (m\Omega nF)$	1.676	3.002

Table 3.7. Equivalent energy capacitance values and FOMs for EPC2040 and ne5.

The FOM of the EPC2040 switch is almost half of that of the *ne5*, indicating it has about half the capacitance, considering the on-resistances of the switches were matched, and $C_{oss(Eq)}$ of the EPC2040 is half of that of the *ne5*, as expected.

The $C_{oss(Eq)}$ value of the EPC2040 matches quite closely to its data sheet. The data sheet tested with $V_{DS} =$ 6 V and $V_{GS} = 0$ V and the typical $C_{oss(Eq)}$ value is 67 pF. The graph of the capacitance relationships with V_{DS} is shown in Figure 3.36 with $C_{oss(Eq)}$ at 5 V marked.

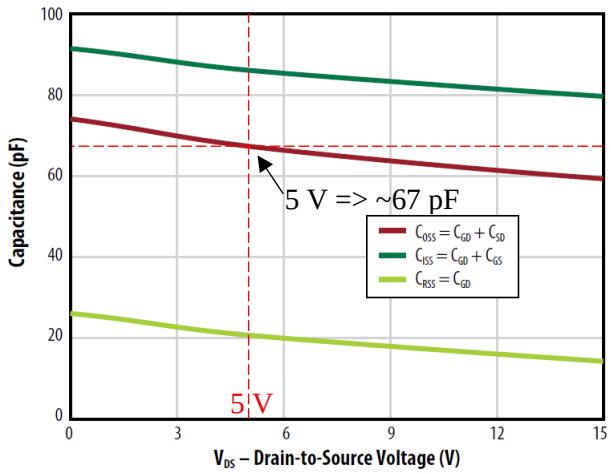


Figure 3.36. EPC2040 small signal capacitances vs. V_{DS}, from datasheet

The data sheet has an effective output capacitance (energy related) of 106 pF and an effective output capacitance (time related) of 87 pF, but these have a rise from 0 V to 40%*BV_{DD} (BV_{DD} = 15 V), and I_D = 300 µA, and the time taken for the rise is not included, so these values are not comparable to the value calculated in this sub-chapter.

3.6 Full Converter Simulations and Operating Waveforms

In this section the 2-level and 3-level buck converters, are compared using the two switch models and the four different inductor models (indicated with green boxes).

The two switches being modelled are the *ne5* switch (a bulk CMOS NMOS for 180 nm xt018 XFAB process) and the EPC2040 switch (a GaN e-HEMT), the W/L ratio of the ne5 set so that r_{on} of both switches are the same.

The four inductors being modelled are the *air-core* inductor, the "*MagPwr*" inductor, a Coilcraft inductor, and a Murata inductor.

The converter models include: the (cascade) bootstrap model (indicated with orange boxes), the Peregrine driver model (indicated with red boxes), and the board parasitic model (indicated with purple boxes).

The board parasitic model $R_{AC(Lpar)}$ roughly represents the near field damping parasitic inductance ringing, the values used to represent this are discussed in chapter 3.7.4.

The duty cycles are the same for the 2-level, as for the 3-level, so V_{out} of the 3-level is half of V_{out} of the 2-level. For these simulations, the duty cycle was chosen to be 0.5, in later sections the duty cycle will be chosen such that V_{out} is the same for the 2-level and 3-level converters.

3.6.1 2-Level *Air-core* Buck Converter

The circuit diagram for the 2-level buck converter is shown in Figure 3.37, it includes the models of the *air-core* inductor, the bootstrap capacitor, the board parasitic inductances, and the Peregrine driver.

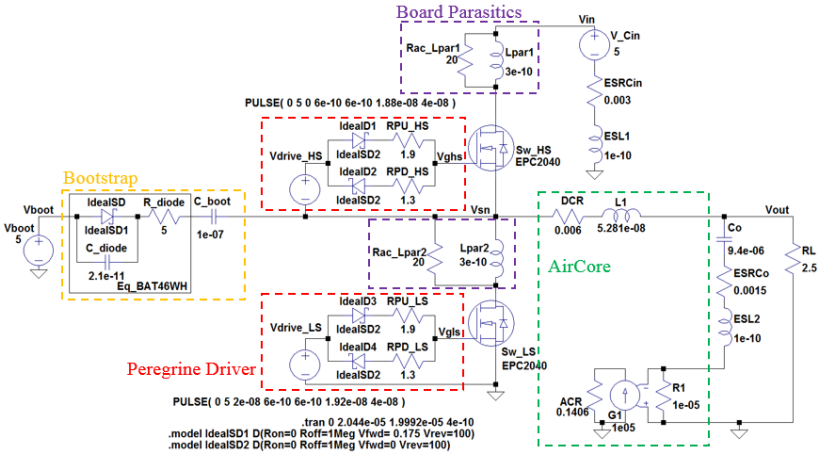


Figure 3.37. Full circuit diagram for the 2-Level buck converter, with the air-core inductor, and EPC2040 or ne5 switches.

Current and Voltage Waveforms for a 2-level Converter with EPC2040 Switches

In Figure 3.38, the output voltage and switch waveforms are shown, for a 2-level buck converter, with EPC2040 switches, and over one period. The converter is operated at $f_{sw} = 25$ MHz, $I_{out} = 1$ A, and $V_{in} = 5$ V. The average $V_{out} = 2.42$ V and $\Delta V_{out} = 16.83$ mV.

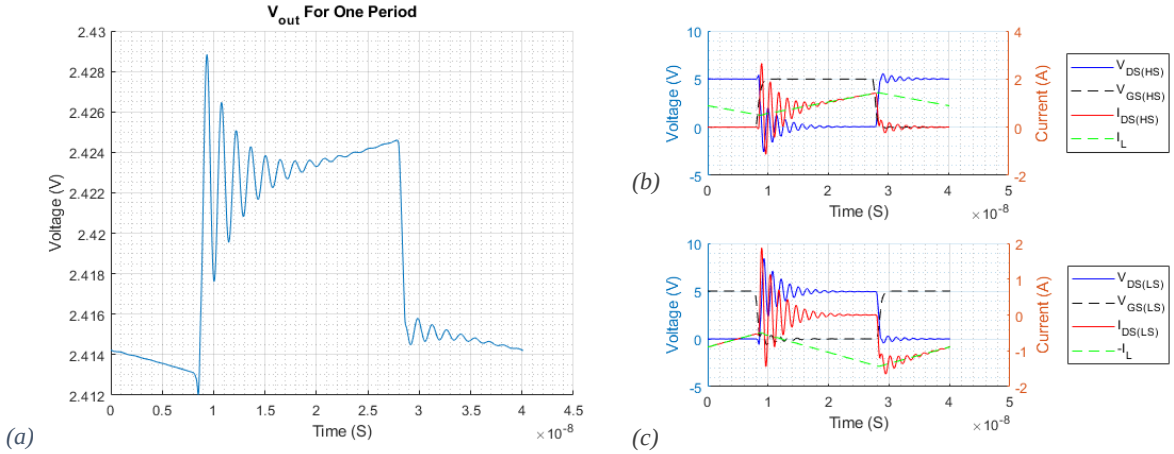


Figure 3.38. (a) V_{out}, (b) Sw_{HS} and (c) Sw_{LS} waveforms, for the 2-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the air-core inductor and EPC2040 switch models.

Current and Voltage Waveforms for a 3-level Converter with ne5 Switches

In Figure 3.39, the output voltage and switch waveforms are shown, for a 2-level buck converter, with *ne5* switches, and over one period. The converter is operated at $f_{sw} = 25$ MHz, $I_{out} = 1$ A, and $V_{in} = 5$ V. The average $V_{out} = 2.398$ V and $\Delta V_{out} = 15.99$ mV.

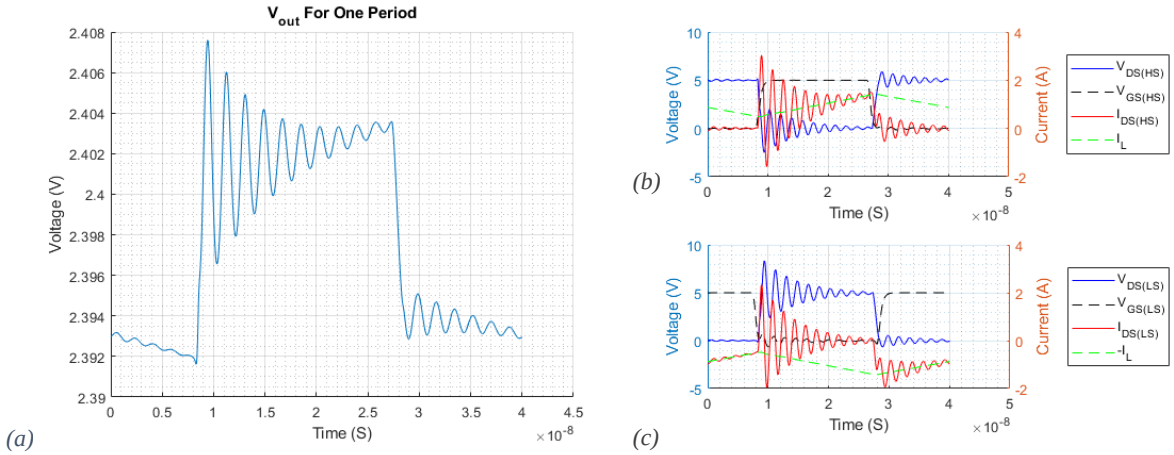


Figure 3.39. (a) V_{out}, (b) Sw_{HS}, and, (c) Sw_{LS} waveforms, for the 2-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the air-core inductor and ne5 switch models.

3.6.2 3-Level *Air-core* Buck Converter

The circuit diagram for the 3-level buck converter is shown in Figure 3.40, it includes the models of the *air-core* inductor, the bootstrap capacitor, the board parasitic inductances, and the Peregrine driver.

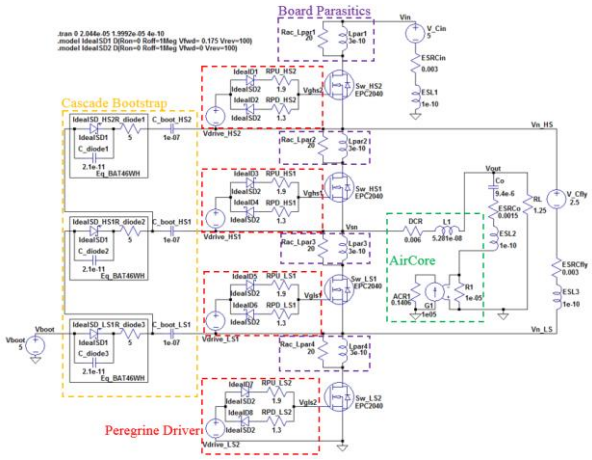


Figure 3.40. Full circuit diagram for the 3-Level buck converter, with the air-core inductor, and EPC2040 or ne5 switches.

Current and Voltage Waveforms for a 2-level Converter with EPC2040 Switches

In Figure 3.41 the output voltage waveform and in Figure 3.42 the switch waveforms are shown, for a 3-level buck converter, with EPC2040 switches over one period. The converter is operated at $f_{sw} = 25$ MHz, $I_{out} = 1$ A, and $V_{in} = 5$ V. The average $V_{out} = 1.13$ V and $\Delta V_{out} = 9.44$ mV.

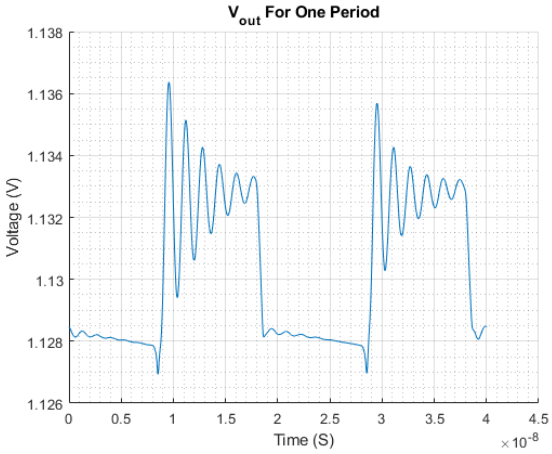


Figure 3.41. V_{out} waveform, for the 3-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the air-core inductor and EPC2040 switch models.

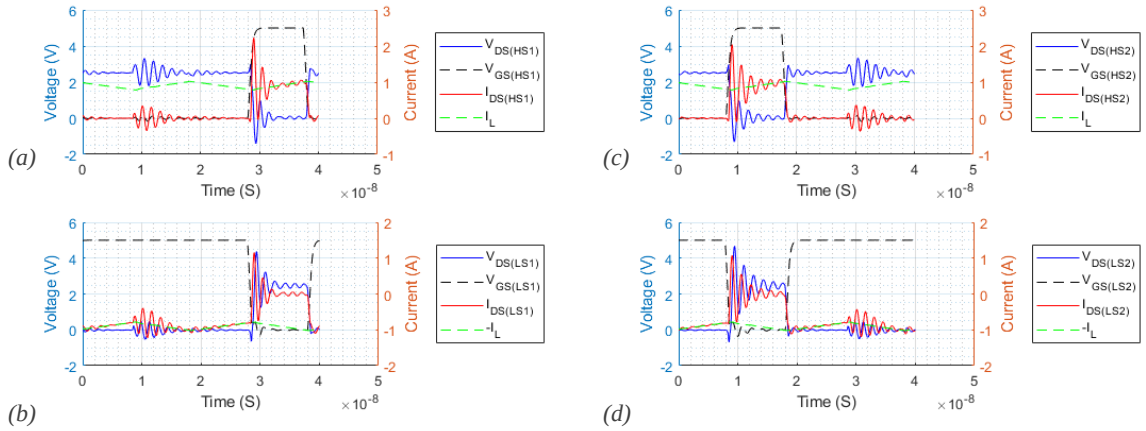


Figure 3.42. (a) Sw_{HS1}, (b) Sw_{LS1}, (c) Sw_{HS2}, and (d) Sw_{LS2} waveforms, for the 3-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the air-core inductor and EPC2040 switch models.

Current and Voltage Waveforms for a 3-level Converter with ne5 Switches

In Figure 3.43 the output voltage waveform and in Figure 3.44 the switch waveforms are shown, for a 3-level buck converter, with *ne5* switches over one period. The converter is operated at $f_{sw} = 25$ MHz, $I_{out} = 1$ A, and $V_{in} = 5$ V. The average $V_{out} = 1.10$ V and $\Delta V_{out} = 8.57$ mV.

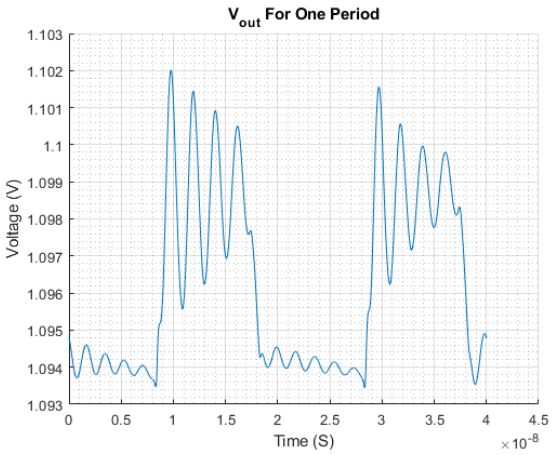


Figure 3.43. V_{out} waveform, for the 3-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the air-core inductor and ne5 switch models.

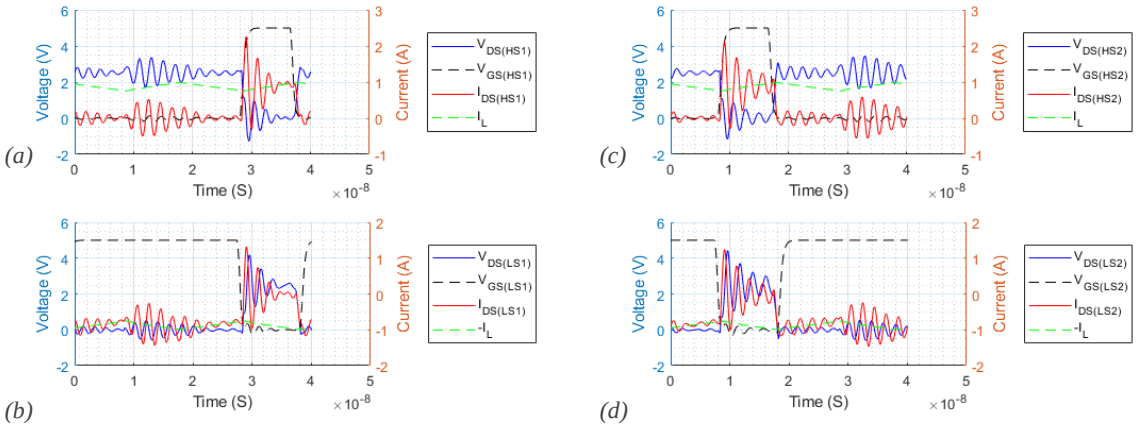


Figure 3.44. (a) Sw_{HS1}, (b) Sw_{LS1}, (c) Sw_{HS2}, and (d) Sw_{LS2} waveforms, for the 3-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the air-core inductor and ne5 switch models.

3.6.3 Buck Converter with Tyndall's TF MoS "*MagPwr*" MS2 inductor

The circuit diagram for the 2-level buck converter is shown in Figure 3.45. It includes the models of the Tyndall's thin-film magnetics, (part no. MS2 fabricated in "*MagPwr*" project), the bootstrap capacitor, the board parasitic inductances, and the Peregrine driver.

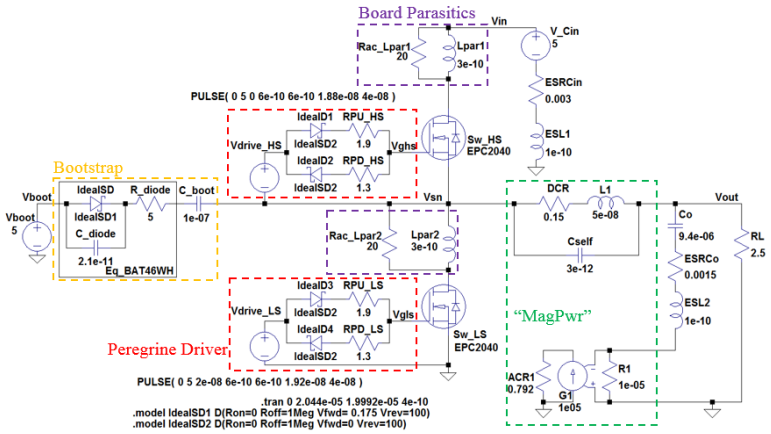


Figure 3.45. Full circuit diagram for the 2-Level buck converter, with the MagPwr inductor, and EPC2040 or ne5 switches.

Current and Voltage Waveforms for a 2-level Converter with EPC2040 Switches

In Figure 3.46, the output voltage and switch waveforms are shown, for a 2-level buck converter, with EPC2040 switches, and over one period. The converter is operated at $f_{sw} = 25$ MHz, $I_{out} = 1$ A, and $V_{in} = 5$ V. The average $V_{out} = 2.29$ V and $\Delta V_{out} = 52.28$ mV.

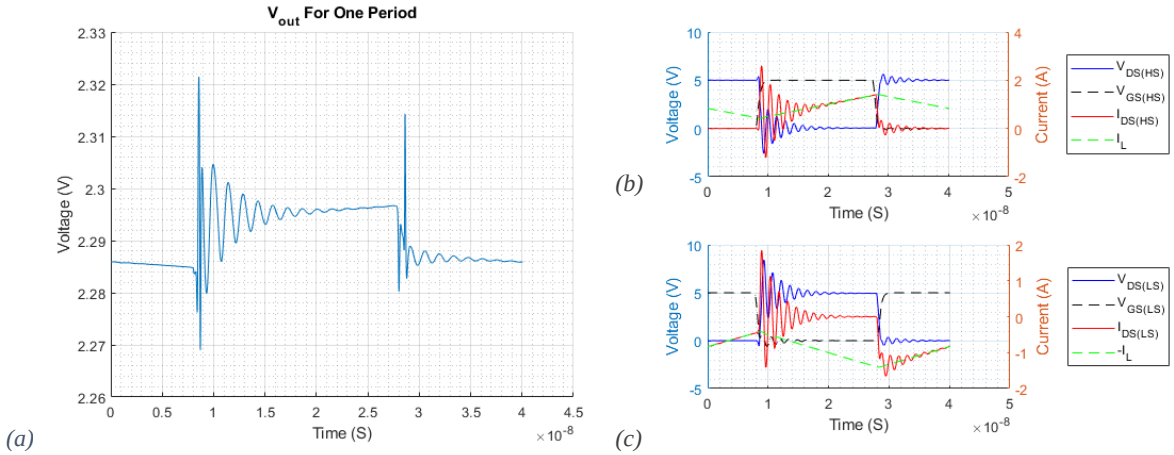


Figure 3.46. (a) V_{out}, (b) Sw_{HS} and (c) Sw_{LS} waveforms, for the 2-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the MagPwr inductor and EPC2040 switch models.

Current and Voltage Waveforms for a 2-level Converter with ne5 Switches

In Figure 3.47, the output voltage and switch waveforms are shown, for a 2-level buck converter, with *ne5* switches, and over one period. The converter is operated at $f_{sw} = 25$ MHz, $I_{out} = 1$ A, and $V_{in} = 5$ V. The average $V_{out} = 2.26$ V and $\Delta V_{out} = 54.21$ mV.

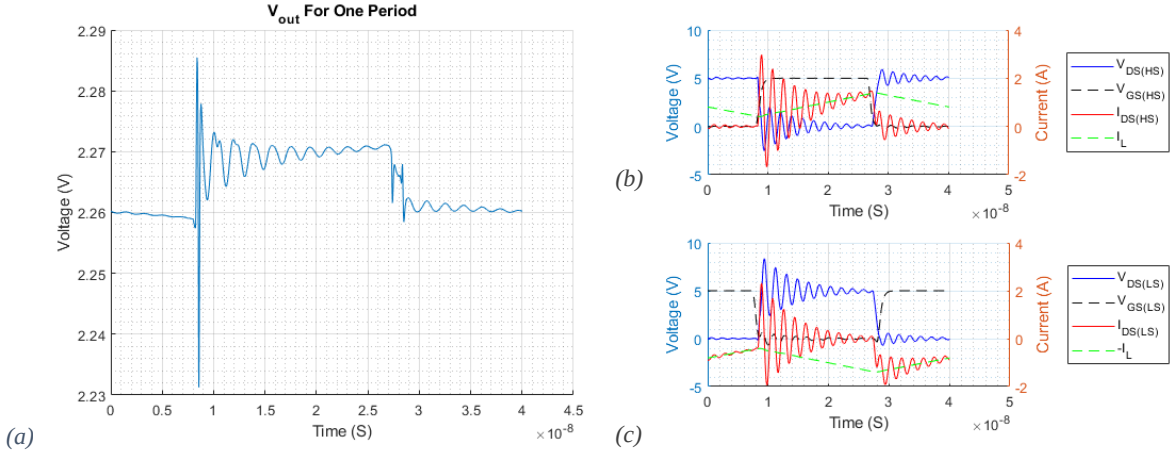


Figure 3.47. (a) V_{out}, (b) Sw_{HS} and (c) Sw_{LS} waveforms, for the 2-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the MagPwr inductor and ne5 switch models.

Current and Voltage Waveforms for a 3-level Converter with EPC2040 Switches

In Figure 3.48, the output voltage waveform and in Figure 3.49, the switch waveforms are shown, for a 3-level buck converter, with EPC2040 switches over one period. The converter is operated at $f_{sw} = 25$ MHz, $I_{out} = 1$ A, and $V_{in} = 5$ V. The average $V_{out} = 1.02$ V and $\Delta V_{out} = 26.69$ mV.

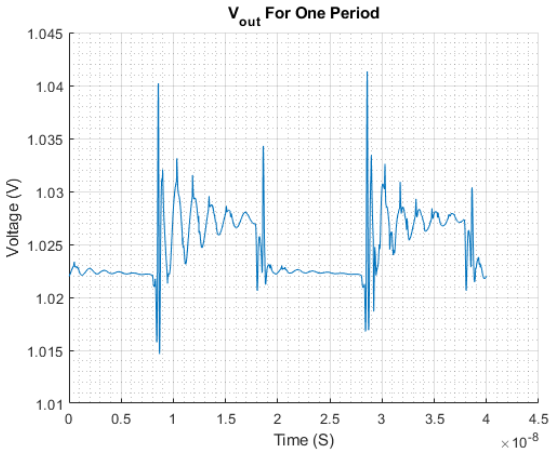


Figure 3.48. V_{out} waveform, for the 3-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the MagPwr inductor and EPC2040 switch models.

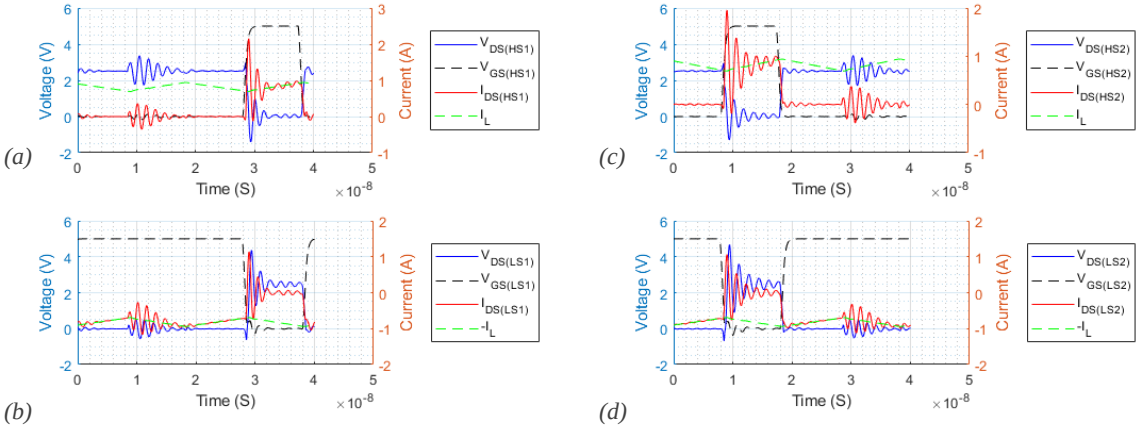


Figure 3.49. (a) Sw_{HS1}, (b) Sw_{LS1}, (c) Sw_{HS2}, and (d) Sw_{LS2} waveforms, for the 3-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the MagPwr inductor and EPC2040 switch models.

Current and Voltage Waveforms for a 3-level Converter with ne5 Switches

In Figure 3.50, the output voltage waveform and in Figure 3.51, the switch waveforms are shown, for a 3-level buck converter, with *ne5* switches over one period. The converter is operated at $f_{sw} = 25$ MHz, $I_{out} = 1$ A, and $V_{in} = 5$ V. The average $V_{out} = 0.99$ V and $\Delta V_{out} = 31.03$ mV.

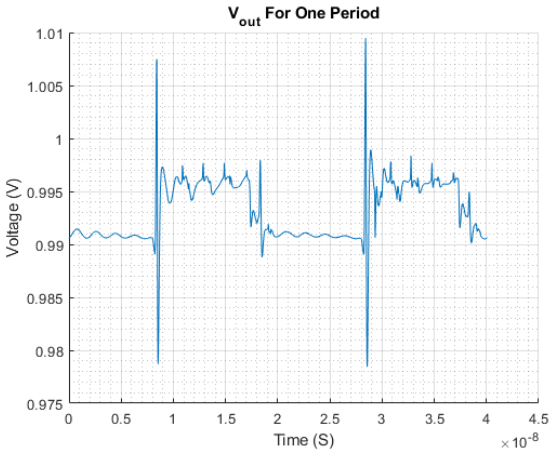


Figure 3.50. V_{out} waveform, for the 3-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the MagPwr inductor and ne5 switch models.

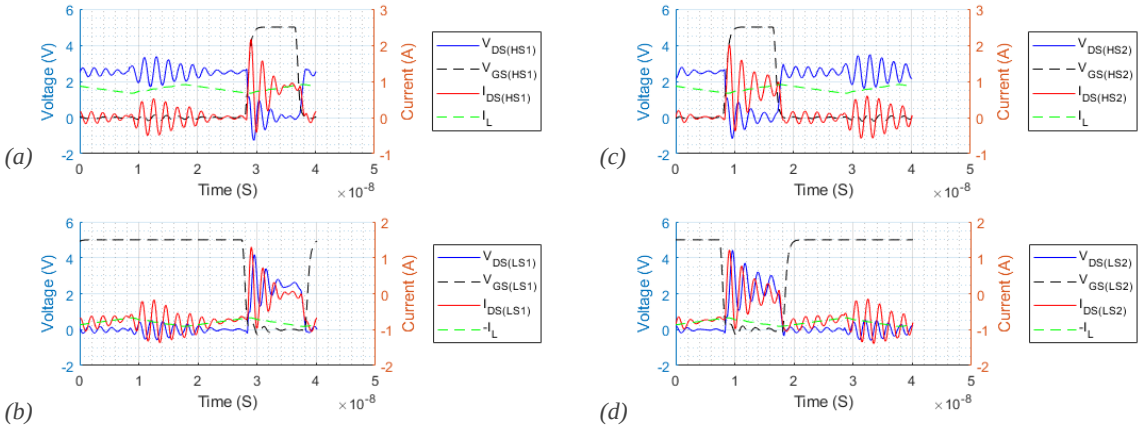


Figure 3.51. (a) Sw_{HS1}, (b) Sw_{LS1}, (c) Sw_{HS2}, and (d) Sw_{LS2} waveforms, for the 3-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the MagPwr inductor and ne5 switch models.

3.6.4 Buck Converter with Coilcraft PFL1005 Inductor

The circuit diagram for the 2-level buck converter is shown in Figure 3.52. It includes the models of the Coilcraft PFL1005 inductor, the bootstrap capacitor, the board parasitic inductances, and the Peregrine driver.

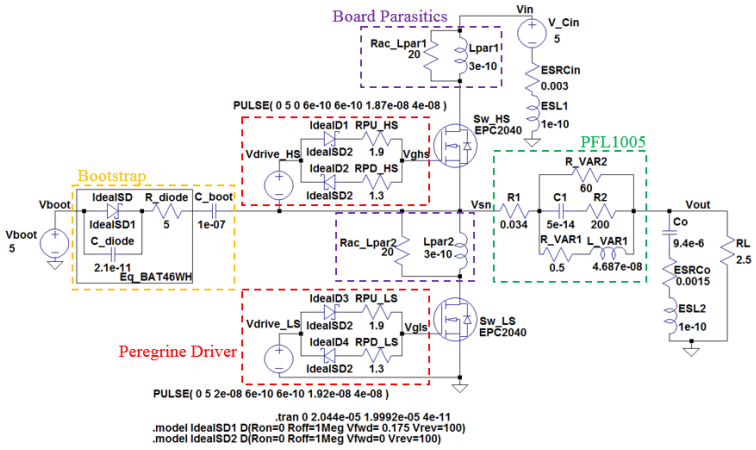


Figure 3.52. Full circuit diagram for the 2-Level buck converter, with the PFL1005 inductor, and EPC2040 or ne5 switches.

Current and Voltage Waveforms for a 2-level Converter with EPC2040 Switches

In Figure 3.53, the output voltage and switch waveforms are shown, for a 2-level buck converter, with EPC2040 switches, over one period. The converter is operated at $f_{sw} = 25$ MHz, $I_{out} = 1$ A, and $V_{in} = 5$ V. The average $V_{out} = 1.98$ V and $\Delta V_{out} = 46.02$ mV.

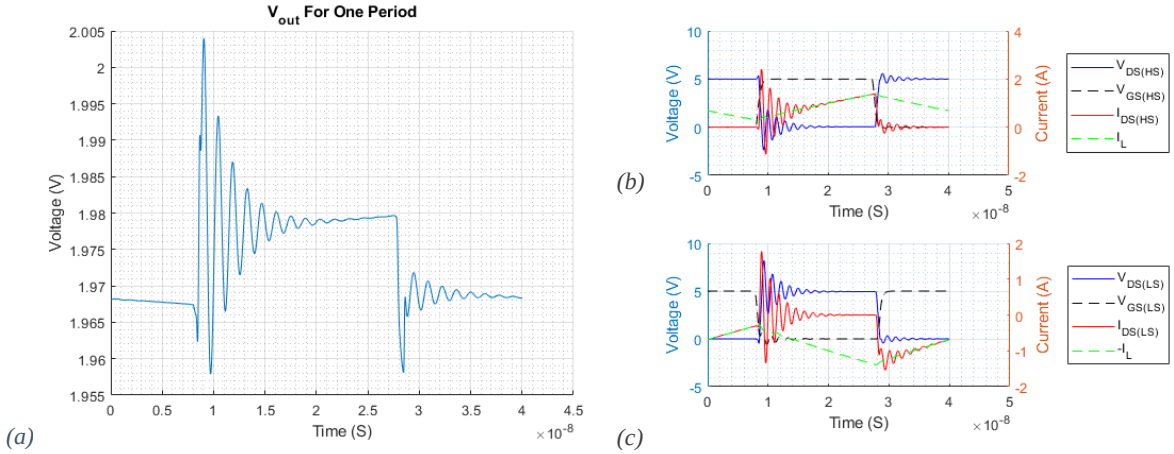


Figure 3.53. (a) V_{out}, (b) Sw_{HS}, and (c) Sw_{LS} waveforms, for the 2-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the PFL1005 inductor and EPC2040 switch models.

Current and Voltage Waveforms for a 2-level Converter with ne5 Switches

In Figure 3.54, the output voltage and switch waveforms are shown, for a 2-level buck converter, with *ne5* switches, and over one period. The converter is operated at $f_{sw} = 25$ MHz, $I_{out} = 1$ A, and $V_{in} = 5$ V. The average $V_{out} = 1.96$ V and $\Delta V_{out} = 37.04$ mV.

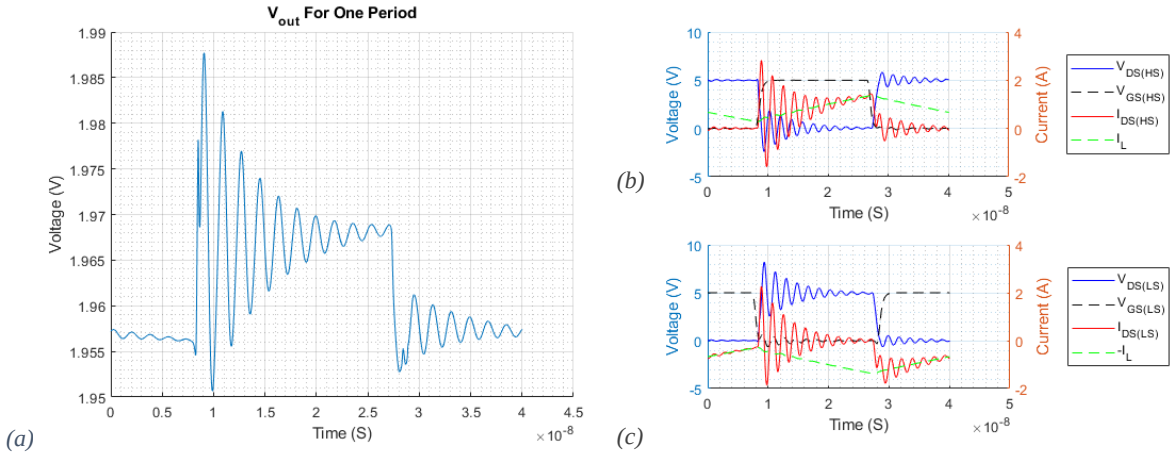


Figure 3.54. (a) V_{out}, (b) Sw_{HS} and, (c) Sw_{LS} waveforms, for the 2-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the PFL1005 inductor and ne5 switch models.

Current and Voltage Waveforms for a 3-level Converter with EPC2040 Switches

In Figure 3.55, the output voltage waveform and in Figure 3.56 the switch waveforms are shown, for a 3-level buck converter, with EPC2040 switches, and over one period. The converter is operated at $f_{sw} = 25$ MHz, $I_{out} = 1$ A, and $V_{in} = 5$ V. The average $V_{out} = 0.73$ V and $\Delta V_{out} = 19.21$ mV.

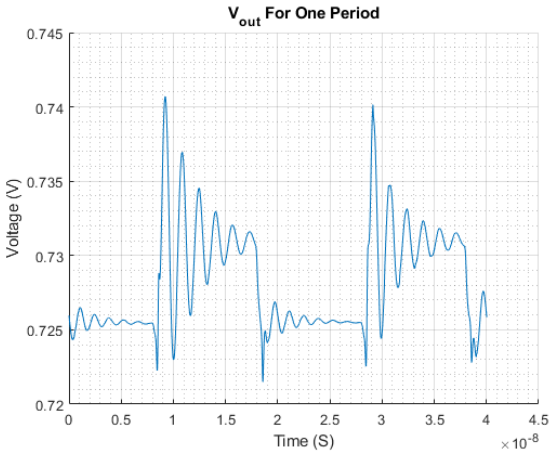


Figure 3.55. V_{out} waveform, for the 3-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With PFL1005 inductor and EPC2040switch models.

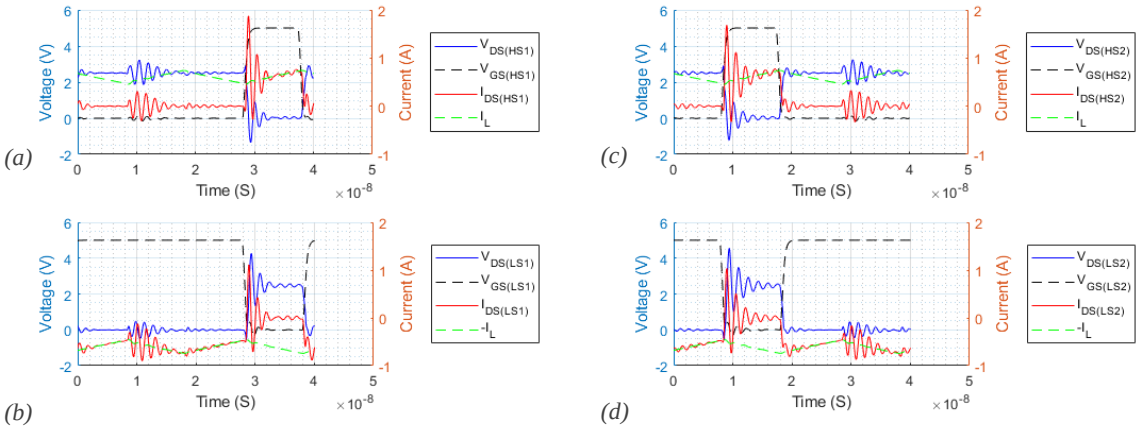


Figure 3.56. (a) Sw_{HS1}, (b) Sw_{LS1}, (c) Sw_{HS2}, and (d) Sw_{LS2} waveforms, for the 3-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the PFL1005 inductor and EPC2040switch models.

Current and Voltage Waveforms for a 3-level Converter with ne5 Switches

In Figure 3.57, the output voltage waveform and the switch waveforms are shown, for a 3-level buck converter, with *ne5* switches over one period. The converter is operated at $f_{sw} = 25$ MHz, $I_{out} = 1$ A, and $V_{in} = 5$ V. The average $V_{out} = 0.71$ V and $\Delta V_{out} = 14.65$ mV.

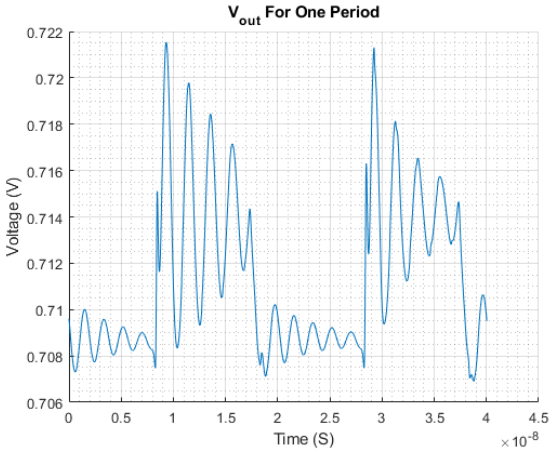


Figure 3.57. The V_{out} waveform, for 3-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With PFL1005 inductor and ne5 switch models.

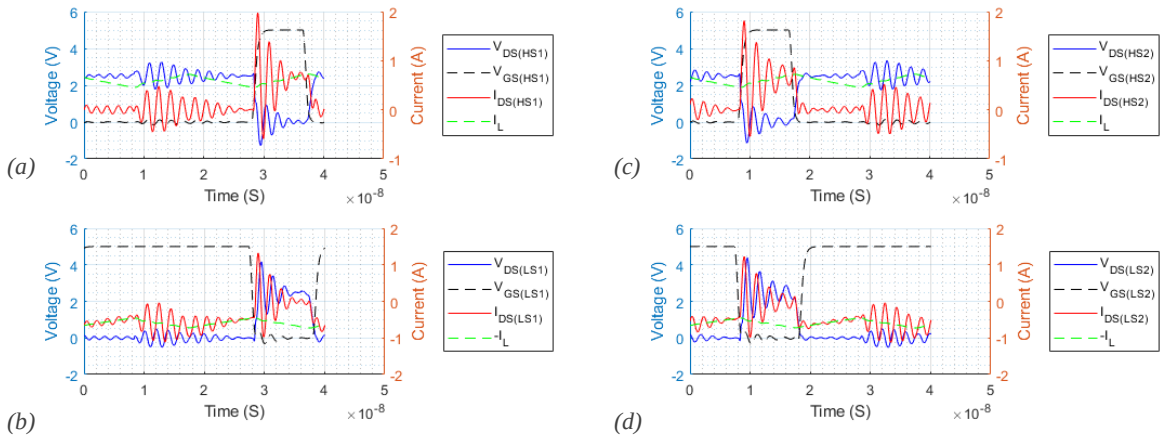


Figure 3.58. (a) Sw_{HS1}, (b) Sw_{LS1}, (c) Sw_{HS2}, and (d) Sw_{LS2} waveforms, for the 3-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With PFL1005 inductor and ne5 switch models.

3.6.5 Buck Converter with Murata LQW18CN55NJ00 Inductor

The circuit diagram for the 2-level buck converter is shown in Figure 3.59. It includes the models of the Murata LQW18CN55NJ00 inductor, the bootstrap capacitor, the board parasitic inductances, and the Peregrine driver.

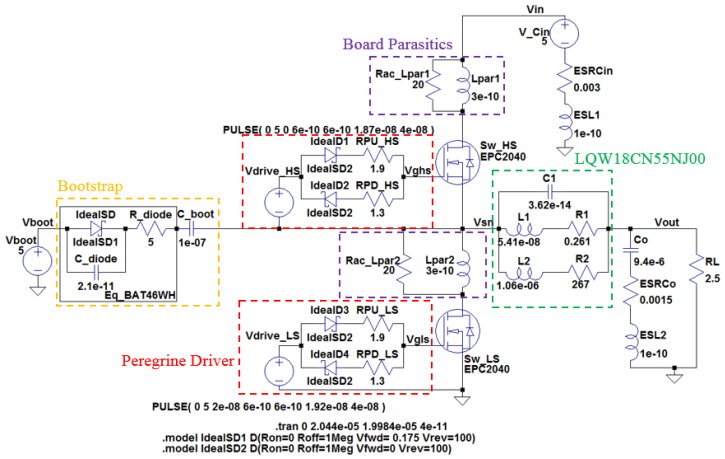


Figure 3.59. Full circuit diagram for the 2-Level buck converter, with the LQW18CN55NJ00 inductor, and EPC2040 or ne 5 switches.

Current and Voltage Waveforms for a 2-level Converter with EPC2040 Switches

In Figure 3.60, the output voltage and switch waveforms are shown, for a 2-level buck converter, with EPC2040 switches over one period. The converter is operated at $f_{sw} = 25$ MHz, $I_{out} = 1$ A, and $V_{in} = 5$ V. The average $V_{out} = 2.19$ V and $\Delta V_{out} = 16.56$ mV.

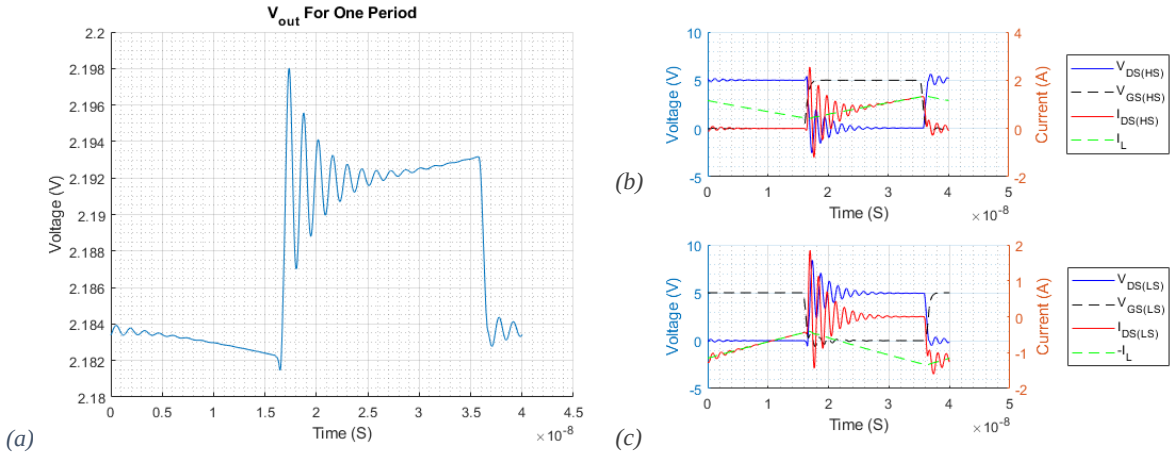


Figure 3.60. (a) V_{out}, (b) Sw_{HS} and, (c) Sw_{LS} waveforms, for the 2-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the LQW18CN55NJ00 inductor and EPC2040 switch models.

Current and Voltage Waveforms for a 2-level Converter with ne5 Switches

In Figure 3.61, the output voltage and switch waveforms are shown, for a 2-level buck converter, with *ne5* switches over one period. The converter is operated at $f_{sw} = 25$ MHz, $I_{out} = 1$ A, and $V_{in} = 5$ V. The average $V_{out} = 2.18$ V and $\Delta V_{out} = 16.02$ mV.

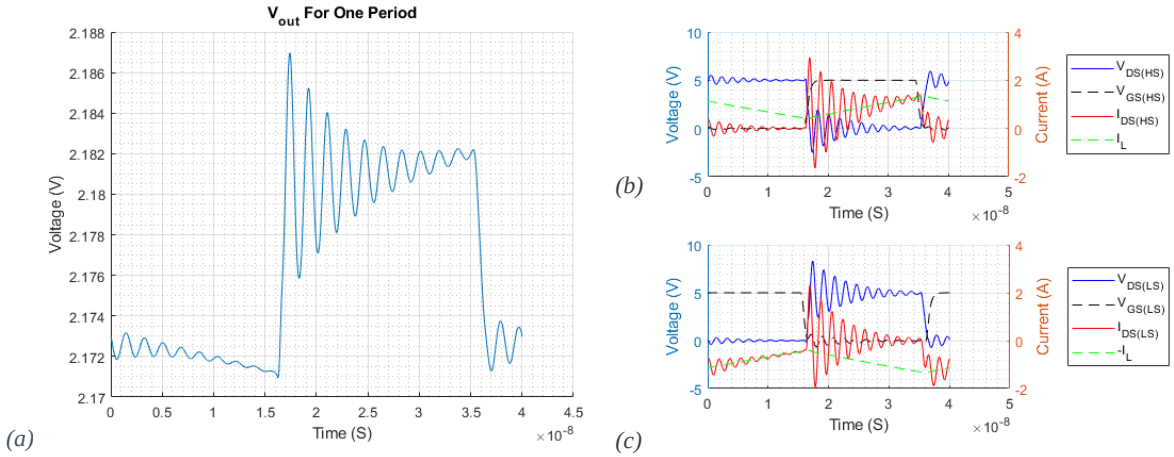


Figure 3.61. (a) V_{out}, (b) Sw_{HS} and, (c) Sw_{LS} waveforms, for 2-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the LQW18CN55NJ00 inductor and ne5 switch models.

Current and Voltage Waveforms for 3-level Converter with EPC2040 Switches

In Figure 3.62, the output voltage waveform and in Figure 3.63, the switch waveforms are shown, for a 3-level buck converter, with EPC2040 switches over one period. The converter is operated at $f_{sw} = 25$ MHz, $I_{out} = 1$ A, and $V_{in} = 5$ V. The average $V_{out} = 0.94$ V and $\Delta V_{out} = 9.23$ mV.

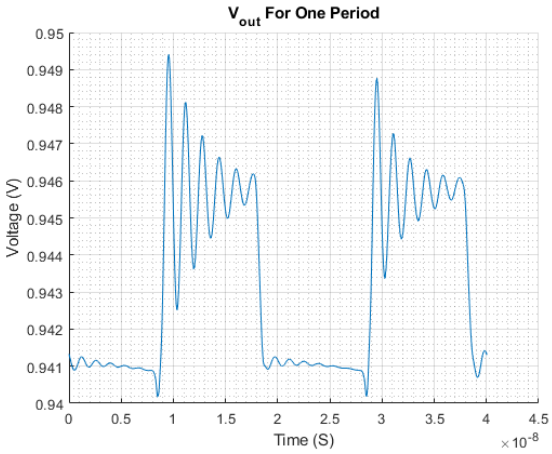


Figure 3.62. V_{out} waveform, for 3-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With LQW18CN55NJ00 inductor and EPC2040 switch models.

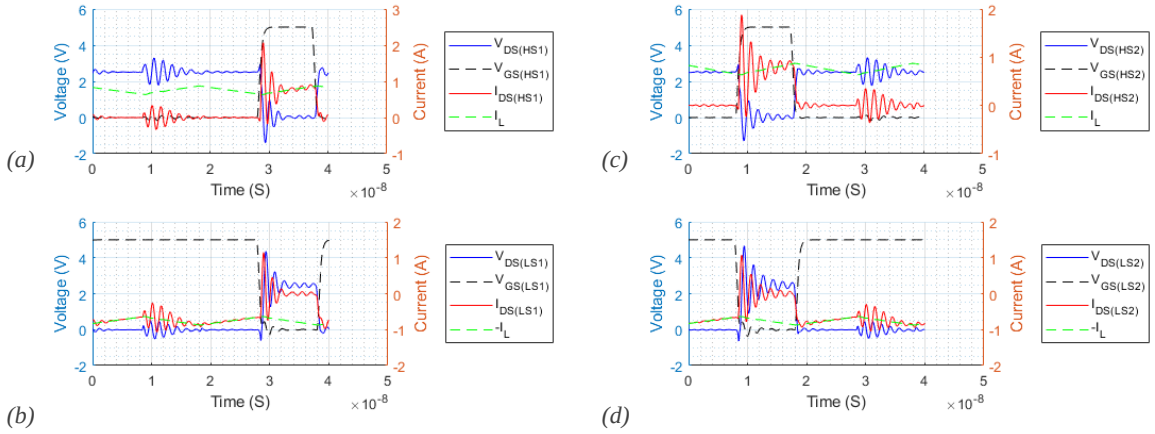


Figure 3.63. (a) Sw_{HS1}, (b) Sw_{LS1}, (c) Sw_{HS2}, and (d) Sw_{LS2} waveforms, for 3-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the LQW18CN55NJ00 inductor and EPC2040 switch models.

Current and Voltage Waveforms for a 3-level Converter with ne5 Switches

In Figure 3.64, the output voltage waveform and in Figure 3.65, the switch waveforms are shown, for a 3-level buck converter, with *ne5* switches over one period. The converter is operated at $f_{sw} = 25$ MHz, $I_{out} = 1$ A, and $V_{in} = 5$ V. The average $V_{out} = 0.99$ V and $\Delta V_{out} = 9.34$ mV.

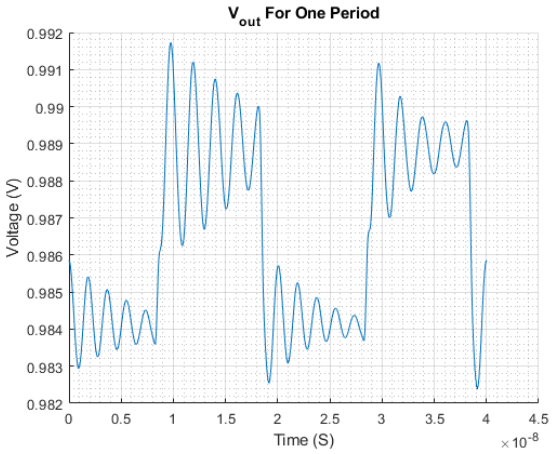


Figure 3.64. V_{out} waveform, for 3-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the LQW18CN55NJ00 inductor and ne5 switch models.

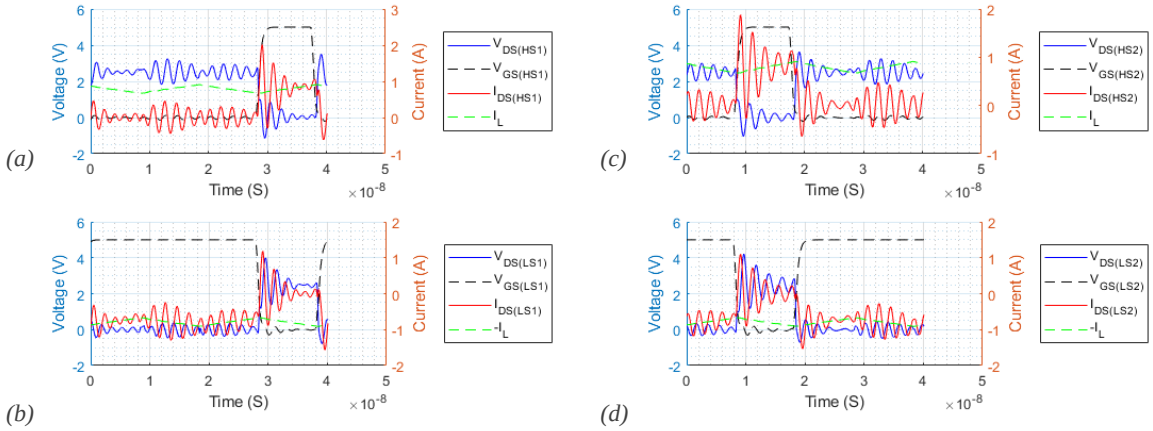


Figure 3.65. (a) Sw_{HS1}, (b) Sw_{LS1}, (c) SwHS2, and (d) SwLS2 waveforms, for 3-level buck converter, at f_{sw} = 25 MHz, I_{out} = 1 A. With the LQW18CN55NJ00 inductor and ne5 switch models.

3.6.6 Analysis

Analysing the graphs, the converters with *ne5* switches have smaller damping ratios than the EPC2040 converters. As r_{on} is the same for both switches this implies that the extra ringing on the ne5 switches is due to them having higher capacitances.

Table 3.8 shows the average values of V_{out} for each of the converters, as well as an estimated efficiency. For 100% efficient converters, the 2-level converter would have an average output voltage of 2.5 V, and the 3-level converter would have an average output voltage of 1.25 V. The simulated V_{out} was divided by the ideal V_{out} to give estimated efficiency. The converters with EPC2040 switches have a higher V_{out} and efficiency than the *ne5* equivalents, except for the 3-level converters with LQW inductors. The highest efficiency inductors in order are; the *air-core*, the "*MagPwr*", the LQW, and the PFL. The 2-level converter is more efficient than the 3-level converter but note that the same switching frequency is used throughout.

Vout (V)	Air-Core	"MagPwr"	PFL	LQW	Efficiency	Air-Core	"MagPwr"	PFL	LQW
2-level EPC	2.42	2.29	1.98	2.19	2-level EPC	96.8%	91.6%	79.2%	87.6%
2-level ne5	2.398	2.26	1.96	2.18	2-level ne5	95.9%	90.4%	78.4%	87.2%
3-level EPC	1.13	1.02	0.73	0.94	3-level EPC	90.4%	81.6%	58.4%	75.2%
3-level ne5	1.1	0.99	0.71	0.99	3-level ne5	88.0%	79.2%	56.8%	79.2%

Table 3.8. The simulated average V_{out} values for all the converters, and their estimated efficiencies.

Table 3.9 shows the values for ΔV_{out} for each of the converters. Note that the voltage ripple includes the converter noise. The table also shows the voltage ripple ratio (ΔV_{rr}) the ratio of $\Delta V_{out}/V_{out}$. The converters with *ne5* switches have a lower ΔV_{out}, except for the converter with a "*MagPwr*" inductor. The 3-level converters have lower ΔV_{out}, except for the converter with a "*MagPwr*" inductor. The convers with LQW inductors had similar ΔV_{out} compared to the converters with *air-core* inductors, but it also had a lower V_{out}; thus it's ΔV_{rr} is larger than the *air-core*'s. The converters with *air-core* and LQW inductors have much smaller ΔV_{rr} than the converters with PFL and "*MagPwr*" inductors. The converters with "*MagPwr*" inductors have slightly smaller ΔV_{rr} than the converters with PFL inductors, when the converters are 2-level, but the opposite is true for 3-level converters with the converters with "*MagPwr*" inductors having much larger ΔV_{rr}.

ΔVout (mV)	Air-Core	"MagPwr"	PFL	LQW	ΔVrr	Air-Core	"MagPwr"	PFL	LQW
2-level EPC	16.83	52.28	46.02	16.56	2-level EPC	0.70%	2.28%	2.32%	0.76%
2-level ne5	15.99	54.21	37.04	16.02	2-level ne5	0.67%	2.40%	1.89%	0.73%
3-level EPC	9.44	26.69	19.21	9.23	3-level EPC	0.84%	2.62%	2.63%	0.98%
3-level ne5	8.57	31.03	14.65	9.34	3-level ne5	0.78%	3.13%	2.06%	0.94%

Table 3.9. The voltage ripple values for all the converters, relative ripple ratio values.

3.7 Breakdown of Switch Losses – Simulated in LTSpice

This section will review the methodology for splitting the total loss each switch over one period into its various different components. The loss components are: Sw_{HS} turn-on loss $P_{on(HS)}$, Sw_{HS} turn-off loss $P_{off(HS)}$, Sw_{HS} conduction loss $P_{con(HS)}$, Sw_{HS} gate loss $P_{gate(HS)}$, Sw_{LS} fall time loss $P_{d(H-L)}$, Sw_{HS} 3rd quadrant conduction loss $P_{3rdQ(LS)}$, Sw_{LS} rise time (turn off) loss $P_{d(L-H)}$, Sw_{LS} conduction loss $P_{con(LS)}$, and Sw_{LS} gate loss $P_{gate(LS)}$.

It is assumed that the converter is always operated in CCM, that I_L is always positive and, that Sw_{LS} is turned on/off with (or close to) ZVS. During Sw_{HS} turn-off and when the channel is closed $C_{oss(HS)}$ is charged (this energy is lost during Sw_{HS} turn-on) and $C_{oss(LS)}$ is discharged (recovered) through the inductor. Figure 3.66 shows Sw_{HS} and Sw_{LS} waveforms: V_{DS}, V_{GS}, I_{DS}, and I_L, for the 2-level synchronous buck converter, with the PFL1005 inductor, EPC2040 switches, and PCB parasitic inductances included. The two main time intervals have been highlighted, firstly the interval between Sw_{LS} turn-off and Sw_{HS} turn-on, and secondly the interval between Sw_{HS} turn-off and Sw_{LS} turn-on.

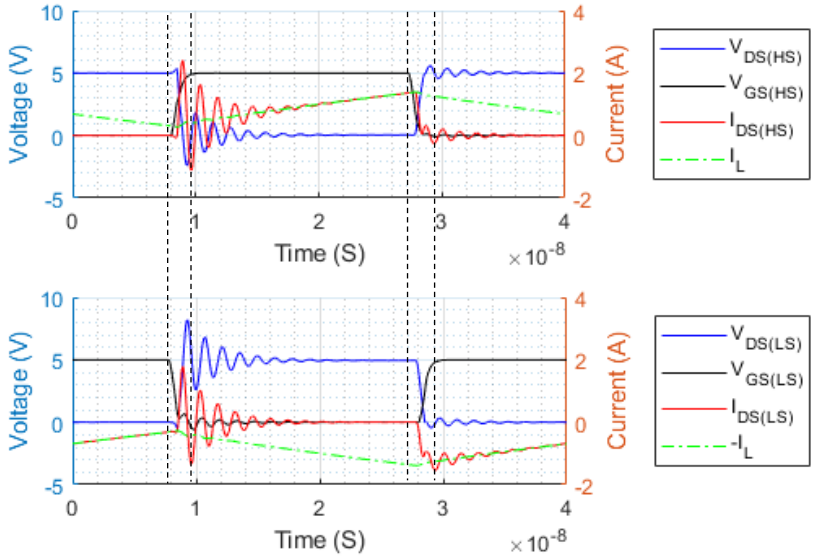


Figure 3.66. The switch waveforms for the 2-level buck converter with a PFL inductor and EPC2040 switches. Operated at f_{sw}=25 MHz, I_{out}=1 A, for one period.

3.7.1 LS Turn-Off, HS Turn-On, Dead Time ($t_{d(L-H)}$)

This section will detail the time interval between Sw_{LS} turn-off and Sw_{HS} turn-on, the dead time referred to as $t_{d(L-H)}$. Figure 3.67 shows the switch waveforms during the time interval of interest, the graph is for a 2-level converter, with a PFL inductor and EPC2040 switches, operated at $f_{sw} = 25$ MHz and $I_{out} = 1$ A. Table 3.10 details how MATLAB finds the time points and the relevance of each in separating loss components, the time labels are written as they appear in the MATLAB code, the MATLAB marker is to assist the code in finding other points.

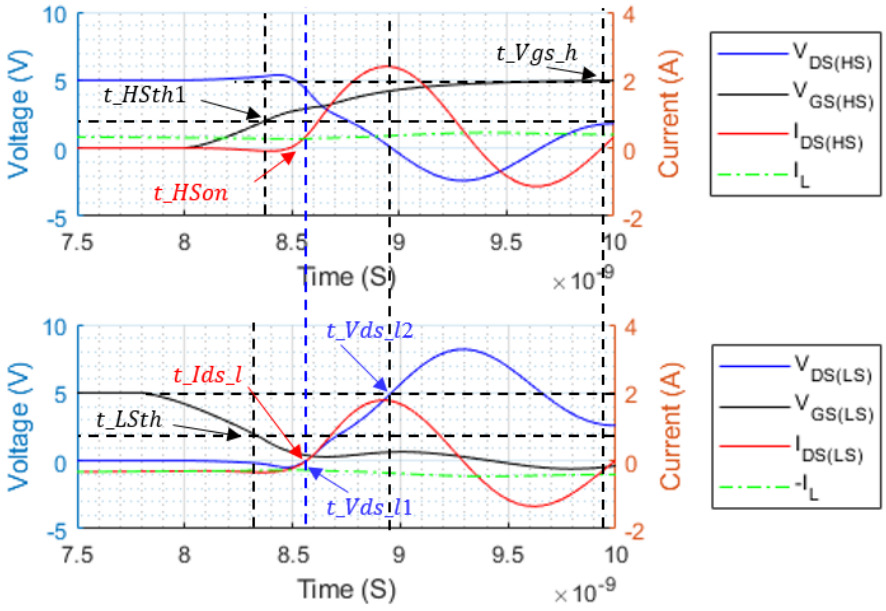


Figure 3.67. Sw_{LS} turn-off and Sw_{HS} turn-on waveforms.
For the 2-level buck converter with a PFL inductor and EPC2040 switches. Operated at f_{sw}=25 MHz, I_{out}=1 A.

Note in Figure 3.67 Sw_{LS} turns off with zero voltage and hence there is no discernible miller plateau.

Time Point Label	Identifying Condition	Relevance of Time Point
t_LSth	$V_{GS(LS)}$ falls to V_{th}	End of Sw_{LS} conduction. Start of Sw_{LS} $t_{d(L-H)}$ loss. Start Diode/3rd quadrant conduction.
t_Ids_l	$I_{DS(LS)}$ rises to 0 A	End of Diode/3rd quadrant conduction. Start of diode/3rd quadrant recovery.
t_HSth1	$V_{GS(HS)}$ rises to V_{th} $I_{DS(HS)}$ rises to 0 A	Start of Sw_{HS} turn-on loss
t_Vds_l1	$V_{DS(LS)}$ rises to 0 V	Diode/3rd quadrant conduction reaches I_{RRM}. Start of $C_{oss(LS)}$ charging through Sw_{HS}.
t_Vds_l2	$V_{DS(LS)}$ rises to V_{in} (V_{in}/2 for 3-level)	End of $C_{oss(LS)}$ charging.
t_Vgs_HS1	$V_{GS(HS)}$ rises to 99% *V_{driver}	MATLAB marker.

Table 3.10. MATLAB time markers, the conditions to identify them, and the relevance to separating loss components.

3.7.2 HS Turn-Off, LS Turn-On, Dead Time ($t_{d(H-L)}$)

This section will detail the time interval between Sw_{HS} turn-off and Sw_{LS} turn-on, the dead time referred to as $t_{d(H-L)}$. Figure 3.68 shows the switch waveforms during the time interval of interest, the graph is for a 2-level converter, with a PFL inductor and EPC2040 switches, operated at $f_{sw} = 25$ MHz and $I_{out} = 1$ A. Table 3.11 details how MATLAB finds the time points and the relevance of each in separating loss components, the time labels are written as they appear in the MATLAB code, the MATLAB marker is to assist the code in finding other points.

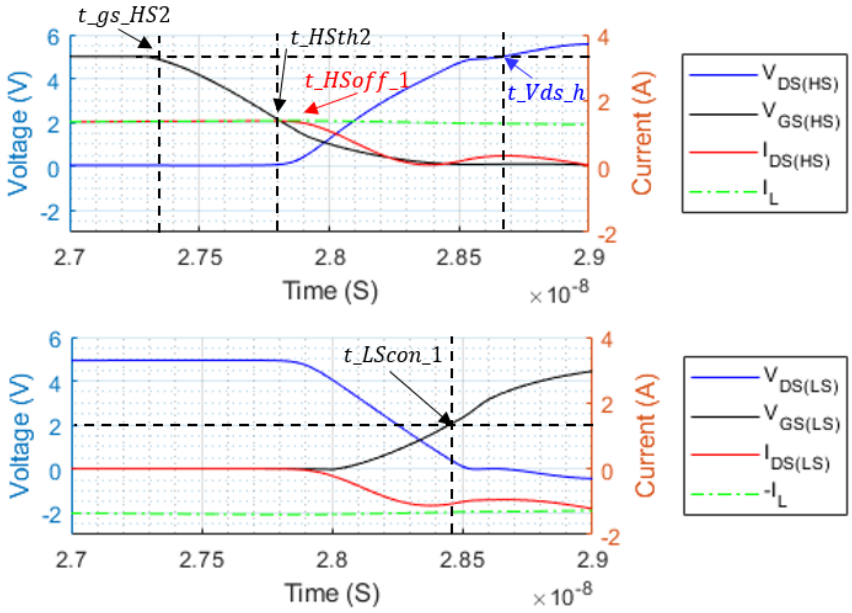


Figure 3.68. Sw_{HS} turn-off and Sw_{LS} turn-on waveforms.
For the 2-level buck converter with a PFL inductor and EPC2040 switches. Operated at f_{sw}=25 MHz, I_{out}=1 A.

Time Point Label	Identifying Condition	Relevance of Time Point
t_Vgs_HS2	$V_{GS(HS)}$ falls to 99% of V_{driver}	MATLAB marker.
t_HSoff_1	$I_{DS(HS)} = I_L$	$I_{DS(HS)}$ in the channel at its maximum. End of Sw_{HS} conduction loss. Start of Sw_{HS} turn off loss.
t_HSth2	$V_{GS(HS)}$ falls to V_{th}	Sw_{HS} channel current is off.
t_ds_h	$V_{DS(HS)}$ rises above V_{in} ($V_{in}/2$ for 3-level)	End of Sw_{HS} turn off loss. Start of Sw_{LS} dead time loss. Switch-node falls to 0 V. As $V_{DS(HS)}$ rises there is some charging through C_{DG} onto C_{GS}.
t_LScon_1	Sw_{LS} rises to V_{th}	End of Sw_{LS} rise time loss. Start of Sw_{LS} conduction loss.

Table 3.11. MATLAB time markers, the conditions to identify them, and the relevance to separating loss components.

3.7.3 Simulated Switch Waveforms Incorporated in MATLAB Code

The waveforms shown in the previous two sections are typical for all of the converters and will only change slightly according to inductor model, switch models, or buck-level count. LTSpice gives current and voltage waveform data sets in the form of arrays with small time-steps between each value. These arrays are extracted into MATLAB. By using averaged numeric integration, the total loss in the switches for one period is calculated, as detailed below.

For the arrays $n = 1$ is the first value ($t = 0\ s$), and $n = N$ is the final value ($t = T_{sw}$). The code starts by finding the average of each consecutive value in the voltage and current arrays, these averaged values are put into new arrays V_{avg} and I_{avg} respectively:

$$V_{avg}(n) = \frac{V(n)+V(n+1)}{2} \quad (3.15)$$

and

$$I_{avg}(n) = \frac{I(n)+I(n+1)}{2} \quad (3.16)$$

this should be done for the source, drain, and gate for each switch. Next the code finds the time difference between each of these averaged values:

$$\Delta t(n) = t(n+1) - t(n) \quad (3.17)$$

there is a single time array for all the voltage and current arrays. The code numerically integrates the current and voltage to get the energy, then the code multiplies the energy by the f_{sw} to get the power loss, for example the gate power loss is:

$$P_{gate} = f_{sw} \sum_{n=1}^{N+1} \left(V_{G_{avg}}(n) I_{G_{avg}}(n) \Delta t(n) \right). \quad (3.18)$$

The code does this numeric integration for each the source, the drain, and the gate. The code combines the three power losses to get the total switch loss for one period. The code also keeps the total gate loss for one period separate and combines the drain and source losses:

$$P_{sw(DS(total))} = P_{Source} + P_{drain}. \quad (3.19)$$

The methodology used in this thesis is to split this total drain-source loss into the constituent intervals as outlined in the previous two sections and in the correct sequence. It is important to note that the simulations are set up in a way whereby Sw_{LS} turn-off is the starting point. Two periods are simulated after steady-state has been achieved, to ensure adequately accurate data to properly compute losses over the full period.

3.7.4 Circuit Board Parasitic Ringing

This section will briefly describe the effect of circuit board parasitic inductances and the resulting high frequency ringing. This ringing is caused by PCB traces form capacitors and inductors. The resultant ringing is observable on the voltage waveforms, and the simulations all have packaging inductances added to them to model these effects.

This section will show the ringing effects added to the waveforms, the ringing waveforms are shown in Figure 3.69, the methodology to separate them from the current and voltage waveforms is described below.

After Sw_{HS} turns on: without ringing $I_{DS(HS)}(t)$ would equal $I_L(t)$, thus the current flowing through Sw_{HS} at this time is $I_L(t)$ plus the parasitic ringing current, $I_{DS(HS)Ringing}(t) = I_{DS(HS)}(t) - I_L(t)$; without ringing $V_{DS(HS)}$ would equal $V_{on(HS)}$, thus the ringing voltage is $V_{DS(HS)Ringing}(t) = V_{DS(HS)}(t) - V_{on(HS)}$. The ringing waveforms are shown in Figure 3.69 (a).

After Sw_{HS} turns on: without ringing $I_{DS(LS)}(t)$ would equal 0 A, thus all of the current flowing through Sw_{LS} at this time is parasitic ringing current, $I_{DS(LS)Ringing}(t) = I_{DS(LS)}(t)$; without ringing $V_{DS(LS)}$ would equal V_{in}, thus the ringing voltage is $V_{DS(LS)Ringing}(t) = V_{DS(LS)}(t) - V_{in}$. The ringing waveforms are shown in Figure 3.69 (b).

After Sw_{HS} turns off: without ringing $I_{DS(HS)}(t)$ would equal 0 A, thus all of the current flowing through Sw_{HS} at this time is parasitic ringing current, $I_{DS(HS)Ringing}(t) = I_{DS(HS)}(t)$; without ringing $V_{DS(HS)}(t)$ would equal V_{in}, thus the ringing voltage is $V_{DS(HS)Ringing}(t) = V_{DS(HS)}(t) - V_{in}$. The ringing waveforms are shown in Figure 3.69 (c).

After Sw_{HS} turns off: without ringing $I_{DS(LS)}(t)$ would equal $I_L(t)$, thus the current flowing though Sw_{LS} at this time is $I_L(t)$ plus the parasitic ringing current, $I_{DS(LS)Ringing}(t) = I_{DS(LS)}(t) - I_L(t)$. ; without ringing $V_{DS(LS)}(t)$ would equal $V_{on(LS)}$, thus the ringing voltage is $V_{DS(LS)Ringing}(t) = V_{DS(LS)}(t) - V_{on(LS)}$. The ringing waveforms are shown in Figure 3.69 (d).

To ensure accurate V_{on} values, the voltages and currents of both switches are measured simultaneously just before the switch begins to turn off. It is assumed that V_{in} is constant.

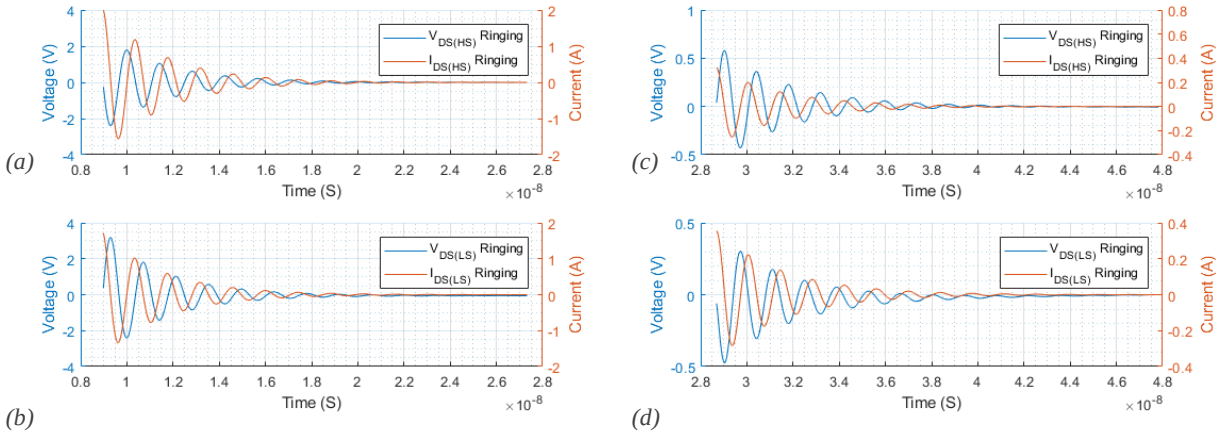


Figure 3.69. The current and voltage ringing waveforms (a) for Sw_{HS} after Sw_{HS} turns on (b) for Sw_{LS} after Sw_{HS} turns on, (c) for Sw_{HS} after Sw_{HS} turns off, and (d) for Sw_{LS} after Sw_{HS} turns off.

4. Open Switch-Node Measurements and Validating Simulations on 2-Level Buck Converter Prototype

4.1 Introduction to Open Switch-Node Measurements

This chapter examines and characterises the driver waveforms and switching bridge performance, for the case of open-circuit switch-node (no inductor fitted). As there is no inductor current, the inductor, dead-time and conduction losses are not present. This chapter details the measured and simulated results, followed by analysis and comparison. Open-circuit switch-node measurements allow better validation of parameters such as C_{oss} based losses while excluding the capacitance of the inductor and body diode recovery loss.

4.1.1 Measurement Equipment

V_{in} is supplied by a KEYSIGHT B2902A Precision Source/Measure Unit (120 fA 2 ch) which also records the value of I_{in}. I_{Driver} is recorded with a KEITHEY 2100 6 ½ Digit Multimeter. A KEYSIGHT 34461A 6 ½ Digit Multimeter is used to measure average voltage values. The PWM signals are supplied by a KEYSIGHT 33500B Series Waveform Generator. A programmable DC electronic load is used to control the load resistance and output current. The voltage waveforms are measured on a Tektronix MDO3104 Mixed Domain Oscilloscope, using primarily FET Input Active Probes (FET input <1 pF, 1 GHz BW), and when specified with lower bandwidth 500 MHz 8 pF passive probes. For all measurements $V_{Driver} = 5$ V.

4.1.2 Buck Converter Circuit Boards

Three different prototype boards were measured, their serial numbers begin with EPC1, EPC2 and EPC3. The MS2 designation in the serial number denotes the *MagPwr* single phase thin film inductor of size 2. The units have two phases but only one phase of each board was powered and used for measurements. The buck converter circuits measured were EPC1 MS2 phase 1, the EPC2 MS2 phase 1 (Figure 4.1), and EPC3 MS2 phase 2 (underside shown in Figure 4.2). All three boards use EPC2040 switches. In Figure 4.1 the components for one phase are indicated with red letters:(A) the MS2 TF MoS *MagPwr* inductor, (B) the Murata Peregrine-Semi PE29102 driver, (C) the EPC2040 e-HEMT GaN 24mΩ switches, (D) the input capacitors (0306 – low ESL), and (E) the output capacitors (0306 – low ESL).

The EPC2 board was also measured as a full converter (inductor, output capacitor and load connected) and that data is in the following chapter.

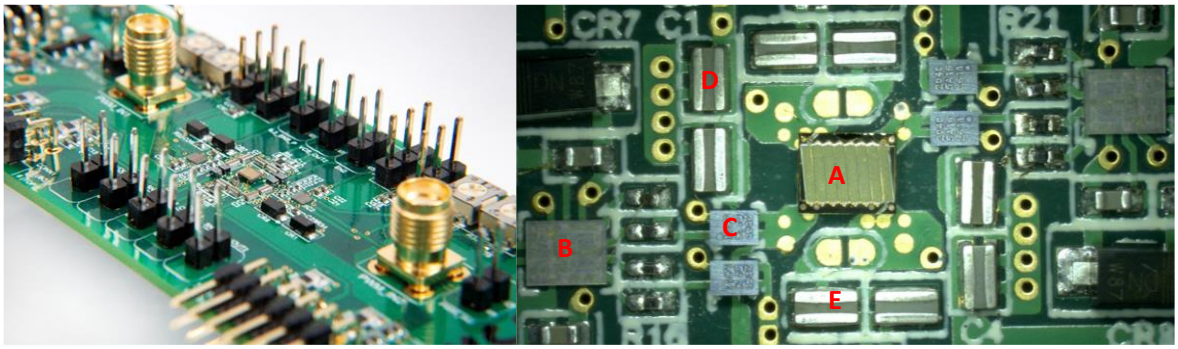


Figure 4.1. Tyndall's "MagPwr", EPC1 MS2 buck converter circuit board.

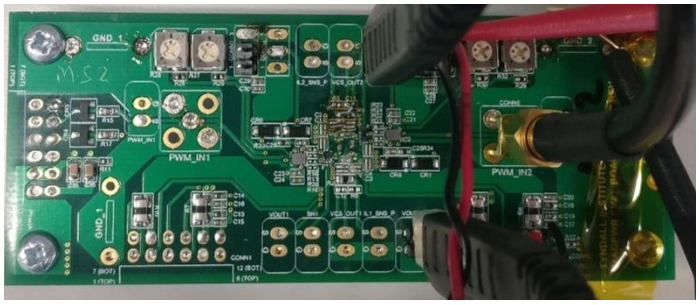


Figure 4.2. Circuit board set-up for later "full-converter" measurements. Inductor device mounted on underside of PCB, EPC3 MS2 circuit board.

4.1.3 Importance of Measurement Points and Scope Probe Ground Lead Set-Up

Figure 4.3 demonstrates the importance of carefully choosing the locations for waveforms measurement on the circuit board, where two identical probes are measuring the same circuit nodes at different points. The "Close Ground Lead" had the 'scope probe ground lead area minimised as much as possible, to reduce stray field pick up from the solenoidal inductors, and the circuit loops. It was grounded at the input decoupling capacitor ground. The "Test Point" measurements were located further away but with the return connected by a ground plane. Stray inductive field pickup (through probe ground loop area) is minimised when using test points and active 'scope probe or direct coaxial connection. The overall shape of V_{sn} waveforms are similar, 0 V when Sw_{HS} is off, 2 V when Sw_{HS} is on, with an increase in voltage as Sw_{HS}turns off. The difference in the parasitic inductance distribution also explains ringing voltage drops; there is more oscillation at the "Close Ground Lead" when Sw_{LS} turns on (stray field pick-up), and more oscillation at the test point when Sw_{HS}turns on (voltage drop difference in the grounding point) due to circuit tracks typically adding 1nH/mm, subject to loop area and causing significant parasitic inductive voltage drop in the primary switching loop as C_{oss} for the low side switch is charged.

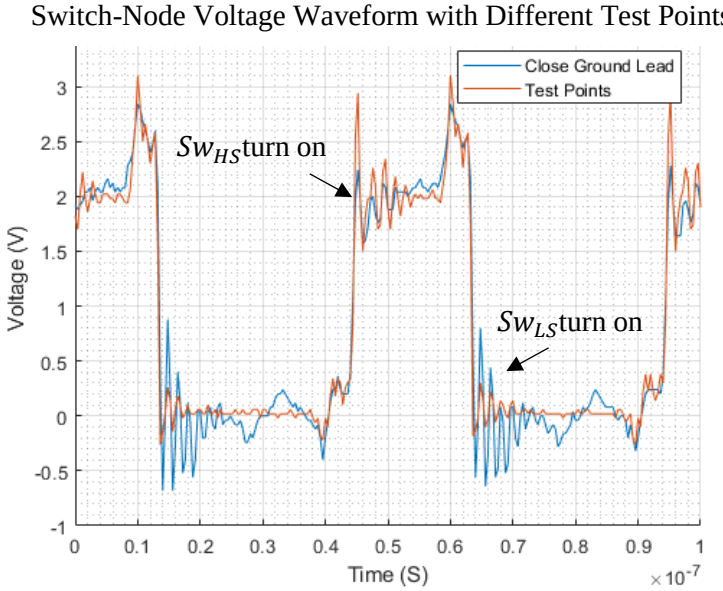


Figure 4.3. V_{sn}, measured with FET Input Probe at Test Point and Passive Probe with Close Ground Lead. EPC1 MS2 buck converter board, open switch-node.

4.2 Open Switch-Node Measurements (No Inductor Fitted)

4.2.1 Switch-Node Voltage Waveforms and Dead-times

Waveforms are recorded during gate driver dead-time trim by potentiometer adjustment. V_{sn} is measured with the Active FET Input probes and the gate voltages are measured with passive probes.

$t_{d(L-H)}$ is the dead-time between Sw_{LS} turn off and Sw_{HS} turn on, and $t_{d(H-L)}$ is the dead-time between Sw_{HS} turn off and Sw_{LS} turn on.

Figure 4.4 shows the voltage waveforms for the EPC1 board, the converter is operated at $f_{sw} = 20$ MHz, $D = 0.33$, and V_{in} is o/c, the dead-times are $t_{d(L-H)} \approx 4.9$ ns and $t_{d(H-L)} \approx 3.6$ ns. All measurements on this board use the same dead-times.

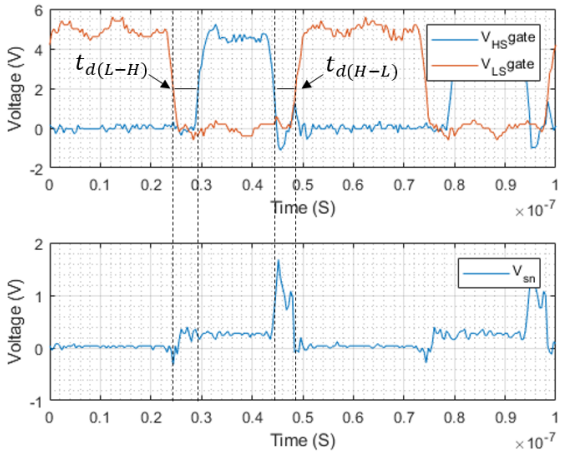


Figure 4.4. Measured voltage waveforms on the EPC1 MS2 board Phase 1, with $t_{d(L-H)} \approx 4.9$ ns and $t_{d(H-L)} \approx 3.6$ ns.

When Sw_{LS} turns off, V_{sn} rises to approximately 0.25 V, because Sw_{LS} capacitances ($C_{ds(LS)}$ and $C_{gd(LS)}$) are charged as $V_{gs(LS)}$ decreases. When Sw_{HS} turns on, V_{sn} remains at 0.25 V because Sw_{LS} is held in an off-state and the switch-node and the input source are o/c so that Sw_{LS} capacitances are not discharged. When Sw_{HS} turns off, current is brought through its capacitances ($C_{ds(HS)}$ and $C_{gd(HS)}$) into the driver giving the resulting voltage increase and positive voltage pump on V_{sn}($\approx$ 1.6 V). Once Sw_{LS} turns on its capacitors can discharge allowing V_{sn} to return to zero.

Figure 4.5 shows the voltage waveforms for the EPC3 board, the converter is operated at $f_{sw} = 20$ MHz,$D = 0.5$, and $V_{in} = 0$ V, the dead-times are $t_{d(L-H)} \approx 6.5$ ns, $t_{d(H-L)} \approx 4.3$ ns (in Figure 4.5(a)) and $t_{d(H-L)} \approx 1.9$ ns (in Figure 4.5(b)).

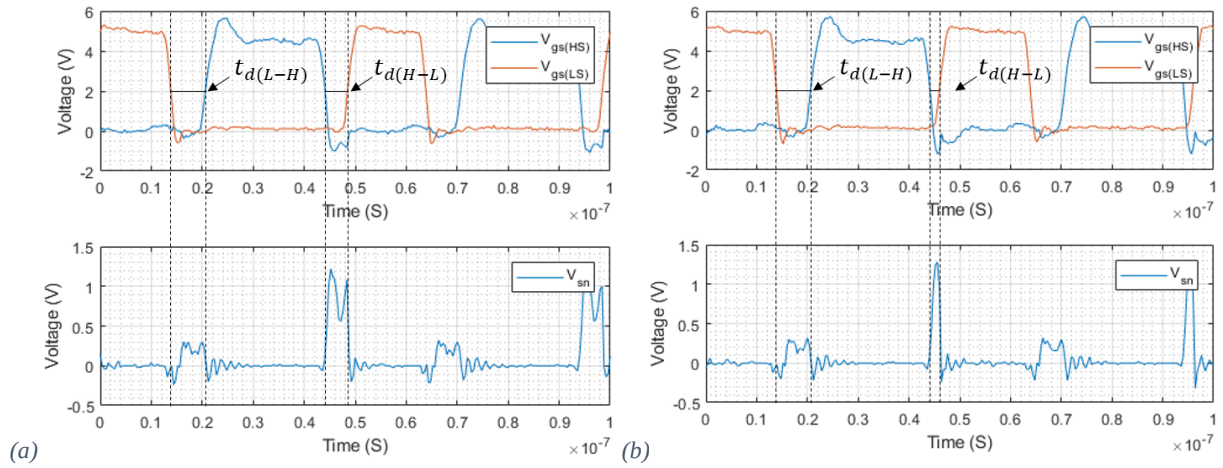


Figure 4.5. Measured voltage waveforms on the EPC3 MS2 board Phase 2. With the dead-time $t_{d(L-H)} \approx 6.5$ *ns, (a)*$t_{d(H-L)} \approx 4.3$ *ns and (b)*$t_{d(H-L)} \approx 1.9$ *ns.*

V_{sn} rises to about 0.3 V after Sw_{LS} turns off and V_{sn} rises to about 1.24 V after Sw_{HS} turns off, in both cases V_{sn} returns to zero once the other switch turns on. V_{sn} can return to zero after Sw_{HS} turns because the input is not o/c as with the EPC1 board – it is set to 0 V. The V_{sn} value after Sw_{LS} turns off for both boards is similar albeit slightly higher for the EPC3 board. The V_{sn} value after Sw_{HS} turns off is higher for the EPC1 board than the EPC3 board, indicating the o/c source allows more charge to accumulate on the high side switch capacitance.

All measured results in the rest of the chapter for a given board were measured with the smaller dead-times.

4.2.2 Measurement Data – Open Switch-node Power Losses

Table 4.1 shows the measured input currents from various V_{in}, and their respective power losses, for the open switch-node EPC1 MS2 circuit board operated at $f_{sw} = 20$ MHz, $D = 0.33$. Table 4.2 shows the measured input currents and their respective power losses, for the open switch-node EPC3 MS2 circuit board, with $D = 0.5$ for various V_{in} and f_{sw}.

Vin (V)	Iin (mA)	Pin (mW)	Idriver (mA)	Pdriver (mW)
o/c	-	-	42.7	213.5
2	6.72	13.44	44.15	220.75
5	16.00	80	45.63	228.15

Table 4.1. The measured power stage losses D=0.33,f_{sw}=20 MHz, V_{driver}=5 V, $t_{d(L-H)} \approx 4.9$ ns and$t_{d(H-L)} \approx 3.6$ ns. For a range of V_{in} with the EPC1 MS2 circuit board.

fsw (MHz)	Vin (V)	Iin (mA)	Pin (mW)	Idd (mA)	Pdd (mW)
20	0	-9.1	0	44	220
	5	20.3	101.5	47.1	235.5
25	0	-11.8	0	52.1	260.5
	5	23.7	118.5	55.98	279.9
30	0	-15.8	0	61.6	308
	5	27.6	138	66.2	331

Table 4.2. The measured power stage losses D=0.5,V_{driver}=5 V, $t_{d(L-H)} \approx 6.5$ ns and $t_{d(H-L)} \approx 1.9$ ns. For a range of V_{in} and f_{sw} with the EPC3 MS2 circuit board.

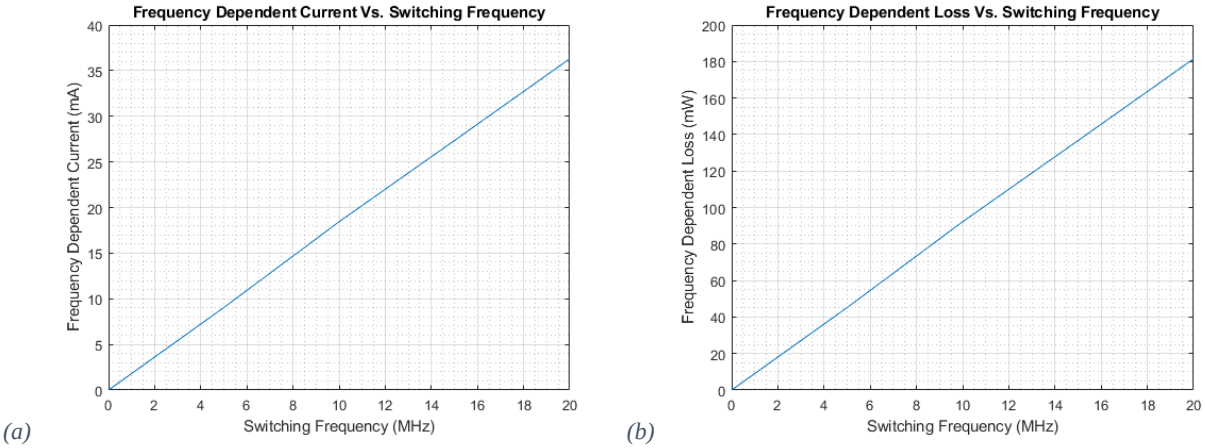
All the power supplied to the boards occurs as power loss as there is no output. The tables show the higher f_{sw} and V_{in}, the higher the losses. Comparing when the boards are operated at $f_{sw} = 20$ MHz, $V_{in} = 0$ and 5 V, the EPC3 board has slightly higher losses, this is due to boards being operated with different dead-times and duty cycles.

Table 4.3 shows the measured driver currents and losses, for $V_{in} = 0$ V and $V_{Driver} = 5$ V at a range of frequencies, for the EPC1 board. The current and power values for $f_{sw} = 0$ MHz are the quiescent current ($I_{DrvQ} = 6.458$ mA), and the quiescent power ($P_{DrvQ} = 32.29$ mW). Subtracting these values from the other values give the frequency dependent values. The frequency dependent driver current is approximately 1.84 mA/MHz, and frequency dependent loss is approximately 9.2 mW/MHz.

fsw (MHz)	Idriver (mA)	Idriver-IdrvQ (mA)	Pdriver (mW)	Pdriver-PdrvQ (mW)
0	6.458	0	32.29	0
5	15.860	9.402	79.3	47.01
10	24.900	18.442	124.5	92.21
15	33.800	27.342	169	136.71
20	42.750	36.292	213.75	181.46

Table 4.3. The measured driver current for the EPC1 MS2 circuit board. Operated with V_{in} = 0 V and V_{Driver} = 5 V, over a range of f_{sw}.

Figure 4.6 shows the relationship between f_{sw} and the calculated frequency dependant (a) driver current and (b) driver loss. The linear relationships validate that by subtracting the quiescent values the driver currents and losses are proportional to f_{sw}.

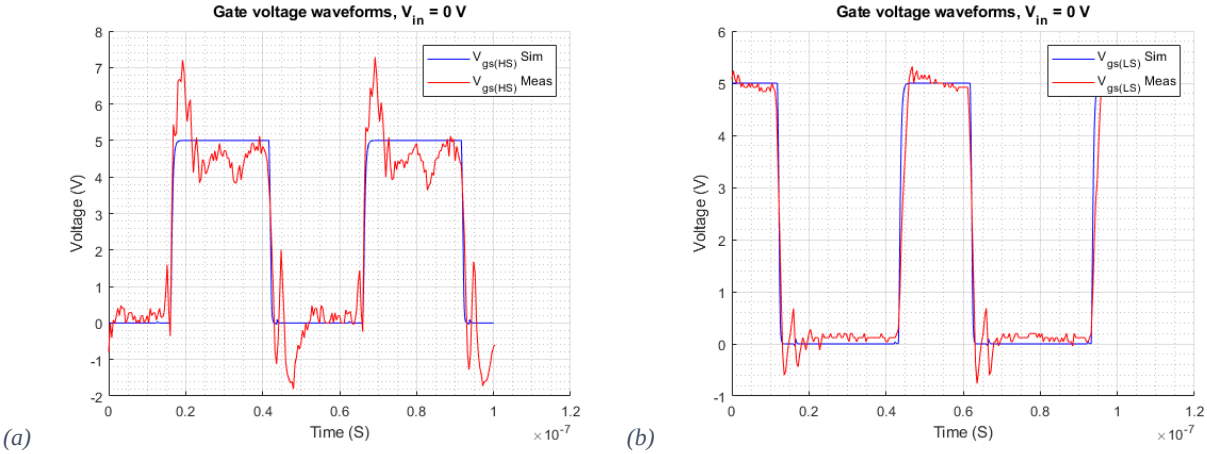


(a) *(b)*

Figure 4.6. Switching frequency vs. frequency dependent (a) driver current and(b) driver loss. Operated with V_{in} = 0 V and V_{Driver} = 5 V, with the EPC1 MS2 circuit board.

4.3 Open Switch-Node Simulation Set-Up

This section compares the measured results to LTSpice simulations, for the open-switch-node converter to match up timing. Simulated and measured waveforms are shown in Figure 4.7. The measured waveforms are from the EPC3 boards. To match the timings the threshold voltages ($V_{th} = 2$ V) of the simulated and measured waveforms were aligned to give the dead-times $t_{d(L-H)} = 4.07$ ns and $t_{d(H-L)} = 1.457$ ns. The timing for the simulated and measured waveforms match, but there is ringing that the simulations do not account for. The circuit was simulated with the parasitic inductances in the circuit board excluded; this is investigated in the next section.

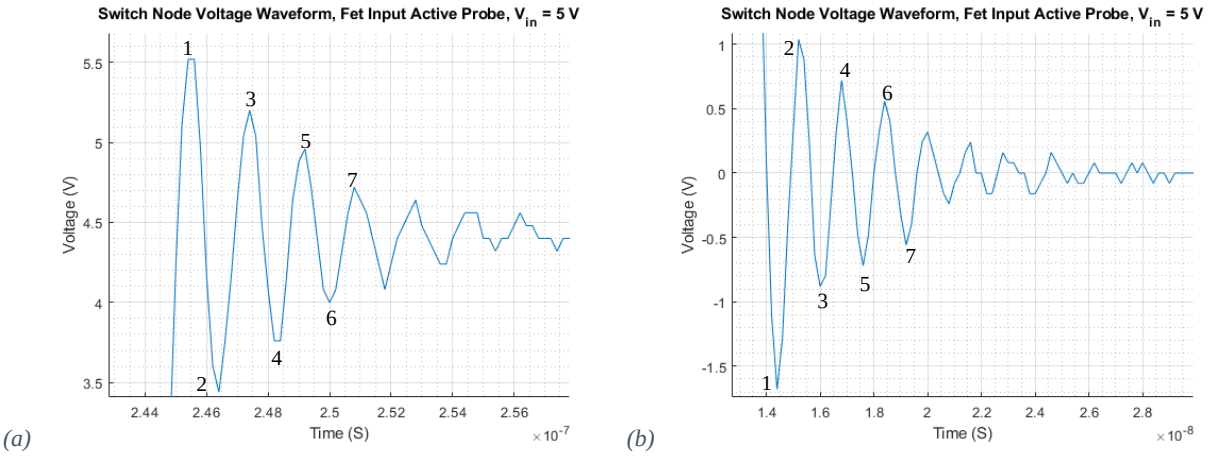


(a) *(b)*

Figure 4.7. (a) $V_{gs(HS)}$ simulated and measured waveforms. (b) $V_{gs(LS)}$ simulated and measured waveforms.

4.3.1 Power Path Parasitic Voltage Ringing

In this section the power path parasitic inductances are calculated using the measured waveforms for the EPC1 board, operated at 20 MHz with $V_{in} = 5$ V. Figure 4.8 shows V_{sn} waveforms (ringing voltages) after (a) Sw_{HS} and (b) Sw_{LS} turn on.



(a) *(b)*

Figure 4.8. Close up look at V_{sn} ripple, for V_{in} = 5 V, open switch-node, EPC1 board. (a) At Sw_{HS} turn on. (b) At Sw_{LS} turn on.

The average period of oscillation is approximately 1.6 ns, hence the frequency of oscillation (f_0) is 625 MHz, and the angular frequency of oscillation (w_0) is 1.25π Grad/sec. To calculate the power path parasitic inductance, the resonant frequency relationship is used:

$$w_0 = 1/\sqrt{LC}. \qquad (4.1)$$

The equivalent energy (linear) capacitance in the power path is $C_{oss(eq)}$ which was calculated to equal 67 pF in chapter 3.5.2 on page - 50 -. The parasitic inductance in the power path is calculated to be 967.84pH. There are PCB trace connections between: the input and Sw_{HS}, Sw_{HS} and the switch-node, and the switch-node and Sw_{LS}. The total parasitic inductance in the primary switching loop was split into three equal components of 320 pH.

4.3.2 Open Switch-Node Waveforms: Measurements and Simulations

This section compares the simulated waveforms using the parasitic inductance calculated in the previous section. Figure 4.9(a) shows the simulated circuit diagram with parasitic inductances included. The graphs in Figure 4.9 show a comparison between this simulated circuit and the measured results, for: (b) V_{in}= 0 V (o/c for the measured), (c) V_{in}= 2 V, and (d) V_{in}= 5 V. The measured results are from the EPC1 board.

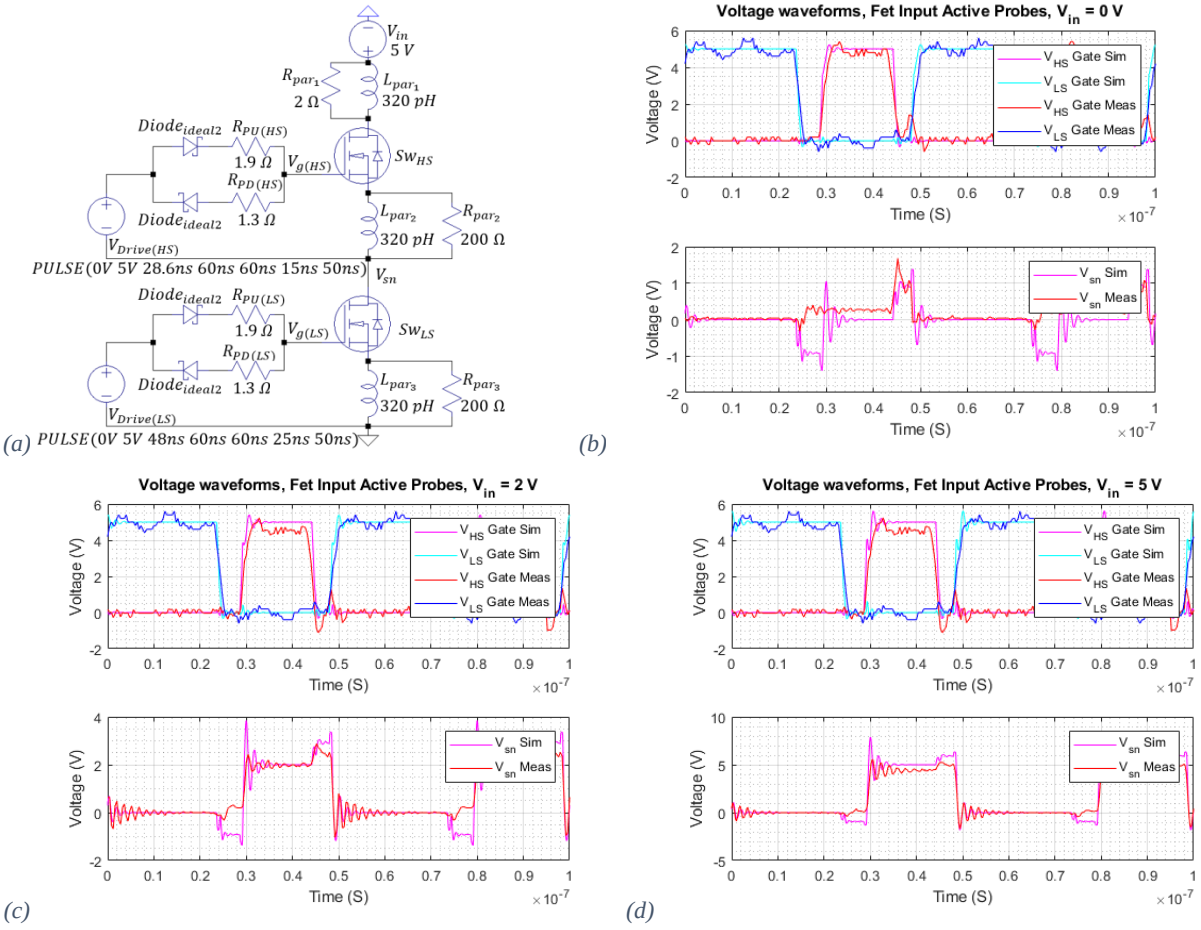


Figure 4.9. (a) Simulations circuit diagram for comparison with measured results. Switch-node and gate-source waveforms for: (b) V_{in} = 0 V (o/c for measurement), (c) V_{in} = 2 V, and (d) V_{in} = 5 V. With added parasitic inductances, open switch-node and dead-times *of $t_{d(L-H)} \approx$ 4.9 ns and $t_{d(H-L)} \approx$ 3.6 ns.*

The voltage levels of all the measured waveforms are lower than the simulated indicating due to there being more resistance than accounted for in the simulations. The main difference is that during $t_{d(L-H)}$, the simulation shows more negative, this will be examined in the next section.

Figure 4.9(b) shows a good match, if accounting for the measured converter having an o/c V_{in} and the simulated converter having $V_{in} = 0$ V (as explained earlier in this chapter).

In Figure 4.9(c) and (d) the overall waveform shapes are similar; after Sw_{LS} turns on there is a very close match in the waveforms. After Sw_{HS} turns on the damping ratio is much smaller for the simulated results, than for the measured results to imply that that there is more resistance (loss) in the measured power path than in the simulated power path. The frequency of oscillation of the ringing match very closely.

4.3.3 Differences between Measurements and Simulations

Parasitic inductances were not included in the gate driver loops and for this reason there is no ringing in the simulated V_{gs} waveforms. The simulations show a negative pumping on the switch-node between Sw_{LS} turn off and Sw_{LS} turn on. This would make sense if C_{ds} is smaller than C_{gd} and there is no off-state leakage current in the EPC switches. There may be a difference C_{ds}:C_{gd} ratio in the measured converter and the simulated converter. There appears to be a C_{oss} discharge mechanism in the measured converter.

4.4 Open Switch–Node Operation

This section analyses the buck switching power stage with EPC2040 switches by simulation for the case of no inductor fitted, to focus on gate driver and power stage switching losses.

The voltage waveforms ($V_{gs(HS)}$, $V_{gs(LS)}$ and V_{sn}) are shown for one period in Figure 4.10, for the simulated EPC2040 with open-circuit switch-node, operated at $f_{sw} = 20$MHz, $V_{in} = 2$ V, $t_{d(L-H)} \approx 4.9$ ns and $t_{d(H-L)} \approx 3.6$ ns. Figure 4.11 shows expanded views of the switching intervals.

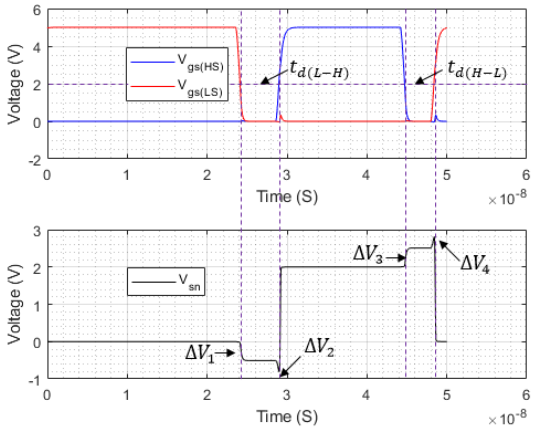


Figure 4.10. $V_{gs(HS)}$, $V_{gs(LS)}$ and V_{sn} waveforms over one period, operated at $f_{sw} = 20$ MHz and $V_{in} = 2$ V.

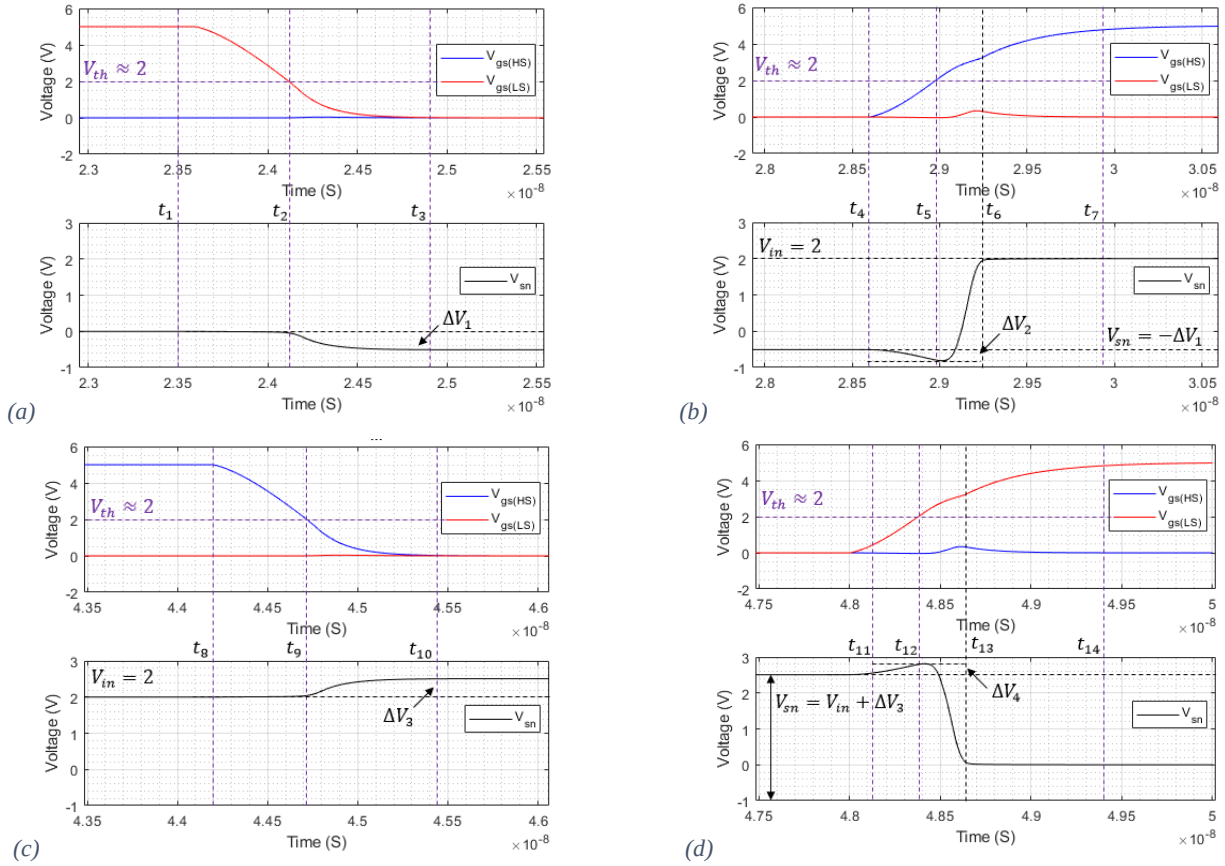


Figure 4.11. Close up views of the simulated open-circuit switch-node voltage waveforms operated at f_s = 20 MHz and V_{in} = 2 V, at(a) Sw_{LS} turn off, (b) Sw_{HS} turn on, (c) Sw_{HS} turn off, and (d) Sw_{LS} turn on.

4.4.1 Open Switch-Node: Sw_{LS} Turn Off

Figure 4.12(a) shows, the simplified voltage waveforms at Sw_{LS} turn off (Figure 4.11(a)). There is no Miller interval because Sw_{LS} was on before this time interval. During this time interval $V_{gs(LS)}$ is decreasing.

At t_1: $V_{gs(LS)} = V_{Driver}$, $V_{gd(LS)} = V_{Driver}$, and $V_{ds(LS)} = V_{sn} \approx 0$ V.

During t_1 *to* t_2: this interval is shown in Figure 4.12(b). The gate capacitances are discharging, and their currents flow into the driver (green), $i_{C_{gd(LS)}}$ flows through the channel.

At t_2: $V_{gs(LS)} = V_{th}$, $V_{gd(LS)} = V_{th}$, and $V_{ds(LS)} = V_{sn} \approx 0$ V.

During t_2 *to* t_3: this interval is shown in Figure 4.12(c). The channel is closed, thus $i_{C_{gd(LS)}}$ must flow through $C_{ds(LS)}$ (green) which negatively charges $C_{ds(LS)}$, adding a negative voltage of magnitude ΔV_1 to the switch-node. As V_{sn} becomes more negative $V_{C_{oss(HS)}}$ increases, this capacitance is charged from the input (orange).

At t_3: $V_{gs(LS)} = 0$ V, $V_{gd(LS)} = \Delta V_1$, and $V_{ds(LS)} = V_{sn} = -\Delta V_1$.

After t_3: there is no further change in the circuit until Sw_{HS} turns on. The magnitude of ΔV_1 depends on ratio of $C_{gd(LS)}$ and $C_{ds(LS)}$.

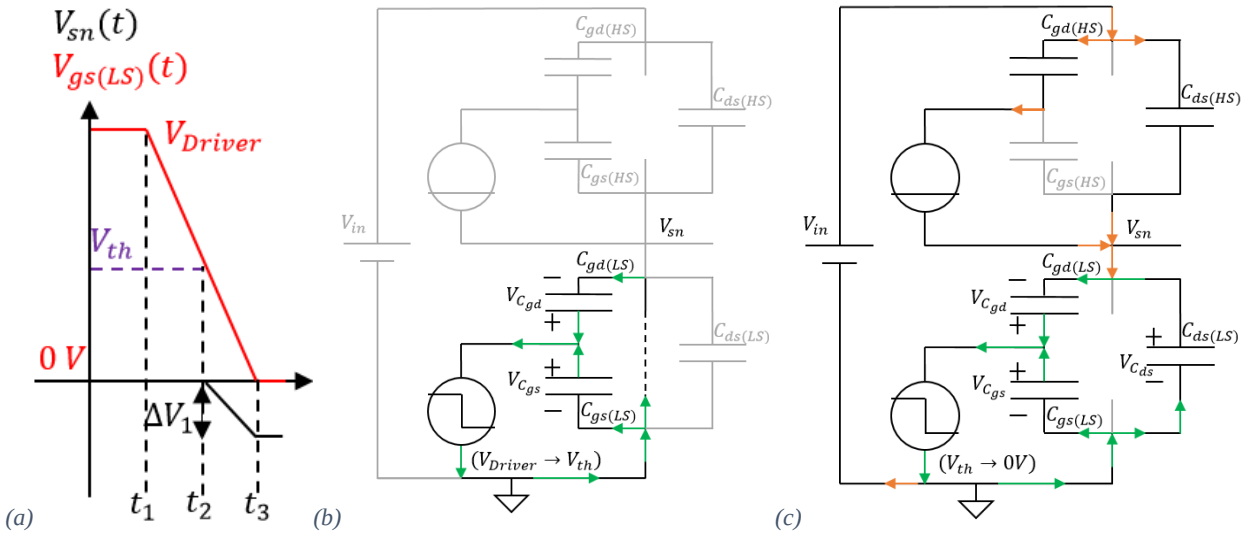


Figure 4.12. (a) The voltage waveforms. The switch capacitances and currents between (b) $t_1 - t_2$, and (c) $t_2 - t_3$. For Sw_{LS} turn off.

4.4.2 Open Switch–Node: Sw_{HS} Turn On

Figure 4.13(a) shows, the simplified voltage waveforms, for Sw_{HS} turn on (Figure 4.11(b)). During the Miller Plateau, $V_{gs(HS)}$ is shown as constant, whereas in reality the plateau will have a slope accordingly to the device's transconductance. During this time interval $V_{gs(HS)}$ is increasing.

At t_4: $V_{gs(HS)} = 0$ V, $V_{gd(HS)} = -(V_{in} + \Delta V_1)$, $V_{ds(HS)} = V_{in} + \Delta V_1$, and $V_{sn} = -\Delta V_1$.

During t_4 *to* t_5: this interval is shown in Figure 4.13(b). $C_{gs(HS)}$ and $C_{gd(HS)}$, are charged with current from the driver (green), as the channel has not yet opened. $i_{C_{gd(HS)}}$ flows through $C_{ds(HS)}$, the voltage across $C_{ds(HS)}$ increases by a magnitude of ΔV_2. This increase in voltage means that $C_{oss(LS)}$ is further negatively charged by the input (orange), the charge stored in $C_{oss(LS)}$ is dissipated in Sw_{LS} during its next turn on, and is classified as $C_{oss(LS)}$ loss.

At t_5: $V_{gs(HS)} = V_{th}$, $V_{gd(HS)} = V_{th} - (V_{in} + \Delta V_1 + \Delta V_2)$, $V_{ds(HS)} = V_{in} + \Delta V_1 + \Delta V_2$, and $V_{sn} = -(\Delta V_1 + \Delta V_2)$.

During t_5 *to* t_6: the interval is shown in Figure 4.13(c). As the channel is opening $V_{ds(HS)}$ drops so that $C_{ds(HS)}$ is discharged and its current flows through the channel (purple). $i_{C_{gd(HS)}}$ cannot flow through $C_{ds(HS)}$, and only a small amount can flow through the channel, thus $C_{gd(HS)}$ does not charge (much) during this interval. Figure 4.11(b) shows that the slope of $V_{gs(HS)}$ in the Miller plateau does not completely flatten but is reduced, as $C_{gs(HS)}$ is still being charged. Sw_{LS} capacitances can be discharged through the channel to input and to ground.

At t_6: $V_{gs(HS)} = V_{PL}$(exited the Miller plateau), $V_{gd(HS)} = V_{PL} - V_{in}$, $V_{ds(HS)} \approx 0$ V,and $V_{sn} = V_{in}$.

During t_6 *to* t_7: the channel is fully open. $C_{gs(HS)}$ is charged to V_{Driver}, $C_{dg(HS)}$ is charged to $V_{Driver} - V_{in}$.

After t_7: there is no further change in the circuit until Sw_{HS}turns off.

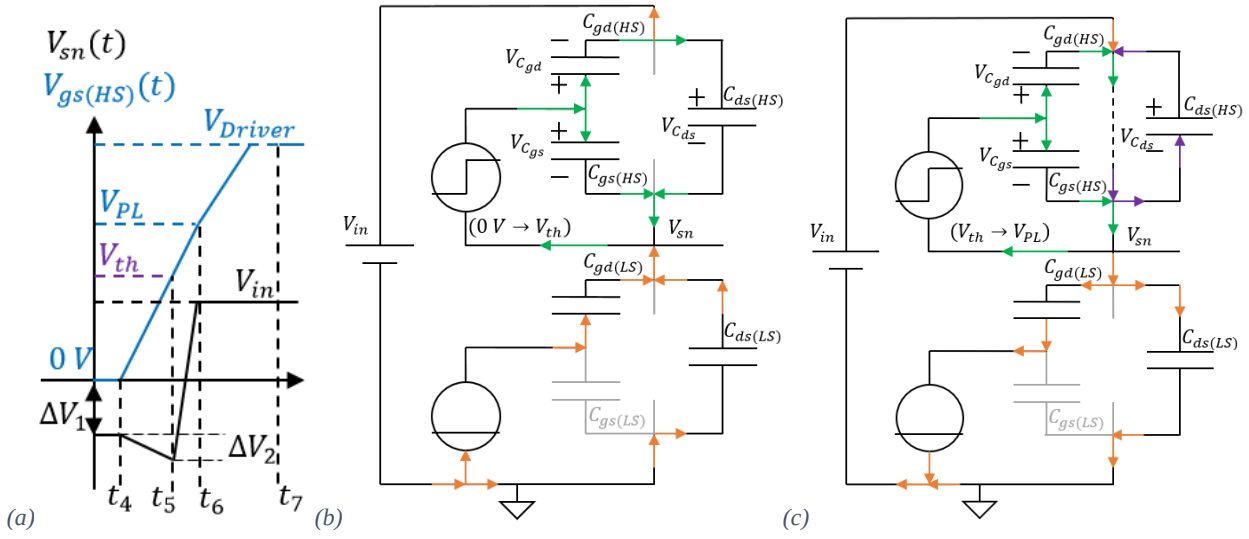


Figure 4.13. (a) The voltage waveforms. The switch capacitances and currents between (b) $t_4 - t_5$, *and (c)* $t_5 - t_6$. *For* Sw_{HS} *turn on.*

4.4.3 Open Switch–Node: Sw_{HS} Turn Off

Figure 4.14(a) shows, the simplified voltage waveforms, for Sw_{HS} turn off (Figure 4.11(c)). There is no Miller interval because Sw_{HS} has been on. During this time interval $V_{gs(HS)}$ is decreasing.

At t_8: $V_{gs(HS)} = V_{Driver}, V_{C_{gd(HS)}} = V_{Driver} - V_{in}, V_{C_{ds(HS)}} \approx 0$ V, and $V_{sn} = V_{in}$.

During t_8 *to* t_9: this interval is shown in Figure 4.14(b). $C_{gs(HS)}$ and $C_{gd(HS)}$discharge through driver (green), $i_{C_{gd(HS)}}$ flows through the channel as it is still open. The voltage across Sw_{LS} remains approximately constant.

At t_9: $V_{gs(HS)} = V_{th}, V_{C_{gd(HS)}} = V_{th} - V_{in}, V_{C_{ds(HS)}} \approx 0$ V, and $V_{sn} = V_{in}$.

During t_9 *to* t_{10}: this interval is shown in Figure 4.14(c). The channel is closed and this means that $i_{C_{gd(HS)}}$ flows through $C_{ds(HS)}$. $C_{ds(HS)}$ voltage is negatively charged by a magnitude of ΔV_3, this causes V_{sn} to increase by a value of ΔV_3 to $V_{in} + \Delta V_3$. $V_{C_{oss(LS)}}$ increases and the capacitance is charged with current from the input (orange).

At t_{10}: $V_{gs(HS)} = 0$ V, $V_{C_{gd(HS)}} = -V_{in}, V_{C_{ds(HS)}} = -\Delta V_3$, and $V_{sn} = 0$ V.

After t_{10}: there are no changes in the circuit until Sw_{LS} turns on.

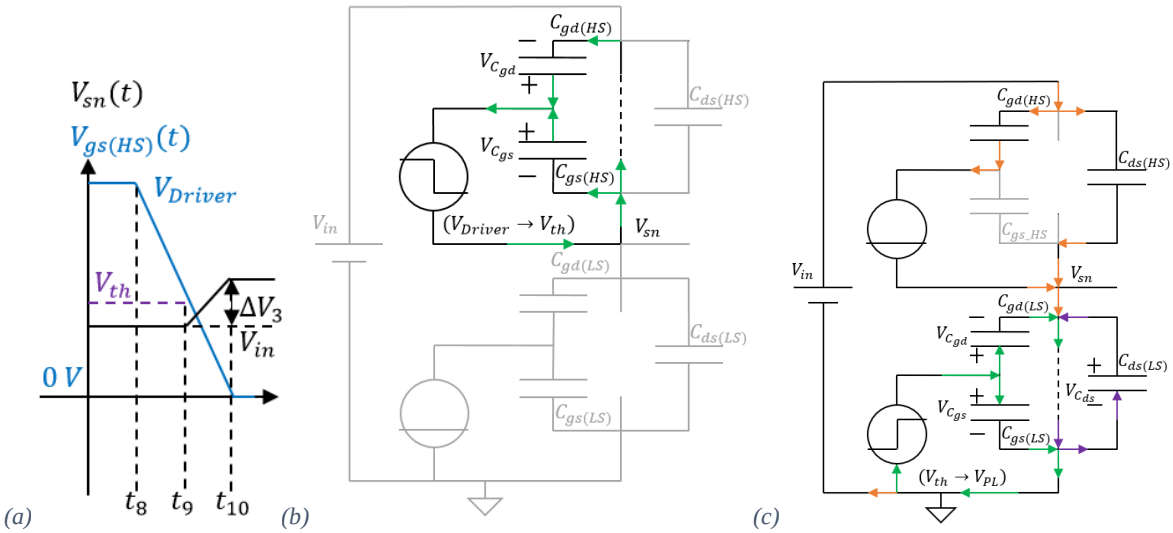


Figure 4.14(a) The voltage waveforms. The switch capacitances and currents between (b) $t_8 - t_9$*, and (c)* $t_9 - t_{10}$*. For* Sw_{HS} *turn off.*

4.4.4 Open Switch–Node: Sw_{LS} Turn On

Figure 4.15(a) shows the simplified voltage waveforms, for Sw_{LS} turn on (Figure 4.11(d)). During the Miller plateau, $V_{gs(LS)}$ is shown to be constant, whereas in reality the plateau will have a slope accordingly to device transconductance. During this time interval $V_{gs(LS)}$ is increasing.

At t_{11}: $V_{gs(LS)} = 0$ V, $V_{gd(LS)} = -(V_{in} + \Delta V_3)$, and $V_{ds(LS)} = V_{sn} = V_{in} + \Delta V_3$.

During t_{11} *to* t_{12}: this interval is shown in Figure 4.15(b). $C_{gd(LS)}$ and the $C_{gs(LS)}$ are charged with current from the driver (green), as the channel is not opened yet $i_{C_{gd(LS)}}$ flows through $C_{ds(LS)}$, the voltage across $C_{ds(LS)}$ increases by a magnitude of ΔV_4. This increase in voltage means that $C_{oss(HS)}$ is negatively charged by the input (orange), the charge stored in $C_{oss(HS)}$, is dissipated the next time Sw_{HS} turns on, and is classified as $C_{oss(HS)}$ loss.

At t_{12}: $V_{gs(LS)} = V_{th}$, $V_{gd(LS)} = V_{th} - (V_{in} + \Delta V_3 + \Delta V_4)$, and $V_{ds(LS)} = V_{sn} = V_{in} + \Delta V_3 + \Delta V_4$.

During t_{12} *to* t_{13}: the interval is shown in Figure 4.13(c). As the channel is opening $V_{ds(LS)}$ drops, thus $C_{ds(LS)}$ is discharged and its current flows through the channel (purple). $i_{C_{gd(LS)}}$ cannot flow through $C_{ds(LS)}$, and only a small amount can flow through the channel, thus $C_{gd(LS)}$ does not charge much during this interval. $V_{gs(LS)}$ is in the Miller plateau, Figure 4.11(d) shows that its slope does not completely flatten but is reduced, as $C_{gs(LS)}$ is still being charged. Sw_{HS} capacitances can be discharged through the channel, input, and ground.

At t_{13}: $V_{gs(LS)} = V_{PL}$(exited the Miller plateau), $V_{gd(LS)} = V_{PL}$, and $V_{ds(LS)} = V_{sn} = 0$ V.

During t_{13} *to* t_{14}: the channel is fully open. $C_{gs(LS)}$ and $C_{dg(HS)}$ are charged to V_{Driver}.

After t_{14}: there is no change in the circuit until Sw_{LS} turns off.

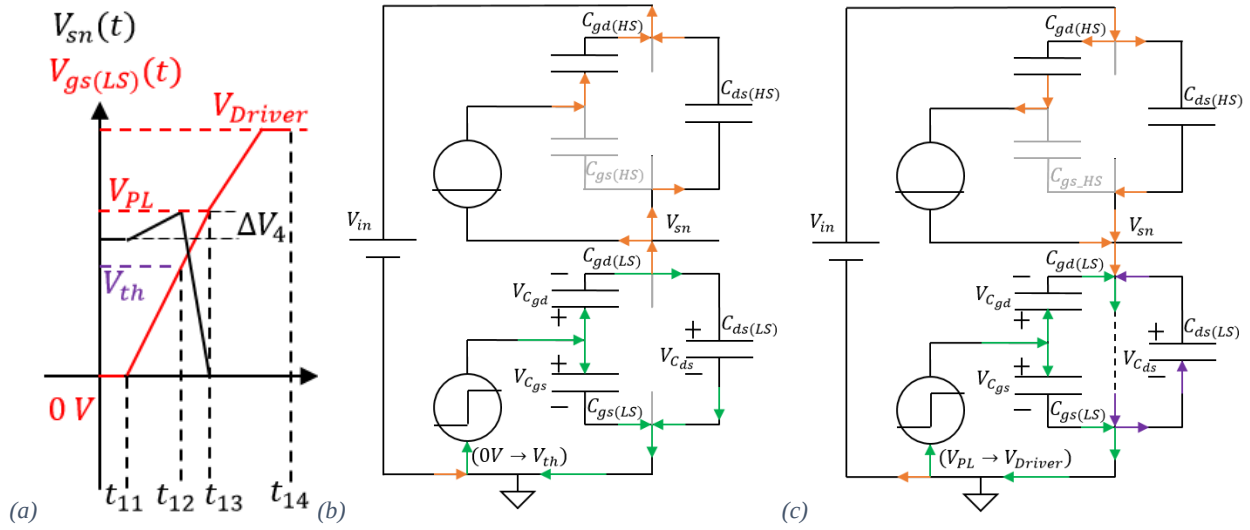


Figure 4.15(a) The voltage waveforms. The switch capacitances and currents between (b) $t_{11} - t_{12}$*, and (c)*$t_{12} - t_{13}$*. For* Sw_{LS} *turn on.*

4.4.5 Simulated Loss Analyses for Open Switch–Node

The following equations are used to determine the losses from the measurements. The power delivered by the driver can be determined by Joule's law:

$$P_{Driver} = V_{Driver} I_{Driver}. \quad (4.2)$$

This power is delivered to the gate and this can be broken down into the frequency independent ($P_{quiescent(Driver)}$) and frequency dependent power loss:

$$P_{Driver} = P_{quiescent(Driver)} + E_{gate} f_{sw} \quad (4.3)$$

where E_{gate} is the gate energy per cycle. E_{gate} is calculated using the gate current and voltage measurements:

$$E_{gate} = I_{gate} V_{gate} / f_{sw} = 1/T_{sw} \int_0^{T_{sw}} P_{gate}(t) dt. \quad (4.4)$$

The change in energy (ΔE_{cap}) required to change the voltage (from V_2 to V_1) of a capacitance C is:

$$\Delta E_{cap} = \frac{1}{2} C (V_1^2 - V_2^2). \quad (4.5)$$

The gate capacitance C_{iss} is defined in Equation (1.6) and the output capacitance C_{oss} is defined in Equation (1.7), on page - 16 -. Switching energy is due to the charge across of C_{oss}.

C_{oss} and C_{iss} are normally small signal quantities which vary with voltage. This section will use effective energy related values $C_{oss(ER)}$ and $C_{iss(ER)}$. This is due to the relationships between capacitance and voltage, as the voltage increases the capacitance decreases. It does not make sense to use either the capacitance value at the beginning or end of a change of voltage charge. The equivalent energy capacitance, is the equivalent capacitance value for a given voltage change to result in the same overall energy (stored or dissipated), using Equations (4.4) or (4.5).

The EPC2040 datasheet [38] defines the switch $C_{oss(ER)} = 106$ pF, for $V_{gs} = 0$ V and V_{ds} transitions through 0 V to 6 V. For C_{iss} the charge, capacitance, voltage relationship is used:

$$Q = VC \quad (4.6)$$

The total gate charge $Q_G = 745$ pC ($V_{DS} = 6$ V, $V_{GS} = 5$ V, $I_D = 1.5$ A), the change in V_{GS} is 0 V to 5 V, thus $C_{iss(ER)} = 149$ pF, for $V_{ds} = 6$ V. Figure 4.16 shows the test circuit, with equivalent lumped circuit model, this circuit is simulated in LTSpice.

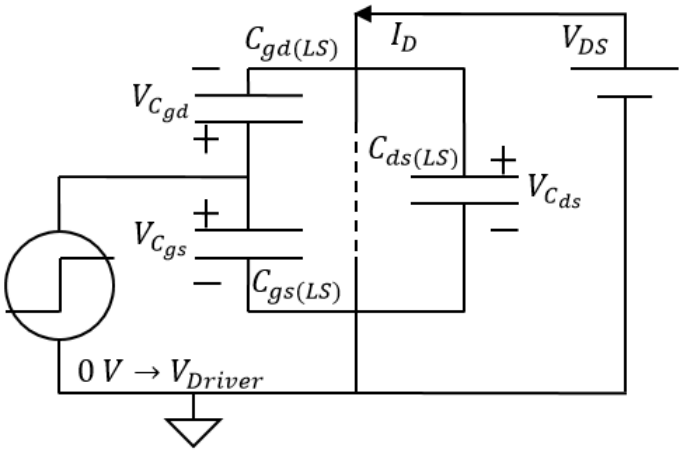


Figure 4.16. The circuit diagram for $C_{iss(ER)}$ test. The test conditions are V_{DS} = 6 V, I_D = 1.5 A and V_{GS} = 0 to 5 V.

For the circuit shown in Figure 4.16, $V_{C_{gs}}$ ranges from 0 to 5 V, and $V_{C_{ds}}$ ranges from -6 to 5 V. The problem with using $C_{iss(ER)}$ value from the datasheet is that $\Delta V_{C_{ds}} = 11$ V ($\Delta V_{C_{ds}} = V_{Driver} + V_{in}$). $C_{iss(ER)}$ needs to be recalculated for the conditions that the switch is used in this thesis.

The drive losses result from the gate charging currents passing though the driver circuit resistances (and internal pre-driver switch capacitances). The driver circuit resistances include the driver output resistances and the added gate driver resistors. The magnitude of the driver resistance does not affect the driver loss. A larger gate resistance would yield a larger RC time constant (hence more charging time) and less current, and a smaller gate resistance would result in a larger driver current and have a smaller RC time constant (hence less charging time). The RC time constant does however create increased channel V-I overlap time duration and will therefore have some impact on circuit switching loss.

Equation (4.3) shows that driver loss is dependent of f_{sw} and E_{gate} . This will be discussed in the following two sections along with how driver loss is also dependent on V_{in}. In open-circuit switch-node the power stage losses are from switching losses. As it is an open-circuit switch-node, there can be no conduction loss, dead-time loss, or diode reverse recovery loss.

4.4.6 Open Switch–Node Analysis: Power Stage Losses

As stated, the only power stage losses in the open-circuit switch-node, are switching losses. During Sw_{HS} turn-on, $C_{oss(ER(LS))}$ is charged; when Sw_{LS} turns on this energy is lost to be Sw_{LS} switching loss. During Sw_{LS} turn-on, $C_{oss(ER(HS))}$ is charged; when Sw_{HS} turns on this energy is lost to be Sw_{HS} switching loss. Thus, the power path losses can be calculated using the energy from Equation (4.5). The change in voltage across $C_{oss(ER(LS))}$ is, 0 V to $V_{C_{oss(ER(LS))}} = \Delta V_1 + \Delta V_2 + V_{in}$. Thus, Sw_{LS} switching loss is:

$$P_{sw(LS)} = \frac{1}{2} C_{oss(ER(LS))} (\Delta V_1 + \Delta V_2 + V_{in})^2 f_{sw}. \qquad (4.7)$$

The change in voltage across $C_{oss(ER(HS))}$ is, 0 V to $V_{C_{oss(ER(HS))}} = \Delta V_3 + \Delta V_4 + V_{in}$. Thus, Sw_{HS} switching loss is:

$$P_{sw(HS)} = \frac{1}{2} C_{oss(ER(HS))} (\Delta V_3 + \Delta V_4 + V_{in})^2 f_{sw}. \qquad (4.8)$$

As the only power stage losses in the open-circuit switch-node are switching losses, all the power from the input is lost charging $C_{oss(LS)}$ and $C_{oss(HS)}$. LTSpice calculates loss via numeric integration of the product of its voltage and current waveforms:

$$P_{in} = f_{sw} \int_0^{T_{sw}} V_{in}(t) I_{in}(t) dt. \quad (4.9)$$

Section 4.5 compares the analytic models to the simulated results.

4.4.7 Open Switch–Node Analysis: Driver Losses

The energy used to charge $C_{oss(LS)}$ and $C_{oss(HS)}$ from the input is assumed to be balanced, this means that charge energy of $(\Delta V_1 + \Delta V_2)$ will balance $(\Delta V_3 + \Delta V_4)$ and this is confirmed in Table 4.4. Regardless of the value of these charge energies (due to the value of V_{in}), the charge values are approximately balanced $(\Delta V_1 + \Delta V_2) \approx (\Delta V_3 + \Delta V_4)$. The small variations can be accounted to as charge being added by the drivers.

The changes in V_{sn} (ΔV_1, ΔV_2, ΔV_3, and ΔV_4), that have previously described, are shown in Table 4.4 for $V_{in} = 0$, 2 and 5 V.

	Input Voltage		
Voltage Change	***0 V***	***2 V***	***5 V***
ΔV_1 (V)	0.5002	0.5085	0.52
ΔV_2 (V)	0.3357	0.3063	0.2675
ΔV_3 (V)	0.5004	0.509	0.521
ΔV_4 (V)	0.3369	0.306	0.264
$\Delta V_1 + \Delta V_2$ (V)	0.8359	0.8148	0.7875
$\Delta V_3 + \Delta V_4$ (V)	0.8373	0.815	0.785

Table 4.4. The simulated voltage changes for V_{in}=0, 2, and 5 V.

Calculating the driver loss for charging $C_{iss(ER)}$, when $C_{iss(ER)} = 149$ pF, $V_{Driver} = 5$ V, and $f_{sw} = 20$ MHz gives:

$P_{Driver} = \frac{1}{2} C_{iss(ER)} (V_{Driver})^2 f_{sw} = 37.25$ mW, there are two drivers => 74.5 mW.

This is the driver power assuming that when the drivers are turning the switches on, that V_{gs} goes from 0 V to V_{Driver}. As is shown in the data from the simulation in Table 4.6, this is a passible estimation for $V_{in} = 2$ V, but only somewhat representative for the other two. Table 4.5 demonstrates the flaw, $V_{C_{gs}}$ is tied to V_{gs} (as it goes from 0 V to V_{Driver}), but $V_{C_{gd}}$ is not and therefore takes a different amount of energy to be charged, and is dependent on V_{in}.

	Sw_{LS} Turn off	**Sw_{LS} Turn on**
$C_{gs(LS)}$	$V_{Driver} \rightarrow 0\ V$	$0\ V \rightarrow V_{Driver}$
$C_{gd(LS)}$	$V_{Driver} \rightarrow \Delta V_1$	$-(V_{in} + \Delta V_3) \rightarrow V_{Driver}$
	Sw_{HS}Turn off	**Sw_{HS}Turn on**
$C_{gs(HS)}$	$0\ V \rightarrow V_{Driver}$	$V_{Driver} \rightarrow 0\ V$
$C_{gd(HS)}$	$V_{Driver} \rightarrow \Delta V_3$	$-(V_{in} + \Delta V_1) \rightarrow V_{Driver}$

Table 4.5. The changes in gate capacitance voltage during their respective switching.

The equations should be:

$$P_{Driver_{gs(LS)}} = \frac{1}{2} C_{gs(ER(LS))} (V_{Driver})^2 f_{sw}, \quad (4.10)$$

$$P_{Driver_{gd(LS)}} = \frac{1}{2} C_{gd(ER(LS))} (V_{Driver}^2 + (V_{in} + \Delta V_3)^2) f_{sw}, \quad (4.11)$$

$$P_{Driver_{gs(HS)}} = \frac{1}{2} C_{gs(ER(HS))} (V_{Driver})^2 f_{sw}, \quad (4.12)$$

and

$$P_{Driver_{gd(HS)}} = \frac{1}{2} C_{gd(ER(HS))} (V_{Driver}^2 + (V_{in} + \Delta V_1)^2) f_{sw}. \quad (4.13)$$

4.5 Simulated Open-Circuit Switch-node Results and Analysis

In this section, the simulated results of the open-circuit switch-node are discussed. Figure 4.17 shows the open-circuit switch-node circuit diagram, operated at $f_{sw} = 20$ MHz, with $V_{in} = 0$ V, and $V_{Driver} = 5$ V. The *Peregrine* lumped circuit models are indicated by the red dashed boxes.

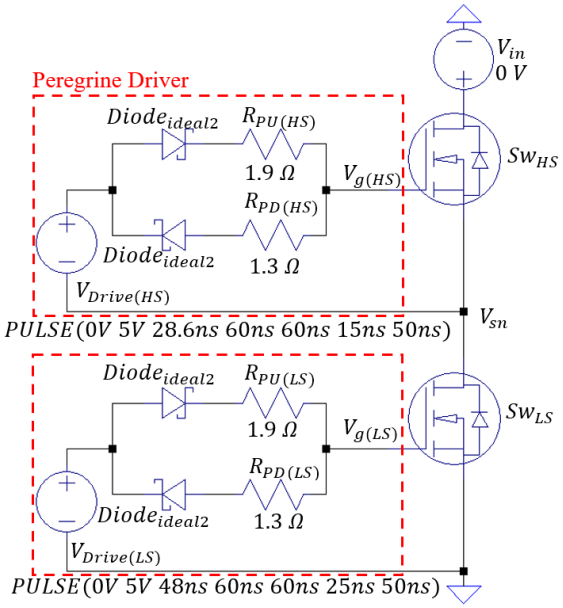


Figure 4.17. LTSpice circuit diagram for open-circuit switch-node, V_{in} = 0 V, V_{Driver} = 5 V, and f_{sw} = 20 MHz.

As noted earlier, the LTSpice internal measure command calculates the losses by performing numeric integration on the product of the voltage and current waveforms, across the given component. The supplied and lost powers from the simulation are shown in Table 4.7, Table 4.8 , and Table 4.9.

They are split into three groups: the power supplied and dissipated in the power path, the power supplied and dissipated by the HS driver, and the power supplied and dissipated by the LS driver. The power path includes the supply power from input (P_{in}), the loss from Sw_{HS} ($P_{sw(HS)}$), and the loss from Sw_{LS} ($P_{sw(LS)}$). This is given by:

$$P_{sw} = f_{sw} \int_0^{T_{sw}} (V_D(t) I_D(t) + V_S(t) I_S(t) + V_G(t) I_G(t)) dt \quad (4.14)$$

where: $V_D(t)$ and $I_D(t)$ are the drain voltage and current waveforms respectively, $V_S(t)$ and $I_S(t)$ are the source voltage and current waveforms respectively, and $V_G(t)$ and $I_G(t)$ are the gate voltage and current waveforms respectively. This gives the total losses in the switches and these losses are separated into losses from the driver and losses from the input.

Table 4.6 shows the o/c switch-node simulated results for the circuit in Figure 4.17, for various f_{sw} and V_{in}. The power supplied by the input is $P_{(in)input}$, the power supplied by the HS and LS drivers is combined in $P_{(in)drivers}$, and the total power supplied to the converter is $P_{(in)total}$. The power dissipated in the HS and LS pull-up and pull-down resistors are combined into $P_{R(driver)}$, the total loss in Sw_{HS} is $P_{Sw_{HS}}$ and the total loss in Sw_{LS} is $P_{Sw_{LS}}$. The losses are all combined into total loss.

F_{sw}	V_{in}	$P_{(in)input}$	$P_{(in)drivers}$	$P_{(in)total}$	$P_{R(driver)}$	$P_{Sw_{HS}}$	$P_{Sw_{LS}}$	Total Loss
20 MHz	0 V	0.00	66.67	66.67	48.02	9.29	9.33	66.64
	2 V	17.56	76.64	94.19	52.29	20.92	20.96	94.16
	5 V	85.38	89.93	175.31	58.69	58.27	58.31	175.28
25 MHz	0 V	0.00	83.29	83.29	60.02	11.60	11.64	83.25
	2 V	21.95	95.74	117.69	65.35	26.12	26.18	117.65
	5 V	106.72	112.35	219.07	73.35	72.82	72.86	219.04
30 MHz	0 V	0.00	98.61	98.61	71.17	13.88	13.52	98.56
	2 V	26.16	113.64	139.80	77.78	31.37	30.59	139.75
	5 V	127.65	133.74	261.39	87.63	87.46	86.25	261.34

Table 4.6. Simulated supplied (source and drive) powers and power losses, for open-circuit switch-node.

Table 4.7 shows the breakdown of the simulated, the supplied and dissipated powers, for Sw_{HS} in the o/c switch-node circuit and for various V_{in} and f_{sw}. The power input to the circuit by the HS driver is $P_{(in)driver_{HS}}$ (green). The power lost in the HS pull-up resistor and pull-down resistor are $P_{(loss)R_{PU(HS)}}$ and $P_{(loss)R_{PU(HS)}}$ respectively (yellow), they are combined into $P_{(loss)R_{Total(HS)}}$ (red). The power supplied from the HS driver is lost either in the HS driver resistances and the HS switch, thus the amount of power lost in the HS switch supplied by the HS driver, $P_{(loss)sw_{driver(HS)}}$ (orange) is calculated by:

$$P_{(loss)sw_{driver(HS)}} = P_{(in)driver_{HS}} - P_{(loss)R_{Total(HS)}}. \quad (4.15)$$

The total power lost in the HS switch, $P_{(loss)sw_{Total(HS)}}$ (grey) must be supplied from the HS driver and the input, thus the amount of power lost in the HS switch supplied by the input, $P_{(loss)sw_{input(HS)}}$ (orange) is calculated by:

$$P_{(loss)sw_{input(HS)}} = P_{(loss)sw_{Total(HS)}} - P_{(loss)sw_{driver(HS)}}. \quad (4.16)$$

Power (mW)	20 MHz			25 MHz			30 MHz		
V_{in}	0 V	2 V	5 V	0 V	2 V	5 V	0 V	2 V	5 V
$P_{(in)driver_{HS}}$	33.32	38.30	44.94	41.62	47.85	56.15	49.93	57.41	67.39
$P_{(loss)R_{PU(HS)}}$	12.58	14.46	16.93	15.72	18.07	21.15	18.86	21.68	25.39
$P_{(loss)R_{PD(HS)}}$	11.43	11.69	12.42	14.29	14.61	15.52	17.04	17.58	18.84
$P_{(loss)R_{Total(HS)}}$	24.01	26.15	29.35	30.01	32.68	36.67	35.90	39.26	44.23
$P_{(loss)sw_{driver(HS)}}$	9.31	12.16	15.60	11.61	15.17	19.48	14.03	18.15	23.16
$P_{(loss)sw_{Total(HS)}}$	9.29	20.92	58.27	11.60	26.12	72.82	13.88	31.37	87.46
$P_{(loss)sw_{input(HS)}}$	-0.02	8.76	42.67	-0.01	10.95	53.34	-0.15	13.22	64.29

Table 4.7. LTSpice simulated supplied and dissipated powers for Sw_{LS}, in the o/c switch-node circuit. The circuit operates with V_{Driver} = 5 V, and various V_{in} and f_{sw}.

Table 4.8 shows the breakdown of the simulated, the supplied and dissipated powers, for Sw_{LS} in the o/c switch-node circuit, for various V_{in} and f_{sw}. The power input to the circuit by the LS driver is $P_{(in)driver_{LS}}$ (green). The powers lost in the LS pull-up and pull-down resistors are $P_{(loss)R_{PU(LS)}}$ and $P_{(loss)R_{PU(LS)}}$ respectively (yellow), they are combined into $P_{(loss)R_{Total(LS)}}$ (red). The power supplied from the LS driver is lost in both the LS driver resistances and the LS switch, thus the amount of power lost in the LS switch supplied by the LS driver, $P_{(loss)sw_{driver(LS)}}$ (orange) is calculated by:

$$P_{(loss)sw_{driver(LS)}} = P_{(in)driver_{LS}} - P_{(loss)R_{Total(LS)}}. \quad (4.17)$$

The total power lost in the LS switch, $P_{(loss)sw_{Total(LS)}}$ (grey) must be supplied from the LS driver and the input, thus the amount of power lost in the LS switch supplied by the input, $P_{(loss)sw_{input(LS)}}$ (orange) is calculated by:

$$P_{(loss)sw_{input(LS)}} = P_{(loss)sw_{Total(LS)}} - P_{(loss)sw_{driver(LS)}}. \quad (4.18)$$

Power (mW)	20 MHz			25 MHz			30 MHz		
V_{in}	0 V	2 V	5 V	0 V	2 V	5 V	0 V	2 V	5 V
$P_{(in)driver_{LS}}$	33.36	38.34	44.99	41.66	47.89	56.20	48.68	56.23	66.35
$P_{(loss)R_{PU(LS)}}$	12.58	14.46	16.93	15.72	18.07	21.15	1813.00	21.00	24.79
$P_{(loss)R_{PD(LS)}}$	11.43	11.69	12.42	14.29	14.61	15.52	17.14	17.52	18.62
$P_{(loss)R_{Total(LS)}}$	24.01	26.15	29.35	30.01	32.68	36.67	1830.14	38.52	43.41
$P_{(loss)sw_{driver(LS)}}$	9.35	12.20	15.64	11.66	15.21	19.52	13.41	17.71	22.95
$P_{(loss)sw_{Total(LS)}}$	9.33	20.96	58.31	11.64	26.18	72.86	13.51	30.59	86.25
$P_{(loss)sw_{input(LS)}}$	-0.02	8.76	42.67	-0.02	10.96	53.35	0.10	12.88	63.31

Table 4.8. LTSpice simulated supplied and dissipated powers for the Sw_{LS}, in the o/c switch-node circuit. The circuit operates with V_{Driver} = 5 V, and various V_{in} and f_{sw}.

Table 4.9 shows a comparison of the simulated power supplied by the input, $P_{(in)input}$ (green) and the calculated total switch loss due to the input, $P_{(loss)sw_{input(Total)}}$ (red), where:

$$P_{(loss)sw_{input(Total)}} = P_{(loss)sw_{input(HS)}} + P_{(loss)sw_{input(LS)}}. \quad (4.19)$$

Power (mW)	20 MHz			25 MHz			30 MHz		
V_{in}	0 V	2 V	5 V	0 V	2 V	5 V	0 V	2 V	5 V
$P_{(loss)sw_{input(HS)}}$	-0.02	8.76	42.67	-0.01	10.95	53.34	-0.15	13.22	64.29
$P_{(loss)sw_{input(LS)}}$	-0.02	8.76	42.67	-0.02	10.96	53.35	0.10	12.88	63.31
$P_{(loss)sw_{input(Total)}}$	-0.04	17.52	85.34	-0.03	21.91	106.69	-0.05	26.10	127.60
$P_{(in)input}$	0.00	17.56	85.38	0.00	21.95	106.72	0.00	26.16	127.65

Table 4.9. Comparison of the power supplied from the input and the calculated total switching losses due to the input. For the o/c switch-node circuit with V_{Driver} = 5 V, and various V_{in} and f_{sw}.

5. Converter Measurements with Tyndall Thin-Film Inductor, *Air-core* Inductor and SMT Chip Inductor

5.1 Comparison of Simulated and Measured Results

In this section, measured waveforms are compared with simulated waveforms for the case of an inductor fitted to the board. The circuit board tested is the "MS2 phase-1 EPC2", a 2-level buck converter, which has EPC2040 GaN eHEMT switches. The inductors tested on this board are the Coilcraft PFL1005 inductor, the low loss solenoid *air-core* inductor, and the "*MagPwr*" thin-film inductor.

The board is operated at: $f_{sw} = 30$ MHz, $I_{out} = 0.5$ A, $V_{in} = 3.3$ V, $D = 0.48$, and dead-times of $t_{d(L-H)} \approx 2.4$ ns and $t_{d(H-L)} \approx 0.2$ ns.

V_{sn} and V_{out} are recorded for the converter with the PFL1005 inductor in Figure 5.1, the *air-core* inductor in Figure 5.2, and the "*MagPwr*" inductor waveforms are shown in Figure 5.4. In the tables "excl. Drv & Ctrl" indicates the power excluding the driver and control, "incl Dynamic Drv." indicates including dynamic driver power and "excl. Drv Quiescent" means excluding the quiescent driver power.

For V_{sn} waveforms there is a good match particularly with the parasitic ringing, the waveform is measured at slightly lower voltage in the lab than for the simulation, seen when Sw_{HS} is on. There is a large amount of noise pick up in the probe ground loop when measuring the waveform for V_{out}, which is not included in the simulation. Neglecting the noise, the simulated V_{out} waveforms are valid, with exception to the PFL1005 based converter.

5.1.1 PFL1005 Inductor, 2-Level EPC2040 Buck Converter

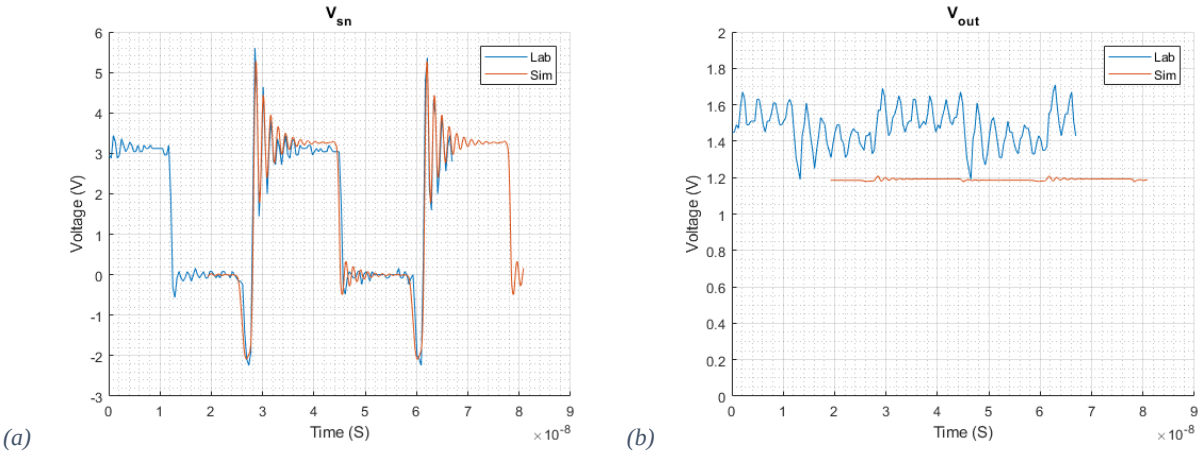


Figure 5.1. (a) Vsn and (b) Vout for 2-level EPC2040 buck converter, with PFL1005 Coilcraft inductor chip.

Table 5.1 shows the measured results and Table 5.2 shows the simulated results, for the PFL inductor on the MS2 EPC2 phase 1 circuit board operated with: $f_{sw} = 30$ MHz, $V_{in} = 3.3$ V, and $V_{Driver} \approx 5$ V. The circuit diagram is shown in Figure 3.52 on page - 63 -, and the inductor model on page - 35 -. There is not a good matchup between the simulated and measured results. The efficiency and output voltage are considerably lower for the simulated results. Thus, the supplied Coilcraft PFL1005, its LTSpice model appears to very much over-estimate loss. The model may not have been proven by them for much lower frequency operation.

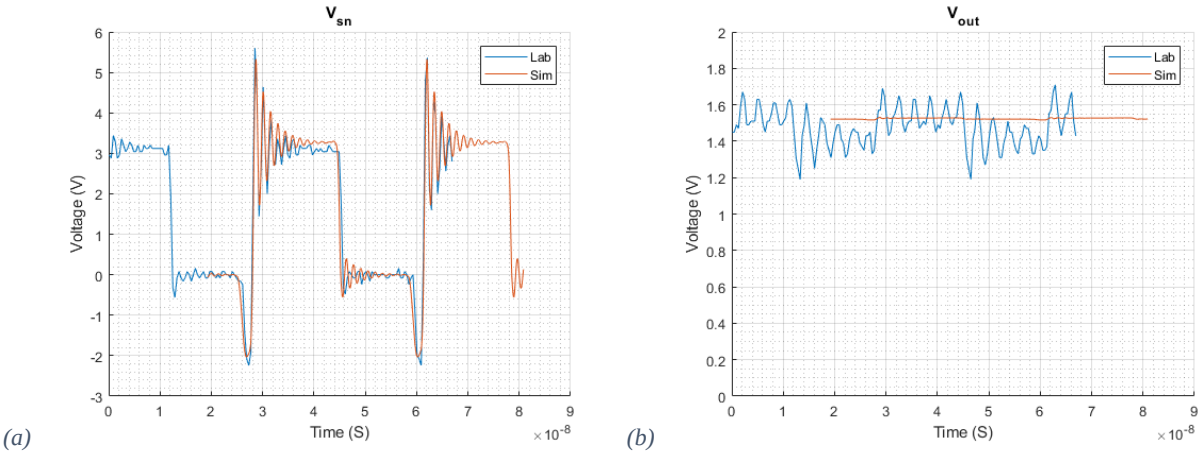
Iout	Vout	Pout	Pin	Pdriver	Efficiency (excl. Drv. & Ctrl)	Efficiency (incl. Dynamic Drv.) (excl. Ctrl.) (excl. Drv. Quiescent)
A	V	W	W	W	%	%
0	1.74	0	0.066	0.3237	0.0%	0.0%
0.5	1.46	0.73	0.9339	0.326688	78.2%	77.9%
0.9	1.39	1.251	1.6434	0.33366	76.1%	75.7%

Table 5.1. Measured PFL converter results, f_{sw} = 30 MHz, V_{in} = 3.3 V, V_{Driver} = 4.98 V.

Iout	Vout	Pout	Pin	Pdriver	Efficiency (excl. Drv. & Ctrl)	Efficiency (incl. Drv.) (excl. Ctrl.)
A	V	W	W	W	%	%
0.499	1.1913	0.5913	1.0518	0.0504	56.2%	53.6%
0.902	0.9467	0.8536	1.6427	0.0483	52.0%	50.5%

Table 5.2. Simulated PFL converter results, f_{sw} = 30 MHz, V_{in} = 3.3 V, V_{Driver} = 5 V.

5.1.2 *Air-core* Inductor, 2-Level EPC2040 Buck Converter



(a) *(b)*

Figure 5.2. (a) V_{sn} and (b) V_{out} for 2-level EPC2040 buck converter, with air-core inductor.

Table 5.3 shows the measured results and Table 5.4 shows the simulated results, for the *air-core* inductor on the MS2 EPC2 phase 1 circuit board operated with: $f_{sw} = 30$MHz, $V_{in} = 3.3$ V, and $V_{Driver} \approx 5$ V. Results for 25 MHz can be found in the appendix on page - 116 -. The circuit diagram is shown in Figure 3.37 on page - 55 - and the inductor model on page - 38 -. The converters show good efficiency if the quiescent driver power is neglected.

Iout	Vout	Pout	Pin	Pdriver	Efficiency (excl. Drv. & Ctrl)	Efficiency (incl. Dynamic Drv.) (excl. Ctrl.) (excl. Drv. Quiescent)
A	V	W	W	W	%	%
0	1.69	0	0.0495	0.325194	0.0%	0.0%
0.25	1.57	0.3925	0.4785	0.326887	82.0%	81.7%
0.5	1.47	0.735	0.9108	0.326688	80.7%	80.6%
0.75	1.39	1.0425	1.3497	0.332863	77.2%	76.8%
0.9	1.36	1.224	1.617	0.335552	75.7%	75.2%
1	1.335	1.335	1.7952	0.337644	74.4%	73.9%
1.1	1.32	1.452	1.9767	0.339636	73.5%	72.9%

Table 5.3Measured air-core converter results, f_{sw} = 30 MHz, V_{in} = 3.3 V, V_{Driver} = 4.98 V.

Iout	Vout	Pout	Pin	Pdriver	Efficiency (excl. Drv. & Ctrl)	Efficiency (incl. Drv.) (excl. Ctrl.)
A	V	W	W	W	%	%
0.250	1.63114	0.407307	0.409328	0.0459	99.5%	89.5%
0.500	1.525	0.762501	0.87201	0.049	87.4%	82.8%
0.751	1.49352	1.12092	1.29062	0.0488	86.9%	83.7%
0.900	1.4781	1.33057	1.53875	0.0485	86.5%	83.83%
0.999	1.46858	1.46717	1.70196	0.0484	86.2%	83.82%
1.090	1.4602	1.59117	1.85167	0.0473	85.9%	83.79%

Table 5.4. Simulated air-core converter results, f_{sw} = 30 MHz, V_{in} = 3.3 V, V_{Driver} = 5 V.

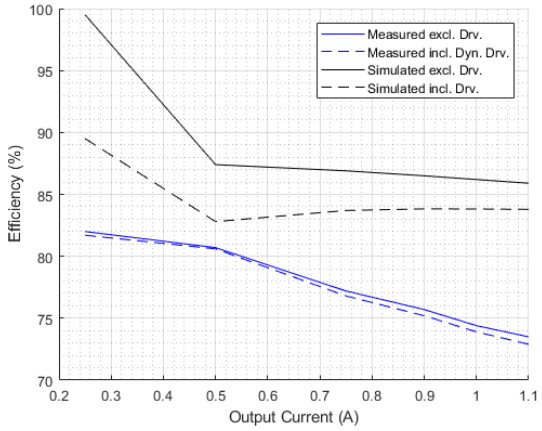
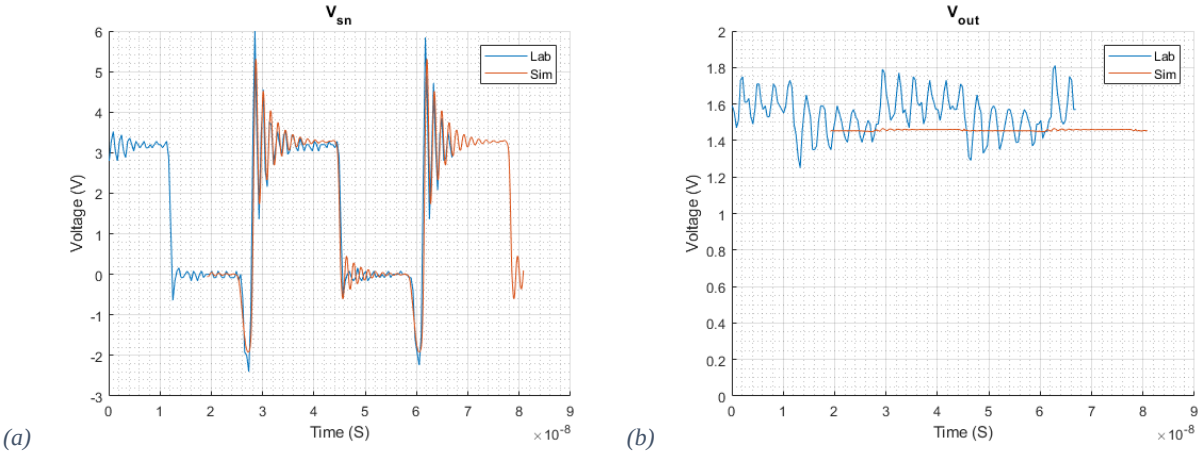


Figure 5.3. Comparison of measured and simulated efficiencies for air-core inductor, f_{sw} = 30 MHz.

The duty cycle for the simulation is set to match the measured waveform shown in Figure 5.2(a). For the converter with the *air-core* inductor, the simulations show a higher average V_{out} and efficiency with this difference becomes larger as I_{out} is increased. This indicates that there is some DC resistance that has been neglected in the simulations. The comparison between simulated and measured efficiencies for a range of I_{out} is shown in Figure 5.3.

5.1.3 Tyndall Thin-Film MS2 *MagPwr* Inductor, 2-Level EPC2040 Buck Converter



(a) *(b)*

Figure 5.4. (a) V_{sn} and (b) V_{out} for 2-level EPC2040 buck converter, with "MagPwr" inductor.

Table 5.5 shows the measured results and Table 5.6 shows the simulated results for the "*MagPwr*" inductor on the MS2 EPC2 phase 1 circuit board operated with: $f_{sw} = 30$ MHz, $V_{in} = 3.3$ V, and $V_{Driver} \approx 5$ V. Results for 20, 25, and 35 MHz can be found in the appendix on page - 116 -. The circuit diagram is shown in Figure 3.45 on page - 59 -, and the inductor model on page - 38 -. The converters show stable efficiency if the quiescent driver power is neglected, as this power does not reflect on the performance of the converter. The converter has highest efficiencies at lower I_{out}, in general the lower f_{sw} the better the performance. There is an exception of 25 MHz which is slightly better than 20 MHz at 0.25 A. At higher f_{sw}, increasing I_{out} reduces the efficiency at a faster rate.

Iout	Vout	Pout	Pin	Pdriver	Efficiency (excl. Drv. & Ctrl)	Efficiency (incl. Dynamic Drv.) (excl. Ctrl.) (excl. Drv. Quiescent)
A	V	W	W	W	%	%
0	1.75	0	0.0561	0.3325	0.0%	0.0%
0.25	1.574	0.3935	0.4851	0.333	81.1%	81.0%
0.5	1.404	0.702	0.9141	0.33405	76.8%	76.7%
0.75	1.261	0.94575	1.3563	0.3385	69.7%	69.4%
0.9	1.18	1.062	1.6335	0.34	65.0%	64.7%
1.1	1.063	1.1693	1.9899	0.347	58.8%	58.3%

Table 5.5.Measured MagPwr converter results, f_{sw} = 30 MHz, V_{in} = 3.3 V, V_{Driver} = 5 V.

Iout	Vout	Pout	Pin	Pdriver	Efficiency (excl. Drv. & Ctrl)	Efficiency (incl. Drv.) (excl. Ctrl.)
A	V	W	W	W	%	%
0.249	1.55421	0.387734	0.513535	0.0473	75.5%	69.1%
0.501	1.45202	0.727026	0.881784	0.049	82.4%	78.1%
0.749	1.38592	1.03827	1.29266	0.0488	80.3%	77.4%
0.899	1.34893	1.21308	1.54089	0.0485	78.7%	76.3%
1.094	1.30244	1.42552	1.86305	0.0483	76.5%	74.6%

Table 5.6. Simulated MagPwr converter results, f_{sw} = 30 MHz, V_{in} = 3.3 V, V_{Driver} = 5 V.

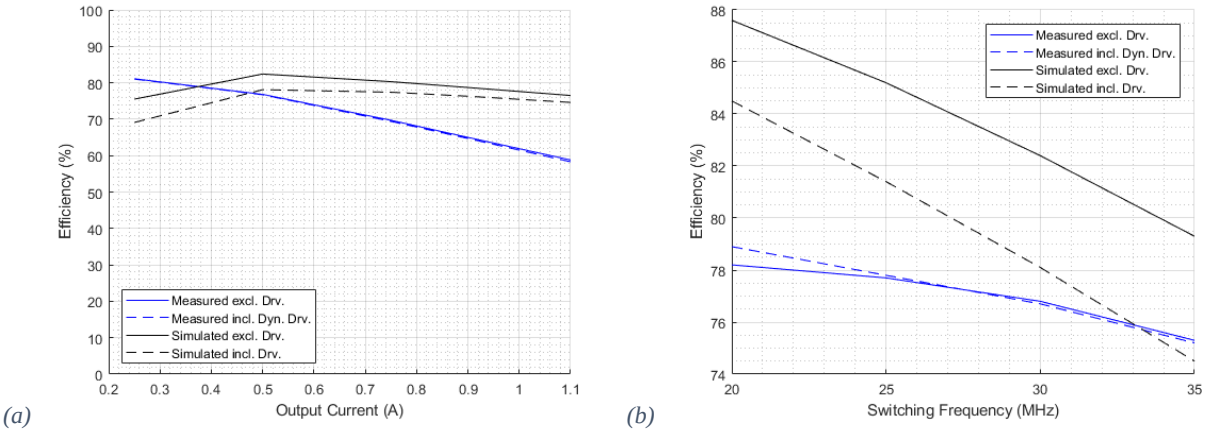


Figure 5.5. Comparison of measured and simulated efficiencies for MagPwr inductor, V_{in} = 3.3 V. (a) Over a range of currents, at f_{sw} = 30 MHz.(b) Over a range of frequencies, at I_{out} = 0.5 A.

The duty cycle for the simulation was to match the measured waveform shown in Figure 5.4(a). For the converter with the *MagPwr* inductor, the simulations show a higher V_{out} and efficiency, this difference becomes larger as I_{out} is increased. This indicates that there is some DC resistance that has been neglected in the simulations or increased loss in the *MagPwr* inductor at higher currents. The simulated model over frequency drops at a faster rate than the measured values, indicating that some of the modelled AC loss components are too large. The relationship between the efficiency and I_{out} is shown in Figure 5.5(a) and the relationship between the efficiency and f_{sw} is shown in Figure 5.5(b), both figures compare the simulated and measured results.

5.2 Conclusions Comparisons between Inductors

The *air-core* inductor is the most efficient of the inductors, followed by the *MagPwr* inductor, then PFL inductor. Comparing the three inductors at $f_{sw} = 30$ MHz, the *MagPwr* inductor has the largest DCR, as I_{out} is increased and the efficiency of the MafPwr converter drops at a larger rate than the other two. The results imply that the *MagPwr* does have lower inductor ACR losses than the PFL, and that the *air-core* inductor has very low ACR loss. When comparing the *MagPwr* and *air-core* at various frequencies, the *air-core* always has higher efficiency, and the *MagPwr* efficiency drops more rapidly with an increase in the I_{out}.

6. Simulated Performance of 2-Level and 3-Level Converters

6.1 Open-Circuit Switch-Node Converters

This section compares the simulated 2-level and 3-level open-circuit switch-node converter losses with EPC2040 (15 V GaN eHEMT) switches and *ne5* (180 nm CMOS 5 V) switches, over a range of switching frequencies. The circuits are operated with $V_{in} = 5$ V and $D = 0.36$ so that on average $V_{out} = 1.8$ V. The circuits have slightly different dead-times, the EPC2040 circuits have $t_{d(L-H)} \approx 0.25$ ns and $t_{d(H-L)} \approx 0.6$ ns, and the *ne5* circuits have $t_{d(L-H)} \approx 0.23$ ns and $t_{d(H-L)} \approx 0.9$ ns.

The results for the 2-level and the 3-level are shown in Table 6.1 and Table 6.2, respectively. Where $P_{(in)inp}$ is the bridge input power, $P_{(in)drivers}$ is the power input to the drivers, $P_{(in)boot}$ is the power input to the bootstrap, $P_{(in)total}$ is the total power input to the circuit, $P_{R(driver)}$ is the power dissipated in the pull-up and pull-down resistors in the drivers (the HS and LS had similar values), $P_{(loss)boot}$ is the power dissipated in the bootstrap diode model resistor(s), $P_{Sw_{HS}}$ is the total Sw_{HS} loss, $P_{Sw_{HS}}$ is the total Sw_{LS} loss, and P_{par} is the loss in the parasitic inductors damping resistors. For the 3-level converter both the high-side switches had similar losses, so they were combined (same for the low-side switches).

Power (mW)		$P_{(in)inp}$	$P_{(in)drivers}$	$P_{(in)boot}$	$P_{(in)total}$	$P_{R(driver)}$	$P_{(loss)boot}$	$P_{Sw_{HS}}$	$P_{Sw_{LS}}$	P_{par}	Total Loss
2-Lv EPC	20 MHz	86.40	36.70	6.60	129.70	25.30	7.80	39.40	41.60	7.41	121.51
	25 MHz	108.30	46.00	8.50	162.80	31.60	9.70	49.30	52.20	9.27	152.07
	30 MHz	129.00	55.10	10.20	194.30	37.90	11.60	59.10	62.20	11.00	181.80
	35 MHz	152.00	64.30	12.40	228.70	44.20	13.70	69.10	73.50	12.83	213.33
	40 MHz	171.80	73.40	14.10	259.30	50.30	15.30	78.80	83.20	14.33	241.93
2-Lv *ne5*	20 MHz	147.60	57.20	9.80	214.60	63.90	12.50	50.40	45.30	26.65	198.75
	25 MHz	181.00	71.40	12.60	265.00	79.90	15.60	62.50	53.00	32.91	243.91
	30 MHz	222.60	85.80	14.40	322.80	94.20	17.90	76.40	74.00	39.62	302.12
	35 MHz	247.70	99.80	17.60	365.10	110.20	21.20	86.30	74.50	45.75	337.95
	40 MHz	284.10	113.90	21.90	419.90	129.90	26.20	100.50	70.90	57.08	384.58

Table 6.1. Simulated power supplied and dissipated, for 2-level open-circuit switch-node converters, with V_{in} = 5 V, D = 0.36.

Power (mW)		$P_{(in)inp}$	$P_{(in)driver}$	$P_{(in)boot}$	$P_{(in)total}$	$P_{R(driver)}$	$P_{(loss)boot}$	$P_{Sw_{HS}}$	$P_{Sw_{LS}}$	P_{par}	Total Loss
3-Lv EPC	20 MHz	47.00	56.80	6.20	110.00	39.10	7.90	25.10	27.50	5.28	104.88
	25 MHz	57.70	71.00	7.70	136.40	49.20	9.80	29.80	34.70	6.65	130.15
	30 MHz	63.20	83.30	7.80	154.30	57.60	9.30	36.00	40.30	5.96	149.16
	35 MHz	80.70	99.40	10.90	191.00	68.90	14.10	41.50	48.10	9.46	182.06
	40 MHz	90.50	112.00	11.50	214.00	77.90	13.10	52.80	53.10	8.87	205.77
3-Lv *ne5*	20 MHz	92.00	100.00	14.70	206.70	100.60	12.90	26.20	29.60	18.60	187.90
	25 MHz	89.80	122.80	17.50	230.10	124.30	14.80	21.30	30.90	20.20	211.50
	30 MHz	122.80	147.70	17.20	287.70	145.80	13.60	52.50	38.40	19.58	269.88
	35 MHz	123.50	169.80	21.20	314.50	167.80	15.80	43.60	43.80	19.59	290.59
	40 MHz	175.40	197.50	29.60	402.50	198.20	25.90	41.70	59.30	34.63	359.73

Table 6.2. Simulated power supplied and dissipated, for 3-level open-circuit switch-node converters, with V_{in} = 5 V, D = 0.36.

The losses in the converters increase with f_{sw}. The total power dissipated is less than the total power supplied, this difference is because bootstrap power loss simulation circuit has no load on the bootstrap capacitors and they do not achieve DC steady state. Parasitic loss is larger in the *ne5* converters which have

higher capacitances and hence higher circuit ringing. The parasitic inductances' losses increase with frequency for both types of switch.

The 3-level converters have lower switch losses, similar bootstrap diode losses, and larger total driver resistance losses. The total converter losses are lower (neglecting the ringing losses) for the 3-level as are the total input powers. The EPC2040 circuits have lower losses than the *ne5* circuits.

6.2 2-Level and 3-Level Converter Power Paths with various Inductors

This section compares the simulated efficiencies and output voltages for the two converter topologies, two switch models, and four inductor models. The 2-level and 3-level converters are operated with equal f_{sw}, this means that the frequency at the switch-node is doubled for the 3-level. Efficiencies are shown with and without including the power supplied to the drivers.

The converters are operated with the following parameters, $V_{in} = 5$ V, $V_{out} = 1.8$ V, $I_{out} = 1$ A and $f_{sw} = 20$ MHz. The converter models have no control circuitry and the duty cycle ($t_{on(HS)}/T_{sw}$) is fixed, if the converters were lossless then $D = 0.36$. The efficiency for each converter is shown in Table 6.3, along with its respective average V_{out} (average), ΔV_{out} and V_{r+n} (ripple and noise ratio), and the required duty cycle for $V_{out} = 1.8$ V. For the EPC2040 converters $t_{d(L-H)} \approx 0.25$ ns and $t_{d(H-L)} \approx 0.6$ ns, and for the *ne5* converters $t_{d(L-H)} \approx 0.23$ ns and $t_{d(H-L)} \approx 0.9$ ns.

Efficiency		Without Driver Power	With Driver Power	Vout Average (V)	Vripple (V)	Vr+n	Duty Cycle
AirCore	2-Lv EPC	93.70%	92.10%	1.7909	0.0143	0.798%	38.0%
	2-Lv ne5	93.00%	90.59%	1.7906	0.0157	0.877%	38.5%
	3-Lv EPC	92.85%	90.44%	1.7952	0.0087	0.485%	39.0%
	3-Lv ne5	93.25%	89.05%	1.8046	0.0087	0.482%	39.5%
LQW	2-Lv EPC	81.18%	80.06%	1.8084	0.0144	0.796%	43.5%
	2-Lv ne5	80.65%	78.87%	1.8062	0.0158	0.875%	44.0%
	3-Lv EPC	81.84%	79.98%	1.8109	0.0092	0.508%	44.5%
	3-Lv ne5	82.43%	79.11%	1.7996	0.0087	0.483%	44.5%
PFL	2-Lv EPC	69.58%	68.76%	1.8107	0.0461	2.546%	43.5%
	2-Lv ne5	69.22%	67.92%	1.8083	0.0383	2.118%	48.5%
	3-Lv EPC	67.33%	65.92%	1.7122	0.025	1.460%	50.0%
	3-Lv ne5	67.62%	65.11%	1.7032	0.0194	1.139%	50.0%
MagPwr	2-Lv EPC	86.44%	85.15%	1.7965	0.0251	1.397%	41.0%
	2-Lv ne5	85.81%	83.77%	1.7957	0.0151	0.841%	41.5%
	3-Lv EPC	86.40%	84.32%	1.8014	0.0226	1.255%	42.0%
	3-Lv ne5	86.79%	83.13%	1.8052	0.0152	0.842%	42.5%

Table 6.3. Simulated efficiencies of converter topologies, switches, and inductors, including V_{out}, $V_{outRipple}$ and duty cycle.

Operated with $V_{in} = 5$ V, $V_{out} = 1.8$ V, $I_{out} = 1$ A, and $f_{sw} = 20$ MHz.

The *air-core* inductor (page - 38 -) is the most efficient of the inductors followed by the thin-film *MagPwr* (page - 38 -), then the Murata LQW (page - 37 -), and the least efficient is the Coilcraft PFL (page - 35 -) inductor. The EPC2040 (page - 22 -) switches are more efficient than the *ne5* (page - 22 -) switches. Between the two converter topologies, the 3-level without driver power is sometimes more efficient than the 2-level, and their efficiencies are close. When the drivers' input powers are included though, the efficiencies of all the converters drop, and the 3-level which has double the driver count drops by a larger degree. The 3-level has half the output voltage ripple of the 2-level.

The 3-level converters have smaller V_{r+n}, than the 2-level as expected because the inductors in the 3-level converters have a doubled effective frequency. Apart from the PFL1005, V_{r+n} is less than 1%; if the application of the converters required a small V_{r+n}, perhaps for the PFL1005 the reduction in V_{r+n} would justify the loss in efficiency in using a 3-level converter. As noted on page - 96 - the PFL inductor converters performed better in the lab than in simulation.

6.3 Efficiency over Switching Frequency and Load for 2-Level and 3-Level Converters

The following sections will compare; the 2-level converter and 3-level converter, with and without driver power, a comparison between the different inductors, a comparison between the two switch models, and a comparison between the 2-level converter and 3-level converter, all over frequency.

The efficiencies comparison for the 2-level converter and 3-level converter, with EPC2040 switches and the Tyndall *MagPwr* inductor, including driver powers, are of particular interest in this thesis. These efficiencies will be examined first. The simulated results of these models provide a very good match up with measured results as shown in chapter 5. As the inductor saturation effects are not included in the models, the Tyndall *MagPwr* inductor results are only valid to < I_{sat}~1.1 A.

6.3.1 Comparison of 2-Level and 3-Level Converter with EPC2040 Switch and *MagPwr* Inductor

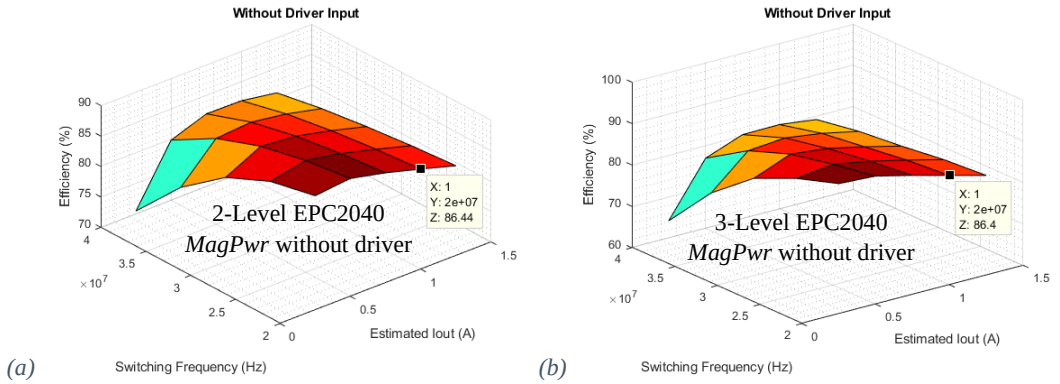


Figure 6.1.The efficiencies of (a) the2-Level converter (D = 0.41) and (b) the3-Level converter (D = 0.42), with the EPC2040 switches and the MagPwr inductor, for various I_{out} and f_{sw}, without driver power included.

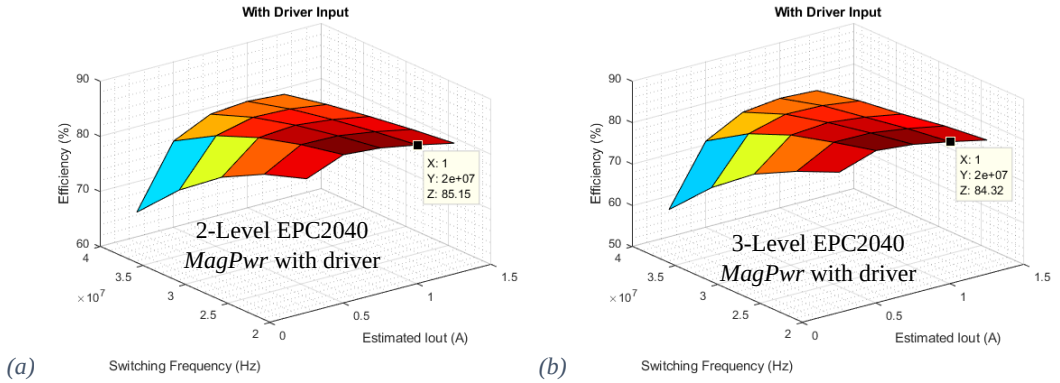


Figure 6.2. The efficiencies of (a) the 2-Level converter (D = 0.415) and (b) the3-Level converter (D = 0.425), with the EPC2040 switches and the MagPwr inductor, for various I_{out} and f_{sw}, with driver power included.

The highest efficiencies for each of the converters occur at the lowest f_{sw} and with low I_{out} (around 0.5 A). The relationship between the efficiency and the f_{sw} is clear, higher f_{sw} results in higher switching and driver losses. The 3-level converter including driver input power has the lowest efficiency point (under 60%) when $f_{sw} = 40$MHz.

As I_{out} increases, the conduction losses in the converter also increase. Increasing I_{out} also increases P_{out} and the losses that are independent of I_{out} (e.g. driver losses) have a smaller effect on efficiency. For larger values of I_{out} the losses due to the increase in f_{sw} have less of an impact on the converter efficiency. Comparing the efficiencies for $I_{out} = 1.25$ A versus $I_{out} = 0.25$ A; as f_{sw} increases, the efficiency falls at a greater rate at $I_{out} = 0.25$ A.

Figure 6.3 shows the delta in efficiencies (3-level efficiency minus 2-level efficiency), Figure 6.3(a) includes the driver input power and Figure 6.3(b) excludes the driver input power. The 3-level converter has the greatest improvement in efficiency when the I_{out} and the f_{sw} are low and the driver input power is excluded. When the driver input power is included the 3-level converter always has a lower efficiency of the 2-level converter with the worst results for large I_{out} and f_{sw}.

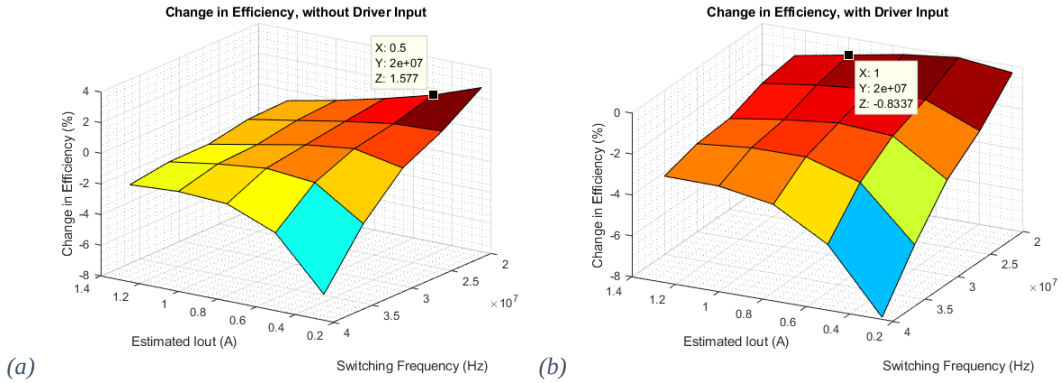


Figure 6.3. Change in efficiency for the MagPwr inductor with the EPC2040 switches, from 2-level to 3-level converter, (a) excluding driver input power and (b) including driver input power.

6.3.2 Comparison of Inductor Models, in a 2-Level Converter with EPC2040 Switches

This section compares the efficiencies (including driver input power) of the four inductors in a 2-level converter with EPC2040 switches, for various I_{out} and f_{sw}. The efficiencies are shown in Figure 6.4 for the *air-core* inductor and the LQW inductor, and in Figure 6.5 for the PFL inductor and the *MagPwr* inductor.

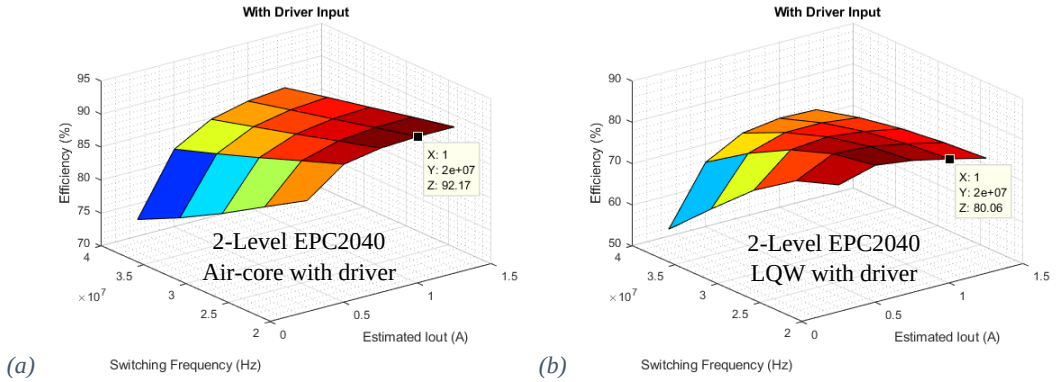


Figure 6.4. The efficiencies of the 2-Level converter with the EPC2040 switches for various I_{out} and f_{sw},

with driver power included, with (a) the air-core inductor (D = 0.38) and (b) the LQW inductor (D = 0.435).

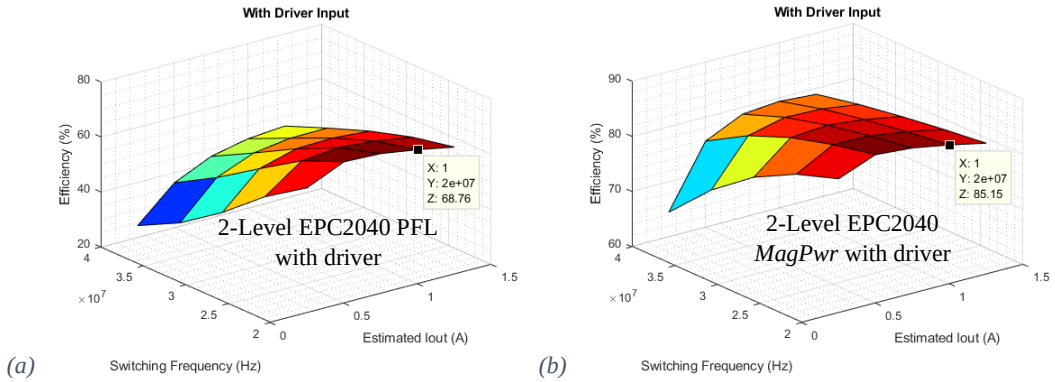


Figure 6.5. The efficiencies of the 2-Level converter with the EPC2040 switches for various I_{out} and f_{sw}, with driver power included, with (a) the PFL inductor (D = 0.435) and (b) the MagPwr inductor (D = 0.41).

The most efficient inductor is the *air-core*, followed by the *MagPwr* inductor, then the LWQ inductor and with the PFL inductor is the least efficient. The *air-core* is the only inductor that has its highest efficiency at a higher I_{out} value (1 A) due to its very low DCR (page - 38 -) and the absence of core material loss.

The highest efficiencies of the LQW, PFL, and *MagPwr* inductors occur at $I_{out} = 0.5$ A and $f_{sw} = 20$ MHz. For high frequencies (40 MHz), the highest efficiencies occur at $I_{out} = 1.25$ A (excluding the *air-core*). These peak efficiencies at highest frequency indicate that there is a balance between the conduction losses (based on RMS current) and the losses proportional to f_{sw}.

The efficiencies of converters with *air-core* and *MagPwr* inductors are the least effected by the increase in f_{sw}, because these inductors have low ACR values. The efficiencies of the converter with the LQW inductor is influenced by f_{sw} more than the *MagPwr* converter, but not as much as the PFL converter. The PFL inductor model's ACR increases rapidly with frequency, thus it is clear the PFL inductor model is not suited to high frequencies.

6.3.3 Comparison of Inductor Models, in a 3-Level Converter with EPC2040 Switches

This section compares the efficiencies (including driver input power) of the four inductors in a 3-level converter with EPC2040 switches, for various I_{out} and f_{sw}. The efficiencies are shown in Figure 6.6 for the *air-core* and the LQW inductor and in Figure 6.7 for the PFL and the *MagPwr* inductor.

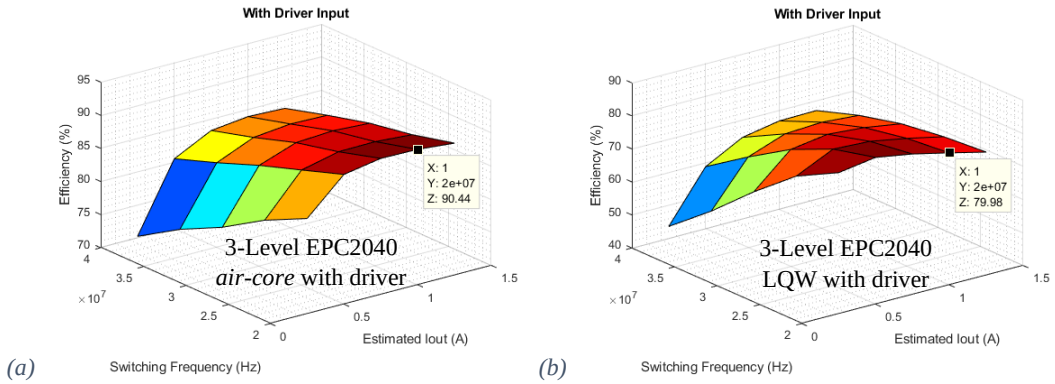


Figure 6.6.The efficiencies of the 3-Level converter with the EPC2040 switches for various I_{out} and f_{sw}, with driver power included, with (a) the air-core inductor (D = 0.39) and (b) the LQW inductor (D = 0.445).

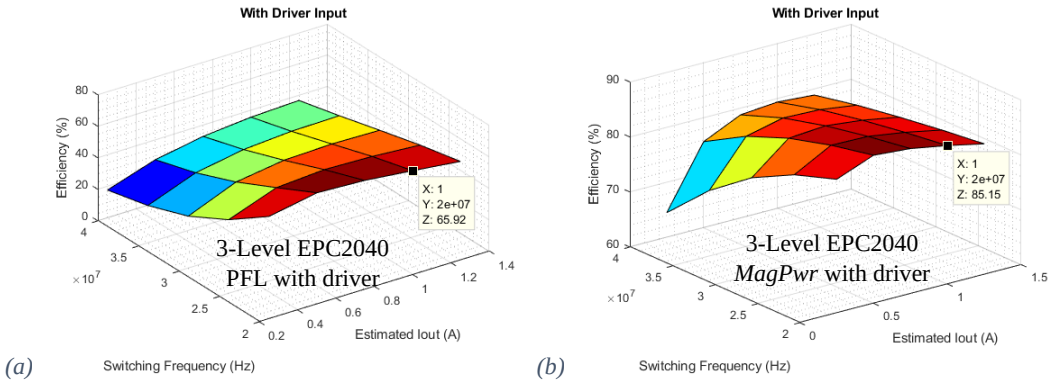


Figure 6.7. The efficiencies of the3-Level converter with the EPC2040 switches for various I_{out} and f_{sw}, with driver power included, with (a) the PFL inductor (D = 0.5) and (b) the MagPwr inductor (D = 0.42).

The overall results of this section are the same as the previous sub-section with the following differences; there is a larger drop-off of efficiency as f_{sw} increases, because when $f_{sw} = 20$ MHz the inductors see an effective switching frequency (f_{Leff}) of 40 MHz. The *air-core* which has the lowest ACR still loses a large amount of efficiency due to the increase of f_{sw}. The efficiency: I_{out} relationship is the same as the previous section. For the 3-level PFL converter, the efficiency was so low that no value of duty of cycle would allow $V_{out} = 1.8$ V, so duty cycle was set to the maximum value of 0.5.

6.3.4 Comparison of EPC2040 and *ne5* Switch Converters with *MagPwr* Inductors

This section compares the efficiencies (including driver input power) of the EPC2040 and *ne5* switches, in both the 2-level and 3-level converter with *MagPwr* inductor, for various I_{out} and f_{sw}. The efficiencies are shown in Figure 6.8 for the 2-level and Figure 6.9 for the 3-level.

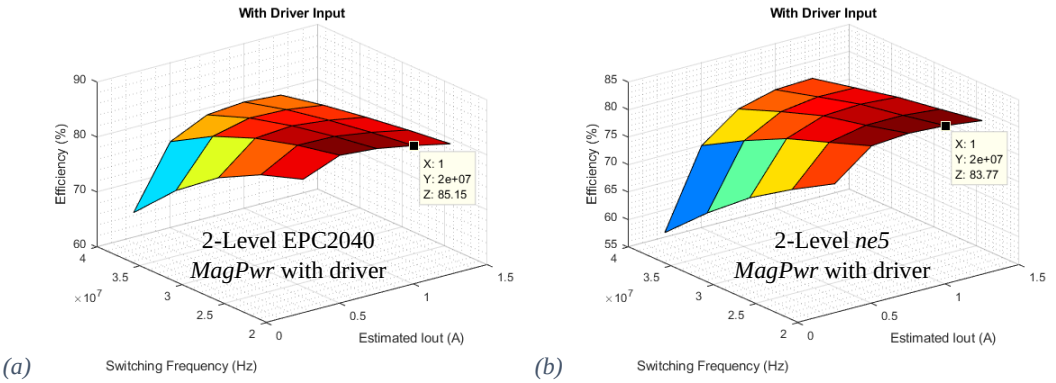


Figure 6.8. The efficiencies of the 2-Level converter with the MagPwr inductor for various I_{out} and f_{sw}, with driver power included, with (a) the EPC2040 switches (D = 0.41) and (b) the ne 5 switches (D = 0.415).

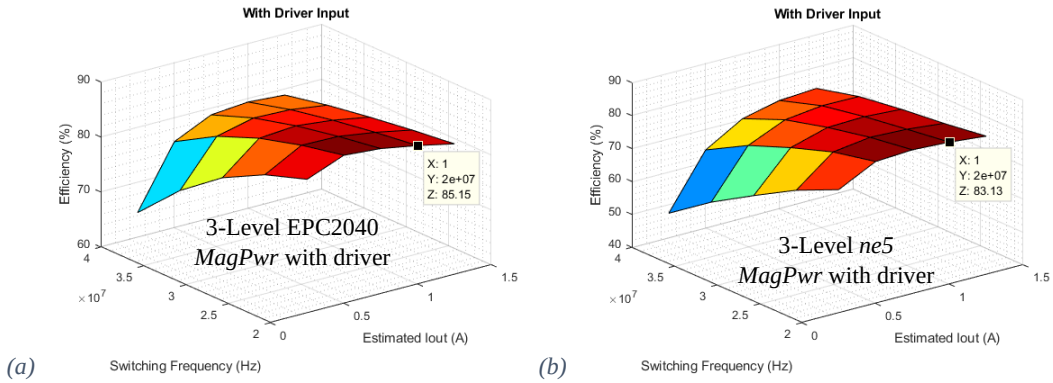


Figure 6.9. The efficiencies of the 3-Level converter with the MagPwr inductor for various I_{out} and f_{sw}, with driver power included, with (a) the EPC2040 switches (D = 0.42) and (b) the ne 5 switches (D = 0.425).

The general efficiency relationships are the same for both switches for both f_{sw} and I_{out}, the difference is that *ne5* is less efficient. As the W/L ratio of the *ne5* switch was selected to have the same r_{on} as the EPC2040 switch, the DC losses in the EPC2040 and *ne5* are approximately the same. As calculated in chapter 3.5.2 on page - 50 - C_{oss} of the *ne5* is 76% larger than the EPC2040, this results in larger frequency dependent losses when using the *ne5* switches.

6.3.5 Comparison of 2-level and 3-Level Converters for the Same Inductor Frequency

This sub-section compares the efficiencies of the 2-level converters and the 3-level converters for the same inductor frequency (f_{Leff}). To have the same f_{Leff} in the 3-level converter f_{sw} is half of the equivalent for the 2-level. Using the f_{Leff} allows a comparison of the two topologies efficiencies, including one of the key advantages of the 3-level topology, $f_{Leff} = 2f_{sw}$. Considering f_{Leff} the 3-level converter has a reduction in frequency dependent losses. These efficiency comparisons use EPC2040 switches, for various I_{out} and f_{Leff}, for all the inductors: the *air-core* in Figure 6.10, the LQW in Figure 6.11, the PFL in Figure 6.12, and the *MagPwr* in Figure 6.13.

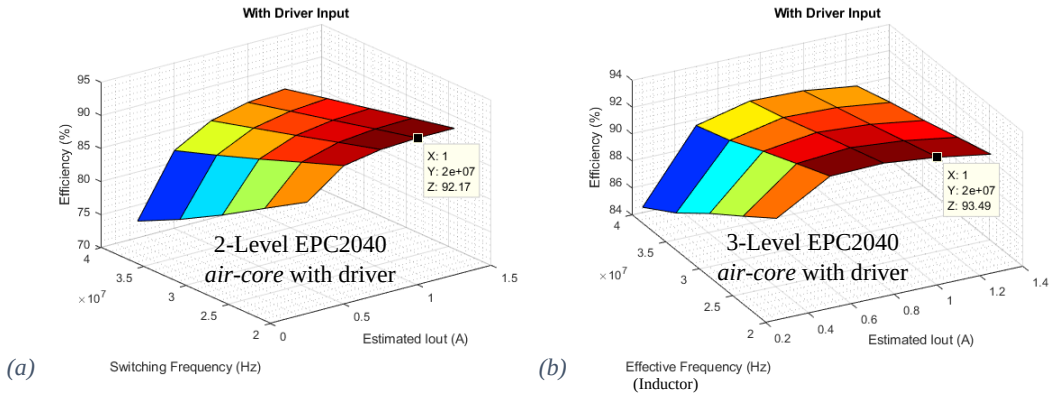


Figure 6.10. The efficiencies of (a) the 2-Level converter (D = 0.38) and (b) the 3-Level Converter (D = 0.39), with the EPC2040 switches and the air-core inductor, for various I_{out} and f_{Leff}, with driver power included.

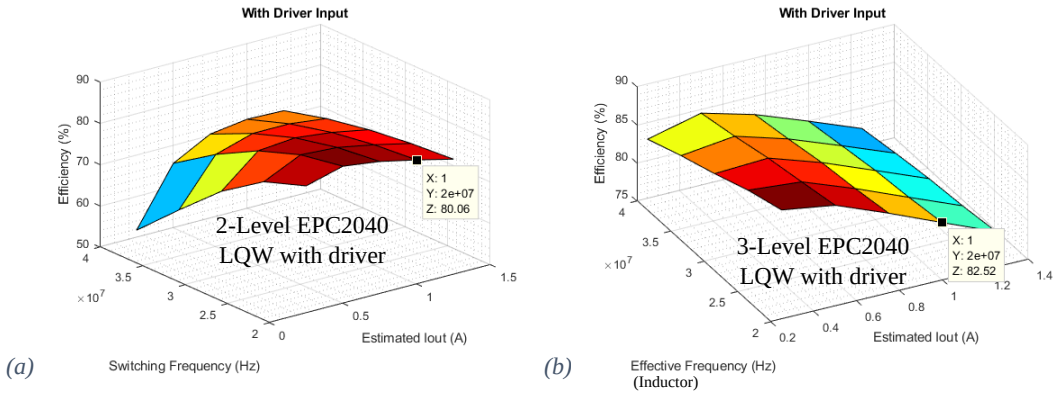


Figure 6.11. The efficiencies of (a) the 2-Level converter (D = 0.38) and (b) the 3-Level Converter (D = 0.39), with the EPC2040 switches and the LQW inductor, for various I_{out} and f_{Leff}, with driver power included.

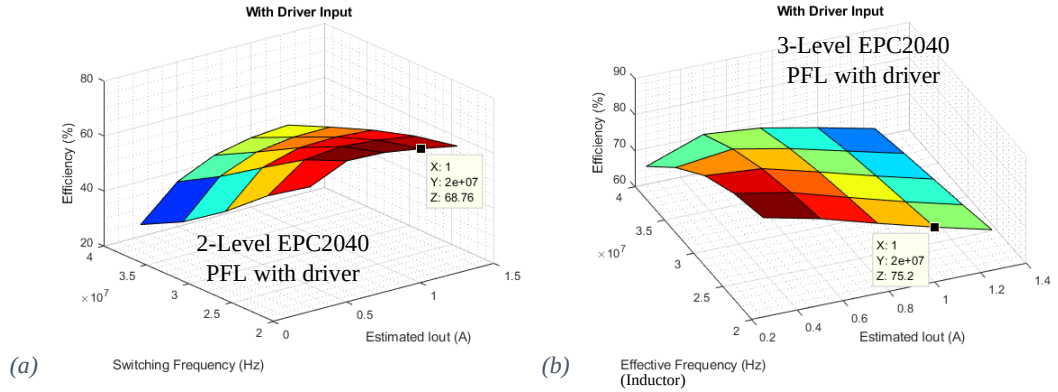


Figure 6.12. The efficiencies of (a) the 2-Level converter (D = 0.435) and (b) the 3-Level Converter (D = 0.50), with the EPC2040 switches and the PFL inductor, for various I_{out} and f_{Leff}, with driver power included.

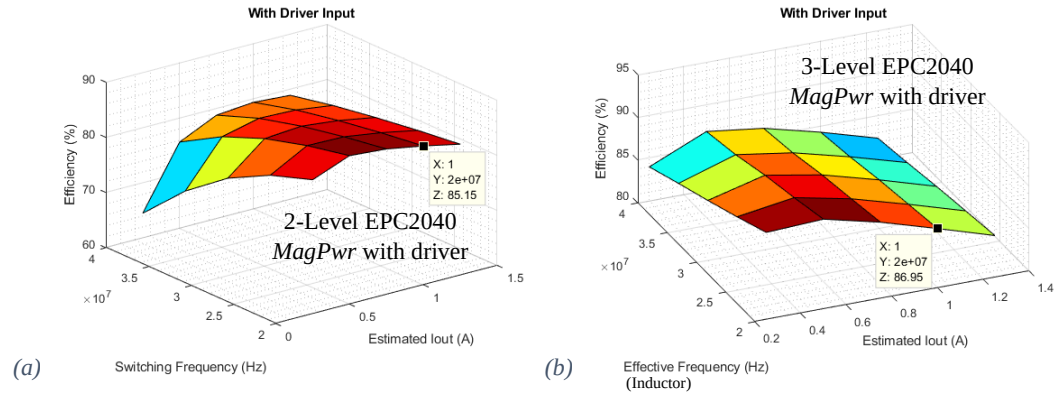
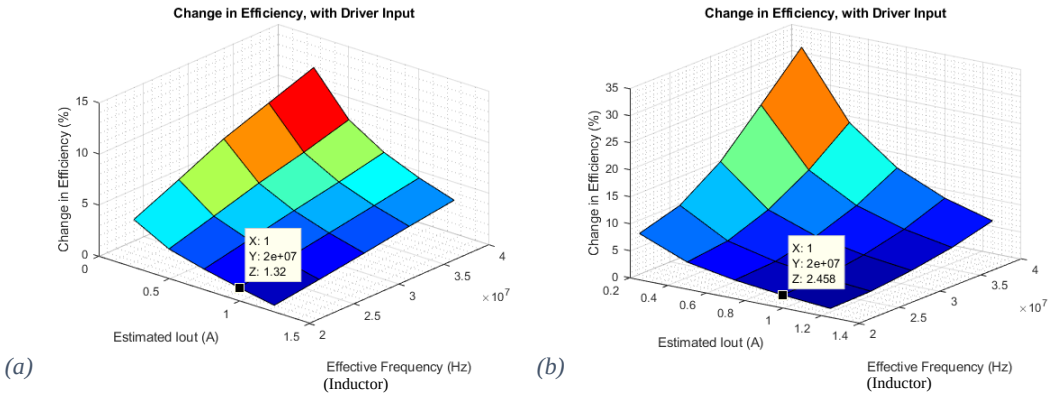


Figure 6.13. The efficiencies of (a) the 2-Level converter (D = 0.41) and (b) the 3-Level Converter (D = 0.42), with the EPC2040 switches and the MagPwr inductor, for various I_{out} and f_{Leff}, with driver power included.

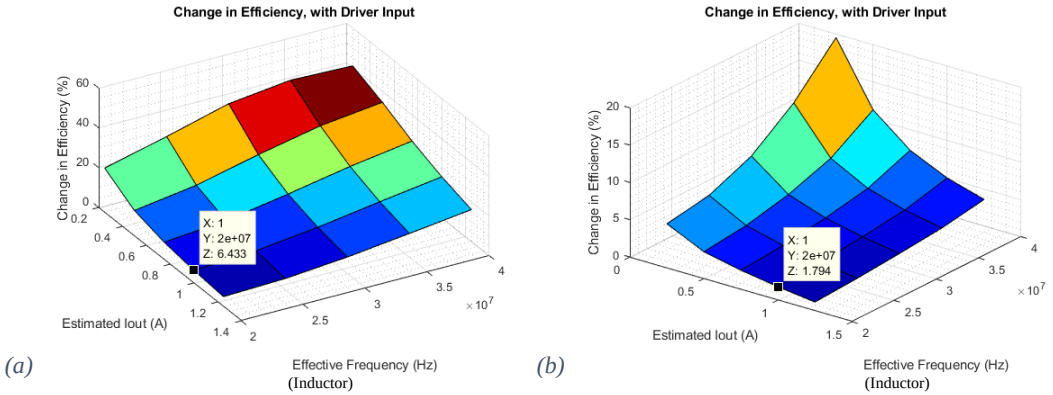
These graphs demonstrate the advantage of the 3-level converter when operated at the same f_{Leff} as the 2-level converter; for each of the inductors there is an increase in efficiency for the 3-level. Operating the 3-level at half f_{sw} decreases the switching losses, the gate losses, and the driver losses. The inductor AC losses are also reduced because of the smaller switch-node driving voltage and effective doubled inductor duty cycle at the switch-node. Even the PFL 3-level converter manages to achieve 70%, and as its ACR

increases with f_{sw} this inductor benefits the most by this application. There is a much smaller degradation in efficiency with an increase in f_{Leff} compared to the 2-level.



(a) *(b)*

Figure 6.14. Change in efficiency, from 2-level to 3-level converter, with the EPC2040 switches, for (a) the air-core inductor and (b) the Murata LQW inductor.



(a) *(b)*

Figure 6.15. Change in efficiency, from 2-level to 3-level converter, with the EPC2040 switches, for (a) the Coilcraft PFL1005 inductor and (b) the Tyndall thin-film MagPwr inductor.

Figure 6.14 and Figure 6.15 show the change in efficiencies (the 3-level efficiency minus the 2-level efficiency), for the various inductor models, with EPC2040 switches and driver input powers included. With low I_{out} and high f_{sw} the 3-level shows the best results. When it comes to the same effective inductor frequency the 3-level always performs better.

6.4 Simulated Loss Breakdown of 2-Level Converter with EPC2040 and *MagPwr*

Figure 6.16 shows the breakdown of losses for the 2-level converter with *MagPwr* and EPC2040. Figure 6.16(a) shows the total converter losses and Figure 6.16(b) and (c) show the losses for Sw_{HS} and Sw_{LS} respectively. This validates the accuracy of the loss breakdown methodology. The converter is operated at $f_{sw} = 20$ MHz, $I_{out} = 1$ A, $V_{in} = 5$ V, and $V_{out} = 1.8$ V.

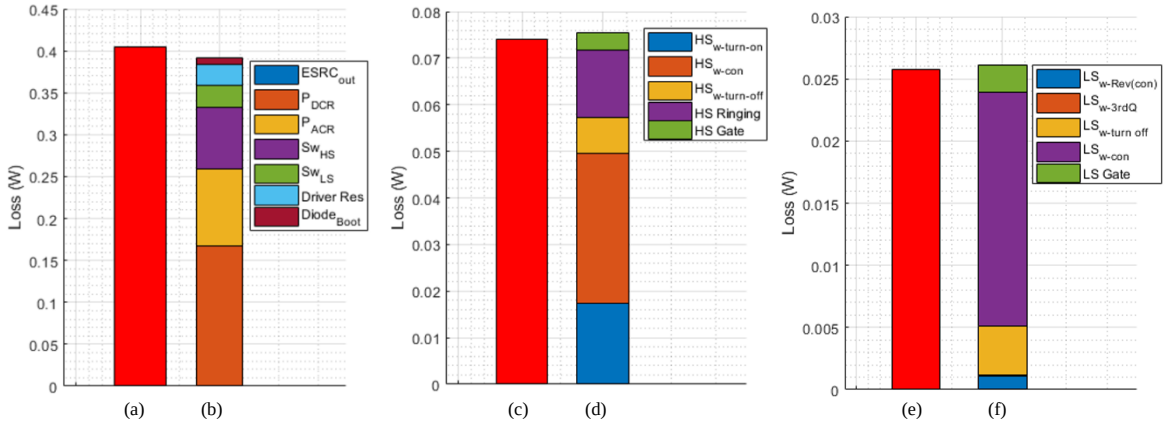


Figure 6.16. (a) The total converter loss, (b) the converter loss breakdown, (c) Sw_{HS} total loss, (d) Sw_{HS} loss breakdown, (e) Sw_{LS} total loss, and (f) Sw_{LS} loss breakdown. For the 2-level MagPwrEPC2040 converter operated at f_{sw}=20 MHz, I_{out}=1 A, V_{in}=5 V, and V_{out}=1.8 V.

Note that Sw_{LS} turn-off losses are due to the non-optimal setting in gate driver delay. Sw_{LS} could have ZVS for the case of a positive I_L value.

Figure 6.17 shows the breakdown of losses for the 3-level converter with *MagPwr* and EPC2040. Figure 6.17(a) shows all the converter losses and Figure 6.17(b) and (c) show the losses for Sw_{HS1} and Sw_{LS1} respectively. The losses for Sw_{HS1} were approximately the same as Sw_{HS2}, as are Sw_{LS} losses. This demonstrates the accuracy of the loss breakdown methodology. The converter is operated at $f_{sw} = 20$ MHz, $I_{out} = 1$ A, $V_{in} = 5$ V, and $V_{out} = 1.8$ V.

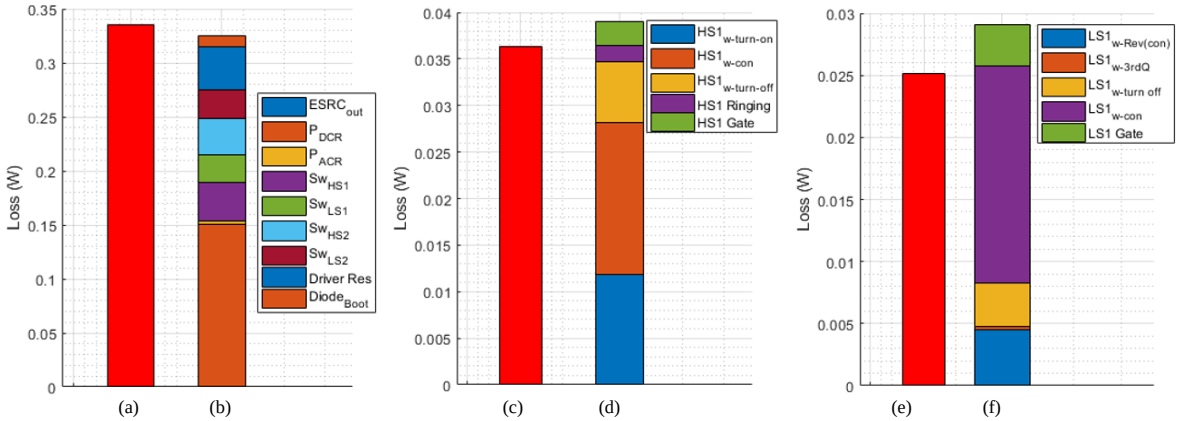


Figure 6.17. (a) The total converter loss, (b) the converter loss breakdown, (c) Sw_{HS1} total loss, (d) Sw_{HS1} loss breakdown, (e) Sw_{LS1} total loss, (f) Sw_{LS1} loss breakdown. For the 3-level MagPwrEPC2040 converter at f_{sw}=20 MHz, I_{out}=1 A, V_{in}=5 V and V_{out}=1.8 V.

6.5 Discussion on Simulated Converter Losses

For this section's results, the converters are operated at $V_{in} = 5, V_{out} = 1.8$ V, $I_{out} = 1$ A and $f_{sw} = 20$ MHz. The losses are split into three tables: Table 6.4 shows the inductor losses, Table 6.5 shows Sw_{HS} losses and Table 6.6 shows Sw_{LS} losses. HS (ring) refers to the power lost in Sw_{HS} after it has turned off due to ringing and damping. LS (Qcon) is the diode/3rd quadrant conduction. LS (off) is Sw_{LS} turn-off loss. Boot (Diode) is the loss of the bootstrap diode. The HS (gate) and LS (gate) show the power measured at the gate node, i.e. the power dissipated in the switches' internal gate resistances.

6.5.1 Inductor Losses

For the LQW inductors, the resistors R_2 and R_4 are considered with the DCR and ACR respectively (page - 37 -). For the PFL inductor, R_1 and R_2 losses are combined as the DCR losses and the losses R_{VAR1} and R_{VAR2} are combined as the ACR losses (page - 35 -).

Converter Type	Inductor Type	AirCore		LQW		PFL		MagPwr	
	Switch Type	EPC 2040	ne5	EPC 2040	ne5	EPC 2040	ne5	EPC 2040	ne5
2-Level	DCR (mW)	6.528	6.515	290.114	289.559	39.803	39.680	166.944	166.725
	ACR (mW)	11.740	11.690	15.417	15.398	632.631	633.909	91.683	91.400
	Total Loss (mW)	18.268	18.205	305.531	304.957	672.434	673.589	258.627	258.125
3-level	DCR (mW)	5.993	6.053	264.556	261.113	32.197	31.797	150.732	151.445
	ACR (mW)	0.497	0.506	0.961	1.050	598.888	593.604	2.438	2.529
	Total Loss (mW)	6.490	6.559	265.517	262.163	631.085	625.401	153.170	153.974

Table 6.4. The Inductor Losses vs. Inductors, Topology, and Switches .f_{sw} = 20 MHz, V_{in} = 5 V, V_{out} = 1.8 V, and I_{out} = 1 A.

For the inductor losses there is very little difference between the converters with the EPC2040 switches and the converters with the *ne5* switches. The DCR losses are smaller for the 3-level, due to smaller ripple on the I_{out}, regardless of the inductor or the switch used.

The ACR losses are reduced significantly in the 3-level configuration, because of the reduction magnitude of the inductor AC current, with the exception of the PFL inductor. The 3-level converter has two effects on the PFL inductor's ACR losses, the AC current is reduced and the ACR value is increased (ACR$\propto \sqrt{f}$). These two opposing effects cause the decrease in ACR losses to be less than the decrease in the other inductors.

The *air-core* inductor has the lowest total loss. The second lowest total loss is the *MagPwr* inductor. In the 2-level configuration the *MagPwr* total loss is only slightly lower than the LQW inductor. In the 3-level configuration the *MagPwr* inductor's AC losses are greatly reduced, resulting in the total loss of the *MagPwr* inductor being about half that of the LQW inductor's total loss. The LQW inductor has the highest DCR loss but its low ACR losses compensate for this. The inductor with the highest loss is the PFL. It has the second lowest DCR losses but its frequency-dependent losses are by far the largest, suggesting that it would be much better suited to lower f_{sw} operations.

6.5.2 Sw_{HS} Loss Breakdown

Table 6.5 shows the breakdown of Sw_{HS} losses as described in chapter 3.7 on page - 71 -. The converters are operated at $V_{in} = 5, V_{out} = 1.8$ V, $I_{out} = 1$ A and $f_{sw} = 20$ MHz.

Converter Type	Inductor Type	AirCore		LQW		PFL		MagPwr	
	Switch Type	EPC 2040	ne5	EPC 2040	ne5	EPC 2040	ne5	EPC 2040	ne5
2-Level	HS(turn_on) (mW)	19.152	17.240	22.170	19.045	16.220	17.317	17.274	17.887
	HS(con) (mW)	28.231	20.430	32.030	25.698	42.821	28.705	32.258	21.605
	HS(turn_off) (mW)	9.790	12.937	12.779	12.144	12.040	13.714	7.823	12.066
	HS(ring) (mW)	13.423	16.637	13.085	17.006	12.179	17.281	14.368	16.963
	HS(gate) (mW)	3.735	1.542	3.667	1.494	3.479	1.477	3.650	1.344
	Total HS Sw Loss (mW)	74.331	68.787	83.731	75.386	86.738	78.494	75.373	69.866
	HS(PU) (mW)	6.793	16.202	6.790	16.247	6.749	16.129	6.796	16.289
	HS(PD) (mW)	5.055	10.548	5.072	10.677	5.081	10.680	5.074	10.628
	Total HS Loss (mW)	86.179	95.537	95.593	102.310	98.569	105.302	87.243	96.783
3-level	HS(turn_on) (mW)	19.683	14.118	21.181	12.697	16.895	13.928	21.359	11.959
	HS(con) (mW)	28.953	20.454	32.071	22.976	33.371	23.344	32.144	24.378
	HS(turn_off) (mW)	4.501	6.447	8.588	6.824	6.473	7.835	6.642	5.896
	HS(ring) (mW)	11.175	14.214	12.838	12.251	9.350	10.115	11.496	14.691
	HS(gate) (mW)	4.867	0.388	4.865	0.117	5.348	0.220	4.884	-0.429
	Total HS Sw Loss (mW)	69.179	55.621	79.542	54.866	71.436	55.441	76.524	56.495
	HS(PU) (mW)	11.171	28.714	11.349	28.580	11.031	28.295	11.230	28.825
	HS(PD) (mW)	8.563	20.480	8.594	20.369	8.473	20.127	8.577	20.615
	Total HS Loss (mW)	88.912	104.814	99.485	103.814	90.941	103.864	96.330	105.935

Table 6.5. Sw_{HS} Losses vs. Inductors, Topology and Switches. f_{sw} = 20 MHz, V_{in} = 5 V, V_{out} = 1.8 V, and I_{out} = 1 A.

For the 3-level converter Sw_{HS1} and Sw_{HS2} loss components are approximately the same, so they are combined into one loss value.

The EPC2040 switches have a greater total Sw_{HS} loss than the *ne5* (excluding the driver resistance losses). The 2-level configuration has slightly lower total HS loss than the 3-level. Each component loss of the switch in the 3-level configuration is approximately half of the 2-level switch equivalent loss. For example, the EPC2040 *air-core* turn on loss, 2-level: 19.152 mW and 3-level: 19.683 mW (combined).

The major difference between the 2-level and 3-level converters is because of the driver pull-up and pull-down losses. The driver resistance losses are slightly less for each of the two 3-level drivers than the equivalent single 2-level driver. Using the EPC2040 switches and *air-core* inductor as an example in the 2-level configuration the total (pull-up and pull-down) driver resistance losses are: 11.848 mW and in the 3-level configuration, the total driver resistance losses are 19.733 mW, almost double.

The largest difference in losses between the *ne5* and the EPC2040 switches, is that the *ne5* switch has over double the pull-up and pull-down losses of the EPC2040 switches. In the 3-level configurations there are twice the number drivers which results in the *ne5* switches in 3-level converters having the highest driver losses. Driver losses will increase with f_{sw}, and at high f_{sw} this difference will be larger. The two switch models have similar turn-on losses in the 2-level configuration. The conduction, turn-off, and gate losses are slightly higher for the EPC2040 switches. As the switches are modelled to have the same r_{on} and the current through them is similar, this conduction loss difference arises from the ringing on the switches as they begin to conduct. The *ne5* switches have higher ringing losses than the EPC2040 switches, because of the *ne5* switches' larger capacitances.

6.5.3 Sw_{LS} Loss Breakdown

Table 6.6 shows the breakdown of Sw_{LS} losses as described in chapter 3.7 on page - 71 -.. The converters are operated at $V_{in} = 5$, $V_{out} = 1.8$ V, $I_{out} = 1$ A and $f_{sw} = 20$ MHz.

Converter Type	Inductor Type	AirCore		LQW		PFL		MagPwr	
	Switch Type	EPC 2040	ne5	EPC 2040	ne5	EPC 2040	ne5	EPC 2040	ne5
2-Level	LS(rev_con) (mW)	1.323	1.437	1.191	1.333	0.680	0.803	1.130	1.272
	LS(Qcon) (mW)	0.362	0.547	-0.259	0.049	0.190	0.227	0.071	0.445
	LS(off) (mW)	3.317	10.429	5.404	21.142	6.869	20.074	3.888	10.478
	LS(con) (mW)	19.359	12.277	17.773	11.428	16.002	10.131	18.841	12.080
	LS(gate) (mW)	2.270	-9.619	2.217	-9.963	2.561	-8.439	2.218	-9.763
	Total LS Sw Loss (mW)	26.631	15.070	26.327	23.989	26.301	22.796	26.148	14.511
	LS(PU) (mW)	7.694	18.564	7.690	18.701	7.400	17.785	7.697	18.667
	LS(PD) (mW)	5.957	13.615	5.946	13.613	5.647	12.900	5.918	13.589
	Total LS Loss (mW)	40.282	47.249	39.963	56.303	39.348	53.481	39.763	46.767
3-level	LS(rev_con) (mW)	8.994	7.486	10.185	8.742	11.184	7.980	8.700	8.934
	LS(Qcon) (mW)	0.935	1.199	0.700	0.358	1.174	0.319	0.609	0.417
	LS(off) (mW)	1.119	6.003	2.171	12.850	-0.129	11.039	1.337	13.646
	LS(con) (mW)	36.364	24.365	33.521	22.331	28.724	18.929	35.017	23.262
	LS(gate) (mW)	6.647	4.202	6.822	4.120	7.178	-3.570	6.811	-4.293
	Total LS Sw Loss (mW)	54.059	43.255	53.399	48.402	48.130	34.696	52.473	41.966
	LS(PU) (mW)	11.384	27.460	11.406	27.421	11.333	27.382	11.349	27.585
	LS(PD) (mW)	8.753	19.660	8.714	19.671	8.665	19.560	8.697	19.718
	Total LS Loss (mW)	74.195	90.375	73.519	95.494	68.128	81.638	72.518	89.269

Table 6.6. Sw_{LS} Losses vs. Inductors, Topology and Switches. f_{sw} = 20 MHz, V_{in} = 5 V, V_{out} = 1.8 V, and I_{out} = 1 A.

For the 3-level converter, the Sw_{LS1} and Sw_{LS2} loss components are approximately the same, so they are combined into a single component loss value.

The EPC2040 switches have a greater total Sw_{LS} loss (excluding the driver loss) than the *ne5* switches. The EPC2040 switches have a total Sw_{LS} loss at an approximately constant value of 26 mW, regardless of inductor or topology configuration while the *ne5* total Sw_{LS} loss values vary a lot more.

The major difference between the 2-level and 3-level converters is because of the driver pull-up and pull-down losses. The driver resistance losses are lower for each of the two 3-level drivers, than the equivalent single 2-level driver. The total driver losses for the 3-level converter is larger than that of the 2-level converter.

The largest difference between the *ne5* and the EPC2040 switches, is that the *ne5* switch has over double the pull-up and pull-down losses of the EPC2040 switches. In the 3-level configurations there are twice the number of drivers. This results in the *ne5* switches in 3-level converters having the highest driver losses. Driver losses will increase with f_{sw}, at high f_{sw} this difference will be larger. The gate losses with the *ne5* switches had a simulation error whereby power was being supplied to the gate, this will affect the other loss components so the *ne5* switch loss components are not considered.

7. Conclusions

The design considerations for a 20-40 MHz PwrSiP POL DC-DC converter with a custom fabricated novel thin-film Co-Zr-Ta-B inductor have been explored. The full power path design process of topology selection, component modelling, losses evaluation and match-up with real hardware has been conducted.

A very large (12 mm by 6 mm diameter) ultra-low loss air-core solenoid was wound to assess converter power path losses by excluding most of the inductor copper and magnetic core losses. A selection of candidate 0402 SMT chip inductors for the 20-40 MHz range was made by a datasheet survey. Coilcraft's PFL1005 inductor was selected for its low DCR value (50 mΩ max as per the datasheet) but its LTSpice model proved in simulation to have much higher resistance, 481.2 mΩ ACR at 20 MHz. The PFL inductor's simulated models subsequently did not match the measured device (which showed much lower loss in circuit). Murata's LQW18CN55NJ00 performed quite well and although it had the largest DCR value, its ACR was small enough such that it could operate in the frequency range of interest. Tyndall's thin-film Magnetics-on-Silicon, multi-laminated Co-Zr-Ta-B "*MagPwr* MS2" inductor, was the most efficient after the air-core inductor. The *MagPwr* inductor's ACR to DCR ratio was measured to be very low over frequency. The models for the *air-core*, PFL, and *MagPwr* inductors were validated in the lab on the "EPC MS2" prototype board, a 2-level buck converter using EPC2040 switches.

A comparison between a 5V NMOS *ne5* device from XFAB 180 nm Bulk CMOS process and a discreet 15 V GaN enhancement mode switch (EPC2040 e-HEMT) for use in a buck converter was desired. To make the comparison between the two switches, the W/L ratio of the *ne5* switches, was selected to give the two types of switches an equal on-resistance, measured in the same simulated conditions to be approximately 24 mΩ with the W/L ratio of the *ne5* set to 125 mm/0.5 µm. An in-depth examination of the *ne5* switch including its capacitances and diode reverse recovery was performed. In the simulated results, the *ne5* had higher switching losses than the EPC2040 and in particular the *ne5* switch drew considerably more power from the drivers, because of a higher gate charge. It also had larger capacitances than the EPC2040 switch, which lead to larger ringing voltages in the converter and therefore overall the 15 V EPC2040 GaN HEMTs proved to be a better option with considerably higher efficiency. The various types of switch loss that occur in a synchronous buck converter were analytically explained and modelled. The key differences between CMOS and e-HEMT switches have been detailed, and the losses associated with both have been examined in simulation. Lumped circuit models for the Peregrine Semiconductor gate drivers were created from datasheet parameters and additionally the bootstrapped bias supply. LTSpice was used for simulations. MATLAB was used to invoke LTSpice over frequency and over output current to enable data exchange for the design space explorations. MATLAB was used for subsequent analyses on the imported waveforms.

Open-circuit switch-node (no inductor fitted) converter simulations and measurements were performed to gain insight into the converter switching losses without inductor, dead-time, or conduction losses present. Then the circuit boards were measured with the *air-core*, "*MagPwr*" and PFL inductors fitted, for full converter measurements. The measurements also allowed the modelling of the PCB parasitic inductances and damping effects, by matchup of ringing waveforms. For the air-core and "*MagPwr*" inductor-based converters a very good match was achieved between hardware and simulations.

The operation and possible benefits and drawbacks of the 3-level buck converter are explained. The switches experience half the voltage stress, allowing a possible reduction in switch losses or the use of smaller switches. The 3-level is best utilised in large step-down ratios, where the 3-level doubles a small duty cycle. The inductor sees a reduction in volt-seconds and would have an effective frequency double

that of the switches to give up to four times benefit in value and size. If correctly used, the penalty of the additional switches, drivers and capacitors can reduce overall losses and probably converter footprint. The accuracy of the various 2-level converter simulations proved all the components models which were developed. The same component models were then implemented in 3-level converter simulations, to perform design space exploration, for 3-level versus 2-level.

The "*MagPwr*" thin-film operated with high efficiency over the 20-40 MHz range of switching frequencies and performed better than the commercially available surface-mounted chip inductors. The EPC2040 (eHEMT) had a lower equivalent energy output capacitance that the *ne5* (CMOS) with the same on-resistance and gave higher efficiency, but this is a discreet switch, and the *ne5* can be implemented in a monolithic CMOS PMIC. The 3-level buck converter does not perform as well as the 2-level, with the same switching frequency, but with the same effective inductor (switch-node) frequency (each switch at half frequency) the 3-level was shown to improves the converter's efficiency.

8. Appendix

8.1 *Air-core* Inductor Converter Measured Results for 25 MHz.

Iout	Vout	Pout	Pin	Pdriver	Efficiency (excl. Drv. & Ctrl)	Efficiency (incl. Dynamic Drv.) (excl. Ctrl.) (excl. Drv. Quiescent)
A	V	W	W	W	%	%
0	1.68	0	0.0429	0.288824	0.0%	0.0%
0.25	1.59	0.3975	0.4554	0.293088	87.3%	86.5%
0.5	1.49	0.745	0.8778	0.293037	84.9%	84.5%

Table 8.1. Measured Air-core converter results, f_{sw} = 25 MHz, V_{in} = 3.3 V, V_{Driver} = 5.076 V.

Iout	Vout	Pout	Pin	Pdriver	Efficiency (excl. Drv. & Ctrl)	Efficiency (incl. Drv.) (excl. Ctrl.)
A	V	W	W	W	%	%
0.254	1.65168	0.419702	0.425192	0.0371	98.7%	90.8%
0.507	1.54491	0.782547	0.868895	0.0404	90.1%	86.1%

Table 8.2. Simulated Air-core converter results, f_{sw} = 25 MHz, V_{in} = 3.3 V, V_{Driver} = 5 V.

8.2 Tyndall Thin-Film MS2 *MagPwr* Inductor Converter Results for 20 MHz.

Note that the quiescent driver power was larger than any of the other results leading to strange efficiency results.

Iout	Vout	Pout	Pin	Pdriver	Efficiency (excl. Drv. & Ctrl)	Efficiency (incl. Dynamic Drv.) (excl. Ctrl.) (excl. Drv. Quiescent)
A	V	W	W	W	%	%
0	1.7	0	0.0561	0.2500096	0.0%	0.0%
0.25	1.545	0.38625	0.4785	0.24156	80.7%	82.2%
0.5	1.399	0.6995	0.8943	0.24255	78.2%	78.9%
0.75	1.253	0.93975	1.3233	0.245223	71.0%	71.3%

Table 8.3. Measured MagPwr converter results, f_{sw} = 20 MHz, V_{in} = 3.3 V, V_{Driver} = 5.14 V.

Iout	Vout	Pout	Pin	Pdriver	Efficiency (excl. Drv. & Ctrl)	Efficiency (incl. Drv.) (excl. Ctrl.)
A	V	W	W	W	%	%
0.251	1.64637	0.413824	0.463784	0.022	89.2%	85.2%
0.500	1.49941	0.749418	0.855314	0.0317	87.6%	84.5%
0.749	1.43144	1.0728	1.26742	0.032	84.6%	82.6%

Table 8.4. Simulated MagPwr converter results, f_{sw} = 20 MHz, V_{in} = 3.3 V, V_{Driver} = 5 V.

8.3 Tyndall Thin-Film MS2 *MagPwr* Inductor Converter Results for 25 MHz.

Iout	Vout	Pout	Pin	Pdriver	Efficiency (excl. Drv. & Ctrl)	Efficiency (incl. Dynamic Drv.) (excl. Ctrl.) (excl. Drv. Quiescent)
A	V	W	W	W	%	%
0.25	1.557	0.38925	0.4785	0.292092	81.3%	
0.5	1.4	0.7	0.9009	0.2925465	77.7%	
0.75	1.253	0.93975	1.3299	0.2965865	70.7%	

Table 8.5. Measured MagPwr converter results, f_{sw} = 25 MHz, V_{in} = 3.3 V, V_{Driver} = 5.05 V.

Iout	Vout	Pout	Pin	Pdriver	Efficiency (excl. Drv. & Ctrl)	Efficiency (incl. Drv.) (excl. Ctrl.)
A	V	W	W	W	%	%
0.250	1.5994	0.3997	0.488124	0.0375	81.9%	76.0%
0.500	1.47398	0.736485	0.864507	0.0404	85.2%	81.4%
0.749	1.40852	1.05529	1.27823	0.0405	82.6%	80.0%

Table 8.6. Simulated MagPwr converter results, f_{sw} = 25 MHz, V_{in} = 3.3 V, V_{Driver} = 5 V.

8.4 Tyndall Thin-Film MS2 *MagPwr* Inductor Converter Results for 35 MHz.

Iout	Vout	Pout	Pin	Pdriver	Efficiency (excl. Drv. & Ctrl)	Efficiency (incl. Dynamic Drv.) (excl. Ctrl.) (excl. Drv. Quiescent)
A	V	W	W	W	%	%
0	1.776	0	0.06204	0.3703095	0.0%	0.0%
0.5	1.407	0.7035	0.9339	0.372042	75.3%	75.2%
0.75	1.273	0.95475	1.3893	0.3762	68.7%	68.4%
0.9	1.198	1.0782	1.6632	0.37917	64.8%	64.5%

Table 8.7. Measured MagPwr converter results, f_{sw} = 35 MHz, V_{in} = 3.3 V, V_{Driver} = 4.95 V.

Iout	Vout	Pout	Pin	Pdriver	Efficiency (excl. Drv. & Ctrl)	Efficiency (incl. Drv.) (excl. Ctrl.)
A	V	W	W	W	%	%
0.499	1.43101	0.713525	0.900314	0.0574	79.3%	74.5%
0.749	1.3631	1.0209	1.31045	0.0572	77.9%	74.6%
0.896	1.32577	1.18763	1.55193	0.0568	76.5%	73.8%

Table 8.8. Simulated MagPwr converter results, f_{sw} = 35 MHz, V_{in} = 3.3 V, V_{Driver} = 5 V.

Variable List

For Thesis	LTSpice Label	Description	Unit
HS		High-Side	
LS		Low-Side	
Sw_{HS}	Sw_HS	High-Side Switch	
Sw_{LS}	Sw_LS	Low-Side Switch	
SC		Switched-Capacitor	
PWM		Pulse Width Modulator	
DAC		Digital-to-Analogue Converter	
DC		Direct Current	
DCR		Direct Current Resistance	
AC		Alternating Current	
ACR		Alternating Current Resistance	
ZVS		Zero Voltage Switching	
ZCS		Zero Current Switching	
POL		Point-of-Load	
BCM		Boundary Conduction Mode	
MOSFET		Metal Oxide-Semiconductor Field-Effect Transistor	
NMOS		n-type MOSFET	
PMOS		p-type MOSFET	
CMOS		Complementary Metal-Oxide-Semiconductor	
VDMOS		Vertically Diffused MOSFET	
LDMOS		Laterally Diffused MOSFET	
MFM		Multi-Finger MOSFET	
MF		Multi-Finger	
SF		Single-Finger	
STI		Shallow Trench Isolation	
LDD		Lightly Diffused Drain	
QRR		Diode Reverse Recovery	
2DEG		Two-Dimensional Electron Gas	
HEMT		High-Electron-Mobility Transistor	
ESR		Effective Series Resistance	Ω
ESL		Effective Series Inductance	Ω
VCCS		Voltage Controlled Current Source	
CC		Current Collapse	
V_{in}	ValVin	Input Voltage	V
V_{out}	Vout	Output Voltage	V
V_{sn}	Vsn	Switch-node Voltage	V
V_{Driver}		Driver Input Voltage	V
I_{Driver}		Driver Input Current	A
R_{Driver}		Driver Resistance	Ω
P_{Driver}		Driver Power	W
P_{Driver}			
P_{Driver}			
P_{Driver}			
V_{gate}	Vgate	Gate Voltage	V
R_{DS}		Drain-Source Resistance	Ω

V_{DS}		Drain-Source Voltage	V
V_{GS}		Gate-Source Voltage	V
V_{GD}		Gate-Drain Voltage	V
I_{out}		Output Current	A
I_{DS}		Drain-Source Current	A
I_{GS}		Gate-Source Current	A
I_{GD}		Gate-Drain Current	A
I_{pk}		Peak Current	A
V_S		Source Voltage	V
V_D		Drain Voltage	V
V_G		Gate Voltage	V
$V_{DS(HS)}$		HS Drain-Source Voltage	V
$V_{GS(HS)}$		HS Gate-Source Voltage	V
$V_{GD(HS)}$		HS Gate-Drain Voltage	V
$I_{DS(HS)}$		HS Drain-Source Current	A
$I_{GS(HS)}$		HS Gate-Source Current	A
$I_{GD(HS)}$		HS Gate-Drain Current	A
$V_{DS(LS)}$		LS Drain-Source Voltage	V
$V_{GS(LS)}$		LS Gate-Source Voltage	V
$V_{GD(LS)}$		LS Gate-Drain Voltage	V
$I_{DS(LS)}$		LS Drain-Source Current	A
$I_{GS(LS)}$		LS Gate-Source Current	A
$I_{GD(LS)}$		LS Gate-Drain Current	A
L	ValL	Output Inductance	H
I_L		Inductor Current	A
Δi_L		Inductor Current Ripple	A
V_L		Inductor Voltage	V
N_{turns}		Number of Turns	
A_{cross}		Cross-Sectional Area	mm^2
μ		Magnetic Permeability	H/m
l_{core}		Mean Core Length	mm
$\mu_A(f)$		Frequency Dependent Amplitude Permibility	H/m
R		Resistance	Ω
ρ or g_m		Transconductance	Siemens
l_{path}		Path Length	mm
C_o	ValC	Output Capacitance	F
ESR_C	ValESRC	Capacitor Resistance	Ω
V_{C_o}		Output Capacitor Voltage	V
Δv		Output/Capacitor Voltage Ripple	V
I_{C_o}		Output Capacitor Current	A
C_{fly}	ValCfly	Flying Capacitance	F
$ESR_{C_{fly}}$	ValESRCfly	Flying Capacitor Resistance	Ω
$V_{C_{fly}}$	ValVCfly	Output Capacitor Voltage	V
$I_{C_{fly}}$		Output Capacitor Current	A
$\Delta v_{C_{fly}}$		Flying Capacitor Voltage Ripple	V

R_L	ValRL	Load Resistance	Ω
$R_{PU(HS)}$	ValRPU	High-Side Pull Up Resistance	Ω
$R_{PD(HS)}$	ValRPD	High-Side Pull Down Resistance	Ω
$R_{PU(LS)}$	ValRPU	Low-Side Pull Up Resistance	Ω
$R_{PD(LS)}$	ValRPD	Low-Side Pull Down Resistance	Ω
V_{Driver}	Vdrive_HS(LS)	Driver Rail Voltage Simulated	V
Pulse:	ValGrnd	Pulse Low Value	V
	ValVdd	Pulse High Value	V
	ValDelHS(LS)	Delay Time	s
	ValTrf	Rise/Fall Time	s
t_{on}	ValTonHS(LS)	On-Time	s
T_{sw}	ValP	Switching Period	s
f_{sw}		Switching Frequency	Hz
f_{eff}		Effective Switching Frequency	Hz
D	D	Duty Cycle	
t_d		Dead-time	s
t_f		Fall Dead-time	s
t_r		Rise Dead-time	s
r_{on}		On Resistance	Ω
T_0		Period of Oscillation	s
f_0		Frequency of Oscillation	Hz
w_0		Angular Frequency of Oscillation	Hz
C_{Boot}	BootC	Bootstrap Capacitor	F
V_F	ValVfwd	Shottky Forward Voltage	V
V_R		Reverse Voltage	V
C_{Diode}	ValDCap	Diode Parallel Capacitance	F
R_{Diode}	ValDRes	Diode Resistance	Ω
I_{RM}		Maximum Reverse Current	A
V_{Diode}		Diode Voltage	V
I_{Diode}		Diode Current	A
I_F		Forward Diode Current	A
I_R		Reverse Diode Current	A
I_{max}		Maximum Current	A
I_{min}		Minimum Current	A
S		Softness Factor	
Q_{GS1}		Gate-Source Charge During Rise from 0 to V_{th}	C
Q_{GS2}		Gate-Source Charge During Rise from V_{th} to V_{PL}	C
Q_{GD}		Gate-Drain Charge During Plateau	C
Q_{sw}		Switch Turn-On Charge	C
Q_a		Body Diode Charge During t_a	C
Q_b		Body Diode Charge During t_b	C
Q_{rr}	$Q_a + Q_b$	Body Diode Reverse Recovery Charge	C
E_{QRR}		Reverse Recovery Energy	J
	StopT	End of Simulation Time	s
	StartT	Start of Simulation Time	s
	MaxT	Maximum Timestep	s
	StartMeas	Start of Measure Commands	s

	StopMeas	End of Measure Commands	s
V_{th}		Threshold Voltage	V
V_{PL}		Plateau Voltage	V
L_{CSI}		Common Source Inductance	H
C_{Eq}		Equivalent Energy Capacitance	F
C_{ds}		Drain-Source Capacitance	F
C_{gd}		Gate -Drain Capacitance	F
C_{gs}		Gate-Source Capacitance	F
C_{iss}	$C_{dg} + C_{gs}$	Switch Input Capacitance	F
C_{oss}	$C_{dg} + C_{ds}$	Switch Output Capacitance	F
C_{rss}	C_{gd}	Reverse Transfer Capacitance	F
$C_{ds(Eq)}$		Drain-Source Equivalent Energy Capacitance	F
$C_{dg(Eq)}$		Drain-Gate Equivalent Energy Capacitance	F
$C_{gs(Eq)}$		Gate-Source Equivalent Energy Capacitance	F
$C_{oss(Eq)}$		Switch Output Equivalent Energy Capacitance	F
$C_{oss(ER)}$		Switch Output Effective Energy Capacitance	F
$C_{iss(ER)}$		Switch Input Effective Energy Capacitance	F
$C_{oss(ss)}$		Switch Output Small Signal Energy Capacitance	F
C_{db}		Drain-Body Capacitance	F
C_{sb}		Source-Body Capacitance	F
E		Energy	J
E_{cap}		Capacitor Energy	J
E_{gate}		Gate Energy	J
I_D		Drain Current	A
I_G		Gate Current	A
I_S		Source Current	A
I_d		Small Signal Drain Current	A
I_g		Small Signal Gate Current	A
I_s		Small Signal Source Current	A
R_d		Small Added Drain Resistance	Ω
R_g		Small Added Gate Resistance	Ω
R_s		Small Added Source Resistance	Ω
R_{drain}		Parasitic Drain Resistance	Ω
R_{gate}		Parasitic Gate Resistance	Ω
R_{sch}		Resistance of Poly Layer	Ω
FOM		Figure of Merit	
P_{sw}		Switching Loss	W
$P_{sw(on)}$		Switching Turn-On Loss	W
$P_{sw(off)}$		Switching Turn-Off Loss	W
P_{QRR}		Reverse Recovery Loss	W
$P_{con(HS)}$		HS Conduction Loss	W
$P_{con(LS)}$		LS Conduction Loss	W
$P_{gate(HS)}$		HS Gate Loss	W
$P_{gate(LS)}$		LS Gate Loss	W
$P_{t_{f(LS)}}$		LS Dead-time Loss	W

$P_{t_{r(LS)}}$		HS Dead-time Loss	W
$P_{sw(total)}$		Total Switch Loss	W
P_L		Inductor Loss	W
r_L		Effective Series Resistance	Ω
$i_{L(rms)}$		Inductor Root Mean Square Current	A
P_{QRR}		Diode Reverse Recovery Loss	W
l_{path}		Path Length	mm
W		Gate Width	mm
L		Gate Length	mm
N_f		Number of Fingers	
W_f		Gate Finger Width	mm
W_{total}		Total Gate Width	mm
R_{sch}		Resistance of Poly Layer (Gate Layer)	Ω
A_D		Drain Junction Area	mm^2
A_S		Source Junction Area	mm^2
P_D		Drain Side Wall Perimeter	mm
P_S		Source Side Wall Perimeter	mm

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