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A 4th-Order Continuous-Time ΔΣ Modulator with Improved Clock Jitter Immunity using RTZ FIR DAC

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***Abstract*— This paper highlights the influence of the main feedback DAC non-idealities affecting the performance of Continuous-Time Delta-Sigma Modulators (CTDSMs) in radio receiver Internet-of-Things (IoT) applications. It proposes the combination of the Return-To-Zero (RTZ) DAC pulse and Finite-Impulse-Response (FIR) DAC to have inherent Inter-Symbol-Interference immunity and reduced clock jitter sensitivity, which is crucial to meet the strict linearity and Signal-To-Noise-Distortion-Ratio (SNDR) requirements for integrated IoT radio receivers. The proposed design is validated through MATLAB® Simulink® simulations, showing that a 4th order single-bit CTDSM with RTZ + FIR DAC can achieve an SNDR performance only 3dB below the ideal even in the presence of $4.2\ ps\ rms$ of clock jitter at $24\ MHz$ sampling frequency in a $250\ kHz$ signal bandwidth.**

Keywords*— Analog-to-Digital Conversion (ADC), CTDSM, radio receiver, return-to-zero finite impulse response (RTZ FIR) DAC, clock jitter, Excess Loop Delay (ELD), ISI, compensation

I. INTRODUCTION

Continuous-Time Delta Sigma Modulators (CTDSM) have become the preferred Analog-to-Digital Converter (ADC) solution in many modern integrated radio receivers [1]. The implicit anti-aliasing filtering and oversampled benefits of CTDSMs allow relaxed front-end filtering requirements, making them popular in radio receiver architectures [2]. In addition to that, the lower power consumption and high silicon area efficiency of CTDSMs, compared to other solutions like Discrete-Time SDM, make them a good solution for Internet-of-Things (IoT) radio-based applications, where high performance at low power is a must.

The performance of the main feedback DAC in CTDSMs can be a limiting factor in the overall modulator's accuracy, since any error introduced by this block appears directly at the output [3]. In multi-bit CTDSMs the DAC mismatch greatly limits the linearity of the overall modulator [4]. On the other hand, CTDSMs with single-bit feedback DAC are inherently linear and more area efficient compared to multi-bit solutions, but they require higher order loop-filters and oversampling ratios (OSR) to achieve similar performance [5],[6] .

The non-ideal turn on/off times of DAC pulses in CTDSMs produce the so called Inter-Symbol-Interference (ISI), which affects the DAC linearity even in single-bit modulators [7]. Previous works have shown that employing a Return-To-Zero (RTZ) feedback DAC pulse, the ISI issue can be mitigated at the expense of increased clock jitter sensitivity [8]. On the other hand, the Finite-Impulse-Response (FIR) DAC technique has been introduced to reduce the clock jitter sensitivity in CTDSMs with a Non-Return-To-Zero DAC [9].

This work combines the lower ISI sensitivity of the RTZ DAC with the lower jitter sensitivity of the FIR DAC to produce a CTDSM suitable for radio receiver IoT applications, where a low jitter source is normally not available due to power consumption constraints [10]. The presented approach uses a similar design methodology to that shown for CTDSMs with NRZ DAC in [9], but applied to a RTZ DAC pulse.

The paper is structured as follows: Section II discusses the issue of ISI and clock jitter and theirs effect on single-bit CTDSM with RTZ feedback DAC. Section III presents a solution to mitigate the impact of jitter in a RTZ DAC using FIR filtering. Section IV presents MATLAB simulation results, and Section VI gives the conclusions.

II. FEEDBACK DAC NON-IDEALITIES IN CTDSM ADCS

In CTDSMs any deviation from the ideal DAC pulse severely affects the performance of the modulator, since the waveform is continuously integrated at the front end of the modulator. ISI interference and clock jitter are the two main limiting factors in the adequate representation of square-shaped DAC waveforms, and the fundamental causes of performance degradation in single bit CTDSM architectures [11].

A. Inter-symbol Interference

ISI can be thought of as a dependence of the modulator feedback energy content on an output bit stream pattern [8]. Fig. 1 shows two output data patterns for NRZ and RTZ DAC pulses. Due to the non-zero rising and falling times, it can be seen that the amount of feedback quantity (assumed to be charge) being integrated in a CTDSM depends on the output data sequence when using a NRZ DAC, this leads to harmonic distortion [7] and performance degradation of the ADC. The effect of DAC waveform imbalances can be removed by using a RTZ DAC pulse, since both rising and falling edges occur within one clock cycle. Fig. 2, illustrates the output spectrum of a 4th order single-bit CTDSM under the presence of ISI, for a NRZ and a RTZ DAC pulses, where it is clear the superior performance of the RTZ DAC

B. Clock Jitter

Clock jitter is a random timing deviation of a clock signal edge from the ideal clock edge. In CTDSMs clock jitter

introduces random variations in the amount of feedback charge per clock period [12]. Thus, the ability of the CTDSM to tolerate timing jitter depends on the type of DAC pulse used in the feedback path. To ease the analysis, the clock jitter is assumed to follow a Gaussian distribution, thus allowing us to model the jitter as an uncorrelated additive white noise on the DAC pulse edges as described in [11] and illustrated in Fig. 3. The clock jitter effect over a 4th order single-bit CTDSM with a RTZ DAC pulse is also depicted in Fig. 4, where it can be seen that even a small σ_{jitter} of 0.01% T_s can lower the SNDR by about 11dB.

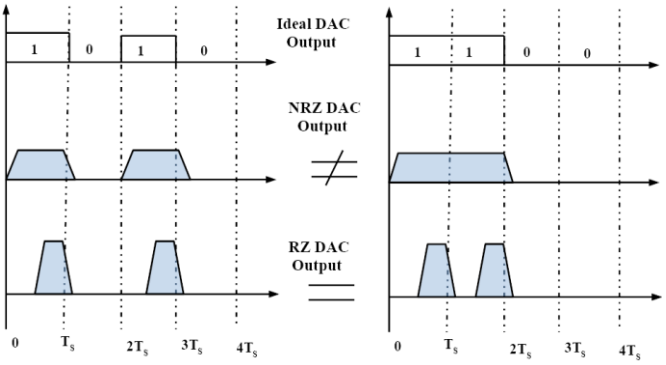


Fig.1: Inter-symbol interference on the feedback DAC waveform

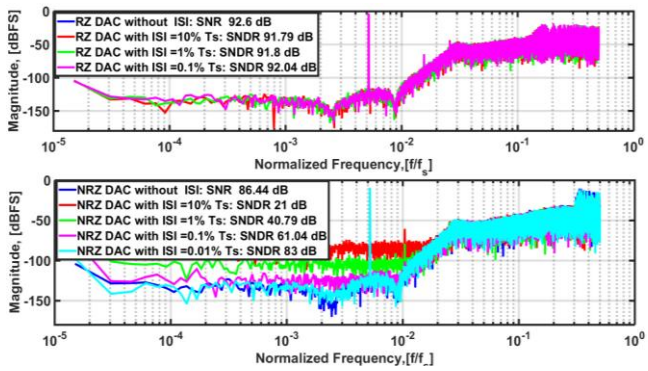


Fig.2: PSD of the 4th order single-bit CTDSM modulators with NRZ and RTZ feedback DACs under the influence of ISI—the same architecture is used in both cases

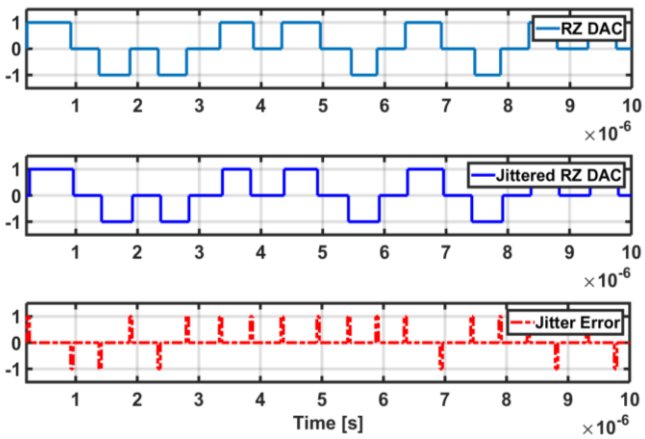


Fig.3: Clock jitter error on the RTZ feedback DAC.

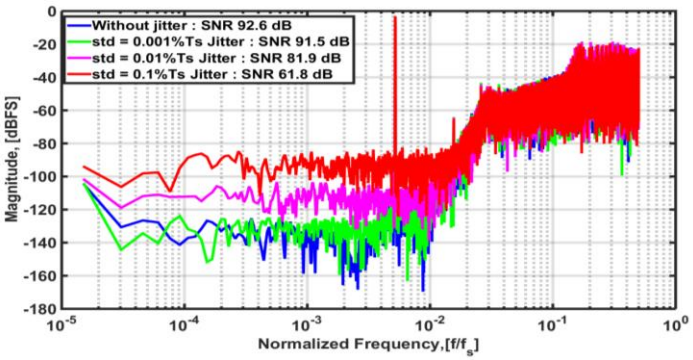


Fig. 4: Simulated PSD for the 4th order CTDSM under clock jitter influence (f_s =24 MHz & input amplitude= 0.35 V)

III. Clock Jitter Alleviation through RTZ FIR DAC

The targeted application of this work is for IoT radio receivers, where both high DR and excellent linearity are required to allow the detection of small desired signals in presence of large blockers [13]. For this reason a single-bit CTDSM with RTZ feedback DAC architecture has been adopted, in order to mitigate ISI. The targeted radio receiver uses a 24 MHz clock as low cost crystal oscillators are available at 24MHz. This means that for a signal bandwidth of 250 kHz, the OSR is restricted to a value of 48. Thus, in order to achieve an 86 dB SNR the loop-filter is chosen to be of the 4th order in the feed forward configuration, as it is illustrated in the proposed architecture of Fig. 5. The ideal modulator produces a SNR of 92.6dB which drops by about 11 dB in the presence of clock jitter with σ_{jitter} = 4.2 ps. (0.01% T_s)

In order to reduce RTZ DAC clock jitter sensitivity, we have incorporated an FIR filter in the feedback path, which is also illustrated in the proposed topology of Fig.5. Adding this FIR filter to the feedback DAC attenuates the high-frequency content of the clock jitter before it is feedback to the input of the modulator, reducing its negative impact in the modulator's accuracy. On the other hand, the FIR filter introduces an additional delay in the feedback path, which compromises the stability of the overall modulator. This additional delay is compensated via a compensation filter F_c around the quantizer as depicted on the right side of Fig.5. This allows the modified loop filter with FIR RTZ DAC impulse response to match the original loop filter impulse response.

The synthesis of the modified CTDSM feedforward coefficients denoted by $c_{m1} \dots c_{m4}$ that will restore the original CTDSM loop filter impulse response is achieved using the method of moments described in [14]. Considering again Fig. 5, the loop filter pulse output can be expressed as:

$$Y(t) = c_4x_4 + c_3x_3 + c_2x_2 + c_1x_1 \,. \qquad (1)$$

By incorporating the FIR DAC into the loop the individual modulator loop paths $x_1 \dots x_4$ will be modified and the resulting loop filter pulse output is modified to:

$$Y_m(t) = c_{m4}x_{m4} + cx_{m3} + c_{m2}x_{m2} + c_{m1}x_{m1} \,. \qquad (2)$$

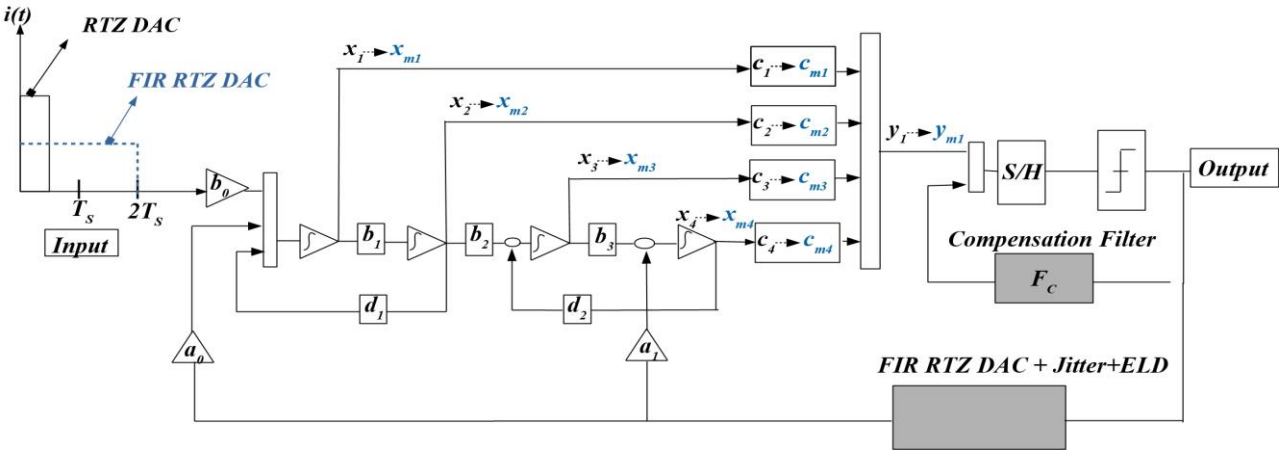


Fig. 5: 4th Order CTDSM Architecture Overview. The original modulator with an RTZ DAC loop filter pulse response is referred to as $y(t)$ and the proposed CTDSM i.e. with the FIR RTZ DAC loop response is denoted by $y_m(t)$

By using the method of moments of [14] and [5], the pulse response of the $\frac{1}{S^N}$ integrating path denoted by $x_N(t)$ is given by:

$$x_N(t) = \frac{t^{N-1}}{(N-1)!}\,\mu_l(t) * p(t) = \frac{1}{(N-1)!}\int_0^t p(\tau)(t-\tau)d\tau \quad (3)$$

where *p(t)* is the total area of the DAC pulse response (ideally equal to 1 after one sample period) and $u_l(t)$ is l^{th} moment of the DAC pulse $\mu_l = \int_0^t \tau^l p(\tau)d\tau$ with *p(t)=1* and $0 \le t \le T_s$.

Substituting the moments of the RTZ DAC pulse into equation (3) and after simplification the original 4th order CTDSM loop filter's individual path pulse responses are:

$$\begin{aligned} x_4(t) &= \frac{1}{6}\mu_0 t^3 - \frac{1}{2}\mu_1 t^2 + \frac{1}{2}\mu_2 t^1 - \frac{1}{6}\mu_3 \\ x_3(t) &= \frac{1}{2}\mu_0 t^2 - \mu_1 t + \frac{1}{2}\mu_2 \\ x_2(t) &= \mu_0 t - \mu_1 \\ x_1(t) &= \mu_0 \end{aligned} \quad (4)$$

A similar method is used to derive the individual path response $(x_{m1} \ldots x_{m4})$ of the modified CTDSM with a 4-tap FIR filter. The amplitude of $y_1(t)$ with RTZ DAC will be reduced from 2 to $2/(Number\ of\ FIR\ taps)$. Thus, the FIR RTZ DAC can now be interpreted as a pulse amplitude $p(t)$ = 0.5 from $0 \le t \le 2T_s$ as illustrated in Fig.5 (blue). The l^{th} moment of this DAC pulse is given by $\mu_{ml} = \int_0^t \tau^l(0.5)d\tau$ and, after substitution into (3), it can be shown that the modified CTDSM pulse responses of the loop filter paths are given by:

$$\begin{aligned} x_{m4}(t) &= \frac{1}{6}\mu_{m0} t^3 - \frac{1}{2}\mu_{m1} t^2 + \frac{1}{2}\mu_{m2} t^1 - \frac{1}{6}\mu_{m3} \\ x_{m3}(t) &= \frac{1}{2}\mu_{m0} t^2 - \mu_{m1} t + \frac{1}{2}\mu_{m2} \\ x_{m2}(t) &= \mu_{m0} t - \mu_{m1} \\ x_{m1}(t) &= \mu_{m0} \end{aligned} \quad (5)$$

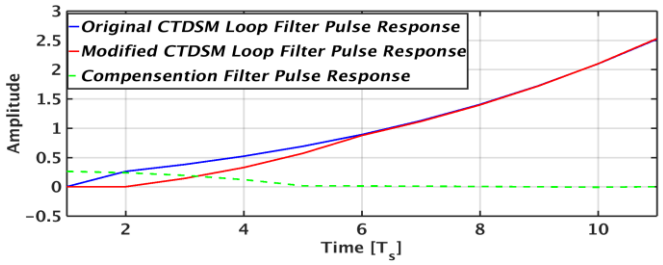


Fig. 6: Illustration of the 4th order CTDSM loop filter response with RTZ DAC (red), the modified CTDSM with a 4 taps FIR RTZ DAC and the responses of the F_c compensation filter.

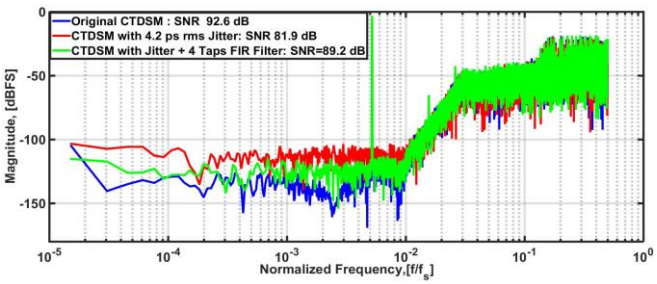


Fig. 7: Simulated PSD with clock jitter, assumed white (σ_{jitter} = 0.01% T_s and fs= 24MHz). The jitter free spectrum is shown in blue. The CTDSM power spectral densities with 4 taps FIR filter in feedback paths is illustrate in green.

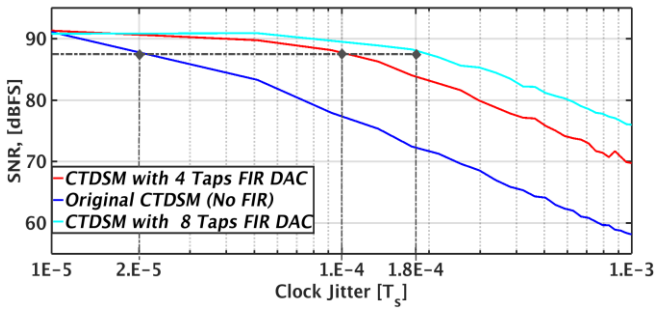


Fig. 8: Comparison of the modulator SNR under clock jitter influence with a 4-tap and 8-tap FIR RTZ DAC.

As shown in Fig.6 the loop filter pulse response of the original CTDSM (blue curve) will be identical to that of the proposed loop filter pulse response with a 4-tap FIR

The new re-scaled loop filter feed-forward coefficients that will enable the loop filters described by equations (1) and (2) to align after t_{delay} = number-of-filter-taps, are as follows:

For $y(t) = y_m(t)$ and $\mu_{m0} = \mu_0 = 1$:

$$c_{m4} = c_4, \; c_{m3} = c_3 + (\mu_{m1} - \mu_1)c_4$$

$$c_{m2} = c_2 + (\mu_{m1} - \mu_1)(c_3 + c_4\mu_{m1}) - \frac{c_4}{2}(\mu_{m2} - \mu_2)$$

$$c_{m1} = c_1 - c_2\mu_1 + \frac{c_3\mu_2}{2} - \frac{c_4\mu_3}{6} + c_{m2}\mu_{m1} + \frac{c_{m4}\mu_{m3}}{6} - \frac{c_{m3}\mu_{m2}}{2}$$

Thus, the F_c compensation filter coefficients can be found as the difference between the original loop filter response (blue) and the modified CTDSM pulse response (red) shown in Fig. 6. Although not included in the previous coefficient derivations, the NRZ DAC can tolerate Excess-Loop-Delay (ELD) up-to 0.5Ts without any extra step in the coefficient derivation [4].

IV. Simulation Results

The proposed 4th order single-bit CTDSM with a 4-tap FIR RTZ DAC was simulated in the MATLAB® Simulink® environment. With a sampling frequency of *24 MHz* over a signal bandwidth of *250 kHz*, and including a clock jitter error sequence of *4.2 ps rms* the designed CTDSM achieves a maximum SNDR of *89.2 dB*, which is illustrated in Fig. 7. This plot validates the reduced jitter sensitivity of the proposed 4th order CTDSM with RTZ + FIR DAC, and shows its improved robustness in presence of clock jitter. Moreover, it is apparent that increasing the number of filter taps results in improved immunity to clock jitter effects. This is illustrated in Fig. 8, where a clock jitter parametric analysis for 4-tap and 8-tap FIR DAC filtering was carried out. It is clear that an 8-tap filtering outperforms the 4-tap one by about 3 dB at σ_{jitter} = 4.2 ps, but it comes at the expense of an increased hardware complexity in both the FIR filter and the F_c filter, leading to increased power consumption, silicon area and loop-filter stability concerns. Therefore, a 4-tap FIR RTZ DAC represents a better trade-off to achieve a low area and cost-efficient design. Finally, it is worth mentioning that to achieve similar SNDR performance without the proposed FIR RTZ DAC method, a clock source of $0.5ps, rms$ clock jitter would have been required, which is not a cost efficient design approach.

V. Conclusions

This paper has highlighted the influence ISI and clock jitter in CTDSMs. Based on this, it was proposed to combine the use of an RTZ and FIR DAC to have inherent ISI immunity and reduced cock jitter sensitivity. The derived loop filter coefficients and mathematical assumptions where validated though MATLAB® simulations, showing that the proposed approach and architecture can simultaneously meet linearity and clock jitter specifications for IoT radio receiver applications

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