A Bias and Control Circuit for Gain Stabilization in Avalanche Photodiodes

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***Abstract*—This paper describes a novel bias and gain control circuit for avalanche photodiodes (APDs) biased in linear mode. The circuit was implemented using a printed circuit board (PCB) and packaged APDs. Experimental results show that the circuit is capable of providing bias voltages up to 40 V for the APDs, precisely setting its gain (error < 2.5 %) and compensating for the changes in the temperature to maintain a stable gain. A 5 V power supply is sufficient for the circuit and it operates without the need for external temperature sensing and control electronics thereby lowering the system cost and complexity. Moreover if the circuit is fabricated on-chip, then only one external component is required making it compact and attractive for integrated APD applications.**

***Keywords* – Avalanche photodiode, multiplication gain, bias circuit, gain stabilization**

I INTRODUCTION

Advances in avalanche photodiode (APD) technology has enabled higher sensitivity and lower operating voltages. These advances as well as lower costs have allowed APDs to replace photomultiplier tubes (PMTs) in many low-light sensing applications. Such applications include astronomy, DNA sequencing, quantum key distribution, LIDAR and medical imaging. The gain of an avalanche photodiode is very sensitive to changes in bias voltage and temperature. To stabilise the device gain the bias voltage must be stabilised. This paper presents a circuit that accomplishes this, while additionally compensating for minor temperature fluctuations by altering the bias voltage to maintain the user set gain.

Carriers generated in avalanche photodiodes are multiplied by a current gain mechanism, through a process known as impact ionisation. The APD gain $M_{Ph}(V)$ at a particular voltage V is defined as the multiplied photocurrent I_{MPh} divided by the Photo-current I_{Ph} at low voltages where no carrier multiplication takes place[1].

$$M_{MPh}(V) = \frac{I_{MPh}(V)}{I_{Ph}} \qquad (1)$$

The multiplication gain is affected by many factors including reverse bias voltage and temperature. Therefore it is necessary to accurately set the required bias voltage for the intended APD gain and maintain that gain for long periods of time under varying environmental conditions [2], [3]. Typically, temperature stable systems or temperature compensation circuits are used to stabilize the APD performance [4], [5]. However, those systems or circuits are bulky, expensive, power intensive and do not compensate for changes in the supply voltage.

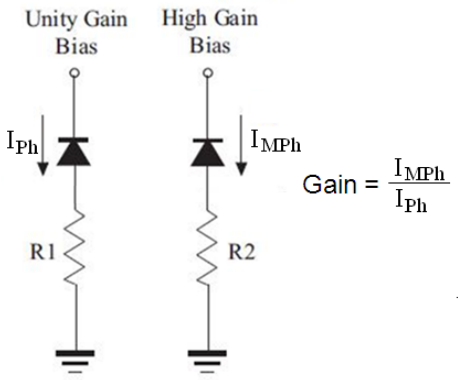

Figure 1: APD bias arrangement using two matched devices.

An alternative gain control technique uses two matched APDs where one is biased at unitary gain (unmultiplied) and the other one is biased at a high gain (multiplied) [6], see Fig. 1. Since the two matched APDs have near identical performance, the gain is simply the ratio of the currents flowing in the two APDs. In principle this technique can be used to set the gain and modify the bias voltage to compensate for the changes in the environment without the need for external temperature sensing and control electronics. Several circuits have been designed using this idea and are described in detail in refs. [6], [7]. Those circuits set the APD gain according to the feedback from the two matched APDs that provide a lower cost and simpler solution for the control of APD gain. However they still have drawbacks. There is no detailed description of how the DC-DC converter operates in [6] and the control logic in [7] is complicated and its bias solution is not compact.

In this paper, a bias control and gain stabilization circuit for planar APDs [8] that are typically designed with a breakdown voltage less than 30 V is described. This circuit uses two matched APDs where one is biased at unitary gain and the other is biased at a high gain mode. A charge pump is used to bias the APD and a gain control circuit is used to set and stabilize the gain. Experimental results for a printed circuit board (PCB) and packaged APDs show that the circuit can precisely set the gain (error < 2.5 %) and compensate for the changes in the temperature to maintain a stable gain. This approach has the advantages of using the matched APDs while providing a simpler and more detailed solution. Moreover, the circuit operates with a 5 V power supply and if fabricated on chip, only one external component is required making it compact and attractive for integrated APD applications.

II CIRCUIT DESCRIPTION

Fig. 2 shows the block diagram of the proposed circuit. A 5 V charge pump DC-DC converter is used to provide the high bias voltage up to 40 V. A gain control circuit is used with the bias circuit and the two matched APDs to set and stabilize the gain in the high gain APD.

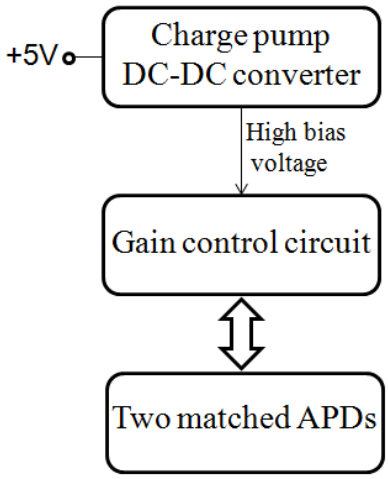

Figure 2: Block diagram of proposed circuit.

a) Charge pump DC-DC converter

The DC-DC converter used is Dickson charge pump circuit [9], see Fig. 3. In the circuit, an inverter is used to invert the phase of the input clocks. The neighbouring pumping capacitors are connected to these two inverse clocks. A load capacitor is used to smooth the output voltage which will be the only external component needed if the circuit is integrated on a chip. Through every stage, the positive charge is transferred by the diodes and pumping clocks to the output. At the output, a high voltage is obtained to bias the APD.

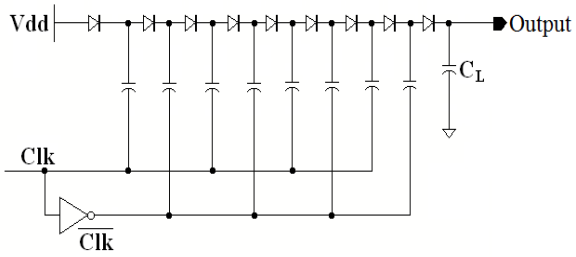

Figure 3: Charge pump DC-DC converter.

b) Gain control and stabilize

A schematic of the gain control circuit with two matched APDs is shown in Fig. 4. APD2 is biased by the charge pump to generate a multiplied current, I_{MPh}. The other photodiode APD1 is biased to give an unmultiplied current, I_{Ph}. In the gain control circuit, an op-amp and an NMOS-transistor are used to sense the voltage feedback from both photodiodes and control the bias voltage from the charge pump to adjust the gain of APD2.

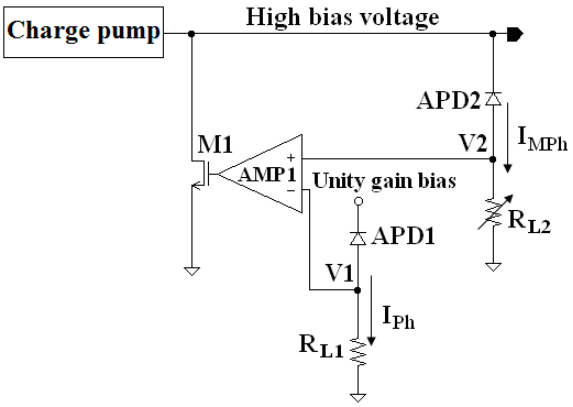

Figure 4: Schematic of gain control circuit with two matched APDs.

The bias voltages generate the unmultiplied and multiplied currents in APD1 and APD2 which flow through the load resistors R_{L1} and R_{L2}. Voltages *V1* and *V2* can be seen at the anode of both photodiodes. *V1* is connected to the inverting input of an op-amp, *Amp1* and *V2* is connected to the non-inverting input of *Amp1*. If *V2* exceeds *V1*, the op-amp generates an output voltage proportional to the difference between *V2* and *V1* and the NMOS-transistor *M1* will be biased to divide the output current. The bias voltage of APD2 will be decreased and *V2* will decrease. If *V2* falls below *V1*, M1 will be turned off, the bias voltage of APD2 can be continuously charged up and *V2* will increase. In this way, *V2* can be set equal to *V1* which makes the multiplication gain in APD2 equal to the ratio of R_{L1} and R_{L2}. When R_{L1} is fixed, by setting the value of the load resistor R_{L2}, the gain of APD2 can be altered.

III SIMULATIONS

In [10], the simulation results were presented. For the simulations, an avalanche photodiode model shown in Fig. 5(a) is used. *R1* and *R2* represent the internal resistance when the APD is reversed biased far from and near the breakdown voltage which are set to 3 MΩ and 25 kΩ respectively. The voltage source *V1* (set to 23 V) is used to model the large increase in gain when the APD is biased close to breakdown voltage. Fig. 5(b) shows the simulation result of this model when the reverse bias is varied from 0 to 30V, demonstrating an approximate I-V characteristic for a planar APD with increasing gain approaching breakdown.

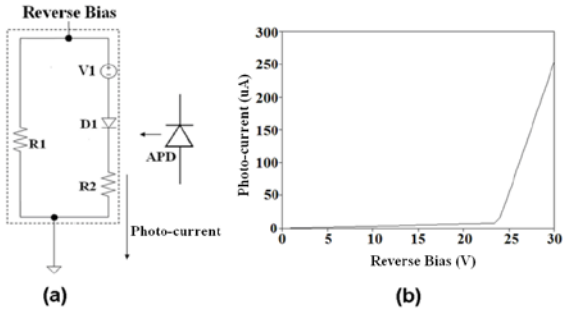

Figure 5: APD model and its simulation result.

The simulations of the proposed circuit were completed using the L-foundry 0.15 µm CMOS process in the Cadence design environment. An 8-stage charge pump is used with the pumping capacitors and load capacitor set to 20 pF and 1 nF, respectively. The clock frequency is 50 MHz with $V_{dd} = V_{clk} = 5$ V. APD1 is biased at V_{dd} to give a unit gain and R_{L1} is set to 500 kΩ. Fig. 6 shows the gain and the bias voltage of APD2 when its gain is set to 100 ($R_{L2} = 5$ kΩ). As can be seen from Fig. 6, the op-amp adjusts the bias voltage according to the feedback from the two photodiodes and control the gain precisely.

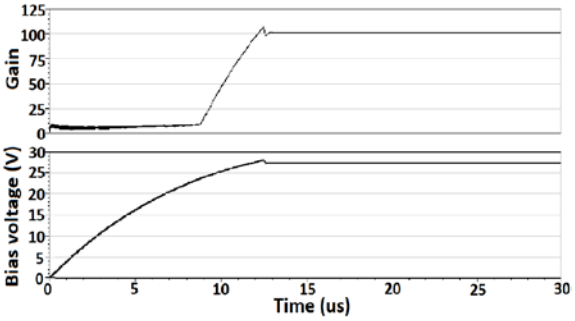

Figure 6: Gain and the bias voltage of APD2 when its gain is set to 100.

IV EXPERIMENTAL RESULTS

With discrete components, a printed circuit board (PCB) was fabricated. Due to large parasitics and speed limitations of a discrete implementation, larger load capacitor is used which is set to 47 nF to smooth the output voltage of the charge pump. The pumping capacitors are 22 pF and the diodes are Schottky diodes BAS40. The NMOS-transistor used is ZVN3306F and the op-amp is MCP6041. The clock frequency is 50 MHz with $V_{dd} = V_{clk} = 5$ V. Fig. 7 illustrates the measured output voltages of the charge pump for different load current. It shows the circuit is capable of providing up to 40 V bias voltage and delivering more than 1mA load current at a bias of 27 V.

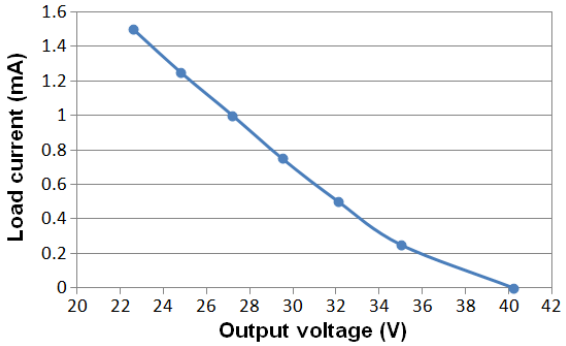

Figure 7: Output voltages of charge pump DC-DC converter for different load current.

For the measurement, two 400 um diameter circular planar shallow junction APDs developed by the Photodetection and Imaging Group from University College Cork [11] were wire bonded in a dual in line (DIP) package, see Fig. 8.

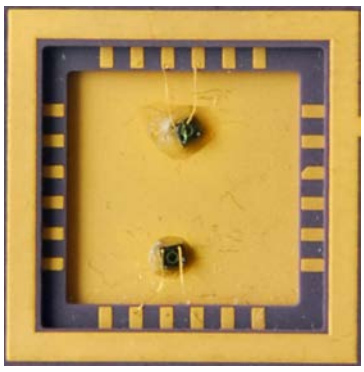

Figure 8: Packaged two matched avalanche photodiodes.

A He-Ne laser source operating at 623 nm with the optical power of 330 nW was used as the incident light that was directed to the packaged diodes through an integrating sphere. A value of 56 was arbitrarily chosen to be the required gain value. Fig. 9 shows an oscilloscope trace of the bias voltage waveform for the high gain APD to achieve the user-set gain.

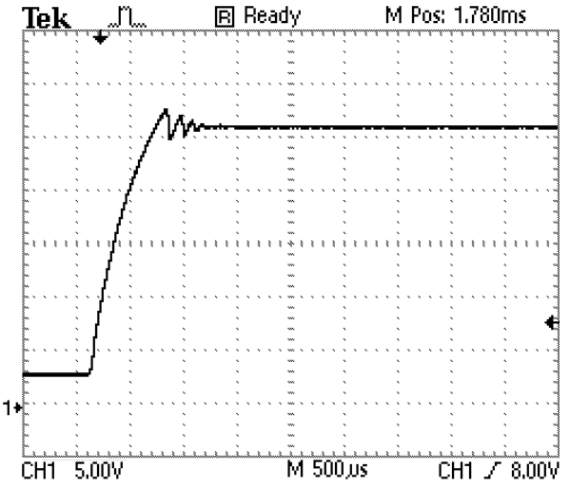

Figure 9: Oscilloscope trace of the bias voltage waveform for the high gain APD.

Fig. 10 describes the gain's variation over a period of time. As can be seen from the figure, the gain was set close to the required gain with an error of less than 2.5%. Results also show that the circuit can compensate for the changes in the temperature and maintain a stable gain for the duration of time.

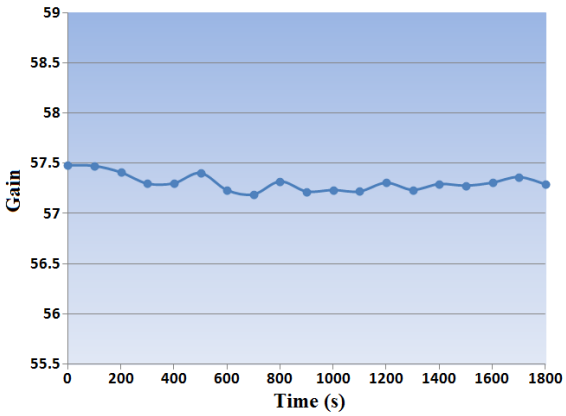

Figure 10: Gain's variation over a period of time with the control of proposed circuit.

V CONCLUSIONS

This paper describes a bias control and gain stabilization circuit for planar APDs. The experimental measurements of the fabricated PCB module and packaged APDs show that the circuit can provide in excess of 40 V bias voltage for the APDs, and set and stabilize its gain with an error of less than 2.5%. This circuit operates without the need for external temperature sensing and control electronics that lower the system cost and complexity. Moreover, the circuit runs off a 5 V power supply and is highly compact (only 1 external component needed if fabricated on chip) making it attractive for low voltage integrated APD applications.

VI ACKNOWLEDGMENTS

This work was funded by Science Foundation Ireland under grant SRC/07/321.

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