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Ultrasonically Powered Compact Implantable Dust for Optogenetics

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***Abstract*—This paper presents an ultrasonically powered microsystem for deep tissue optogenetic stimulation. All the phases in developing the prototype starting from modelling the piezoelectric crystal used for energy harvesting, design, simulation and measurement of the chip, and finally testing the whole system in a mimicking setup are explained. The developed system is composed of a piezoelectric harvesting cube, a rectifier chip, and a micro-scale custom-designed light-emitting-diode (LED), and envisioned to be used for freely moving animal studies. The proposed rectifier chip with a silicon area of $300\mu m \times 300\mu m$ is implemented in standard TSMC $0.18\mu m$ CMOS technology, for interfacing the piezoelectric cube and the microLED. Experimental results show that the proposed microsystem produces an available electrical power of $2.2mW$ while loaded by a microLED, out of an acoustic intensity of $7.2mW/mm^2$ using a $(1mm)^3$ crystal as the receiver. The whole system including the tested rectifier chip, a piezoelectric cube with the dimensions of $(500\mu m)^3$, and a μLED of $300\mu m \times 130\mu m$ have been integrated on a $3mm \times 1.5mm$ glass substrate, encapsulated inside a bio-compatible PDMS layer and tested successfully for final prototyping. The total volume of the fully-packaged device is estimated around $2.85mm^3$.**

***Index Terms*—Energy Harvesting, Implantable Devices, CMOS, Rectifier, Ultrasonic Powering, Piezoelectric.**

I. Introduction

IN the ever evolving and advancing field of combining electronics within the field of medicine, novel treatment methods open up as it becomes possible to make the envisioned devices significantly smaller. One particular concept of micro-sized electronic devices, known as neural dust [1], has shown potentials to be used for brain signal recording. A similar approach can be used for *in vivo* deep brain electrical stimulation (DBS) [2], optical neuromodulation, i.e., optogenetics [3], and even triggered localized drug delivery [4]. Optogenetics, which is the main intended application of this work, can outperform DBS because of its capability of local stimulation of specific populations of neurons using millimeter or sub-millimeter brain implants. This technique is envisioned to be a possible future treatment modality of neurological disorders such as Parkinson's Disease (PD) and Alzheimer's Disease, among others. The work done and described in this paper is part of an EU-funded project, called STARDUST,

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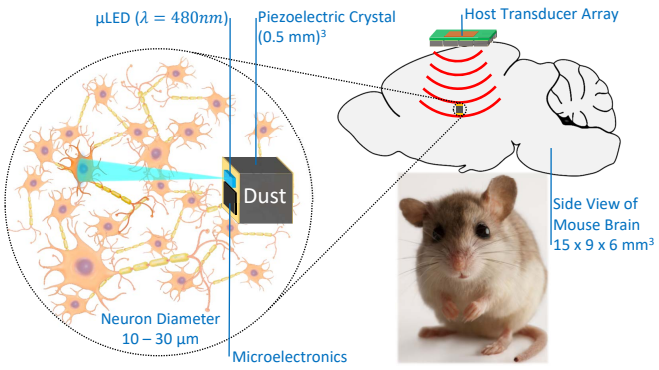


Fig. 1. Conceptual sketch of a neuron illuminated by an implanted Dust, consisting of a piezoelectric crystal with the chip and μLED mounted on top, which in turn is powered by the ultrasonic waves coming from the external host transducer array placed on the surface of the skin.

that aims to deliver a conceptually new device capable of optogenetics, electrophysiology, and triggered localized drug delivery, with the aim of enabling new therapeutic approaches for PD [5], starting here with designing a prototype dust for the purpose of driving a microLED (μLED) for optogenetics in deep regions of the brain, as illustrated in Fig. 1.

As the envisioned device is initially going to be tested on mice, the dust needs to be millimeter sized, preferably sub-millimeter sized, with the possibility of being powered at depths of several centimeters below the skin in anticipation of future human trials. Examples of this can be seen in [6]–[8], where the method of powering is focused on micro-electromechanical systems (MEMS) based on piezoelectric crystals, where ultrasound is used to drive the piezoelectric element, and from that harvest the energy required to drive the integrated microelectronics. Some recent works [9] [10] has shown feasibility studies with promising results regarding miniaturization of the dust into sub-millimeter range, and proposing some techniques for optimizing the power transfer from the crystal to the load. On the basis of these proven concepts, an integrated deep brain implantable dust is envisioned, which itself imposes certain requirements for any design conceived, most notably the size that should be within sub-millimeter range. For practical reasons, the crystal used during characterization tests of the integrated chip is chosen as $(1mm)^3$ cube, but for the final integration, we use a crystal with a size of $(500\mu m)^3$. This was made possible by limiting the maximum area of the Complementary Metal-

Oxide-Semiconductor (CMOS) chip to $300\mu m \times 300\mu m$. The CMOS chip contains an active bridge rectifier to harvest and convert the incoming AC power from the crystal into DC power available for the μLED load at the output of the bridge.

Although the load for this first version of the envisioned device is to power only a μLED for optogenetics purpose, the future prospects of integrating more analog and digital circuitries into the system for other purposes will require a DC supply, and thus a rectifier will be needed. The simplest form of a bridge-rectifier is the commonly known passive diode-based. However, the passive rectifiers suffer form rather high voltage drop over the passive components, which results in low voltage conversion ratio and low power conversion efficiency. Therefore, active rectifiers have been proposed in the literature for overcoming the aforementioned drawbacks [7], [11]–[14]. One of the challenges of these circuits, addressed frequently in the literature [15]–[20], is safe and fast start-up of the system when the DC supply rails are not charged to a minimum level that can be used by active circuitry of the active rectifier. In some works, it has been proposed to configure the active diodes in a passive mode before a power-on-reset circuit detects an adequate level of DC voltage on the rectified output voltage [16], [17]. However, the power-on-reset circuits usually include $M\Omega$-range resistors that demand rather large silicon area. In [15], it is proposed to use an auxiliary power path using passive components for powering some of the active circuitry in the active rectifier. Even though this approach guarantees the safe start-up of the active rectifier, it does not match with the area constraints of this work. In contrary to the above approaches that ensure proper start-up for the price of silicon area with a small power consumption, there are some approaches that proposes to increase the forward current to the storage capacitor at the output of active rectifier to be higher than the reverse current from the storage capacitor to the input of the active rectifier [18]–[21]. Thereby, the extra current to the output storage capacitor will eventually build up to the minimum voltage required for the active diode to start operating as designed. For this purpose, passive diode-connected transistors are used in parallel to active diodes in [19], [20] and [21], body parasitic diodes are biased in such a way to increase the forward current to the output of the rectifier in start-up mode. In our work, the passive diode-connected transistors in parallel to the active diodes are adopted, and a new circuit is proposed to speed up the start-up process.

Simulations based on proper modeling of ultrasonic link may result in considerable savings in cost and time in comparison with directly testing a new idea through experiments. Today, powerful tools are developed based on finite element methods (FEM) (e.g. COMSOL Multiphysics) that enable researchers to perform realistic simulations [10], [22], [23], such as finding the effect of scaling on the output power and to design a procedure for maximizing the power transmission efficiency. However, these simulations can be very computationally heavy and time-consuming. Even though the Finite Element Methods (FEM) tools have also shown proper functionality for simulations including simple electrical circuits, their interfaces with chip design tools like CADENCE Virtuoso has not been developed, properly. Furthermore, for a preliminary behavioural analysis of ultrasonic links, a more tangible and computationally light model is required. Thus, lumped element models have been widely used for analysis and preliminary simulation of the electro-mechanical behaviour of the ultrasonic links in conjunction with attached electrical circuits [10], [24]–[27].

Among all the lumped element models, KLM model [28] is often used for analysis of ultrasonic links for implantable microsystems. Even though this model is very useful when analyzing the characteristics of a given crystal over a given frequency range [24], [26], it is not directly suitable for transient analysis in chip design tools. Therefore, in some works it is suggested that the KLM model can be significantly simplified to its Thévenin equivalent [24] at a given frequency for impedance matching strategies [9], [10]. However, since the Thévenin model of the piezoelectric crystal is at a given frequency, it cannot reflect the true transient characteristics of the piezoelectric crystals properly when loaded by non-linear loads. The importance of being able to simulate accurately with a model in the time domain cannot be overstated, since the loading circuit connected to the piezoelectric crystal is rarely just a simple linear impedance, but an active circuit where the loading changes dynamically over time, which in turn has an effect back on the crystal itself. W. Marshall Leach, Jr, proposed in [29] a different equivalent circuit for modelling acoustic transducers by using only a single transmission line, controlled sources, and standard passive components. This model benefits from two main advantages: 1) its equivalent circuit is easy to implement in SPICE based simulation tools, 2) it functions in both frequency and time domain, thereby enabling transient simulations. In this paper, this model is used for simulations in conjunction with power management circuitry. Therefore, the capabilities of this model compared with real experiments are studied in terms of reflecting the electromechanical properties of the piezoelectric crystal.

The process of modeling, designing, and testing the developed ultrasonically powered microsystem, will be described in the following sections. Section II describes the approach used to design the active bridge-rectifier. Section III and IV shows the respective simulation and measurement results for the developed microsystem prototype. Section V details the integration and assembly of a compact prototype, and section VI details a practical experiment successfully demonstrating its functionality. Finally, section VII summarizes and concludes on the results.

II. Active Bridge-Rectifier Design Approach

The piezoelectric crystal will be loaded by an active bridge rectifier with storage capacitors. Given the FDA-limit acoustic intensity of $7.2mW/mm^2$, and an expected crystal size in the range from $(500\mu m)^3$ to $(1mm)^3$, the total power available will be in the milliwatt range, maybe lower, leaving even less for self powering. Also, a high operating frequency range of 1 - 5 MHz is expected as a direct result of the physical dimensions and material properties of the crystal itself. Finally, the CMOS layout of the complete design is restricted to an area of $300\mu m$ by $300\mu m$ on the die, in preparation of future

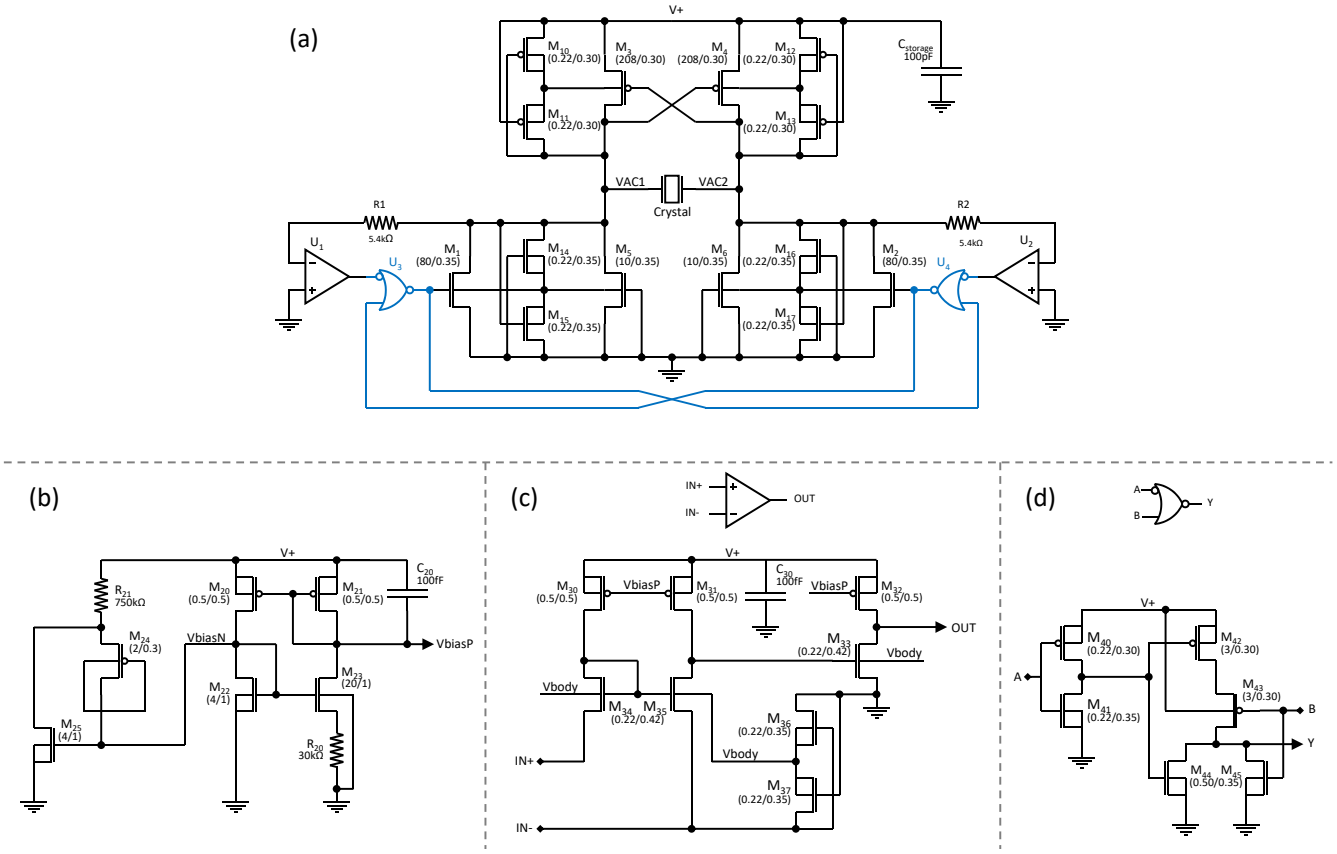


Fig. 2. All transistor dimensions are (width/length) in micrometers. (a) Active bridge-rectifier, including the crystal to illustrate its circuit connections, with the new protection logic to prevent shorting of the crystal shaded in blue. (b) Current-reference, with start-up circuit, common for the OpAmps. (c) Common-Gate 2-stage OpAmp. (d) NOR-gate with the A-input inverted.

integration where it will be placed on top of a crystal with a μLED. This severely limits the amount of room for on-chip capacitance to approximately $100pF$, which is all used as the local storage capacitor $C_{storage}$. A conscious choice is made here not to use any of that area for any capacitor that could otherwise be used for impedance matching between the crystal and the active-bridge.

The designed active bridge-rectifier in this work follows the standard design, with few exceptions described shortly, and the transistor-level schematic of the whole design is illustrated in Fig. 2. The primary philosophy behind this design is its simplicity and robustness over complexity, in order to ensure functionality and operation over as wide a voltage range as possible, within the stated limitations. Therefore, only $3.3V$ nominal NMOS/PMOS transistors from the standard TSMC $0.18\mu m$ CMOS technology are used, in order to extend the chip operating voltage as much as this technology allows.

The OpAmps U_1 and U_2 in Fig. 2 (a) are used as comparators, and as can be seen in details in Fig. 2 (c), has a common-gate configuration as the first stage, with a second stage to boost the gain before driving the following logic gates. The individual OpAmps are biased to use a total of $6\mu A$ at $2.5V$ supply voltage to keep power usage low, at which they have a unity gain bandwidth of $1.93GHz$ and a open loop gain of $74.6dB$. This two-stage OpAmp concept gives a high bandwidth and gain, but at the cost of not being able to make a symmetric layout of the circuit, which leads to uneven parasitic components between the plus and minus input branches which will give a rise to offset errors visible in post-layout simulations. The offset error, however, can be sufficiently cancelled out by adding a resistor in series with the minus inputs, which leads to the addition of the resistors R_1 and R_2. Both OpAmps U_1 and U_2 share a conventional current reference circuit, detailed in Fig. 2 (b), that includes a start-up circuit. The start-up circuit, comprised of M_{24}, M_{25} and R_{21}, is based on the *Accelerated Leakage Component* concept detailed by the work in [30].

One notable difference from the standard design of active bridges is that the bridge shown in Fig. 2 (a) includes two NOR-gates (U_3 and U_4) with one input inverted. They where originally two NOT-gates (inverter) in series to act as drivers of the NMOS switches M_1 and M_2, respectively. It was discovered during simulation of the circuit, using the Leach model as a power source, if the bridge output was relatively heavily loaded compared to the input power, an unfortunate start-up situation could occur where both NMOS switches are driven semi-on. This basically shorts the crystal and thereby risks delaying full start-up of the bridge, significantly, or in the theoretical worst case scenario, prevent start-up from happening at all. The cause behind this lies in the OpAmps U_1 and U_2 being unstable until the internal current reference stabilizes, thereby a risk occurs where they both get ”stuck”

outputting a logic high to the subsequent gates. To solve this issue, we propose a circuit by addition of the two NOR gates that negates the worst of this problem by forming a SR-latch that is disabling a logic high on both outputs at the same time, and instead retains the output state from before the two inputs go high. An analysis with simulations about this issue is done in section III.

Another point to note is that the designed final circuit does not contain any over-voltage protection between the rectified voltage ($V+$) and ground. This is attributed to: 1) The chip is designed using only thick-gate devices in standard TSMC $0.18\mu m$ CMOS technology, which can tolerate an operating voltage up to $3.3V$, unlike standard gate devices that can only tolerate $1.8V$. 2) The load intended for the chip is the μLED shown in Fig. 12 in section V which is used for the integration prototype. Based on the I-V-curve of the μLED it is estimated that it will require more than $20mW$ to force the forward voltage of it above the chip limit of $3.3V$. This amount of power is considered highly unlikely to ever occur and it is far above the amount of harvested power achieved during experiments documented in this paper.

III. Simulation strategy and results

During the design phase of the active-bridge, the Leach model of the crystal is used as the power source of the system during simulations as Fig. 3 depicts. When using the leach model in transient simulations, we should be aware of its relatively slow start-up phase when starting from zero power, which means that any circuit powered by it is forced along this relatively slow start-up phase. This behaviour in transient simulations exposes an inherent flaw in the standard active bridge design, where one or both of the primary NMOS switches (M_1 and M_2 in Fig. 2) are being driven semi-ON during chip start-up, as described in section II. A brief simulation of the start-up of two examples, with and without the NOR-gate logic in the active-bridge, can be seen in Fig. 4 showing the gate voltages of M_1 and M_2 along with the rectified voltage (V_{rect}) that powers the internal transistor circuits, all with respect to the local ground. In this example, the overall circuit is configured as shown in Fig. 3. The Leach model is setup as described in [29] using the parameter values given in Table I, with the frequency set for $1.7MHz$. With this setup, the open circuit voltage and output impedance seen at the electrical port of the Leach model becomes: $V_{oc} = 4.28V$ and $Z_{crystal} = 2.55k\Omega + j4.45k\Omega$, respectively. For the price of only four additional transistors the worst-case scenario of shorting the crystal is removed. However, one of the two switches (M_1, M_2) may still get "stuck" high during start-up, though, this behaviour is always observed to be faster than when the NOR-gate logic is not used.

The final CMOS transistor layout of the active bridge-rectifier can be seen in Fig. 5 (a) and (b), which shows the overall design including the locally placed storage capacitors totalling approximately $100pF$, the four bonding pads, and all of it fitted within the limited area of $300\mu m \times 300\mu m$ as specified earlier. A close-up picture of the design on the silicon die can be seen in Fig. 5 (c).

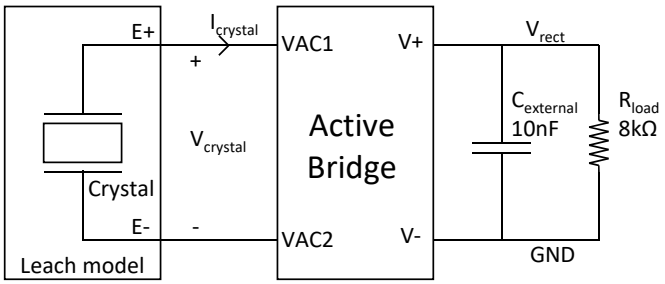


Fig. 3. Principle test setup for simulations using the Leach model as the power source for the active bridge-rectifier.

TABLE I
Parameter values used in the Leach model for simulations. Based directly on values given for lead zirconate titanate (PZT-4) piezoelectric crystal.

Parameter	Value
I_{RMS}	7200 W/m^2
A	1×10^{-6} m^2
d	1×10^{-3} m
ρ_{water}	1000 kg/m^3
$v_{p_{water}}$	1484 m/s
$\rho_{crystal}$	7600 kg/m^3
$v_{p_{crystal}}$	4010 m/s
ϵ_r	1275
ϵ_0	8.854188 pF/m
k_t	0.72

The post-layout model of the active bridge design is setup for simulation as illustrated in Fig. 3, loaded with the resistor R_{load} and external storage capacitors $C_{External}$ set to $8k\Omega$ and $10nF$ respectively, and powered by the Leach model setup as previously described with the parameter values listed in Table I. Fig. 6 (a) shows the simulation results of the voltage and current curves of the Leach model long after start-up, when the system has settled into a normal state of operation. For comparison, a second similar simulation is setup where the Leach model is replaced with the simplified Thévenin model of the KLM model. The Thévenin model has the same open circuit voltage as the Leach model, though the impedance is simplified to contain only the real part, ($Z_{crystal} = 2.55k\Omega$), since this gives the closest behaviour to reality. The result of running the same simulation but with the Thévenin model instead can be seen in Fig. 6 (b). Comparing the simulation results of the two models show clear differences, where the voltage and current curves of the Leach model in Fig. 6 (a) will be shown in the following section to be strikingly similar in shape and behaviour with what has been measured in the experiment. To the best of our knowledge, no one has used the Leach model for behavioural prediction of a piezoelectric crystal connected with electrical/integrated circuits in the context of power harvesting, even though the Leach model was proposed a long time ago.

There are, however, a couple of caveats to be aware of here: 1) The Leach model here assumes water on the backside, where the real test setup has a PCB board which will give

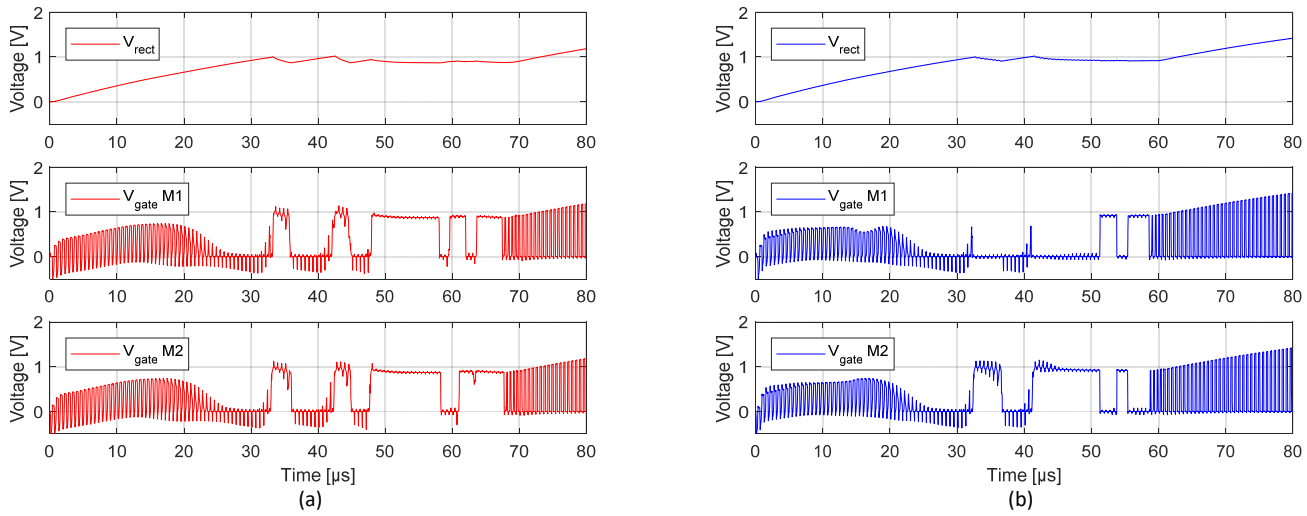


Fig. 4. Shows example simulation results observing the rectified voltage (V_{rect}) and the gate voltage of the two NMOS switches M_1 and M_2 during start-up, with respect to local ground. (a) Without NOR-gate logic, both M_1 and M_2 are observed being driven ON simultaneously, actual start-up happen at approximately $70\mu s$. (b) With NOR-gate logic, only M_1 or M_2 can be driven on at any given time, actual start-up happen at approximately $60\mu s$.

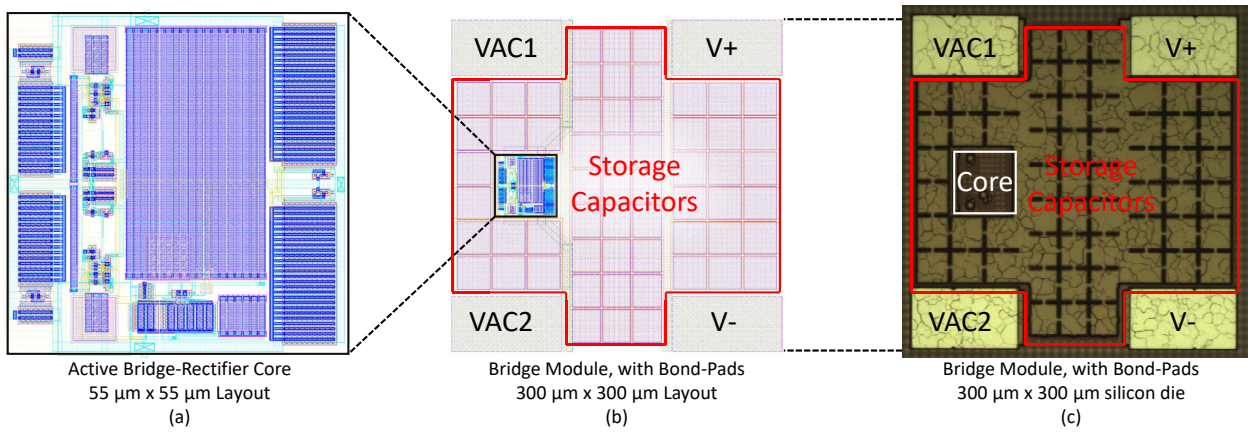


Fig. 5. (a) Zoom in on the core transistor design of the active bridge. (b) Overview of the full active bridge system, including bond pads and locally placed storage capacitors totalling approximately $100pF$. (c) Close-up picture of the CMOS design implemented on a silicon die.

a different value for the acoustic impedance of the back port. 2) The model is a simple 1-dimensional model that in no way can take any side-wall effects into account, since in the real world, the crystal will be surrounded by acoustic waves. For those kinds of details, FEM simulations should be considered, however, the price will be a significant loss of speed and thus flexibility of the simulation, which is the original reason for using the Leach model in the first place. 3) The Leach model also elegantly represents the limited power available from a crystal on its electrical port in transient simulations, in that it cannot supply more power than it first absorbs from its acoustic ports, and vice versa. However, a quick test of the Leach model using the parameter values listed in Table I will, even with perfect impedance matching on the electrical port as a load, never be able to deliver more than $900\mu W$ out of the theoretical $7.2mW$ that hits its acoustic port. This is a major deviation of the results found through measurements described in the following section, where much higher levels of power are harvested, but this comes back to the previous note that the model is 1-dimensional. In fact, the version of the model used here was originally meant for piezoelectric discs or plates, with much higher aspect ratios, and here it is used for a cube. However, that being said, the way it dynamically responds in conjunction with the CMOS circuits connected to its electrical port is what makes it a highly valuable tool for simulations to use during development. In any case, one can choose to boost the simulated incoming acoustic power to compensate for this if deemed necessary. With the $900\mu W$ limited power available in mind, the actual average output power of the crystal in the simulation that Fig. 6 is taken from, is only $788\mu W$. It is believed this reduction mainly comes from the fact that no matching capacitor has been added in series with the crystal, which potentially could increase the electrical power output of the crystal [9]. However, $730\mu W$ of power is delivered to R_{load}, which in turn gives a chip efficiency of approximately 92.6% for the simulation, which later will be shown to be very similar to the results of the experimental results in the next section.

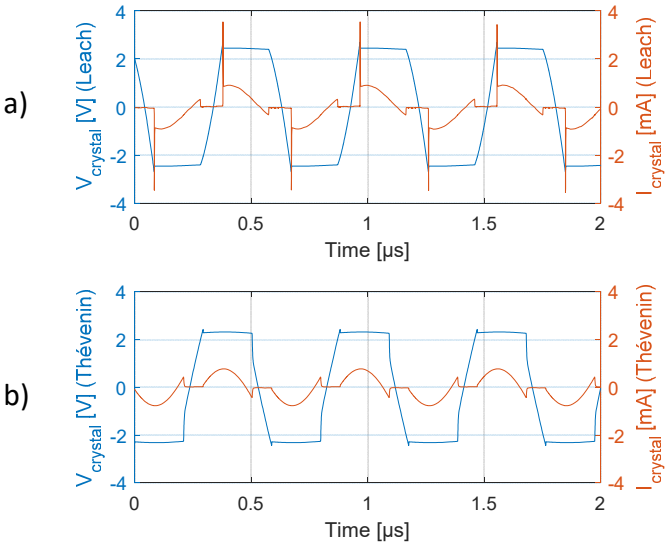


Fig. 6. (a) Leach model, (b) Thévenin model, with simulated voltage (blue) and current (red) curves versus time, of the respective models. Both models are loaded by the active bridge model created from parasitic extraction of the layout, with the resistor R_{load} and external storage capacitors $C_{External}$ on the bridge output, as illustrated in Fig. 3.

IV. Measurement Results

The test setup used for characterizing the chip with the active rectifier includes a $(1mm)^3$ lead zirconate titanate (PZT-4) piezoelectric crystal cube as the chip power source, and a blue μLED as the load, with a $10nF$ capacitor as external storage. The crystal was diced with a Disco DAD-321 dicing saw. A V303-SU transducer from Olympus is driven by an arbitrary signal generator amplified by a 50 dB RF amplifier to deliver the acoustic power to the crystal. A principle schematic of the experimental test setup can be seen in Fig. 7, which includes additional circuits shaded in blue that are needed for measuring voltages and currents passing between the crystal and the chip. The reason for these additional measurement circuits are to "insulate" the crystal and chip circuits from the oscilloscope used, that would otherwise cause adverse effects and disturb the measurements.

Fig. 8 (a) shows the full experimental test setup with the water tank, (b) a close-up of the test board with the chip built for measurements, and the HGL-0400 hydrophone and AH-2010 pre-amplifier from Onda Corporation used for calibrating the acoustic intensity. Before every experiment, the hydrophone is placed in front of the transducer where the acoustic intensity is calibrated to $7.2mW/mm^2$ at that position, after which the test board with the crystal takes its place and testing can commence.

A. Measured input power

Starting on the input side of the chip, the input power to the chip can be determined from the outputs of the amplifier (OpAmps) in Fig. 7 that represents the voltage across the crystal and the current through the chip respectively. Practical tests have shown that the maximum power extraction from the crystal used in the experiment occurs at a frequency of $1.38MHz$. The resulting voltage across the crystal and the current through the chip, with the μLED and $10nF$ storage capacitor as a load, can be seen in Fig. 9. The shape of these curves corresponds well with the simulation results, shown previously in Fig. 6 (a).

TABLE II
Summary of powers in the system during experimental tests.

Ref.	Component	Power	Notes
$P_{crystal}$	Crystal	$2.4975\ mW$	Output
$P_{R_1R_2}$	R_1, R_2	$17.3204\ \mu W$	Loss
P_{R_3}	R_3	$71.3893\ \mu W$	Loss
P_{chip}	Active-bridge	$2.4088\ mW$	Input
$P_{\mu LED}$	μLED	$2.1976\ mW$	Load

One thing to note is the reverse current where power actually runs back to the crystal. Despite being undesirable, it will be shown later that this does not immediately seem to affect the power efficiency, noticeably. Based on the voltage and currents measured in the system, the average power to the chip plus the loss in R_3, as well as the power loss in the voltage divider resistors R_1 and R_2 can be found. From these, the total average power extracted from the crystal and the average power sent to the chip can be derived. All relevant values are summarized in Table II.

B. Measured output power

The average output power of the active-bridge delivered to the μLED is determined by measuring the rectified voltage across the μLED and deriving the resulting current from the I-V-curve of it, and the resulting power can be seen in Table II. The rectified voltage across the μLED can be seen in Fig. 10 that shows a short snippet of raw data measured with an oscilloscope. As can be seen in the graph, the voltage is limited to approximately $2.55V$ caused by the μLED, as expected, which corresponds to an average current at approximately $900\mu A$.

Based on the values collected in Table II, the overall efficiency of the system from incoming acoustic power of $7.2mW$ to the power delivered to the μLED, as well as the individual efficiency of the crystal and the active-bridge itself, can be found as shown in (1), (2) and (3), respectively.

$$\eta_{system} = \frac{P_{\mu LED}}{7.2mW} = 30.5\% \tag{1}$$

$$\eta_{crystal} = \frac{P_{crystal}}{7.2mW} = 34.7\% \tag{2}$$

$$\eta_{chip} = \frac{P_{\mu LED}}{P_{chip}} = 91.2\% \tag{3}$$

The μLED used for integration in the later section V has been determined to have a wall-plug efficiency of 37% before encapsulation, which gives a good estimation of optical output power when applied here in (4). Likewise, the optical power density can be estimated in (5) given the LED mesa size of $100\mu m$ in diameter.

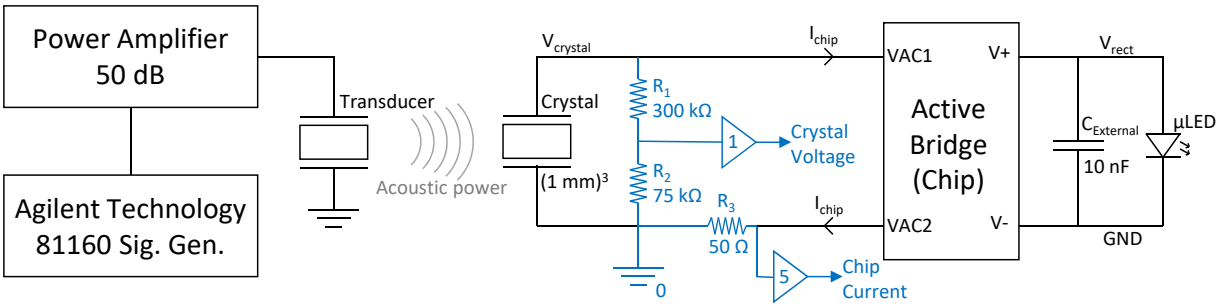


Fig. 7. Schematic of the experimental test setup used for measurements. The components shaded in blue are additional circuitry added for practical measurement purposes.

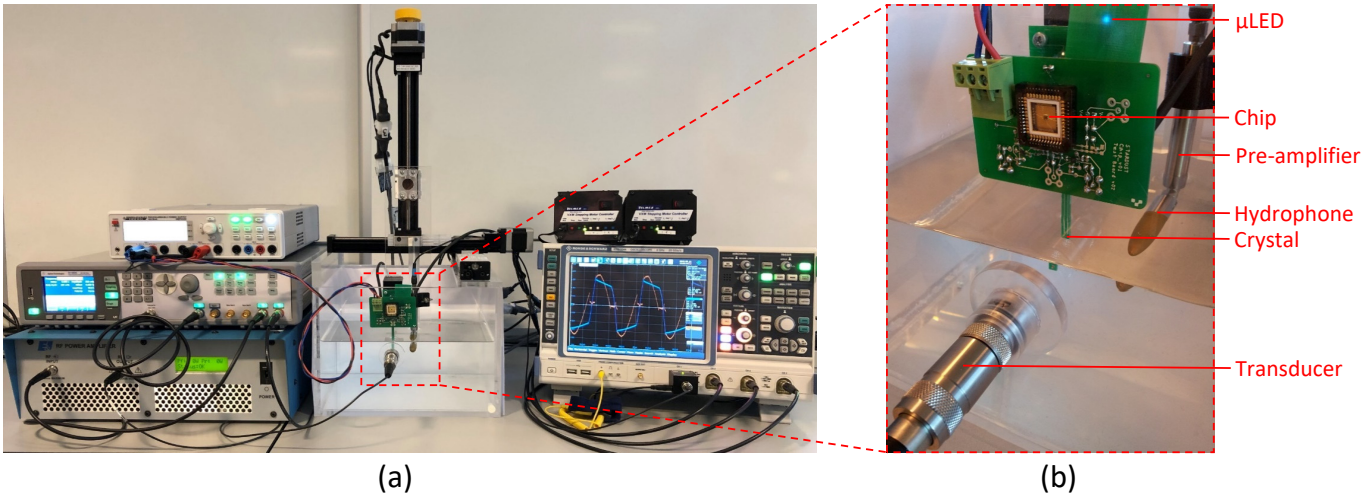


Fig. 8. (a) Picture of the experimental test setup used for measurements. Test equipment shown is: Agilent Technologies 81160A Pulse Function Arbitrary Generator, Electronics & Innovation RF Power Amplifier 50 dB, Rhode & Schwarz RTO 1044 Oscilloscope, Rhode & Schwarz Programmable Power Supply HMP2030. (b) Picture of the test board used for measurements with the active bridge rectifier chip, including the crystal dipped into the demineralized water below. Hanging to the right of the PCB is the HGL-0400 hydrophone and AH-2010 pre-amplifier from Onda Corporation used for calibrating the acoustic intensity. In the foreground the V303-SU transducer from Olympus can be seen.

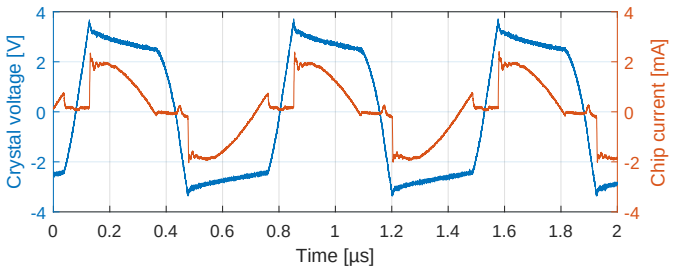


Fig. 9. Graph shows the voltage (blue) across the crystal and the current (red) through the chip during experimental tests.

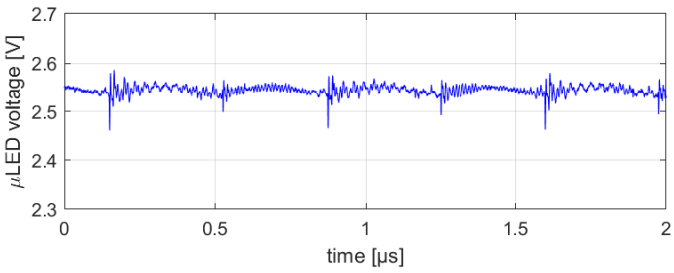


Fig. 10. Graph shows the voltage measured across the μLED during experimental tests.

$$P_{photo} = \eta_{wallplug} \times P_{\mu LED} = 813.11\mu W \quad (4)$$

$$P_{photoDensity} = \frac{4 \times P_{photo}}{\pi \times (0.1mm)^2} = 103.53mW/mm^2 \quad (5)$$

Despite the increasing activities in the field of ultrasonically powered devices, it has proven hard to find prior works, in which active rectifiers are employed, for comparison purpose. As a result, comparisons are also made to active rectifiers designed for inductive powering with a similar frequency range, which can be seen in Table III.

V. Integration

The final step is to integrate all the components in a compact manner. To this end, as a prototype, we first integrated all the components including a new application-specific μLED, a piezoelectric crystal and the diced CMOS chip containing the active bridge rectifier on a small glass substrate ($3mm \times 1.5mm$), and then covered the components with

TABLE III
COMPARISON WITH SIMILAR STATE-OF-THE-ART ACTIVE RECTIFIERS

	JSSC 2015 [15]	**JSSC 2017 [31]**	**TBCAS 2013 [19]**	**TBioCAS 2018 [7]**	**This work**
Technology (nm)	65 - TSMC (GP)	350 - 2P4M	350	180 - HV BCD	180 - TSMC (GP)
Chip Area with Pads (mm^2)	2.0	1.56	0.186	3.58	0.090
Powering Method	Ultrasonic	Inductive	Inductive	Ultrasonic	Ultrasonic
Frequency (MHz)	1.0	1.0	13.56	1.314	1.38
Amplitude of Input Voltage (V)	0.6 - 1.2	Not Available	1.5 - 4.0	3 - 4.5	1.5 - 3.3
Output Voltage (V)	1.0	3.2 - 3.3	1.19 - 3.52 (@ 500 Ω load)	3 V / 15	1.5 - 3.3
Output Power (mW)	0.1 (LDO output)	0.1 - 20	24.8 (max)	Not Available	0 - 6
Power Conversion Efficiency (%)	89.4 (@ 100 μW, simulated)	77 (@ 10 mW)	82.2 - 90.1% (@ 500 Ω load)	71.4	91.2 (@ 2.4 mW)

a Polydimethylsiloxane (PDMS) layer for bio-compatibility purpose. The integration is explained in the following sub-sections.

A. Micro-LED fabrication and characterization

The blue-emitting μLEDs were designed and fabricated by taking into account performance requirements and geometrical limitations in optogenetic applications. Due to supply power limitations for in-vivo applications, the μLED needs to be ultra-efficient at low currents, $0.5 - 5mA$, generate $1-20mW/mm^2$ of power density at a wavelength of $480nm$, while heating of the device ought to be under $1K$ to avoid cell damage, and it should be equipped for working in pulsed mode. To integrate the μLED with the rectifier, the μLED bond pads were $100\mu m \times 70\mu m$ in order to to match to the rectifier bond pads. We show below that a $100\mu m$ diameter mesa μLED meets the requirements. The $InGaN$ based LED material was grown on a Patterned Sapphire Substrate (PSS) to aid out-scattering of the light. The μLEDs were processed with p-type contacts $(Pd : Ni : Au = 10 : 20 : 30nm)$; high quality ohmic p-contact with contact resistivity of $10^{-4}\Omega cm^2$ was obtained; mesas were etched to the n-side $(1.2\mu m)$; n-type contact $(Ti : Al : Ti : Au = 20 : 170 : 50 : 100nm)$; deposition of a SiO_2 passivation layer $(295nm)$ and opened to the contact pads followed by the deposition of bond-pad metallization $(Ti : Au = 20 : 200nm)$. Then the sapphire substrate was ground and polished to reduce the thickness from $350\mu m$ to $120\mu m$. Finally, $83nm$ of SiO_2 was sputtered on the backside of the wafer to produce an Anti-Reflection Coating (ARC). The LEDs were diced to dimensions of $300\mu m \times 130\mu m$ to permit wirebonding to the crystal related pads when mounted on the rectifier.

The electro-optical performance of the μLEDs with different mesa sizes was evaluated. The turn-on voltage of the μLEDs is $2.5V$. The diode current voltage characteristic (6) shows that the diode ideality factor, η, reaches a low value of 1.2 at a voltage of $2.5V$ which is characteristic of efficient radiative recombination. In order to compare different device geometries the optical power from a solid angle of emission of $\pm 30^\circ$ (Numerical Aperture = 0.5) was measured. The External Quantum Efficiency (EQE) as a function of current and aperture size was measured (Fig. 11). EQE refers to the percentage of injected electrons that end up as photons out, (7).

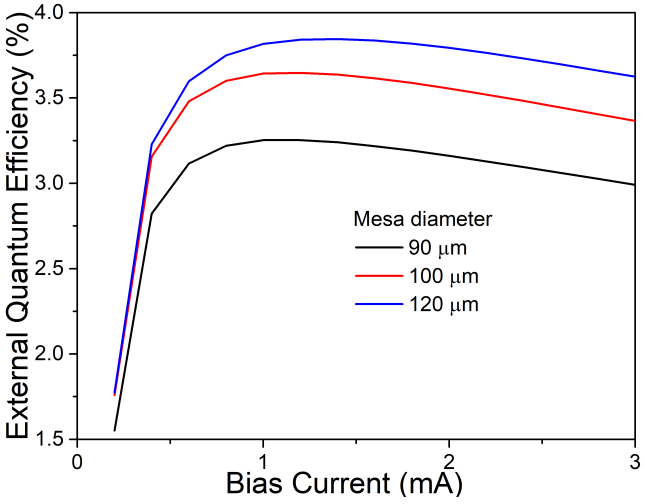


Fig. 11. External Quantum Efficiency as a function of bias current and mesa size.

The μLED with the largest mesa $(120\mu m)$ has the highest EQE of 3.8%, for a numerical aperture of 0.5 and this is reached at a current of $1.2mA$. However, the power *density* from a $100\mu m$ diameter mesa is higher while its EQE reaches a maximum of 3.6% at $1mA$ for a collection NA of 0.5. These currents match those expected for the device operation.

$$I = I_0 \exp \frac{qV}{\eta KT} \tag{6}$$

$$EQE = \frac{P_{photo}}{I \times \frac{hc}{\lambda}} \tag{7}$$

Fig. 12 shows the light emission collected into a numerical aperture of 1, which corresponds to all the light emitted downwards from the LED chip. This is obtained by placing the μLED directly onto the detector. We note that more than $1.5mW$ of optical power is measured at a current of $3mA$. This corresponds to $190mW/mm^2$ power density obtained from a $100\mu m$ mesa μLED, which is more than required for excitation of channelrhodopsin (ChR). The angular spread for a numerical aperture of 1 is 7 times that of a numerical aperture 0.5. As the power has increased by that amount, this suggests very effective scattering of the light. There is

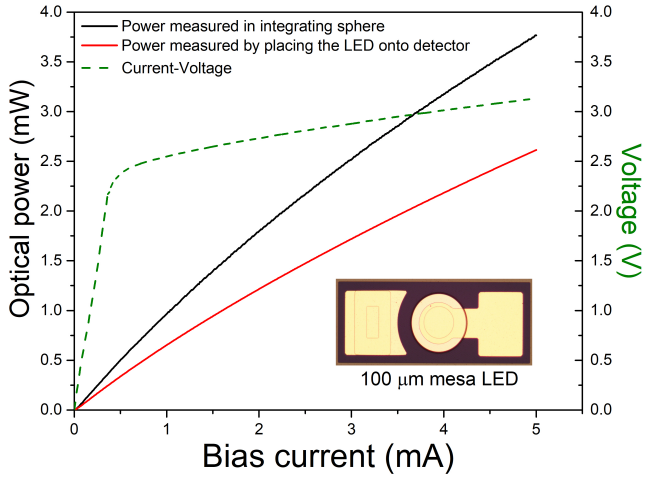


Fig. 12. Optical power and voltage as a function of bias current measured into $NA = 1$ and in integrating sphere. Inset is an image of the μLED

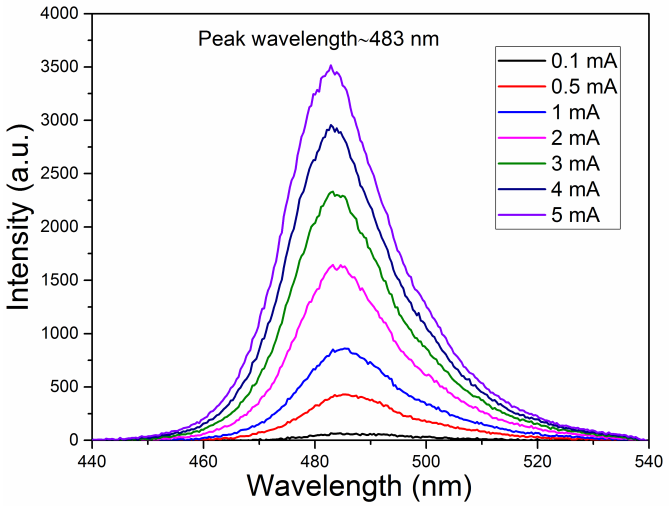


Fig. 13. Electroluminescence spectra from $100\mu m$ diameter mesa LED as a function of current.

additional light to be collected from the sides of the chip. Fig. 12, also demonstrates that an output power of $2.5mW$ is obtained when the emission is measured using an integrating sphere at $3mA$, which corresponds to collection of light from all the sides of the μLED. An extremely high EQE of 33% is obtained in this situation. Also, by embedding the μLED in an epoxy or in a index matching fluid about 8% more light can be extracted. At 1mA the measured integrated power is $0.94mW$ and voltage is 2.54 V and so the wall-plug efficiency of the μLED is 37% before encapsulation.

Finally, Fig. 13 shows the spectra of the emitted light which is peaked at $483nm$ and this is perfectly suited for excitation of channelrhodopsin transfected cells [32], [33].

B. Device integration

The integration concept of the device consisting of μLED $(330\mu m \times 130\mu m \times 120\mu m)$, rectifier chip $(300\mu m \times 300\mu m$ with $300\mu m$ thickness) and a piezoelectric crystal (PZT-4) $(500\mu m)^3$ is schematically illustrated in Fig. 14. Submounts of dimensions $3mm \times 1.5mm$ were designed and implemented on a $500\mu m$ thick glass wafer by evaporating gold pads to interconnect the individual elements of the power converter. The μLED pads are $500\mu m \times 500\mu m$ and the crystal pad is $1mm^2$ in size. An open space was left for the rectifier chip. Two gold studs were put down on the LED pads and $50\mu m$ solder bumps were put down on the studs. The bumps were then coined. Then the μLED was flip-chip bonded onto the studs of the μLED's pads using thermal compression at $270^{\circ}C$ for 20 seconds. Non-conductive epoxy was used on the μLED to hold the μLED strongly to the glass substrate. The crystal was mounted with conductive silver epoxy. A room temperature curable epoxy (curing time 8 hours) was used to prevent damage to the crystal by exposure to heat. Next, non-conductive epoxy was used to mount the rectifier chip to the glass submount. Precautions were taken while taking care of the rectifier chip as it doesn't have electrostatic discharge (ESD) protection. Finally, the interconnections are finished by gold wire bonding.

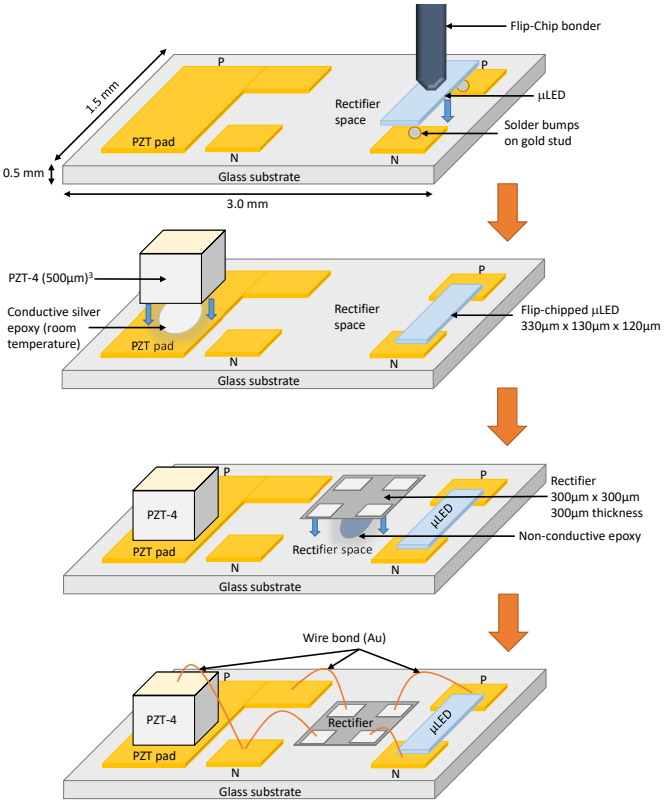


Fig. 14. Schematics for device integration steps.

C. Protective encapsulation

PDMS is a bio-compatible material that gives good acoustic impedance matching with water and tissue [34]. Therefore, it has been used here to encapsulate the integrated dust. For encapsulating, PDMS Sylgard 184 has been mixed with a hardener (10:1). Before deposition, the prepared PDMS should be degassed in a vacuum chamber to remove any bubbles. The

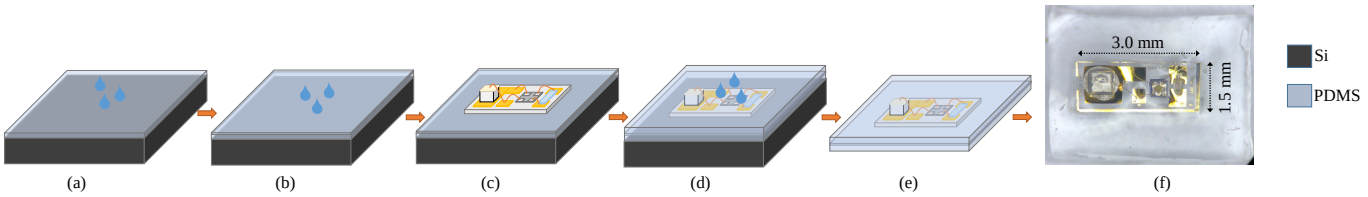


Fig. 15. (a) Spin coating and baking the first PDMS layer, (b) spin coating the 2nd PDMS layer, (c) placing the integrated dust and baking in the oven, (d) spin coating and baking the last PDMS layer on top of the whole sample, (e) peeling off the encapsulated integrated dust from the Si wafer, and (f) microscopic image of the encapsulated dust.

best approach among different recipes has been selected, and the procedure is explained as follows:

1) Spin coating PDMS layer at 500 rpm and 30 seconds on top of a cleaned silicon wafer.
2) Baking the sample in an oven at 80°C for 15 minutes.
3) Depositing another PDMS layer on top of the previous sample at 2000 rpm and 30 seconds.
4) Placing the integrated dust from the bottom inside the PDMS layer.
5) Placing the whole sample in the oven at 80°C for 15 minutes.
6) Spin coating the last PDMS layer on top of the whole sample at 500 rpm and 30 seconds.
7) Baking it in the oven at 80°C for 15 minutes.
8) Peeling off the PDMS encapsulated sample from the silicon wafer.

The schematic of the whole process and image of the encapsulated dust are shown in the Fig. 15. The total volume of the fully-packaged device is estimated around $2.85mm^3$, where 79% of this is the volume of the glass substrate provided for testing purpose only. The size of the substrate can be significantly reduced by using a thin-layer flexible substrate instead, e.g. few tens of micrometers. Furthermore, using advanced integration techniques, e.g. flexible substrate instead of wire-bonding as well as design of the chip in more scaled technology nodes can lead to a significant reduction of the total volume of the dust, which is envisioned to be done in the future by our group. Table IV shows the advantage and potential of the proposed device in terms of number and size of the components.

TABLE IV
COMPARISON WITH OTHER STATE-OF-THE-ART ULTRASONICALLY POWERED MINIATURIZED DEVICES

	This Work	TBioCAS 2018 [7]	JSSC 2019 [35]
Application	Brain Stimulation	peripheral nerve Stimulation	Neural Recording
Power carrier frequency (MHz)	3.14	1.314	1.78
Chip Area (mm^2)	0.09	3.58	0.25
On-Chip Cap. (pF)	100	1500	130
Technology	180-nm Standard	180-nm HV BCD	65-nm LP CMOS
Crystal Volume (mm^3)	0.125	4.084	0.421
Off-Chip Capacitors	No	Yes	No
Fully Packaged	Yes	Yes	Yes
Total Volume (mm^3)	2.85	39	0.8

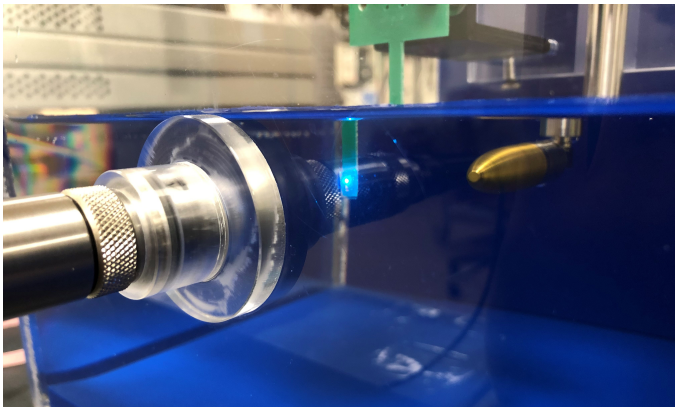


Fig. 16. Picture of the integration prototype under ultrasonic stimulation that in turn powers up and drives the μLED.

VI. DEMONSTRATION

To demonstrate the complete ultrasonically-powered microsystem, the integrated prototype dust, detailed in section V with its protective encapsulation, is mounted on the end of a narrow PCB and submerged in water in front of a transducer in the same way as the crystal in section IV, as seen in Fig. 16. As before, the prototype is subjected to an acoustic intensity calibrated to $7.2mW/mm^2$, however, this time at a frequency of $3.14MHz$ because of the smaller crystal dimensions of $(500\mu m)^3$. Given the integrated nature of the prototype dust and its complete electrical isolation, the only available feedback of successful ultrasonic power transfer is to visually observe that the μLED turns on. This can be seen successfully achieved in Fig. 16 where the blue light emitted from the μLED can be seen. Based on the numbers found in (5) and taking the reduced size of the receiving crystal into account (only a quarter power available), the optical power density of the μLED can be estimated to be $25.88mW/mm^2$. A video of the prototype dust during experimentation is uploaded as supplementary information to this paper. In the video the μLED blinks because the ultrasonic power is duty cycled and only transmits 10% of the time at a repetition frequency of $1Hz$. The acoustic intensity is $7.2mW/mm^2$ during duty cycle ON-time.

VII. Conclusion

A complete design cycle of creating an ultrasonically powered microsystem prototype, from concept through design, simulation, integration and experimental testing, confirming the process is viable and accurate, is given. The use of the Leach model for modeling piezoelectric crystals has proven a valuable addition to the repertoire of tools available for electrical simulations, especially since the model naturally supports transients analysis. This has led to the design and implementation of a compact integrated microsystem that has been tested successfully. The experimental results showed a 91.2 % efficiency of the rectifier chip. Practical issues arising from connected measurement equipment to the prototype test setup, particular the oscilloscope, has been solved successfully by adding local buffering and amplifier circuits right in between crystal and chip, thereby separating and isolating the equipment causing adverse effects and prevent corruption of measurements. The developed prototype in this paper is then integrated with a μLED with a wall-plug efficiency of 37% and packaged using bio-compatible materials, and successfully demonstrated in a laboratory setup.

In the future, further miniaturization via novel integration techniques, smaller μLEDs as well as smaller piezoelectric cubes and designing the integrated chip using more scaled technology nodes will be done to achieve smaller volume of the dust allowing optogenetic study of free-moving animals using fully-implantable dusts. Such device is not only applicable for Parkinson's disease but also other neurological disorders e.g. epilepsy.

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