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Broadband 5Gb/s Optical RAM Cell over the C-band

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Abstract: A broadband optical RAM cell comprising a monolithic InP Flip-Flop and a Random Access Gate is experimentally presented with at least 5 Gb/s error-free operation and less than 4.5dB power penalty across the whole C-band. © 2021 The Author(s)

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1. Introduction

Today the processor-memory bottleneck known as "Memory Wall" continues to plague system's performance by forcing its operation at memory's lower frequency, highlight the bandwidth limitation as predominant obstacle in data-centric computing [1]. As such, research community has been recently shifting towards optical memories [2] to fully exploit the optical interconnects at different computing hierarchy levels that will allow delivering several high-speed operation [3-7], energy and footprint [4,8,9] benefits. Towards scaling to multi-bit optical RAM architectures, the adoption of Wavelength Division Multiplexing (WDM) techniques [5,6,7] has validated the benefits of releasing hardware sharing, energy efficiency and scalability capability [6] with a few technology platforms recently achieving to demonstrate multi-bit memories using VCSELs [8], Phase-Change Memories (PCM) [9] or BH-PhC nanocavities [5] with up to 128-bit capacity [5]. However, these typically require wavelength-specific resonant designs with cavity optimization or high quality Q-factors, which on the one hand add significant design complexity while at the same time limit operation at a few certain wavelengths even below <0.5 nm [4,5] with strict power conditions [8,9]. On the contrary, optical memories relying on coupled MZI devices, despite not deploying any recirculating or feedback loop, have been theoretically proven to support resonant frequency response similar to ring cavities [10], towards robust operation with broad wavelength support and multi-bit WDM RAM architectures.

In this paper, we present the first such broadband optical RAM cell operation, relying on a monolithic InP Flip-Flop (FF) memory chip and a SOA-MZI Access Gate (AG), successfully performing all Write, Read, Grant Random Access functionalities under a wide wavelength range of external optical signals. The proposed optical RAM cell is evaluated at 5Gb/s under different SET/RESET memory-control wavelength pairs from 1534 up to 1560 nm, showing constantly clear eye diagrams and error-free operation of less than 4.5dB BER penalty, forming the first integrated optical RAM cell that supports almost the whole C-band. The proposed device can eliminate the need for M×N wavelength-specific RAM cells by simply replicating it as a generic unit at all column/rows of two-dimensional matrices, opening a path for all-passive wavelength address decoding of multi-bit WDM RAM banks.

2. Device and Experimental setup

The architecture of two-dimensional WDM optical RAM banks is shown in Fig. 1(a), where the proposed cell can act as a basic building block. It is designed using a master-slave SOA-MZI configuration based on the monolithic InP platform of Fraunhofer HHI [3] and an InP Semiconductor Optical Amplifier Mach-Zehnder Interferometer (SOA-MZI) AG employing WDM data encoding [6]. The InP chip has been optically and electrically packaged by Tyndall, as shown in Fig.1(b), while the GDS mask is shown in Fig. 3(c). Fig. 1(d), depicts the setup for testing the optical RAM cell. Two CWs (λ_{Bit}, $\lambda_{\overline{Bit}}$) by tunable laser sources (TLS) were modulated by Ti:LiNbO3 modulators (MOD) by 5Gb/s pattern generator (PPG) to produce complementary NRZ PRBS 2^7-1 Bit and $\overline{Bit}$ data, which were

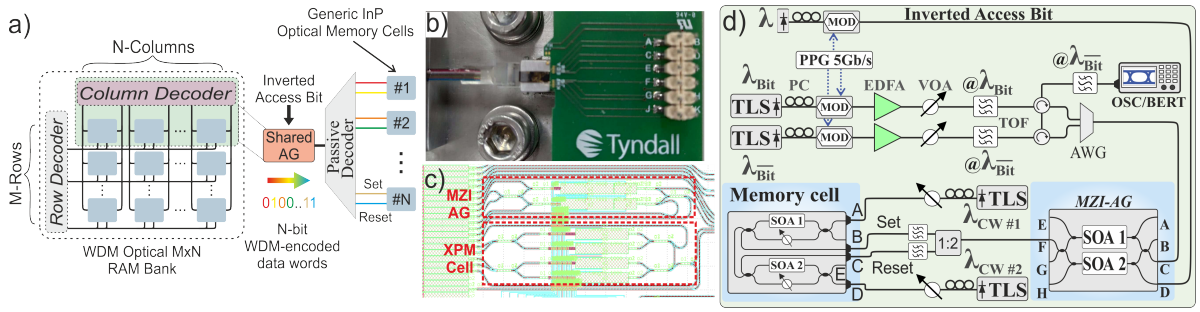
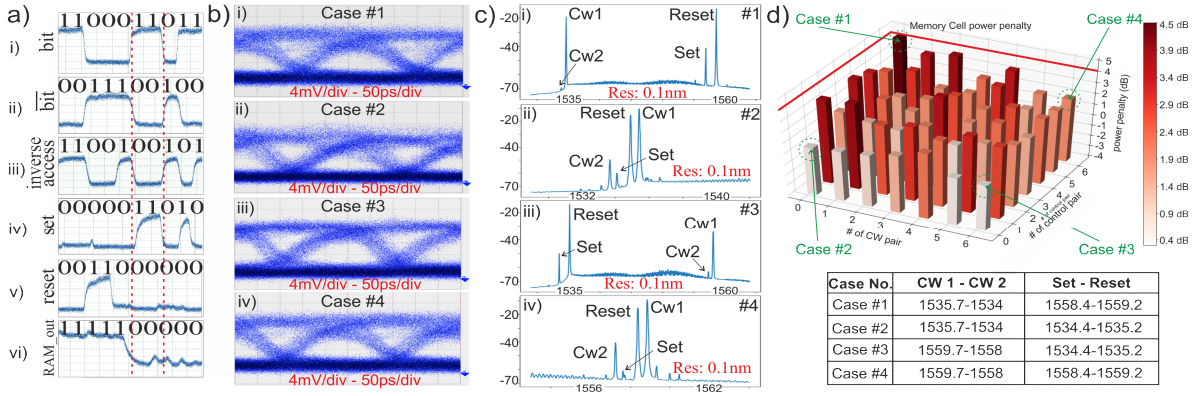


Fig. 1. a) WDM-enabled optical RAM bank with different SET/RESET wavelengths, shared AG and Passive DEMUX-based decoding, b) packaged InP monolithic chip, c) mask layout of SOA-MZI optical memory and AG and d) experimental setup for the broadband evaluation.

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Case No.	CW 1 - CW 2	Set - Reset
Case #1	1535.7-1534	1558.4-1559.2
Case #2	1535.7-1534	1534.4-1535.2
Case #3	1559.7-1558	1534.4-1535.2
Case #4	1559.7-1558	1558.4-1559.2

Fig.2. a) Experimental traces of 5Gb/s RAM operation, b) Eye diagrams at 50ps/div for the Wavelength pair Cases i) 1, ii) 2, iii) 3 and iv) 4 shown in the c) output spectra for the same cases and d) BER values for 49 different CW-Control wavelength pair combinations.

multiplexed via an AWG. The Bit and $\overline{Bit}$ were injected into the SOA-MZI-AG as input signals, along with an Inverted Access signal, decorrelated through different fiber propagation and fed as control to the SOA-MZI XPM On/Off-switch, determining if the data signals will be propagated to the memory or not. The propagated data stream is then splitted via a 1:2 coupler and then filtered by two optical bandpass filters, forming the SET and RESET wavelengths respectively. Both enter the FF through ports B and C, while $\lambda_{cw\#1}$ and $\lambda_{cw\#2}$ are propagated through ports A and D to provide 5Gb/s RAM cell operation [7]. The λ_{Bit} and $\lambda_{\overline{Bit}}$ were tested for [1534.4 - 1558.4] nm and [1535.2 - 1559.2] nm with a step of 4 nm, respectively and the two CWs ($\lambda_{cw\#1}$, $\lambda_{cw\#2}$) were tested for [1535.7 - 1559.7] nm and [1534 -1558] nm, with a step of 4 nm, respectively. The Inverse Access Bit signal was set at 1554.8 nm. The output signals during WRITE operation of the RAM cell were collected at C and E ports through a time oscilloscope (OSC) and at a Bit-Error-Rate-Tester (BERT) for further signal quality evaluation. Erbium-Doped fiber Amplifiers (EDFAs), Variable Optical Attenuators (VOAs) and Polarization Controllers (PCs) were used as shown in the setup, to tune the power and polarization of the signals in the range of [8.5-11] dBm for the $\lambda_{cw\#1}$ and $\lambda_{cw\#2}$ and [13.5-16] dBm for $\lambda_{ctr\#1}$ (SET) and the $\lambda_{ctr\#2}$ (RESET), while the SOAs were driven by 250 mA.

3. Experimental Results

Fig. 2(a), shows the synchronized time-traces of the principle of operation at 5Gb/s during WRITE and GRANT Memory Access of (i)-(ii) the Bit/$\overline{Bit}$, iii) Inverse Access, (iv)-(v) SET/RESET and (vi) RAM cell output signals. For the first 5 bits, Random Access is not granted to the Bit, leading to '0' SET pulses, where memory is retained for 1 ns, while the red marker highlights a successful Write of Bits '00' in the cell when the Inverted Access is '00'

Fig. 2(b) and (c), represent the eye diagrams and output spectra for four distinctly different cases of SET/RESET and CW wavelength pair combinations, placed at the four edges of the tested cases. The results were obtained at C and E ports of the InP memory chip, where the RAM output and CW1 and RESET emerge as powerful signals and CW2 and SET appear weakly after reflection. For all four cases, the eye diagrams exhibit an Extinction Ratio of 4.7 dB. Finally, various possible combinations of control and CW pairs in the SOA-gain spectrum were tested with a 4nm step-resolution in the 26nm range, resulting in a two-dimensional set of 49 measurements (7x7 steps). All BER penalty values are plotted in the bar diagram of Fig. 2(d), with a light-to-dark coloring between a 0.4-to-4.4 dB range, being constantly lower than a 4.5 dB upper limit, verifying 5Gb/s fast, error-free and broadband optical RAM cell operation across almost the whole C-band.

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