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Digital Control of a Multi-Channel Boundary-Conduction-Mode Boost Converter for Power-Factor-Correction Applications

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A thesis presented to the National University of Ireland for the degree of Doctor of Philosophy

Submitted September, 2019

Supervised by Dr. John G. Hayes

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Ireland

DECLARATION

I hereby declare that I am the sole author of this thesis and all of the work undertaken in this thesis is original in content and was carried out by the author. Work carried out by others has been duly acknowledged in this thesis.

This is a true copy of the thesis, including any required final revisions, as accepted by my examiners. The work presented has not been accepted in any other previous application for a degree.

Signed: 

Date: 15/04/2021

ABSTRACT

This thesis focuses on the design of digital control schemes for multi-channel boundary-conduction-mode (BCM) boost converters. Multi-channel BCM boost converters are commonly used for the front-end power-factor-corrected (PFC) stage of isolated ac-dc power supplies due to the advantages of being low cost and having high efficiency for a universal line-voltage input. Single-channel and two-channel BCM boost converters using analog control ICs have been commonly used in industry. However, the use of multi-channel BCM boost converters with more than two-channels has been limited as there are no analog control integrated circuits (IC) existing on the market with the ability to control BCM boost converters with more than two channels. Digital microcontrollers are an enabling technology, which can be used to implement a control scheme for a multi-channel BCM boost converter with any number of boost-converter channels.

Moreover, digital microcontrollers have the added benefit of reducing the power supply's overall system cost. For example, in an ac-dc medical power supply, there is typically a dedicated analog control IC for the PFC stage, a dedicated analog control IC for a dc-dc isolated stage, and a low-power microcontroller used for safety and house-keeping functions, such as reducing standby power, detecting line-fault conditions, providing external communications, etc. The total system cost is reduced by replacing these three chips with a single microcontroller, which provides all the same functions. This requires the development of digital control algorithms which enable the microcontroller to match the performance of the analog control IC for the PFC stage. These functions include providing a well-regulated output voltage, ensuring the input current has high power quality, and permitting interleaving between the different boost-converter channels.

It is difficult to have a well-regulated output voltage for two reasons. Firstly, the controller must provide fast output-voltage dynamics over the universal line-voltage range from 85 Vrms to 265 Vrms. Secondly, the output voltage of PFC rectifiers contains a 2^{nd} harmonic ripple which can be fed into the control loop and distort the line current. In this work, an adaptive notch filter which works over a range of line frequencies, is designed to attenuate the feedback of the 2^{nd} harmonic ripple. The notch filter allows the voltage compensator to be designed at a higher bandwidth, thus ensuring fast output-voltage regulation. Moreover, an adaptive voltage-compensator gain is used to guarantee fast output-voltage regulation at all line voltages.

BCM boost converters have a variable switching frequency. Hence, a phase-shift control scheme is used to allow interleaving between the different boost-converter channels. It is important that the phase-shift control scheme requires minimal microcontroller computational

resources. This allows a low-cost microcontroller to be used. In this work, a novel phase-shift control scheme is proposed. The phase-shift control algorithm is executed at a fixed frequency much lower than the maximum switching frequency of the converter. This reduces the computational requirements of the algorithm.

It is important that the PFC controller provides low input-current distortion. BCM boost PFC rectifiers suffer from a zero-crossing distortion of the line current. Feedforward control is commonly adopted in to overcome this problem, however most digital feedforward control schemes require complicated design procedures or are computationally expensive. In this work, a novel feedforward algorithm is proposed which has a simple design procedure, low computational requirements and provides high power factor.

In applications which are not cost sensitive, it can be more preferable to use a more powerful microcontroller and more computationally expensive algorithms. Hence, a digital average-current-mode-control (ACMC) scheme is proposed to regulate the input current of BCM boost converter. The algorithm allows for an even greater improvement in power quality of the input line current compared to feedforward control, but comes at the cost of a more complex controller implementation.

The design, implementation and performance of the proposed digital control algorithms have been experimentally verified. Experimental results for the different control schemes are demonstrated on a 2-channel 600 W and a 3-channel 1 kW BCM PFC rectifier.

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2. R. T. Ryan, J. G. Hayes, R. Morrison and D. Hogan, "A digital closed-loop control strategy for maintaining the 180° phase shift of an interleaved BCM boost converter for PFC applications," *IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 4927-4934.

3. R. T. Ryan, J. G. Hayes, R. J. Morrison and D. N. Hogan, "Improved zero-crossing distortion of a boundary-conduction-mode boost converter with digital average-current-mode control," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 1846-1853.

4. R. T. Ryan, J. G. Hayes, R. J. Morrison and D. N. Hogan, "Using feedforward digital control to improve the power quality of a three-channel BCM boost converter for PFC applications," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, 2019, pp. 1743-1750.

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NOMENCLATURE

ac	Alternating current
ACMC	Average-current-mode control
ADC	Analog-to-digital converter
ASIC	Application-specific integrated circuit
BCM	Boundary-conduction mode
BOM	Bill of materials
CENELEC	European committee for electrotechnical standardization
CCM	Continuous-conduction mode
CE	Conformité européenne
CM	Common mode
COTC	Constant-on-time control
CPU	Central processing unit
CrCM	Critical-conduction mode
CT	Computed tomography
dc	Direct current
DCM	Discontinuous-conduction mode
DM	Differential mode
DSP	Digital signal processor
EMC	Electro-magnetic compliance
EMI	Electro-magnetic interference
ESR	Equivalent-series resistance
FF	Feedforward
IC	Integrated circuit
IEC	International Electrotechnical Commission
LED	Light-emitting diode
LCD	Liquid-crystal display
LUT	Look-up table
MCU	Microcontroller
MOSFET	Metal-oxide field-effect transistor
MRI	Magnetic-resonance imaging
PFC	Power-factor correction
PLL	Phase-locked loop
PWM	Pulse-width modulation
rms	Root mean squared
S&H	Sample and hold
Si	Silicon

SiC ..... Silicon Carbide

SMPS .... Switched-mode power supply

UVLO ... Under-voltage lockout

ZCD ..... Zero-current detection

ZOH ..... Zero-order hold

a ..... Lead-lag controller transfer function coefficient

A_e ..... Elliptic-filter denominator fixed-point scaling coefficient

A_n ..... Notch-filter denominator fixed-point scaling coefficient

A_v ..... Voltage-controller denominator fixed-point scaling coefficient

A_k ..... Voltage-controller adaptive-gain fixed-point scaling coefficient

A_m ..... Phase-shift controller gain fixed-point scaling coefficient

A_x ..... Notch-filter input fixed-point scaling coefficient

a_{e1} ..... Elliptic-filter denominator coefficient

a_{e2} ..... Elliptic-filter denominator coefficient

A_{e1} ..... Elliptic-filter fixed-point denominator coefficient

A_{e2} ..... Elliptic-filter fixed-point denominator coefficient

a_{v1} ..... Voltage-controller denominator coefficient

a_{v2} ..... Voltage-controller denominator coefficient

A_{v1} ..... Voltage-controller fixed-point denominator coefficient

A_{v2} ..... Voltage-controller fixed-point denominator coefficient

B_e ..... Elliptic-filter numerator fixed-point scaling coefficient

B_n ..... Notch-filter numerator fixed-point scaling coefficient

B_v ..... Voltage-controller numerator fixed-point scaling coefficient

b_{e0} ..... Elliptic-filter numerator coefficient

b_{e1} ..... Elliptic-filter numerator coefficient

b_{e2} ..... Elliptic-filter numerator coefficient

B_{e0} ..... Elliptic-filter fixed-point numerator coefficient

B_{e1} ..... Elliptic-filter fixed-point numerator coefficient

B_{e2} ..... Elliptic-filter fixed-point numerator coefficient

b_{n0} ..... Notch-filter numerator coefficient

b_{n1} ..... Notch-filter numerator coefficient

b_{n2} ..... Notch-filter numerator coefficient

B_{n0} ..... Notch-filter fixed-point numerator coefficient

B_{n1} ..... Notch-filter fixed-point numerator coefficient

B_{n2} ..... Notch-filter fixed-point numerator coefficient

b_{v0} ..... Voltage-controller numerator coefficient

b_{v1} ..... Voltage-controller numerator coefficient

b_{v2} ..... Voltage-controller numerator coefficient

B_{v0} ..... Voltage-controller fixed-point numerator coefficient

B_{v1} ..... Voltage-controller fixed-point numerator coefficient

B_{v2} ..... Voltage-controller fixed-point numerator coefficient

C_2 ..... Capacitor used as part of the current sense circuit

C_{ds} ..... Drain-source capacitance

C_{in} ..... Input capacitance

C_o ..... Output capacitance

$C_c(s)$ ..... Current-controller transfer function in the Laplace domain

$C_v(s)$ ..... Voltage-controller transfer function in the Laplace domain

$C_v(z)$ ..... Voltage-controller transfer function in the $\mathcal{Z}$-domain

C_{zcd} ..... Zero-current detection timing capacitor

d ..... Duty cycle

D_Q ..... Boost-switch body diode

D_z ..... Zener diode used in the ZCD circuit

D ..... Boost diode

D_1 ..... Boost diode of the first boost-converter channel

D_2 ..... Boost diode of the second boost-converter channel

D_n ..... Boost diode of the n^{th} boost-converter channel

D_{s1} ..... Input voltage sensing diode

D_{s2} ..... Input voltage sensing diode

e ..... Euler's number

e_c ..... Current error signal

$E_c(z)$ ..... Current error signal representation in the $\mathcal{Z}$-domain

e_v ..... Voltage error signal

$E_v(z)$ ..... Voltage error signal representation in the $\mathcal{Z}$-domain

f_L ..... Line frequency

f_p ..... Current-sensor pole frequency

f_{pwm} ..... PWM peripheral clock frequency

f_{sw} ..... Switching frequency

$G_i(s)$ ..... Open-loop model of the current loop in the Laplace domain

$H_e(z)$ ..... Elliptic-filter transfer function in the $\mathcal{Z}$-domain

H_i ..... Comined gain of the current sense circuit, ADC, and scaling in microcontroller software

$H_n(z)$ ..... Notch-filter transfer function in the $\mathcal{Z}$-domain

H_v ..... Output voltage sensor and ADC gain

H_{vin} ..... Input voltage sensor and ADC gain

i_e ..... Error current

i_{Cin} ..... Average current that flows through the input capacitor

i_{in} ..... Rectified input current

$i_{in(avg)}$ .... Average rectified input current over a switching period

$I_{in(pk)}$ ..... Peak rectified input current

$I_{in(rms)}$ .... Rms value of the rectified input current

$\widetilde{i_{in(avg)}}$ .... Deviation of the average input current from its dc operating point

I_{in} ..... Dc operating point for the switching-period-averaged rectified input current

$I_{in}(s)$ ..... Rectified-input-current representation in the Laplace domain

i_L ..... Inductor current

$i_{L(avg)}$ .... Average inductor current

$i_{L1(avg)}$ ... Average inductor current of the first channel

i_{L1} ..... Inductor current of the first boost-converter channel

i_{L2} ..... Inductor current of the second boost-converter channel

i_{Ln} ..... Inductor current of the n^{th} boost-converter channel

i_{LN} ..... Inductor current of the N^{th} boost-converter channel

$i_{L(pk)}$ ..... Peak inductor current

i_{line} ..... Line current

i_o ..... Output current

$i_{o(avg)}$ .... Average output current

$I_{o(avg)}$ .... Dc operating point of the average output current

$\widetilde{i_{o(avg)}}$ .... Deviation of the average output current from its dc operating point

i_{ref} ..... Reference current

$I_{ref(pk)}$ ... Peak reference current

i_{relay} ..... Soft-start relay current

I_1 ..... Constant-current source used to generate the analog PWM ramp signal of the master channel

I_n ..... Constant-current source used to generate the analog PWM ramp signal of the n^{th} channel

I_{n1} ..... Constant-current source used to generate the analog S&H phase shift and switching period signals of the n^{th} channel

k ..... Current-reference scaling factor

K ..... Voltage controller gain

k_c ..... Digital voltage controller gain

k_v ..... Digital voltage controller adaptive gain

K_i ..... Current controller integral gain

k_i ..... Adaptive digital current controller gain

k_{ci} ..... Digital current controller gain

k_m ..... Phase-shift controller gain

K_m ..... Phase-shift controller fixed-point gain

K_v ..... Voltage controller fixed-point gain

L ..... Boost inductance

M_1 ..... Transistor used to generate the analog PWM ramp signal of the master channel

M_n ..... Transistor used to generate the analog PWM ramp signal of the n^{th} channel

M_{n1} ..... Transistor used to generate the analog S&H phase shift and switching period signals of the n^{th} channel

n ..... Index number which is used to describe each boost converter channel

N ..... Number of boost converter channels

N_{vin} ..... Number of input voltage samples taken within a half-line period

P_o ..... Output power

PWM_1 ... PWM signal of the first boost-converter channel

PWM_2 ... PWM signal of the second boost-converter channel

PWM_3 ... PWM signal of the third boost-converter channel

PWM_n ... PWM signal of the n^{th} boost-converter channel

Q ..... Boost switch

Q_1 ..... Boost switch of the first boost-converter channel

Q_2 ..... Boost switch of the second boost-converter channel

Q_n ..... Boost switch of the n^{th} boost-converter channel

r ..... Notch-filter selectivity

R ..... Load resistance

R_1 ..... Resistor which is part of the current sensing circuit

R_2 ..... Resistor which is part of the current sensing circuit

R_{shunt} .... Current-sense shunt resistor

R_{zcd} ..... Current-limiting resistance for the ZCD circuit

s ..... Laplace operator

t ..... Time

t_2 ..... Time when the drain-source voltage has charged to the output voltage level

t_3 ..... Time when the inductor current first reaches zero

t_4 ..... Time when the valley in the drain-source voltage occurs

t_5 ..... Time when the inductor current reaches zero and the drain-source voltage is zero

t_{add} ..... Additional on-time added to the voltage-compensator output

$TBPRD$ .. Time-base period register of the PWM peripheral

$TBCTR$ .. Time-base counter register of the PWM peripheral

$T_{ci}(z)$ ..... Compensated open-loop current-loop transfer function in the $\mathcal{Z}$-domain

$T_{ci}(s)$ ..... Compensated open-loop current-loop transfer function in the Laplace domain

$T_{cv}(z)$ .... Compensated open-loop voltage-loop transfer function in the $\mathcal{Z}$-domain

$T_{cv}(s)$ .... Compensated open-loop voltage-loop transfer function in the Laplace domain

T_L ..... Line period

T_m ..... Phase-shift control loop execution period

t_{off} ..... Off-time

t_{on} ..... On-time

$t_{on(ticks)}$ ... On-time in units of clock ticks

t_{on1} ..... On-time of the first channel

$t_{on1(ticks)}$ .. On-time of the first channel in units of clock ticks

t_{on2} ..... On-time of the second channel

$t_{on2(ticks)}$ .. On-time of the second channel in units of clock ticks

t_{on3} ..... On-time of the third channel

$t_{on3(ticks)}$ .. On-time of the third channel in units of clock ticks

t_{onn} ..... On-time of the n^{th} channel

$t_{onn(ticks)}$ .. On-time of the n^{th} channel in units of clock ticks

$t_{\Delta n}$ ..... Perturbation added to the on-time of the n^{th} channel

$t_{on(min)}$ ... Minimum on-time which multichannel operation is possible for

$\widetilde{t_{on}}$ ..... Deviation of the on-time from its dc operating point

T_{on} ..... Dc operating point of the on-time

$T_{on}(s)$ .... On-time representation in the Laplace domain

$T_{on(ticks)}(z)$ On-time in units of clock ticks representation in the $\mathcal{Z}$-domain

t_{psn} ..... Phase shift between the first and the n^{th} boost-converter channel

t_{psn} ..... Phase shift between the first and the n^{th} boost-converter channel in units of clock ticks

t_{ps2} ..... Phase shift between the first and the second boost-converter channel

t_{ps3} ..... Phase shift between the first and the third boost-converter channel

t_{refn} ..... Reference phase shift for the the n^{th} boost-converter channel

$t_{refn(ticks)}$. Reference phase shift for the n^{th} boost-converter channel in units of clock ticks

$t_{ref2(ticks)}$. Reference phase shift for the second boost-converter channel in units of clock ticks

$t_{ref3(ticks)}$. Reference phase shift for the third boost-converter channel in units of clock ticks

$T_v(z)$ ..... Voltage-controller sampling period

t_{sw} ..... Switching period

t_{sw1} ..... Switching period of the first boost converter channel

v_{aux} ..... Voltage across the boost inductor auxiliary winding

v_c ..... Voltage-compensator output

v_{dc1} ..... Output voltage of the first module

v_{dc2} ..... Output voltage of the second module

v_{dcx} ..... Output voltage of the x^{th} module

V_{EA} ..... Analog voltage error-amplifier output

V_{EA_n} ..... Adjusted analog voltage error-amplifier output for the n^{th} boost-converter chan-

nel

v_{ds} ..... Drain-source voltage

v_{gs} ..... Gate-source voltage

v_{gs1} ..... Gate-source voltage of the first boost-converter channel

v_{gs2} ..... Gate-source voltage of the second boost-converter channel

v_{gsn} ..... Gate-source voltage of the n^{th} boost-converter channel

v_{gsN} ..... Gate-source voltage of the N^{th} boost-converter channel

v_{iin} ..... Output voltage of the current-sense circuit

$V_{iin}(s)$ .... Representation of v_{iin} in the Laplace domain

v_{in} ..... Rectified input voltage

$\widetilde{v_{in}}$ ..... Deviation of the rectified input voltage from its dc operating point

$V_{in(max)}$ ... Maximum rated instantaneous rectified input voltage

$V_{in(avg)}$ ... Average input voltage over a line cycle

$V_{in(avg(nom))}$ Nominal average input voltage over a line cycle

$V_{in(pk)}$ .... Peak rectified input voltage

$V_{in(rms)}$ ... Rms value of the rectified input voltage

$V_{in(rms(nom))}$ Nominal rms input voltage over a line cycle

$V_{in(th)}$ .... Input voltage threshold for sensing the line period

$V_{in}(z)$ .... Instantaneous input voltage $\mathcal{Z}$-domain representation

$V_{in(avg)}(z)$. Average input voltage $\mathcal{Z}$-domain representation

v_{line} ..... Line voltage

$V_{line(rms)}$ .. Line voltage rms value

v_o ..... Output voltage

$\widetilde{v_o}$ ..... Deviation of the output voltage from its dc operating point

V_o ..... Dc operating point of the output voltage

v_{ramp} ..... Analog PWM ramp signal

V_{ref} ..... Reference reference

v_{zcd} ..... Output voltage from the ZCD circuit

z ..... $\mathcal{Z}$-domain operator

ZCD ..... Zero-current-detection signal

ZCD_1 .... Zero-current-detection signal for the first boost-converter channel

ZCD_2 .... Zero-current-detection signal for the second boost-converter channel

ZCD_3 .... Zero-current-detection signal for the third boost-converter channel

ZCD_n .... Zero-current-detection signal for the n^{th} boost-converter channel

x_n ..... Notch-filter input

y_n ..... Notch-filter output

η ..... Efficiency

ω ..... Angular frequency

ω_c ..... Angular cross-over frequency

ω_{ci} ..... Angular cross-over frequency of the current loop

ω_L ..... Angular line frequency

ϕ_m ..... Phase margin

ϕ_p ..... Angular frequency of the current sensor pole

ω_r ..... Angular resonant frequency between the boost inductor and boost switch's parasitic capacitance

ϕ_{max} ..... Maximum phase injected by the lead-lag controller

τ ..... Lead-lag controller transfer function coefficient

1 INTRODUCTION

This chapter presents an overview of the research topics discussed in this dissertation. The body of work is focused on the implementation of digital control schemes for a multi-channel boundary-conduction-mode boost converter used as an ac-dc PFC power supply. The application of this converter is for modular configurable ac-dc power supplies which are predominately used in medical and industrial applications. This chapter introduces the modular configurable power supply architecture and its application, the multi-channel BCM boost converter used as a PFC rectifier, and the motivation for using digital control to reduce cost and improve the performance of the PFC stage of the power supply.

1.1 Overview

Modular configurable power supplies have become a widely-adopted industry solution to power the next generation of medical equipment. Companies such as Excelsys Technologies, Vox Power, Mean Well, TDK-Lambda, Delta and Artesyn have all developed a range of products for this growing market [2]–[7]. This type of power supply is used in applications such as surgical-robotic systems, medical-laser systems, clinical-diagnostic equipment and medical-imaging machines, such as magnetic-resonance-imaging (MRI), X-ray and computed tomography (CT) machines.

The main driving factor for the growth in the market for medical equipment and medical power supplies is the aging population. The proportion of the global population aged 60 years and over is expected to increase from 10.0% in 2000 to 21.8% in 2050 and to 32.2% in 2100 [8]. Figure 1.1 shows the United Nations projected forecast for the number of people aged 60 years and over in the world population [1]. The same trend is true for Ireland's population, and the population of the developed regions of the world.

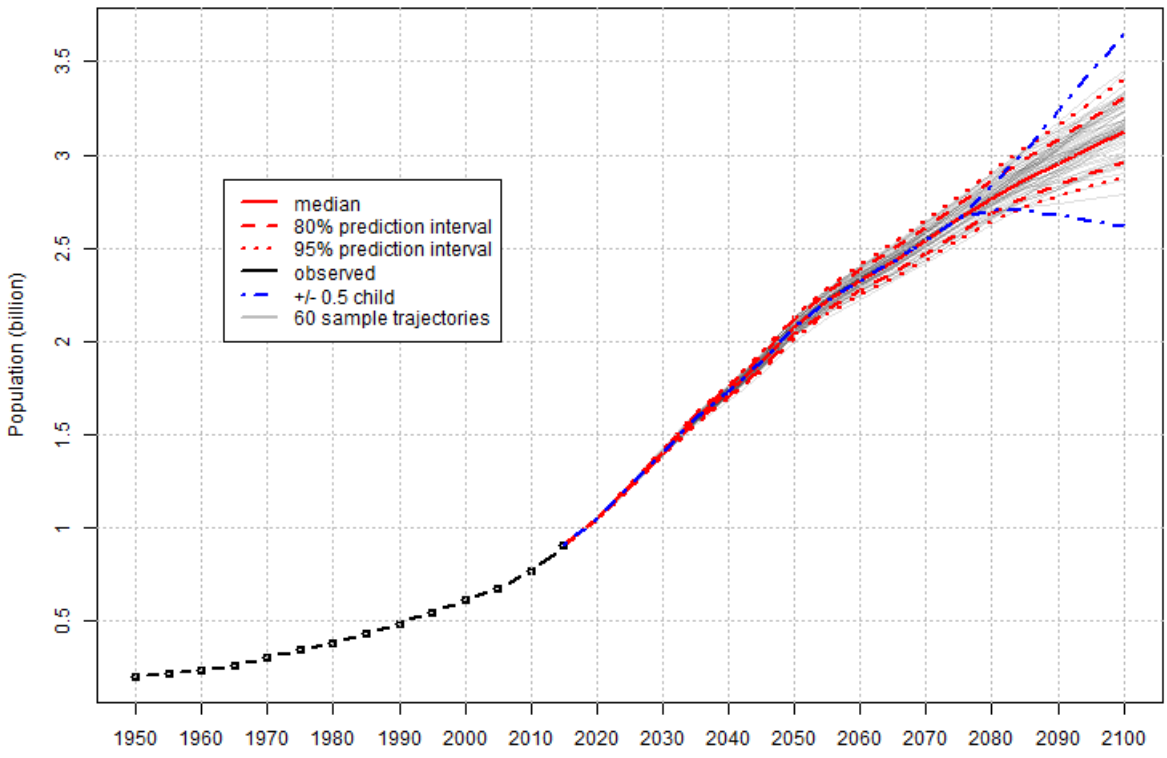


Figure 1.1. World population aged 60 years and over [1].

An example of a modular configurable power supply used in medical applications is the CoolX600 from Excelsys Technologies shown in Figure 1.2. It converts the ac mains voltage to four isolated well-regulated dc output voltages. It can supply a total output power of 600 W, with each individual output capable of delivering a maximum power of 200 W.

The architecture for this type of power supply is shown in Figure 1.3. There are three stages of power conversion in this power supply. The first stage consists of an ac-dc power-

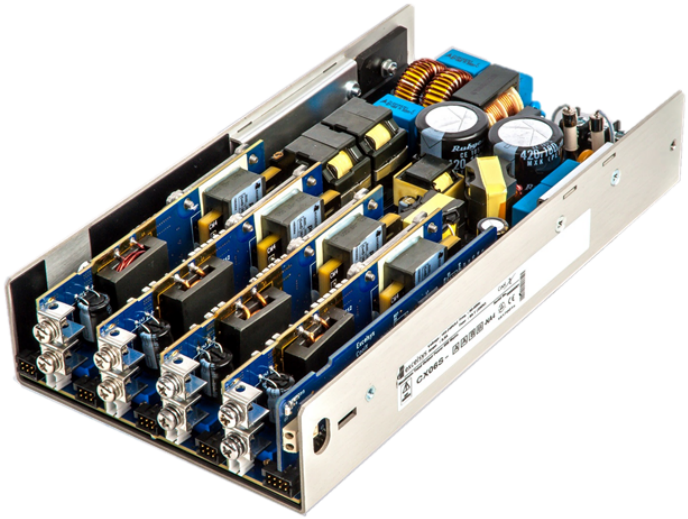


Figure 1.2. The CoolX600 modular configurable ac-dc 600 W medical power supply from Excelsys Technologies.

factor-correction (PFC) stage, it converts the universal mains input voltage to a non-isolated regulated dc voltage of typically around 400 V. The second stage is a dc-ac isolation stage, typically either an LLC converter or a phase-shifted full-bridge or half-bridge converter. This stage converts the large dc voltage to a high-frequency ac voltage, to create an ac bus that feeds several small high-frequency transformers. The third stage is the rectifier and dc-dc stage. For low voltage applications of less than 48 V output, this stage typically consists of a center-tapped synchronous rectifier which rectifies the high-frequency ac voltage from the transformer secondary. The output voltage from the synchronous rectifier is an isolated, but poorly-regulated, dc voltage. A synchronous dc-dc buck converter transforms this voltage to a well-regulated output voltage, denoted v_{dcx}. Each rectifier and dc-dc stage is known as a module. The CoolX600 in Figure 1.2 has four modules. It is possible to design each module for different output voltage ranges. This type of power supply architecture is highly configurable, as each of the module outputs can be series connected for higher voltage loads, parallel connected for higher current loads, or left as independent isolated outputs. The advantage of this configurable modular solution for the power-supply user is that system development time, and the ability to maintain safety approvals is mush easier than for a custom power supply design for a specific application.

For certain applications there is a large demand to develop power supplies with low vibration and low acoustic noise. This is particularly true for all vibration-sensitive measuring equipment. Power-supply cooling fans are a major source of vibrational and acoustic noise. However, fans are very advantageous for power supplies, as they allow heat generated by losses in the power supply to be removed by forced convection. To build a power supply with no fans requires a high efficiency, so that less heat is generated inside the power supply. Designing a power supply to achieve excellent power density is not as critical because power-

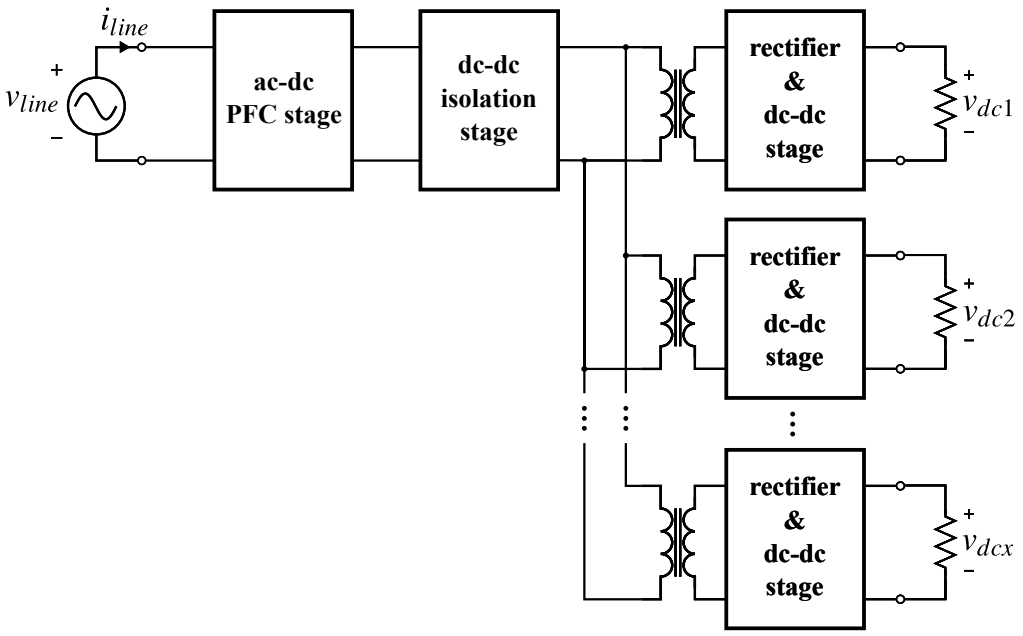


Figure 1.3. Modular power-supply architecture.

supply components must have adequate surface area to remove heat by natural convection. Furthermore, removing the fans from a power supply greatly increases system reliability by removing the only moving mechanical parts which can wear over time. This leaves power-supply designers with the challenging task of building high efficiency fan-less power supplies while still maintaining the low-cost solution which customers demand.

An ac-dc power supply is dependant on many different control feedback loops to ensure proper operation. For instance, the output voltage of the buck converter inside a module is typically regulated using peak-current-mode control. The PFC stage must regulate its output voltage at 400 V, while also controlling the shape of the line current so that it has the same shape as the line voltage. Typically, these control functions are implemented using application-specific integrated circuits (ASICs). However, recent improvements and lower costs of microcontrollers and digital-signal processors (DSPs) for power-electronics applications have led to the increased adoption of digital control in switched-mode power supplies. These advances have presented power-supply designers with the opportunity to improve power-supply performance, while simultaneously lowering system cost, by replacing analog control with digital control.

This dissertation introduces the use of digital control to improve the performance of an ac-dc PFC power converter. A digital control scheme is designed and built for a 600 W 2-channel boundary-conduction-mode (BCM) boost converter. A second digital control scheme is developed for a 3-channel 1 kW BCM converter using a low-cost microcontroller, which exhibits excellent performance in terms of output voltage tracking andpower quality, as well as other inherent advantages of digital control.

The objective of this chapter is to give a brief introduction to the modular configurable

power supply and its applications in medical equipment, as well as the motivation for developing solutions with lower costs and improved efficiencies using digital control. Section 1.1 presents a short overview for the motivation of the work described in this thesis. Section 1.2 describes the objectives of this thesis. Section 1.3 gives a chapter-by-chapter summary of the thesis. Section 1.4 discusses power factor, power-factor correction and applicable standards. Finally, Section 1.5 explains the fundamental operation of the boost converter, followed by the advantages of using a multi-channel BCM boost converter topology.

1.2 Thesis Objectives

This thesis has the following four objectives.

The first objective is the design of a suitable control scheme to regulate the output voltage of the converter that is suitable for implementation on an inexpensive microcontroller. The control scheme must be robust and capable of handling rated-power loadsteps and worst-case line voltage disturbances. Similarly, the proposed control scheme must display satisfactory behaviour for a universal line-voltage input. Moreover, the control scheme must provide good tracking performance of the output voltage while simultaneously ensuring the input line current maintains a good power factor.

The second objective is to design a digital-control scheme that can maintain the correct interleaving of a multi-channel BCM boost converter. Maintaining the correct phase-shift between different boost converter channels is important as this dramatically reduces the input and output current ripple of the interleaved converter, which in turn reduces rms current stress and the electromagnetic interference generated by the converter. As the BCM boost topology has a natural variable switching frequency, maintaining the correct phase shift between the different boost-converter channels becomes a challenging design task. It is also important that the proposed control scheme ensures that proper BCM operation of each boost-converter channel is always maintained, and that no channel can ever enter continuous-conduction-mode (CCM) or discontinuous-conduction-mode (DCM) operation. Furthermore, the proposed control scheme must be suitable for implementation on a low-cost microcontroller.

The third objective is to propose a simple effective variable-on-time digital feedforward (FF) algorithm to improve the power quality of a BCM boost converter for PFC applications. BCM boost converters are known to suffer from a zero-crossing distortion of the line current. The distortion is caused by the converter's valley-switching behaviour and effects of the input filter capacitor. The proposed digital feedforward scheme must be easy to design and easy to implement, with a significant reduction in the converter's line-current distortion over the universal line-voltage range and power range.

The final objective is to introduce a novel digital control scheme that uses average-current-mode-control (ACMC) to improve the power factor of a multi-channel BCM boost converter. Although feedforward control works well at reducing the line-current distortion of BCM boost converters, it is limited by the accuracy of the feedforward algorithms and is unable to reduce the line-current distortion associated with the input filter capacitor. These shortcomings can be overcome by using a current-feedback control loop to reduce the line-current distortion, at the expensive of a more costly microcontroller.

1.3 Thesis Structure

This thesis is divided into 5 chapters. Chapter 1 is the introductory chapter and it gives a short summary of the motivation and objectives of the research undertaken. The use of modular configurable power supplies in the growing field of medical equipment is discussed, where it is shown that the PFC stage is a major part of the modular configurable power supply. A review of the true definition of power factor for sinusoidal and non-sinusoidal waveshapes is given, the advantages of having a high power factor are presented, and the standards on input-current harmonics for electronic equipment are discussed. The fundamental operation of the boost converter is presented, including a description of its operation in CCM, BCM and DCM. The use of a boost converter as a PFC rectifier when operating in BCM and CCM is discussed. The multi-channel BCM boost topology is introduced and the advantages of interleaving several boost-converter channels together are explained. The advantages of using digital control are explored.

Chapter 2 discusses the design of the voltage compensator for a constant-on-time-control (COTC) control scheme. The voltage compensator has two main functions: to ensure fast output voltage regulation is achieved, and to maintain a high input power factor. A complete small-signal analysis is carried out to determine how changes in the on-time of the boost converter's switches affects the output voltage. The small-signal analysis is used to derive the recursive feedback algorithms implemented in microcontroller software using a fixed-point implementation. The performance of the voltage compensator is improved by adding a notch filter to filter out the 2^{nd}-harmonic ripple which affects all PFC stages. The notch filter is designed to change its coefficients depending on the line frequency of the ac mains, so that it works correctly in a range of line frequencies. The performance of the voltage compensator is further improved by introducing an adaptive gain to improve the voltage compensator's bandwidth at low levels of line voltage. The firmware design of the prototype converter is presented with details of the power-stage interface with the microcontroller, and the microcontroller's software flow. The proposed control scheme is experimentally validated on a 3-channel 1 kW prototype BCM boost converter.

Chapter 3 presents the design of a digital closed-loop scheme which maintains the correct phase-shift between each boost-converter channel. The advantages of using closed-loop feedback to control the phase-shift between each converter channel, versus using open-loop or feedforward methods, are discussed. The main advantage of a closed-loop scheme is that each boost-converter channel always uses its own ZCD circuit to trigger the boost switch's turn-on instant, thus ensuring BCM operation with valley switching is always guaranteed. A brief description of the converter's valley switching behaviour is given, showing how it reduces the converter's switching losses. A computationally-inexpensive closed-loop feedback system is derived to control the phase shift between the different boost converter

channels. The method is designed to be computationally inexpensive by implementing the control scheme with fixed-point math, having simple feedback control laws, and by executing the feedback algorithms at a fixed sampling frequency, thus ensuring the proposed method can be used on a low-cost microcontroller. Stability analysis of the proposed control scheme is performed, and a firmware implementation is discussed. The performance of the proposed control scheme is verified on a 3-channel 1 kW prototype BCM boost converter.

Chapter 4 presents the design of a simple digital variable-on-time feedforward algorithm to reduce the line-current zero-crossing distortion associated with the BCM boost converter. In this chapter, a detailed review is provided for how the valley switching behaviour and the current drawn by the input filter capacitor create the line-current distortion. The valley-switching analysis is used to derive a simple feedfoward algorithm which calculates the additional on-time needed to cancel the line-current-distortion effects of the converter. As a result, the converter now operates with a variable on-time over each line cycle, instead of a near-constant on-time over each line cycle. The additional on-time is calculated as a function of the input voltage only. Hence only a single look-up table (LUT) is required for implementation. The performance of the proposed control scheme is verified on a 3-channel 1 kW prototype BCM boost converter and compared to using COTC alone.

Chapter 5 discusses implementing an average-current-mode control (ACMC) scheme design to remove the line-current distortion of the BCM boost converter. A brief comparison of COTC, variable-on-time feedforward control, and ACMC is presented, where it is explained that COTC does not reduce the zero-crossing distortion of the BCM boost converter. Variable-on-time feedforward control can significantly reduce the line-current distortion but has some limitations. ACMC can overcome these limitations and reduce the line-current distortion further. A current-compensator design is carried out based on the converter's current-loop small-signal analysis. An adaptive gain is introduced into the design of the current compensator of the ACMC scheme to ensure the compensator has a fast bandwidth for all input voltages. The novel digital control scheme is combined with the variable-on-time feedforward control scheme to further improve the power quality. The control scheme is compared to a COTC scheme, a variable-on-time feedforward control, an ACMC scheme, and an ACMC scheme with feedforward control. Experimental results are demonstrated on a 2-channel 600 W prototype converter showing the proposed ACMC combined with FF control provides the best result in terms of improved power factor, but it comes at the cost of requiring a more expensive microcontroller to implement.

Chapter 6 presents the conclusions of the research of each chapter.

1.4 Power-Factor Correction

Most modern electrical loads are dc loads. For example, the charging of a battery of a plug-in hybrid or electric car requires a regulated dc current [9]. Other common examples are light-emitting diodes (LEDs), fluorescent lamps, laptops, computers, TVs, smart phones, all requiring regulated dc voltages or currents. Medical equipment contains different dc loads such as lasers, liquid-crystal-display (LCD) screens and powerful microprocessors etc. However, our electrical grid transfers energy using ac voltages. Therefore, to power these dc loads from the grid, an ac-dc PFC power supply is typically used. Power-factor correction is a method by which power supplies shape the input line current drawn by the power supply to have the same shape as the ac mains voltage [10]. This is done primarily to increase the real power that can be drawn from the grid, but it also must be done to meet applicable standards, e.g. EN61000-3-2, limiting the allowable input current harmonics that ubiquitous electronic equipment can draw from the mains.

1.4.1 Power Factor

Power factor is defined as the ratio of real power P to apparent power S and can be calculated as

$$PF = \frac{real\ power}{apparent\ power} = \frac{P}{S} \tag{1.1}$$

The real power drawn by a power supply is given by the average value of the instantaneous input power. The instantaneous input power $p(t)$ is calculated as the product of the line voltage $v_{line}(t)$ and the line current $i_{line}(t)$ as follows

$$p(t) = v_{line}(t) i_{line}(t) \tag{1.2}$$

The line voltage can be approximated as a sinusoidal waveform. The voltage level and frequency of the line voltage delivered to domestic users differs from country to country. Here in Ireland, for instance, the domestic supply is delivered to homes at an rms (root-mean-squared) voltage of 230 V and a line frequency of 50 Hz. Most other European countries, including France, Britain, Belgium, Germany and Italy, use the same level and frequency. The same is true for Australia and New Zealand. In the United States and in Canada, the grid is supplied to housholds at a rms voltage of 120 V and a line frequency of 60 Hz. In Japan, the mains voltage is supplied at 100 V and at line frequency of either 60 Hz or 50 Hz, depending on which part of the country you are in. As a result of the variation, ac-dc power supplies are typically rated to operate at a universal-line voltage range of 80 V to 265 V and a line frequency of 47 Hz to 63 Hz. Sometimes power supplies are rated to operate at line frequencies up to 400 Hz, as this frequency is commonly used on ships and in aircraft applications.

The real power delivered from the mains P is the average power, which for periodic waveforms can be calculated by integrating the instantaneous power over a full line period T_{line}, as shown in (1.3).

$$P = \frac{1}{T_{line}} \int_0^{T_{line}} p(t)dt = \frac{1}{T_{line}} \int_0^{T_{line}} v_{line}(t) i_{line}(t)dt \tag{1.3}$$

The apparent power on the other hand, is defined in (1.4) as the product of the rms value of the line voltage and line current.

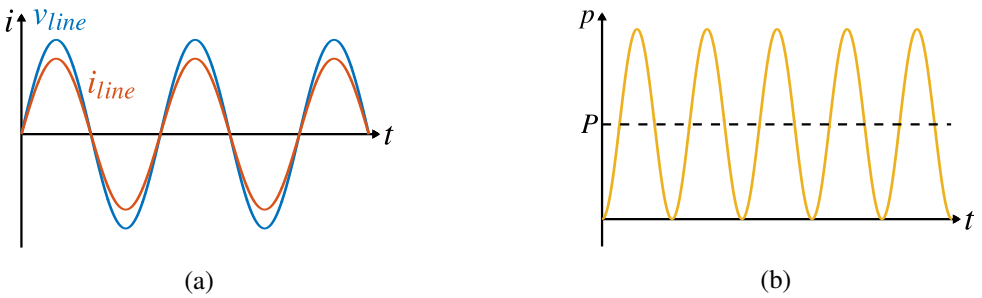
$$S = V_{line} I_{line} \tag{1.4}$$

where the rms value of the line voltage and line current are denoted V_{line} and I_{line}, and are defined by (1.5) and (1.6) respectively.

$$V_{line} = \sqrt{\frac{1}{T_{line}} \int_0^{T_{line}} v_{line}(t)^2 dt} \tag{1.5}$$

$$I_{line} = \sqrt{\frac{1}{T_{line}} \int_0^{T_{line}} i_{line}(t)^2 dt} \tag{1.6}$$

If the line voltage and line current are both pure sinusoidal waveforms given by $v_{line} = \sqrt{2} V_{line} sin(2\pi f_{line} t)$ and $i_{line} = \sqrt{2} I_{line} sin(2\pi f_{line} t)$, and f_{line} is the line frequency, then the input power and apparent power are equal and the power factor is unity. The shapes of the line voltage and line current in this scenario are shown in Figure 1.4. The instantaneous power for this case, is depicted in Figure 1.4(b). The instantaneous power has a frequency twice that of the line voltage and line current. This case can occur if an ac source is connected to a resistive load such as a heating element or incandescent light bulb.

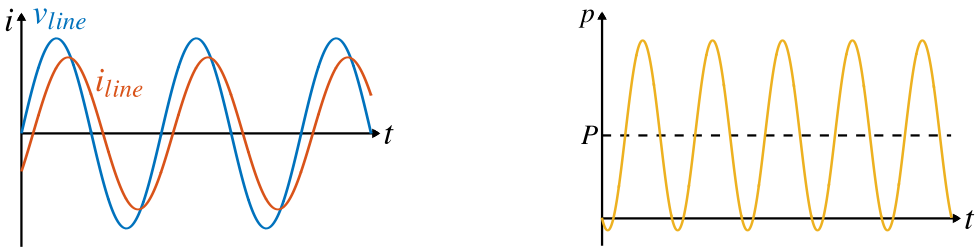


(a) (b)

Figure 1.4. Waveshapes of line voltage and line current assuming purely sinusoidal waveforms with $PF = 1$.

If a phase shift ϕ is introduced between the voltage and the current, such that the line current now equals $\sqrt{2} I_{line} sin(2\pi f_{line} t - \phi)$, as shown in Figure 1.5(a), the power factor becomes less than unity. The phase-shift ϕ causes the instantaneous power to become negative at times, as shown in Figure 1.5(b). As a result the average power P is reduced. A common example of the waveshapes displayed in Figure 1.5 corresponds to when an ac

source is used to power an inductive load such as a motor.



(a) (b)

Figure 1.5. Waveshapes of line voltage and current assuming purely sinusoidal waveforms when $\phi = 30^\circ$ and $PF = 0.866$.

For the cases depicted in Figure 1.4 and Figure 1.5, the instantaneous power can be determined as follows

$$\begin{aligned} p(t) &= v_{line}(t) i_{line}(t) \\ &= \sqrt{2} V_{line} \sin(2\pi f_{line} t) \times \sqrt{2} I_{line} \sin(2\pi f_{line} t - \phi) \\ &= V_{line} I_{line} (\cos\phi - \cos(4\pi f_{line} t - \phi)) \end{aligned} \tag{1.7}$$

It is clear from (1.7) that the instantaneous power is composed of a constant term given by $V_{line} I_{line} \cos\phi$, and a time-varying sinusoidal term given by $-V_{line} I_{line} \cos(4\pi f_{line} t - \phi)$. As the mean value of a sinusoidal signal is zero. The average power is given by $P = V_{line} I_{line} \cos\phi$. Therefore, the power factor can be calculated as

$$PF = \frac{P}{S} = \frac{V_{line} I_{line} \cos\phi}{V_{line} I_{line}} = \cos\phi \tag{1.8}$$

This is a common equation for PF given in many text books. However, it only applies to the case when both v_{line} and i_{line} are pure sinusoidal waveforms with the same fundamental frequency.

An example of when (1.8) can not be used to calculate the power factor is given in Figure 1.6. In this example the line current is in phase with the line voltage such that $\phi = 0$. However, the line current now has significant zero-crossing distortion and is not a perfect sinusoid. In this case the power factor is calculated using (1.1). These waveshapes will be re-visitedlater on in this thesis when the zero-crossing distortion in the line current drawn by BCM boost converters is discussed.

1.4.2 Advantages of Power-Factor Correction

There are several advantages to using a power supply with active power-factor correction. The main advantage is that the rms line current drawn from the ac mains is reduced. Reduced currents in the ac distribution system are beneficial as they result in less resistive power

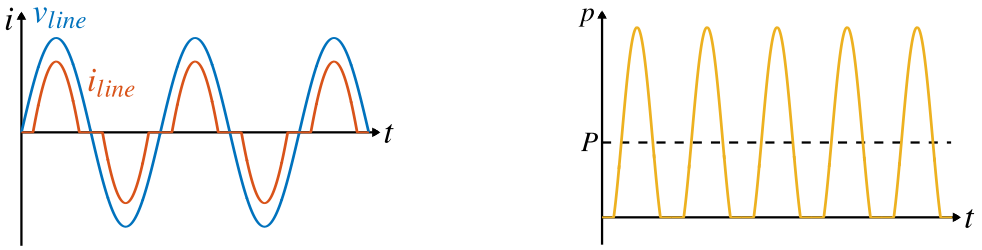


Figure 1.6. Waveshapes of line voltage and current with $\phi = 0°$ and $PF = 0.94$.

losses in conductors. Moreover, the maximum power that can be sourced from the supply is increased as, it's current limited.

Figure 1.7 shows the typical architecture of a switched-mode power supply with no PFC stage. It consists of a full-bridge rectifier followed by a large electrolytic capacitor connected to an isolated dc-dc converter. The full-bridge rectifier and electrolytic capacitor peak rectify the input ac voltage. When the line voltage is greater than the voltage across the electrolytic capacitor, denoted v_{bus}, the line current can flow to charge the capacitor and transfer power to the isolated dc-dc converter. When the line voltage drops lower than v_{bus}, no line current flows and the electrolytic capacitor powers the isolated dc-dc converter. As a result, the line current has large periodic peaks and poor power factor. The line current also contains many current harmonics at multiples of the line current frequency. The unwanted higher-order harmonics create power losses through the mains distribution system, particularly in transformers.

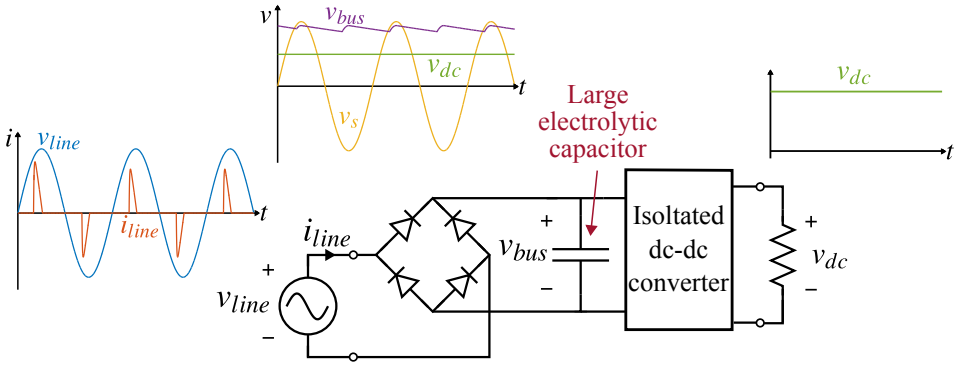


Figure 1.7. An ac-dc power supply with no PFC stage.

Another disadvantage of the poor power factor is that the distorted line current waveform can also distort the line voltage. This can result in interference with other equipment and reliability issues. Furthermore, commercial and industrial customers of the power utility can be financially penalized for demanding currents with a low power factor.

An example of a power supply which uses active PFC is shown in Figure 1.8. It consists of a full-bridge rectifier followed by a boost converter. The output capacitor of the boost converter is a large electrolytic capacitor used for energy storage. The boost converter is controlled so that the input current it draws has the same shape as its input voltage.

This results in a near-unity power factor, typically greater than 0.98 at full power for most commercial power supplies. The output voltage of the boost converter must always be greater than the input voltage. Since the universal rms line voltage range is 85 to 265 V, the output voltage of the boost converter must be greater than the peak of a rms line voltage of 265 V, which is 375 V. Typically, the output is set to 380 V to 400 V. The large regulated dc voltage at the input to the isolated dc-dc converter gives a power supply with PFC another advantage, compared to the power supply with no PFC in Figure 1.7, where for a universal input voltage range, the voltage at the input to the isolated dc-dc supply varies from 120 V to 375 V. The higher voltage generated by the PFC stage results in lower current stress, better efficiency and smaller size for the design of the isolated dc-dc converter. Furthermore the higher voltage allows for a reduction in the size of the large electrolytic capacitor and better hold-up time under all line voltages.

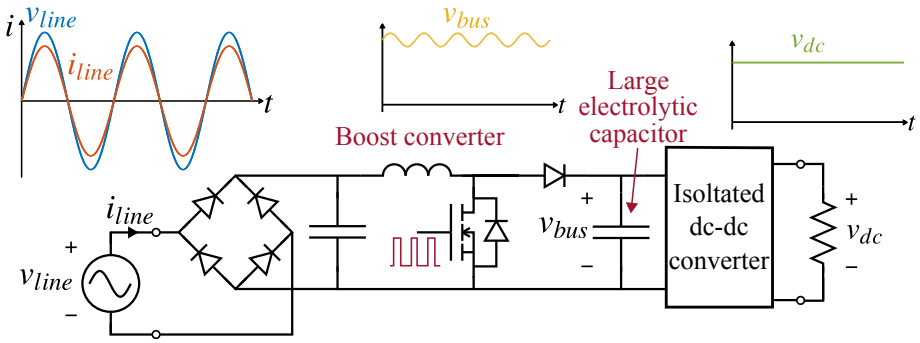


Figure 1.8. An ac-dc power supply consisting of a full-bridge rectifier and flyback converter.

1.4.3 Input Current Harmonic Standards

IEC 1000-3-2 is a standard limiting the amount of harmonic currents drawn by electronic equipment drawing up to 16 A and connected into the public supply system. It was first published in 1995 by the International Electrotechnical Commission (IEC). The European Committee for Electrotechnical Standardization (CENELEC) published the EN 61000-3-2 standard in the same year based on the IEC 1000-3-2 recommended standard. The EN 61000-3-2 standard is part of the European 'EMC-directive', which must be complied with for the purpose of CE marking, as of 2001 [11].

The standard divides electronic equipment into 4 separate classes, denoted Class A, B, C and D. Each class has its own harmonic limits. Class B applies to portable tools and arc welding equipment greater than or equal to 75 W. Class C applies to all lighting equipment greater than or equal to 25 W, as well as to discharge fluorescent lamps less than or equal to 25 W. Class D applies to personal computers, monitors and TVs. Lastly, Class A applies to all other appliances greater than 75 W.

The Class A harmonic limits are shown in Figure 1.9. They are used as a current harmonic metric throughout this thesis. They are measured at an rms voltage of 230 V and a line

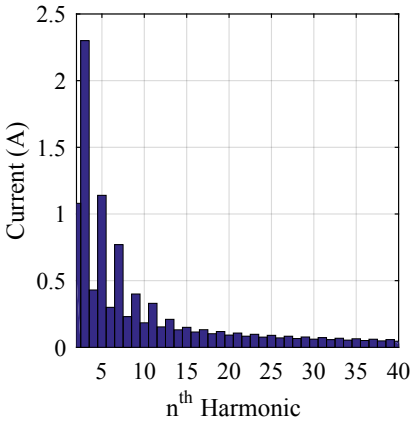


Figure 1.9. Class A input current harmonic limits.

frequency of 50 Hz at the maximum rated power of the power supply.

1.5 Boost Converter Fundamentals

The combination of a bridge rectifier and boost converter is a widely-used topology for PFC front ends. This circuit topology is shown in Figure 1.10. The boost converter switch Q, which is typically a power MOSFET, is toggled on and off by applying a pulse-width-modulation (PWM) signal to its gate-source terminals, in order to simultaneously control the inductor current i_L and the output voltage v_o.

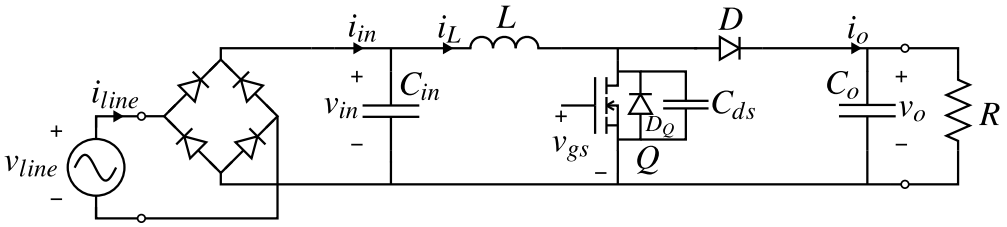


Figure 1.10. A single-channel boost converter used as a pfc rectifier.

There are three different operational modes for the boost converter. The waveshapes of the inductor current i_L and gate-source voltage of the boost converter switch v_{gs} are shown in Figure 1.11 for the three different modes. The modes are continuous-conduction mode (CCM), as shown in Figure 1.11(a), boundary-conduction mode (BCM), as shown in Figure 1.11(b) and discontinous-conduction mode (DCM), as shown in Figure 1.11(c). The BCM is sometimes referred to as the critical-conduction mode (CrCM) or the transition mode.

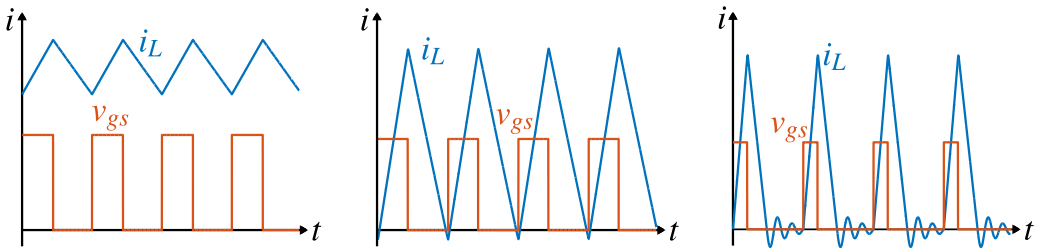


Figure 1.11. Waveshapes of inductor current for CCM, BCM and DCM.

In CCM the inductor current never reaches zero and is therefore continuous. This mode of operation has the advantage of low peak-peak inductor current ripple and a powdered iron core is typically used as the boost inductor. The powdered iron core has better power density than a ferrite core, but is unsuitable for many applications with large inductor current ripple due to increased core loss. CCM operation also has low rms current stress in the boost switch and diode. However, this mode has the disadvantage that both the MOSFET turn on and turn off occur when there is significant current flowing through the switch, and a voltage of v_o across the MOSFET's drain-source voltage v_{ds}. As a result, both the MOSFET turn-on and turn-off instances are hard-switching events. Thus, CCM operation suffers from significant switching losses. The switching losses are more severe if the boost diode has

poor reverse recovery performance [12], [13]. If a diode is in the forward conducting state, and then is immediately switched to the reverse condition, the diode has stored charge that must be discharged before the diode enters a non-conducting state. This effect causes the diode to conduct a reverse current at the moment it is turned off, which is commonly known as the reverse-recovery current. The reverse-recovery charge of silicon (Si) power diodes is substantial, and it is common for CCM boost converters to use more expensive silicon carbide diodes (SiC), as they have very little reverse recovery charge.

In BCM the switch is turned on when the inductor current has reached zero, therefore the diode does not conduct a reverse-recovery current, and cheaper Si diodes can be used without increasing the switching loss. On the other hand, BCM operation suffers from higher peak-peak inductor current ripple compared to CCM operation. Ferrite inductors are typically used for the boost inductor as they can handle the large magnetic flux swing associated with the large current ripple, without excessive core loss. Ferrite inductors are cheaper than a powdered iron alternative, but are also larger. The rms current of the switch and diode are also higher in BCM operation, which increases conduction losses. However, BCM has the advantage that the switch turn-on occurs when the inductor current is zero, resulting in lower switching losses of the BCM converter compared to the CCM converter. Furthermore, the BCM converter can operate with zero-voltage switching and near-zero-voltage switching during the turn-on instant of the switch. The BCM topology operates with variable switching frequency. The variable switching frequency can be beneficial in terms of electromagnetic interference (EMI), as it creates a natural dithering, reducing the differential-mode (DM) and common-mode (CM) EMI generated by the converter. The downside of the variable switching frequency is that the switching frequency can become excessively high at no load, and the switching frequency variation can become too large for higher power designs, making magnetics design much more challenging.

In DCM the the inductor current is allowed to become zero before the switch is turned on. In this mode there is a region after the inductor current reaches zero where the switch remains off, and the MOSFET drain-source capacitance C_{ds} and the boost inductor resonate with each other. DCM operation suffers from larger peak-to-peak inductor current ripple, greater than that of BCM and CCM. Similar to BCM, a ferrite inductor is typically used to avoid excessive core loss. The DCM mode of operation suffers the highest rms switch and diode currents compared to BCM and CCM at the same power level. In DCM the MOSFET turns on with zero-current switching, therefore the switching loss is lower than that of CCM. An advantage of the DCM operation is that it can be designed to operate at a fixed switching frequency. This makes the design of magnetic components and the EMI filter simpler. The main drawback of the DCM converter is the high rms current stress, which limits the power of this topology to low power PFC applications.

1.5.1 BCM Boost Converter as a PFC Rectifier

The single-channel BCM boost converter is a popular topology for PFC applications at power levels below 300 W [14]–[36]. This is due to advantages of simple control structure, zero-current turn off of the boost diode and low switching losses. At higher power levels the higher rms currents lower efficiency and degrade the performance of this topology. The higher input current ripple also increases the size of the required input DM EMI filter [37], [38].

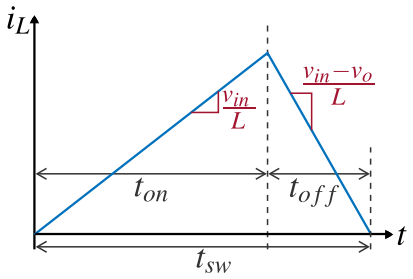


Figure 1.12. A single switching cycle of the inductor current assuming negligible resonant period.

Figure 1.12 shows how the inductor current waveform looks over a single switching cycle if the resonance between the boost inductor and MOSFET drain-source capacitor is ignored. The average input current drawn by the converter can be calculated as half of the peak inductor voltage, such that

$$i_{in} = \frac{1}{2}\frac{v_{in}t_{on}}{L} \tag{1.9}$$

where $i_{L(pk)}$ is the peak inductor voltage, v_{in} is the input voltage to the boost converter and t_{on} is the on-time of the switch. If the on-time t_{on} is constant, the input current i_{in} equals a constant number times v_{in}. Therefore, the BCM boost topology can achieve unity power factor if the on-time remains constant and the resonance between L and C_{ds} is negligible.

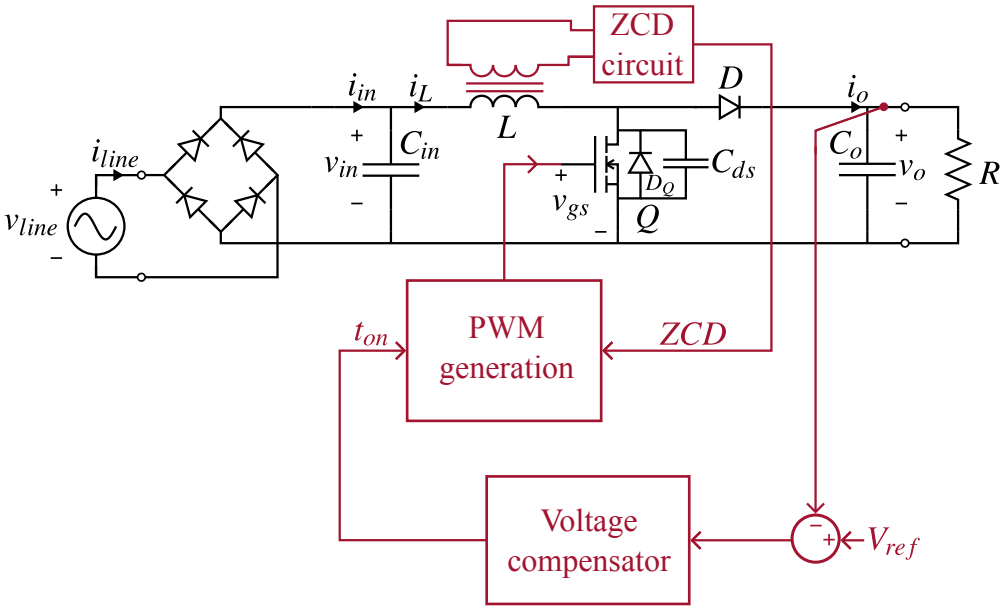


Figure 1.13. A COTC scheme for a single-channel BCM boost converter.

This is the basis of constant-on-time control (COTC) [39]. COTC is a control method whereby the on-time of the switch is kept relatively constant over each line cycle of the ac mains voltage, so that the BCM topology draws a near-unity power factor. The on-time is varied slowly to control the output voltage of the boost converter at a regulated dc value. This is done by using a single voltage compensator with a slow bandwidth, typically 10 to 20 Hz, to calculate the required on-time of the converter.

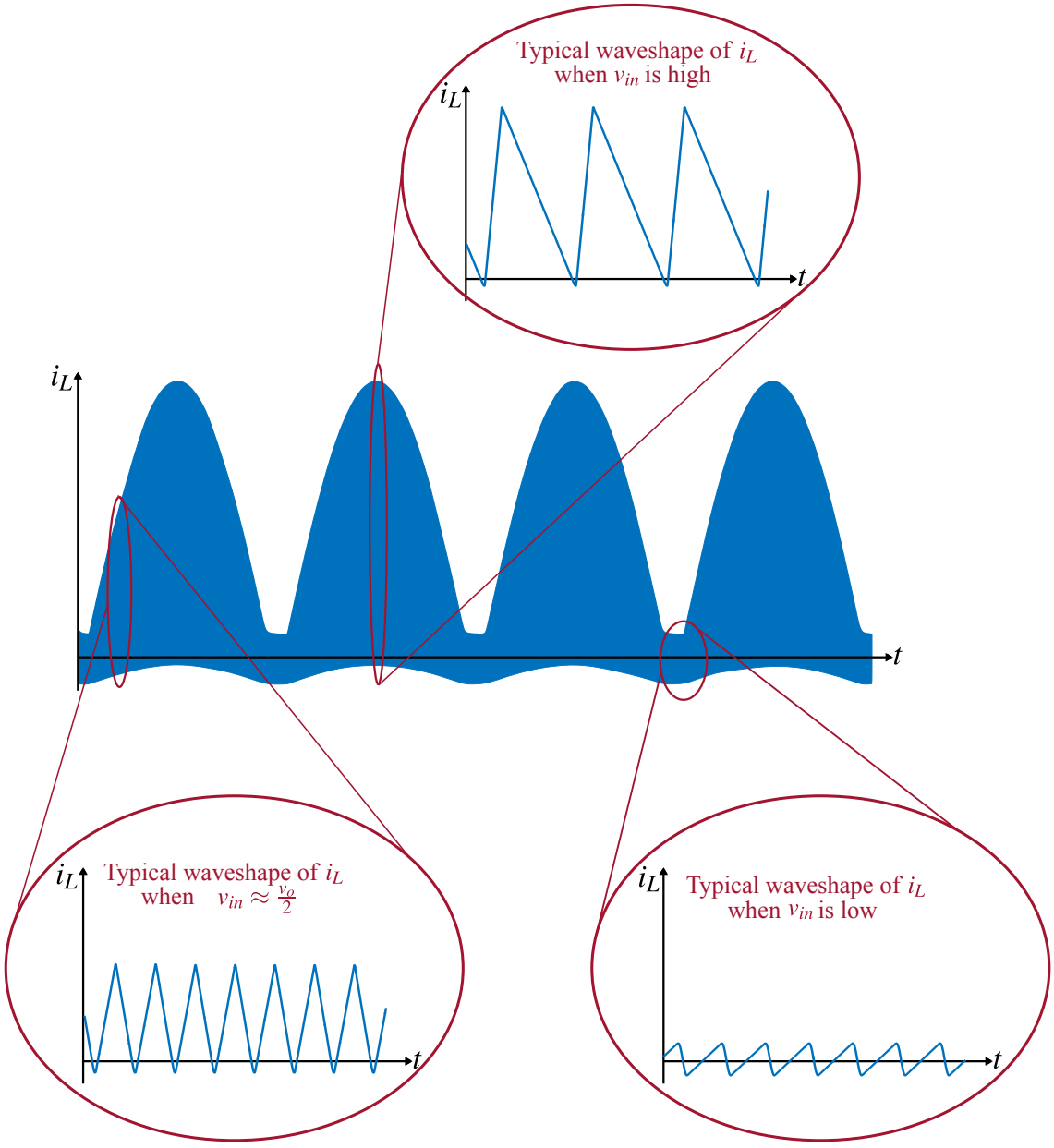


Figure 1.14. Typical boost inductor waveshape of a BCM boost converter over two line cycles.

Figure 1.13 shows a simplified block diagram of how a COTC scheme works. The output voltage is sensed and compared to a reference V_{ref} to create an error signal. The voltage compensator uses the error to calculate the switch on-time. The on-time is used by the PWM generation circuitry to determine when the MOSFET is turned off. The turn-on instant of the MOSFET occurs when the inductor current reaches zero. This is achieved by using an

auxiliary winding on the boost inductor and a zero-current detection (ZCD) circuit.

The typical waveshape of the inductor current over two line cycles of the mains voltage, when a COTC is used, is shown in Figure 1.14. The resonance between C_{ds} and L creates a slightly negative inductor current before the turn-on instant of the MOSFET. This is why the inductor current envelope is slightly negative over the entirety of the two line cycles. The on-time of the switch is almost constant over the 2 line cycles, however the off-time changes dramatically. When the voltage v_{in} is high, the off-time is large, therefore the switching frequency is low. As v_{in} gets lower the off-time reduces and the switching frequency becomes higher. This creates a natural variation of the switching frequency over each line cycle. During the zero-crossings of the line voltage the inductor current has a near-zero value due to the negative current created by the resonance between C_{ds} and L. This effect creates a region around the zero crossings of the line voltage where no current flows through the bridge rectifier. This effect is known as zero-crossing distortion, and it results in the BCM topology having a power factor less than 1. We will revisit this distortion and how to reduce it using digital control in later sections of this thesis.

1.5.2 CCM Boost Converter as a PFC Rectifier

The CCM boost converter is widely-used as a PFC rectifier in the power range of 200 W to 7.2 kW [40]–[55]. It is suited to the higher power levels due to its lower rms current stresses, and conduction losses compared to the BCM. The CCM boost converter is normally regulated using average-current-mode control (ACMC) [56], [57]. Although many other control schemes do exist such as peak-current-mode control [58], predictive control [43], [59], [60], hybrid control [44], [53], [61], modulated-carrier control [50], sliding-mode control [62], and non-linear-carrier control [63]. ACMC is the most commonly-adopted and well-known control scheme.

A simplified block diagram of a CCM boost converter using ACMC control is shown below in Figure 1.15

The ACMC scheme works by using an inner current compensator with a fast bandwidth, typically from 2 kHz to 10 kHz, to control the shape of the inductor current. The current compensator calculates the duty cycle of the PWM signal applied to the gate-source terminal of the MOSFET, so that it tracks a reference current signal denoted i_{ref}. The reference current signal has the same shape as the rectified input voltage. As a result, the input line current drawn by the converter has a near-unity power factor. The reference current is calculated by multiplying the sensed input voltage by the voltage compensator output v_c, and a constant scaling term denoted k. Similar to the BCM COTC scheme, the voltage compensator for the CCM ACMC scheme has a relatively slow bandwidth so that v_c is near constant over several line cycles. Thus, i_{in} has the same waveshape as v_{in}. The voltage compensator adjusts the level of v_c so that the output voltage of the boost converter tracks the reference v_{ref}. The

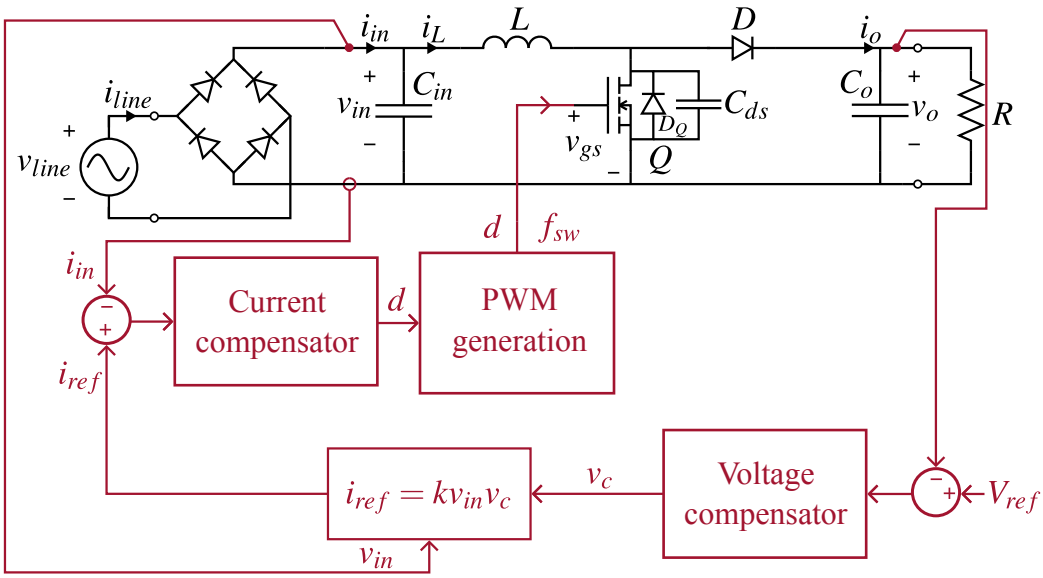


Figure 1.15. An ACMC scheme for a single-channel CCM boost converter.

typical waveshape of the inductor current and reference current over 2 line cycles for a CCM boost converter with ACMC is shown in Figure 1.16.

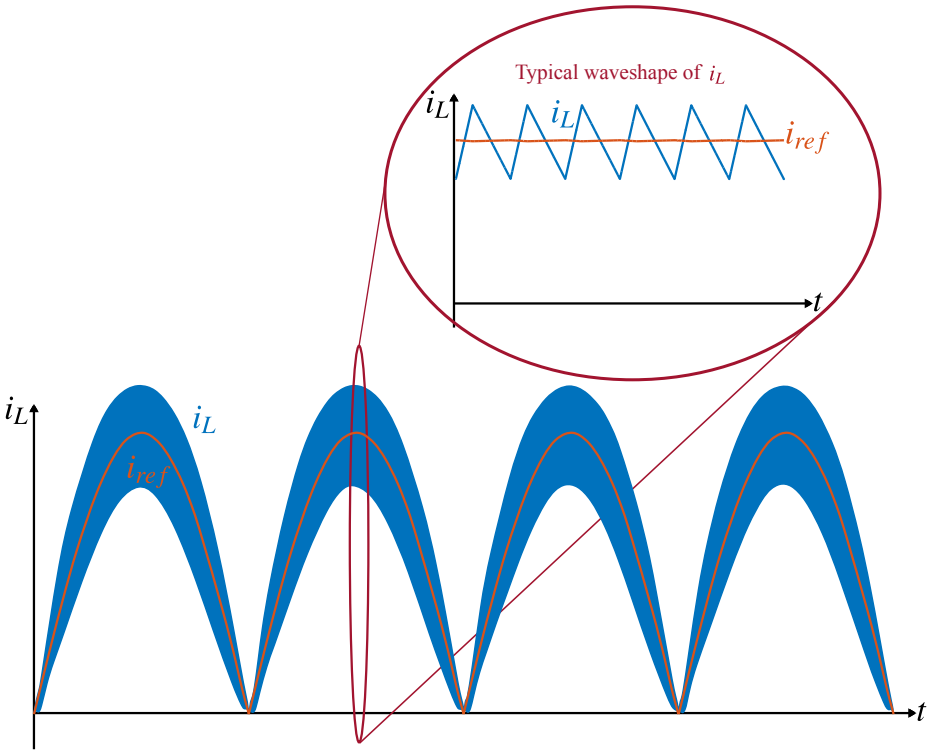


Figure 1.16. Typical boost inductor waveshape of an ACMC CCM boost converter over 2 line cycles.

For CCM boost converters using an ACMC control, the line current can become distorted by operating in DCM, which occurs near zero crossings of the line current and at light load. To overcome this, techniques such as duty-cycle feedforward control can be used [41], [64]. Furthermore, the ACMC control scheme can be applied to interleaved CCM boost converters, so long as additional active current sharing is applied to each channel of the interleaved

converter [65].

1.5.3 Multi-Channel BCM Boost Converter as a PFC Rectifier

Interleaving several BCM boost converter channels to create a multi-channel BCM boost converter has several advantages that allows the topology to become more suited to higher power applications. The 2-channel BCM boost topology is commonly used up to 600 W [66]–[75]. The 3-channel BCM boost topology is more rarely adopted but is typically used at power levels to 1 kW [76]–[78]. The topology for a multi-channel boost converter, with a total of N channel is shown in Figure 1.17.

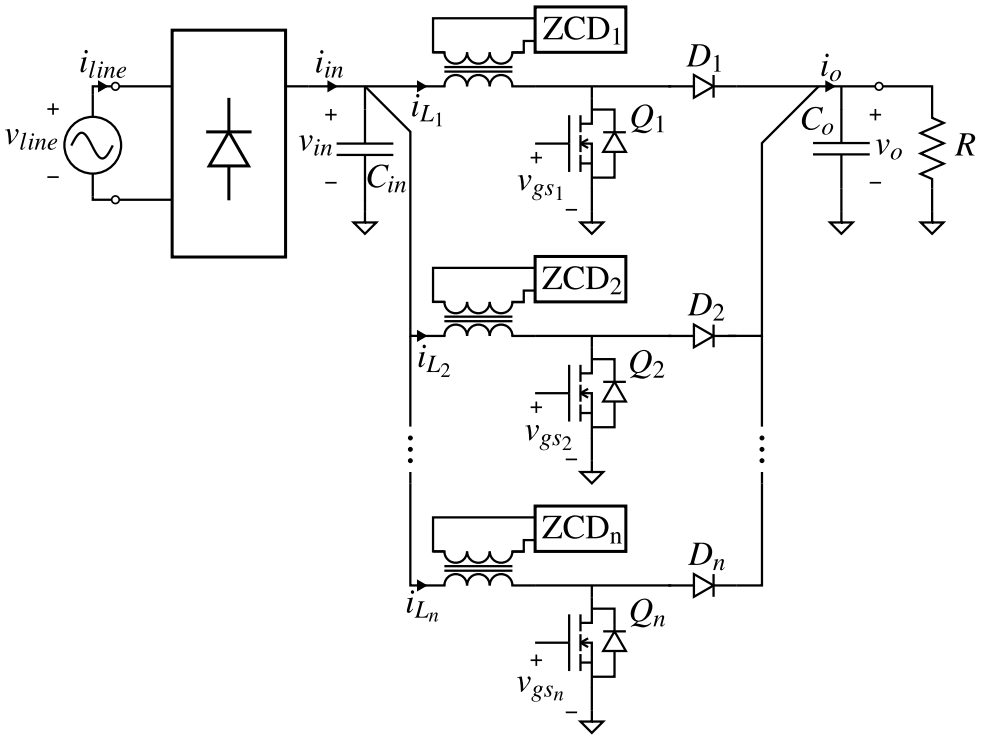


Figure 1.17. A multi-channel BCM boost converter used as a PFC rectifier.

The main advantage is that the peak-to-peak input current ripple is dramatically reduced. This reduction in the input current ripple is shown in Figure 1.18 for a 2-channel BCM boost converter and in Figure 1.19 for a 3-channel BCM boost converter. Moreover, the effective switching frequency of the ripple component of the input current becomes twice the switching frequency for the 2-channel converter, and 3 times the switching frequency for the 3-channel converter. The combination of the lower peak-to-peak input current ripple, and the multiplication of the effective switching frequency dramatically reduces the size of the required DM EMI filter.

A similar effect is seen when looking at the output current from the multi-channel boost converter. Figure 1.20 shows the shape of the output current over a full line cycle for a 2-channel BCM boost converter. The effective switching frequency of the output current is twice that of the switching frequency. This reduces the high frequency ripple on the output

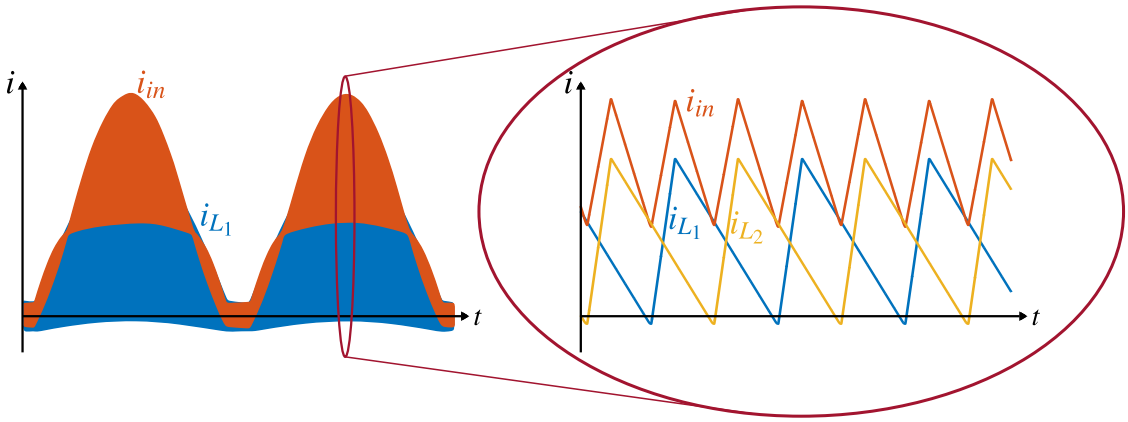


Figure 1.18. Inductor current of a 2-channel converter.

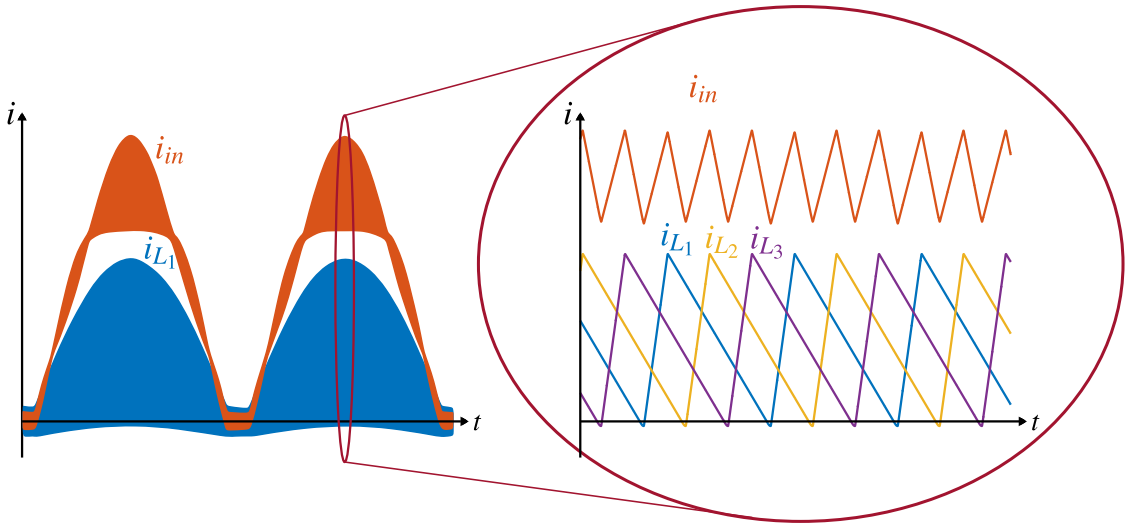


Figure 1.19. Inductor current of a 3-channel converter.

of the converter. Furthermore, since the peak-to-peak current ripple of the output current is reduced, the rms current that flows into the output electrolytic capacitor is reduced. As a result, there is less power loss from the capacitor equivalent-series resistance (ESR) and its lifetime is increased.

Figure 1.21 demonstrates the shape of the output current for a 3-channel BCM boost converter. With 3 channels the effective switching frequency is 3 times the switching frequency and the rms current seen by the output capacitor is even further reduced.

Another advantage of the multi-channel BCM boost converter is that its switching frequency variation is reduced by turning off some channels at lighter loads. This is known as phase shedding. Phase shedding under lighter loads has other added advantages, such as improved power factor and higher efficiency with load variation.

Despite the high number of components, the multi-channel topology has a lower cost compared to using other circuits for PFC applications. The multi-channel topology only requires a total of N low-side gate drivers and no high-side gate drivers, which are more expensive to drive. Cheap small ferrite inductors can be used instead of powered iron cores.

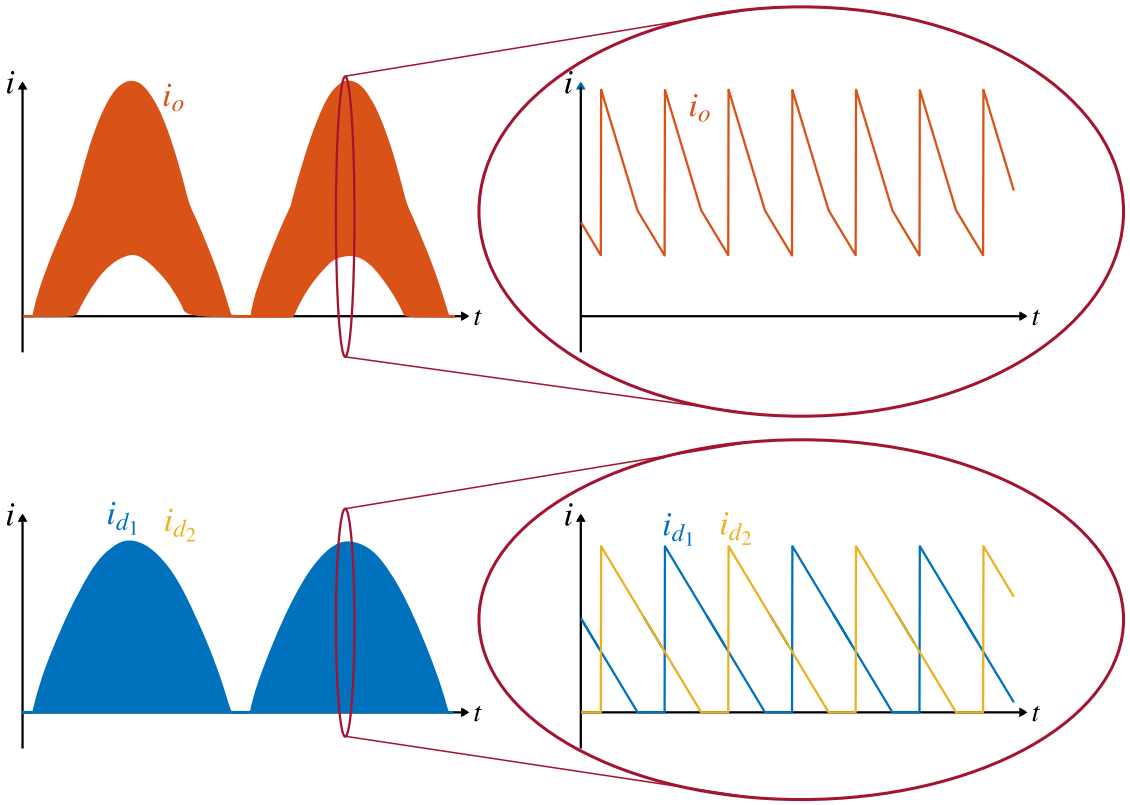


Figure 1.20. Output current of a 2-channel converter.

Although there are N switches and N diodes, each of the MOSFETs and diodes have lower current ratings. Moreover, as the BCM boost diode works with zero-current turn-off, the reverse recovery current of Si diodes does not incur extra switching losses in the boost MOSFET, and so the Si diodes are the preferred choice over more expensive SiC Schottky diodes.

One of the downsides of the multi-channel BCM topology is that the variable switching frequency makes the interleaving of different channels a challenging design task [22], [70], [72]–[74], [76]–[78]. As a result, the control scheme for the topology must also incorporate a phase-shift control scheme to maintain the correct phase shift between channels, and also to have the ability to reduce the number of channels operating at lighter loads.

Although there are many commercially available analog PFC control integrated circuits (ICs) available on the market for 2-channel BCM boost converters, such as the FAN9611 [79], UCC28063 [80] and NCP1631 [81], there are currently no PFC control ICs for more than 2 channels. Using a digital microcontroller makes it possible to build an interleaved BCM boost converter with more than 2 channels, provided that the microcontroller has sufficient suitable peripherals for the number of channels.

This thesis describes the design and implement of different digital control schemes for multi-channel BCM boost PFC rectifiers. The control schemes are validated experimentally on a 600 W 2-channel and a 1 kW 3-channel BCM boost converter.

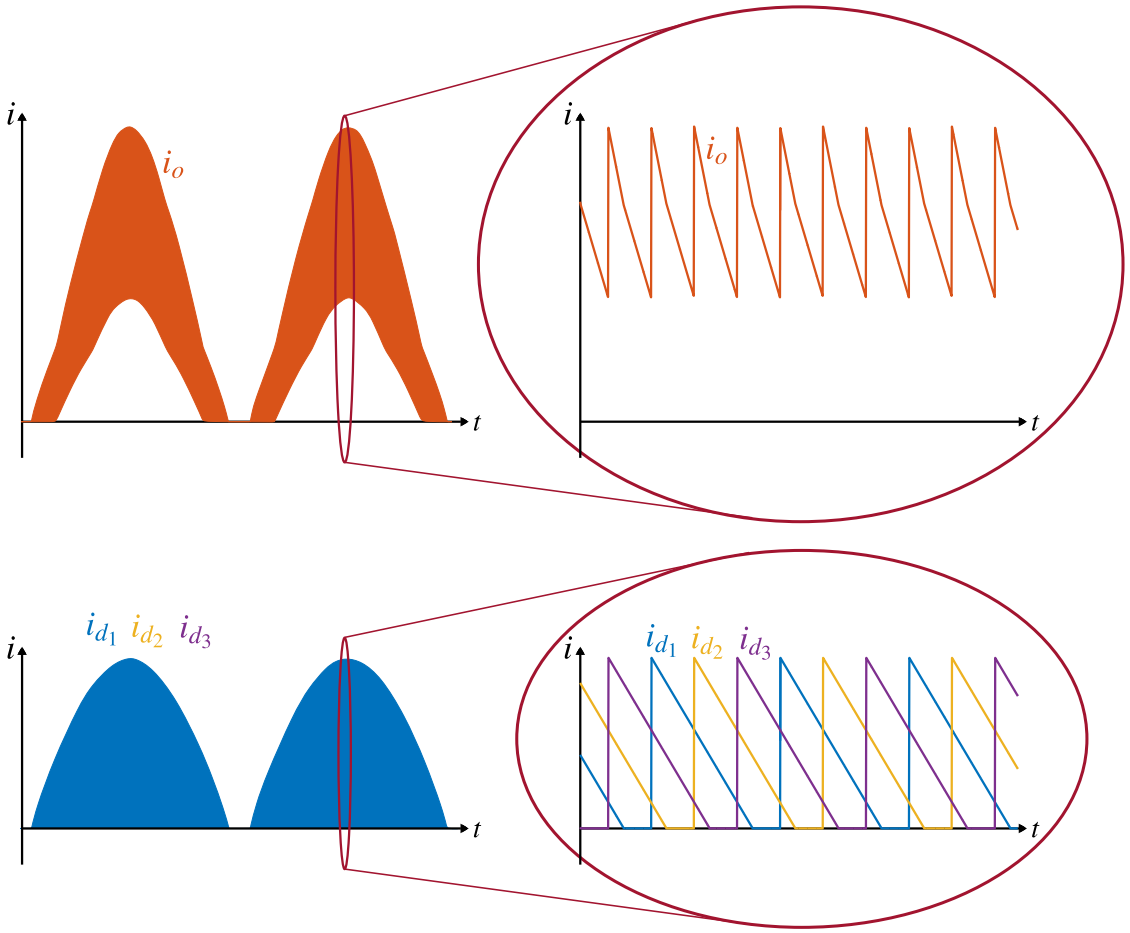


Figure 1.21. Output current of a 3-channel converter.

1.6 Digital Control

Recent decades have seen significant improvement in microcontroller technology, with better processing power, lower cost and improved peripherals dedicated to power electronics applications [82], [83]. There are many examples of digitally-controlled single-channel and interleaved BCM boost power supplies for PFC applications existing in the literature [17]–[19], [33], [35], [67], [76]–[78]. The adoption of digital control in power supplies has the potential to create performance improvements as well as design challenges. The following advantages of digital control over analog control have motivated the research carried out in this dissertation in the control of digital PFC rectifiers:

- **Adaptive control laws** - Adaptive control allows the coefficients and gain terms of compensators to be changed depending on the operating condition of the system. For instance, the output-voltage tracking performance of a BCM boost PFC rectifier can be improved by implementing an adaptive gain that increases at lower levels of operating input voltage [84]. Although such an example can also be implemented with an analog controller, it is much easier to design such a control law when using a digital-control scheme.

- **Cost Reduction** - If the price of a microcontroller is directly compared to that of an analog IC, for the function of controlling a ac-dc PFC converter, the microcontroller is typically slightly more expensive. However, using a microcontroller can reduce the total system costs by incorporating the function of several analog control ICs into a single chip. Typically a PFC rectifier is followed by an isolated dc-dc stage. The isolated dc-dc stage also requires an analog control IC to perform safety functions, control functions, and generate the PWM waveforms. As well as this, it is very common for a power supply to have a lower power microcontroller to perform communications functions, as well as some safety and house-keeping functions. Using a single more powerful microcontroller to implement the same functions of these 3 ICs lowers the total bill-of-materials (BOM) cost. Furthermore, given the recent trend of decreasing microcontroller cost, it is expected that the cost of microcontrollers suitable for use in SMPS will continue to drop into the future. A comparison of BOM costs for a PFC power supply designed with analog control versus digital control is done in [85] where it is shown digital control has significantly lower BOM costs.

- **Less Sensitivity** - Digital control is less sensitive to process variation, temperature variation and noise, compared to an analog feedback control scheme. This is because component tolerances of resistors and capacitors can effect the performance of analog feedback networks between power supplies with the same design. Similarly, resistor and capacitor values of components and silicon properties of op-amps used in analog feedback networks can change with temperature. In a digital control scheme, digital calculations are highly accurate as they have no direct dependencies with temperature or tolerance variations.

- **Improved Design** - Power-supply designers, who only use analog control, are limited by the circuit topology they can use, because the chosen circuit topology must have a dedicated control analog IC available on the market. On the other hand, if digital control is used, the same microcontroller can be used for a wide number of different topologies. Furthermore, additional safety functions can be added to a digital design such as over-voltage, over-temperature, over-power, and other warning signals. With analog control the designer is limited to the safety functions incorporated on the analog control IC.

- **Easier to implement Advanced Control Techniques** - Microcontrollers can multiply numbers easily, store large arrays of numbers in look-up tables, and easily perform logic operations, such as if statements and while loops. This allows microcontrollers to implement advanced control techniques more easily than analog control. Some examples are the digital notch filter used in [51] to improve the power factor of a PFC rectifer, the self-tuning digital comb filter designed for a CCM pfc rectifier in [52], and

the digital control law is used in [86] to enable a CCM boost PFC rectifier to operate with valley skipping when in DCM at light load.

In this thesis, we design and implement different digital control schemes for multi-channel BCM boost converters, which capitalize on the the advantages of digital control to improve power-supply performance where possible. The thesis is structures as follows, Chapter 2 focuses on regulating the output voltage of the converter. Chapter 3 discusses the use of phase-shift control to maintain proper interleaving between different boost converter channels. Chapter 4 explores using feedforward control to improve the input power quality of the converter. Chapter 5 discusses the use of average-current-mode control for BCM boost converters, and how it can be used to further improve the converter's input power quality. Lastly, Chapter 6 gives a conclusion to each chapter, and and outlines possible future work.

2 CONSTANT-ON-TIME CONTROL

The objective of this thesis is to develop a digital control scheme for a multi-channel BCM boost converter for PFC applications. As such, the first step in the process is to design a feedback network to regulate the converter's output voltage. This chapter focuses on the use of COTC to regulate the output voltage.

There are two main reasons as to why it is challenging to design a suitable feedback control scheme to regulate the output voltage of PFC boost rectifiers. The first is that the output voltage of the boost converter contains a 2^{nd} harmonic ripple component which is fed back into the control loop and distorts the waveshape of the input current, thus degrading the input power factor. The second reason is that the control feedback must ensure that the output voltage has a fast transient response for a wide input voltage range. In this work, an adaptive notch filter, is designed to work over a range of line frequencies to reduce the distortion caused by the 2^{nd} harmonic ripple. The gain of the control loop is also increased at low line voltages to ensure that the voltage compensator maintains a fast transient response for all line voltages.

The results of this chapter have been published in the following paper:

- R. T. Ryan, J. G. Hayes, R. Morrison and D. Hogan, "Digital control of an interleaved BCM boost PFC converter with fast transient response at low input voltage," *IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 257-264.

2.1 Introduction

Constant-on-time control (COTC) is normally used to regulate the output voltage of BCM boost converters. COTC is advantageous due to its simplicity. As shown in Figure 2.1, it only requires a single voltage compensator with a low bandwidth, thus making it a low-cost solution that is easy to implement.

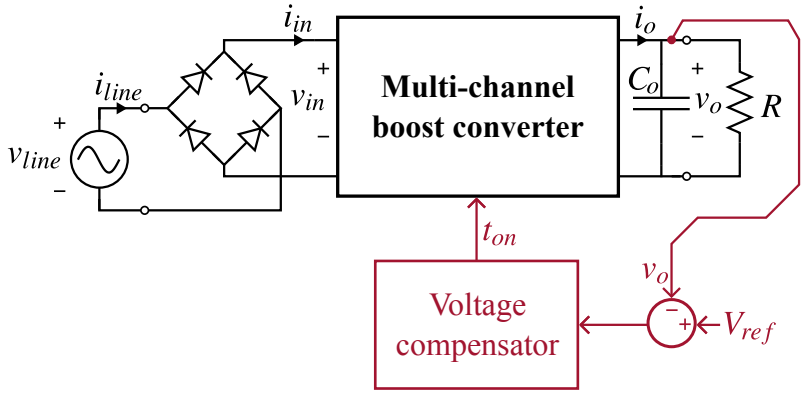


Figure 2.1. COTC scheme for a multi-channel BCM boost converter.

The voltage compensator has two functions. First, it must ensure that the output voltage v_o tracks a constant reference voltage V_{ref} with a fast dynamic response. Second, it must ensure that the on-time t_{on} is calculated such that the input current has a high power factor. A high power factor is important for the multiple reasons outlined earlier in Chapter 1, such as meeting current-harmonic regulations, sourcing maximum power, lowering the rms line current, etc. A fast dynamic response is important because it enables the converter to successfully track the reference voltage during output-load and line-voltage disturbances.

A slow output-voltage dynamic response can lead to large peak overshoots of the output voltage that may exceed the rated voltage of the electrolytic output capacitors, or, in more extreme cases, can cause damage to power semiconductors and other circuitry. Moreover, a slow dynamic response can lead to excessive peak undershoots of the output voltage. Peak undershoots can create increased current stress inside the downstream dc-dc converter, which typically acts as a constant-power load. Therefore, when the output voltage dips, the current drawn by the downstream converter increases. As a result, the downstream converter must be designed to handle substantial transients, which adds to the converter's cost. Severe undervoltages can also trigger the under-voltage-lockout (UVLO) or the over-current protections of the downstream converter, thus making the power supply less reliable.

Designing the voltage compensator to achieve both a fast dynamic response and a high input power factor is challenging. This is because the output voltage of a PFC converter has a significant 2nd harmonic voltage ripple. The voltage ripple can feed through the voltage compensator into its output and distort the line current drawn by the converter.

The 2nd harmonic ripple can be explained by looking at the time-averaged output current $i_{o(avg)}$ flowing into the output capacitor and load. Applying the power balance equation,

gives an expression for $i_{o(avg)}$

$$i_{o(avg)} = \frac{\eta v_{in} i_{in(avg)}}{v_o} \tag{2.1}$$

where η is the converter efficiency, v_{in} is the rectified input voltage, v_o is the output voltage and $i_{in(avg)}$ is the time-averaged rectified input current. If the input voltage and average input current are assumed to be ideal rectified sinusoids, and the output voltage is assumed to be a fixed dc value defined by V_o, the output current can be calculated by

$$\begin{aligned} i_{o(avg)} &= \frac{\eta V_{in(pk)} |\sin(\omega_L t)| I_{in(pk)} |\sin(\omega_L t)|}{V_o} \\ &= \frac{P_o}{V_o}(1 - \cos(2\omega_L t)) \end{aligned} \tag{2.2}$$

where $V_{in(pk)}$ is the peak input voltage, $I_{in(pk)}$ is the peak value of the average input current, ω_L is the angular line frequency and P_o is the converter's output power. The output current defined by (2.2) is comprised of two parts, a dc part with a magnitude P_o/V_o and a 2nd harmonic part with a magnitude of $P_o/V_o \cos(2\omega_L t)$. If the dc part is assumed to flow into the output load, and the 2nd harmonic part is assumed to flow into the large electrolytic output capacitor, then the instantaneous output voltage across the output capacitor can be calculated by integrating the current that flows into it, and adding an initial condition, as follows:

$$\begin{aligned} v_o &= \frac{1}{C_o} \int_{\tau=0}^{\tau=t} -\frac{P_o}{V_o} \cos(2\omega_L \tau) + V_o \\ &= V_o - \frac{1}{C_o} \frac{P_o}{V_o} \frac{1}{2\omega_L} \sin(2\omega_L t) \end{aligned} \tag{2.3}$$

Therefore, the output voltage contains a voltage ripple with a frequency twice that of the line frequency. Figure 2.2 shows the typical waveshapes of v_{in}, $i_{in(avg)}$, $i_{o(avg)}$ and v_o for a single-channel BCM boost converter during steady-state operating conditions, demonstrating how the 2nd harmonic ripple is created on the output.

The voltage compensator must heavily attenuate at the 2nd harmonic ripple to achieve a good power factor. This can be achieved by using a voltage compensator with a low bandwidth, typically in the range of 7 Hz to 15 Hz. The downside to using a voltage compensator with a low bandwidth is that the output voltage has a poor transient response.

The design of the voltage compensator is made more complicated by the non-linearity of the converter's system model, and the wide range of different operating conditions for a universal-line input. For instance, the voltage compensator must provide good performance at any rms line voltage in the range of 85 V to 265 V, at any line frequency in the range 48 Hz to 62 Hz, and at any power level from no load to rated power. Furthermore, it must be

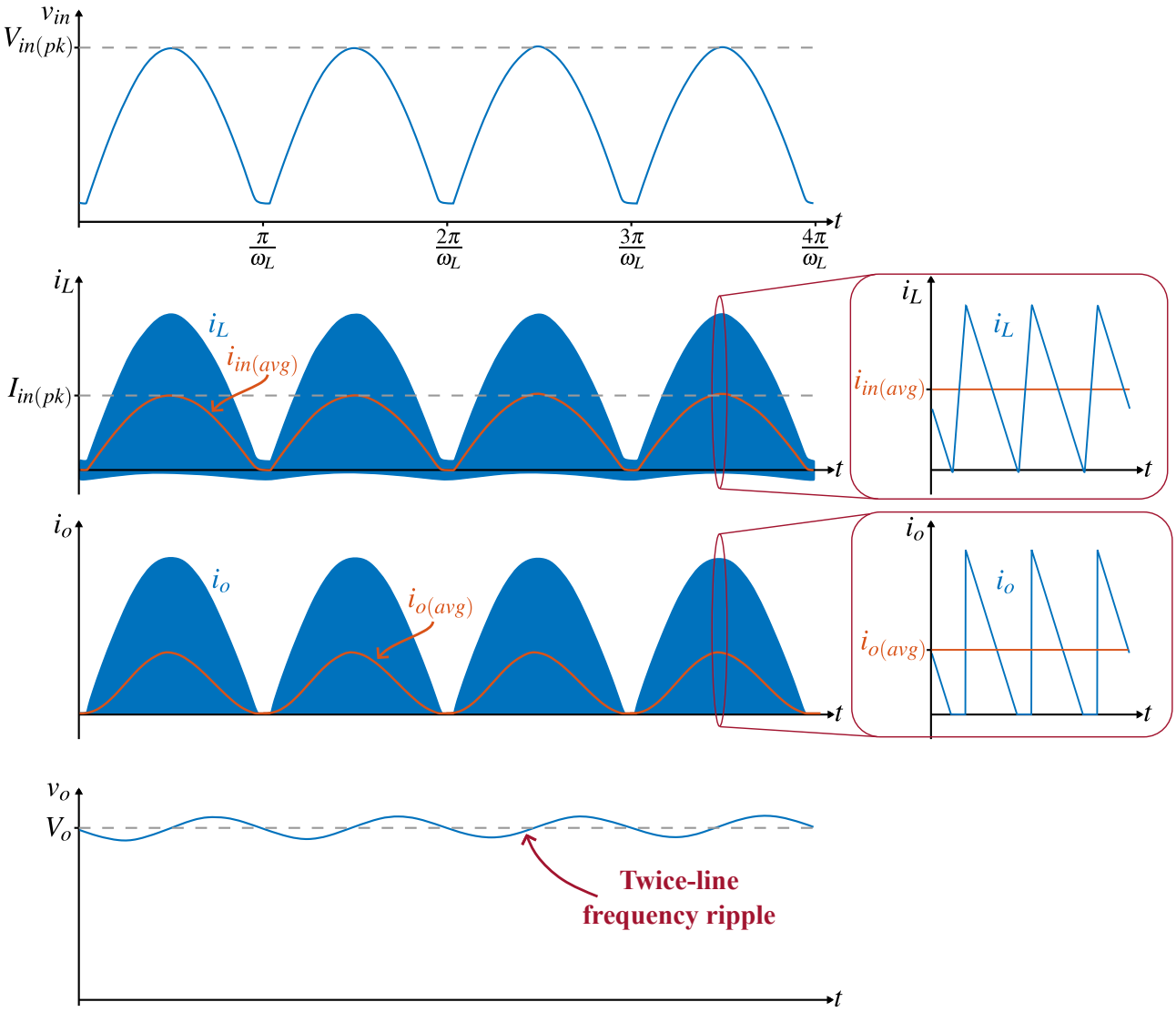


Figure 2.2. Typical waveshapes of v_{in}, $i_{in(avg)}$, $i_{o(avg)}$ and v_o for a single-channel BCM boost converter during steady-state operating conditions.

capable of operating with good performance when the line voltage is a pure sinusoid of a single frequency, or when the line voltage is heavily distorted by higher frequency harmonics.

Many solutions have been proposed in the literature to overcome these design issues. These solutions have mainly focused on reducing the 2nd harmonic voltage ripple to allow a faster bandwidth to be used. A commonly adopted approach is to estimate the 2nd harmonic ripple present on the output voltage, and to subtract this estimate from the sensed output voltage. This is known as active-ripple cancellation [49], [87]–[93]. As a result, the error signal input to the voltage compensator has much less 2nd harmonic ripple, and thus a voltage compensator with a high bandwidth can be used without penalty.

Another approach is to use either a notch or comb filter to remove the 2nd harmonic voltage ripple [51], [52], [94]–[96]. It is difficult to achieve a high attenuation with analog notch filters at the 2nd harmonic frequency due to component tolerances and temperature variations of analog circuit components. Digital notch and comb filters on the other hand

are insensitive to aging and component tolerances. Furthermore, they can be designed to achieve a high selectivity or Q factor, which enables a high attenuation of the output voltage ripple. Another advantage of digital notch and comb filters is that they can be designed to introduce only a small phase delay, and therefore have negligible effect on the phase margin of the control loop. For a universal line voltage input, the line frequency can vary from 48 Hz to 63 Hz. This presents a significant design challenge as the notch or comb filter must be designed to attenuate the output voltage ripple over this range of frequencies. This issue is overcome later on in Section 2.7 by designing an adaptive notch filter that senses the current line frequency, and uses this information to adapt the notch filter coefficients to successfully attenuate the 2^{nd} harmonic ripple at this line frequency.

It is also possible to remove the 2^{nd} harmonic ripple from the sensed ouput voltage by sampling the output voltage at a rate two or four times the line frequency [97]–[99]. Although this method effectively removes the output voltage ripple, it also limits the controller bandwidth to a very low level, and can be prone to limit-cycle oscillations and jitter at low power levels.

Another possible method is to use a "dead-zone" or "regulation-band" method as in [96], [100]. The "dead zone" or "regulation band" is simply a range of voltages within which the output voltage is maintained within during steady-state operation. For example, a typical boost PFC rectifier regulates its output voltage at 400 V. At maximum output power, there could be a 2^{nd} harmonic voltage ripple of ± 20 V. In this case the "dead-zone" is defined as the voltage range from 380 V to 420 V. If the output voltage is within this range, the voltage compensator has a low bandwidth. The low bandwidth ensures low line-current distortion during steady-state. If, however, the output voltage exceeds the boundaries of the "dead zone", which may occur due to a load or line-voltage variation, the voltage compensator switches to a faster bandwidth. This ensures the output voltage has a fast transient response during load steps and changes in line voltage. An issue with the "dead zone" method is that the output voltage can suffer from limit cycle oscillations. This is especially true at lower power levels where the output voltage is considerably smaller than the "dead-zone" region. As a result, when a load step occurs from a low power level, the output voltage may take some time before exiting the "dead zone", at which point the controller switches to a higher bandwidth. If the bandwidth is high enough, the voltage controller overcompensates so that the output voltage re-enters the "dead zone" and continues to the opposing "dead-zone" boundary, where the voltage controller again overcompensates, forcing the output voltage to transition back to the original "dead-zone" boundary. By this means, the output voltage continually transitions from the upper boundary to the lower boundary of the "dead zone" in an undesirable oscillatory fashion. The method can be improved by using a self-tuning "dead zone", whereby the boundaries that define the "dead zone" change to slightly exceed the output voltage ripple. This helps reduce the limit-cycle oscillations and instability issues

at low power.

Other methods that have also been proposed in the literature focus on more advanced voltage-compensator design. These methods include using dual-voltage compensators [99], [101], predictive control [99] and non-linear optimal control [102]. These methods enable faster output voltage response but come at the trade-off of more complex controller design or implementation. It is also possible to use load-current feedforward control [87], [103], where the output load current is sensed and used to estimate the on-time needed for steady-state operation. This method allows for a very fast output voltage response, even when the controller has a low bandwidth, but requires an accurate estimation of the load current and additional sense circuitry.

The overall aim of this chapter is to design a suitable voltage controller that can achieve fast output voltage tracking and a high input power factor at the same time. Section 2.2 begins by deriving the small-signal model of the voltage loop for the multi-channel boost converter. The small-signal analysis is used to design a digital voltage compensator using classical linear feedback control, and this is described in Section 2.3. The limitations of using a simple digital voltage compensator are examined in detail in Section 2.4. In Section 2.5, the performance of the digital voltage compensator is improved by introducing an adaptive gain which improves the output-voltage dynamic response at low line voltages, but which is suitable for implementation on a low-cost fixed-point microcontroller. Section 2.6 discusses a method to design the voltage compensator using fixed-point math. In Section 2.7, an adaptive digital notch filter is designed to improve the power quality of the PFC boost rectifier. The filter works over a range of line frequencies and is designed using fixed-point math. Finally, in Section 2.8 experimental results are provided to validate the performance of the voltage compensator design on a 1 kW 3-channel interleaved BCM boost converter prototype.

2.2 Voltage Loop Small-Signal Analysis

The first step in designing the voltage compensator is to derive the small-signal model of the converter. The small-signal model describes how the converter responds transiently to load steps and to changes in line voltage.

The time-averaged current of the inductor over a single switching cycle can be written as follows

$$i_{L(avg)} = \frac{1}{2}\frac{t_{on}v_{in}}{L} \tag{2.4}$$

This equation is equivalent to the input current drawn by a single-channel BCM boost converter described by (1.9). The total average input current i_{in} into all channels of the multi-channel converter with N channels is

$$i_{in(avg)} = \frac{N}{2}\frac{t_{on}v_{in}}{L} \tag{2.5}$$

The output current flows into the output capacitor C_o and the equivalent load of resistance R. Therefore, the relationship between the current $i_{o(avg)}$ and the output voltage v_o is given by

$$i_{o(avg)} = C_o\frac{dv_o}{dt} + \frac{v_o}{R} \tag{2.6}$$

Equations (2.5), (2.6) and the power balance equation defined earlier in (2.2), are the three governing equations that describe the system model. However, (2.5) and (2.2) are non-linear. It is necessary to first build an accurate linear model of the system, in order to design the voltage compensator using classical linear control,

2.2.1 Linear Small-Signal Model

Combining the power balance expression given by (2.2) with (2.5), the current $i_{o(avg)}$ can be described as a non-linear function of v_{in}, t_{on} and v_o as follows.

$$i_{o(avg)} = \frac{\eta N}{2L}\frac{v_{in}^2 t_{on}}{v_o} = f(v_{in}, t_{on}, v_o) \tag{2.7}$$

This function for $i_{o(avg)}$ can be linearised around a dc operating point, OP, as follows

$$\widetilde{i_{o(avg)}} = \left.\frac{\partial f}{\partial v_{in}}\right|_{OP}\widetilde{v_{in}} + \left.\frac{\partial f}{\partial t_{on}}\right|_{OP}\widetilde{t_{on}} + \left.\frac{\partial f}{\partial v_o}\right|_{OP}\widetilde{v_o} \tag{2.8}$$

where $\widetilde{i_{o(avg)}}$, $\widetilde{t_{on}}$ and $\widetilde{v_o}$ each define the deviation of the time-averaged output current, on-time and output voltage from the dc operating point, and can be calculated by $\widetilde{i_{o(avg)}} = i_{o(avg)} - I_{o(avg)}$, $\widetilde{t_{on}} = t_{on} - T_{on}$, and $\widetilde{v_o} = v_o - V_o$. The terms I_o, T_{on} and V_o describe the output current, on-time and output voltage dc level at the operating point. Expanding (2.8) the

following expression can be obtained for $\widetilde{i_{o(avg)}}$.

$$\widetilde{i_{o(avg)}} = \frac{\eta N T_{on} V_{in(avg)}}{L V_o} \widetilde{v_{in}} + \frac{\eta N V_{in(avg)}^2}{2 L V_o} \widetilde{t_{on}} - \frac{\eta N V_{in(avg)}^2 T_{on}}{2 L V_o^2} \widetilde{v_o} \tag{2.9}$$

The on-time at the operating point T_{on} can be redefined in terms of V_o, $V_{in(avg)}$, $V_{in(rms)}$ and P_o by using (2.5).

$$\begin{aligned} T_{on} &= \frac{2L}{N} \frac{I_{in(avg)}}{V_{in(avg)}} = \frac{2L}{N} \frac{I_{in(rms)}}{V_{in(rms)}} \\ &= \frac{2L}{N} \frac{1}{V_{in(rms)}^2} V_{in(rms)} I_{in(rms)} \\ &= \frac{2L}{N} \frac{1}{V_{in(rms)}^2} \frac{P_o}{\eta} \end{aligned} \tag{2.10}$$

Substituting this value of T_{on} into (2.9), we get

$$\widetilde{i_{o(avg)}} = 2 \frac{V_{in(avg)}}{V_{in(rms)}^2} \frac{P_o}{V_o} \widetilde{v_{in}} + \frac{\eta N V_{in(avg)}^2}{2 L V_o} \widetilde{t_{on}} - \frac{V_{in(avg)}^2}{V_{in(rms)}^2} \frac{P_o}{V_o^2} \widetilde{v_o} \tag{2.11}$$

The complete linear model of the system is obtained by linearising (2.6) around the same operating point. Thus,

$$\widetilde{i_{o(avg)}} = C_o \frac{d\widetilde{v_o}}{dt} + \frac{P_o}{V_o^2} \widetilde{v_o} \tag{2.12}$$

Combining (2.11) and (2.12), the full linear system model can be described by a single equation as

$$C_o \frac{d\widetilde{v_o}}{dt} + \frac{P_o}{V_o^2} \widetilde{v_o} = 2 \frac{V_{in(avg)}}{V_{in(rms)}^2} \frac{P_o}{V_o} \widetilde{v_{in}} + \frac{\eta N V_{in(avg)}^2}{2 L V_o} \widetilde{t_{on}} - \frac{V_{in(avg)}^2}{V_{in(rms)}^2} \frac{P_o}{V_o^2} \widetilde{v_o}$$

or

$$C_o \frac{d\widetilde{v_o}}{dt} + \left(\frac{P_o}{V_o^2} \left(1 + \frac{V_{in(avg)}^2}{V_{in(rms)}^2} \right) \right) \widetilde{v_o} = 2 \frac{V_{in(avg)}}{V_{in(rms)}^2} \frac{P_o}{V_o} \widetilde{v_{in}} + \frac{\eta N V_{in(avg)}^2}{2 L V_o} \widetilde{t_{on}} \tag{2.13}$$

By converting (2.13) into the Laplace domain and re-arranging, the open-loop transfer function of the plant of $\frac{V_o}{T_{on}}(s)$ can be obtained as follows

$$s C_o V_o(s) + \left(\frac{P_o}{V_o^2} \left(1 + \frac{V_{in(avg)}^2}{V_{in(rms)}^2} \right) \right) V_o(s) = 2 \frac{V_{in(avg)}}{V_{in(rms)}^2} \frac{P_o}{V_o} V_{in}(s) + \frac{\eta N V_{in(avg)}^2}{2 L V_o} T_{on}(s)$$

$$\left(s C_o + \frac{P_o}{V_o^2} \left(1 + \frac{V_{in(avg)}^2}{V_{in(rms)}^2} \right) \right) V_o(s) = 2 \frac{V_{in(avg)}}{V_{in(rms)}^2} \frac{P_o}{V_o} V_{in}(s) + \frac{\eta N V_{in(avg)}^2}{2 L V_o} T_{on}(s)$$

$$\therefore \frac{V_o}{T_{on}}(s) = \frac{\eta N V_{in(avg)}^2}{2LV_o} \frac{1}{sC_o + \frac{P_o}{V_o^2}\left(1 + \frac{V_{in(avg)}^2}{V_{in(rms)}^2}\right)} \tag{2.14}$$

For a dc input $V_{in(avg)} = V_{in(rms)}$, as is the case for a dc-dc converter, thus (2.14) can be written as

$$\frac{V_o}{T_{on}}(s) = \frac{\eta N V_{in(avg)}^2}{2LV_o} \frac{1}{sC_o + 2\frac{P_o}{V_o^2}} \tag{2.15}$$

For an ac input $V_{in(avg)} = \frac{2\sqrt{2}}{\pi} V_{in(rms)}$, and (2.14) can be written as

$$\frac{V_o}{T_{on}}(s) = \frac{\eta N V_{in(avg)}^2}{2LV_o} \frac{1}{sC_o + \frac{P_o}{V_o^2}(1 + \frac{8}{\pi^2})} \tag{2.16}$$

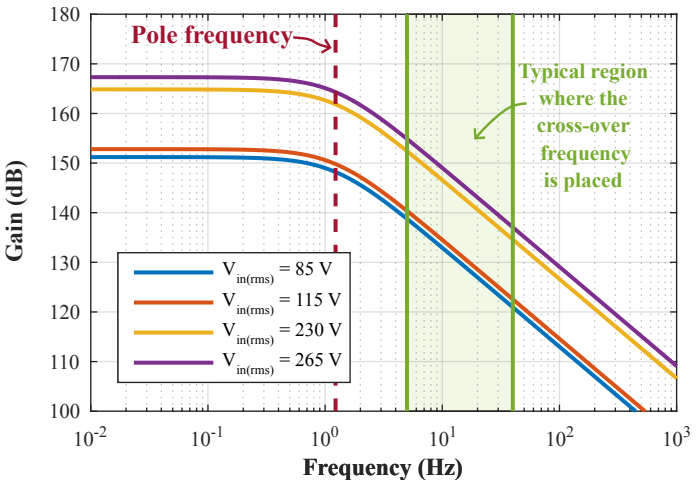
It is clear from examining (2.15) and (2.16) that the open-loop system is a function of both the average input voltage and the output power. The open-loop gain changes proportionally to $V_{in(avg)}^2$, and the position of the transfer function's pole is a function of the converter's output power. The open-loop Bode plot described by (2.16) is plotted over its entire line-voltage range at an output power of $P_o = 500$ W in Figure 2.3. The magnitude response is given in Figure 2.3(a), while the phase response is given in Figure 2.3(b). The plots demonstrate the change in the open-loop response with the applied line voltage. A list of the other power stage parameters used to calculate the open-loop response is given in Table 2.1. The typical region where the voltage-loop cross-over frequency is placed is highlighted in Figure 2.3. The voltage-loop cross-over frequency is the frequency at which the compensated open-loop system response crosses 0 dB, and is the same frequency as the controller's bandwidth. The highlighted region is important, as the cross-over frequency dictates the system's bandwidth and phase-margin. The gain of the open-loop magnitude response in this region is reduced at low line voltages, thus the output voltage transient response becomes slower at low line voltages.

The pole frequency is to the left of the highlighted region, therefore the variation in the dc level of the output power has no noticeable effect on the phase margin and bandwidth of the designed controller, and thus the output power has little effect on the transient response of the output voltage.

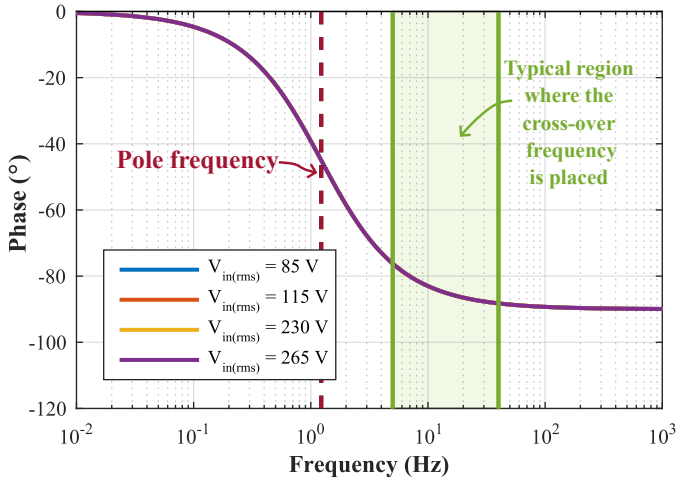
The open-loop transfer function described by (2.15) and (2.16), can be approximated by (2.17) in the cross-over-frequency region highlighted in Figure 2.3.

$$\frac{V_o}{T_{on}}(s) \simeq \frac{\eta N V_{in(avg)}^2}{2LV_o} \frac{1}{sC_o} \tag{2.17}$$

Since only the highlighted region of Figure 2.3 is important for the controller design, this simplified transfer function can be used to design the voltage controller.



(a)



(b)

Figure 2.3. The variation of (a) the open-loop magnitude response and (b) the open-loop phase response with respect to changes in the rms value of the line voltage.

TABLE 2.1
LIST OF POWER STAGE PARAMETERS

Parameter	Value
Efficiency, η	0.96
Number of channels, N	3
Boost inductance, L	130 µH
Output capacitance, C_o	880 µF
Output voltage, V_o	400 V
RMS line voltage, $V_{in(rms)}$	85 V to 265 V
Output Power P_o	0 kW to 1 kW

2.3 Simple Voltage-Compensator Design

An integral lead-lag compensator or a proportional-integral compensator are suitable choices of controller to regulate the output voltage. In this work, an integral lead-lag compensator is used. The transfer function of an integral lead-lag compensator in the analog domain is

given in (2.18).

$$C_v(s) = \frac{K}{s}\frac{1+a\tau s}{1+\tau s} \tag{2.18}$$

This type of controller has a pole at $s = 0$, which ensures infinite dc gain and thus zero steady-state tracking error of the reference voltage, for constant-voltage tracking. The gain term K is used to ensure the desired open-loop cross-over frequency is achieved, while the terms a and τ are chosen to inject a certain amount of phase into the system at the cross-over frequency.

The terms K, a and τ can be understood by looking at the magnitude and phase response of a non-integral lead-lag compensator, also called a lead-lag compensator for simplicity. A lead-lag compensator has a transfer function of $K\frac{1+a\tau s}{1+\tau s}$. This transfer function is equivalent to the controller transfer function described by (2.18), except that the integral term of $\frac{1}{s}$ has been removed. The magnitude and phase Bode plots for a lead-lag compensator are shown

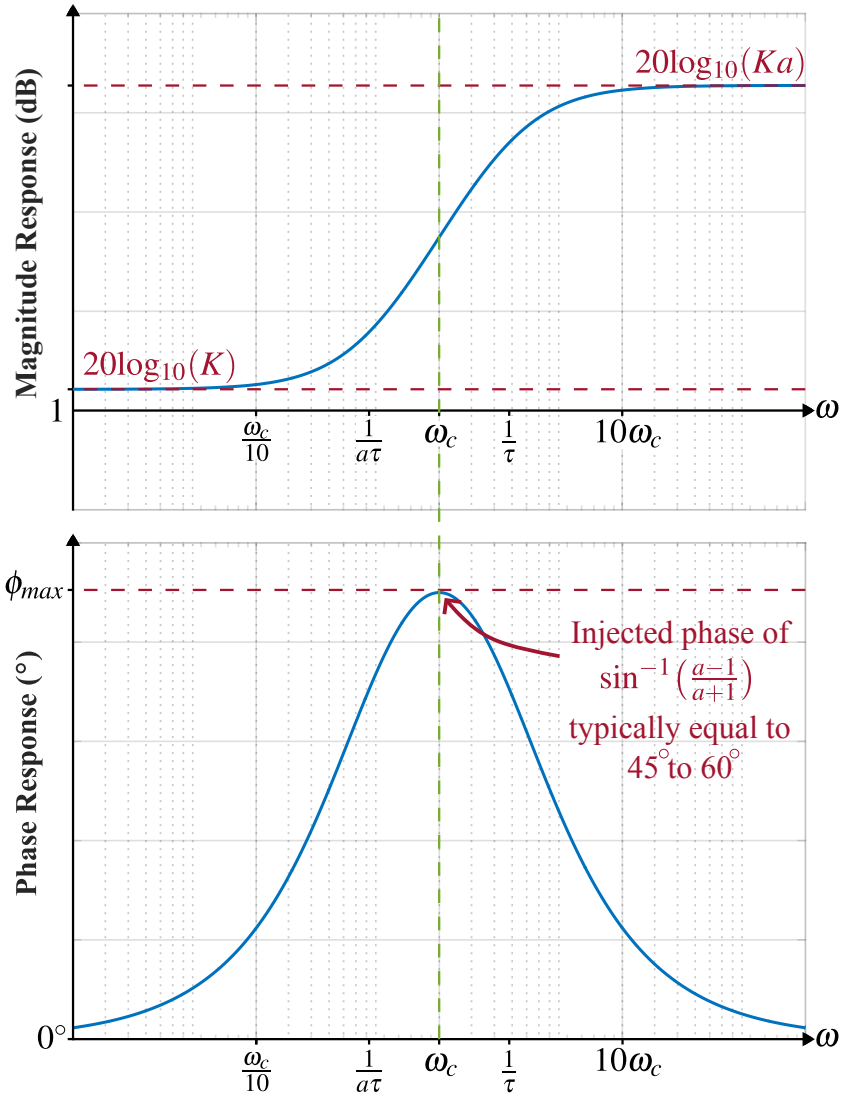


Figure 2.4. Magnitude response (upper) and phase response (lower) of a non-integral lead-lag controller with a transfer function of $K\frac{1+a\tau s}{1+\tau s}$, where $a > 1$.

in Figure 2.4 for the case when $a > 1$. When the term a is set greater than unity the lead-lag

controller injects a positive phase into the system, and it is called a lead compensator. When the term a is less than unity a negative phase is injected into the system, and the controller is called a lag compensator. The term a is chosen to set the desired amount of phase injected by the lead compensator. The maximum phase that can be injected by the lead compensator is denoted ϕ_{max}, and is calculated by

$$\phi_{max} = \sin^{-1}\left(\frac{a-1}{a+1}\right) \tag{2.19}$$

By re-arranging this equation, an expression can be found for the term a in terms of ϕ_{max}.

$$a = \frac{\sin(\phi_{max})+1}{1-\sin(\phi_{max})} \tag{2.20}$$

It is desirable have a phase margin of 45° to 60° in order to achieve a fast response with reasonable peak overshoot. From Figure 2.3(b), the phase of the open-loop system in the cross-over frequency region is from -80° to -90°. The integral part of the controller introduces a phase shift of -90° at all frequencies. Therefore, in order to achieve a phase-margin of 45° to 60°, a phase of about 45° must be injected by the lead compensator. Thus, the injected phase is set to $\phi_{max} = 45^\circ$, and the term a can be calculated as

$$\begin{aligned} a =& \frac{\sin(45^\circ)+1}{1-\sin(45^\circ)} \\ =& 5.83 \end{aligned} \tag{2.21}$$

The term τ is calculated so that the maximum phase injected by the lead compensator is injected at the cross-over frequency ω_c. The cross-over frequency is the frequency at which the Bode plot of the compensated open-loop system equals unity or 0 dB. The cross-over frequency is also the bandwidth frequency of the controller.

$$\tau = \frac{1}{\omega_c\sqrt{a}} \tag{2.22}$$

2.3.1 Digital Integral Lead-Lag Controller

The transfer function of the integral lead-lag controller described in (2.18) is in the analog domain. Our goal is to design a controller in the digital domain with the same characteristic as that described by (2.18). The bilinear transformation is used to convert the analog transfer function to an equivalent digital transfer function with similar characteristics. The bilinear transformation is described by

$$s = \frac{2}{T_v}\frac{z-1}{z+1} \tag{2.23}$$

where T_v is the sampling period of the output voltage, and s is the Laplace operator defined by $s = j\omega$, and z is the $\mathcal{Z}$-domain operator defined by $z = e^{sT_v}$. By replacing the Laplace operator s in (2.18), with the expression for s obtained from the bilinear transformation, the following digital transfer function for an integral lead compensator is derived.

$$C_v(z) = k_c \frac{z+1}{z-1}\left(\frac{z(1+\frac{2a\tau}{T_v})+(1-\frac{2a\tau}{T_v})}{z(1+\frac{2\tau}{T_v})+(1-\frac{2\tau}{T_v})}\right) \tag{2.24}$$

The term k_c is a constant gain term which is chosen to achieve the desired cross-over frequency.

2.3.2 Compensated Open-Loop Bode Plots

The gain term k_c is obtained by evaluating the system compensated open-loop bode plots at the cross-over frequency. Hence, in order to calculate k_c, an expression must be obtained to describe the system's compensated open-loop magnitude response.

The full control block diagram of the voltage loop is given in Figure 2.5. It includes a gain of $\frac{1}{f_{pwm}}$, which is the clock frequency of the microcontroller PWM peripheral that scales the on-time in clock ticks, $t_{on(ticks)}$, to the on-time in seconds t_{on}. It also includes a delay of z^{-1}, and a zero-order-hold (ZOH) block created by the code execution and the analog-to-digital-converter (ADC) output-voltage sampling, as well as the combined gain of the output voltage sensor (typically a potential divider circuit) and ADC conversion, which is denoted H_v. The compensated open-loop transfer function is denoted $T_{cv}(z)$, and it is the

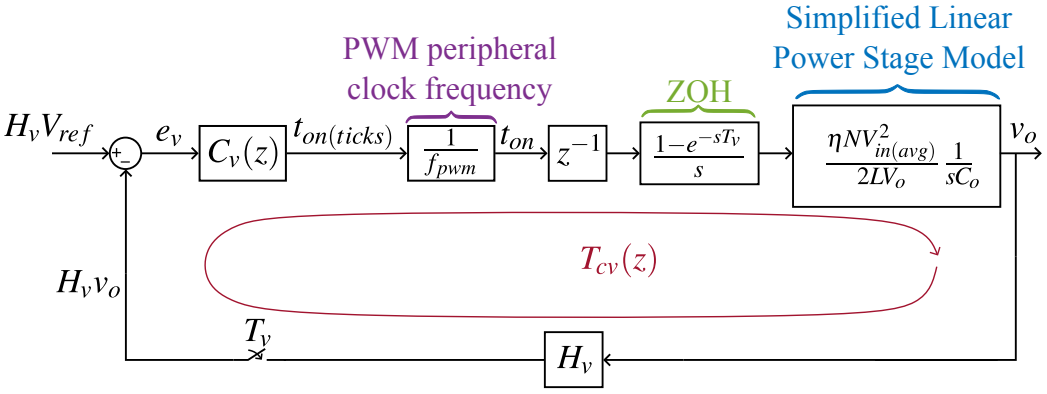


Figure 2.5. Voltage-loop control block diagram.

product of the ZOH, the simplified linear power-stage model and the sensor-ADC gain the controller transfer function, the PWM peripheral clock frequency and microcontroller delay.

$$\begin{aligned} T_{cv}(z) &= z^{-1}C_v(z)\frac{1}{f_{pwm}}\mathcal{Z}\left\{\frac{1-e^{-sT_v}}{s}H_v\frac{\eta NV_{in(avg)}^2}{2LV_o}\frac{1}{sC_o}\right\} \\ &= z^{-1}C_v(z)\frac{1}{f_{pwm}}H_v\frac{\eta NV_{in(avg)}^2}{2LV_o}\frac{T_v}{C_o}\frac{1}{z(z-1)} \end{aligned} \tag{2.25}$$

With the transfer function $T_{cv}(z)$ defined, it is possible to calculate the appropriate value of k_c which ensures that $T_{cv}(z)$ has a gain of unity at the cross-over frequency ω_c:

$$|T_{cv}(e^{j\omega_c})| = 1 \tag{2.26}$$

Combining (2.24), (2.25) and (2.26) and substituting $z = e^{j\omega_c}$, the following expression can be found for the controller gain k_c:

$$k_c = \frac{2LV_oC_of_{pwm}|e^{j\omega_cT_v} - 1|^2 \, |e^{j\omega_cT_v}(1+\frac{2\tau}{T_v}) + (1-\frac{2\tau}{T_v})|}{\eta NV_{in(avg)}^2 H_vT_v \, |e^{j\omega_cT_v} + 1| \, |e^{j\omega_cT_v}(1+\frac{2a\tau}{T_v}) + (1-\frac{2a\tau}{T_v})|} \tag{2.27}$$

Now that all three terms k_c, a and τ are defined, the controller transfer function described by (2.24) is fully defined, and can be used to derive a recursive algorithm that can be executed in microcontroller software.

2.3.3 Digital Controller Recursive Algorithm

The transfer function defined in (2.24) must be re-written in the form shown in (2.28) to derive a recursive algorithm that can be used to implement the controller transfer function.

$$C_v(z) = \frac{b_{v0} + b_{v1}z^{-1} + b_{v2}z^{-2}}{1 - a_{v1}z^{-1} - a_{v2}z^{-2}} \tag{2.28}$$

where b_{v0}, b_{v1}, b_{v2}, a_{v1} and a_{v2} are constant coefficients which define the voltage controller. This is made possible by simply multiplying and expanding the terms in (2.24) as follows

$$\begin{aligned}
C_v(z) &= k_c\frac{z+1}{z-1}\left(\frac{z(1+\frac{2a\tau}{T_v}) + (1-\frac{2a\tau}{T_v})}{z(1+\frac{2\tau}{T_v}) + (1-\frac{2\tau}{T_v})}\right) \\
&= \frac{(k_c(1+\frac{2a\tau}{T_v})) + z^{-1}(2k_c) + z^{-2}(k_c(1-\frac{2a\tau}{T_v}))}{(1+\frac{2\tau}{T_v}) + z^{-1}(-\frac{4\tau}{T_v}) + z^{-2}(\frac{2\tau}{T_v} - 1)} \\
&= \frac{\left(\frac{k_c(1+\frac{2a\tau}{T_v})}{1+\frac{2\tau}{T_v}}\right) + z^{-1}\left(\frac{2k_c}{1+\frac{2\tau}{T_v}}\right) + z^{-2}\left(\frac{k_c(1-\frac{2a\tau}{T_v})}{1+\frac{2\tau}{T_v}}\right)}{1 - z^{-1}\left(\frac{\frac{4\tau}{T_v}}{1+\frac{2\tau}{T_v}}\right) - z^{-2}\left(\frac{1-\frac{2\tau}{T_v}}{1+\frac{2\tau}{T_v}}\right)} \\
&= \frac{\left(k_c\frac{T_v+2a\tau}{T_v+2\tau}\right) + z^{-1}\left(\frac{2k_cT_v}{T_v+2\tau}\right) + z^{-2}\left(k_c\frac{T_v-2a\tau}{T_v+2\tau}\right)}{1 - z^{-1}\left(\frac{4\tau}{T_v+2\tau}\right) - z^{-2}\left(\frac{T_v-2\tau}{T_v+2\tau}\right)}
\end{aligned} \tag{2.29}$$

Comparing (2.28) to (2.29), the controller coefficients can be defined by equating each of the coefficients with the corresponding term. Thus

$$b_{v0} = k_c \frac{T_v + 2a\tau}{T_v + 2\tau} \tag{2.30}$$

$$b_{v1} = k_c \frac{2T_v}{T_v + 2\tau} \tag{2.31}$$

$$b_{v2} = k_c \frac{T_v - 2a\tau}{T_v + 2\tau} \tag{2.32}$$

$$a_{v1} = \frac{4\tau}{T_v + 2\tau} \tag{2.33}$$

$$a_{v2} = \frac{T_v - 2\tau}{T_v + 2\tau} \tag{2.34}$$

With the controller coefficients defined, it becomes very simple to derive a recursive algorithm to implement the controller by converting (2.28) from the $\mathcal{Z}$-domain into the time domain. The transfer function $C_v(z)$ is equal to the transfer function $\frac{T_{on(ticks)}(z)}{E_v(z)}$, where $T_{on(ticks)}(z)$ is the $\mathcal{Z}$-domain representation of the time-domain function $t_{on(ticks)}$, and $E_v(z)$ is the $\mathcal{Z}$-domain representation of the voltage error signal, which is also the input to the voltage controller and can be defined in the time domain as $e_v[n] = H_v(V_{ref} - v_o[n])$. The term n is used to define an integer number that represents the index of the output voltage sample taken by the ADC. Thus, the time-domain recursive algorithm used to implement the voltage controller can be derived as follows,

$$\frac{T_{on(ticks)}(z)}{E_v(z)} = \frac{b_{v0} + b_{v1}z^{-1} + b_{v2}z^{-2}}{1 - a_{v1}z^{-1} - a_{v2}z^{-2}}$$

$$\therefore T_{on(ticks)}(z)\left(1 - a_{v1}z^{-1} - a_{v2}z^{-2}\right) = E_v(z)\left(b_{v0} + b_{v1}z^{-1} + b_{v2}z^{-2}\right)$$

$$\therefore T_{on(ticks)}(z) = E_v(z)\left(b_{v0} + b_{v1}z^{-1} + b_{v2}z^{-2}\right) + T_{on(ticks)}(z)\left(a_{v1}z^{-1} + a_{v2}z^{-2}\right) \tag{2.35}$$

By converting (2.35) to the time domain, the following discrete-time expression is obtained.

$$t_{on(ticks)}[n] = b_{v0}e_v[n] + b_{v1}e_v[n-1] + b_{v2}e_v[n-2] + a_{v1}t_{on(ticks)}[n-1] + a_{v2}t_{on(ticks)}[n-2] \tag{2.36}$$

The recursive algorithm is now defined by (2.36), and can be used to implement the controller if the microcontroller uses floating-point arithmetic. The disadvantage to using floating-point arithmetic is that the microcontroller must have a floating-point math unit built into its CPU, or else it requires a very long execution time to implement the floating-point algorithm using

fixed-point operations. Microcontrollers with a floating-point math unit built-in to their CPU, such as the Texas Instrument Piccolo and Delfino series [104],[105], are more expensive than microcontrollers that have no special floating-point capabilities, such as the Infineon XMC series [106]. Therefore, for a low-cost implementation it is more desirable to implement the voltage compensator using fixed-point math. For a fixed-point math implementation, special care must be taken in the scaling of controller coefficients to ensure that no fixed-point computation suffers from significant quantization error or integer overflow. Implementing the voltage compensator using fixed-point arithmetic is discussed later in Section B.1.

2.4 Controller Limitations

In order to explore the controller limitations in more detail, a Simulink model was built for a single-channel BCM boost converter. The model was then used to compare the different controller bandwidths and operating conditions.

A simplified schematic diagram depicting the Simulink simulation is shown in Figure 2.6. A full description of the Simulink model is provided in Appendix A. The model consists of an ac source, a LCLC differential-mode EMI filter, followed by a single-channel BCM boost converter with a digital voltage compensator. The model also includes a 0.68 µF input capacitor and a linear 100 pF capacitor, which is placed across the MOSFET's drain and source terminals to model the drain-source capacitance of the MOSFET. The model does not take into account the effects of the ADC resolution. The voltage compensator has been designed using the methods outlined in Subsection 2.3.2 and Subsection 2.3.3.

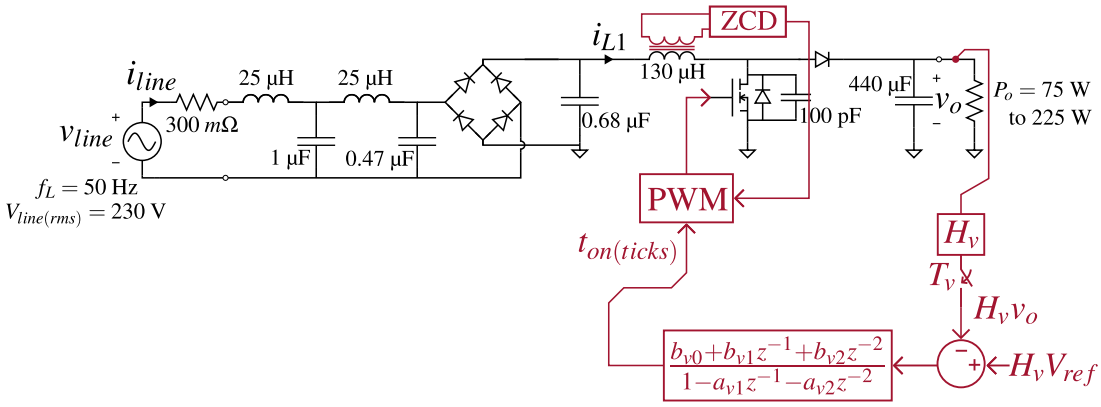


Figure 2.6. Simplified block diagram of the Simulink model (a full description of the Simulink model is given in Appendix A).

2.4.1 Controller Bandwidth Trade-off

First, we investigate the effects of using high or low bandwidths. The Simulink model was simulated using a controller with a low bandwidth of 8 Hz, and then the simulation was repeated for a controller designed to have a faster bandwidth of 50 Hz. Table 2.2 gives a list of parameters for both controllers.

Figure 2.7 shows the simulation results for when the bandwidth is set to 8 Hz. The figure shows four different waveform graphs. The top graph shows the response of the inductor current i_{L1} and averaged inductor current $i_{L1(avg)}$. The second waveform shows the response of the output voltage v_o. The third waveform shows the response of the on-time t_{on} computed by the voltage controller. The bottom waveform shows the shape of the line voltage and line current. All graphs have the same time axis, but different y axes. It is evident from the output voltage's response, that when the bandwidth is set to this low value of 8 Hz, that the output voltage suffers from a significant peak undershoot of nearly 50 V, and moreover, has a considerable settling time before it accurately tracks the setpoint voltage reference

TABLE 2.2
LIST OF SIMULATED VOLTAGE COMPENSATOR PARAMETERS

Parameter	8 Hz Bandwidth	50 Hz Bandwidth
Cross-over frequency, ω_c	2π8 rad/s	2π50 rad/s
Voltage sampling period, T_v	100 µs	100 µs
PWM resolution, f_{pwm}	96 MHz	96 MHz
Sensor-ADC gain, Hv	8.11	8.11
Injected phase , ϕ_{max}	45°	45°
Controller Gain , k_c	1.72e-04	6.724e-3
Controller coefficients, a_{v1}, a_{v2}	1.9879, -0.9879	1.9269, -0.9269
Controller coefficients, b_{v0}, b_{v1}, b_{v2}	0.998e-3, 0.0021e-3, -0.996e-3	3.800e-2, 0.049e-2, -3.751e-2

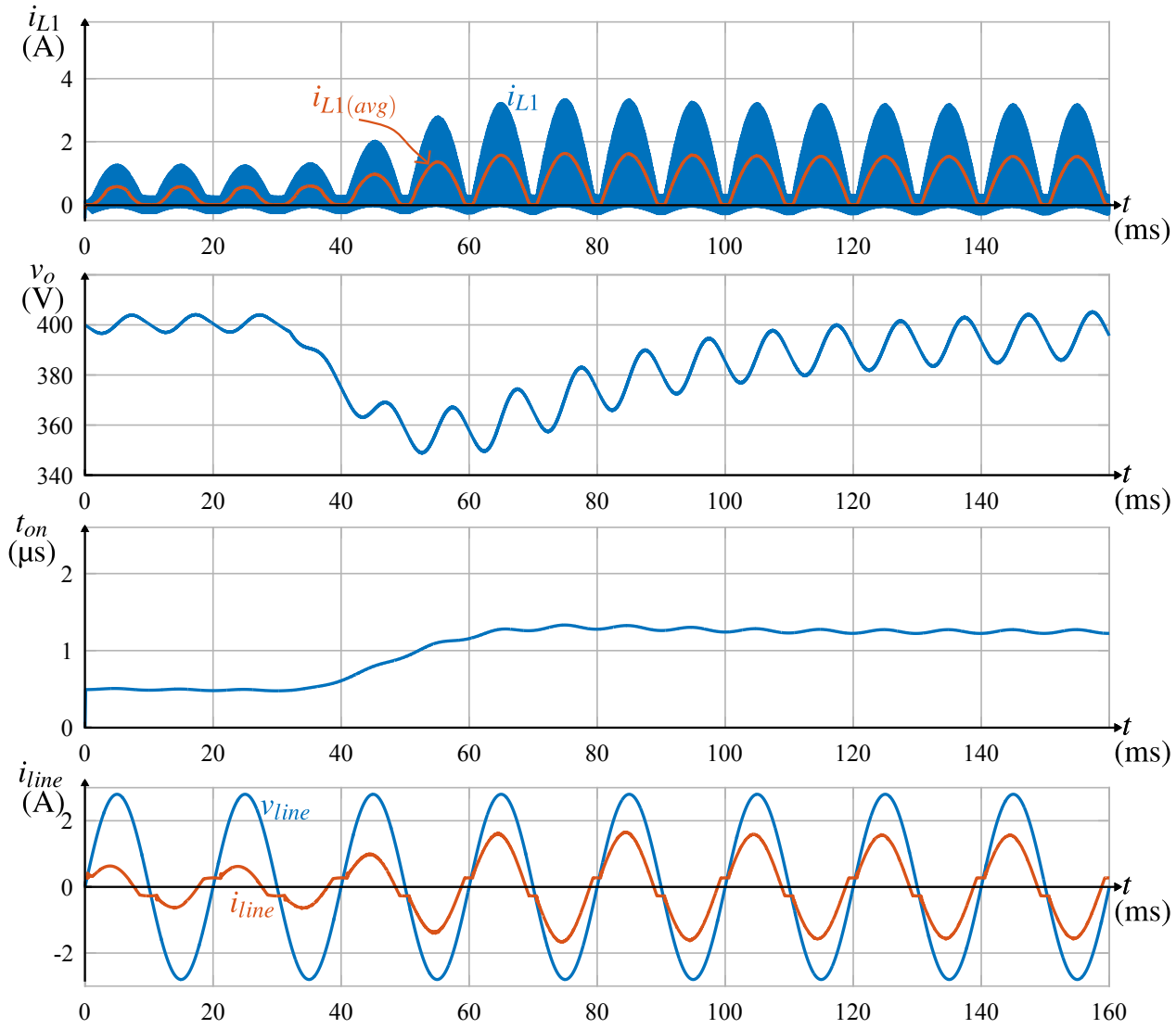


Figure 2.7. Simulation results for a load step of 75 W to 225 W at $t = 0.032$ s, when the controller is designed for a cross-over frequency of $\omega_c = 2\pi 8$ rad/s.

again. However, the lower bandwidth also ensures that the 2nd harmonic ripple present on the computed on-time is heavily attenuated by the voltage compensator. Therefore, the line current contains very little of the 2nd harmonic ripple, and has a very sinusoidal shape during steady-state operation. The line current is still distorted by the input capacitor, which

creates a phase-leading characteristic, and the boost MOSFET's drain-source capacitor, which creates a region where the average inductor current is zero. The voltage compensator design has negligible effect on the input capacitor and MOSFET drain-source-capacitor line-current distortions. These effects will be re-visited in more detail in Chapter 3.

Figure 2.8 shows the same waveforms when the simulation is repeated with the controller bandwidth set to 50 Hz. The faster bandwidth results in much faster output voltage dynamics, and as a result, there is almost no undershoot of the output voltage. The negative effect of the higher bandwidth is that the on-time now contains a large amount of the 2nd harmonic ripple. The 2nd harmonic ripple component creates distortion in the line current wave shape and severely degrades the converter's power factor.

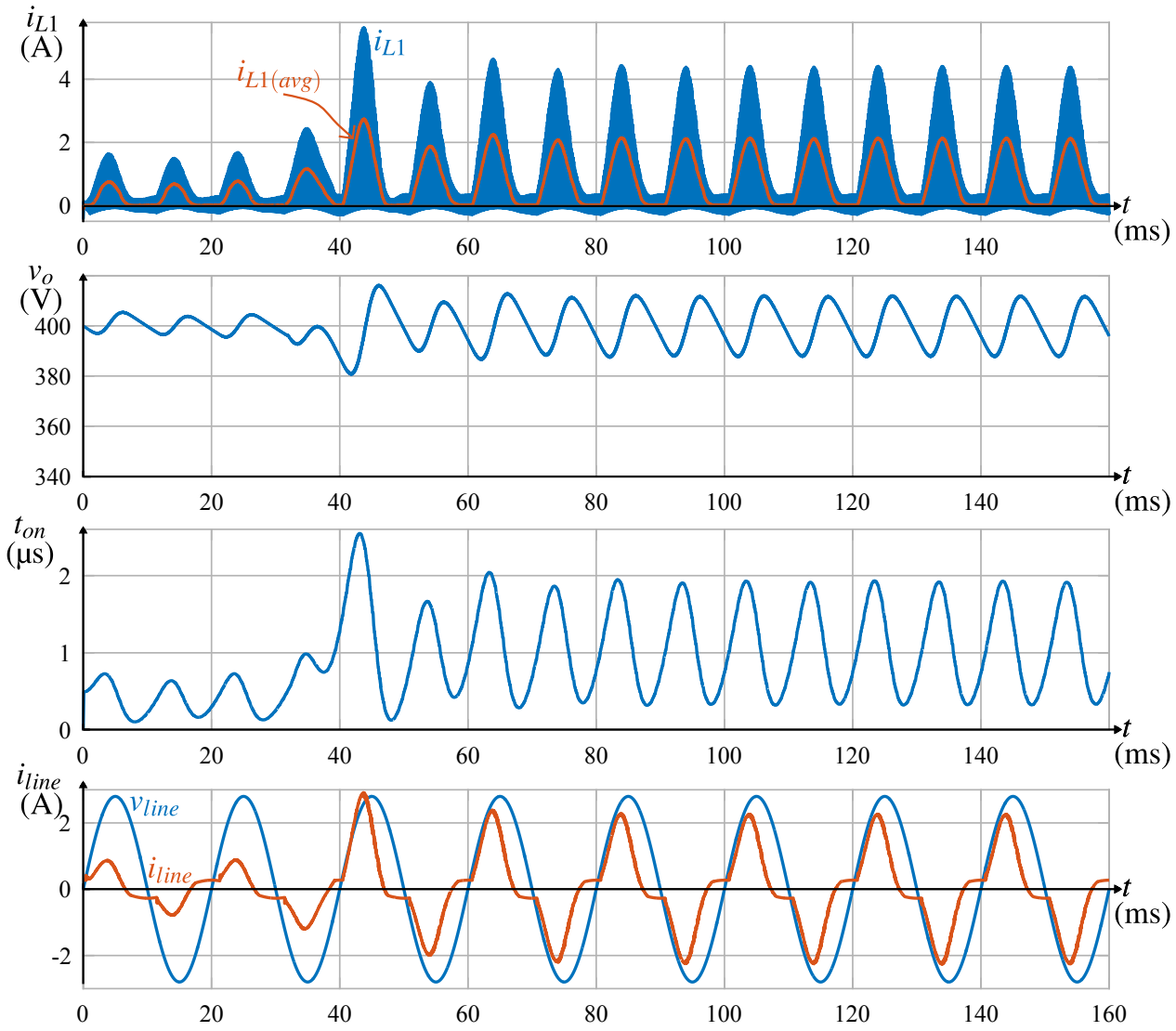


Figure 2.8. Simulation results for a load step of 75 W to 225 W at $t = 0.032$ s, when the controller is designed for a cross-over frequency of $\omega_c = 2\pi 50$ rad/s.

2.4.2 Effects of Line Voltage on the Output Voltage Dynamic Response

Another disadvantage of the controller shown in Figure 2.6, is that the output-voltage dynamic response degrades severely at low line voltages. In order to demonstrate this behaviour, the controller was re-designed to have a bandwidth of 15 Hz, and the same load step from 75 W to 225 W was run at 230 Vrms, followed by 115 Vrms using the same controller coefficients. Figure 2.9 shows the waveshape of the output voltage and line current at 230 Vrms. It can be seen in this case that the 15 Hz bandwidth provides a good trade-off between having a fast output-voltage transient response and maintaining a low level of line-current distortion.

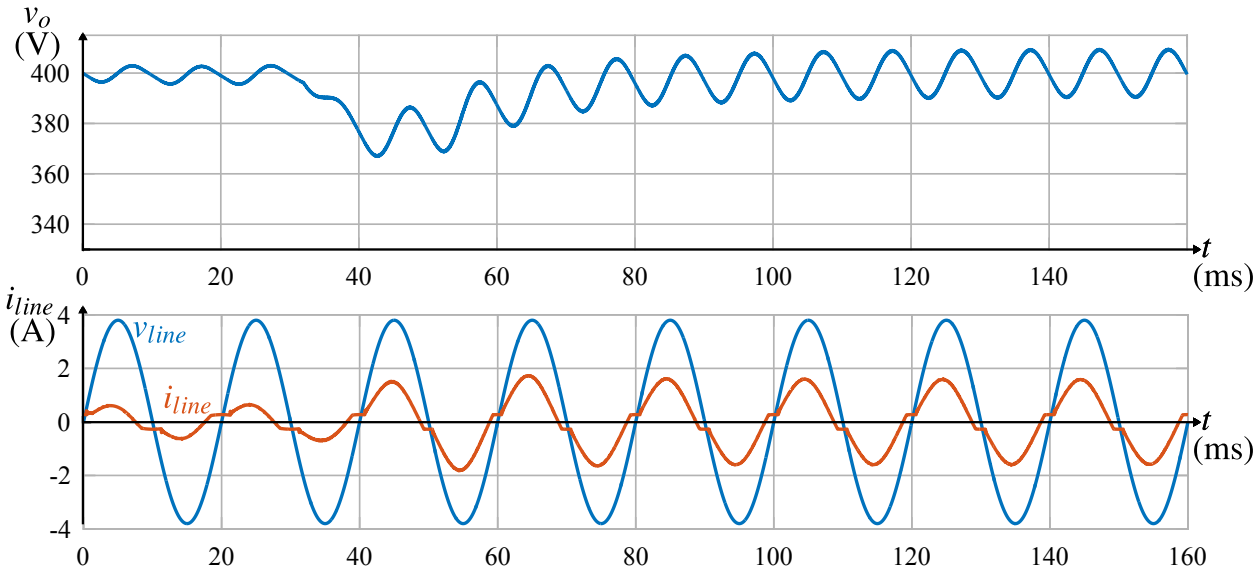


Figure 2.9. Simulation results for a load step of 75 W to 225 W at 230 Vrms, when the controller is designed for a cross-over frequency of $\omega_c = 2\pi 15$ rad/s.

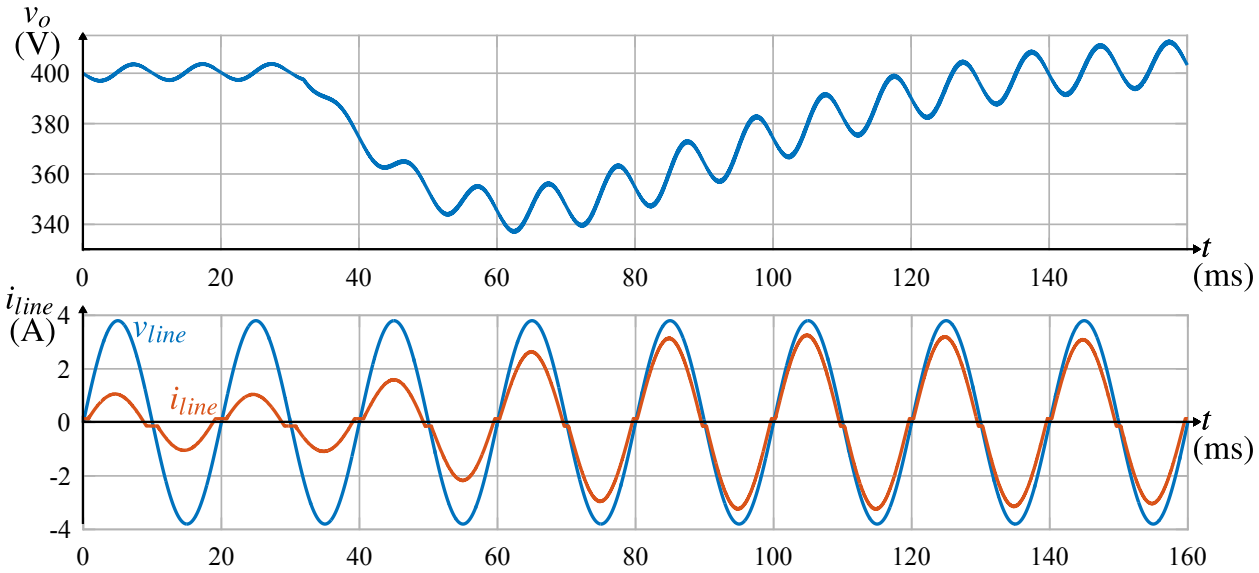


Figure 2.10. Simulation results for a load step of 75 W to 225 W at 115 Vrms, when the controller is designed for a cross-over frequency of $\omega_c = 2\pi 15$ rad/s.

Figure 2.10 demonstrates the simulation result for using the same controller, but re-running the simulation at 115 Vrms. In this case the output voltage dynamic response

becomes much slower and results in a severe peak undershoot of the output voltage. In the next section, an adaptive gain is implemented that increases the controller's gain at low line voltages, in order to counteract this behaviour.

It is important to point out here that the gain of $\frac{V_o}{T_{on}}(s)$ is proportional to $V_{in(avg)}^2$. Therefore for lower levels of input voltage the system has a lower open-loop gain and slower output voltage tracking.

2.5 Voltage Compensator Design with an Adaptive Gain

This Section describes implementing the voltage controller with an adaptive gain. The effect of the line voltage on the output voltage dynamics must be better understood in order to design and optimise the adaptive gain. This is accomplished by examining the variation in the voltage loop's compensated open-loop response $T_{cv}(z)$.

2.5.1 Compensated Open-Loop Bode Plot Variation

From the analysis provided in Section 2.4.2, it is clear that the voltage compensator has slower output-voltage dynamics when the line voltage is low. This can be better understood by plotting the variation of the compensated open-loop Bode plot $T_{cv}(z)$ at different line voltages.

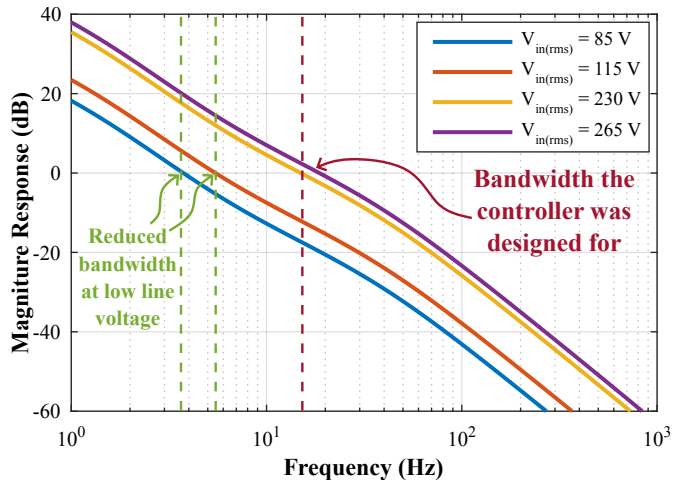
Figure 2.11 shows the Bode plot variation of $T_{cv}(z)$ for the 3-channel BCM converter with parameters described in Table 2.1. The digital voltage compensator is designed to have a bandwidth of 15 Hz at 230 Vrms. It can be seen that, although the controller achieves the desired bandwidth at 230 Vrms, the controller's bandwidth is severely reduced at lower line voltages. As a result, the controller has a bandwidth of 5.4 Hz at 115 Vrms, and a bandwidth of 3.7 Hz at 85 Vrms.

Similarly, the controller achieves a phase margin of 50° when the line voltage is 230 V, but since lower line voltages reduce the bandwidth, the phase margin is also reduced. This is undesirable, as a lower phase margin creates larger peak overshoots and undershoots during load and line disturbances.

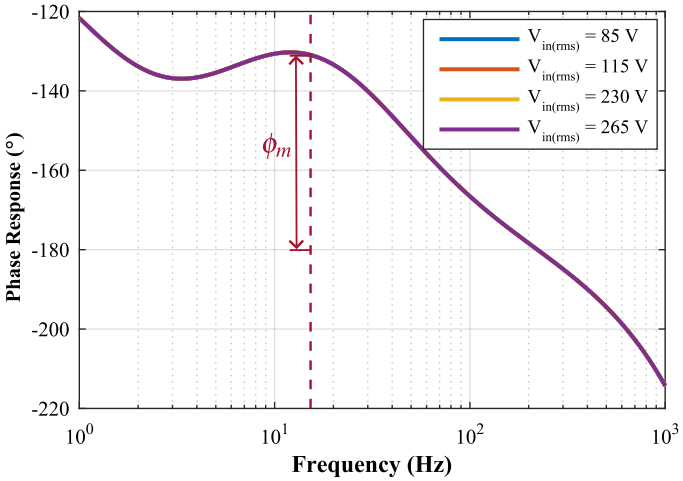
It is also possible to plot the variation in $T_{cv}(z)$ with load power. This is done in Figure 2.12. Changes in load power have no significant effect on the transient performance of the output voltage. This is because power has no significant effect on the controller's bandwidth as can be seen from the magnitude response in Figure 2.12(a). Examining the variation in the phase response in Figure 2.12(b), it can be observed the phase margin increases slightly as the load power increases. This causes the output voltage response to be more damped at higher load powers, but since the variation in phase margin is small, there is no significant effect.

2.5.2 Adaptive Gain

The next step is to compensate for the reduced controller bandwidth at low line voltage. The adaptive gain k_v was introduced to the voltage compensator, which increases the system's gain based on a function of the average input voltage $V_{in(avg)}$. Figure 2.13 shows a controller block diagram of the system including the gain k_v. It is important to place the gain k_v at the input to the voltage compensator instead of at the output, as this ensures that the changes in the gain k_v are effectively low-pass filtered by the voltage compensator. If the gain k_v



(a)



(b)

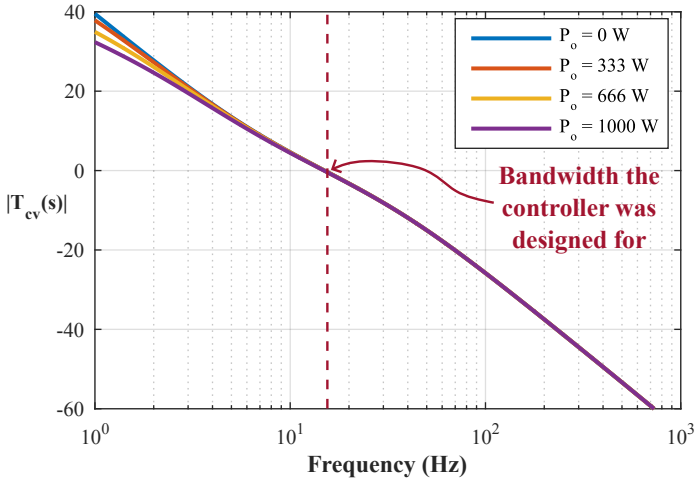
Figure 2.11. Compensated open-loop Bode plot variation with changes in line voltage at P_o = 600 W.

is placed at the output of the voltage compensator, then sudden changes in k_v can result in sudden steps in the on-time, which would heavily distort the line current.

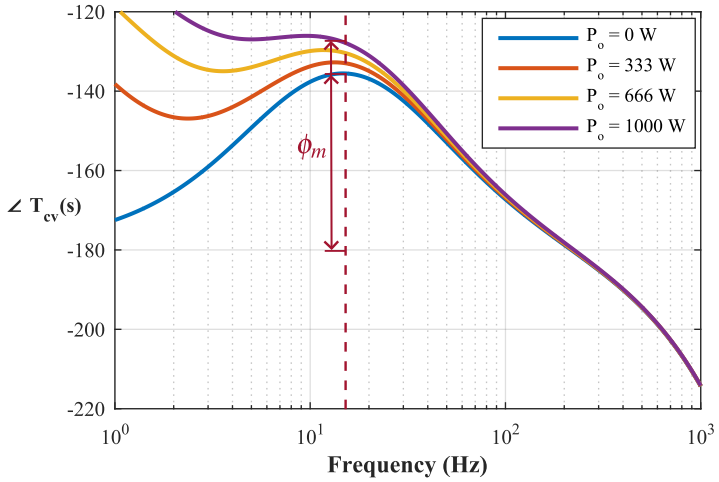
From an examination of (2.27), which was used earlier to calculate the voltage controller gain k_c, it is clear that the adaptive gain must vary inversely with the term $V^2_{in(avg)}$. Hence, the term k_v can be calculated as follows;

$$k_v = \frac{V^2_{in(avg(nom))}}{V^2_{in(avg)}} \tag{2.37}$$

where $V_{in(avg(nom))}$ is the nominal average voltage for which the controller was originally designed. However, using (2.37) requires a division operation which takes a significant amount of computation time when using a low-cost microcontroller. The computation of k_v can be dramatically sped up by using a simple eight-part look-up table (LUT) for the calculation of k_v. Table 2.3 gives a list of the eight different values of k_v for the entire universal-line voltage range. This can be done by separating the universal line input voltage range of 85 V $< V_{in(rms)} \leq$ 265 V into eight separate regions. The average rms voltage of



(a)



(b)

Figure 2.12. Compensated open-loop Bode plot variation with changes in output power at $V_{line(rms)}$ = 230 Vrms.

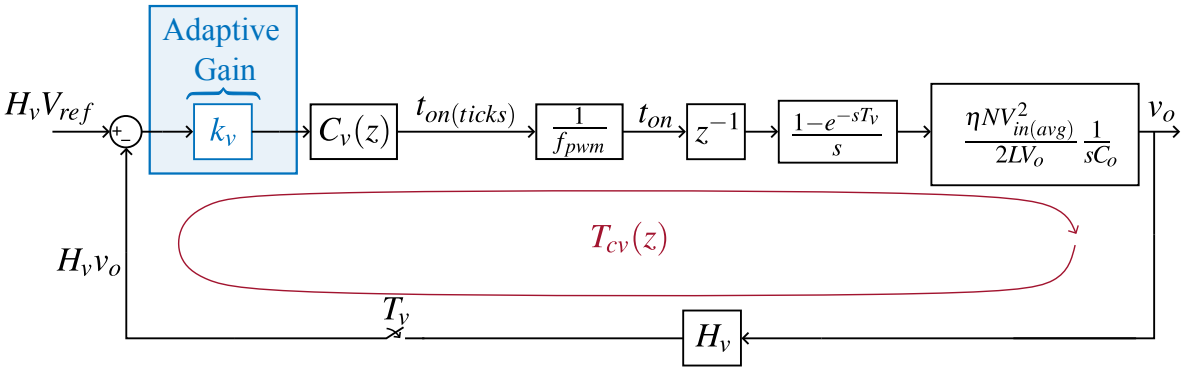


Figure 2.13. Voltage-loop control block diagram including the adaptive gain k_v.

each region, denoted $V_{in(rms(avg))}$, is used to calculate k_v as follows

$$k_v = \frac{V_{in(rms(nom))}^2}{V_{in(rms(avg))}^2} \tag{2.38}$$

where $V_{in(rms(nom))}$ is the nominal input voltage of 230 Vrms. The rms ratio is used, instead of the average values in order to simplify the design procedure.

TABLE 2.3
ADAPTIVE GAIN k_v LOOK-UP TABLE

Region	RMS Voltage Range (Vrms)	$V_{in(rms(avg))}$ (Vrms)	k_v
1	$85 < V_{in(rms)} \leq 107.5$	96.25	5.71
2	$107.5 < V_{in(rms)} \leq 130$	118.75	3.75
3	$130 < V_{in(rms)} \leq 152.5$	141.25	2.65
4	$152.5 < V_{in(rms)} \leq 175$	163.75	1.97
5	$175 < V_{in(rms)} \leq 197.5$	186.25	1.52
6	$197.5 < V_{in(rms)} \leq 220$	208.75	1.21
7	$220 < V_{in(rms)} \leq 242.5$	231.25	0.99
8	$242.5 < V_{in(rms)} \leq 265$	253.75	0.82

2.5.3 Sensing the Average Rectified Input Voltage

The average input voltage must be sensed to execute the look-up table (LUT) described by Table 2.3 . This is done by sensing the instantaneous rectified input voltage v_{in} and passing it through a low-pass second-order digital elliptical filter executed in microcontroller software. An elliptic filter is a suitable choice as it has a very steep attenuation role-off which allows for strong attenuation of the 2nd harmonic component of the rectified input voltage.

Typically the voltage v_{in} must be sensed for other functions, such as detecting line-voltage drop outs, under-voltage protection and over-voltage protection, etc. Therefore, this method does not require additional sense circuitry. The elliptic filter is designed to have a low bandwidth of 7 Hz. There is a trade-off in the selection of the bandwidth. A lower bandwidth allows for better rejection of the 2nd harmonic voltage ripple. A higher bandwidth allows for faster changes in the gain k_v with respect to line-voltage disturbances.

A second-order low-pass elliptic filter has the following transfer function

$$H_e(z) = \frac{V_{in(avg)}(z)}{V_{in}(z)} = \frac{b_{e0} + b_{e1}z^{-1} + b_{e2}z^{-2}}{1 - a_{e1}z^{-1} - a_{e2}z^{-2}} \tag{2.39}$$

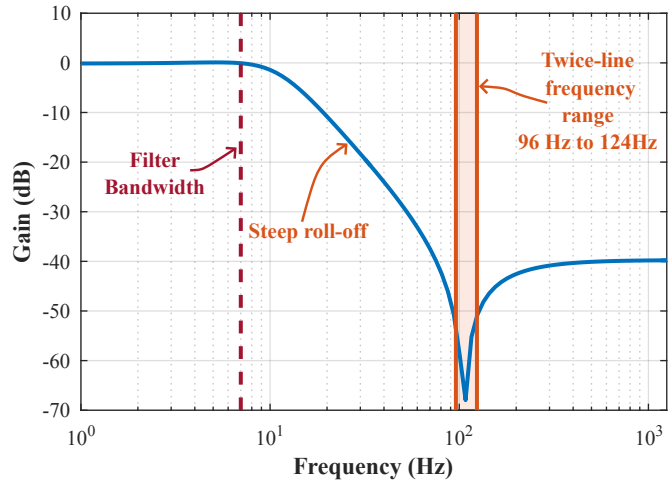
where b_{e0}, b_{e1}, b_{e2}, a_{e1} and a_{e2} are coefficients which define the elliptical filter. The filter was designed to achieve a pass-band attenuation of 0.2 dB and a stop-band attenuation of 40 dB. The sampling frequency for the filter was 2.5 kHz, which is half the voltage compensator sampling frequency. Using a lower sampling frequency for the filter reduces its computational requirements, thus making it more suitable for implementation on a low-cost microcontroller. The filter coefficients were easily calculated using dedicated Matlab elliptic-filter-design functions to calculate the filter coefficients [107]. Table 2.4 gives a summary of the elliptic-filter coefficients.

The magnitude and phase response Bode plots for the filter are given in Figure 2.14. It is

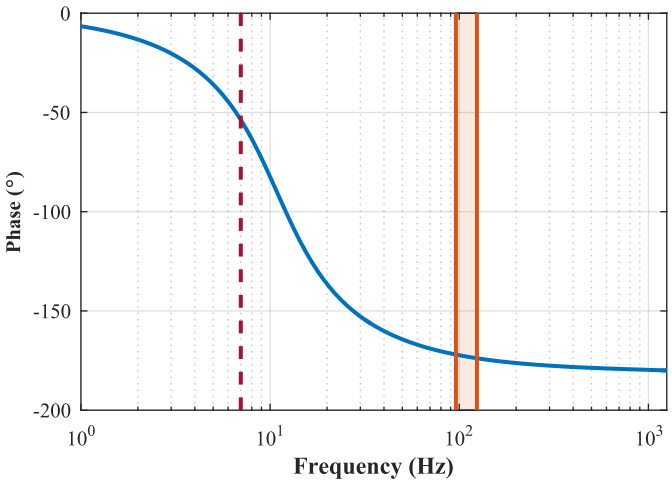
TABLE 2.4
ELLIPTIC FILTER DESIGN PARAMETERS

Parameter	Value
Passband attenuation	0.2 dB
Stopband attenuation	40 dB
Sampling Frequency	2.5 kHz
Filter coefficients, a_{e1}, a_{e2}	1.9661, -0.9668
Filter coefficients, b_{e0}, b_{e1}, b_{e2}	0.0102, -0.0198, 0.0102

clear from the magnitude response of the filter, that as well as providing a steep roll-off in attenuation, the filter also provides excellent attenuation in the 2nd harmonic frequency range from 96 Hz to 124 Hz.



(a)



(b)

Figure 2.14. Elliptic filter (a) magnitude response and (b) phase response.

Equation (2.39) is converted from the $\mathcal{Z}$-domain into the time domain. As a result, the following recursive algorithm is derived, which can be used to implement the filter in

microcontroller software.

$$V_{in(avg)}[n] = b_{e0}v_{in}[n] + b_{e1}v_{in}[n-1] + b_{e2}v_{in}[n-2] + a_{e1}V_{in(avg)}[n-1] + a_{e2}V_{in(avg)}[n-2] \tag{2.40}$$

This recursive algorithm requires fixed-point operations in order to run on a low-cost microcontroller. However, the recursive algorithm defined in (2.40) is not suitable for fixed-point implementation as the filter coefficients are non-integer numbers. Therefore, the coefficients b_{e0}, b_{e1} and b_{e2} are scaled by a gain of 2^{B_e} and the coefficients a_{e1} and a_{e2} are scaled by a gain of 2^{A_e}. This creates a new set of controller coefficients, denoted B_{e0}, B_{e1}, B_{e2}, A_{e1} and A_{e2}, all of which are integers and are suitable for implementation with fixed-point arithmetic. Each of the coefficients B_{e0}, B_{e1}, B_{e2}, A_{e1} and A_{e2} are calculated as follows

$$\begin{aligned} B_{e0} &= \text{round}\langle 2^{B_e} b_{e0} \rangle \\ B_{e1} &= \text{round}\langle 2^{B_e} b_{e1} \rangle \\ B_{e2} &= \text{round}\langle 2^{B_e} b_{e2} \rangle \\ A_{e1} &= \text{round}\langle 2^{A_e} a_{e1} \rangle \\ A_{e2} &= \text{round}\langle 2^{A_e} a_{e2} \rangle \end{aligned} \tag{2.41}$$

where the function round$\langle x \rangle$ denotes rounding a real number x to the nearest integer. Figure 2.15 shows a block diagram of the fixed-point implementation of the filter, including the scaling of the input-voltage sense circuit and the ADC gain, denoted H_{vin}.

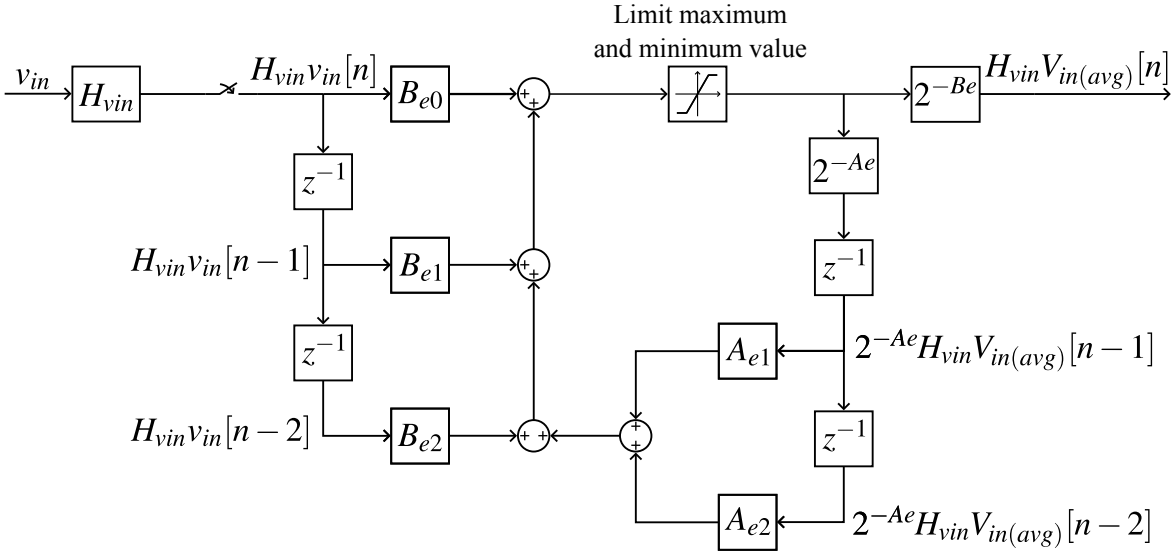


Figure 2.15. Elliptic filter block diagram for a fixed-point implementation.

The terms A_e and B_e are positive integers. This enables the gain blocks that are denoted 2^{-A_e} and 2^{-B_e}, as shown in Figure 2.15, to be easily implemented in microcontroller software

using shift-right bit operations.

The microcontroller software uses signed 32-bit math for the execution of the elliptic filter. The maximum value that any software variable can be is $2^{31}-1$, and if any variable exceeds this value, it overflows positively, causing the filter output to vary widely and out of control. Similarly, if any variable becomes lower than -2^{31}, it overflows negatively creating the same effect.

The term B_e must be selected to be suitably high to minimize quantization error of the filter coefficients, while at the same time, not so high as to cause integer overflow. The maximum value of B_e, for which positive-integer overflow can not occur, is calculated by summing the maximum output of each filter-coefficient-gain block shown in Figure 2.15, and ensuring the result is less than $2^{31}-1$. This results in the inequality obtained in (2.42).

$$\begin{aligned}\max\langle B_{e0}H_{vin}v_{in}[n]\rangle + \max\langle B_{e1}H_{vin}v_{in}[n-1]\rangle + \max\langle B_{e2}H_{vin}v_{in}[n-2]\rangle + \ldots \\ \max\langle 2^{B_e}a_{e1}H_{vin}V_{in(avg)}[n-1]\rangle + \max\langle 2^{B_e}a_{e2}H_{vin}V_{in(avg)}[n-2]\rangle < 2^{31}-1 \quad (2.42)\end{aligned}$$

where the function $\max\langle x\rangle$ denotes the maximum possible value of the variable x.

The input voltage ADC has a 12-bit resolution. Therefore, the maximum value of the input to the filter, denoted $H_{vin}v_{in}[n]$ in Figure 2.15, is $2^{12}-1=4095$, while its minimum value is zero. Since the coefficient b_{e0} is positive, and the maximum possible value of $H_{vin}v_{in}[n]$ is 4095, the term $\max\langle B_{e0}H_{vin}v_{in}[n]\rangle$ simplifies to $2^{B_e}b_{e0}(4095)$. However, since the coefficient b_{e1} is negative, the maximum possible value of the term $\max\langle B_{e1}H_{vin}v_{in}[n-1]\rangle$ occurs when the term $H_{vin}v_{in}[n-1]$ is at its minimum value, which is zero, hence $\max\langle B_{e1}H_{vin}v_{in}[n-1]\rangle = 0$. The maximum value of $H_{vin}V_{in(avg)}[n]$ is assumed to be twice the maximum value of $H_{vin}v_{in}[n]$ to account for any peak overshoot of the filter's output. Hence, the term $\max\langle 2^{B_e}a_{e1}H_{vin}V_{in(avg)}[n-1]\rangle$ simplifies to $2^{B_e}a_{e1}2(4095)$. Applying the same analysis to the remaining terms of (2.44), the inequality can be simplified and solved as follows.

$$2^{B_e}b_{e0}(4095)+0+2^{B_e}b_{e2}(4095)+2^{B_e}a_{e1}2(4095)+0<2^{31}-1$$

$$2^{B_e}(4095)(b_{e0}+b_{e2}+2a_{e1})<2^{31}-1$$

$$2^{B_e}<\frac{2^{31-1}}{(4095)(b_{e0}+b_{e2}+2a_{e1})}$$

$$B_e<\log_2\left(\frac{2^{31}-1}{(4095)(b_{e0}+b_{e2}+2a_{e1})}\right)$$

$$B_e<\log_2\left(\frac{2^{31}-1}{(4095)(0.0102+0.0102+2(1.9661))}\right)$$

$$B_e < 18.0172 \tag{2.43}$$

A similar analysis must be performed to check that no variable of the filter can overflow negatively. This results in the following inequality.

$$\begin{aligned}\min\langle B_{e0}H_{vin}v_{in}[n]\rangle + \min\langle B_{e1}H_{vin}v_{in}[n-1]\rangle + \min\langle B_{e2}H_{vin}v_{in}[n-2]\rangle + \ldots \\ \min\langle 2^{B_e}a_{e1}H_{vin}V_{in(avg)}[n-1]\rangle + \min\langle 2^{B_e}a_{e2}H_{vin}V_{in(avg)}[n-2]\rangle > -2^{31}\end{aligned} \tag{2.44}$$

where the function $\min\langle x\rangle$ denotes the minimum possible value of the variable x. This inequality can be solved as follows.

$$0 + 2^{B_e}b_{e1}(4095) + 0 + 0 + 2^{B_e}a_{e2}2(4095) + 0 > -2^{31}$$

$$2^{B_e}(4095)(b_{e1} + 2a_{e2}) > -2^{31}$$

$$2^{B_e} < \frac{-2^{31}}{(4095)(b_{e1} + 2a_{e2})}$$

$$B_e < \log_2\left(\frac{-2^{31}}{(4095)(b_{e1} + 2a_{e2})}\right)$$

$$B_e < \log_2\left(\frac{-2^{31}}{(4095)(-0.0198 + 2(-0.9668))}\right)$$

$$B_e < 19.0340 \qquad \therefore \qquad B_e = 18 \tag{2.45}$$

Therefore, the term B_e is set to $B_e = 18$ to satisfy both (2.44) and (2.45), thus ensuring neither positive or negative integer overflow can occur.

The term A_e must be set suitably high to minimize the quantization error associated with the rounding of the filter coefficients a_{e1} and a_{e2}, while also being as low as possible to minimise the integer rounding associated with shift-right bit operations of the gain block denoted 2^{-Ae} in Figure 2.15. It is possible to calculate the effect of the coefficient-quantization error on the filter's magnitude response by replacing the filter coefficients b_{e0}, b_{e1}, b_{e2}, a_{e1} and a_{e2}, with the fixed-point coefficients B_{e0}, B_{e1}, B_{e2}, A_{e1} and A_{e2}. Therefore, the filter transfer function described in (2.39), can be re-written as follows

$$H_e(z) = 2^{A_e - B_e}\frac{B_{e0} + B_{e1}z^{-1} + B_{e2}z^{-2}}{2^{A_e} - A_{e1}z^{-1} - A_{e2}z^{-2}} \tag{2.46}$$

The transfer function can be calculated for different values of A_e in order to determine a value of A_e which has acceptably low coefficient-quantization error. Figure 2.16 shows the filter transfer function calculated for three different values of A_e, and the ideal transfer function

with no filter-coefficient quantization error calculated using (2.39). When A_e is set to a low value, such as when $A_e = 5$ and $A_e = 10$, there is excessive coefficient-quantization error, and as a result, the elliptic filter's magnitude response does not match the ideal magnitude response. When A_e is set to 14, there is a good match between the desired and actual magnitude response, hence this value was used in the design. Setting A_e to a higher value would result in greater computational-error associated with right-shift bit operations, with no improvement in the filter-coefficient quantization error. Hence A_e is not made larger than 14.

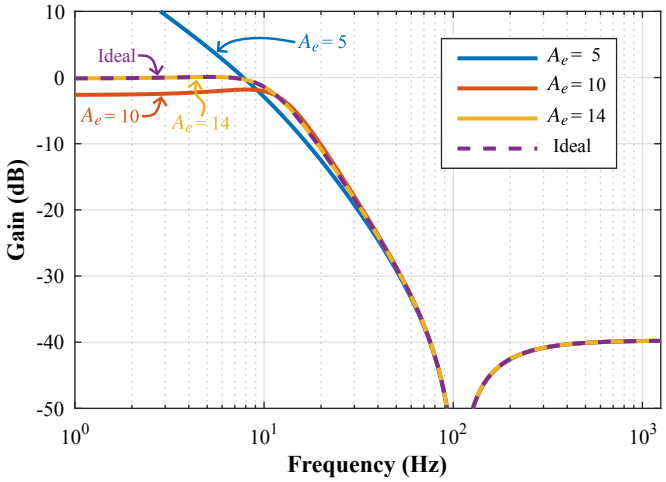


Figure 2.16. Elliptic filter magnitude Bode plot variation with different values for A_e.

With an appropriate value set for the term A_e, all filter coefficients for a fixed-point implementation can be calculated using (2.41). A list of the fixed-point filter coefficients are given in Table 2.5.

TABLE 2.5
ELLIPTIC FILTER FIXED-POINT COEFFICIENTS

Parameter	Value
Input voltage ADC-sensor gain, H_{vin}	10.51
Coefficient, B_e	18
Coefficient, A_e	14
Coefficient, B_{e0}	2685
Coefficient, B_{e1}	-5181
Coefficient, B_{e2}	2685
Coefficient, A_{e1}	32213
Coefficient, A_{e2}	-15841

2.6 Voltage Compensator Design using Fixed-Point Math

In this section a voltage compensator is designed using fixed-point math. The voltage compensator is designed to have a bandwidth of 15 Hz and an injected phase of 45° at 230 Vrms. The output voltage sampling rate is set to 200 µs, which corresponds to a frequency of 5 kHz. The controller coefficients are calculated using the design procedure, described earlier in Section 2.3, for the 3-channel BCM PFC converter with the circuit parameters listed in Table 2.1. This results in the set of controller coefficients listed in Table 2.6.

TABLE 2.6
VOLTAGE COMPENSATOR DESIGN PARAMETERS

Parameter	Value
Cross-over frequency, ω_c	$2\pi 15$ rad/s
Voltage sampling period, T_v	200 µs
PWM resolution, f_{pwm}	96 MHz
Sensor-adc gain, H_v	8.11
Injected phase , ϕ_{max}	45°
Controller coefficients, $b_{v0},\ b_{v1},\ b_{v2}$	0.01847, 0.0001436, -0.01832
Controller coefficients, $a_{v1},\ a_{v2}$	1.956, -0.9555

The filter coefficients must be integer values to be suitable for a fixed-point implementation. Therefore, the coefficients b_{v0}, b_{v1} and b_{v2} are scaled by a gain of 2^{B_v}, while the coefficients a_{v1} and a_{v1} are scaled by a gain of 2^{A_v}. This creates a new set of controller coefficients, denoted B_{v0}, B_{v1}, B_{v2}, A_{v1} and A_{v2}, which are integers and are suitable for implementation with fixed-point operations. Each of the coefficients B_{v0}, B_{v1}, B_{v2}, A_{v1} and A_{v2} are calculated as follows

$$\begin{aligned} B_{v0} &= \text{round}\langle 2^{B_v} b_{v0} \rangle \\ B_{v1} &= \text{round}\langle 2^{B_v} b_{v1} \rangle \\ B_{v2} &= \text{round}\langle 2^{B_v} b_{v2} \rangle \\ A_{v1} &= \text{round}\langle 2^{A_v} a_{v1} \rangle \\ A_{v2} &= \text{round}\langle 2^{A_v} a_{v2} \rangle \end{aligned} \tag{2.47}$$

where the terms A_v and B_v are constant integers. Similarly, the adaptive voltage compensator gain k_v is converted to an integer value as follows:

$$K_v = \text{round}\langle 2^{A_k} k_v \rangle \tag{2.48}$$

where the terms A_k is a constant integer.

The terms A_v, B_v and A_k are calculated to minimise the coefficient-quantization error and computational error, similar to the fixed-point design of the elliptic filter carried out in

Section 2.5.3. The calculation of these terms is described fully in Appendix B.

A block diagram of the voltage compensator implemented using fixed-point math is given in Figure 2.17. The voltage compensator block diagram includes the output-voltage gain H_v and the adaptive gain.

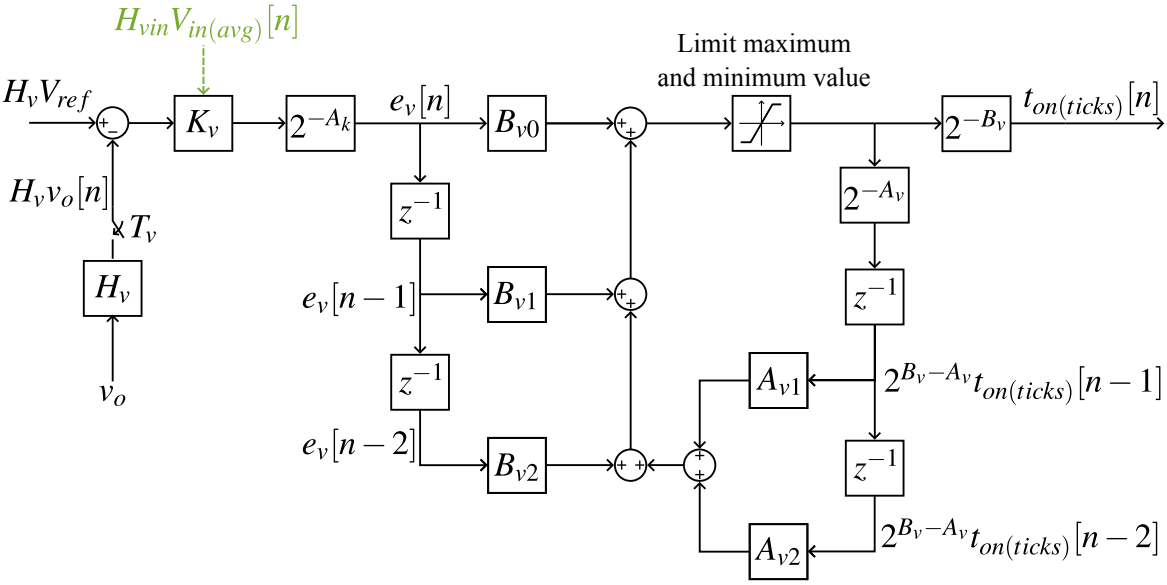


Figure 2.17. Voltage compensator block diagram for a fixed-point implementation.

Table 2.7 gives a full-list of the voltage compensator fixed-point coefficients, which are used in microcontroller software to define the fixed-point recursive algorithm implemented by the controller.

TABLE 2.7
VOLTAGE CONTROLLER FIXED-POINT COEFFICIENTS

Parameter	Value
Input voltage adc-sensor gain, H_v	8.11
Coefficient, A_k	16
Coefficient, B_v	18
Coefficient, A_v	10
Coefficient, B_{v0}	4841
Coefficient, B_{v1}	38
Coefficient, B_{v2}	-4803
Coefficient, A_{v1}	2002
Coefficient, A_{v2}	-978

2.7 Voltage Compensator With an Adaptive Notch Filter

In this section, an adaptive notch filter is designed in order to remove the 2nd harmonic ripple from the output of the voltage compensator. This results in reduced input current distortion and improved power factor, but at the cost of a more complicated controller. The filter must work over the line-frequency range of 48 Hz to 62 Hz. Thus, the notch filter is designed to adaptively change its coefficients based on the sensed line frequency of the applied input voltage.

2.7.1 Single-Frequency Notch Filter

The first step in the design process for the adaptive notch filter is to design a notch filter which works at a single line frequency. The transfer function of a digital notch filter [108] with unity dc gain, a notch at the 2nd harmonic frequency, and the same execution rate as the voltage compensator of $\frac{1}{T_v}$, is given by

$$H_n(z) = \left(\frac{1 - 2r\cos(4\pi f_L T_v) + r^2}{2 - 2\cos(4\pi f_L T_v)} \right) \frac{1 - 2\cos(4\pi f_L T_v) z^{-1} + z^{-2}}{1 - 2r\cos(4\pi f_L T_v) z^{-1} + r^2 z^{-2}} \tag{2.49}$$

where r is a constant that determines the selectivity of the filter. As r tends towards unity the filter becomes more selective. Figure 2.18 shows the magnitude response and phase response of the notch filter $H_n(z)$ for different values of r. As the filter becomes more selective, its stopband becomes more narrow, and the phase delay introduced by the filter is reduced. It is desirable to have the phase delay introduced by the filter to be as small as possible, so that the voltage compensator's phase margin remains unchanged. However, if r becomes too close to unity, the stopband becomes too narrow, and the filter becomes more prone to the quantization error of the filter coefficients. Hence, the value of r is chosen to be $r = 0.97$, to provide a good trade-off between the stopband width and the phase delay.

In order to derive a suitable recursive algorithm to implement the notch filter, the filter's transfer function described by (2.49) is rewritten in the form

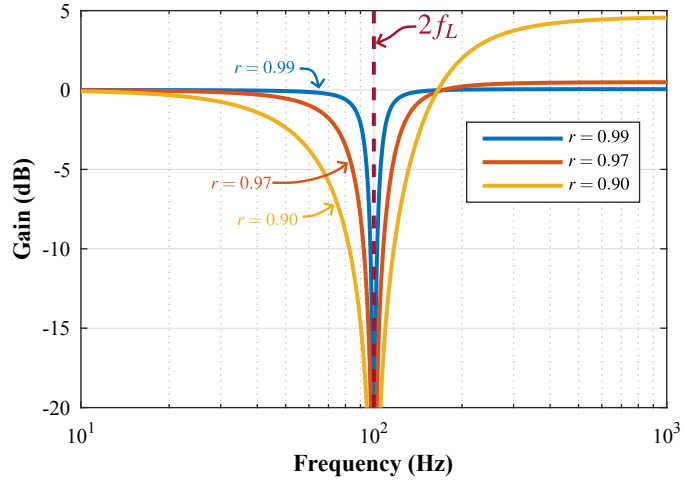
$$H_n(z) = \frac{b_{n0} + b_{n1} z^{-1} + b_{n2} z^{-2}}{1 - a_{n1} z^{-1} - a_{n2} z^{-2}} \tag{2.50}$$

where the coefficients b_{n0}, b_{n1}, b_{n2}, a_{n1} and a_{n2} are defined as follows

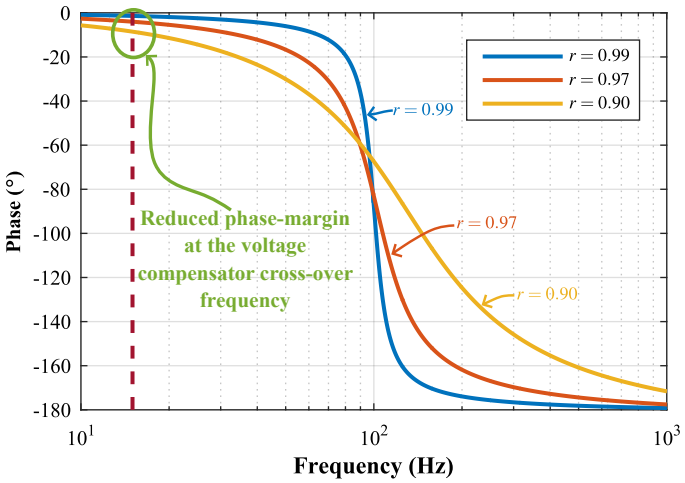
$$b_{n0} = b_{n2} = \left(\frac{1 - 2r\cos(4\pi f_L T_v) + r^2}{2 - 2\cos(4\pi f_L T_v)} \right)$$

$$b_{n1} = -\left(\frac{1 - 2r\cos(4\pi f_L T_v) + r^2}{2 - 2\cos(4\pi f_L T_v)} \right) 2\cos(4\pi f_L T_v)$$

$$a_{n1} = 2r\cos(4\pi f_L T_v)$$



(a)



(b)

Figure 2.18. Notch filter magnitude and phase response variation with coefficient r.

$$a_{n2} = -r^2 \tag{2.51}$$

The following recursive algorithm can be defined to implement the notch filter by converting (2.50) to the time-domain.

$$y_n[n] = b_{n0}x_n[n] + b_{n1}x_n[n-1] + b_{v2}x_n[n-2] + a_{n1}y_n[n-1] + a_{n2}y_n[n-2] \tag{2.52}$$

where $x_n[n]$ is the notch filter input and $y_n[n]$ is the notch filter output. Table 2.8 gives a list of the notch filter design parameters and filter coefficients for a line frequency of 50 Hz.

2.7.2 Notch Filter Fixed-Point Implementation

The recursive algorithm defined in (2.52) is suitable for floating-point math. However, in order to implement the filter on a low-cost microcontroller, it must be implemented using fixed-point math.

Therefore, the coefficients b_{n0}, b_{n1} and b_{n2} are scaled by a gain of 2^{B_n}, while the coefficients a_{n1} and a_{n2} are scaled by a gain of 2^{A_n}. This creates a new set of controller coefficients,

TABLE 2.8
NOTCH FILTER DESIGN PARAMETERS

Parameter	Value
Line Frequency, f_L	50 Hz
Voltage sampling period, T_v	200 µs
Selectivity coefficient, r	0.97
Filter coefficients, $b_{n0},\ b_{n1},\ b_{n2}$	1.027, -2.037, 1.027
Filter coefficients, $a_{n1},\ a_{n2}$	1.925, -0.9409

denoted B_{n0}, B_{n1}, B_{n2}, A_{n1} and A_{n2}, which are integers, and are suitable for implementation with fixed-point arithmetic. Each of the coefficients B_{n0}, B_{n1}, B_{n2}, A_{n1} and A_{n2} are calculated as follows:

$$\begin{aligned} B_{n0} &= \text{round}\langle 2^{B_n} b_{n0} \rangle \\ B_{n1} &= \text{round}\langle 2^{B_n} b_{n1} \rangle \\ B_{n2} &= \text{round}\langle 2^{B_n} b_{n2} \rangle \\ A_{n1} &= \text{round}\langle 2^{A_n} a_{n1} \rangle \\ A_{n2} &= \text{round}\langle 2^{A_n} a_{n2} \rangle \end{aligned} \tag{2.53}$$

where the terms A_n and B_n are positive integers. The notch filter is placed at the output to the voltage compensator. Figure 2.19 shows a block diagram representation of the voltage compensator and notch filter together. The output of the voltage compensator, which is the input to the notch filter and is denoted $x_n[n]$, is scaled by a gain of 2^{A_x} where A_x is a positive integer. This is done to reduce the computational error. A gain of 2^{-A_x} is added to the output of the notch filter to maintain the notch filter's unity dc gain. The output to the notch filter is the computed on-time in ticks $t_{on(ticks)}[n]$, which is similar to the voltage compensator designed in Section 2.6, except that the 2$^{\text{nd}}$ harmonic component that was present in the on-time is effectively removed by the notch filter. All voltage compensator coefficients remain unchanged from those designed in Section 2.6.

The terms A_n, B_n and A_x must be defined to calculate the controller coefficients. The calculation of these terms is fully described in Appendix B. With these terms now defined, it is possible to calculate the fixed-point notch filter coefficients using (2.53). A full list of all notch filter fixed-point coefficients is presented in Table B.2.

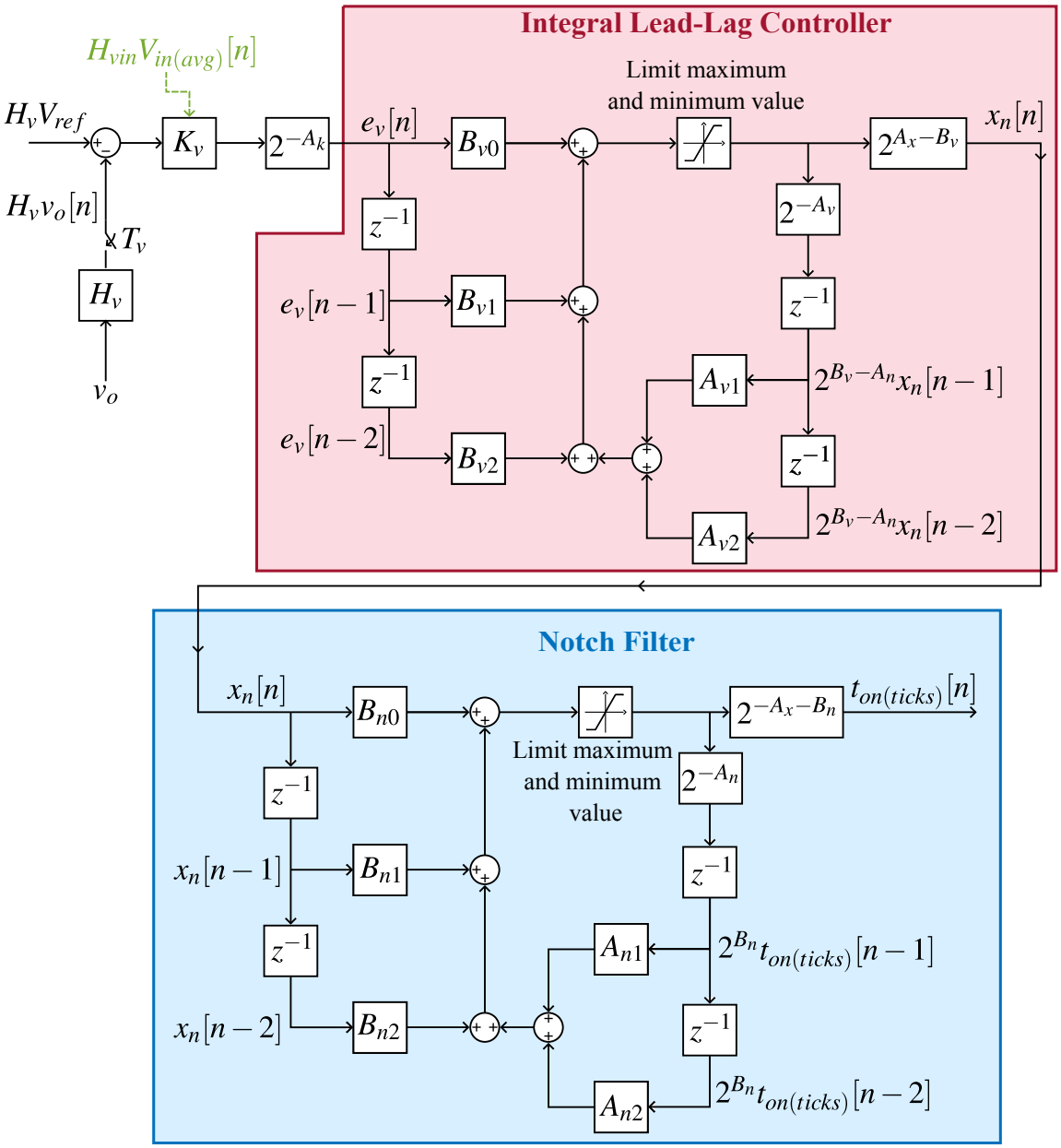


Figure 2.19. Notch filter block diagram for a fixed-point implementation.

TABLE 2.9
NOTCH-FILTER FIXED-POINT COEFFICIENTS

Parameter	Value
Coefficient, A_x	4
Coefficient, B_n	13
Coefficient, A_n	11
Coefficient, B_{n0}	8414
Coefficient, B_{n1}	-16695
Coefficient, B_{n2}	8414
Coefficient, A_{n1}	3942
Coefficient, A_{n2}	-1927

2.7.3 Adaptive Notch Filter

The notch filter that has been designed so far works at a single line frequency only. However, the filter must be able to handle a universal line voltage input, with a line-frequency variation of 48 Hz to 62 Hz. The coefficients b_{n0}, b_{n1}, b_{n2} and a_{n1}, which are described in (2.51), are all functions of the line frequency f_L. Therefore, these coefficients need to be recalculated at a different line frequency in order for the filter to work at that different line frequency.

The coefficients b_{n0} and b_{n2} are approximately equal to 1 over the range of possible line frequencies as seen in Figure 2.20, which plots these coefficients over the line frequency range. Therefore, it's possible to keep these coefficients unchanged, and only recalculate the

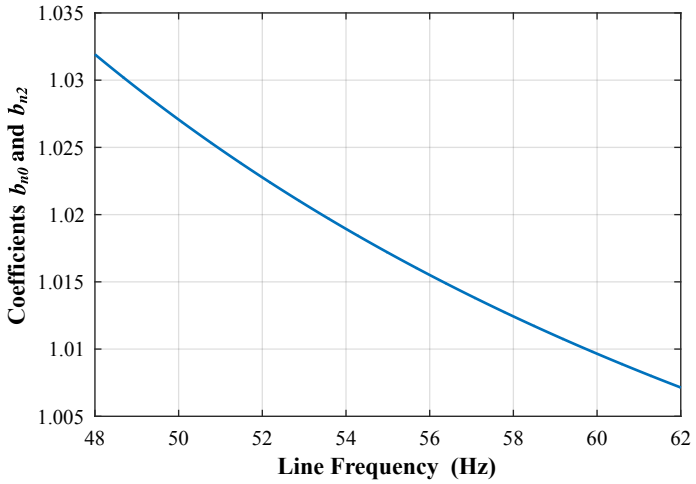


Figure 2.20. Notch-filter coefficients, b_{n0} and b_{n2}, variation with line frequency.

coefficients b_{n2} and a_{n1} for the filter to operate at a different line frequency.

By this approach the fixed-point coefficients B_{n1} and A_{n1} can be recalculated at each possible line frequency. However, as it is easier to sense the line period, the terms B_{n1} and A_{n1} are instead recalculated over a line-period range corresponding to the line frequencies in the range 48 Hz to 62 Hz. This requires sensing the line period. The line period T_L can be sensed by counting the number of input voltage ADC samples which occur every half-line period. This method is depicted in Figure 2.21, where the number of input voltage ADC samples is counted at a sampling rate of T_v, starting when the input voltage v_{in} surpasses a threshold denoted $V_{in(th)}$ and ending when v_{in} surpasses the same threshold for the second instant. For accurate sensing of the line period the input voltage is sampled with a sampling period, denoted T_v, that is much smaller than the line voltage's line period. The same sampling period as the one used to sense the output voltage is used to keep the firmware design simple, which was T_v = 200 µs, corresponding to a sampling frequency of 5 kHz.

The line frequency range of 48 Hz to 62 Hz corresponds to a line period range of 16.13 ms to 20.83 ms. A line frequency of 48 Hz corresponds to 52 input voltage samples and a line voltage of 62 Hz corresponds to 41 input voltage samples, with a total of 12 different

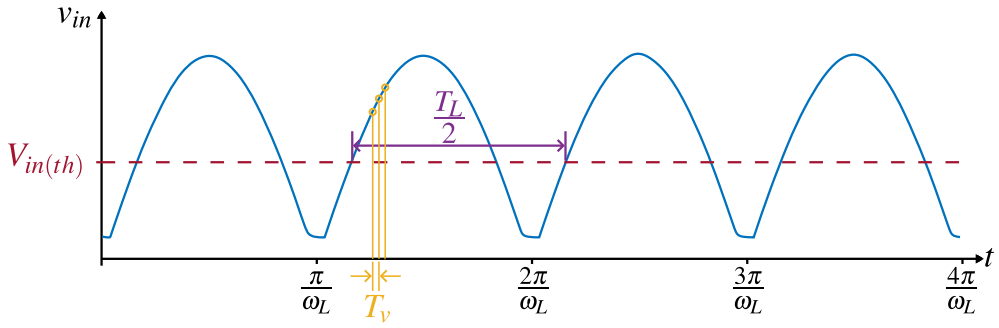


Figure 2.21. Method to sense the line period by sampling the input voltage.

possible number of samples over line-frequency range.

The universal line period was divided into 12-equally spaced points, corresponding to every 2 additional input voltage samples as follows

$$N_{vin} = 41,\ 42,\ 43,\ \ldots\ 50,\ 51,\ 52 \tag{2.54}$$

where N_{vin} denotes the number of input voltage samples which have been recorded in a half-line period. Each of the possible values of N_{vin} corresponds to a line period of $T_L = 2N_{vin}T_{vin}$. Thus, the coefficients A_{n1} and B_{n1} must be re-calculated at each of the following line periods:

$$T_L = 16.4,\ 16.8,\ 17.2,\ \ldots\ 20,\ 20.4,\ 20.8\ \text{ms} \tag{2.55}$$

The coefficients A_{n1} and B_{n1} can be recalculated using the coefficient b_{n0} defined for the single-frequency notch filter, as follows

$$B_{n1} = \text{round}\left\langle 2^{B_v} b_{n0} 2\cos\left(4\pi\frac{T_v}{T_L}\right)\right\rangle$$
$$A_{n1} = \text{round}\left\langle 2^{A_v} 2r\cos\left(4\pi\frac{T_v}{T_L}\right)\right\rangle$$

This results in 12 different possible values for the coefficient B_{n1} and A_{n1}, as follows

$$B_{n1} = 16629, 16638, 16647, \ldots, 16694, 16699, 16704 \tag{2.56}$$
$$A_{n1} = 3927, 3929, 3931, \ldots, 3942, 3943, 3944$$

This method lends itself heavily to being executed with a microcontroller, as the different possible values for the terms A_{n1} and B_{n1}, can be stored in two separate arrays that are 12 words in length, and the number of input voltage samples recorded can be used as the array index term, which determines which word in the array to use.

The end result of this method is that the notch filter can sense the current operating line period and then adapt its coefficients in a computationally inexpensive way, by using

arrays as LUTs to determine the coefficients that need to change. Therefore, the notch filter's magnitude response changes as the number of recorded input voltage samples change. This variation of the notch filter's magnitude response is shown in Figure 2.22 for three different possible sensed line frequencies.

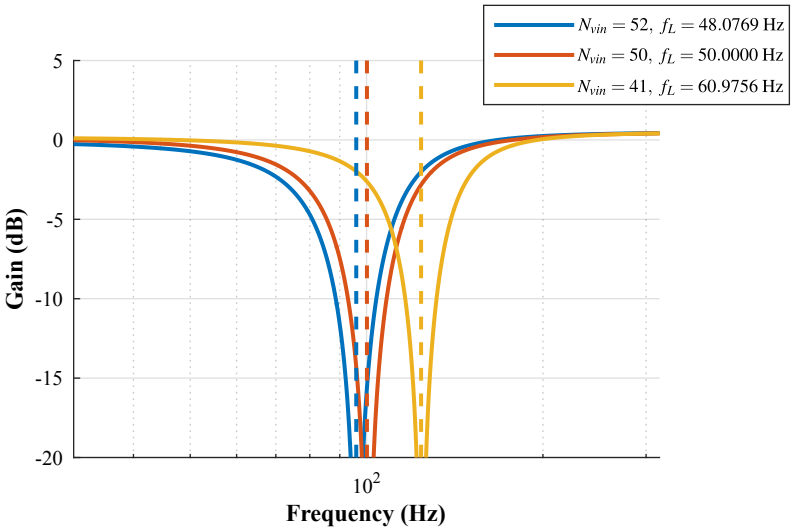


Figure 2.22. Notch-filter magnitude response, calculated at different values of N_{vin}.

2.8 Firmware Design

This section describes the firmware used to implement the control algorithms for the multi-channel BCM boost converter prototype. Two different prototypes were developed in this work, one rated for an output power of 600 W and the other for an output power of 1 kW. The 600 W 2-channel BCM boost converter was developed using a TMS320f28069 microcontroller from Texas instruments. The 1 kW 3-channel BCM boost converter prototype was developed using an XMC1402-Q040X0032 microcontroller from Infineon Technologies. The more expensive TMS320f28069 microcontroller has a faster CPU clock frequency of 90 Mhz, a more advanced CPU instruction set, and a floating-point math unit. The XMC1402-Q040X0032 microcontroller, on the other hand, has a slower CPU clock frequency of 48 Mhz, a less advanced CPU instruction set, and no floating-point math unit, but it is cheap, and so is more desirable to use for commercial applications.

The 600 W prototype was used to measure the open-loop voltage-loop Bode plot for a BCM boost converter. The prototype was also used again in Chapter 5 to implement an ACMC scheme. The 1 kW prototype was used to implement the control algorithms described in the other chapters, and so, the firmware design for the 1 kW prototype is described here. The firmware design for the 600 W prototype is nearly identical, except that the control algorithms are implemented with floating-point math, and the interleaved boost converter has only 2 channels instead of 3.

2.8.1 Interfacing the Microcontroller with the Hardware

Figure 2.23 shows a simplified block diagram of the circuits used to interface the microcontroller with the interleaved BCM boost converter, and the critical control algorithms executed in microcontroller software. The interfacing circuits consist of voltage-sense circuits to sense the input voltage and output voltage. These sense circuits are implemented using resistive potential-divider networks. A shunt resistor and differential-amplifier op-amp circuit are used to sense the input current. Sensing the output voltage is required in order to calculate the on-time, while sensing the input current and input voltage is required for fault-detection algorithms. As well as this, a separate ZCD circuit is used for each boost converter channel to detect when the inductor current of each channel reaches zero. This circuit interfaces with the PWM peripheral on the microcontroller to trigger the instant when the MOSFET of each channel turns on. The ZCD circuit is covered in more detail in Section 3.2.1. The microcontroller creates the PWM signals that trigger the turn-on instant of each MOSFET. The current rating of the microcontroller pins is not high enough to drive the boost MOSFETs, and so two FAN3224 dual low-side gate drive ICs were required to drive the 3 MOSFETs [109]. The prototype is also used a low-power flyback converter to create a 12 V rail from the 400 V output voltage to power the gate driver ICs. Separate 12 V to 5 V linear voltage regulators

were used to create suitable power sources to drive the microcontroller and analog op-amp used for the current-sense circuit.

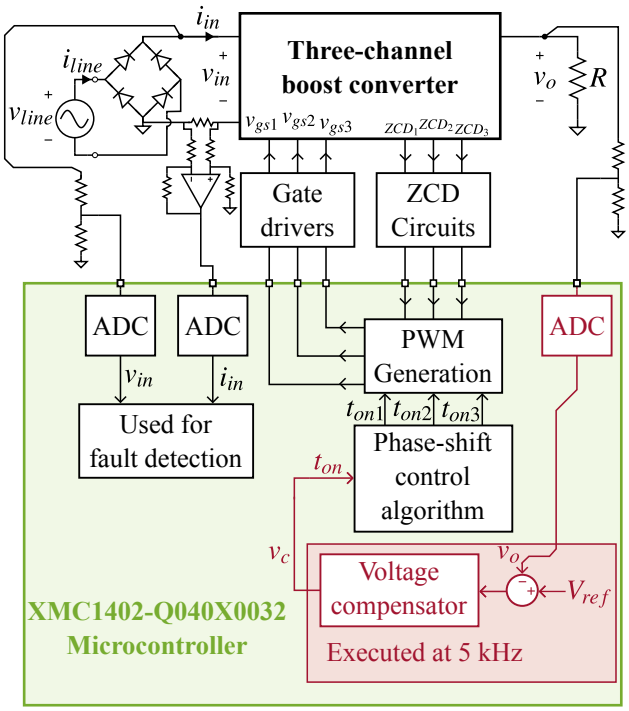


Figure 2.23. Simplified block diagram of the microcontroller and the boost converter power stage.

2.8.2 State-Machine Description

The microcontroller firmware is responsible for executing the control algorithms which regulate the output voltage, and the phase-shift control algorithms which maintain the correct interleaving between separate boost converter channels. The phase-shift control is covered in Chapter 3. Additionally, the microcontroller executes different fault-detection algorithms and must execute a soft-start algorithm to allow the converter to safely charge the large output capacitors when the mains voltage is first applied. The state-machine used to implement these functions is shown in Figure 2.24. The state machine has 4 different states as follows,

Initialization - This state occurs when the microcontroller is first powered up, or when a microcontroller reset occurs. When the mains voltage is first applied to the input, an inrush-current-limiting resistor is used to limit the current which charges the large output capacitors of the boost converter to the peak of the line voltage. As the output voltage charges, the flyback converter starts-up, and creates the 12 V rail. This rail creates the 5 V to power the microcontroller from the linear voltage regulator, thus causing the state machine to transition to the initialization state. In this state, the microcontroller runs the peripheral initialization code. The initialization code defines the microcontroller peripheral operation, the function of different microcontroller pins, the CPU clock frequency, and how the interrupts are enabled and triggered, etc.

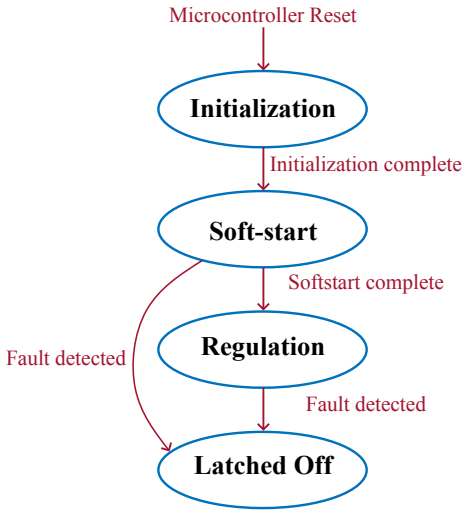


Figure 2.24. Microcontroller software state-machine diagram.

Soft-Start - Once the initialization code is complete, the state machine transitions to the soft-start state. The microcontroller checks if the output voltage has charged to the peak of the line voltage, and that the line voltage is within the universal-line range. The soft-start relay, which is in parallel with the inrush current limiter, is then closed. The relay creates a low impedance path for current to flow through during normal operation. After the relay is turned on, the interrupt functions running the voltage-compensator code and phase-shift control algorithm are enabled. An interrupt is a signal that is used to alert the CPU to stop what it is doing and run a certain interrupt function. When this function is complete the CPU goes back to the code it was executing before the interrupt was called. Interrupt functions are used to execute the voltage compensator and phase-shift control algorithms, because these functions must be implemented at fixed execution rates. The phase-shift control interrupt is run at a faster execution rate than the voltage-compensator algorithm, hence two different interrupts are used to execute both algorithms. The voltage-compensator interrupt is described in the next section in more detail, and the phase-shift control interrupt is discussed in the next chapter. Timer peripherals are used to trigger the instant at which the voltage-loop interrupt and phase-shift control interrupt are called. After the interrupts are enabled, the output-voltage reference signal V_{ref} is initially set to the peak of the line voltage, and is then allowed to slowly ramp to its steady-state value. This ensures that the output voltage is slowly charged, and that the converter does not pull excessively high line current during start-up.

Regulation - After the output-voltage reference has ramped to its final value, the state machine transitions to the regulation state. In this state, the microcontroller checks if a fault flag has been set in an infinite while loop. The fault flag is simply a Boolean variable, where 1 represents the fact that a fault has occurred, and 0

represents no fault has occurred. The fault flag is set by either a firmware fault-detection algorithm executed within one of the interrupt functions, or a hardware fault. The microcontroller comparator peripherals are used for direct hardware-fault detection. This is implemented by feeding the input-current and output-voltage sense signals into the the positive terminal of the analog comparator within the microcontroller. The negative terminal is connected to a fixed threshold voltage created from a potential divider from the 5 V power rail. If the input-current or output-voltage sense signals exceed the threshold voltage, the respective comparator output is pulled high. The comparator output is used to directly disable the PWM outputs, independent of the CPU. The software is also designed to check if either the comparator has gone high, and if so, set the fault-detected flag. This hardware-fault-detection mechanism is useful as it can work even in the case where the microcontroller code freezes.

Latched off - This state is entered if the fault detection flag is set. If so, the PWM outputs are set low to force all MOSFETs off, both interrupts are disabled, and the code is frozen in an infinite while loop. As a result, the converter stops switching and remains idle until the microcontroller is reset. It is also possible to implement an auto-restart feature by forcing a microcontroller to reset after a fault is detected.

2.8.3 Voltage-Feedback Interrupt Description

The voltage-feedback interrupt is responsible for several important functions. A full software-flow block diagram that describes this interrupt is provided in Figure 2.25. The interrupt is executed at the sampling period of the output voltage T_v, which corresponds to a rate of 5 kHz for the 3-channel 1 kW prototype. The interrupt begins by reading the output and input voltages from the the corresponding ADC registers. The recursive algorithms described in Figure 2.19 are then implemented, which execute the voltage compensator and notch filter code to calculate the converter's on-time. The on-time is used in the phase-shift control algorithm to calculate the on-time of each individual channel, so that each PWM peripheral register can be updated.

The voltage-loop interrupt is also used to run the input-voltage elliptic-filter recursive equation which calculates $V_{in(avg)}$. An identical filter is used to calculate the average rectified input current. Both filters are executed at the slower rate of 2.5 kHz, by using a 2-case switch statement, which reduces the computational requirements of both filters.

Next, an 8-case switch statement is used to execute other required functions. Each case of this switch statement is executed at a rate of 5 kHz divided by 8, or 625 Hz. This greatly reduces the computational requirements of the algorithms executed within the switch statement, as the microcontroller has more time to execute each algorithm. This switch statement is used to update the adaptive voltage compensator gain k_v. Similarly, an adaptive gain used in the phase-shift control algorithm is updated here. The notch filter coefficients

are also updated.

The switch statement is also used to execute different fault-detection algorithms, such as, if the line voltage drops outside the universal input voltage range for an excessively long time, or if an output voltage tracking failure occurs, or if the output power exceeds it's steady-state rating for too long. The output power is calculated by multiplying the average rectified input current by the average rectified input voltage, which in turn is calculated using the elliptic filters from the 2-case switch statement. If any fault is detected, the PWM outputs are immediately disabled and the fault-detected flag is set high.

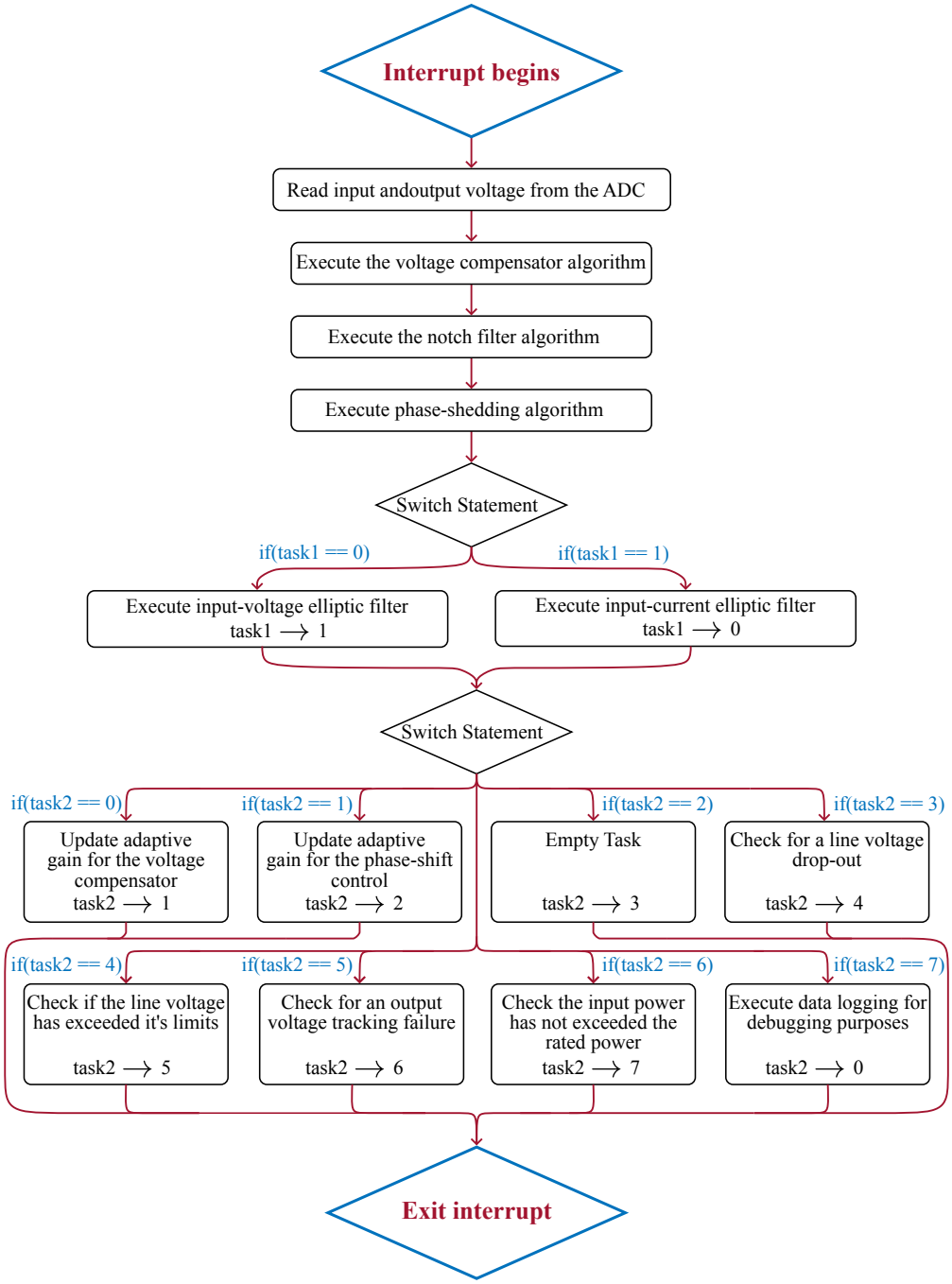


Figure 2.25. Software-flow block diagram description of the voltage-feedback interrupt function.

2.9 Experimental Results

A 1 kW 3-channel BCM boost converter prototype was built to validate the digital control algorithms described in this chapter. An image of this prototype is given in Figure 2.26. The ac input voltage is connected to the 3-pin barrier terminal block connector, shown on the upper left-hand side of the photo. The 3 pins correspond to the live, neutral and earth wires. The ac input passes through a fuse, followed by the EMI filter, before reaching the bridge rectifier, shown in the bottom left corner of the image. The three ferrite inductors, MOSFETs and power diodes, that make up the 3 channels of the multi-channel boost converter, are shown toward the lower right-hand side of the image. The board also contains 4 large 220 µF electrolytic capacitors which make up the output capacitor. The flyback converter in the upper right-hand corner is used to convert the 400 V output to the 12 V rail and powers the gate drives, relay and microcontroller. Just below the flyback converter there is a 2-pin terminal barrier connector, which connects the converters output voltage to an external load.



Figure 2.26. An image of the 3-channel 1 kW boost converter.

The 1 kW prototype uses an Infineon XMC1402Q040 microcontroller to implement the digital control scheme. This is a low-cost microcontroller with limited computational power. The microcontroller was located on the underside of the PCB board.

A second 2-channel 600 W prototype was also built. This prototype is shown in Figure 2.27. The 600 W prototype used the same semiconductor switches, diodes and boost-inductor value as the 1 kW prototype. The main difference with the 600 W prototype is that a more powerful TMS320f28069 microcontroller from Texas Instruments was used. The higher-power microcontroller was used to measure the open-loop Bode plots of the power stage and validate the theoretical derivation of the transfer function described by (2.15). It is also used again in Chapter 4 to implement a more computationally expensive digital control scheme

using floating-point math.

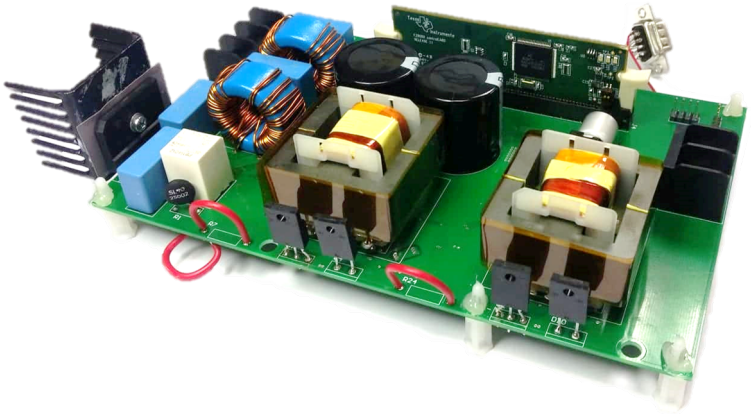


Figure 2.27. An image of the 2-channel 600 W boost converter.

2.9.1 Model Verification

The open-loop Bode plots of the system were calculated theoretically using (2.15) and also measured experimentally on the 600 W BCM boost converter. The theoretical and measured results were compared to each other in order to verify the accuracy of the system model. The comparison is shown below in Figure 2.28 at different dc input voltages.

The converter has an output capacitance C = 360 µF and a boost inductance L = 130 µH. The voltage compensator is executed at a sampling period of 100 µs. A dc voltage source was connected to the input of the converter, while an electronic load was connected to the output of the converter. The converter's on-time was adjusted until the output voltage reached 400 V. An ac perturbation was added to the on-time at a given frequency. The output voltage was sensed by the microcontroller's ADC and used to calculate the gain and phase of the open-loop system at that frequency. The frequency of the perturbation was swept to create a Bode plot. This procedure was repeated for a range of input dc voltages and output powers.

The microcontroller computation of t_{on} introduces a computational delay of a single computational cycle, which can be approximated in the Laplace domain as e^{-sT_v}, where T_v is the sampling period of the voltage compensator. Therefore, the theoretical open-loop transfer function can be more accurately described by

$$\frac{V_o}{T_{on}}(s) = \frac{\eta N V_{in(avg)}^2}{2LV_o} \frac{1}{sC_o + 2\frac{P_o}{V_o^2}} e^{-sT_v} \tag{2.57}$$

Figure 2.28 shows how increasing the average input dc voltage increases the system open-loop gain. As can be seen, there is an excellent correlation between the theoretical and experimental result. Similarly, Figure 2.29 shows the impact of output power variation on the open-loop Bode plot, with experimental and theoretical results matching each other well.

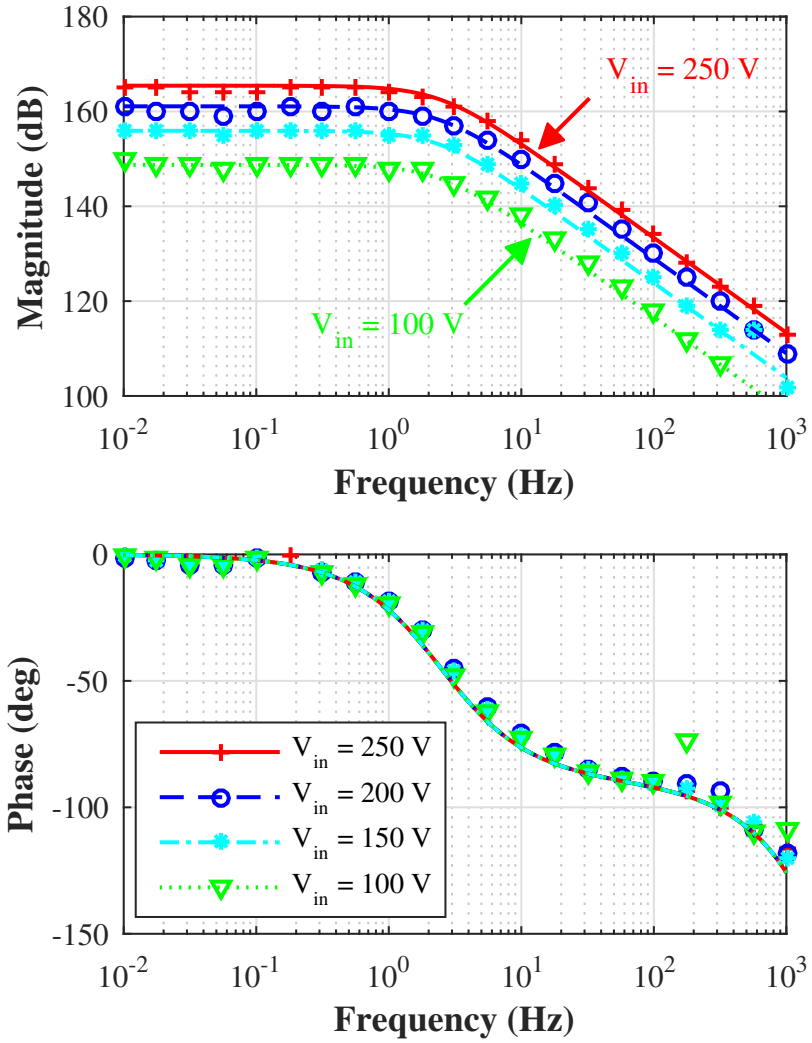


Figure 2.28. Measured (x,o,*,▽) and theoretical (dashed or continuous line) open-loop Bode $\frac{V_o}{T_{on}}(s)$ plot variation, measured at $P_o = 450$ W, with different input dc voltages.

2.9.2 Steady-state Operation

Having verified the open-loop model in the previous section, we can now design a suitable voltage compensator to regulate the output voltage as per the methods described in Sections 2.5 to 2.7. A digital control scheme and software architecture was developed as per Section 2.8, and a phase-shift control algorithm was developed which is described fully in the next chapter. C code was developed to run the 1 kW prototype at full power converting ac power to dc power.

The steady-state operating waveforms of the line voltage v_{line}, inductor current i_{L1}, output voltage v_o and input current i_{in} are shown in Figure 2.30 and Figure 2.31. The converter is rated to a maximum of 1 kW at 230 Vrms, and 700 W at 115 Vrms. Both sets of waveforms are taken at rated power, with Figure 2.30 taken at 230 Vrms and Figure 2.30 taken at 115 Vrms.

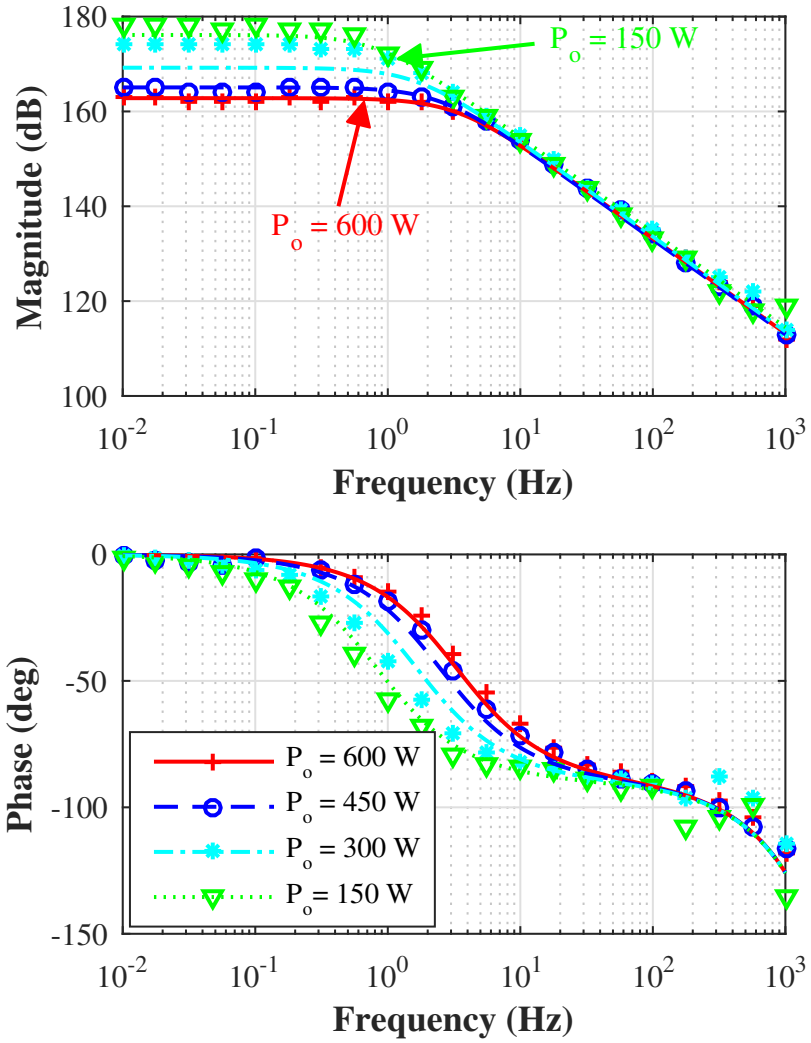


Figure 2.29. Measured (x,o,*,▽) and theoretical (dashed or continuous line) open-loop Bode $\frac{V_o}{T_{on}}(s)$ plot variation at $V_{in} = 250$ V with different levels of output power P_o.

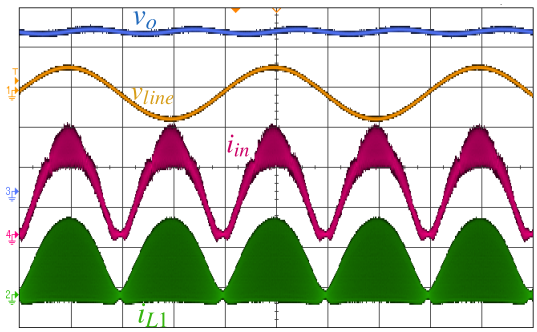


Figure 2.30. Line voltage v_{line}, inductor current i_{L1}, output voltage v_o and input current i_{in} when the converter operates at rated power of P_o = 1 kW at 230 Vrms. (v_{line}: 500 V/div, i_{L1}: 2.5 A/div, v_o: 100 V/div, i_{in} = 3 A/div , timebase : 5 ms/div).

2.9.3 Soft-Start Operation

A soft-start algorithm was also developed to allow the bus voltage to slowly charge to 400 V when the line voltage was first supplied. An oscilloscope printscreen of the line voltage v_{line},

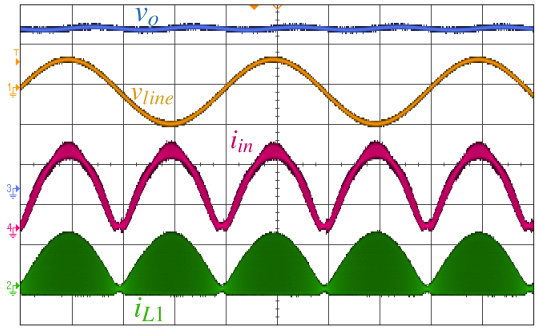


Figure 2.31. Line voltage v_{line}, inductor current i_{L1}, output voltage v_o and input current i_{in} when the converter operates at rated power of P_o = 700 W at 115 V. (v_{line}: 200 V/div, i_{L1}: 5 A/div, v_o: 100 V/div, i_{in} = 5 A/div, timebase : 5 ms/div).

inductor current i_{L1}, output voltage v_o and relay current i_{relay} during start up is shown in Figure 2.32. During the first 400 ms the output voltage charges to the peak of the line voltage, the flyback converter is then powered up to create the 12 V rail which is passed through a linear voltage regulator to power the microcontroller. On power up, the microcontroller runs the initialization code, and checks that the output has charged to the peak of the line. The soft-start procedure is then initiated.

An inrush current-limiting resistor is placed between the bridge rectifier and boost inductors to limit the initial current that is needed to charge the large output electrolytic capacitors. Once the output has successfully charged to the peak of the line voltage, the setpoint voltage of the voltage compensator is set to the sensed output voltage value, and the voltage compensator is enabled. This setpoint voltage is then slowly incremented and ramps up to equal the reference voltage. When the output voltage equals the peak of the line voltage plus 30 V, the current limiting is no longer needed, and the microcontroller closes the relay that is in parallel with the inrush current limiter. The additional 30 V margin ensures the ZCD circuit of each channel can operate properly. The setpoint voltage is continually incremented for the next 1000 ms, until it has reached the desired reference value of 400 V, at which voltage the output capacitors are fully charged, and the converter can begin delivering power to the load. In a conventional power supply the isolated dc-dc converter would then be enabled.

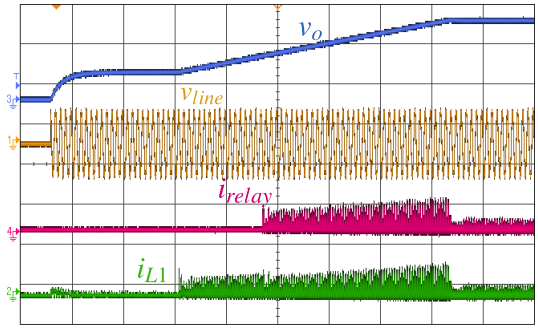


Figure 2.32. Line voltage v_{line}, inductor current i_{L1}, output voltage v_o and relay current i_{relay} when the converter is first started up. (v_{in}: 200 V/div, i_{L1}: 5 A/div, v_o: 100 V/div, $i_{relay} = 5A/div$, timebase : 200 ms/div).

2.9.4 Switching-Frequency Variation

The switching frequency of each channel has a wide variation. The variation is predominantly a function of boost inductor value, input voltage, output voltage and the power being delivered by that channel. However, it is also a function of the resonance between the MOSFET output capacitance and the boost inductor, and the timing delays of the ZCD circuits and gate driver circuits. Thus, it is difficult to accurately predict and calculate the switching frequency. As a result, it is much easier to obtain the switching frequency by measuring it over the rated power of a single channel at different line voltages. Figure 2.33 shows the measured frequency of one channel of the 1 kW converter over a half-line period. The x-axis shows the time from 0 ms to 10 ms as the line voltage varies from 0 at 0 ms, to its peak at 5 ms and again to zero at 10 ms. The measurements were re-taken at different output powers from 50 W to 300 W. Figure 2.33(a) shows the switching frequency variation at 115 Vrms, while Figure 2.33(b) shows the variation at 230 Vrms.

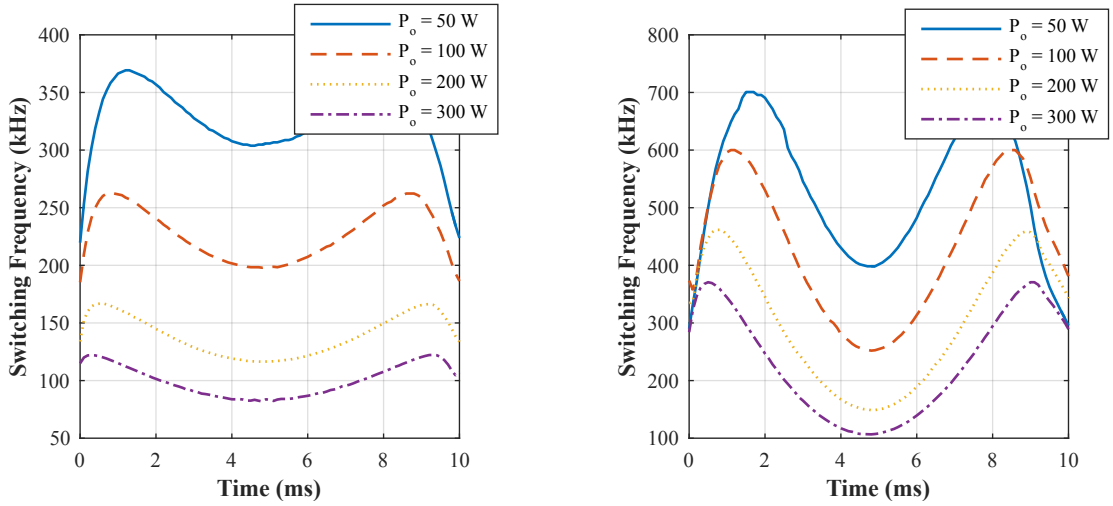


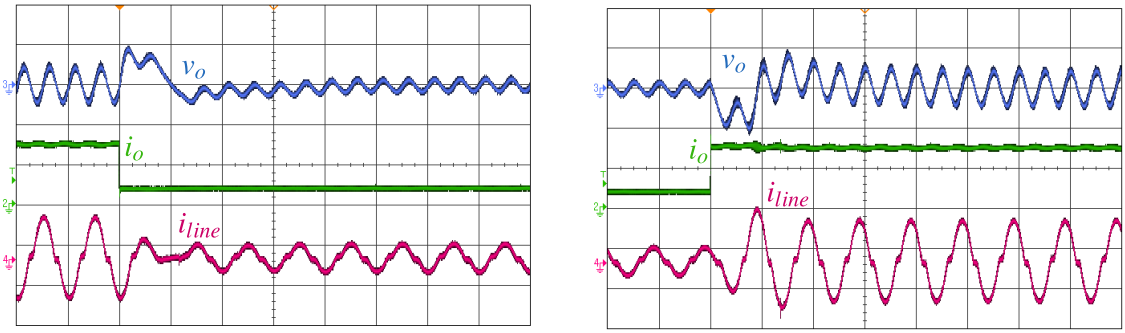
Figure 2.33. Switching frequency variation, measured over a half line period, at (a) 115 Vrms and (b) 230 Vrms.

The figure demonstrates that each channel of the BCM converter undergoes a large variation in switching frequency over each half line cycle. This is quite beneficial in reducing the conducted EMI, as it creates a natural dithering of the switching frequency. On the other hand, the large switching frequency variation makes the design of the magnetics and other circuitry, such as gate drives, more challenging.

2.9.5 Load steps

Different load steps were carried out to verify that the output voltage had a reasonably fast dynamic response. Figure 2.34 shows a load step from an output power of 250 W to 750 W, and also a load step from 750 W to 250 W, taken at 230 Vrms. The oscilloscope printscreen shows the output voltage (ac coupled to the scope), the output current which undergoes a

step change, and the line current. The voltage compensator was designed for a nominal line voltage of 230 V, and so, the output voltage has a fast transient response at this point. This is evident from the output voltage waveforms shown in Figure 2.34, which demonstrate a fast settling time, and a low peak undershoot and overshoot.



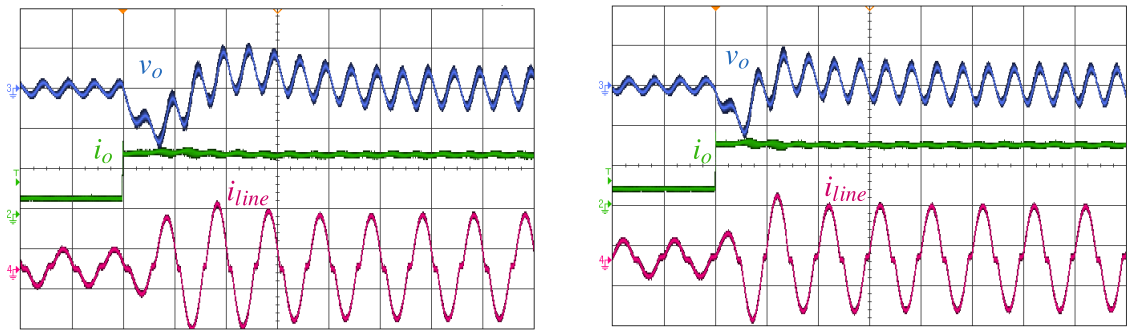
(a) (b)

Figure 2.34. Output current i_o, output voltage v_o (ac coupled) and line current i_{line}, during a load step (a) from P_o = 750 W to 250 W and (b) from P_o = 250 W to 750 W, at 230 Vrms. (i_o: 1 A/div, v_o: 10 V/div, i_{line}: 5 A/div, timebase : 20 ms/div).

If the line voltage is lowered to a rms value of 180 V, and the same load step is performed, the output voltage dynamics become slightly slower. It is assumed, of course that, the adaptive gain k_v, which is described in Section 2.5, is not enabled. This scenario is presented in Figure 2.35(a), for a load step from 250 W to 750 W. The same load step is presented in Figure 2.36(a), but for the opposite load step from 750 W to 250 W. The output voltage dynamics become slower because the open-loop system gain decreases at lower levels of input voltage. The adaptive gain k_v was introduced to the voltage-compensator design to counteract this behaviour, as discussed earlier in Section 2.5 and described by Table 2.3. The same load steps from 250 W to 750 W, and visa versa, are shown in Figure 2.35(b) and Figure 2.36(b) respectively. The adaptive gain of the voltage compensator increases from 1 to 1.52 at 180 Vrms. This results in a noticeable small improvement in the settling time of the output voltage. There are also similar small improvements in the peak overshoot and undershoot of the output voltage.

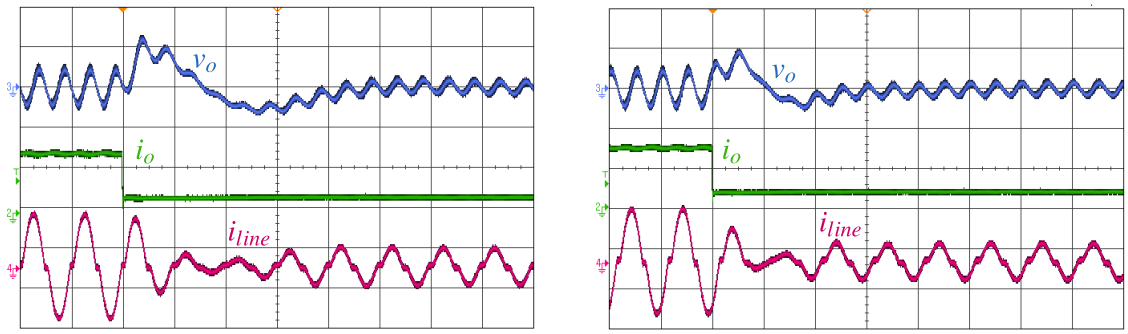
The improvement in the output voltage dynamic response becomes much more noticeable at lower line voltages, where there is a more significant decrease in the open-loop gain of the voltage loop. For example, Figure 2.37 demonstrates a load step from 150 W to 450 W at a rms line voltage of 115 V, with and without the adaptive gain enabled. Figure 2.37(a) demonstrates the output voltage transient response when no adaptive gain is used. This results in a large peak undershoot and a long settling time. Figure 2.37(b) shows the same load step with the adaptive gain enabled. Thus results in a much lower peak undershoot and settling time of the output voltage.

Similarly, Figure 2.38 shows a load step with and without the adaptive gain enabled at a line voltage of 115 V, but in this case the load steps go from 450 W to 150 W.



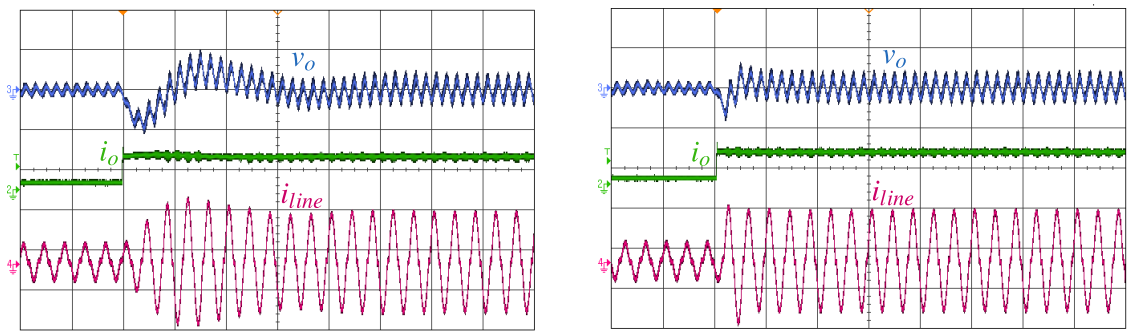
(a) (b)

Figure 2.35. Output current i_o, output voltage v_o (ac coupled) and line current i_{line}, during a load step from P_o = 250 W to 750 W at 180 Vrms, with (a) the adaptive gain disabled and (b) the adaptive gain enabled. (i_o: 1 A/div, v_o: 10 V/div, i_{line}: 5 A/div, timebase : 20 ms/div).



(a) (b)

Figure 2.36. Output current i_o, output voltage v_o (ac coupled) and line current i_{line}, during a load step from P_o = 750 W to 250 W at 180 Vrms, with (a) the adaptive gain disabled and (b) the adaptive gain enabled. (i_o: 1 A/div, v_o: 10 V/div, i_{line}: 5 A/div, timebase : 20 ms/div).

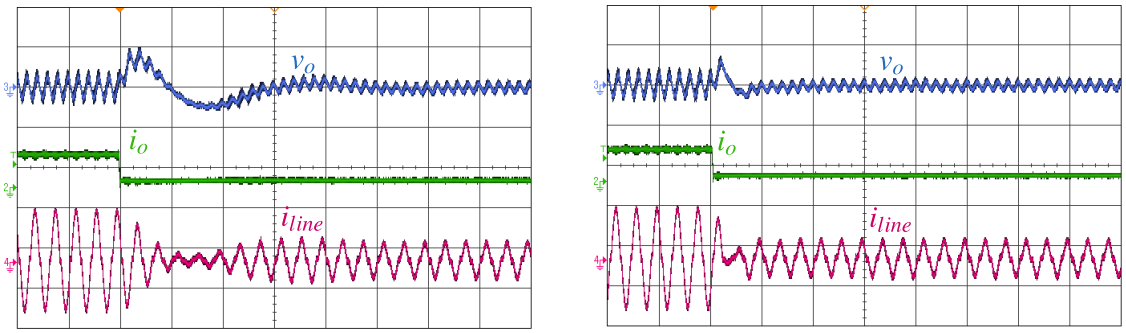


(a) (b)

Figure 2.37. Output current i_o, output voltage v_o (ac coupled) and line current i_{line}, during a load step from P_o = 150 W to 450 W at 115 Vrms, with (a) the adaptive gain disabled and (b) the adaptive gain enabled. (i_o: 1 A/div, v_o: 10 V/div, i_{line}: 5 A/div, timebase : 50 ms/div).

2.9.6 Line-Voltage Disturbances

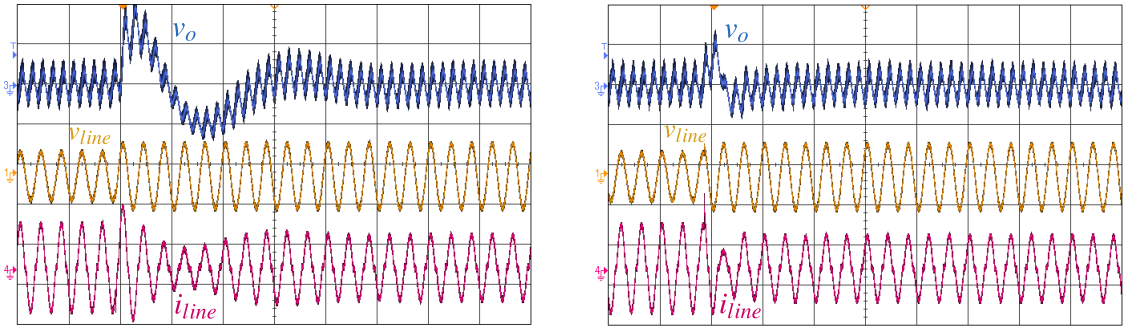
The adaptive gain improves the output voltage's response due to disturbances in the line voltage. This improvement is demonstrated by Figure 2.39 which shows the effect of a step in line voltage from 85 V to 115 V. The oscilloscope printscreen shows the waveforms of



(a) (b)

Figure 2.38. Output current i_o, output voltage v_o (ac coupled) and line current i_{line}, during a load step from P_o = 450 W to 150 W at 115 Vrms, with (a) the adaptive gain disabled and (b) the adaptive gain enabled. (i_o: 1 A/div, v_o: 10 V/div, i_{line}: 5 A/div, timebase : 50 ms/div).

the output voltage (ac coupled), the line voltage and the line current during the change in line voltage rms level. The oscilloscope printscreen was captured at an output power of 300 W. Figure 2.39(a) shows the output voltage transient response when the adaptive gain is not used, whereas Figure 2.39(b) shows the output-voltage transient response when the adaptive gain is used. By comparing the response of the output voltage in both figures, it is clear, that using the adaptive gain greatly improves the dynamic performance of the output voltage due to variations in the line voltage.

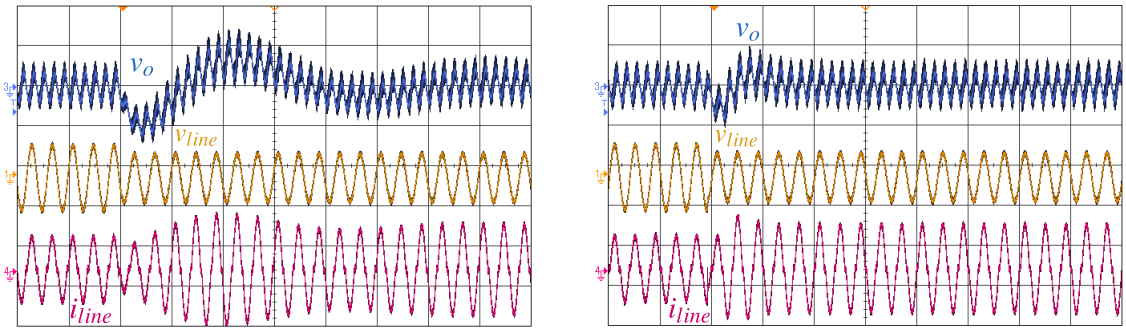


(a) (b)

Figure 2.39. Line voltage v_{line}, output voltage v_o (ac coupled) and line current i_{line}, during a line voltage transient from 85 V to 115 V with (a) the adaptive gain disabled and (b) the adaptive gain enabled. (v_{in}: 200 V/div, v_o: 5 V/div, i_{line}: 5 A/div, timebase : 50 ms/div).

Akin to Figure 2.39, Figure 2.40 shows the output-voltage transient response to the opposite change in line voltage from 115 V to 85 V.

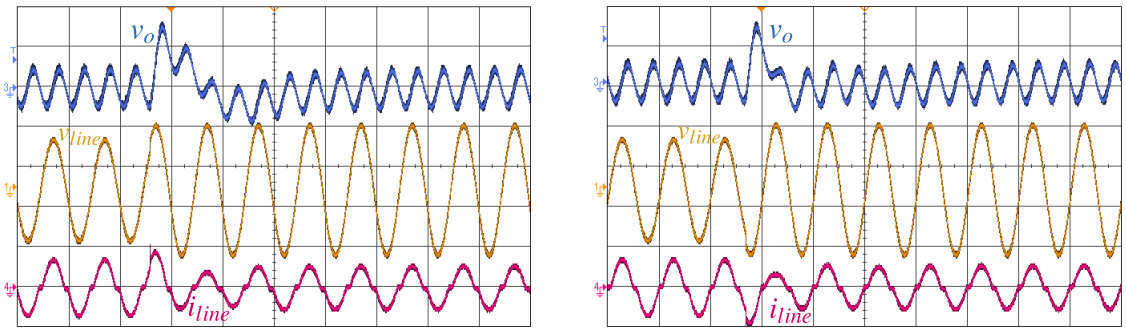
A smaller improvement is observed for line-voltage disturbances that occur at higher rms voltage levels. For instance, Figure 2.41 shows the transient response of the output voltage to a change in line voltage from 180 V to 230 V. The oscilloscope printscreen displayed in Figure 2.41 was taken at an output power of 800 W. In this case, the improvement in the output-voltage transient response is quite small, as the adaptive gain does not change much between 180 V and 230 V, but since there is already a fast transient response at this higher



(a) (b)

Figure 2.40. Line voltage v_{line}, output voltage v_o (ac coupled) and line current i_{line}, during a line-voltage transient from 115 V to 85 V with (a) the adaptive gain disabled and (b) the adaptive gain enabled. (v_{in}: 200 V/div, v_o: 5 V/div, i_{line}: 5 A/div, timebase : 50 ms/div).

rms voltage, there is no strong need to improve the output voltage dynamics.



(a) (b)

Figure 2.41. Line voltage v_{line}, output voltage v_o (ac coupled) and line current i_{line}, during a line-voltage transient from 180 V to 230 V with (a) the adaptive gain disabled and (b) the adaptive gain enabled. (v_{in}: 200 V/div, v_o: 10 V/div, i_{line}: 10 A/div, timebase : 20 ms/div).

Figure 2.42 shows the same line-voltage disturbance as Figure 2.41, but in the opposite direction, with the line voltage changing from 230 V to 180 V. In this case the adaptive gain can only provide a very small improvement, because it initially starts out equal to 1 when the line voltage is 230 V, and then must wait for the sensed average input voltage to reduce, before it increases in value. Even so, there is still a noticeable improvement, with less peak overshoot when the adaptive gain is enabled.

2.9.7 Power Factor

A disadvantage of using the adaptive gain with the voltage compensator, is that the magnitude of the 2nd harmonic ripple produced at the output of the voltage compensator is increased. This in turn increases the 2nd harmonic component in the line current, which lowers the power factor of the line current drawn by the converter. However, if the adaptive notch filter described in Section 2.7 is added to the output of the voltage compensator, the 2nd harmonic component is greatly reduced. As a result, the voltage controller can have both a fast transient

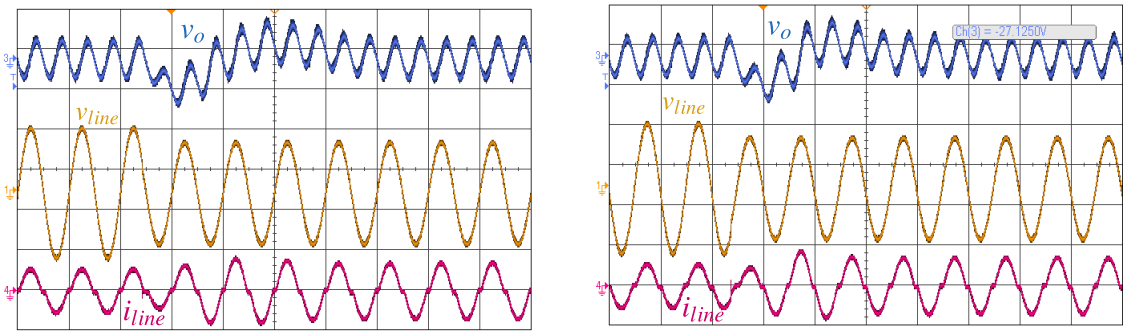


Figure 2.42. Line voltage v_{line}, output voltage v_o (ac coupled) and line current i_{line}, during a line-voltage transient from 230 V to 180 V with (a) the adaptive gain disabled and (b) the adaptive gain enabled. (v_{in}: 200 V/div, v_o: 10 V/div, i_{line}: 10 A/div, timebase : 20 ms/div).

response and good power factor.

The power factor was measured with different voltage-controller configurations to demonstrate the effect that the adaptive gain and notch filter have on the power factor of the prototype. First, the measurement was taken when the voltage controller had no adaptive gain or notch filter, second, the adaptive gain was enabled but the notch filter was disabled, and third, both the adaptive gain and notch filter were enabled. The power-factor measurements are given in Figure 2.43 for 115 Vrms and 230 Vrms. Figure 2.43(a) shows the comparison for 115 Vrms, in this case, is is evident that using the adaptive gain significantly reduces the power factor at all levels of output power. However, if the notch filter recursive algorithm is enabled, the power factor actually becomes slightly better than if no adaptive gain or notch filter was used at all. Therefore, it is possible to achieve both a good power factor and fast voltage tracking at low line voltages, because the notch filter has no effect on the transient response of the output voltage.

Figure 2.43(b) shows the comparison measured at 230 Vrms. There is no difference between having the adaptive gain enabled or disabled, because the adaptive gain has a value of $k_v = 1$. Hence, the measured power factor with and without the adaptive gain is identical. It can be observed, however, that using the notch filter dramatically increases the power factor of the converter at all power levels.

The notch filter improves the power factor by reducing the 2$^{\text{nd}}$ harmonic component in the voltage-compensator output. This can be observed by plotting the input and output to the notch filter. The measured notch-filter input and output are shown in Figure 2.44 at rated power, at 115 Vrms and 230 Vrms. Figure 2.44(a) shows the filter input and output at 115 Vrms while Figure 2.44(b) shows the same waveforms at 230 Vrms. The filter input $x_n[n]$ and output $t_{on(ticks)}$ are given in units of microseconds by scaling the input by 1 over $2^{A_x} \times f_{pwm}$ and scaling the output by a factor of 1 over f_{pwm}. In both cases, it is clearly shown that the adaptive notch filter dramatically reduces the 2$^{\text{nd}}$ harmonic component.

A comparison of the input current harmonics with and without the notch filter is given in

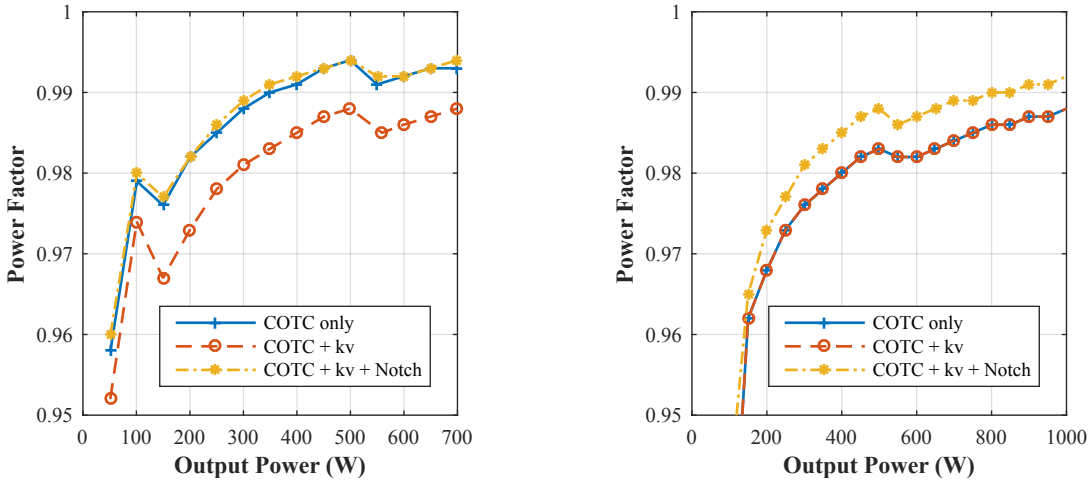


Figure 2.43. Power factor comparison of COTC only, COTC with an adaptive gain k_v and COTC with an adaptive gain k_v as well as a notch filter, measured at (a) 115 Vrms and (b) 230 Vrms.

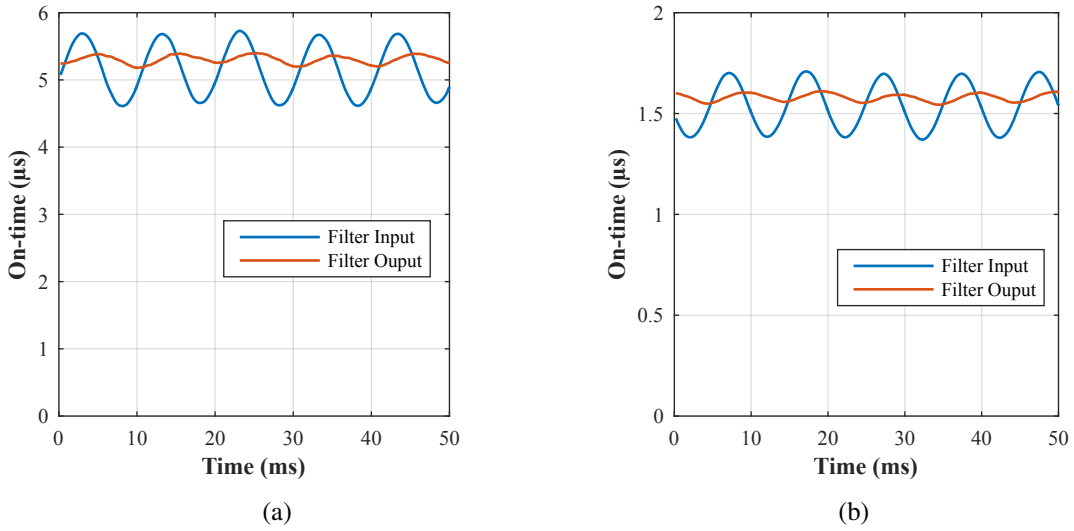
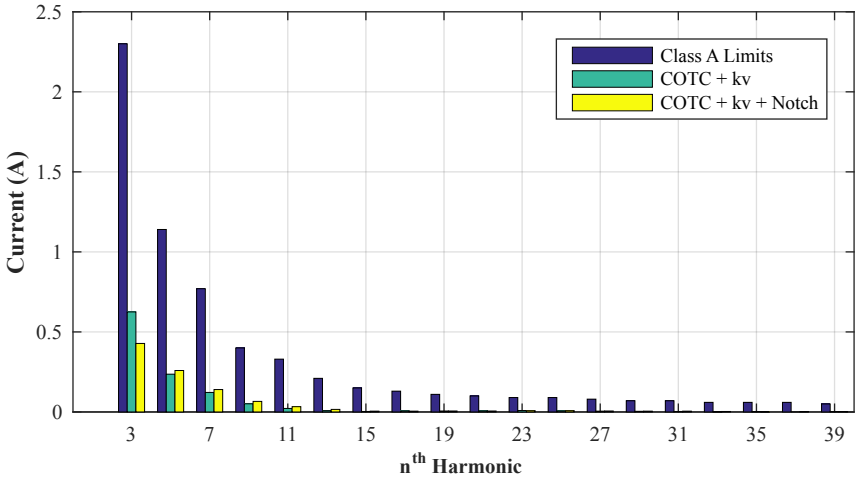
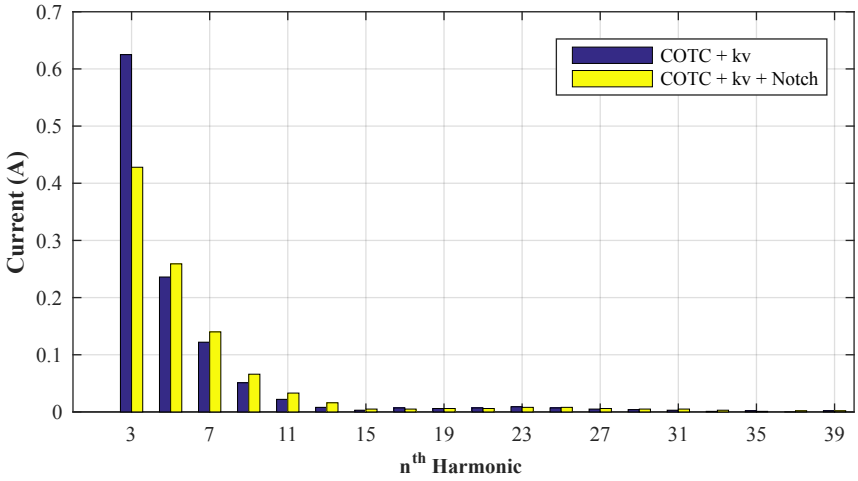


Figure 2.44. The input and output to the notch filter measured at rated power at (a) 115 Vrms and (b) 230 Vrms.

Figure 2.45 to further demonstrate the improvement in the power quality provided by using the notch filter. In Figure 2.45(a) the measurements are compared to the EN61000-3-2 Class A limits, showing that both sets of measurements are well below the Class A limits. While in Figure 2.45(b) both sets of measurements are compared to each other without the limits, demonstrating the notch filter dramatically reduces the third harmonic magnitude, at the cost of small increases in the current at higher harmonics. No even-ordered harmonics are shown as these are all 0 A in magnitude.



(a)



(b)

Figure 2.45. The input current harmonics measured at 230 Vrms and an output power of 1 kW, with and without the notch filter enabled. In subfigure (a) the measured harmonics are compared to the Class A limits and in subfigure (b) there are no Class A limits.

2.10 Conclusion

This chapter presented a digital control strategy to regulate the output voltage of a multi-channel BCM boost converter for PFC applications. The chapter discusses how converting the ac mains voltage to a regulated dc output voltage creates a significant 2^{nd} harmonic ripple on the output voltage. The effect of the 2^{nd} harmonic ripple on the design of the voltage compensator is explained in detail. The ripple is shown to create a significant design challenge in building a voltage feedback network that can provide both good input power factor, and fast tracking of the output voltage.

The time-averaged small-signal model of a multi-channel BCM boost converter is derived, this model was linearised and converted from the time-domain to the frequency domain to formulate a transfer function, which was subsequently used to design a suitable controller to regulate the output voltage. A design procedure was given to design a voltage compensator

using classical linear feedback control, where an integral lead compensator was used. The voltage compensator design was verified using Simulink simulations. Furthermore, the simulations were used to explore the limitations of the controller design, demonstrating how using a controller with a high bandwidth has fast output-voltage tracking but high line-current distortion, while a controller with a low bandwidth has poor output-voltage dynamics and low line-current distortion. The simulation was also used to show how the output voltage tracking becomes worse at lower levels of input voltage.

The design of the voltage compensator was improved upon by the introduction of an adaptive gain, which increased in value as the line voltage dropped, in order to compensate for the slower tracking at lower line voltages. The voltage-compensator design was expanded upon to allow a fixed-point implementation, this ensured the design was suitable for implementation on a low-cost microcontroller.

Next, the converter's power factor was improved by using a digital notch filter. The filter was designed to remove the 2^{nd} harmonic ripple from the output of the voltage compensator. The digital notch-filter design was altered so that some of the filter coefficients changed with the sensed line period, this enabled the notch filter to work over a range of different line frequencies.

Lastly, experimental results were provided on a 600 W 2-channel BCM boost converter using an expensive Texas Instruments TMS320f28069 microcontroller and a 1 kW 3-channel BCM boost converter using a low-cost Infineon XMC1402 microcontroller. The 600 W prototype was used to verify the small-signal analysis of the converter, by measuring the converter's open-loop response and comparing the measured results to the theoretically-derived results. The 1 kW prototype was used to verify the design of the voltage compensator. The performance of the voltage compensator was analysed with and without the use of the adaptive gain, demonstrating that the output voltage response significantly worsens at lower line voltages if the adaptive gain is not used. Whereas, if the adaptive gain is used, the output voltage response is much faster at low line voltages. Similarly, the power factor variation with load power was measured, with and without the notch filter enabled, demonstrating the digital notch filter improved the power quality.

3 PHASE-SHIFT CONTROL

This chapter presents a novel closed-loop digital control scheme to maintain proper interleaving operation of a multi-channel boundary-conduction-mode (BCM) boost converter, as used in power-factor-correction (PFC) applications. The proposed control scheme is suitable for implementation on a low-cost microcontroller. This is made possible by executing the control scheme at a constant sampling rate that is much slower than the maximum switching frequency of the converter. The performance of the control scheme is further improved by using an adaptive gain that scales with the on-time of the converter, and provides optimal phase-shift control and stability under all operating conditions. The digital closed-loop control scheme is validated experimentally on a 3-channel 1 kW prototype ac-dc converter. The converter has an output voltage of 400 V and a universal input voltage range of 85 V to 265 V. The prototype converter uses a low-cost microcontroller, while demonstrating correct interleaving operation.

Results of this chapter have been published in the following papers,

- R. T. Ryan, D. N. Hogan, R. J. Morrison and J. G. Hayes, "Digital closed-loop control strategy to maintain the phase shift of a multi-channel BCM boost converter for PFC applications," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 7001-7012, July 2019.

- R. T. Ryan, J. G. Hayes, R. Morrison and D. Hogan, "Digital control of an interleaved BCM boost PFC converter with fast transient response at low input voltage," *IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 257-264.

3.1 Introduction

In this chapter, a closed-loop digital control scheme is designed to maintain correct interleaving operation of a multi-channel BCM boost converter, as shown earlier in Figure 1.17. A phase shift of $\frac{n-1}{N} \times 360^\circ$ must be maintained between the inductor currents of each channel, where N is the total number of boost converter channels that are enabled, and n is the index number of a particular channel, for example $n = 1$ for the first channel, $n = 2$ for the second channel, and so on. However, the switching frequency of the BCM boost converter varies with input voltage and output power [14]. This makes interleaving of a multi-channel BCM boost converter a challenging design task.

Several methods already exist in the literature to maintain the correct phase shift between the different channels of interleaved BCM boost converters. These methods include analog closed-loop control, analog open-loop control, digital open-loop control and digital feedforward control. In this work, a digital closed-loop control scheme is designed to maintain the correct phase shift. This method is most closely related to the analog closed-loop method, so we will first take a more in-depth look at how the analog closed-loop phase-shift control works.

3.1.1 Analog Closed-Loop Method

In analog closed-loop schemes, one of the boost-converter channels is denoted the master channel, while the remaining boost converter channels are denoted the slave channels. The phase shift of the slave channels are synchronised to the master channel by forming a closed-loop feedback network that adjusts the turn-off instant of each slave-channel MOSFET based on the sensed switching period of the master channel and the previous phase-shift of the slave-channel [22], [66], [72], [75].

The generation of the analog PWM signals must be discussed in order to understand how the analog closed-loop method works. Figure 3.1 demonstrates how the PWM signal PWM_1, which controls the MOSFET Q_1, is generated for the master channel using analog circuitry. Figure 3.2 shows the corresponding timing diagram for the circuit. The signal PWM_1 is set by the signal ZCD_1 which is created by a zero-current-detection (ZCD) circuit. The ZCD circuit detects when the energy stored in the drain-source capacitor of Q_1 has discharged as much as possible back into the input capacitor C_{in}. This causes the inductor current i_{L1} to become negative before the turn-on instant of the switch. By this means, the ZCD circuit reduces the converter's switching loss by transferring the energy stored in the MOSFET drain-source capacitor back into the input capacitor. Moreover the ZCD circuit ensures the inductor current reaches zero before the MOSFET is re-triggered to turn-on, hence ensuring the converter remains in BCM. The MOSFET can also be triggered by a reset timer. The timer is used during start-up, or in the case when no ZCD_1 pulse is generated by the ZCD

circuit. This can happen at low power when the on-time or voltage-error amplifier signal has a magnitude close to or equal to zero. The master-channel MOSFET is turned off after an on-time of t_{on1} has elapsed. This is implemented by using the constant-current source I_1, transistor M_1 and a capacitor to make a ramp signal, denoted v_{ramp}, that is compared to the voltage V_{EA}, to trigger the switch's turn-off instant. The voltage denoted V_{EA} is the output of the analog voltage-error amplifier, which is proportional to the on-time and is adjusted by the analog voltage compensator to maintain the output voltage at its setpoint value.

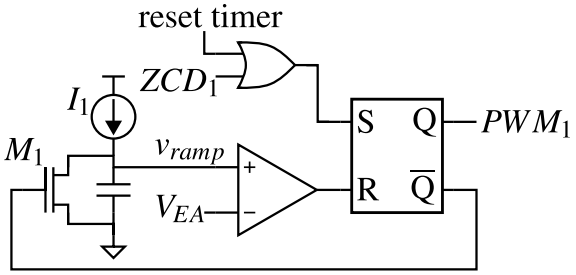


Figure 3.1. PWM generation of the master channel using analog circuitry.

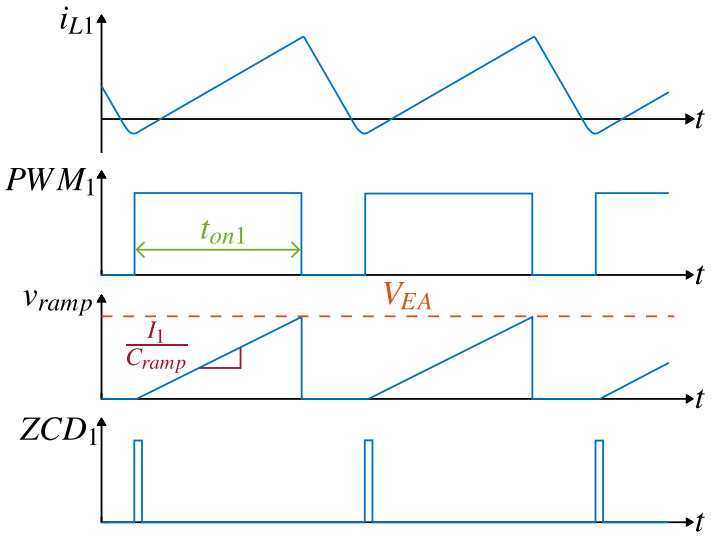


Figure 3.2. Master-channel PWM generation using analog circuitry.

The closed-loop method uses ZCD circuits to trigger the MOSFET's turn-on instant for all interleaved channels, thus ensuring perfect valley switching of all switches under all conditions, and therefore lower switching losses. Using a separate ZCD circuit for each channel also ensures the converter cannot enter continuous-conduction mode (CCM), which may cause damage to components. The phase-locked-loop (PLL) method is a commonly adopted analog closed-loop control scheme [72], [75]. This method is shown in Figure 3.3. In this method the phase shift is sensed by passing the ZCD signals of the master and slave channel through a flip flop. This creates a square wave with a mean value proportional to the ratio between the the phase shift of the n^{th} channel t_{psn}, and the switching period of the master channel t_{sw1}. The square wave passes through a RC low-pass filter and is subtracted

from a constant voltage setpoint, that is proportional to $\frac{n-1}{N}$, to create an error signal. This generates the error current i_e that has a magnitude proportional to the error signal, and is used to adjust the turn-off instant of the slave channel by adjusting the slope of the v_{rampn} signal used in the PWM generation. Selecting the correct gain value for k_m ensures the phase shift tracks the desired setpoint. The turn-off instant of the slave channel can also be adjusted by adding a voltage to the voltage-error amplifier signal of the slave channel V_{EAn}. The downside of the PLL method is that the use of the low-pass filter to sense the

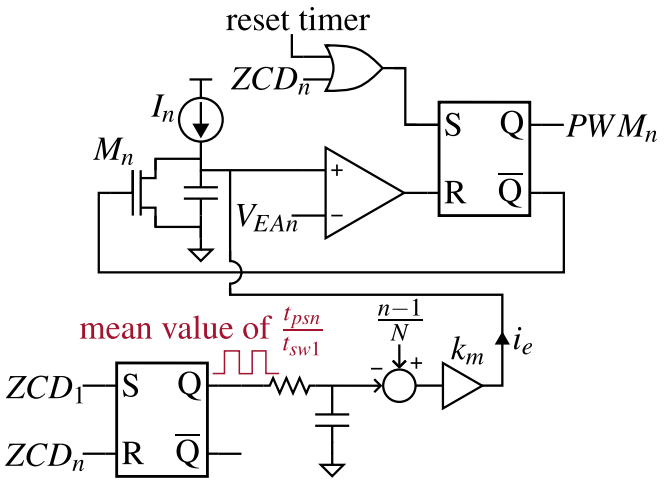


Figure 3.3. Phase-shift control and PWM generation of a single slave channel using analog circuitry with the PLL method and turn-off adjustment by altering the PWM generation ramp signal.

phase shift leads to a slow dynamic response of the control loop and can lead to significant phase error. In [66], a closed-loop scheme is adopted where the phase shift and switching period are sensed using sample-and-hold blocks. This method is more advantageous than the closed-loop PLL method as it does not require low-pass filtering of the sensed phase shift, thus improving the tracking performance of the control loop. This method is depicted in Figure 3.4. The constant current source I_{n1}, transistor M_{n1}, and ramp capacitor are used to generate a ramp signal. This ramp signal is then fed into two separate sample-and-hold blocks triggered by ZCD_1 and ZCD_n. The output of the sample-and-hold triggered by ZCD_1 is a voltage proportional to the switching period of the master channel. The signal is scaled by the factor $\frac{n-1}{N}$ to generate the reference signal of the control loop, and is denoted v_{refn}. The output of the sample-and-hold block triggered by ZCD_n is a voltage proportional to the current phase shift between the master channel and the n^{th} slave channel. This voltage is denoted v_{psn}. An error signal is generated by subtracting v_{psn} from v_{refn}. A closed feedback loop is formed by adjusting the error signal by a gain of k_m, and adding the signal to the voltage error signal to adjust the switches turn-off instant. It is also possible to adjust the switches turn-off instant by adjusting the slope of the PWM ramp signal of the slave converter as in Figure 3.3.

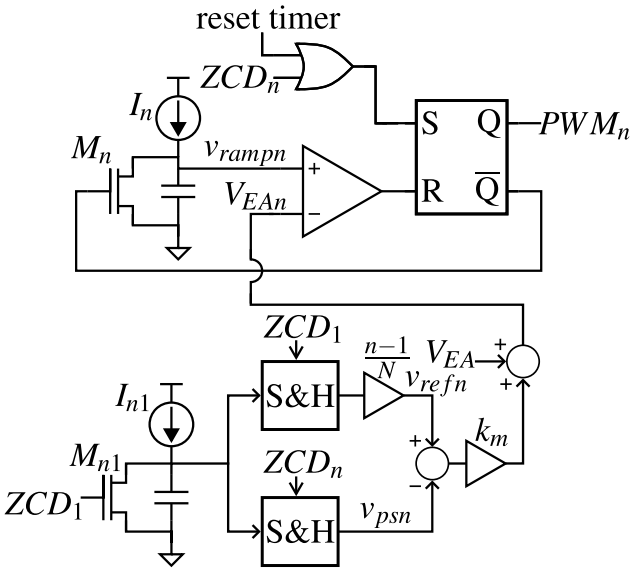


Figure 3.4. Phase-shift control and PWM generation of a single slave channel using analog circuitry with the closed-loop method and turn-off adjustment by altering the voltage error amplifier signal.

3.1.2 Analog Open-Loop Method

It is also possible to interleave multiple channels of a BCM boost converter using an open-loop method [69], [70], [73]. Similar to the closed-loop method, the open-loop method works by assigning one of the interleaved channels as the master and the others as the slaves. The master works as a standalone converter with its own ZCD circuit, therefore the master channels MOSFET turn-on instant is always triggered by its own ZCD circuit. The turn-on instants of the MOSFETs in the slave channels are obtained by delaying the ZCD signal of the master channel with a time delay of $\frac{n-1}{N} \times t_{sw1}$. The open-loop method suffers from severe sub-harmonic oscillations when implemented using voltage-mode control for duty cycles greater than 0.5 [73], meaning it must be implemented with current-mode control which requires additional sense circuitry. The slave converter must have a lower inductance than the master channel to prevent it entering into CCM. As a result, the open-loop method also requires the ability to sense which channel has the lowest inductance. If there is only a small mismatch in the boost inductance of each channel the slave converter operates slightly in DCM, and valley switching is ensured. However, if there is significant mismatch between the boost inductances of both channels, the slave channel operates in DCM and loses its valley-switching operation.

3.1.3 Existing Digital Solutions

Several examples of digitally-controlled interleaved BCM boost converters already exist in literature. These examples maintain their phase shift by either open-loop master-slave control [19], or by the use of feedforward algotithms [76]. The digital open-loop method is almost identical to the analog open-loop method except that a digital timer and other digital circuitry are used to delay the PWM signal of the master channel, by the appropriate phase

delay for each slave channel. The digital feedforward method works by using algorithms to estimate the converter's switching period. The estimated switching period is used to dictate when the slave-channel MOSFET is to be turned on. However, similar to the open-loop method, this method also does not ensure BCM operation and valley switching if the system is disturbed by a load change.

3.1.4 Proposed Digital Closed-Loop Solution

In this chapter, a digital closed-loop solution is proposed to maintain the correct phase shifts for a multi-channel BCM boost converter.

The implementation of the phase-shift feedback control, and the PWM generation of the master and a slave channel, as described in this work, are shown in Figure 3.5. The switching period of the master channel is measured by feeding the ZCD_1 signal of the master channel into a capture peripheral on the microcontroller. The capture peripheral has a digital timer independent of the CPU that can be used to measure the time between the ZCD pulses. As a result, it is possible to measure the switching period of the master channel every switching period. This is equivalent to the sample-and-hold method used in the analog solution of Figure 3.5. The feedback control is accomplished by executing a feedback algorithm in the microcontroller CPU. The feedback algorithm reads the sensed switching period and phase shift from each capture peripheral. It then calculates the reference for each slave channel t_{ref_n} based on the sensed switching period of the master channel. The phase-shift error is determined by subtracting the sensed phase shift from the reference phase shift. The phase-shift error is used to adjust the on-time of each channel to ensure the desired phase shift is maintained. This method uses a similar feedback control as the analog solution shown in Figure 3.5. The analog solution has an advantage that the turn-off instant of the slave channels is updated by the feedback network on each switching cycle. Attempting to update the turn-off instant of the microcontroller on a cycle-by-cycle basis requires a very expensive microcontroller because the phase-shift algorithm executed by the CPU would have to run in an interrupt every switching instance. Therefore, the microcontroller needs to execute the phase-shift control algorithm faster than the minimum switching period of the boost converter. This would require a microcontroller with a powerful CPU and high clock frequency, which is more expensive. A better solution is to run the phase-shift control algorithm at a fixed sampling period T_m which is much smaller than the minimum switching period of the converter. This enables a much cheaper microcontroller to be used.

The microcontroller uses a compare or PWM peripheral to generate the PWM signals of each boost converter channel. The timing diagram of Fig. 3.6 demonstrates how the PWM peripheral for each channel is configured. The PWM signal is configured to turn on when the counter register of the PWM timer $TBCTR$ has a value of $TBPRD - t_{onn}$, where $TBPRD$, is the constant value stored in the period register of the PWM peripheral. The PWM peripheral

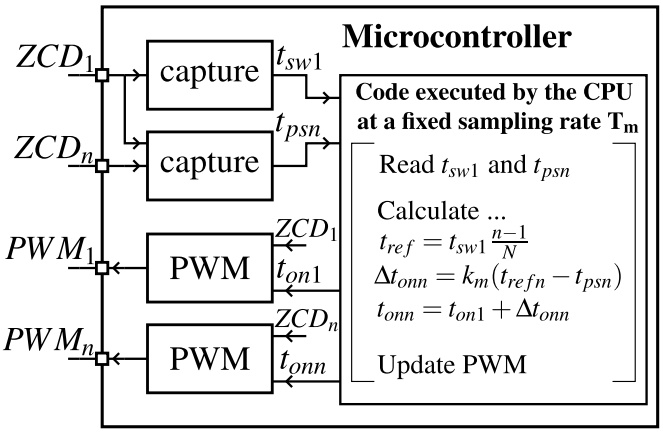


Figure 3.5. Phase-shift control and PWM generation of the master and a single slave channel using digital circuitry with the closed-loop method and turn-off adjustment made by altering the slave channel's on-time.

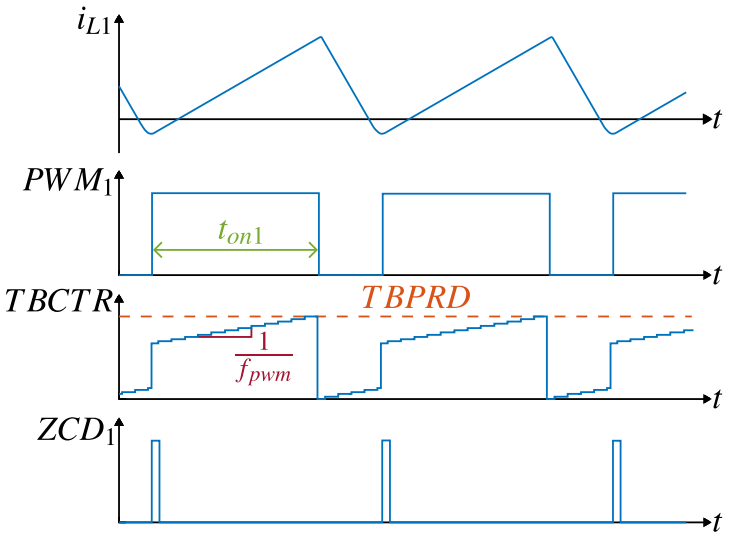


Figure 3.6. Timing diagram for the PWM generation of the master channel using digital circuitry.

is also configured to load the $TBCTR$ register with a value of $TBPRD - t_{onn}$ when the ZCD signal is triggered. When the $TBCTR$ reaches a value of $TBPRD$ the PWM signal is set low, and the counter restarts. Using this method results in the PWM signal of each channel having a natural reset timer. If the ZCD signal is not triggered, the $TBCTR$ continues counting until it reaches a value of $TBPRD - t_{onn}$. This method is helpful as sometimes the ZCD signal is not triggered, for instance during converter start-up or at very light load when the on-time becomes zero.

This chapter is divided into four different sections as follows. Section I provides a brief review of how the valley-switching operation works and how it reduces power losses. Section II describes the operation and design of the phase-shift control loop. Section IV demonstrates the experimental results of a prototype 1 kW multi-channel BCM converter, demonstrating correct interleaving action for 2-channel and 3-channel operation.

3.2 Valley Switching

The main advantage of using a closed-loop control scheme to maintain the correct phase shifts is that each channel has its own ZCD circuit that ensures valley-switching operation is always maintained. This reduces switching losses. The valley switching of the BCM converter can be explained by looking at a single channel of the boost converter with the MOSFET drain-source capacitance C_{ds} as shown in Figure 3.7.

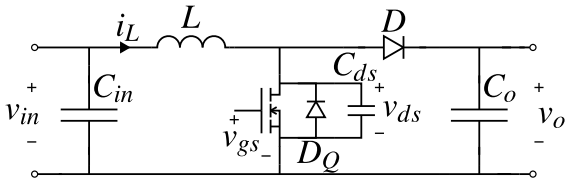


Figure 3.7. A single channel of the interleaved boost converter including the MOSFET drain-source capacitance and body diode.

Figure 3.8 and Figure 3.9 show the behaviour of the drain-to-source voltage v_{ds} and inductor current i_L during MOSFET turn-off. As the inductor current discharges to zero, the diode D is forward biased, therefore $v_{ds} = v_o$, where v_o is the output voltage. Once i_L reaches zero, the MOSFET remains off, and the capacitance C_{ds} begins to discharge through the boost inductor L into the input capacitor C_{in}.

Zero-voltage switching is achieved when $v_{in} < \frac{1}{2}v_o$. Once v_{ds} fully discharges to 0 V, the negative inductor current forces the MOSFET's body diode D_Q to conduct. The ZCD circuit then triggers the switch to turn on while $v_{ds} = 0$, as shown by the solid lines of Figure 3.8. If the MOSFET remains off, the circuit enters DCM, causing the inductor to resonate with the MOSFET drain-source capacitor, as shown by the dashed lines of Figure 3.8.

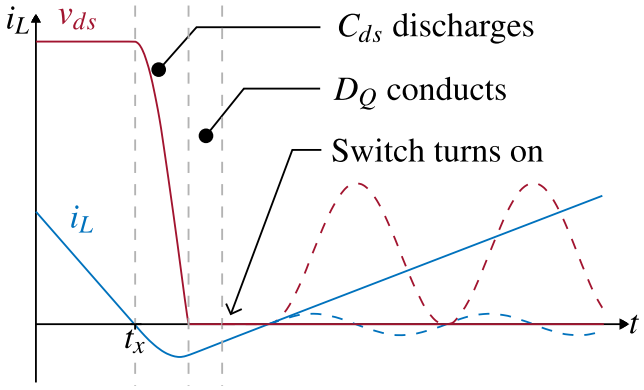


Figure 3.8. Zero-voltage switching $v_{in} < \frac{1}{2}v_o$.

If $v_{in} > \frac{1}{2}v_o$, then C_{ds} does not fully discharge, but instead reaches a valley at $v_{ds} = 2v_{in} - v_o$ as shown in Figure 3.9. The ZCD circuit ensures that the switch turns on at this valley to minimize the switching losses.

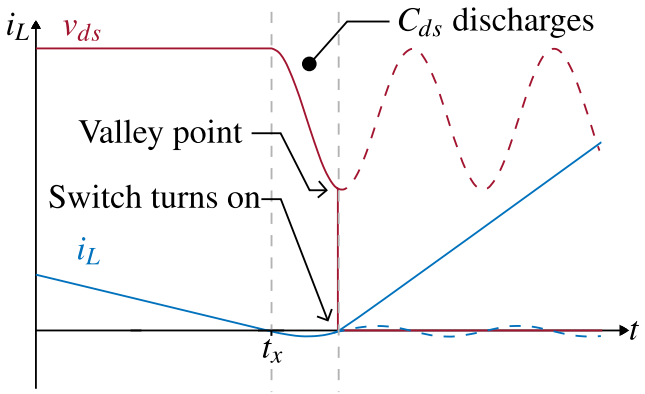


Figure 3.9. Near-zero-voltage switching $v_{in} > \frac{1}{2}v_o$.

3.2.1 Zero-Current Detection

The valley switching is achieved in the experimental prototype by using the ZCD circuit shown in Figure 3.10.

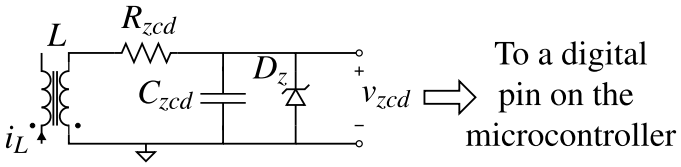


Figure 3.10. Zero-current-detection circuit.

The ZCD circuit consists of an auxiliary winding on the boost inductor, a current-limiting resistor R_{zcd}, a capacitor C_{zcd} that adds a small amount of low-pass filtering and a Zener diode D_z that clamps the voltage v_{zcd} to between 0 and 5 V, so that it can be input to a microcontroller pin. Figure 3.11 shows a timing diagram of the inductor current, inductor voltage v_L and the voltage v_{zcd} created by the ZCD circuit. The voltage v_{zcd} is a square wave,

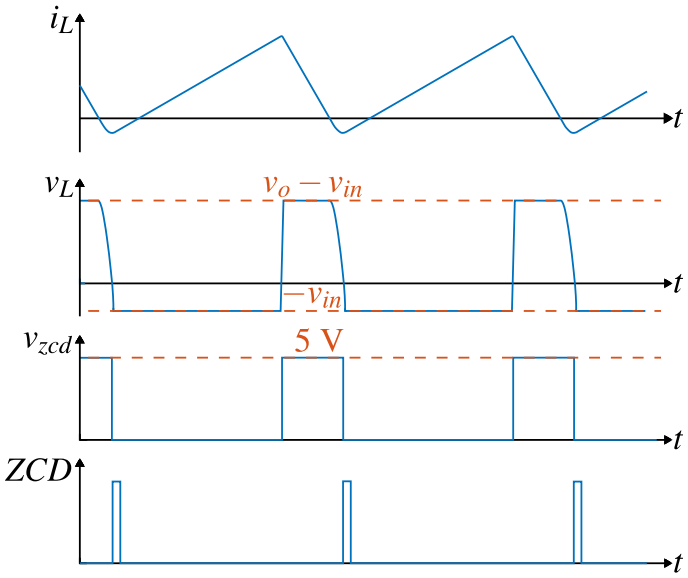
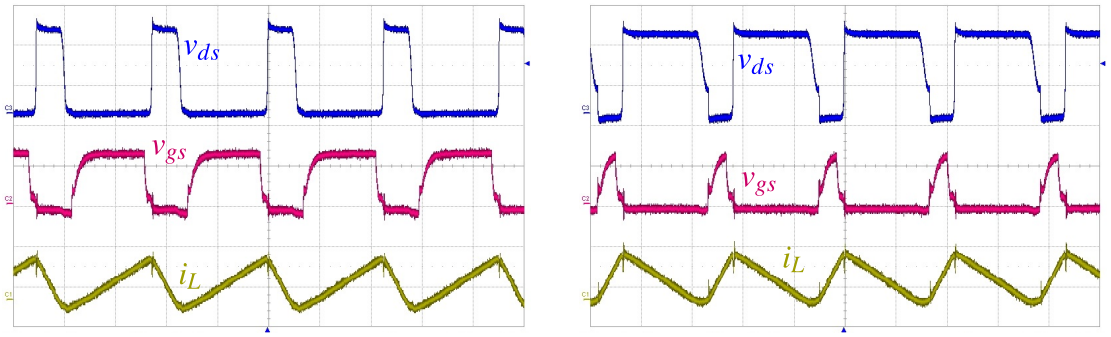


Figure 3.11. Timing diagram for the ZCD generation.

with a falling edge that corresponds to the instant that the boost converter MOSFET should

be turned on to achieve valley switching. The voltage v_{zcd} is connected to a regular digital pin on the microcontroller, and the PWM peripheral is configured to trigger MOSFET turn-on on a falling edge of this signal. This method is advantageous because it does not require a comparator, thus making the implementation cheaper. Requiring an external comparator would add cost. Additionally, any available comparators in the microcontroller can now be used for safety functions, such as over-voltage and over-current protections.

Figure 3.12 shows experimental results of the prototype converter operating in BCM with valley switching when $v_{in} = 100$ V and $v_{in} = 300$ V. The figures demonstrate that when the input voltage is 100 V, the MOSFET drain-souce voltage fully discharges to zero, and zero-voltage switching is achieved. Conversely, when the input voltage is 300 V, the drain-source voltage discharges to a valley point of approximately 100 V, and near-voltage switching is achieved. In both cases the MOSFET turns on with zero-current switching.



(a) (b)

Figure 3.12. v_{ds}, v_{gs} and i_L waveforms showing valley switching for (a) v_{in} = 100 V and (b) v_{in} = 300 V (v_{ds}: 200 V/div, v_{gs}: 10 V/div, i_L: 2 A/div, timebase : 2 µs/div).

3.3 System Model

In this section the design of the phase-shift control algorithm is discussed. The phase-shift control is responsible for maintaining the correct phase shift between the boost inductor currents.

The phase-shift control algorithm takes the on-time calculated by the voltage compensator and adjusts it to calculate the individual on-time for each channel of the converter to maintain the desired phase shift between the different channels.

First, it is necessary to develop a mathematical system model to design the phase-shift control algorithm. The model describes how adding a perturbation of $t_{\Delta n}$ to the individual on-time of the n^{th} slave channel affects the phase shift t_{psn} between the master channel and the n^{th} slave channel. The on-time of the master channel is denoted t_{on1}. The on-time of the n^{th} slave channel is denoted t_{onn}. If the on-time of the master and slave channel are initially equal in value, and thena perturbation of $t_{\Delta n}$ is added to the slave channel's on-time, the slave channel on-time becomes

$$t_{onn} = t_{on1} + t_{\Delta n} \tag{3.1}$$

The effect of adding this perturbation to the on-time t_{onn} is shown in Figure 3.13 over a single switching cycle of the inductor currents i_{L1} and i_{Ln}, where i_{L1} is the inductor current of the master channel, and i_{Ln} is the inductor current of the n^{th} boost-converter channel. It is assumed that the effects of the resonance between the boost inductor and MOSFET drain-source capacitance are negligible in order to simplify our analysis. If $t_{psn}[k]$ is the phase shift between the master and n_{th} slave channel during the k^{th} switching cycle, the phase shift of the $(k+1)^{th}$ switching cycle can be calculated by

$$t_{psn}[k+1] = t_{psn}[k] + \frac{t_{\Delta 1} t_{sw1}}{t_{on1}} \tag{3.2}$$

where t_{sw1} is the switching period of the master channel. This change in the phase shift is graphically displayed in Figure 3.13. By expanding (3.2) over a total of K switching cycles, the phase shift of the $(k+K)^{th}$ switching cycle can also be calculated by (3.3), where it is assumed that the t_{sw1} and t_{on1} remain constant over the K switching cycles.

$$t_{psn}[k+K] = t_{psn}[k] + K\frac{t_{\Delta n} t_{sw1}}{t_{on1}} \tag{3.3}$$

The open-loop system model is now described by (3.3). This equation is used in the next section to design a closed feedback loop to control the phase shift t_{psn}.

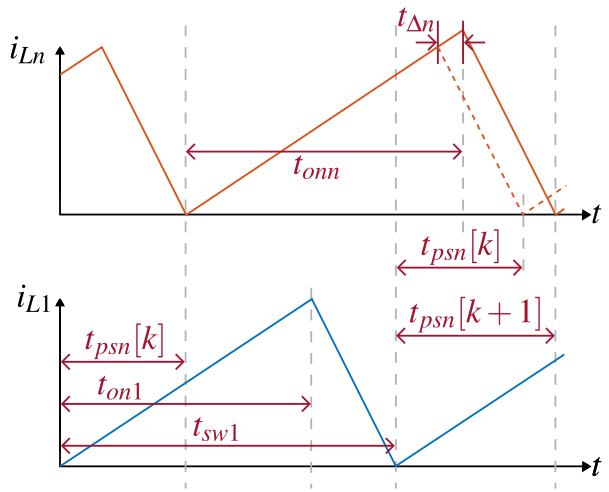


Figure 3.13. Change in phase shift due to an on-time perturbation $t_{\Delta n}$.

3.4 Closed-Loop Control

Closed-loop control is used to ensure that the phase shift t_{psn} tracks a reference phase shift t_{refn}. Figure 3.14 shows the proposed structure of the phase-shift control loop. The error signal given by $t_{refn} - t_{psn}$ is multiplied by the gain k_m to form a proportional controller, and the result is added to the on-time t_{on1} to give the on-time t_{onn} for that slave channel.

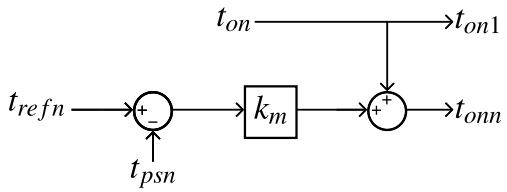


Figure 3.14. Phase-shift control loop block diagram structure.

The value of k_m must be selected to obtain the best tracking performance while still ensuring the stability of the system under all operating conditions. The phase-shift control algorithm can be described by the following equation:

$$t_{onn} = t_{on1} + k_m(t_{refn} - t_{psn}[k]) \tag{3.4}$$

Substituting $t_{\Delta n} = t_{onn} - t_{on1}$ into (3.4), the following expression is obtained.

$$t_{\Delta n} = k_m(t_{refn} - t_{psn}[k]) \tag{3.5}$$

By combining (3.5) with the expression obtained earlier in (3.3), the effect of the phase-shift control feedback on the phase shift t_{psn} after K switching cycles can be obtained as follows.

$$t_{psn}[k+K] = t_{psn}[k] + Kk_m\frac{t_{sw1}}{t_{on1}}(t_{refn} - t_{psn}[k]) \tag{3.6}$$

The phase-shift control algorithm given in (3.4) is executed at a constant sampling rate,

with a sampling period of T_m. A total of $K = T_m/t_{sw1}$ switching cycles occur over a single execution of the phase-shift control algorithm. A time-averaged approximation is taken by substituting this value of k into (3.6). As a result, the value of the phase shift t_{psn} after a single execution of the algorithm can be obtained as follows.

$$t_{psn}[i+1] - t_{psn}[i] = k_m \frac{T_m}{t_{on1}}(t_{refn} - t_{psn}[i]) \tag{3.7}$$

where i is an integer number describing the number of executions of the phase-shift control algorithm which have taken place. For ideal phase-shift tracking, the value of t_{psn} after a single execution of the algorithm should equal t_{refn}. Therefore, (3.7) becomes

$$t_{refn} - t_{psn}[i] = k_m \frac{T_m}{t_{on1}}(t_{refn} - t_{psn}[i]) \tag{3.8}$$

By re-arranging (3.8), the value of k_m that gives the best tracking performance can be calculated as

$$k_m = \frac{t_{on1}}{T_m} \tag{3.9}$$

3.4.1 Phase-Shift Control Stability

The phase-shift control loop remains stable provided that after a single execution of the phase-shift control algorithm, the phase shift t_{psn} stays bound to the region $0 < t_{psn} < t_{sw1}$. Re-arranging (3.7), the following equation can be found to describe the phase shift t_{psn} after $(i+1)$ execution cycles of the control algorithm,

$$t_{psn}[i+1] = k_m \frac{T_m}{t_{on1}}(t_{refn} - t_{psn}[i]) + t_{psn}[i] \tag{3.10}$$

The phase shift $t_{psn}[i]$ is bound to the region $0 < t_{psn}[i] < t_{sw1}$. The worst-case scenario occurs when either $t_{psn}[i] = 0$ or $t_{psn}[i] = t_{sw1}$. Looking first at the case where $t_{psn}[i] = 0$, $t_{psn}[i+1]$ is given by

$$t_{psn}[i+1] = k_m \frac{T_m}{t_{on1}} t_{refn} \tag{3.11}$$

Applying this result to the inequality $0 < t_{psn}[i+1] < t_{sw1}$, the following inequality can be obtained for the values of k_m for which the system is stable.

$$0 < k_m < \frac{t_{on1}}{T_m} \frac{t_{sw1}}{t_{refn}} \tag{3.12}$$

Now looking at the case where $t_{ps1}[i] = t_{sw1}$, $t_{psn}[i+1]$ is given by,

$$t_{psn}[i+1] = k_m \frac{T_m}{t_{on1}}(t_{refn} - t_{sw1}) + t_{sw1} \tag{3.13}$$

Again, applying the result from (3.13) to the inequality $0 < t_{psn}[i+1] < t_{sw1}$, a second inequality can be obtained for the values of k_m for which the system remains stable.

$$0 < k_m < \frac{t_{on1}}{T_m} \frac{t_{sw1}}{t_{sw1} - t_{refn}} \tag{3.14}$$

The inequalities given in (3.12) and (3.14) now describe the values of k_m for which stability is achieved in terms of the tracking reference t_{refn}. The reference signal is calculated from the switching period t_{sw1} by $t_{refn} = t_{sw1} \frac{n-1}{N}$. Substituting this value for t_{refn} into the inequalities (3.12) and (3.14) gives the following.

$$0 < k_m < \frac{t_{on1}}{T_m} \frac{N}{n-1} \tag{3.15}$$

and

$$0 < k_m < \frac{t_{on1}}{T_m} \frac{N}{N-n+1} \tag{3.16}$$

However, n is an integer number, with a value in the region $2 \leq n \leq N$. The strictest condition to satisfy (3.15) occurs when n is at its maximum value of $n = N$. Similarly for (3.16), the strictest condition occurs when n is at its minimum value of $n = 2$. Applying the strictest condition for n to both (3.15) and (3.16) results in the following single inequality.

$$0 < k_m < \frac{t_{on1}}{T_m} \frac{N}{N-1} \tag{3.17}$$

For 2-channel operation $N = 2$, so that k_m must satisfy $0 < k_m < 2\frac{t_{on1}}{T_m}$ to remain stable. Figure 3.15 demonstrates the waveshape of the input current drawn by the converter in 2-channel operation when k_m satisfies the stability inequality and when k_m is increased so that it no longer satisfies this inequity.

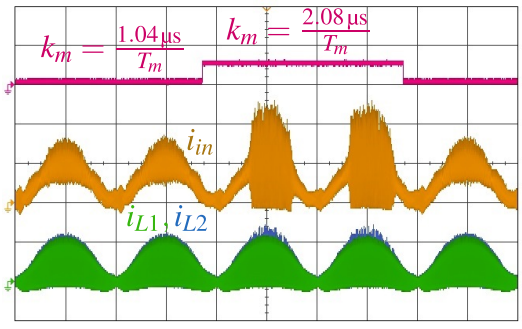


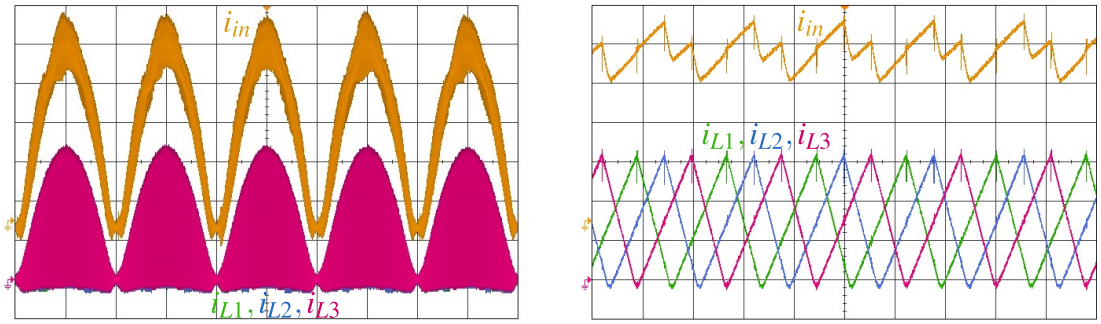
Figure 3.15. Input current i_{in} and inductor currents i_{L1} and i_{L2} when the gain k_m is toggled from a value of $k_m = \frac{1.04\,\mu s}{T_m}$ to a value of $k_m = \frac{2.08\,\mu s}{T_m}$ at P_o = 225 W and 200 Vrms. (i_{in}: 2 A/div, i_{L1}: 2 A/div, i_{L2}: 2 A/div, timebase : 5 ms/div).

Figure 3.15 is taken at an output power of 225 W, and an input rms voltage of 200 V. Under this condition the measured on-time t_{on1} is 0.9 µs. For the initial two half-line cycles, the gain k_m is set to a value of $k_m = \frac{1.04\,\mu s}{T_m}$. Therefore, the stability inequality given by $0 < k_m < \frac{1.8\,\mu s}{T_m}$ is satisfied, and the input current maintains the correct interleaving with low

peak-to-peak current ripple. The gain k_m is then increased to $k_m = \frac{2.08\,\mu s}{T_m}$ so that the stability inequality is not satisfied. The phase-shift control loop is no longer able to maintain correct interleaving and the input current has a very large peak-to-peak ripple. For the last half-line cycle shown in the figure, k_m is reduced again to $k_m = \frac{1.04\,\mu s}{T_m}$ and the system becomes stable once more.

3.4.2 Adaptive Gain

If a proportional control scheme is used where k_m has a constant value, then k_m must be set to satisfy the stability inequality (3.17). Therefore, the value of k_m is designed based on the minimum on-time $t_{on(min)}$ that occurs for multi-channel operation and can be calculated by $k_m = \frac{t_{on(min)}}{T_m}$. A minimum on-time exists because at lighter loads the converter turns off channels until only a single channel is operating. At low power levels this value for k_m works well because its value is close to the value that gives the best tracking performance, as described by (3.9). However, when the converter is operating at high power levels and low input voltage the on-time dramatically increases. As a result, the chosen value for k_m becomes much less than the value given by (3.9). This effect is shown in Figure 3.16 when the on-time is at its maximum operating value at P_o = 700 W and 115 Vrms. This is the maximum rated power of the prototype converter at low line voltage. The value of k_m has been set to $\frac{0.8\,\mu s}{T_m}$.



(a) (b)

Figure 3.16. i_{L1}, i_{L2}, i_{L3} and i_{in} when all 3 boost converter channels are enabled at P_o = 700 W and a rms line voltage of 115 V when k_m is a constant gain (i_{in}: 2 A/div, i_{L1}: 2 A/div, i_{L2}: 2 A/div). (a) Line frequency components (timebase : 5 ms/div). (b) Switching frequency components (timebase : 5 µs/div).

The input current shown in Figure 3.16 has a large peak-to-peak input-current ripple. This is caused by the poor tracking performance of the phase-shift control at this condition. This problem can be overcome by introducing an adaptive gain that scales the value of k_m with the operating on-time t_{on1} using the value of k_m obtained in (3.9). Thus, for best tracking performance the proportional gain k_m is replaced with a multiplier block that multiples the error signal by t_{on1} and a proportional gain of $1/T_m$, as is shown in Figure 3.17.

Figure 3.18 shows the same waveforms as Figure 3.16 at the same operating condition but when an adaptive gain is used for k_m. By comparing the waveforms of Figure 3.16 to

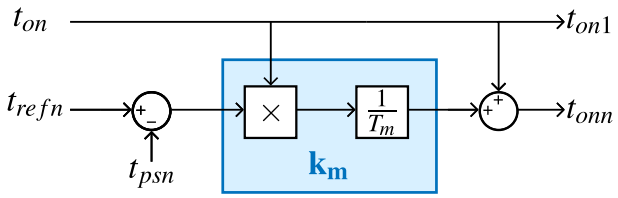
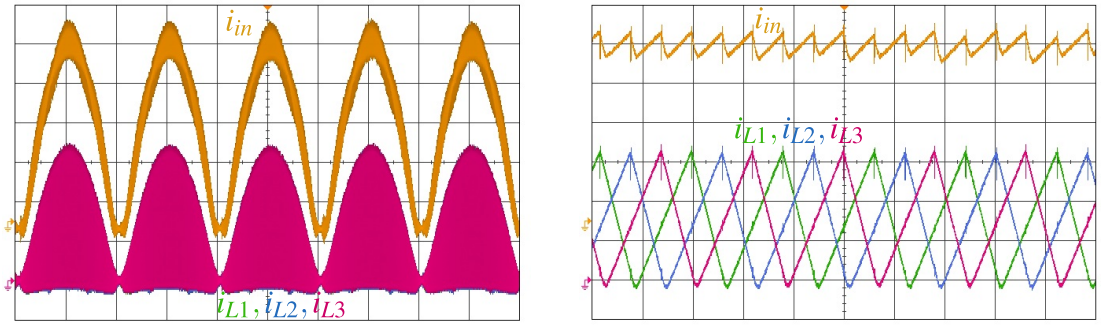


Figure 3.17. Phase-shift control loop block diagram structure when an adaptive gain is used.

Figure 3.18 it is clear that using an adaptive gain dramatically reduces the input current peak-to-peak ripple, and improves the tracking performance of the phase-shift control loop. Additionally, given that the the value of k_m used for the adaptive gain always satisfies the stability inequality given in (3.17), it is evident that the use of an adaptive gain always ensures the phase-control loop remains stable for all values of t_{on}.



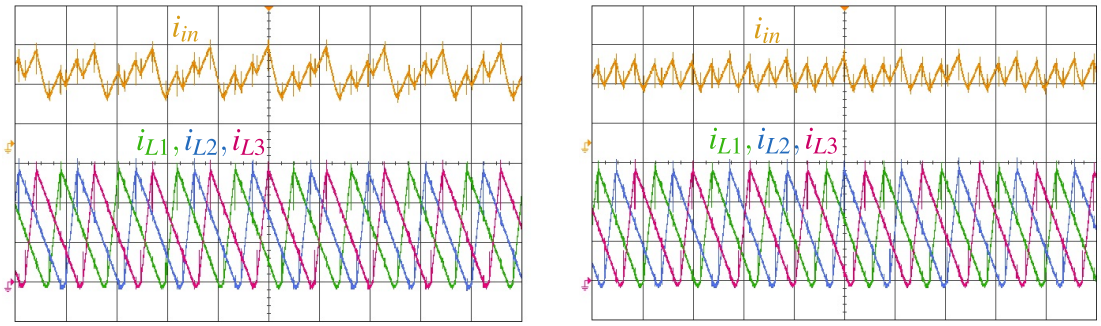
(a) (b)

Figure 3.18. i_{L1}, i_{L2}, i_{L3} and i_{in} when all 3 boost converter channels are enabled at P_o = 700 W and 115 Vrms when k_m is an adaptive gain (i_{in}: 2 A/div, i_{L1}: 2 A/div, i_{L2}: 2 A/div). (a) Line frequency components (timebase : 5 ms/div). (b) Switching frequency components (timebase : 5 µs/div).

3.4.3 Appropriate Value for T_m

Choosing an appropriate value of the rate of execution of the phase-shift control algorithm is important, because the slower the control algorithm, the less computational power is required to execute it. Therefore, a cheaper the microcontrollercan be used. However if the the value of T_m is set too long, there exists significant quantization error in the phase-shift control loop. This phenomenon is worst at low levels of on-time and switching period, which exist at high input voltage, and the lowest power level for the operation of a given number of channels. Figure 3.19 demonstrates the waveshape of the input current and inductor currents when 3 channels of the boost converter are enabled at 600 W output and 230 Vrms.

This is the near worst-case operating condition for the quantization noise created when T_m is too slow, as it is near the maximum input voltage and minimum power for 3-channel operation. Below this power level the converter switches to 2-channel operation increasing the switching period and on-time and decreasing this type of quantization error. In Figure 3.19(a) the value of T_m is set to 30 µs, whereas in Figure 3.19(b), the value of T_m is set to 10 µs. It is clear from comparing both figures, that having T_m set to too low a value results in



(a) (b)

Figure 3.19. i_{L1}, i_{L2}, i_{L3} and i_{in} when all 3 boost converter channels are enabled at P_o = 600 W and a rms line voltage of 230 V (i_{in}: 2 A/div, i_{L1}: 2 A/div, i_{L2}: 2 A/div, timebase : 5 µs/div). (a) When T_m is set to have an execution frequency of 34 kHz (b) and when T_m is set to have an execution frequency of 100 kHz.

poor tracking performance.

3.4.4 Fixed-Point Implementation

The gain term $\frac{1}{T_m}$ shown in Figure 3.17 must be calculated in units of ticks^{-1} instead of s^{-1} to execute the phase-shift control algorithm with a fixed-point implementation. The gain must also be scaled by a factor 2^{Am} so that it is suitably high to not suffer from the integer rounding associated with fixed-point math. This creates a new fixed-point phase-shift gain K_m, that can be calculated as

$$K_m = \text{round}\left\langle \frac{1}{T_m f_{pwm}} 2^{A_m} \right\rangle \tag{3.18}$$

This scaling is demonstrated in the control-loop block diagram for a fixed-point implementation is shown in Figure 3.17.

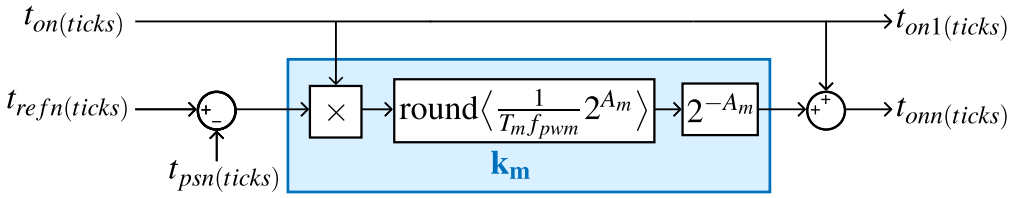


Figure 3.20. Phase-shift control-loop block diagram when an adaptive gain is used with a fixed-point implementation.

As the term A_m becomes larger, the rounding error for the coefficient K_m becomes lower. However, if the term A_m is set too high it can cause positive or negative integer overflow. For a 16-bit signed integer implementation, the following inequality must be satisfied to prevent positive integer overflow.

$$\max\left\langle (t_{refn(ticks)} - t_{psn(ticks)}) \frac{1}{T_m f_{pwm}} 2^{A_m} \right\rangle < 2^{15} \tag{3.19}$$

The reference phase-shift in ticks $t_{refn(ticks)}$ is equal to the sensed switching period of

the master boost-converter channel in ticks. Since the PWM peripherals are configured to have a minimum switching frequency of 20 kHz, this corresponds to a maximum period of $\frac{20\text{ kHz}}{f_{pwm}} = \frac{20\text{ kHz}}{96\text{ MHz}} = 4800$ ticks. The reference phase-shift of the n^{th} channel is calculated as the switching period of the master channel times $\frac{n-1}{N}$. Hence, for a 3-channel boost converter, t_{refn} has a maximum value of $(\frac{2}{3})(4800)$ ticks or 3200 ticks. The sensed phase-shift has a minimum value of zero ticks. Thus (3.19) can be simplified and solved as follows.

$$(3200)\frac{f_{pwm}}{T_m}2^{A_m} < 2^{31}$$

$$2^{A_m} < 2^{15}\frac{T_m f_{pwm}}{(3200)}$$

$$A_m < \log_2\left(2^{15}\frac{T_m f_{pwm}}{(3200)}\right)$$

$$A_m < \log_2\left(2^{15}\frac{(96\text{ MHz})}{(70\text{ kHz})(3200\text{ ticks})}\right)$$

$$A_m < 13.77 \tag{3.20}$$

To prevent negative integer overflow the following inequality must be satisfied.

$$\min\left\langle (t_{refn(ticks)} - t_{psn(ticks)})\frac{1}{T_m f_{pwm}}2^{A_m}\right\rangle > -2^{15}+1 \tag{3.21}$$

The reference phase-shift has a minimum value of $\frac{1}{N}$ times the maximum switching period, which is $\frac{1}{N}(4800)$ ticks or 1600 ticks. While the sensed phase-shift has a maximum value equal to the maximum value of the switching period, which is 4800 ticks. Hence (3.21) can be simplified and solved as follows.

$$(1600-4800)\frac{1}{T_m f_{pwm}}2^{A_m} > -2^{15}+1$$

$$2^{A_m} < (2^{15}-1)\frac{T_m f_{pwm}}{(3200)}$$

$$A_m < 13.77 \tag{3.22}$$

Therefore to prevent both positive and negative integer overflow the term A_m was set to 13, and the gain K_m was calculated as 5.

3.5 Software Flow

The phase-shift control algorithm is executed in a fast interrupt at an execution period equal to T_m. This interrupt has the highest priority, so that it can interrupt the voltage-loop interrupt, but the voltage-loop interrupt cannot interrupt it. If the voltage-loop interrupt is set while the phase-shift interrupt is being executed, the CPU completes execution of the phase-shift control interrupt function, and then begins the execution of the voltage-loop interrupt function.

A software-flow block diagram of the phase-shift interrupt for the 3-channel BCM boost converter prototype is given in Figure 3.21. The interrupt then proceeds to run the fixed-point

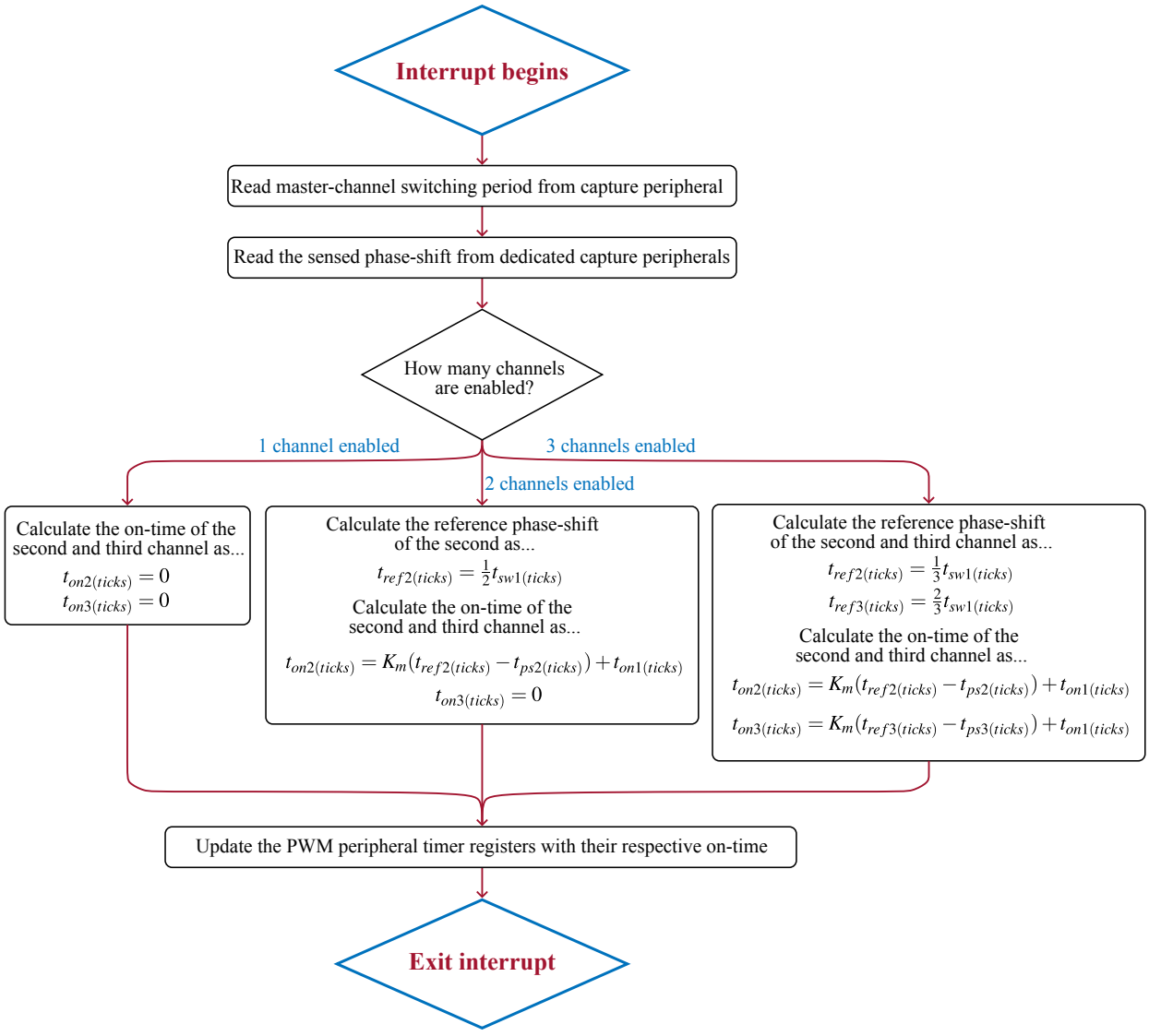


Figure 3.21. Software-flow block diagram description of the phase-shift control interrupt function.

phase-shift control algorithm with 16-bit mathematics. As the phase-shift control algorithm varies depending on the number of enabled channels, a switch statement is used to alter the algorithm depending on the number of enabled channels. The number of enabled channels is calculated in the voltage-loop interrupt as part of the phase-shedding function, similarly the

calculated on-time is also scaled depending on the number of channels in the voltage-loop interrupt. If only a single channel is enabled, then the on-times of the second and third channels are set to zero. If two channels are enabled, the reference phase-shift is set to half the sensed switching period, the on-time of the second channel is calculated,by the phase-shift control law described in Figure 3.20, and the on-time of the third channel is disabled. If the third channel is enabled, the reference phase shift of the second and third channel are set to one third and two thirds of the sensed switching period, respectively. Then the on-time of both the second and third channels are calculated as described by Figure 3.20.

Once the on-time of each channel is calculated, the dedicated PWM peripheral register for each channel is updated, and the interrupt is complete.

3.6 Experimental Results

The 3-channel experimental prototype described in Chapter 2 was used to verify the proposed digital phase-shift control scheme. The main power-stage parameters of the 3-channel boost converter are described in Table 2.1. The microcontroller runs the code for the voltage-loop in a slow 5 kHz interrupt. The code for the phase-shift control is run in a faster 70 kHz interrupt. Thus, the phase-shift control sampling period T_m was equal to 14.3 µs. The switching frequency of the converter is a complex function of input voltage, output power, on-time and boost inductance, the switching frequency variation of the prototype described in this work was 70 kHz to 700 kHz.

Figure 3.22 shows the inductor currents and input current when operating at a low input line voltage of 115 V in 2-channel operation. Near-perfect interleaving operation is maintained at this operating condition. Figure 3.22(c) shows the same waveshapes, but at the zero-crossing point of the line voltage, demonstrating that the control scheme also works well at this point.

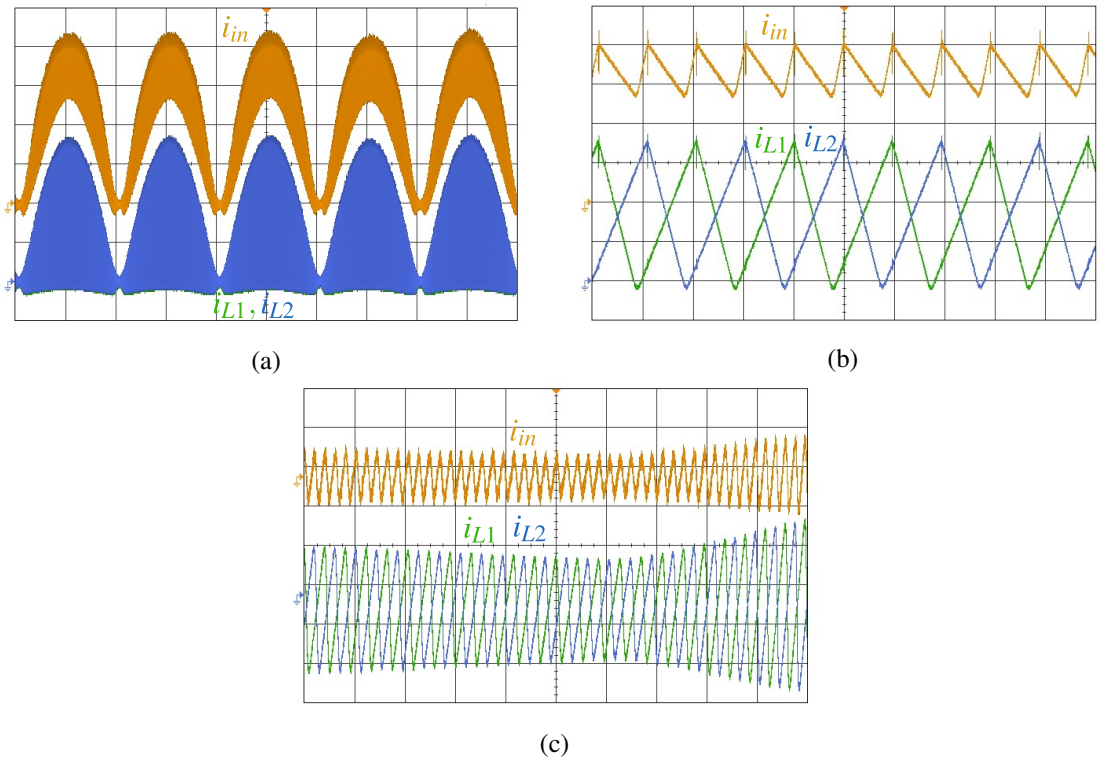
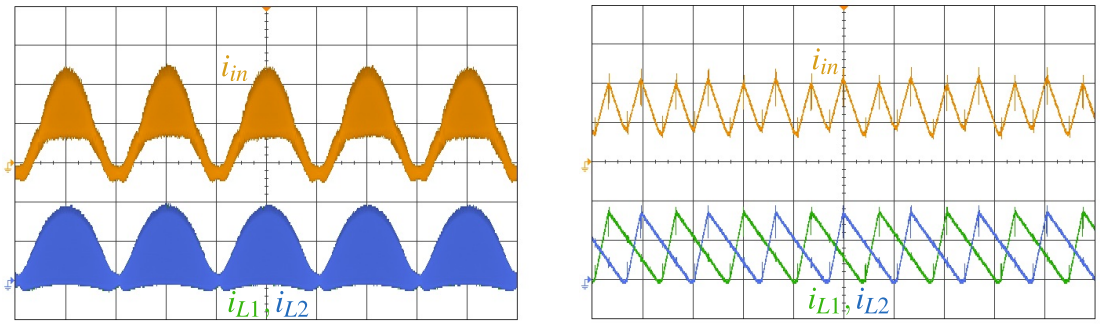


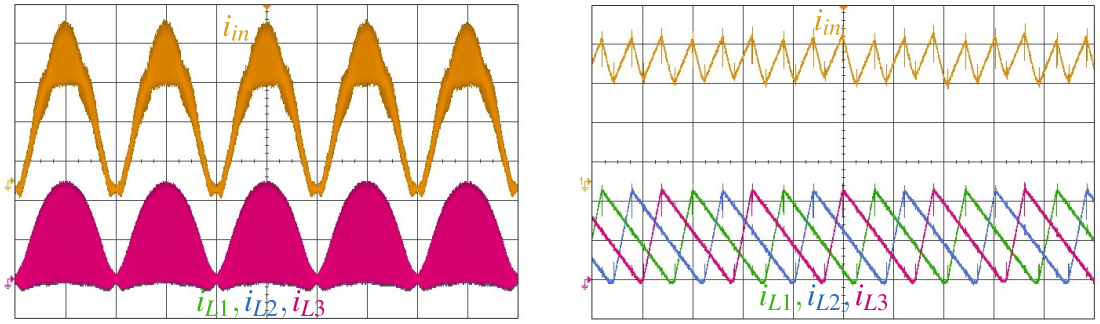
Figure 3.22. i_{L1}, i_{L2} and i_{in} when 2 boost converter channels are enabled at P_o = 500 W and 115 Vrms (i_{in}: 2 A/div, i_{L1}: 2 A/div, i_{L2}: 2 A/div). (a) Line frequency components (timebase : 5 ms/div). (b) Switching frequency components (timebase : 5 µs/div). And (c) at the zero-crossing point of the line voltage (i_{in}: 200 mA/div, i_{L1}: 100 mA/div, i_{L2}: 100 mA/div, timebase : 20 µs/div) .

Figure 3.23 shows the converter operating at 500 W and 230 Vrms. Near-perfect interleaving operation can be observed when operating in 2-channel mode at this operating condition, as demonstrated by the perfect shape of the input current i_{in}, and the low peak-to-peak current ripple.



(a) (b)

Figure 3.23. i_{L1}, i_{L2} and i_{in} when 2 boost converter channels are enabled at P_o = 500 W and a rms line voltage of 230 V (i_{in}: 2 A/div, i_{L1}: 2 A/div, i_{L2}: 2 A/div). (a) Line frequency components (timebase : 5 ms/div). (b) Switching frequency components (timebase : 5 µs/div).



(a) (b)

Figure 3.24. i_{L1}, i_{L2}, i_{L3} and input current i_{in} when all 3 boost converter channels are enabled at P_o = 1 kW and a rms line voltage of 230 V (i_{in}: 2 A/div, i_{L1}: 2 A/div, i_{L2}: 2 A/div). (a) Line frequency components (timebase : 5 ms/div). (b) Switching frequency components (timebase : 5 µs/div).

Similarly, Figure 3.24 shows the converter operating with 3 channels enabled at the full rated output power of 1 kW with an input rms line voltage of 230 V. There is near-perfect interleaving operation at this operating condition, as demonstrated again by the low peak-to-peak current ripple of the input current.

At lighter loads, either one or two channels of the converter are shut-off to improve the converter's efficiency and also reduce the switching frequency of the converter, which increases drastically at lighter loads. Therefore, the phase-shift control algorithm needs to be capable of operating with either one channel enabled, two channels enabled, or with all three channels enabled. Fig. 3.25 shows the waveshape of the inductor currents and input currents when the converter transitions from 3-channel to 2-channel operation.

At the instant the phase-shift control loop changes from 3-channel operation to 2-channel operation, the third channel is disabled, and the on-time t_{on} is scaled by a factor of $3/2$. This keeps the average instantaneous input current the same. The phase-shift control loop which controls t_{ps3} is disabled and the reference of the phase-shift control loop controlling t_{ps2} is stepped from $t_{sw1}/3$ to $t_{sw1}/2$. It then takes the controller two to three cycles of the phase-shift control algorithm execution to transition from a 120° phase shift, to a 180° phase

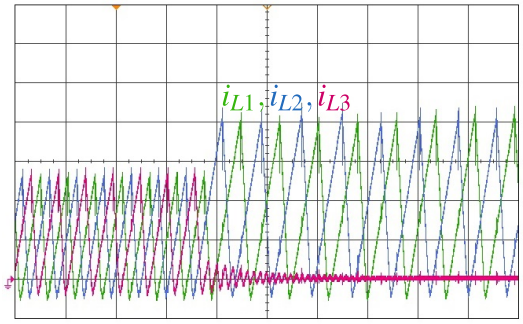


Figure 3.25. i_{L1}, i_{L2} and i_{L3} when entering 2-channel BCM (i_{L1}: 1 A/div, i_{L2}: 1 A/div, i_{L3}: 1 A/div, timebase : 30 µs/div).

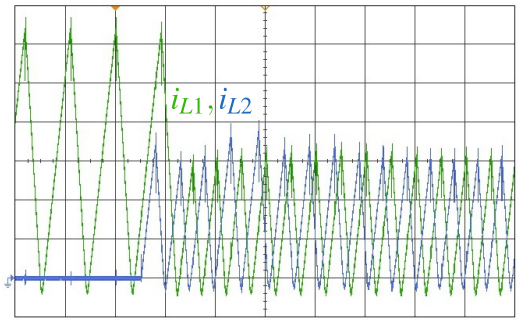


Figure 3.26. i_{L1} and i_{L2} when entering 2-channel BCM (i_{L1}: 1 A/div, i_{L2}: 1 A/div, timebase : 30 µs/div)

shift. A similar transition occurs when the converter transitions from 2-channel to 3-channel operation.

Figure 3.26 shows the inductor currents as the converter transitions from single-channel operation to 2-channel operation. When the second channel and phase-shift control loop for t_{ps2} are re-enabled, t_{ps2} has a random initial value in the range $0 < t_{ps2} < t_{sw1}$. The phase-shift control loop takes two to three executions before t_{ps2} settles to its reference at $t_{sw1}/2$. This transition is shown in Figure 3.26.

The main advantage of disabling the boost converter channels at lower power levels is that it increases the converter's efficiency at lighter load. The efficiency of the prototype converter is given in Figure 3.27(a) for an input 230 Vrms, while Figure 3.27(b) gives the efficiency for 115 Vrms. It is clear that at lighter load, reducing the number of channels increases efficiency. This is mainly due to the lower switching frequency which reduces switching losses and inductor core losses.

A similar effect is seen when comparing the power factor in 1-channel, 2-channel and 3-channel operation. This comparison against output power is given in Figure 3.28(a) for 230 Vrms, and in Figure 3.28(b) for 115 Vrms. It is evident from these figures that disabling the number of channels at lighter load increases the power quality of the converter. At higher power levels it is better to use multiple channels to reduce current stress and thermal stress in components, as well as the DM conducted EMI drawn by the converter.

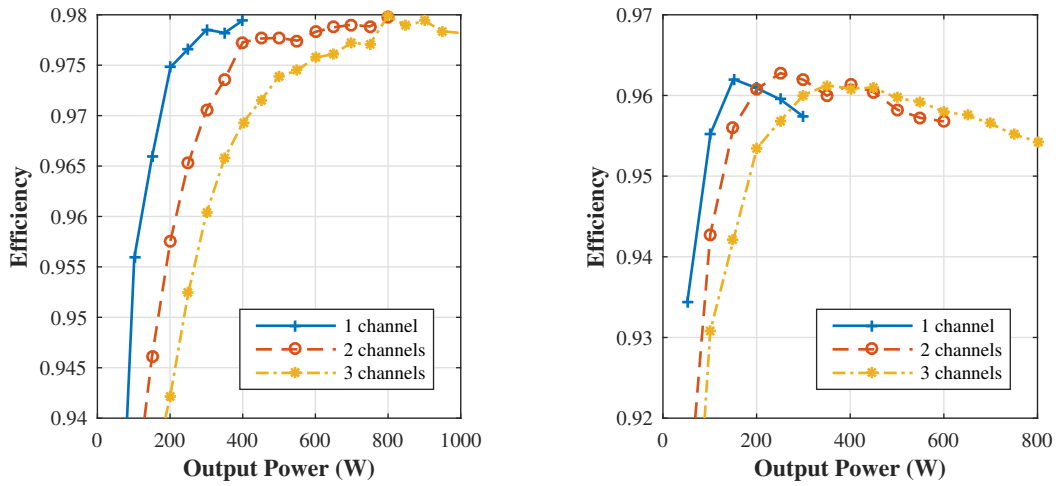


Figure 3.27. Efficiency against output power for 1-channel, 2-channel and 3-channel operation at (a) 230 Vrms and (b) 115 Vrms.

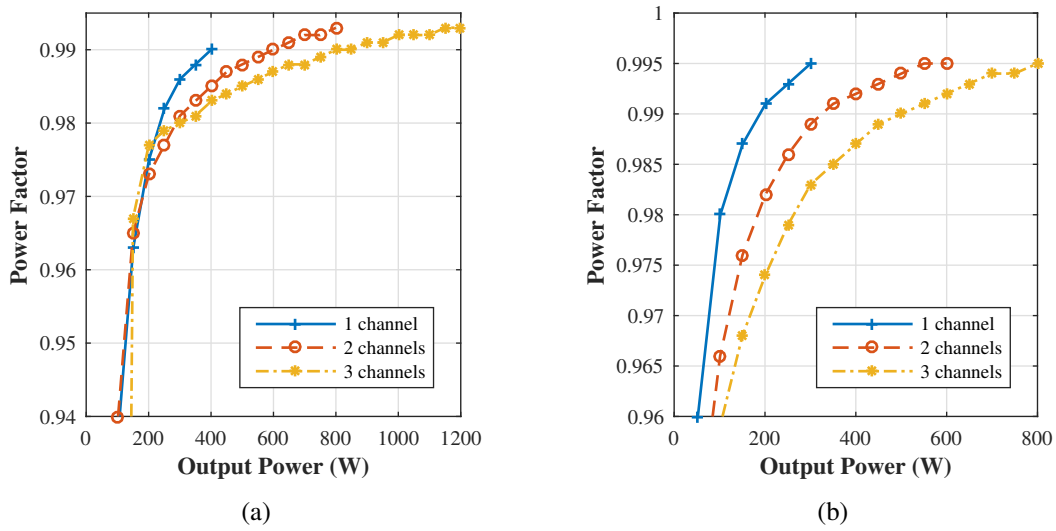


Figure 3.28. Power factor against output power for 1-channel, 2-channel and 3-channel operation at (a) 230 Vrms and (b) 115 Vrms .

3.7 Conclusion

A closed-loop digital control strategy maintaining correct interleaving operation of a multi-channel BCM boost converter has been presented. The importance of using separate ZCD circuits for each channel of the interleaved converter to maintain valley-switching operation has been discussed, and details of how the ZCD circuit interfaces with the microcontroller were given.

A digital closed-loop control scheme to maintain correct interleaving operation of the converter was proposed. A mathematical analysis was derived to find the gain of a proportional controller which provided the best tracking performance and maintained stability of the control loop. An adaptive gain was incorporated into the control loop to give the best

tracking performance and ensure stability under all operating conditions. A design method was given to implement the controller with fixed-point arithmetic.

Finally, the experimental results of a prototype 3-channel converter, demonstrates correct interleaving operation of the converter operating in 2-channel and 3-channel modes over the converter's full range of line voltage and output power. Experimental results demonstrated how the converter performed phase shedding by disabling the number of operating boost converter channels at lighter loads. The advantages of phase shedding at lighter loads were explored experimentally, demonstrating that the converter exhibits better efficiency and power factor over the entire output power range when phase shedding is implemented.

4 FEEDFORWARD CONTROL

This chapter proposes a simple and effective digital feedforward algorithm to improve the power quality of a boundary-conduction-mode (BCM) boost converter for power-factor-correction (PFC) applications. BCM boost converters suffer from a zero-crossing distortion of the line current caused by the valley switching of the converter. The feedforward algorithm works by increasing the switch on-time around the zero crossing of the line voltage, which in turn increases the line current at this point. The feedforward algorithm has a very simple design procedure with the implementation requiring only a single look-up table (LUT) in microcontroller software. Experimental results are given for a prototype converter demonstrating a significantly improved power quality, when the feedforward algorithm is used.

Results of this chapter have been published in the following paper,

- R. T. Ryan, D. N. Hogan, R. J. Morrison and J. G. Hayes, "Using feedforward digital control to improve the power quality of a three-channel BCM boost converter for PFC applications", *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, 2019, pp. 1743-1750.

4.1 Introduction

The BCM boost converter suffers from a zero-crossing distortion of the line current. This distortion is predominately caused by the valley-switching operation of the converter. The valley switching results in a slightly negative inductor current at the instant before switch turn on, which distorts the line current causing it to become near zero at the zero crossings of the line voltage. This reduces the converter's power factor. The input line current is further distorted by the current drawn by the input filter capacitor. The voltage across the input filter capacitor is a rectified sinusoid with a period of twice the line frequency. This voltage causes significant current, at harmonics of the line frequency, to flow through the input filter capacitor. The current drawn by the input capacitor distorts the line current drawn by the converter, giving it a phase-leading characteristic.

Different solutions have been proposed in the literature to reduce the distortion of the line current. These solutions can be divided into a variable on-time feedforward method or a closed-loop average-current-mode control (ACMC) method. In this chapter, the use of the variable on-time feedforward method is explored to improve the converter's power quality.

The most popular solution is to increase the on-time around the zero-crossings using feedforward control as a function of the sensed input voltage only. Increasing the on-time at the zero-crossing of the line current allows the converter to pull a larger input current, therefore cancelling the effects of the line-current distortion attributed to the valley-switching operation. An analog solution is proposed in [23], where the slope of the PWM ramp generation signal is varied with input voltage in order to increase the on-time at the zero-crossing points. Although this allows for a simple and cost-effective implementation, the method must be tuned experimentally for best results, leading to a difficult design procedure for optimal results. Similarly in [29], [30] an additional on-time is calculated based on the instantaneous input voltage but must also be tuned experimentally. Another method is to theoretically derive the additional on-time required to cancel the valley switching effects as a function of input voltage only. This is implemented in [110] showing a significant improvement in power quality, but requires a complex numerical calculation to calculate the additional on-time needed. A limitation of the feedforward algorithm is that it does not reduce the input-capacitor distortion. In [17] this limitation is overcome by combining the feedforward variable on-time method to reduce the valley-switching distortion, with another feedforward method to reduce the distortion created by the input capacitor. A more accurate calculation of the additional on-time is required in order to improve the feedforward variable on-time method. Therefore, other solutions use more than just the input voltage to estimate the additional on-time needed, as in [33] where the optimal additional on-time is calculated as a function of input voltage, switching period and voltage compensator output. The function is then implemented in microcontroller software, but is complex, therefore requiring a high-cost

microcontroller. A theoretical analysis of the inductor current was carried out in order to predict its waveshape over a single switching cycle in [31]. Based on this analysis, an iterative algorithm was created to calculate the additional on-time needed to remove the valley-switching distortion. However, this implementation requires pre-loading different look-up tables into a microcontroller, and selecting the required on-time as a function of input voltage and input current, resulting in an expensive implementation. Therefore, the optimal on-time is derived in [32] by the same analysis, but curve fitting is used to find a simple function based on using input voltage only to calculate the additional on-time, allowing for a cheap and simple analog implementation, but also resulting in a complicated design procedure.

Another feedforward control method to reduce the zero-crossing distortion is to use analog peak-current-mode control, and to adjust the peak-current reference to increase the line current at the zero crossings, as in [16]. This method can also be extended to reduce the distortion caused by the input capacitor. Although this method works well, it can only be implemented with peak-current-mode control, which requires additional current-sense circuitry.

4.1.1 Proposed Solution

In this work, a digital feedforward control algorithm is proposed to improve the line-current distortion of a 3-channel BCM boost converter. The method is derived based on a theoretical analysis of the valley-switching operation. A feedforward algorithm is derived to calculate the additional on-time required to cancel the valley-switching distortion using only the sensed input voltage. This method allows for a very simple design procedure, does not require any experimental tuning, and also has a very easy implementation, as only a single look-up table is needed. The proposed feedforward algorithm provides a good improvement in power quality under all operating conditions.

This chapter is structured as follows, Section 4.2 gives a detailed analysis of the valley-switching operation of the converter. Section 4.3 introduces the simple feedforward algorithm used to reduce the line-current distortion, which is derived from the analysis given in Section 4.2. Finally, in Section 4.4 experimental results are demonstrated on the 1 kW interleaved 3-channel BCM boost converter. A significant improvement in the power quality of the converter is obtained when the feedforward algorithm is enabled.

4.2 Detailed Valley Switching Analysis

The line-current distortion is primarily due to the resonance between the MOSFET drain-source capacitance C_{ds} and the boost inductance L. The resonance has a dramatic effect on the shape of the inductor current waveform. Therefore, a review of the circuit operation for a single channel of the converter is worthwhile. Figure 4.1 shows a simplified circuit diagram of the boost converter including the MOSFET drain-source capacitor C_{ds} and body diode D_Q, without the input rectifier.

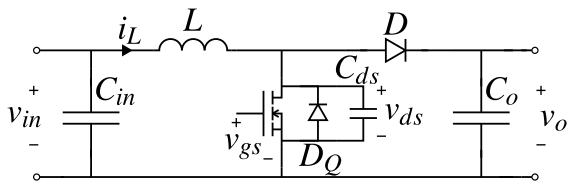


Figure 4.1. A single channel of the interleaved boost converter including the MOSFET drain-source capacitance and body diode.

If the boost diode, MOSFET and MOSFET's body diode are assumed to behave like ideal components, the circuit shown in Figure 4.1 can be described by three different modes of operation. The first mode of operation is when either the boost switch is closed, or a negative inductor current forces the MOSFET's body diode to conduct. In this case the circuit acts as shown in Figure 4.2. The boost diode becomes reversed biased and the large output capacitor makes the output voltage v_o act as a constant voltage source. Similarly as the input capacitor is much larger than the MOSFET drain-source capacitor, it can also be assumed to act as a constant voltage source, with a voltage of v_{in}. In this mode, the boost inductor current is charged by the input voltage. Therefore, the boost inductor current and MOSFET drain-source voltage v_{ds}, are given by (4.1) and (4.2).

$$i_L(t) = \frac{v_{in}}{L}t + i_L(0) \tag{4.1}$$

$$v_{ds}(t) = 0 \tag{4.2}$$

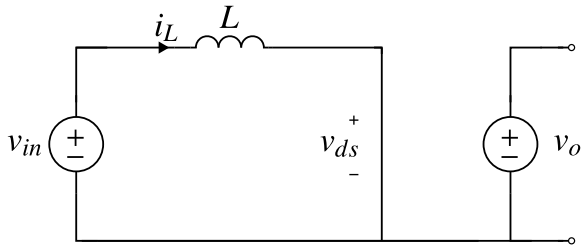


Figure 4.2. Equivalent circuit when the MOSFET or body diode conducts in Mode 1.

Figure 4.3 shows equivalent circuit of the boost converter in Mode 2. In this mode the boost diode and switch body diode are reversed biased, and the boost switch is off. In this

case the boost inductor and MOSFET drain-source capacitor resonate with each other. In this case, i_L and v_{ds} can be found by solving the characteristic equation given in (4.3) and using initial conditions.

$$LC_{ds}\frac{d^2v_{ds}(t)}{dt^2} + v_{ds}(t) = v_{in} \tag{4.3}$$

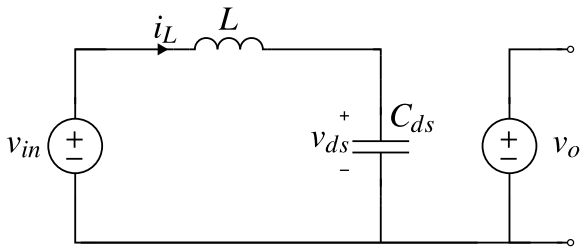


Figure 4.3. Equivalent circuit when MOSFET is off and the drain-source capacitor conducts in Mode 2.

The third scenario is Mode 3, depicted in Figure 4.4, when the boost diode is forward biased and the boost switch is off. In this case the i_L and v_{ds} can be found by (4.4) and (4.5) respectively.

$$i_L(t) = \frac{(v_{in} - v_o)}{L}t + i_L(0) \tag{4.4}$$

$$v_{ds}(t) = 0 \tag{4.5}$$

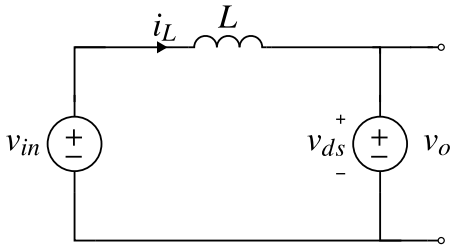


Figure 4.4. Equivalent circuit when MOSFET is off and the boost diode conducts in Mode 3.

Now that the equivalent circuits of the boost converter in its different operating modes are understood, an analysis of the waveforms of the inductor current and the drain-source voltage over a single switching cycle can be performed. There are three different cases that alter the shape of i_L and v_{ds} depending on the input voltage level.

4.2.1 Case I: $v_{in} > \frac{1}{2}v_o$ and $v_{in} \geq \frac{v_o}{1+\sqrt{1+\omega_r^2 t_{on}^2}}$

The wave shape of i_L and v_{ds} over a single switching cycle of the boost converter are shown in Figure 4.5. Initially the boost converter is in Mode 1, and the boost inductor charges linearly until the converters on-time has elapsed. The on-time varies with input voltage and output power and can be estimated using (2.10).

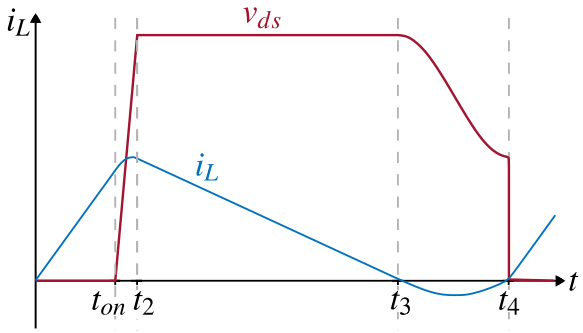


Figure 4.5. Case I: Inductor current and drain-source voltage over a single switching cycle when $v_{in} > \frac{1}{2}v_o$ and $v_{in} \geq \frac{v_o}{1+\sqrt{1+\omega_r^2 t_{on}^2}}$.

During this period i_L and v_{ds} can easily be calculated by (4.6).

$$i_L(t) = \frac{v_{in}}{L}t$$

and

$$v_{ds}(t) = 0 \tag{4.6}$$

After the full on-time t_{on} has elapsed, the switch turns off. The circuit then operates in Mode 2, as the boost inductor and MOSFET drain-source capacitor resonate with each other. This continues until v_{ds} rises to v_o, and the boost diode becomes forward biased at $t = t_2$. During the interval $t_{on} \leq t < t_2$, the waveforms of i_L and v_{ds} can be calculated by solving the characteristic equation defined by (4.3) and using the conditions $v_{ds}(0) = 0$ and $i_L(0) = \frac{v_{in}}{L}t_{on}$. This results in the following equations obtained in (4.7). A full derivation for (4.7) is given in Appendix C.

$$i_L(t) = \omega_r v_{in} C_{ds}\sqrt{1+\omega_r^2 t_{on}^2}\cos(\omega_r(t-t_{on})+\theta)$$

and

$$v_{ds}(t) = v_{in} + v_{in}\sqrt{1+\omega_r^2 t_{on}^2}\sin(\omega_r(t-t_{on})+\theta) \tag{4.7}$$

where ω_r is the resonant frequency of the boost inductance and MOSFET drain-source capacitance given by $\omega_r = \frac{1}{\sqrt{LC_{ds}}}$, and the term θ is given by

$$\theta = \tan^{-1}\left(\frac{-1}{\omega_r t_{on}}\right) \tag{4.8}$$

The time t_2 occurs when the drain-source voltage has increased to the point that it equals the output voltage. Hence an expression for this time can be found by setting $t = t_2$ and $v_{ds}(t_2) = 0$ in (4.7). This results in the following expression:

$$t_2 = t_{on} + \frac{1}{\omega_r}\sin^{-1}\left(\frac{v_o - v_{in}}{v_{in}\sqrt{1+\omega_r^2 t_{on}^2}}\right) - \frac{\theta}{\omega_r} \tag{4.9}$$

After v_{ds} has charged to v_o the output capacitor is clamped at v_o. Meanwhile the energy stored in the boost inductance linearly discharges into the output capacitor. This continues in the interval $t_2 \leq t < t_3$ until i_L reaches zero and the boost diode is reversed biased once more.

During this time interval i_L and v_{ds} are calculated by

$$i_L(t) = \frac{v_{in} - v_o}{L}(t - t_2) + i_L(t_2)$$

and

$$v_{ds}(t) = v_o \tag{4.10}$$

The term $i_L(t_2)$ can be calculated by substituting the value of t_2 obtained in (4.9) into (4.7) and solving. Hence,

$$\begin{aligned} i_L(t_2) &= \omega_r v_{in} C_{ds} \sqrt{1 + \omega_r^2 t_{on}^2} \cos(\omega_r (t_2 - t_{on}) + \theta) \\ &= \omega_r v_{in} C_{ds} \sqrt{1 + \omega_r^2 t_{on}^2} \cos\left(\sin^{-1}\left(\frac{v_o - v_{in}}{v_{in}\sqrt{1 + \omega_r^2 t_{on}^2}} \right) \right) \\ &= \omega_r v_{in} C_{ds} \sqrt{1 + \omega_r^2 t_{on}^2} \sqrt{1 - \left(\frac{v_o - v_{in}}{v_{in}\sqrt{1 + \omega_r^2 t_{on}^2}} \right)^2} \\ &= \omega_r C_{ds} \sqrt{v_{in}^2 \omega_r^2 t_{on}^2 - v_o^2 + 2 v_o v_{in}} \end{aligned} \tag{4.11}$$

The time t_3 can be determined by setting $t = t_3$, and solving (4.10).

$$t_3 = t_2 + \frac{L}{v_o - v_{in}} i_L(t_2) \tag{4.12}$$

At the instant the boost diode becomes reversed biased $v_{ds} = v_o$ and the switch remains off. Therefore the voltage v_{ds} begins to fall as the energy stored in C_{ds} discharges through the boost inductor into C_{in}. During this interval the circuit operates in Mode 2 again. The boost inductor and capacitance C_{ds} continue to resonate until i_L becomes zero and the voltage v_{ds} has reached a valley point. During this interval $t_3 \leq t < t_4$ the waveforms of i_L and v_{ds} are described by (4.13). A full derivation for (4.13) is given in Appendix C.

$$i_L(t) = -C_{ds} \omega_r (v_o - v_{in}) \sin(\omega_r (t - t_3))$$

and

$$v_{ds}(t) = v_{in} + (v_o - v_{in}) \cos(\omega_r (t - t_3)) \tag{4.13}$$

The time t_4 occurs when the voltage v_{ds} is at it's minimum value. This occurs at a half resonant period after t_3, hence

$$t_4 = t_3 + \frac{\pi}{\omega_r} \tag{4.14}$$

Once $t = t_4$ a zero-current detection (ZCD) circuit triggers the MOSFET turn-on, and the next switching period begins.

4.2.2 Case II: $\frac{v_o}{1+\sqrt{1+\omega_r^2 t_{on}^2}} \leq v_{in} < \frac{1}{2}v_o$

When v_{in} is less than $\frac{1}{2}v_o$ but still greater than $\frac{v_o}{1+\sqrt{1+\omega_r^2 t_{on}^2}}$, the waveforms of i_L and v_{ds} over a single switching cycle are as shown in Fig. 4.6. For the time interval $0 \leq t < t_3$ case I

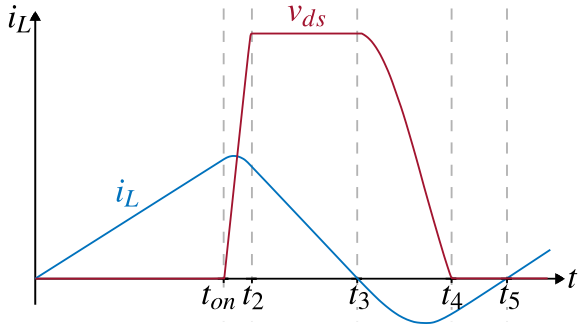


Figure 4.6. Case II: Inductor current and drain-source voltage over a single switching cycle when $\frac{v_o}{1+\sqrt{1+\omega_r^2 t_{on}^2}} \leq v_{in} < \frac{1}{2}v_o$.

and case II have the exact same behaviour. For the time interval from $t_3 \leq t < t_4$, case II behaves similarly to case I. During this interval the energy stored in C_{ds} resonates back into C_{in} through the boost inductor, but the difference is the voltage v_{ds} now fully discharges to zero instead of reaching a valley point. For this reason, i_L and v_{ds} are still described by (4.13). However, the time t_4 now occurs when $v_{ds} = 0$ instead of at the valley point. Therefore, in this case, a value for t_4 can be obtained by setting $v_{ds} = 0$ and $t = t_4$ in (4.13).

$$t_4 = t_3 + \frac{1}{\omega_r}\cos^{-1}\left(\frac{v_{in}}{v_{in} - v_o}\right) \tag{4.15}$$

After $t = t_4$, the voltage v_{ds} remains at zero. The inductor current must remain continuous. Therefore, the body diode of the boost switch is forced to conduct and the circuit operates in Mode 1. During this region i_L and v_{ds} are given by,

$$i_L(t) = \frac{v_{in}}{L}(t - t_4) - i_L(t_4)$$

and

$$v_{ds}(t) = 0 \tag{4.16}$$

An expression can be obtained for $i_L(t_4)$ by substituting the value obtained for t_4 in (4.15) into the expression obtained for i_L in (4.13). Thus

$$\begin{aligned} i_L(t_4) &= -C_{ds}\omega_r(v_o - v_{in})\sin(\omega_r(t_4 - t_3)) \\ &= -C_{ds}\omega_r(v_o - v_{in})\sin\left(\cos^{-1}\left(\frac{v_{in}}{v_{in} - v_o}\right)\right) \\ &= -C_{ds}\omega_r(v_o - v_{in})\sqrt{1 - \left(\frac{v_{in}}{v_{in} - v_o}\right)^2} \\ &= C_{ds}\omega_r\sqrt{v_o^2 - 2v_{in}v_o} \end{aligned} \tag{4.17}$$

Substituting this value for $i_L(t_4)$ into (4.16) and solving for when $i_L = 0$, the following expression can be found to describe the time instant t_5.

$$t_5 = t_4 + \frac{1}{\omega_r}\frac{1}{v_{in}}\sqrt{v_o^2 - 2v_{in}v_o} \tag{4.18}$$

After $t = t_5$ the switching cycle is complete and the ZCD circuit the triggers MOSFET turn-on to begin the next switching instant.

4.2.3 Case III: $v_{in} < \frac{v_o}{1+\sqrt{1+\omega_r^2 t_{on}^2}}$

The third case is when the input voltage is so low that the boost inductor does not have enough energy to sufficiently charge the capacitance C_{ds} to reach v_o. Therefore the boost diode never becomes forward biased, and no energy is transferred to the output capacitor. Figure 4.7 shows the shape of i_L and v_{ds} for case III.

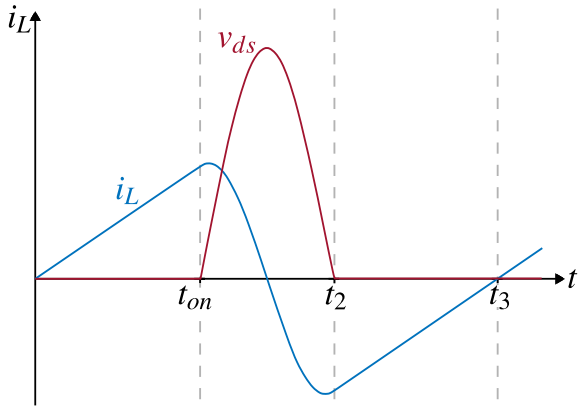


Figure 4.7. Case III: Inductor current and drain-source voltage over a single switching cycle when $v_{in} < \frac{v_o}{1+\sqrt{1+\omega_r^2 t_{on}^2}}$.

For this case, the time period $0 \leq t < t_{on}$ is identical to case I and case II, and the inductor current is charged linearly by the input voltage. For the time period of $t_{on} \leq t < t_2$ the inductor current and drain-source current are calculated using (4.7). The maximum value of the drain-source voltage can be calculated by setting the sine term in (4.7) equal to unity, hence the maximum drain-source voltage is

$$\max\langle v_{ds}(t)\rangle = v_{in} + v_{in}\sqrt{1+\omega_r^2 t_{on}^2} \tag{4.19}$$

Case III occurs when this maximum value is less than v_o, so that the boost diode can never become forward biased. Therefore, the condition for case III to occur is defined by

$$v_{in} + v_{in}\sqrt{1+\omega_r^2 t_{on}^2} < v_o$$

and

$$v_{in} < \frac{v_o}{1+\sqrt{1+\omega_r^2 t_{on}^2}} \tag{4.20}$$

As a result, if the inequality defined by (4.20) is satisfied and the drain-source voltage remains below v_o, it reaches a peak value when all the stored energy is transferred from the boost inductor to the drain-source capacitor, and then falls to zero when $t = t_2$ as this energy is returned to the input capacitor. The time t_2 is now determined by when the voltage v_{ds} equals zero. Therefore the time t_2 is calculated by setting $t = t_2$ and $v_{ds} = 0$ in (4.7).

$$t_2 = t_{on} + \frac{\pi}{\omega_r} - \frac{2\theta}{\omega_r} \tag{4.21}$$

After $t = t_2$ the boost inductor current stays continuous and forces the switch body diode to conduct. In this region, where $t_2 \leq t < t_3$, the converter operates in Mode 1, and the boost inductor is charged linearly by the input voltage. Thus i_L and v_{ds} can be described by

$$\begin{aligned} i_L(t) &= \frac{v_{in}}{L}(t - t_2) - \frac{v_{in} t_{on}}{L} \\ v_{ds}(t) &= 0 \end{aligned} \tag{4.22}$$

The boost inductor continues to charge until the inductor current reaches zero, at which point the ZCD circuit re-triggers the MOSFET turn-on at $t = t_3$. The time t_3 can be found by

$$t_3 = t_2 + t_{on} \tag{4.23}$$

It is important to note for case III, that the average inductor current that flows over a whole switching cycle is zero. Hence, case III only exists at a very low input voltage, which happens around the zero-crossing of the line voltage. As a result, a region exists around the zero crossing of the line voltage where the average inductor current is zero.

In the next section the presented valley-switching analysis is expanded over a half-line cycle of the line voltage to explain the zero-crossing distortion.

4.3 Line-Current Distortion

The line current drawn by BCM boost converters suffers from significant zero-crossing distortion. The line-current distortion has two primary causes. The first being the effects of the valley-switching, and the second being the effects of the input capacitor C_{in}.

4.3.1 Valley-Switching Distortion

The analysis carried out in Section 4.2 can be used to find the effect of the valley switching on the shape of the input current drawn by a single channel of the converter over a half-line cycle. This is achieved by using a computer algorithm to calculate the shape of i_L over a single switching cycle using the equations developed in Section 4.2, and then repeating the algorithm over an entire half-line cycle.

Over a half-line cycle the line voltage v_{line} can be calculated as $\sqrt{2}V_{in(rms)}\sin(\omega_L t)$. The rectified input voltage v_{in} can be calculated as the absolute value of the line voltage for case I and case II. This assumes negligible diode-forward-voltage drop across the bridge-rectifier diodes. For case III, since the average inductor current is zero, and the average current drawn by the input capacitor must also be zero, it can be concluded that the average rectified input current drawn by the converter is zero. Thus, during case III all bridge-rectifier diodes are reversed biased, and as a result the input voltage holds a constant value of $\frac{v_o}{1+\sqrt{1+\omega_r^2 t_{on}^2}}$. This of course assumes no resistive losses, diode-forward-voltage-drop losses, switching losses or boost-inductor core losses occur during case III. This assumption is valid since these losses are small. Hence, over a half-line cycle the rectified input voltage can be approximated as

$$v_{in} = |v_{line}| \qquad \text{for} \qquad |v_{line}| > \frac{v_o}{1+\sqrt{1+\omega_r^2 t_{on}^2}}$$

and

$$v_{in} = \frac{v_o}{1+\sqrt{1+\omega_r^2 t_{on}^2}} \qquad \text{for} \qquad |v_{line}| \leq \frac{v_o}{1+\sqrt{1+\omega_r^2 t_{on}^2}} \tag{4.24}$$

The average input current can be calculated over each switching cycle to see the effect of the valley-switching distortion. This is done in Figure 4.8 for the case of P_o = 300 W for a single channel of the converter, at 230 Vrms. The plots show both the inductor current shape and time-averaged input current shape. The input current has significant regions about the zero crossing of the line voltage near 0 ms and 10 ms, where $i_{in} = 0$. This distortion reduces the converter's power factor.

Figure 4.9 shows a similar plot to Fig. 4.8, except at a lower power level of P_o = 50 W. At this lower power level, the zero-crossing distortion worsens. As a result, the power factor is further reduced.

The analysis in Section 4.2, assumes that the MOSFET capacitance C_{ds} is linear. In reality it is a non-linear function of the voltage v_{ds}. Additionally, the diode capacitance is assumed negligible as it is much smaller than C_{ds}. The analysis in Section 4.2 also does

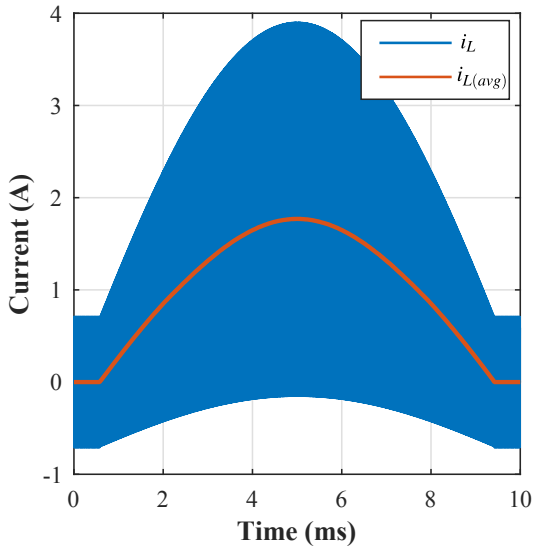


Figure 4.8. Theoretically predicted inductor current i_L and time-average input current i_{in} of a single channel of the interleaved BCM boost converter, at P_o = 300 W and 230 Vrms.

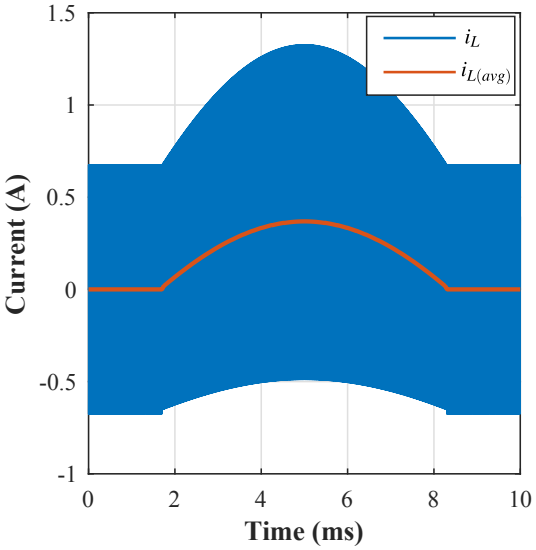


Figure 4.9. Theoretically predicted inductor current i_L and time-average input current i_{in} at P_o = 50 W at 230 Vrms.

not take into account the exact timings of the ZCD circuit, PWM circuit and gate driver circuit. As a result the waveforms given in Figure 4.8 and Figure 4.9 do not give an accurate description of the inductor current, but do allow for an intuitive understanding of how the valley switching causes the distortion in the line current and how the distortion worsens with lower output power.

The typical waveshape of the line voltage and line current are shown below in Figure 4.10. A region exists around the zero-crossing of the line voltage where the line current is zero.

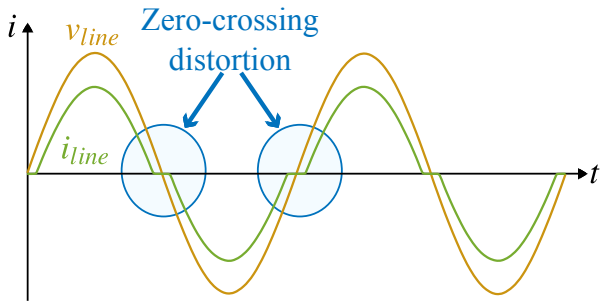


Figure 4.10. Typical waveform of the line voltage v_{line} and line current i_{line} for a BCM boost converter with significant zero-crossing distortion.

4.3.2 Input-Capacitor Distortion

The input current drawn by the converter is also distorted by the input capacitor C_{in}, which gives the input current a phase-leading characteristic. The voltage across C_{in} is v_{in}, and can be approximated as the absolute value of the line voltage $v_{in} = V_{in(pk)}|\sin(\omega_L t)|$. The current that flows through C_{in} can then be described by:

$$\begin{aligned} & i_{Cin} = C_{in}\frac{d}{dt}V_{in(pk)}|\sin(\omega_L t)| \\ & i_{Cin} = \omega_L C_{in} V_{in(pk)}\cos(\omega_L t) \qquad \text{for} \qquad 0 < \omega_L t \leq \pi \\ \text{and} \qquad & i_{Cin} = -\omega_L C_{in} V_{in(pk)}\cos(\omega_L t) \qquad \text{for} \qquad \pi < \omega_L t \leq 2\pi \end{aligned} \tag{4.25}$$

Figure 4.11 shows the shapes of v_{in} and i_{Cin} over two line cycles.

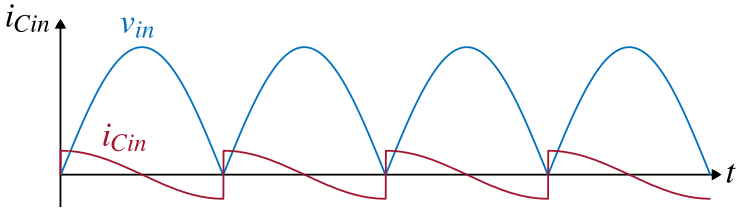


Figure 4.11. Waveshape of the rectified input voltage v_{in} and input capacitor current i_{Cin}

The total input current drawn by the converter is a sum of the current pulled by each boost-converter channel and the current drawn by the input capacitor. As a result, the input capacitor distorts the input current, giving it a phase-leading characteristic. This phase-leading characteristic is shown in Figure 4.12, and demonstrates the typical waveshape of i_{line} when both the effects of the valley-switching distortion and input-capacitor distortion are taken into account. As the magnitude of i_{Cin} is proportional to $V_{in(pk)}$ the distortion associated with the input capacitor varies as a function of the input voltage. A similar effect occurs as the line frequency increases, thus increasing ω_L and the current in the input capacitor.

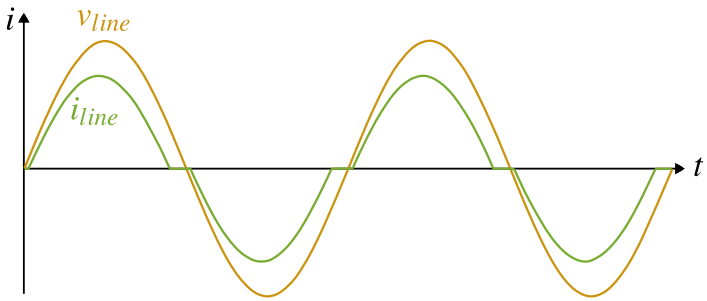


Figure 4.12. The waveshape of v_{line} and i_{line} when the input-capacitor distortion and the valley-switching distortion are taken into account.

4.4 Simple Feedforward Algorithm

It is possible to derive the additional on-time t_{add}, which must be added to the on-time calculated by the voltage compensator to cancel the effects of the valley switching. The additional on-time can be derived from the analysis carried out in in Section 4.2. This is achieved by assuming the additional on-time needed to remove the valley-switching distortion is equal to the time interval when the inductor current is negative, given by $(t_4 - t_3)$ when $v_{in} > \frac{1}{2}v_o$, and $(t_5 - t_3)$ when $v_{in} \leq \frac{1}{2}v_o$. Therefore, the additional on-time can be obtained from (4.14), (4.15) and (4.18) as follows,

$$t_{add} = t_4 - t_3 = \frac{\pi}{\omega_r} \qquad \forall \quad v_{in} > \frac{1}{2}V_{ref}$$

$$t_{add} = t_5 - t_3 = \frac{1}{\omega_r}\cos^{-1}\left(\frac{v_{in}}{v_{in} - V_{ref}}\right) + \ldots \\ \frac{1}{\omega_r}\frac{1}{v_{in}}\sqrt{V_{ref}^2 - 2v_{in}V_{ref}} \qquad \forall \quad v_{in} \leq \frac{1}{2}V_{ref} \tag{4.26}$$

The term v_o describes the output voltage which varies with time. The voltage v_o is replaced by the term V_{ref} in (4.26) to simplify the equations. The term V_o is the reference voltage for the voltage compensator and is a constant 400 V. As a result, the feedforward algorithm defined by (4.26) only has a single variable v_{in}. This allows for a very simple implementation in a digital system as the curve of t_{add} versus v_{in} can be calculated once, as is done in Figure 4.13, over the entire range of v_{in} from 0 to 375 V. A single look-up table can then be used to calculate t_{add} in the microcontroller software. As the MOSFET has a non-linear drain-source capacitance that varies with the drain-source voltage, the term ω_r is calculated assuming a constant capacitance given by the time-effective output capacitance from the device datasheet.

Figure 4.14 depicts how the feedforward algorithm was implemented as part of the digital control scheme for the 3-channel BCM boost converter. A voltage compensator with a bandwidth of 20 Hz was designed to regulate the output voltage to a constant 400 V. The on-time equals the voltage compensator output v_c plus the additional on-time calculated by the feedforward algorithm per (4.26), so that $t_{on} = v_c + t_{add}$. The feedforward algorithm was executed at a rate of 35 kHz.

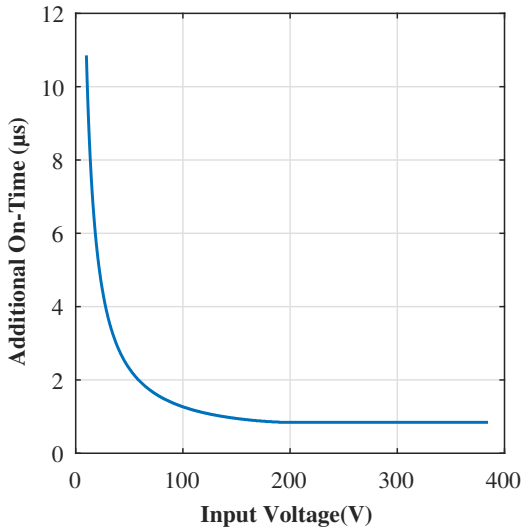


Figure 4.13. Additional on-time added by the feedforward algorithm versus input voltage.

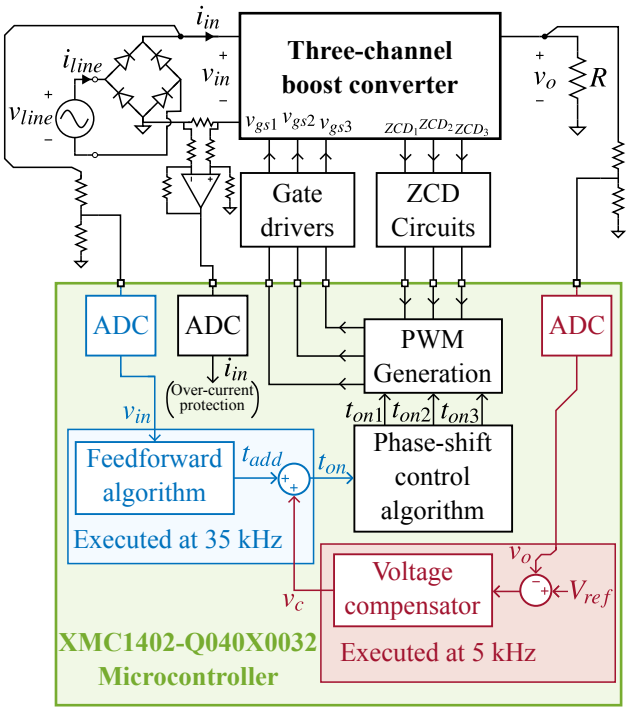
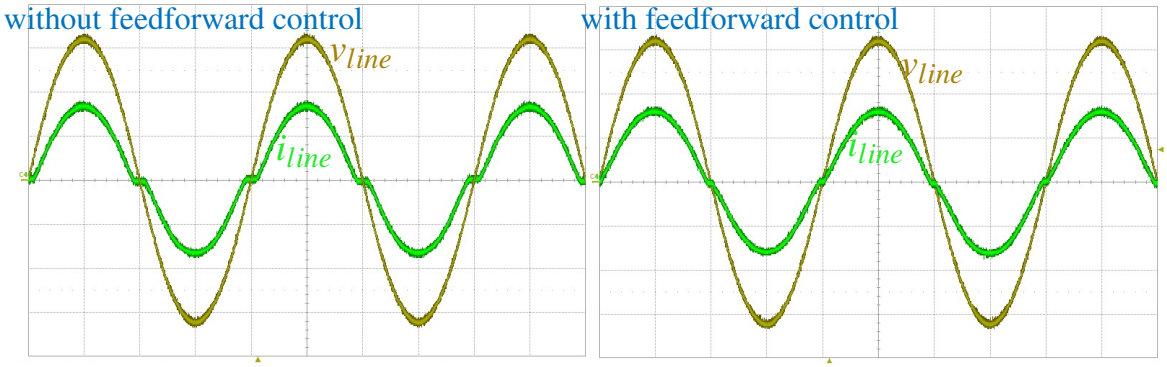


Figure 4.14. Three-channel boost converter control circuit.

4.5 Experimental Results

The 1 kW 3-channel BCM boost converter prototype was used to verify the performance of the proposed feedforward algorithm.

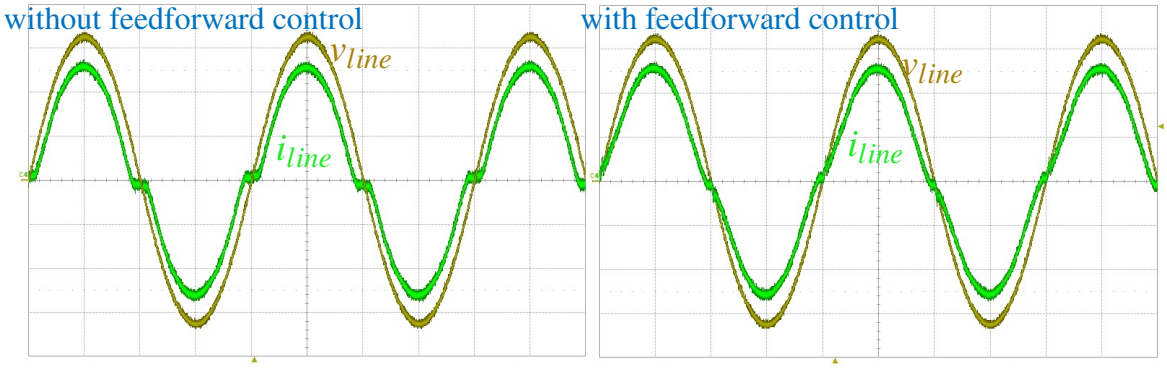
The converter was run with and without the feedforward control algorithm enabled under different conditions in order to verify the effectiveness of the feedforward control algorithm. Figure 4.15 shows a comparison of the shape of the line voltage and line current i_{line} at 700 W output power and 115 Vrms, with and without the feedforward control algorithm implemented. It is clear that when the feedforward algorithm is used, the zero-crossing distortion of the line current is significantly reduced.



(a) (b)

Figure 4.15. v_{line} and i_{line} at P_o = 700 W and a 115 Vrms line voltage (a) without feedforward control and, (b) with feedforward control (v_{line}: 50 V/div, 1_{line}: 5 A/div, timebase: 5 ms/div).

Figure 4.16 shows a comparison of the line voltage and line current waveshape with and without the feedforward control enabled at 230 Vrms. It is clear from comparing the waveshapes of the line current that there is again a significant reduction in the line current zero-crossing distortion when the feedforward control algorithm is implemented.



(a) (b)

Figure 4.16. v_{line} and i_{line} at P_o = 900 W and 230 Vrms (a) without feedforward control and, (b) with feedforward control (v_{line}: 100 V/div, 1_{line}: 2 A/div, timebase: 5 ms/div).

The feedforward control algorithm reduces the line current zero-crossing distortion by

drastically increasing the on-time around this point. This increases the average input current drawn by the converter at the line current zero-crossing points. If the feedforward algorithm is disabled, then the on-time calculated by the voltage compensator is near constant in steady-state operation. When the feedforward control algorithm is enabled, there are large variations in on-time as the line voltage changes. This variation in on-time is demonstrated in Figure 4.17 and Figure 4.18 with and without the feedforward control algorithm enabled at 115 Vrms and 230 Vrms, respectively.

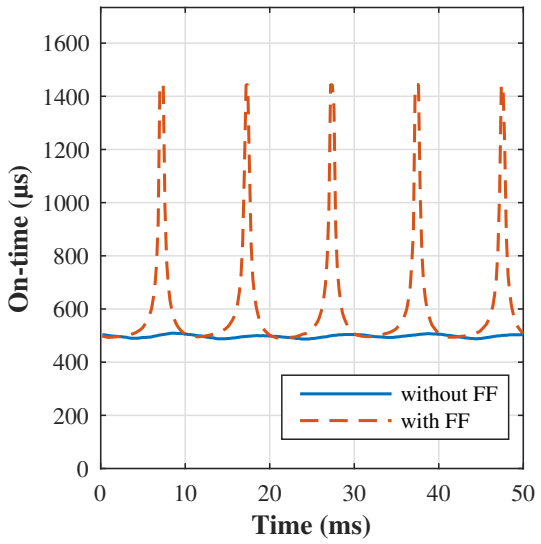


Figure 4.17. Measured on-time variation at P_o = 700 W and 115 Vrms without feedforward (FF) control (continous line) and with the feedforward (dashed line) control.

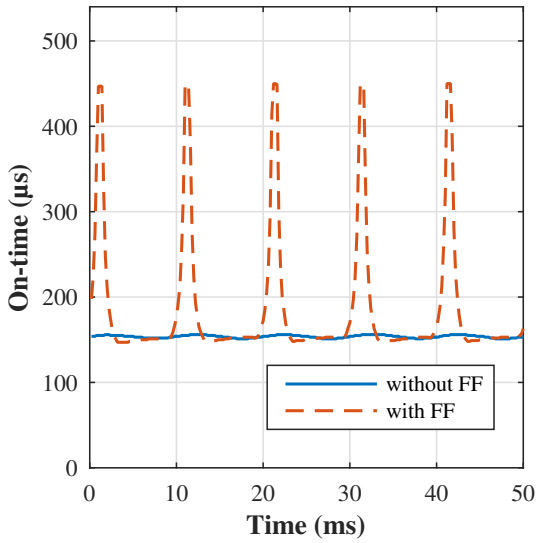


Figure 4.18. Measured on-time variation at P_o = 1 kW and 230 Vrms without feedcforward (FF) control (continous line) and with the feedforward (dashed line) control.

The power factor of the converter was measured against output power with, and without, the feedforward control algorithm enabled. This is done in Figure 4.19 at 115 Vrms, and

demonstrates a significant improvement in power factor under all load conditions when the feedforward control is enabled. Similarly, Figure 4.20 shows the power factor comparison at 230 Vrms, again with a significant improvement in the converter's power factor under all load conditions.

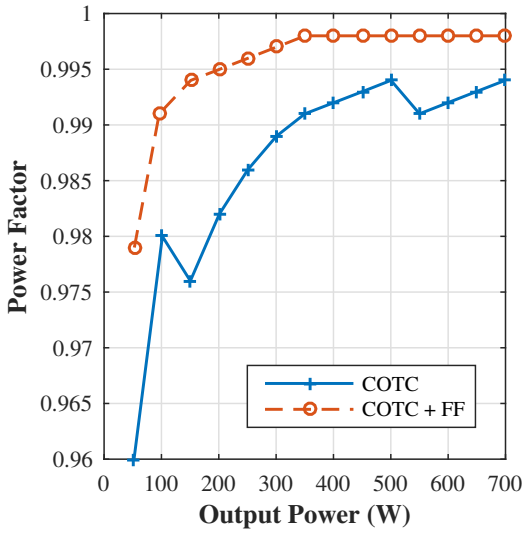


Figure 4.19. Power factor comparison without feedforward (FF) control (continuous line) and with feedforward control (dashed line) at 115 V line voltage against output power.

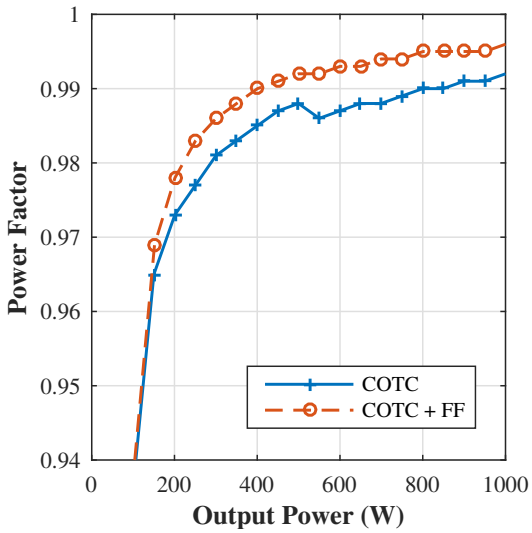
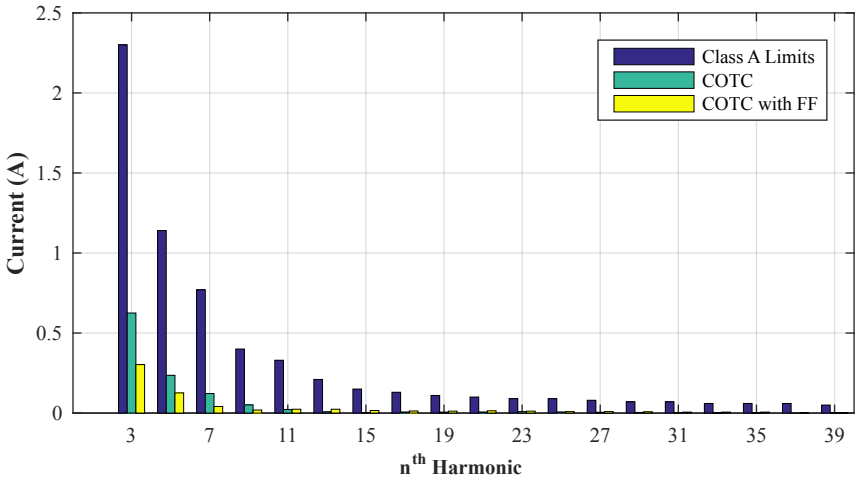


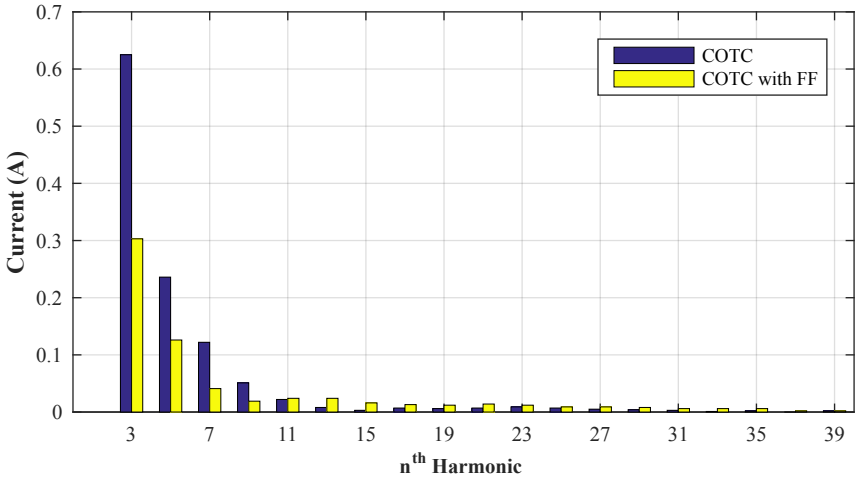
Figure 4.20. Power factor comparison without feedforward (FF) control (continuous line) and with feedforward control (dashed line) at 230 V line voltage against output power.

A comparison of the input current harmonics of the converter at rated power and rms line voltage of 230 V, with and without the feedforward control enabled is given in Figure 4.21, demonstrating a substantial reduction in low-order harmonic components. In Figure 4.21(a) the measurements are compared to the EN61000-3-2 Class A limits, showing both sets of measurements are well below the Class A limits. In Figure 4.21(b) both sets of

measurements are compared to each other without the limits, demonstrating the feedforward algorithm successfully reduces the current magnitudes at the first 4 odd harmonics.



(a)



(b)

Figure 4.21. The input current harmonics measured at 230 Vrms and an output power of 1 kW, with and without the feedforward algorithm enabled. In subfigure (a) the measured harmonics are compared to the Class A limits and in subfigure (b) there are no Class A limits.

4.6 Conclusion

This chapter presented the use of digital variable-on-time control to improve the power quality of a multi-channel BCM boost converter. A detailed analysis of the valley switching behaviour of the converter was carried out. It was demonstrated that the valley switching causes the inductor current to have an average value of zero near the line voltage zero-crossing points, which in turn creates a distortion in the line current. The effect of the boost-converter input capacitor was also explored, demonstrating the capacitor creates a phase-leading characteristic in the input line current which further reduces power factor.

A novel, low-cost and easy-to-implement feedforward control algorithm was proposed to calculate the additional on-time needed to reduce the valley-switching related distortion. The algorithm was derived from the valley-switching analysis carried out in earlier sections. The algorithm calculates the additional on-time as a function of input voltage, and requires no experimental tuning, thus making the algorithm very simple to implement. Moreover, as the additional on-time is calculated based solely on the value of the sensed input voltage, only a single LUT is required for implementation, thus simplifying the firmware requirements.

Experimental results were demonstrated on a 3-channel BCM boost PFC prototype. Experimental waveforms demonstrate that the algorithm dramatically reduces the line current's zero-crossing distortion under all operating conditions. Similarly, power factor measurements were presented for different line voltages over the converter's rated power range, demonstrating the feedforward algorithm provides significant improvement in power factor.

5 AVERAGE-CURRENT-MODE CONTROL

This chapter proposes a novel digital control scheme that uses average-current-mode control (ACMC) to significantly improve the power quality of a boundary-conduction-mode (BCM) boost converter. BCM boost converters used in power-factor-correction (PFC) applications are normally regulated using constant-on-time control (COTC). The downside to using COTC is that the line current drawn by the converter suffers from a zero-crossing distortion, caused by the valley-switching operation of the converter and the converter's input capacitor. Feedforward control can be used to reduce the line-current distortion associated with the valley-switching behaviour of the converter, but is ineffective at removing the distortion associated with the input capacitor. ACMC control, on the other hand, allows for a significant reduction in the valley-switching distortion and input-capacitor distortion of the line current, but at the cost of a more expensive and complex controller implementation.

Results of this chapter have been submitted for publication to the following journal,

- R. T. Ryan, D. N. Hogan, R. J. Morrison and J. G. Hayes, "Digital average-current-mode control for a BCM boost PFC rectifier", *IEEE Transactions on Industrial Electronics*, under review, 2019.

5.1 Introduction

5.1.1 Constant-On-Time Control

The output voltage of the BCM boost topology is usually regulated using COTC as described by Chapter 2. A simplified block diagram demonstrating how a COTC scheme regulates the output voltage of a multi-channel interleaved boost converter is given in Figure 5.1. The output of the voltage compensator v_c is equal to the on-time t_{on} of the boost-converter MOSFETs. The phase-shift control and PWM generation are responsible for creating the gate-source voltages v_{gs1}, v_{gs2} to v_{gsN} for the MOSFET of each boost-converter channel.

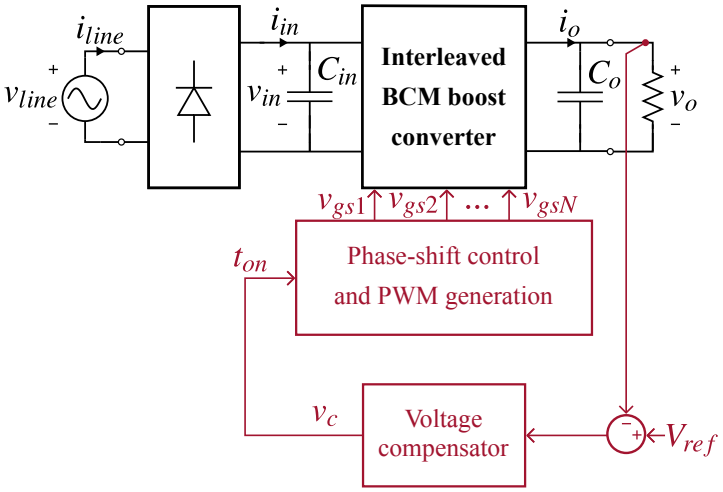


Figure 5.1. Constant-on-time control scheme.

COTC is advantageous as it only requires a single voltage compensator with a low bandwidth to regulate the output voltage, allowing for a low-cost solution. However, the downside to using COTC is that the line current drawn by the converter suffers significant line-current distortion.

5.1.2 Variable-On-Time Feedforward Control

The most popular method to reduce the line-current distortion is to use feedforward control. Feedforward control works by calculating an additional on-time t_{add} which is added to the voltage compensator output and cancels the effects of converter's soft-switching behaviour. A block diagram of the feedforward control method is shown in Figure 5.2. This method was discussed in Chapter 3.

The variable-on-time feedforward method works very well at reducing the line-current distortion of BCM boost converters. However, this solution is fundamentally limited by the fact that it is not a closed-loop solution. Therefore, it requires accurate FF algorithms to adjust the on-time by the correct amount to remove the zero-crossing distortion. Moreover feedforward control only acts to reduce the valley-switching related distortion, and not the input-capacitor related distortion.

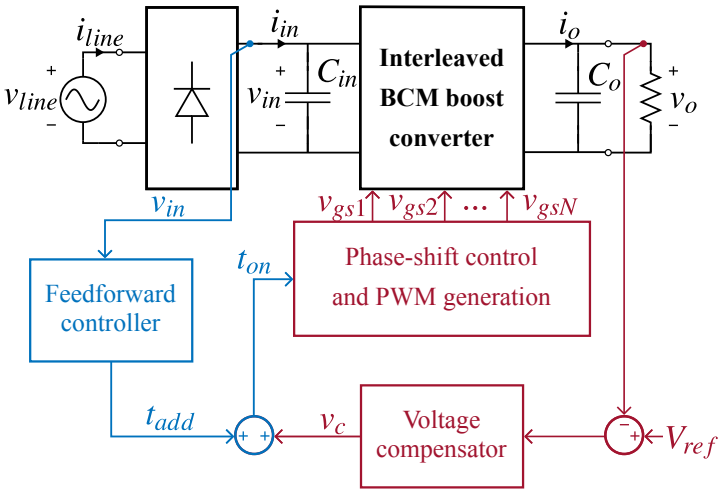


Figure 5.2. COTC scheme with FF control.

5.1.3 Average-Current-Mode Control

ACMC is a technique that has been widely adopted for the control of CCM boost converters used in PFC applications [44], [111], [112]. Figure 5.3 shows a simplified block diagram of how an ACMC control scheme can be used to regulate an interleaved BCM boost converter. Using ACMC to regulate the input current of a CCM boost converter is very different to using ACMC for a BCM boost converter. The main difference being as follows: in a CCM boost converter the current compensator is designed based on the open-loop model of how changes in duty cycle affect the inductor current, whereas in the BCM boost converter, the current compensator is designed from the open-loop model of how changes in the on-time affect the inductor current. Additionally, the BCM and CCM boost converters have very different small-signal models describing the inductor current's transient behaviour. As a result, both have very different open-loop transfer functions, and require different design methods for the current compensator.

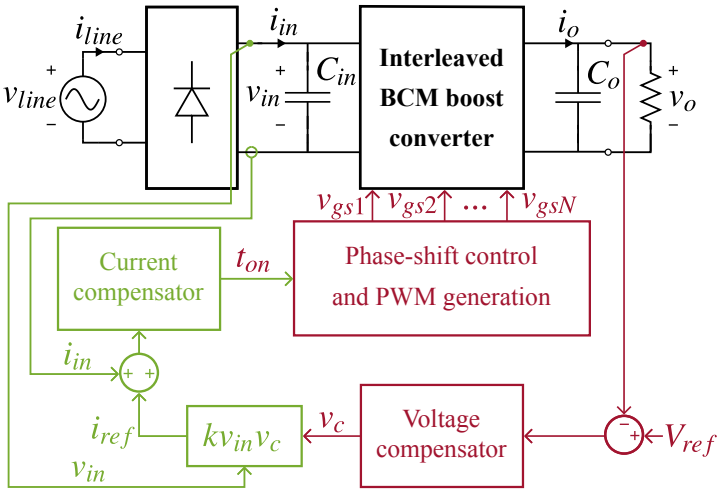


Figure 5.3. Average-current-mode control scheme.

An analog ACMC scheme is proposed for a BCM boost in [36] and [77] to reduce the

line-current zero-crossing distortion. The control scheme uses a sample-and-hold method to generate the current reference by sampling the inductor current at the midpoint of the on-time. The sample-and-hold scheme works well to reduce the system cost of an analog solution as it removes the need for a multiplier. However, the sample-and-hold method senses the input current drawn by the boost converter only, and not that of the input capacitor. Therefore, although the method can reduce the line-current distortion attributed to the valley-switching operation, it cannot remove the input-capacitor distortion.

5.1.4 Research Contribution in this Work

The work presented in this chapter describes a novel closed-loop digital ACMC scheme that can reduce both the valley-switching line-current distortion and the input-capacitor line-current distortion. Some of the key functions of the ACMC scheme described in this work are as follows. Instead of sensing the current drawn by the interleaved boost converter, the total input current drawn by the combination of the interleaved boost converters and the input capacitor is sensed, which allows for the ACMC control to also reduce the input-capacitor distortion. The gain of the current compensator changes with the converter's sensed input voltage in order to maintain the desired current-loop bandwidth. Overall this scheme leads toa significant improvement in power quality but also leads to a more expensive implementation than a simple COTC scheme as it requires a more powerful microcontroller.

This chapter is divided as follows: Section 5.2 discusses the design of the voltage compensator. Section 5.3 discusses the design of the current compensator. The firmware design for the ACMC scheme is discussed in Section 5.4. Experimental results are presented in Section 5.5, with comparison of COTC, COTC with FF control and ACMC.

5.2 Voltage Compensator Design

The same voltage compensator design must be used for both COTC and ACMC to allow for a fair comparison. The full voltage-compensator design process is the same as that outlined in Chapter 2, except that in this work the voltage compensator is implemented using floating-point variables. The 2-channel 600 W prototype with the more powerful TMS320f28069 microcontroller is used instead of the 3-channel 1 kW prototype.

The ACMC and COTC schemes can use the same voltage compensator design, provided that the open-loop voltage-loop transfer function is identical for both schemes. For COTC, this transfer function is derived from (2.5) in Chapter 2. This equation can be re-written in terms of the voltage compensator output by replacing t_{on} with the term v_c. Hence

$$i_{in(avg)} = \frac{N}{2}\frac{t_{on}v_{in}}{L} = \frac{N}{2}\frac{v_c v_{in}}{L} \tag{5.1}$$

For COTC, the voltage compensator output and on-time are equal, so that $v_c = t_{on}$. For ACMC, the voltage compensator output and on-time are not equal; instead the on-time is calculated by the current compensator, as shown by Figure 5.3.

For ACMC, the average input current drawn by the converter can be calculated assuming that the current compensator has perfect tracking. Therefore, the input current is given by

$$i_{in(avg)} = i_{ref} = kv_{in}v_c \tag{5.2}$$

where k is a constant scaling term. The design of the voltage compensator for both COTC and ACMC is exactly the same provided that the constant term k is set so that both schemes have the same mathematical relationship between $i_{in(avg)}$ and v_c. Thus, by setting (5.1)and (5.2) equal to each other, k can be calculated as

$$k = \frac{N}{2}\frac{1}{L} \tag{5.3}$$

This approach enables a fair comparison between ACMC and COTC, as both systems have identical output-voltage dynamics.

A summary of the power-stage parameters for the 2-channel 600 W prototype converter is given below in Table 5.1. Both prototype converters operate over a universal line voltage range and have the same boost inductance. However the 2-channel prototype has a lower rated power, and smaller output capacitance.

Using the same voltage compensator design methodoutlined in Chapter 2, the voltage compensator used in the experimental work described in this chapter was designed for a 15 Hz bandwidth and an injected phase margin of 45°. The voltage compensator was executed at a rate of 10 kHz. A PWM clock frequency of 90 MHz was used as this is the highest allowable clock frequency for the TMS320f28069 microcontroller. The ADC reading of the

TABLE 5.1
LIST OF POWER STAGE PARAMETERS FOR THE 2-CHANNEL PROTOTYPE

Parameter	Value
Number of channels, N	2
Boost inductance, L	130 µH
Output capacitance, C	360 µF
Output voltage, V_o	400 V
RMS line voltage, $V_{line(rms)}$	85 V to 265 V
Output Power P_o	0 W to 600 W

output voltage was scaled by the inverse of the ADC and sense circuit gain, this results in an ADC-sensor gain of $H_v = 1$, and all microcontroller variables that describe the output voltage being in units of volts. This resulted in the voltage compensator coefficients shown in Table 5.2.

TABLE 5.2
VOLTAGE COMPENSATOR DESIGN PARAMETERS FOR THE 2-CHANNEL PROTOTYPE

Parameter	Value
Cross-over frequency, ω_c	$2\pi 15$ rad/s
Voltage sampling period, T_v	100 µs
PWM clock frequency, f_{pwm}	90 MHz
Sensor ADC gain, H_v	1
Injected phase , ϕ_{max}	45°
Controller coefficients, b_{v0}, b_{v1}, b_{v2}	0.08615, 0.00067, -0.08548
Controller coefficients, a_{v1}, a_{v2}	1.955, -0.9555

5.3 Current Compensator Design

5.3.1 Open-Loop Model

The open-loop system transfer function relating i_{in} to t_{on} must be derived in order to design the current compensator. The average input current of the interleaved BCM boost converter can be calculated by using (5.1). This equation defines the time-averaged system model, and demonstrates how $i_{in(avg)}$ is a function of the input to the system t_{on} and the disturbance to the system v_{in}. By linearising (5.1) about a dc operating point, the system is described by the following linear time-averaged model.

$$\widetilde{i}_{in(avg)} = \frac{N}{2}\frac{V_{in}}{L}\widetilde{t_{on}} \tag{5.4}$$

where V_{in} is the dc operating point of the instantaneous input voltage, $\widetilde{i}_{in(avg)}$ is the deviation of the average input current from its dc operating point given by $\widetilde{i}_{in(avg)} = i_{in} - I_{in}$, and $\widetilde{t_{on}}$ is the deviation of the on-time from its dc operating point given by $\widetilde{t_{on}} = t_{on} - T_{on}$. By converting (5.4) into the Laplace domain, the open-loop transfer function of the power stage is derived as follows.

$$\frac{I_{in}(s)}{T_{on}(s)} = \frac{N}{2}\frac{V_{in}}{L} \tag{5.5}$$

The input current to the boost converter contains a large amount of current ripple due to the triangular shape of the inductor currents. The total input current is sensed using a shunt resistor connected to a differential amplifier with a single pole that acts as an analog low-pass filter. The low-pass filter is used in order to remove this switching-frequency ripple component. The amplifier's pole is placed at the angular frequency ω_p. The output of the differential amplifier is input to the microcontroller's ADC. The pole at ω_p is placed at a suitable frequency to attenuate the switching-frequency ripple from the input current. The switching frequency of the converter described in this work varies from 75 kHz up to 590 kHz. Therefore, the pole ω_p must be placed at a frequency much less than the minimum switching frequency to provide sufficient attenuation. However, placing the pole at too low a frequency can also reduce the current controller's frequency response.

The circuit diagram of the current-sense circuit is shown in Figure 5.4. It consists of a shunt resistor and differential-amplifier circuit. The shunt resistor is placed between the negative terminal of the input capacitor, and bridge rectifier, so that the circuit's ground is referenced to the same ground as the microcontroller. The relationship between the input current and the sense circuit's output voltage v_{iin} can be derived as

$$\frac{V_{iin}(s)}{I_{in}(s)} = R_{shunt}\frac{R_2}{R_1}\frac{1}{sR_2C_2+1} = R_{shunt}\frac{R_2}{R_1}\frac{1}{\frac{s}{\omega_p}+1} \tag{5.6}$$

where $V_{iin}(s)$ and $I_{in}(s)$ are the Laplace domain representations of the voltage v_{iin} and the

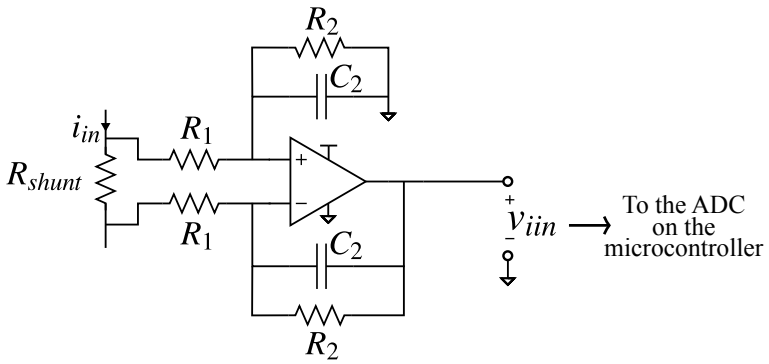


Figure 5.4. Current-sense differential op-amp circuit.

current i_{in} respectively. The resistor R_2 and the capacitor C_2 are chosen to achieve the selected pole angular frequency ω_p, while the ratio of the resistors R_1 to R_2 is selected to achieve the appropriate gain for the circuit, which scales the maximum measurable input current to the maximum readable ADC voltage.

With the addition of the current-sense circuit, the total open-loop system model now becomes

$$G_i(s) = \frac{H_i I_{in}(s)}{T_{on}(s)} = \frac{N}{2}\frac{V_{in}}{L}\frac{H_i\omega_p}{s+\omega_p} \tag{5.7}$$

The term H_i is the combined gain of the current-sense circuit and the microcontroller's ADC. It is clear from this transfer function that the open-loop gain of the system varies with the applied instantaneous dc input voltage V_{in}. This variation is shown in Figure 5.5, which plots the open-loop uncompensated system transfer function, described by (5.7), for different levels of input voltage. The curves are calculated for $H_i = 1$, and $f_p = 10$ kHz, where $f_p = \frac{\omega_p}{2\pi}$ is the pole's frequency in units of Hz. This is an undesirable characteristic as it lowers the system's gain when the input voltage is low, which causes the current controller's bandwidth to be reduced at lower input voltages. Later on in this section, an adaptive gain is introduced in the current compensator design that counteracts this unwanted variation in the open-loop system. The open-loop system phase response is unchanged by the input voltage.

The variation of the open-loop system magnitude and phase response for different pole frequencies from 3 kHz to 15 kHz is shown in Figure 5.6 . As the pole f_p is decreased, the gain of the magnitude response becomes lower at higher frequencies, thus the current loop is less effected by the noise created from the switching-frequency ripple on the input current. However, as f_p is increased, the phase response of the open-loop transfer function becomes more delayed. This reduces the phase margin of the controller and can lead to excessive peak-overshoot, or even instability. Therefore once the controller bandwidth is known, the pole f_p can be selected to be as low as possible while still achieving a suitable phase delay.

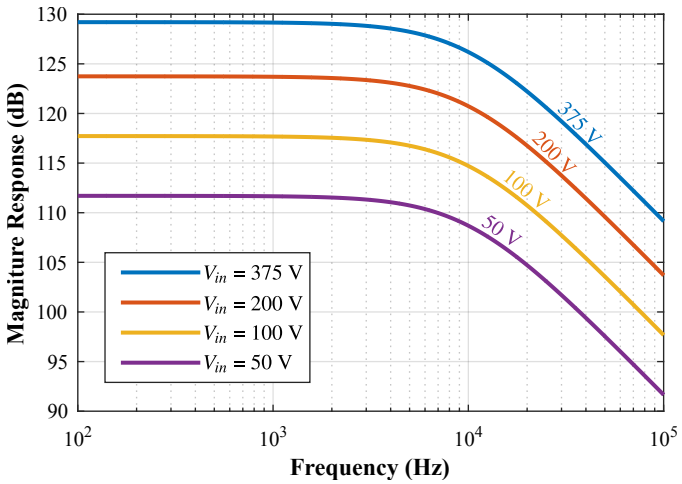
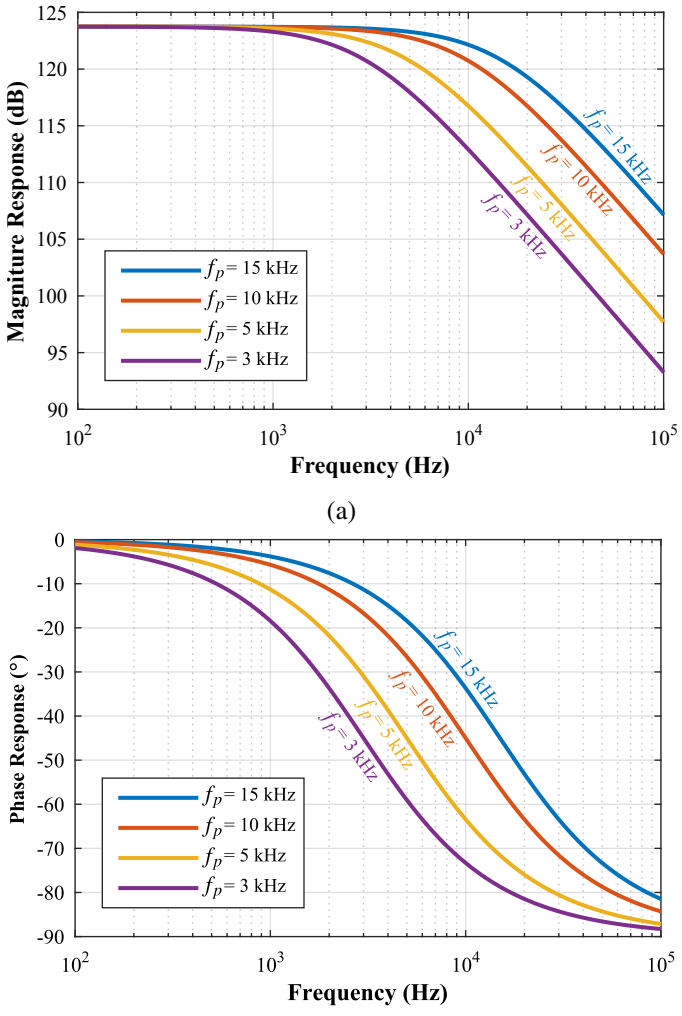


Figure 5.5. Open-loop system magnitude response $|G_i(s)|$ calculated at different levels of instantaneous input voltage, calculated with $H_i = 1$ and $\omega_p = 2\pi 10$ krad/s.



(a)

(b)

Figure 5.6. Open-loop system magnitude response $|G_i(s)|$ and phase response $\angle G_i(s)$ calculated at different pole frequencies f_p.

5.3.2 Selecting the Controller's Bandwidth

A suitable controller bandwidth and phase margin must be selected to design the current compensator. Selecting the phase margin to be between 45° and 60° is a suitable choice,

as it provides a good trade-off between settling time and peak overshoot of the controller's transient response. The bandwidth on the other hand, must be high enough to track the reference current, which has the shape of a rectified sinusoid at a given line frequency. The reference current i_{ref} can be approximated as an ideal rectified sinusoid.

$$i_{ref} = I_{ref(pk)} \left| \sin(\omega_L t) \right| \tag{5.8}$$

where $I_{ref(pk)}$ is the peak value of the reference sinusoid, which is the same magnitude as the peak value of the line current and rectified input current. Figure 5.8 demonstrates the waveshape of the reference current over two line cycles.

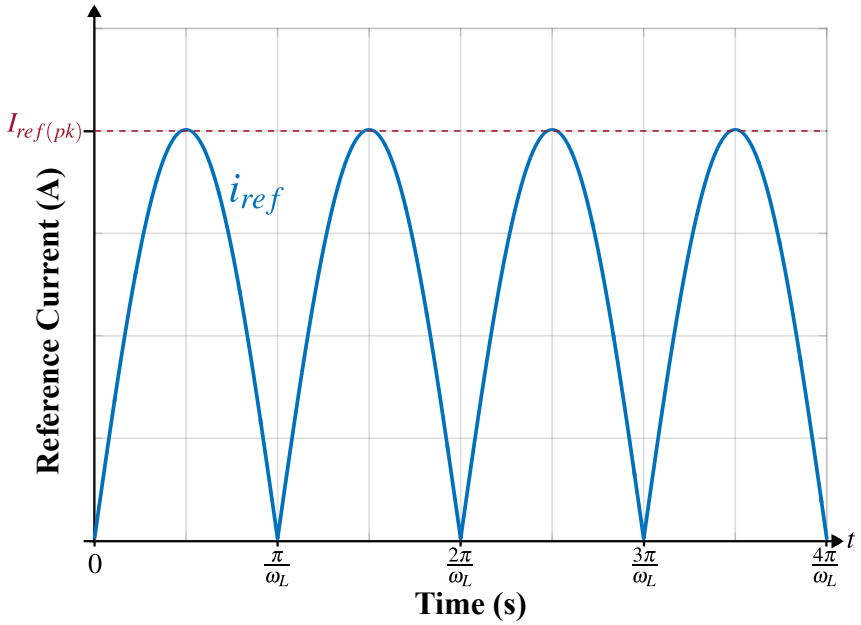


Figure 5.7. The waveshape of the rectified-sinusoidal reference current with amplitude $I_{ref(pk)}$ and an angular line frequency of ω_L.

The frequency-domain representation of the reference current can be calculated by using Fourier analysis. This frequency spectrum is shown in Figure 5.8, which depicts the magnitude plotted on a log scale and the frequency along the x-axis given in multiples of the line frequency. The plot demonstrates that the reference current contains a dc part with a magnitude of $\frac{2}{\pi} I_{ref(pk)}$, and parts at every even harmonic of the line frequency, with decreasing magnitude as frequency increases. Once the harmonic index is greater than 12, the magnitude of the harmonic is less than one hundredth of the peak of the reference current. Therefore, the significant harmonics in the spectrum of the reference current are limited to about the 12^{th} harmonic, which for a 50 Hz line frequency is 600 Hz, and for a 60 Hz harmonic is 720 Hz. Since the current compensator must be capable of tracking this reference it must have a bandwidth greater than these frequency.

The bandwidth for a typical CCM boost-converter current compensator is set in the

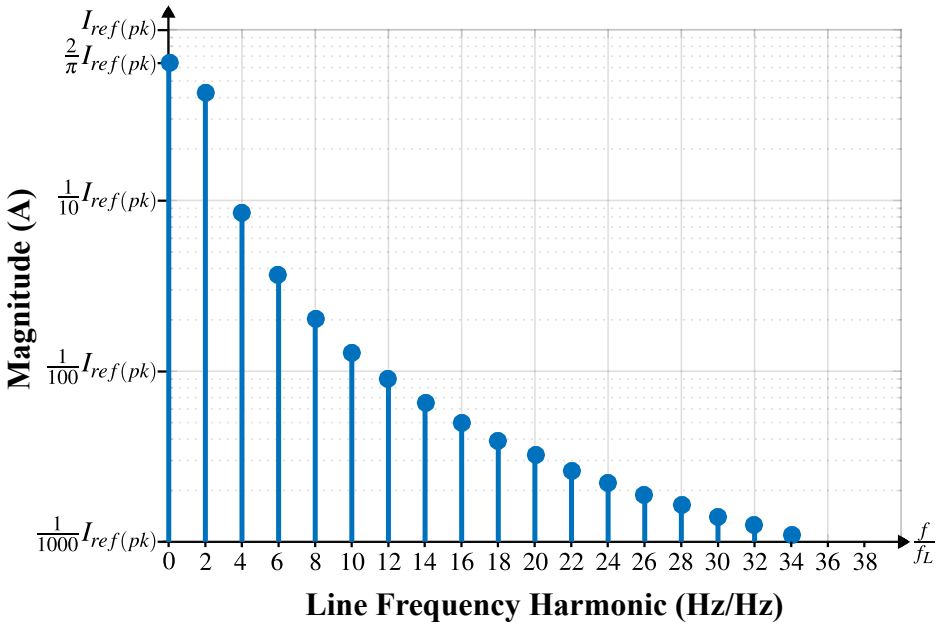


Figure 5.8. The frequency spectrum of a rectified-sinusoidal reference current with amplitude $I_{ref(pk)}$ and an angular line frequency of ω_L.

frequency range of 2 kHz to 10 kHz. This is a suitable frequency range that allows for good tracking of a rectified sinusoid. Setting the bandwidth higher allows the current compensator to react better to disturbances and other effects that may distort the line current. For instance, in a CCM boost converter the line current is heavily distorted as the system transitions from DCM operation to CCM operation during every line cycle. Increasing the bandwidth can reduce this distortion. The downside to increasing the bandwidth is that the system becomes more susceptible to high-frequency noise created by the switching frequency ripple. Furthermore, an increased bandwidth can increase the high-order current harmonics of the line frequency drawn by the converter.

For the BCM boost converter, selecting the bandwidth in the same frequency range of 2 kHz to 10 kHz is also a suitable choice. The high bandwidth ensures that the current compensator can track the reference rectified sinusoid, and also ensures that the compensator can significantly reduce the line-current distortion from the valley switching and input capacitor. In this work, the bandwidth is placed at 4 kHz.

5.3.3 Controller Design

An integral controller is a suitable choice to achieve the 4 kHz bandwidth and greater than 45° phase margin. The analog transfer function of an integral controller is given by

$$C_c(s) = \frac{K_i}{s} \tag{5.9}$$

where the term K_i is a constant term selected to achieve the desired cross-over frequency. The integral action of the controller ensures zero steady-state tracking error. The controller

additionally introduces a phase advance of 90°.

The current-sensor pole frequency f_p is selected to achieve the desired phase margin. For a greater-than 45° phase-margin, the current-sensor must introduce a phase-delay less than −45° at the cross-over frequency. From an examination of Figure 5.6(b) a suitable pole frequency can be selected to achieve this phase delay. Hence the frequency f_p is selected $f_p = 10$ kHz, and $\omega_p = 2\pi 10$ krad/s, which corresponds to a phase-delay of around −30°.

The bilinear transformation is used to derive a digital controller transfer function with similar frequency characteristics as the analog controller defined by (5.9). The bilinear transformation approximates the Laplace operator $s = j\omega$, as a function of the $\mathcal{Z}$-domain operator $z = e^{j\omega T_m}$ as follows:

$$s = \frac{T_m}{2}\frac{z-1}{z+1} \tag{5.10}$$

where T_m is the sampling rate of the input current. The sampling rate is chosen to be identical to the sampling rate of the phase-shift control in order to simplify the firmware design. Substituting the bilinear transformation into (5.9), leads to the following current controller transfer function in the $\mathcal{Z}$-domain with similar characteristics to the analog controller.

$$C_c(z) = K_i\frac{2}{T_m}\frac{z+1}{z-1} = k_{ci}\frac{z+1}{z-1} \tag{5.11}$$

The term k_{ci} is the gain of the digital controller, and is selected to achieve the desired cross-over frequency. The compensated open-loop current-loop transfer function must be derived to determine the appropriate value for k_{ci}.

Fig. 5.9 shows the control block diagram of the current loop. The sensed input current is subtracted from the reference signal to generate the current error signal which is input into the current compensator. The transfer function $C_c(z)$ is the current-compensator transfer function implemented in microcontroller software. The microcontroller introduces a delay of z^{-1} and a zero-order hold (ZOH). The transfer function of the current-sense circuitry is given by $H_i\frac{\omega_p}{s+\omega_p}$.

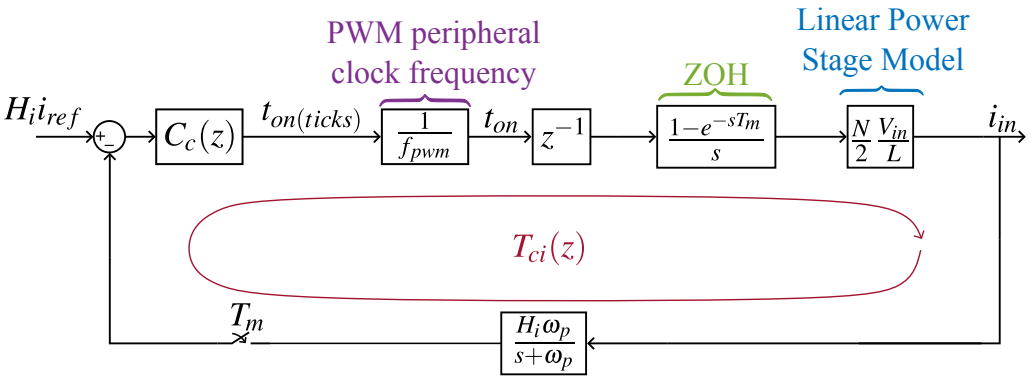


Figure 5.9. Control block diagram of the current loop.

Thus, the full compensated open-loop transfer function $T_{ci}(z)$ is given by

$$\begin{aligned} T_{ci}(z) &= z^{-1}\frac{1}{f_{pwm}}H_i C_c(z)\mathcal{Z}\left\{\frac{1-e^{-sT_m}}{s}\frac{N}{2}\frac{V_{in}}{L}\frac{1}{\frac{s}{\omega_p}+1}\right\} \\ &= z^{-1}\frac{1}{f_{pwm}}H_i C_c(z)\frac{N}{2}\frac{V_{in}}{L}\frac{1-e^{-\omega_p T_m}}{z-e^{-\omega_p T_m}} \end{aligned} \tag{5.12}$$

Therefore, the gain k_{ci} can be determined by setting the system's open-loop gain, defined in (5.12), equal to unity at $z = e^{j\omega_{ci}T_m}$.

$$|T_{ci}(e^{j\omega_{ci}T_m})| = 1 \tag{5.13}$$

Substituting the terms in (5.11) and (5.12) for $C_{ci}(z)$ and $T_{ci}(z)$ respectively into (5.13) and re-arranging, the following expression can be found for the digital current compensator gain

$$k_{ci} = \frac{2Lf_{pwm}|e^{j\omega_{ci}T_m}-1||e^{j\omega_{ci}T_m}-e^{-\omega_p T_m}|}{NV_{in(max)}H_i(1-e^{-\omega_p T_m})\,|e^{j\omega_{ci}T_m}+1|} \tag{5.14}$$

The gain k_{ci} is initially calculated at the maximum input voltage of $V_{in(max)}$ to ensure system stability, which occurs at the peak of the line voltage $V_{in(max)} = \max\langle V_{in(pk)}\rangle = 265\sqrt{2}$ V = 375 V.

With the terms k_{ci} and ω_p both defined, the transfer function for the current compensator $C_c(z)$ in (5.11) is fully defined. As a result, the compensated open-loop response can be calculated using the value determined for k_{ci}. Figure 5.10 shows the compensated open-loop Bode plots at different levels of input voltage of the prototype converter, with Figure 5.10(a) showing the magnitude response and Figure 5.10(b) showing the phase response. The prototype converter is a 2-channel interleaved boost converter, with a boost inductance of $L =$ 130 µH and a sampling rate of $T_m = 10$ µs. It can be observed that as the instantaneous input voltage drops, the controller phase response stays the same, but the cross-over frequency of the system is dramatically decreased from 4 kHz at 400 V, to below 600 Hz at 50 V. This is a very undesirable trait, because for the current compensator to successfully reduce the zero-crossing distortion, which occurs at low levels of input voltage, it must have very fast tracking performance under this condition.

The phase response of the compensated system does not change with the input voltage. However, since a lower input voltage reduces the system's bandwidth, the frequency at which the phase margin is defined is reduced. The phase margin ϕ_m is defined as 180° degrees minus the system's phase delay at the controller's bandwidth, such that $\phi_m = 180° - \angle T_{ci}(e^{j\omega_{ci}T_m})$. Hence, as the input voltage is lowered, the phase margin approaches 90°, resulting in the system's response becoming more damped.

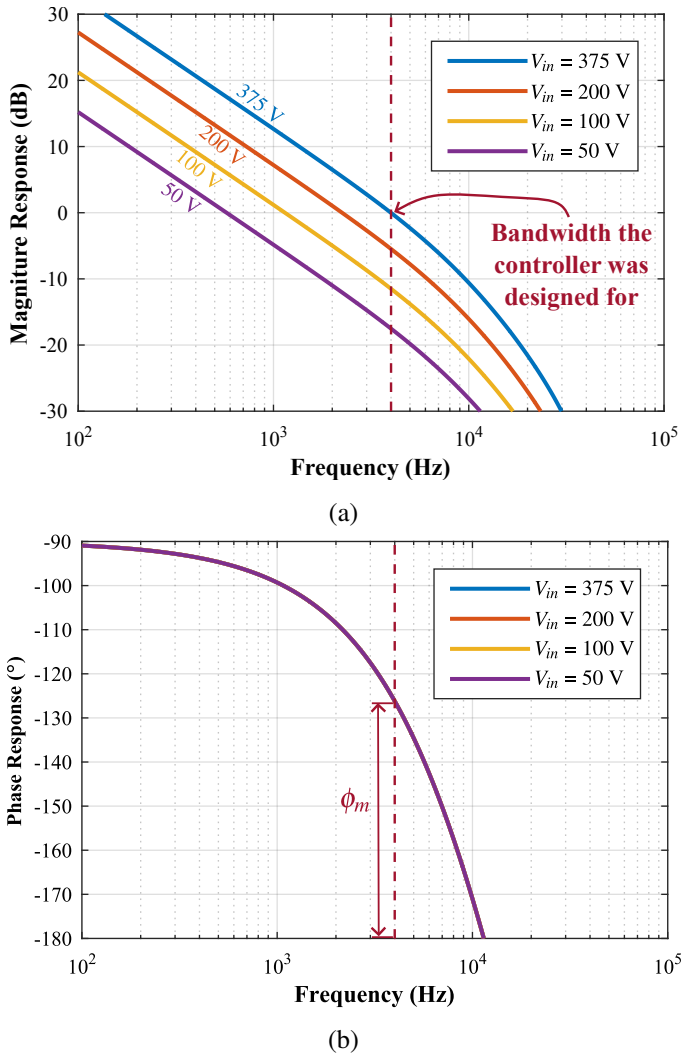


Figure 5.10. Compensated open-loop magnitude response $|T_{ci}(z)|$ and phase response $\angle T_{ci}(z)$ variation with V_{in}.

5.3.4 Adaptive Gain

An adaptive gain k_i was used to adjust the gain of the current compensator in order to counteract the reduced controller bandwidth at low input voltage. From (5.14) it is clear that the gain k_{ci} is inversely proportional to V_{in}. Therefore, by adjusting k_i inversely proportionately to the rectified input voltage v_{in}, as follows:

$$k_i = \frac{V_{in(max)}}{v_{in}} \tag{5.15}$$

the bandwidth of the current compensator remains at the desired value, irrespective of the applied instantaneous input voltage.

The gain k_i calculated per (5.15) is shown in Figure 5.11, plotted over the entire range of the input voltage v_{in}. Since the gain k_i approaches infinity as the input voltage tends towards zero, an upper limit of 15 is enforced on the gain k_i. This function was implemented in the prototype converter using a division function since an expensive microcontroller was

used. However, the function can also be easily implemented using a LUT to reduce the computational requirements associated with a division operation.

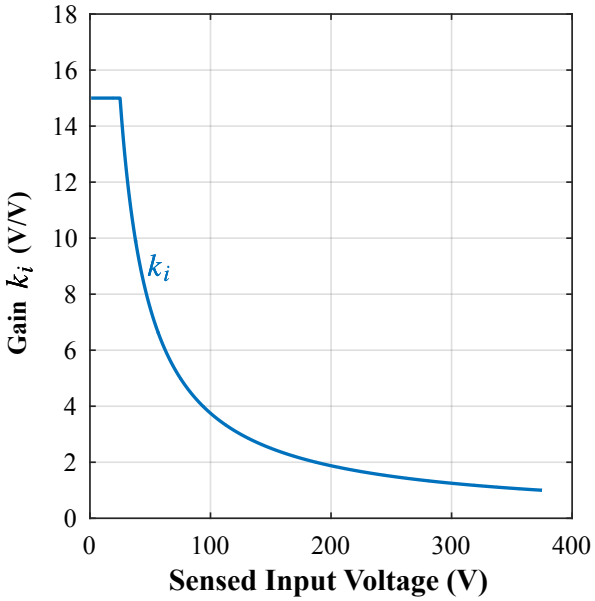


Figure 5.11. Plot of the gain k_i as a function of the input voltage.

5.3.5 Controller Implementation

A time-domain recursive algorithm describing the controller is required for implementation in the microcontroller software. This recursive algorithm can be derived from the current controller transfer function defined in (5.11). However, this controller transfer function must be re-written to include the adaptive gain k_i. Hence,

$$C_c(z) = \frac{T_{on(ticks)}(z)}{E_c(z)} = k_i \frac{k_{ci} + k_{ci} z^{-1}}{1 - z^{-1}}$$

where the term $E_c(z)$ is the $\mathcal{Z}$-domain representation of the scaled current error signal $e_c[n] = H_i(i_{ref}[n] - i_{in}[n])$. In order to convert this $\mathcal{Z}$-domain transfer function to the time-domain, it is easiest to first re-arrange the equation as follows

$$T_{on(ticks)}(z)\left(1 - z^{-1}\right) = E_c(z) k_i \left(k_{ci} + k_{ci} z^{-1}\right)$$

$$T_{on(ticks)}(z) = E_c(z) k_i \left(k_{ci} + k_{ci} z^{-1}\right) + T_{on(ticks)}(z)\left(z^{-1}\right) \tag{5.16}$$

The expression defined in (5.16) can now be converted to the time-domain to obtain the following discrete-time expression.

$$t_{on(ticks)}[n] = k_i(k_{ci} e_c[n] + k_{ci} e_c[n-1]) + t_{on(ticks)}[n-1] \tag{5.17}$$

The recursive algorithm is now defined by (5.17), and can be used to implement the controller if the microcontroller uses floating-point arithmetic.

A full parameter list of the current-compensator design parameters used in the prototype converter is given in Table 5.3, including the controller gain k_{ci}.

TABLE 5.3
CURRENT COMPENSATOR DESIGN PARAMETERS

Parameter	Value
Cross-over frequency, ω_{ci}	2π4000 rad/s
Controller phase margin , ϕ_m	53°
Current sampling period, T_m	10 µs
PWM clock frequency, f_{pwm}	90 MHz
Sensor-ADC gain, H_i	1
Current-sense pole frequency, f_p	10 kHz
Controller gain, k_{ci}	4.234

A full block diagram of the current controller is depicted in Figure 5.12, which shows the current reference generation, the adaptive gain, the compensator's recursive algorithm, and the typical waveshapes of i_{ref}, v_{in}, k_i and t_{on} over a full line cycle.

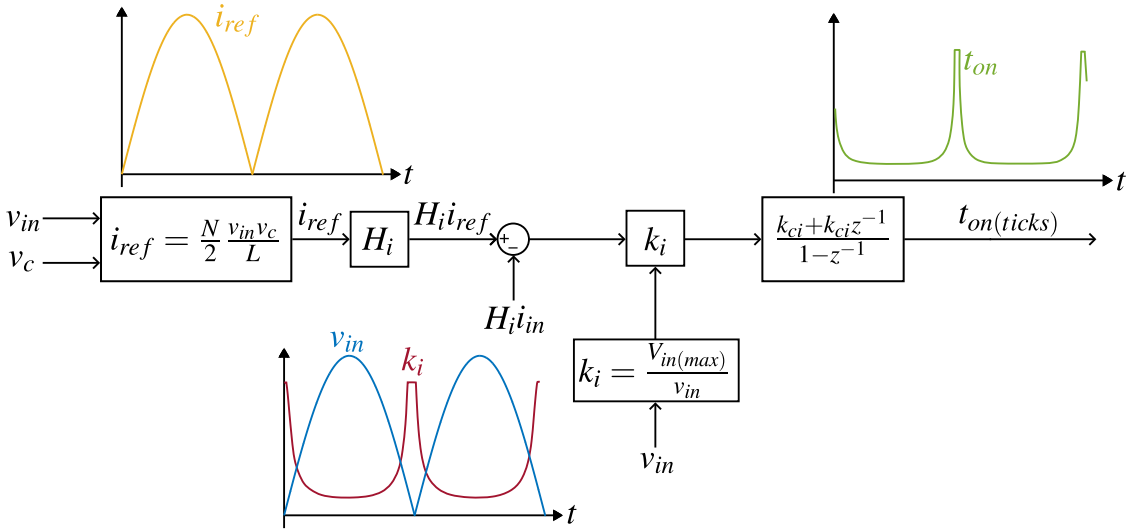


Figure 5.12. Current compensator detailed structure including the adaptive gain.

5.3.6 Distortion-Free Current-Sensor and Voltage-Sensor

Depending on the implementation of the current sensor or voltage sensor, the sensed input current and input voltage can be distorted by the zero-crossing distortion of the converter.

For instance, it is important that the current sense resistor R_{shunt} is placed on the line side of the input capacitor, so that it senses the current i_{in} and not the current $i_{L1}+i_{L2}+\ldots+i_{LN}$, as depicted in Figure 5.13, as this ensures that the current compensator also acts to reduce the input-capacitor distortion. Figure 5.13 also shows how the input voltage is sensed using two extra diodes D_{s1} and D_{s2}. Doing this is important as it ensures the rectified input line

voltage is sensed, as opposed to the voltage across C_{in}, which is also distorted by the valley switching.

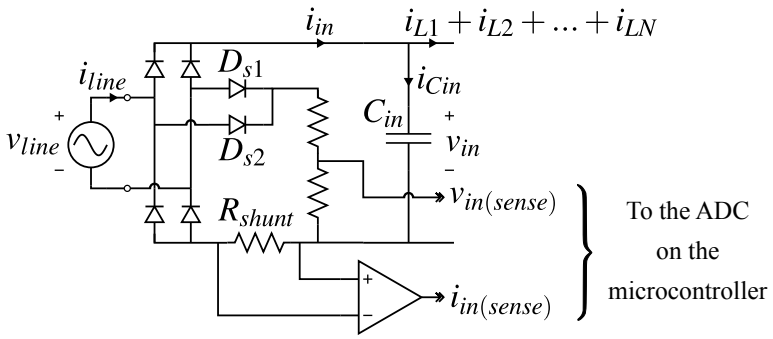


Figure 5.13. Position of the current-sense shunt resistor R_{shunt} in the prototype converter.

5.4 Firmware Design

This section describes the firmware used to implement the COTC, ACMC and FF control methods described in this chapter. The prototype converter described in this section is a 2-channel 600 W interleaved BCM boost converter. The prototype uses a powerful TMS320f28069 microcontroller from Texas Instruments.

5.4.1 Interfacing the Microcontroller with the Hardware

Figure 5.14 shows a simplified diagram of the boost converter control circuitry and how it interfaces with the power stage. This is similar to the diagram given in Chapter 2,Figure 2.23, except that the converter has only 2 channels and a different microcontroller is used. The microcontroller now executes the ACMC scheme. The other difference is that both the sensed input voltage and sensed input current are used as part of the control algorithms, as well as for safety protection functions.

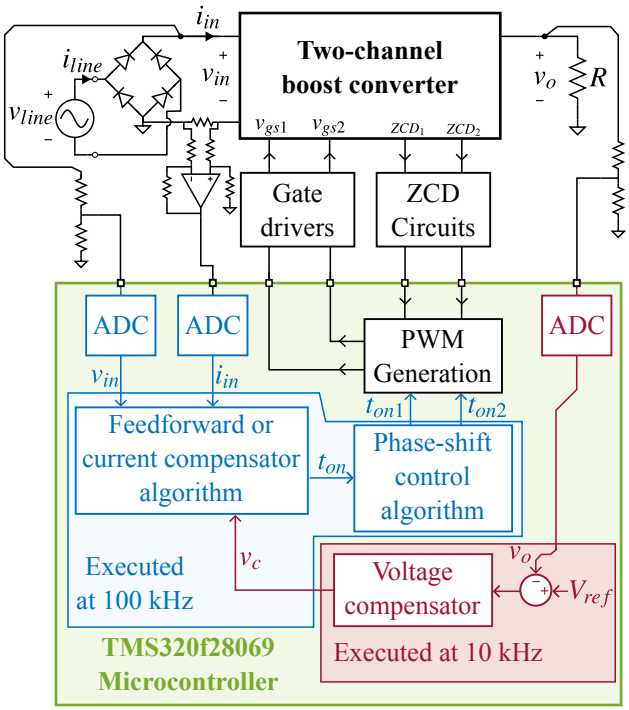


Figure 5.14. Two-channel boost converter control circuit.

5.4.2 Software Flow

The microcontroller code runs the same state-machine and voltage-loop interrupt as described in Chapter 2. However, floating-point math is used, and the voltage-loop interrupt execution rate is increased to to 10 kHz.

The phase-shift control interrupt on the other hand was expanded upon to include the ACMC algorithms. Hence, the feedforward control algorithm, current-compensator algorithm and phase-shift control algorithm are all executed in the same interrupt at a rate of 100 kHz.

A software flow block diagram describing this interrupt is presented in Figure 5.15. The interrupt is called by a timer independent of the CPU, which ensuresa fixed execution frequency.

Once the interrupt is called, the input voltage and input current are read from their appropriate ADC registers. The sensed input voltage is scaled and multiplied by the voltage compensator output to generate the current reference. The recursive current controller algorithm calculates the switch on-time. Then, the phase-shedding and phase-shift control algorithms are executed similar to the manner described by Figure 3.21, except for a 2-channel boost converter. The phase-shift control algorithm calculates the on-time of each individual channel, which is used to update the PWM registers. With the PWM registers updated, the interrupt exits execution.

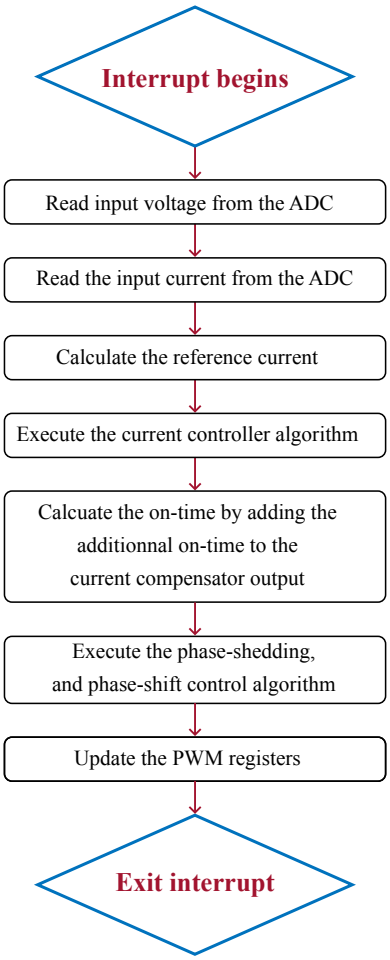


Figure 5.15. Software-flow block diagram description of the phase-shift control interrupt function.

5.5 Experimental Results

A 600 W prototype of the interleaved BCM boost PFC converter was built, and is capable of using either COTC, COTC with FF control or ACMC. Table 5.4 gives a list of the main parameters which describe the converter.

TABLE 5.4
LIST OF POWER STAGE PARAMETERS

Parameter	Value
Microcontroller	TMS320F28069
Number of channels, N	2
Boost inductance, L	130 µH
Output capacitance, C	360 µF
Output voltage, V_o	400 V
RMS line voltage, $V_{in(rms)}$	85 V to 265 V
Output Power P_o	0 W to 600 W
Voltage compensator sampling time, T_v	100 µs
Current compensator sampling time, T_m	10 µs

5.5.1 Steady-State Operation

The steady-state waveforms of the output voltage v_o, the line voltage v_{line}, the input current i_{in} and the inductor current i_{L1} are given in Figure 5.16. The waveforms are taken at 600 W output and 115 Vrms input. Similarly, Figure 5.17 shows the same waveforms but measured at 230 Vrms. Both sets of waveforms show the converter successfully regulating the output voltage at 400 V, and maintaining decent phase-shift control.

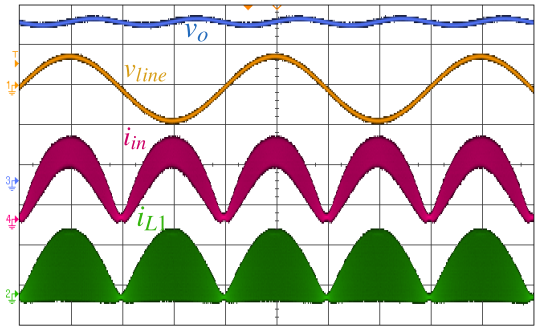


Figure 5.16. Line voltage v_{line}, inductor current i_{L1}, output voltage v_o and input current i_{in} when the converter operates at rated power of P_o = 600 W at 115 Vrms. (v_{line}: 200 V/div, i_{L1}: 5 A/div, v_o: 100 V/div, i_{in} = 5 A/div , timebase : 5 ms/div).

5.5.2 Improvement from the Adaptive Gain

The waveshape of the line current was examined with and without the adaptive gain k_i enabled in order to verify its effectiveness. The comparison is shown in Figure 5.18. The measurements are taken at 450 W and 115 Vrms. Figure 5.18(a) shows the waveshape of

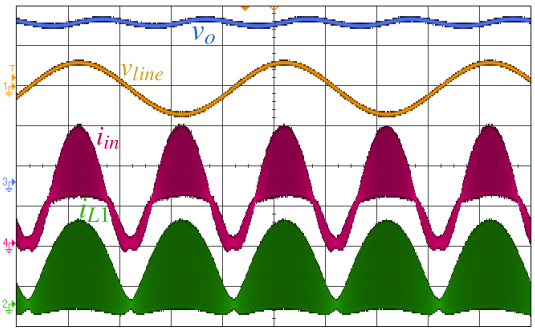
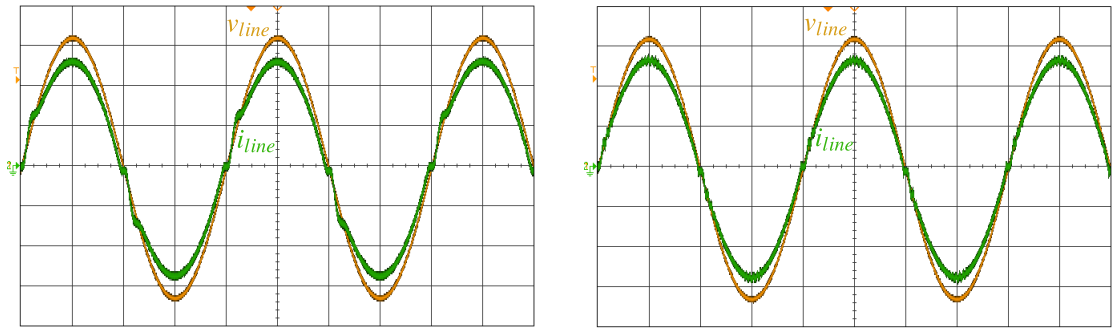


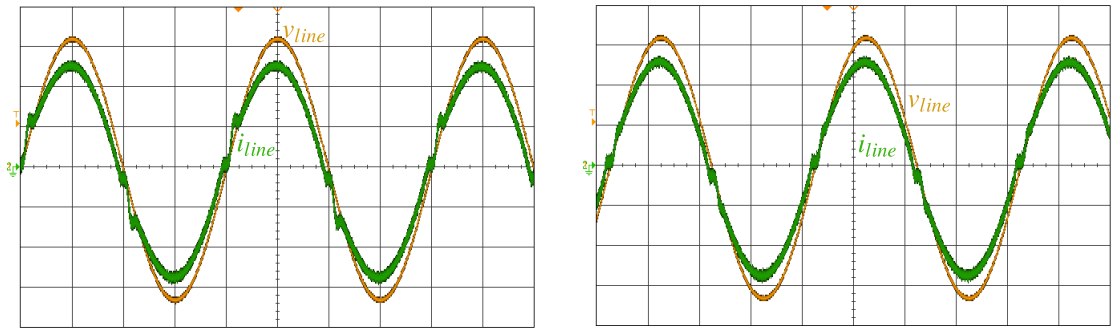
Figure 5.17. Line voltage v_{line}, inductor current i_{L1}, output voltage v_o and input current i_{in} when the converter operates at rated power of P_o = 600 W at 230 Vrms. (v_{line}: 500 V/div, i_{L1}: 2 A/div, v_o: 100 V/div, i_{in} = 2 A/div, timebase : 5 ms/div).

the line current when the adaptive gain is not enabled, and Figure 5.18(b) shows the line current when the adaptive gain is enabled. The same comparison is shown in Figure 5.19 but measured at 230 Vrms. The comparisons demonstrate that when the adaptive gain is enabled the line current has a more sinusoidal shape, especially near the cross-over point of the line voltage.



(a) (b)

Figure 5.18. v_{line} and i_{line} at P_o = 450 W and at 115 Vrms (a) no adaptive gain ($k_i = 1$), (b) an adaptive gain $\left(k_i = \frac{V_{in(max)}}{v_{in}}\right)$. ($v_{line}$: 50 V/div, i_{line}: 2 A/div, timebase: 5 ms/div)



(a) (b)

Figure 5.19. v_{line} and i_{line} at P_o = 450 W and at 230 Vrms (a) no adaptive gain ($k_i = 1$), (b) an adaptive gain $\left(k_i = \frac{V_{in(max)}}{v_{in}}\right)$. ($v_{line}$: 100 V/div, i_{line}: 1 A/div, timebase: 5 ms/div)

The power factor of the converter was measured at different line and load voltages to

ensure that the adaptive gain always provided an improvement in power quality. Figure 5.20 shows the measured power-factor comparison taken at 115 Vrms and 230 Vrms. It is evident from the comparison that the adaptive gain always improves the power factor for ACMC.

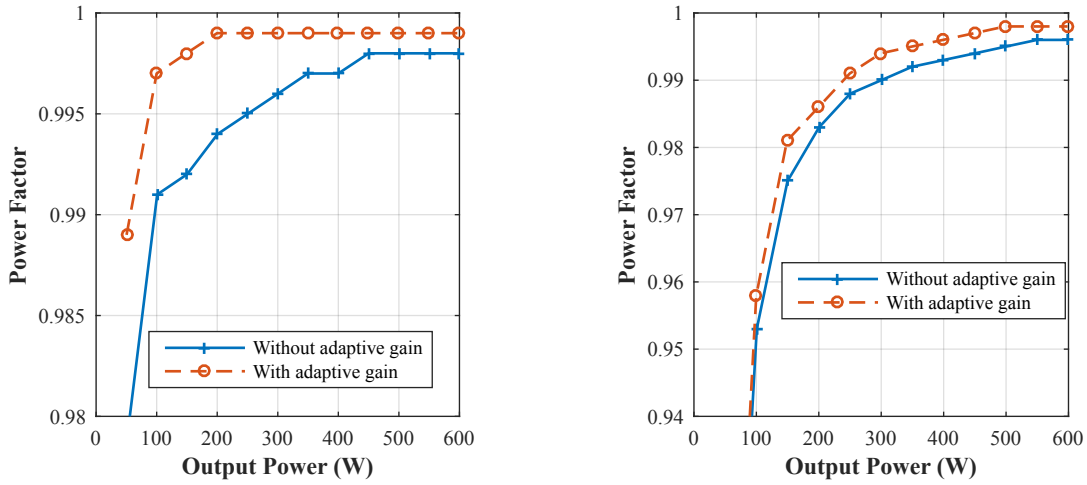


Figure 5.20. Power-factor comparison with and without the adaptive gain k_i enabled, measured at (a) 115 Vrms and (b) 230 Vrms.

5.5.3 Line-Current Comparison

The waveshape of the line current with ACMC was compared to the waveshape when COTC and FF control schemes were used. These comparisons are shown in Figure 5.21 which is measured at 200 W output and 115 Vrms. Figure 5.21(a), Figure 5.21(b) and Figure 5.21(c) show the waveshape of the line current when the COTC, COTC with FF and ACMC are used respectively. Figure 5.21(a) demonstrates that when COTC is used there is significant line-current cross-over distortion. If FF control is used the distortion is dramatically reduced. However, when ACMC is used the line current demonstrated the most sinusoidal shape with the least distortion.

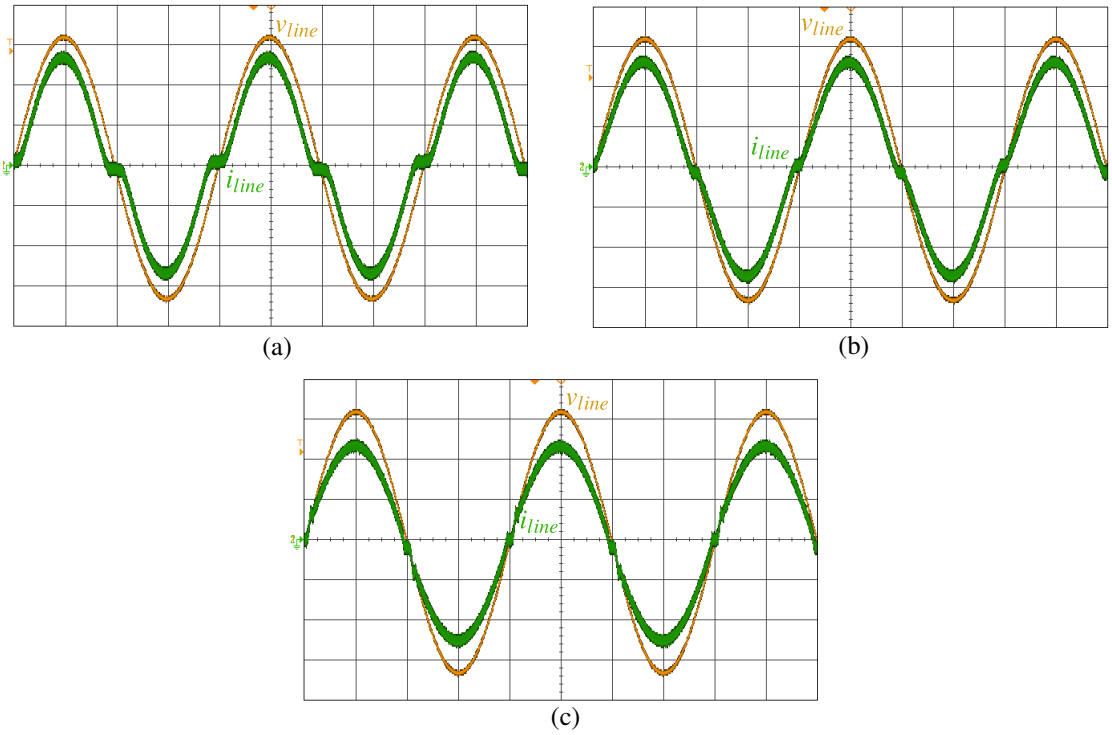


Figure 5.21. v_{line} and i_{line} at 200 W and 115 Vrms using (a) COTC, (b) COTC with FF and, (c) ACMC (v_{line}: 50 V/div, i_{line}: 1 A/div, timebase: 5 ms/div).

Figure 5.22 gives the same line-current comparison but measured at 230 Vrms instead of 115 Vrms. The FF control algorithm is not as effective at removing the line-current distortion at the higher input voltage, due to the the input-capacitor distortion which becomes more dominant at higher line voltages. It is clear from comparing the waveshapes of each control scheme that ACMC provides the best improvement in power quality at 230 Vrms also.

Further line-current comparisons are given in Figure 5.23, Figure 5.24, Figure 5.25 and Figure 5.26. Figure 5.23 is taken at 450 W and 115 Vrms. Figure 5.24 is taken at 450 W and 230 Vrms.

Figure 5.25 is taken at 600 W and 115 Vrms. Figure 5.26 is taken at 600 W and 230 Vrms. Each comparison demonstrates that COTC suffers significant line-current distortion, FF control reduces this line-current distortion and the best reduction in the distortion is

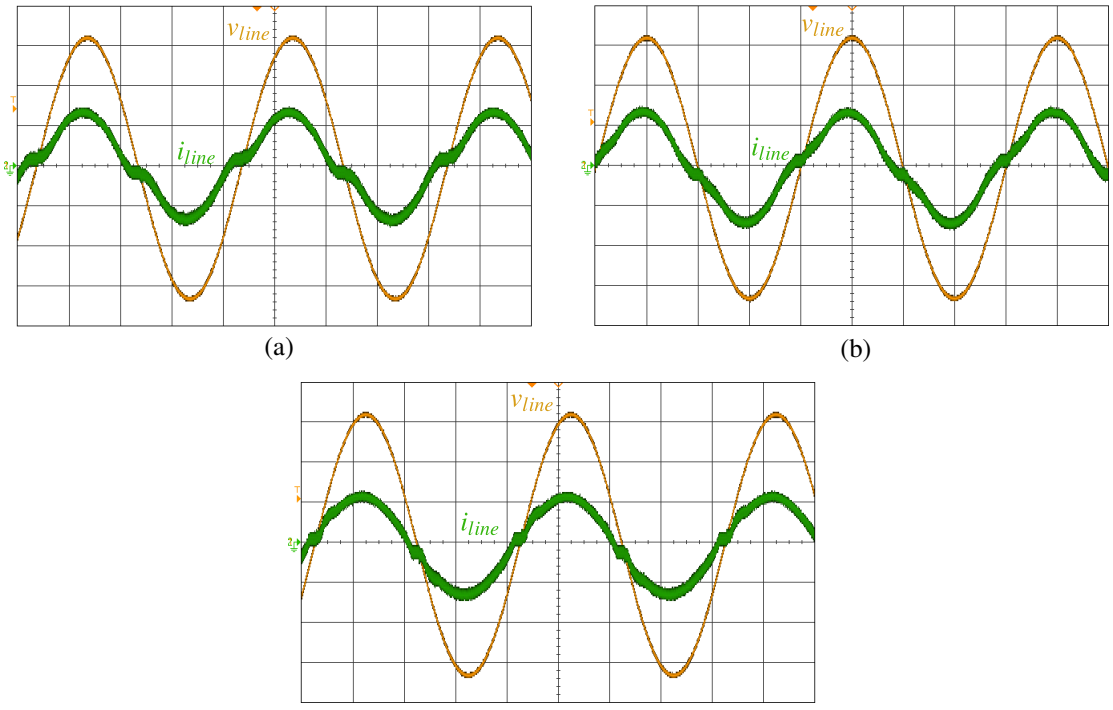


Figure 5.22. v_{line} and i_{line} at 200 W and 230 Vrms using (a) COTC, (b) COTC with FF and, (c) ACMC (v_{line}: 100 V/div, i_{line}: 1 A/div, timebase: 5 ms/div).

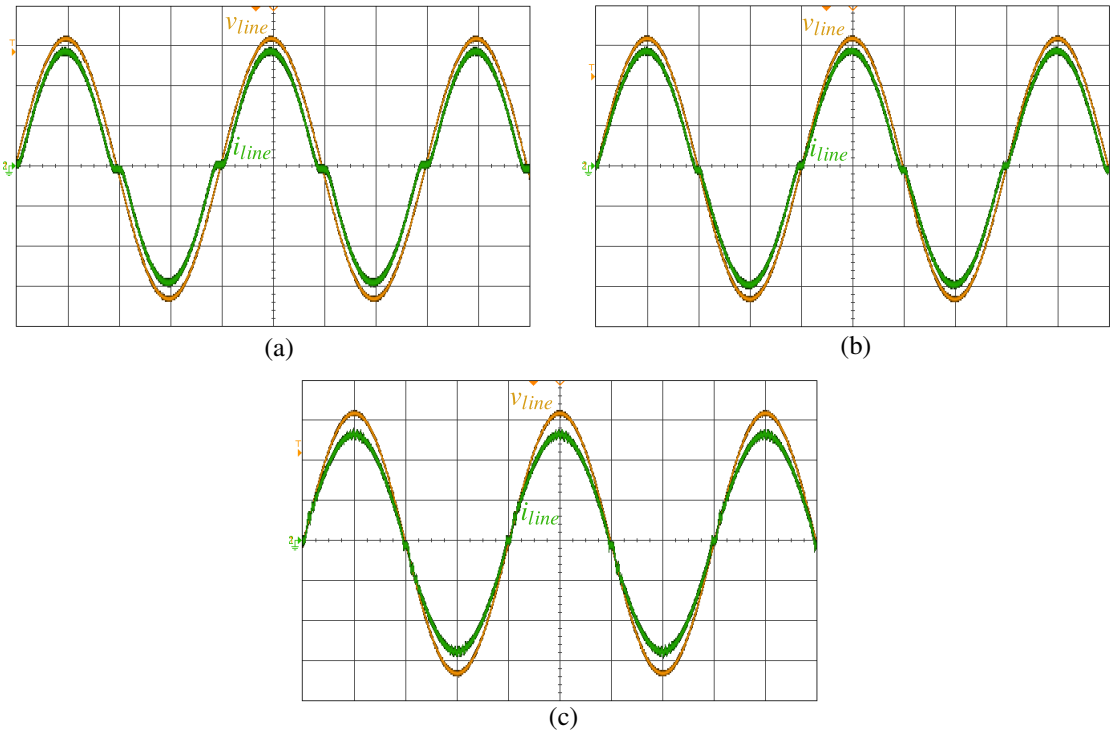


Figure 5.23. v_{line} and i_{line} at 450 W and 115 Vrms using (a) COTC, (b) COTC with FF and, (c) ACMC (v_{line}: 50 V/div, i_{line}: 2 A/div, timebase: 5 ms/div).

achieved by ACMC.

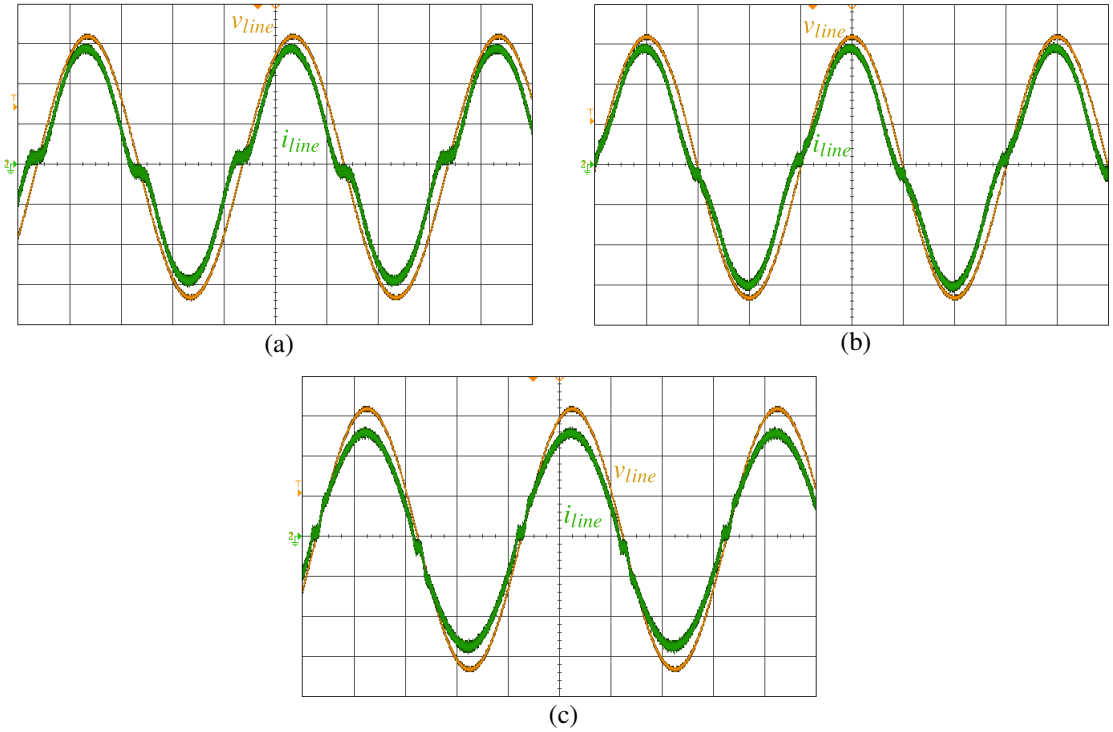


Figure 5.24. v_{line} and i_{line} at 450 W and 230 Vrms using (a) COTC, (b) COTC with FF and, (c) ACMC (v_{line}: 100 V/div, i_{line}: 1 A/div, timebase: 5 ms/div).

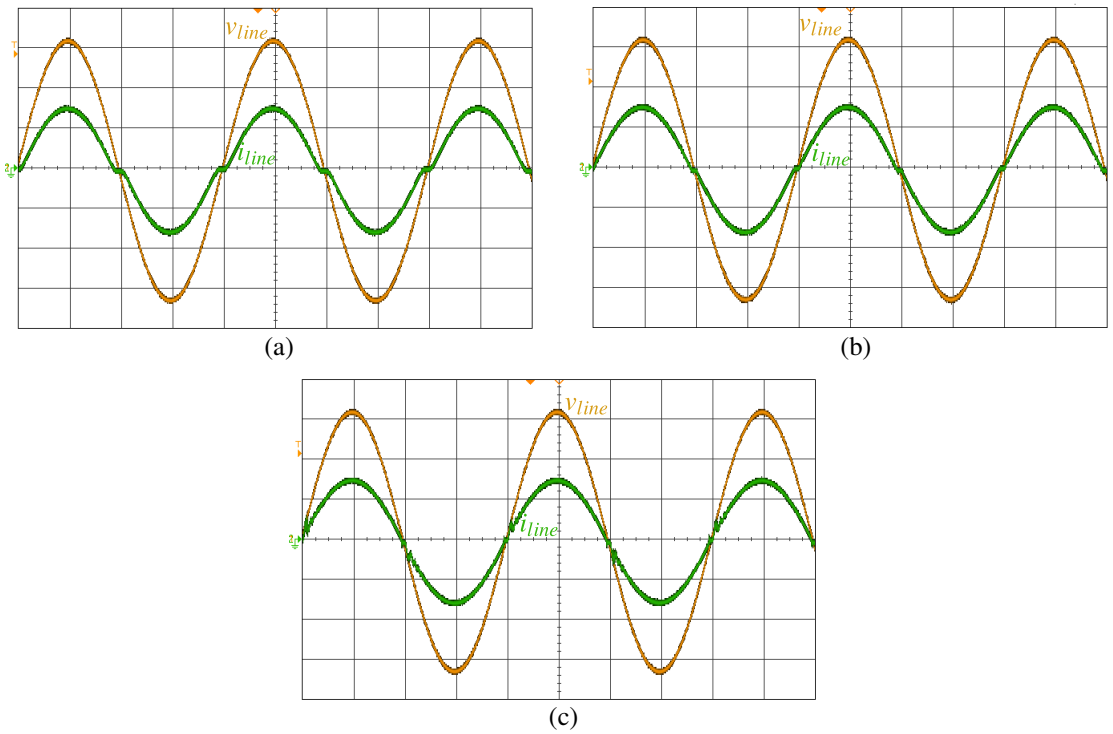


Figure 5.25. v_{line} and i_{line} at 600 W and 115 Vrms using (a) COTC, (b) COTC with FF and, (c) ACMC (v_{line}: 50 V/div, i_{line}: 5 A/div, timebase: 5 ms/div).

5.5.4 PF and ICH

The power factor of the three schemes was measured at different loads and line voltages to verify that the ACMC scheme worked well under all operating conditions. The measured power factor of each control scheme with load is shown in Figure 5.27. Figure 5.27(a) shows

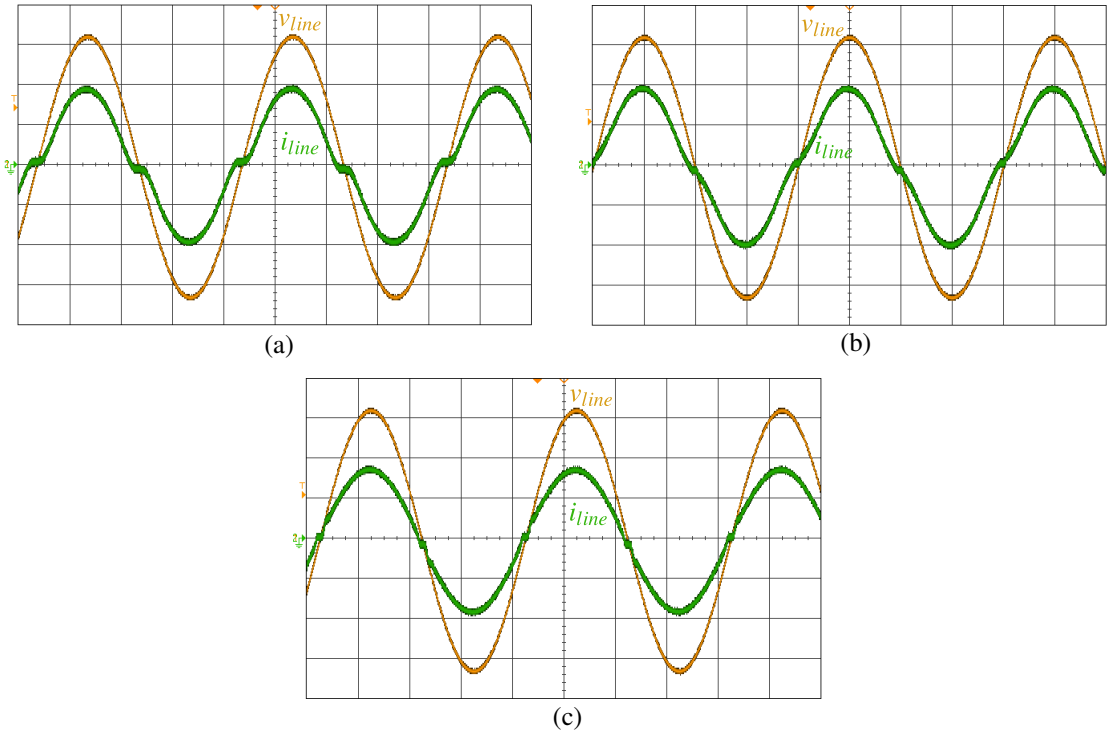


Figure 5.26. v_{line} and i_{line} at 600 W and 230 Vrms using (a) COTC, (b) COTC with FF and, (c) ACMC (v_{line}: 100 V/div, i_{line}: 2 A/div, timebase: 5 ms/div).

the measured power factor at 115 Vrms and Figure 5.27(a) shows the measured power factor at 230 Vrms.The power-factor comparisons show ACMC provides the best power factor at all load and line conditions. COTC with FF control also provides significant improvement but not as much as ACMC.

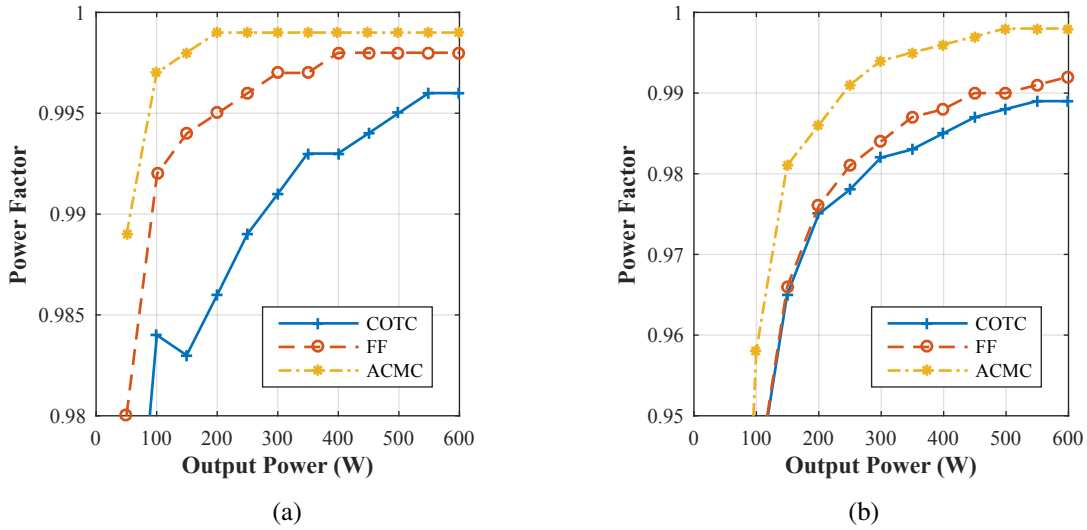
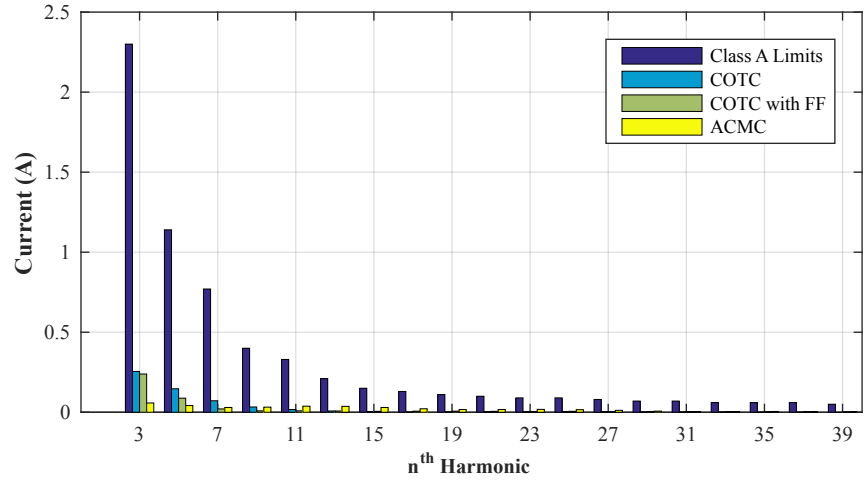


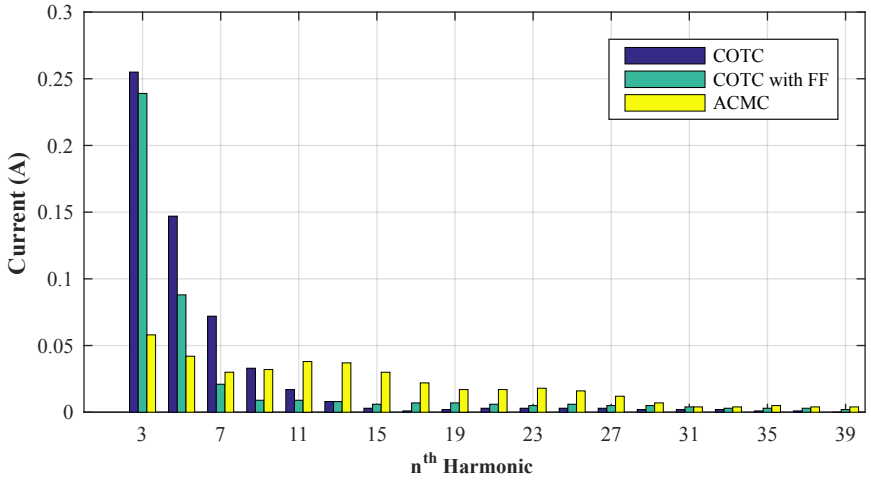
Figure 5.27. Power-factor comparison between COTC, COTC with FF control and ACMC, measured at (a) 115 Vrms and (b) 230 Vrms.

Figure 5.28 gives a comparison of the current harmonics of the three control schemes. Figure 5.28(a) includes the EN61000-3-2 Class A limits demonstrating that each control

scheme is well below the limits. Figure 5.28(b) provides a current-harmonic comparison of the three control schemes only, without the limits to allow for a more visible comparison. The measurements are taken at 230 Vrms and 600 W output. The results show that ACMC provides the lowest harmonic magnitudes especially at the 3rd harmonic.



(a)



(b)

Figure 5.28. The input current harmonics measured at 230 Vrms and 600 W, for COTC, COTC with FF control and ACMC . In subfigure (a) the measured harmonics are compared to the Class A limits and in subfigure (b) there are no Class A limits.

5.6 Conclusion

A digital ACMC scheme was proposed to increase the power factor of BCM boost PFC rectifiers. COTC can be used to control BCM boost converters. It has the advantage that has a simple design procedure and a simple implementation. However the valley-switching behaviour and the input capacitor create an zero-crossing distortion in the line current of the BCM boost converter that degrades the power quality. Feedforward control is commonly used to reduce the distortion. However, feedforward control has two main drawbacks. First, the feedforward control is ineffective at reducing the input-capacitor related distortion. Second, it is sensitive to accurate system modelling to accurately estimate the additional on-time needed to remove the zero-crossing distortion. Hence an input-current controller based on ACMC is proposed to reduce the line-current distortion.

An open-loop model was derived that describes how changes in the on-time affects the input current. The model was linearised and converted to the Laplace domain in order to design a suitable current controller. A digital integral controller was chosen as a suitable choice. An adaptive gain was introduced to the current compensator design in order to increase the tracking performance near the zero-crossing region of the line voltage.

Experimental results were demonstrated on a 2-channel 600 W prototype converter. The results demonstrated that the proposed adaptive gain successfully improved the tracking performance of the current controller. As a result, the adaptive gain was successful in increasing the converter's power factor under a wide set of operating conditions. The ACMC scheme was compared to both the COTC scheme and COTC with a FF control scheme. The results demonstrated that ACMC provided the least line-current distortion and the best power factor under all operating conditions.

6 CONCLUSIONS AND FUTURE WORK

This chapter presents a summary of the findings of each chapter presented in this thesis. The work presented in this thesis discussed designing a digital controller for a multi-channel BCM boost converter. The digital controller was responsible for regulating the output voltage, maintaining the correct phase shift between each boost converter channel, and ensuring the line current drawn by the converter had good power quality.

6.1 Chapter Summaries

6.1.1 Chapter 1

Chapter 1 presented the motivation for the work described in this thesis. Modular configurable power supplies are widely used to power medical equipment. The growth in demand for medical power supplies is fueled by the aging of the world's population. These medical power supplies require a front-end PFC rectifier to ensure the line current has high power quality. A multi-channel BCM boost converter is a suitable choice for such a PFC rectifier. The cost and performance of this topology can be reduced by using digital control. Hence, this thesis focuses on the design of a digital controller for a multi-channel BCM PFC rectifier.

The objective of the thesis was introduced, which was to develop suitable digital control schemes to regulate the output voltage, maintain the correct interleaving between boost-converter channels and ensure the converter draws sinusoidal input current with low distortion.

An introduction to power factor and applicable standards was given and the benefits of ensuring good power factor were discussed. The single-channel boost converter was introduced as a PFC rectifier. The converter has three different modes of operation which are DCM, BCM and CCM. In BCM, the converter has low switching loss and zero-current turn on of the boost diode, so that cheap Si diodes can be used without increasing the switching losses. The drawback of the BCM boost converter is that at higher powers the converter suffers significant current stress. Therefore, it is better to operate the converter in CCM, or interleave several channels together.

The control structure of the boost PFC rectifier was briefly described. The BCM boost rectifier is normally regulated using COTC, which is simple and easy to implement. The CCM boost converter requires a more complicated double control-loop structure with a fast inner current loop, and a slow outer voltage loop.

The circuit topology of a multi-channel BCM boost converter was described in more detail. The advantage of the topology is that interleaving several channels together dramatically reduces the input and output current ripples.

A brief discussion was presented on the advantages and growth of digital control in power supplies. The advantages of digital control include improved performance, lower system cost and increased design flexibility.

6.1.2 Chapter 2

Chapter 2 discussed the output voltage regulation of the multi-channel BCM boost converter using COTC. The output voltage of PFC rectifiers contains significant voltage ripple at the 2^{nd} harmonic of the line frequency. This 2^{nd} harmonic ripple can be fed back through the output-voltage regulation loop and cause the input current to become distorted. As a result,

the voltage compensators of PFC rectifiers are typically designed to have a low bandwidth which ensures the 2nd harmonic ripple component is heavily attenuated. The drawback of the low bandwidth is that the output voltage has a poor transient response.

Hence, the goal of this work was to design a voltage compensator which provided both fast output-voltage regulation and low input-current distortion. The open-loop system model was derived based on a theoretical modelling of the system. The open-loop model was linearised in order to design a simple voltage controller with classical linear feedback control.

The voltage compensator was designed to have a fast dynamic response by using an adaptive gain. The adaptive gain worked by increasing the controller's gain at low line voltage in order to ensure the converter had good output voltage regulation for a wide input voltage range. A design method for the voltage compensator using fixed-point math was presented.

An adaptive notch filter was introduced to the voltage compensator design to reduce the input current distortion by attenuating the 2nd ripple on the voltage compensator output. The notch filter sensed the line period and changed its coefficients to adapt to any line frequency from 47 Hz to 63 Hz. A design method for the notch filter with a fixed-point implementation was given.

Experimental results were demonstrated on the 3-channel 2 kW BCM boost PFC rectifier. The results demonstrated the effectiveness of the adaptive voltage-controller gain at improving the output voltage regulation at low line voltages. The converter's power factor was measured with and without the notch filter to demonstrate that the notch filter greatly improved the input power quality.

6.1.3 Chapter 3

A digital closed-loop control scheme for a multi-channel BCM boost converter was proposed. The control scheme used a separate ZCD circuit for each boost converter channel. This ensured that the switch of each channel always operated in BCM with valley switching and reduced switching losses. The ZCD circuit was comprised of an auxiliary winding on the boost choke, a zener diode clamp circuit, and a single microcontroller pin.

A closed-loop feedback system was proposed which sensed the phase shift of each channel and compared it to the switching period of the master channel. This information was used to adjust the turn-off instant of the boost switch by changing the individual on-time of each channel. The proposed feedback scheme could be executed at a fixed sampling rate much lower than the maximum switching frequency of the converter. This allowed the algorithm to be implemented on a low-cost microcontroller. A theoretical analysis was performed to find the gain with the best tracking performance, and the gain for when the system becomes unstable. An adaptive gain was proposed to guarantee the best tracking

performance under all operating conditions.

Experimental results were demonstrated on the 3-channel 1 kW BCM PFC rectifier prototype. The results demonstrated the adaptive gain provided significant improvement. The results also demonstrated that the phase-shift control scheme worked well under a wide range of voltage and power operating conditions. At lower power levels the proposed control scheme disabled the number of boost converter channels that were active. This allowed the converter to increase its light-load power factor and efficiency.

6.1.4 Chapter 4

A simple digital feedforward variable-on-time was proposed to improve the zero-crossing distortion of BCM boost PFC rectifiers. A theoretical analysis of the inductor current waveshape and valley-switching operation of the boost rectifier was carried out. Based on this analysis, an additional on-time was derived that could be added to the voltage compensator output to calculate the switch on-time, while creating no valley-switching distortion in the line current. The proposed algorithm allowed for a very simple design procedure and required no experimental tuning. The algorithm also had a very simple implementation and only required a single LUT to implement.

Experimental results were demonstrated on the 3-channel 1 kW prototype. The results showed that the feedforward algorithm dramatically reduced the zero-crossing distortion, and created a more sinusoidal input current. The converter's power factor was measured over a wide range of input voltages and output powers demonstrating the algorithm provided an improvement in power quality under all operating conditions.

6.1.5 Chapter 5

A digital ACMC scheme was presented for a BCM boost PFC converter. A brief review of how COTC is used to regulate PFC BCM boost was presented, including details of how the line current suffers from a cross-over distortion which degrades the converter's power quality. Similarly, a brief review of how feedforward control can be used to reduce this line-current distortion was presented. The ACMC control scheme was introduced, and a current controller was designed with an adaptive gain to accurately regulate the input current.

Experimental results were given demonstrating the effectiveness of the current controller's adaptive gain. The ACMC control scheme was experimentally compared to COTC and feedforward control, where it was demonstrated that ACMC provides the best improvement in power quality at all line and load conditions.

6.2 Future Work

Possible future work on this project may be divided into the following areas.

6.2.1 Sensorless Control

The BCM boost topology requires a separate ZCD circuit for each channel to ensure BCM operation. Additionally input voltage sensing is required to generate the reference current as part of the ACMC scheme and to perform safety checking functions as part of the COTC scheme. The overall system cost could be reduced if this sensing capability was not required. Suitable digital predictive control algorithms would be developed to operate the boost converter in BCM without the need for ZCD circuits or an input voltage sensor. These algorithms must of course guarantee BCM operation under all operating conditions, and maintain good output voltage tracking and input power quality.

6.2.2 Bridgless Multi-Channel PFC

The topology used in this body of work was a bridged multi-channel BCM boost PFC. This topology is advantageous as it is quite low cost. However, the topology also suffers from significant conduction losses, especially at low line voltage, which degrade the efficiency of the converter. The bridge rectifier is a major contributor to these losses. The topology could be switched to a multi-channel bridgless totem-pole BCM boost converter to reduce the conduction losses and hence increase the switching frequency. The topology also enables full zero-voltage switching at any input voltage, as opposed to the bridged topology which can only achieve zero-voltage switching at low input voltages. The topology could be implemented with SiC or GaN transistors to reduce the turn-off switching losses, and thus enable higher switching frequencies, a smaller boost choke, and a smaller EMI filter.

This topology does of course come at the cost of a more expensive implementation per channel as each channel now requires more complex ZCD circuits, 2 MOSFETs and a high-side gate driver per channel, instead of a simple ZCD circuit, 1 MOSFET with a low-side driver and a cheap diode. However, given that the cooling requirements, EMI and inductor size could all be reduced, the overall system cost may also be reduced.

6.2.3 Switching Frequency Limiting

A limitation of this body of work is that the switching frequency of the converter was allowed to vary from 80 kHz to 700 kHz. Although this variation is beneficial for the conducted EMI of the converter, it also causes some design issues. First, the boost inductor design is more challenging, as core losses must not be excessive over the entire operating range. Second, the gate drives can overheat at low power and high switching frequencies. The switching frequency could be limited with adequate digital control algorithms that preform valley

skipping, to ensure that the converter's soft switching is not lost. Valley skipping occurs when the converter operates in DCM, but the boost switch is only turned on at a valley point of the drain-source voltage to maintain the soft-switching behaviour. The disadvantage of operating the converter in DCM with valley skipping is that there is increased current stress compared to BCM operation. However at low power this is not a big issue, as current stress is low. It is also possible that valley skipping could increase the efficiency at low power, as the lower switching frequency will significantly reduce the turn-off switching losses which dominate at low power, while the increase in conduction loss at lower power would be small.

REFERENCES

[1] https://population.un.org/wpp/Graphs/Probabilistic/POP/60plus/. Accessed on 24/09/2018.

[2] https://www.excelsys.com/industry-solutions/medical/. Accessed on 24/09/2018.

[3] http://www.vox-power.com/medical-power-supplies/. Accessed on 24/09/2018.

[4] https://www.meanwellaustralia.com.au/products/nmp650. Accessed on 24/09/2018.

[5] http://www.us.tdk-lambda.com/lp/products/qm-series.htm. Accessed on 24/09/2018.

[6] http://www.deltapsu.com/products/configurable-power-supply?serie=meg&nav=2. Accessed on 24/09/2018.

[7] https://www.artesyn.com/power/solutions/healthcare/medical. Accessed on 24/09/2018.

[8] W. Lutz, W. Sanderson, and S. Scherbov, "The coming acceleration of global population ageing," *Nature*, vol. 451, pp. 716–719, Feb. 2008.

[9] J. G. Hayes and A. G. Goodarzi, *Electric Powertrain: Energy Systems, Power Electronics and Drives for Hybrid, Electric and Fuel Cell Vehicles*. Wiley & Sons, 2018.

[10] O. Garcia, J. A. Cobos, R. Prieto, P. Alou *et al.*, "Single phase power factor correction: a survey," *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 749–755, May. 2003.

[11] "Harmonic current emissions: Guidelines to the standard EN 61000-3-2," EPSMA, 2010. http://www.epsma.org/PFCver100406_b.pdf. Accessed on 08/10/2018.

[12] W. Choi and S. Young, "Effectiveness of a SiC schottky diode for super-junction MOSFETs on continuous conduction mode PFC," in *SPEEDAM*, pp. 562–567, Jun. 2010.

[13] G. Spiazzi, S. Buso, M. Citron, M. Corradin *et al.*, "Performance evaluation of a schottky SiC power diode in a boost PFC application," *IEEE Transactions on Power Electronics*, vol. 18, no. 6, pp. 1249–1253, Nov. 2003.

[14] J. . Lai and D. Chen, "Design consideration for power factor correction boost converter operating at the boundary of continuous conduction mode and discontinuous conduction mode," in *IEEE Applied Power Electronics Conference and Exposition,*, pp. 267–273, Mar. 1993.

[15] C. Adragna, "Design-oriented analysis of ECOT-controlled DCM/CCM boundary boost PFC pre-regulators," in *AEIT International Annual Conference*, pp. 1–6, Sep. 2017.

[16] A. Bianco, C. Adragna, and G. Scappatura, "Enhanced constant-on-time control for DCM/CCM boundary boost PFC pre-regulators: Implementation and performance evaluation," in *IEEE Applied Power Electronics Conference and Exposition*, pp. 69–75, Mar. 2014.

[17] J. Kim and G. Moon, "Minimizing effect of input filter capacitor in a digital boundary conduction mode power factor corrector based on time-domain analysis," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3827–3836, May. 2016.

[18] Y. Lai, C. Yeh, and K. Ho, "A family of predictive digital-controlled PFC under boundary current mode control," *IEEE Transactions on Industrial Informatics*, vol. 8, no. 3, pp. 448–458, Aug. 2012.

[19] J. Shin, G.-S. Seo, B. Cho, and K.-C. Lee, "Modeling and implementation of digital control for critical conduction mode power factor correction rectifier," in *IEEE 13th Workshop on Control and Modeling for Power Electronics*, pp. 1–8, Jun. 2012.

[20] S. Yang, S.-J. Chen, and C.-M. Huang, "Small-signal modeling and controller design of BCM boost PFC converters," in *IEEE Conference on Industrial Electronics and Applications*, pp. 1096–1101, Jul. 2012.

[21] S. Yang, S. Chen, and C. Huang, "Analysis, modeling and controller design of CRM PFC boost ac/dc converter with constant on-time control IC FAN7530," in *IEEE Conference on Industrial Electronics and Applications*, pp. 354–359, Jun. 2014.

[22] L. Huber, B. T. Irving, and M. M. Jovanovic, "Line current distortions of DCM/CCM boundary boost PFC converter," in *IEEE Applied Power Electronics Conference and Exposition*, pp. 702–708, Feb. 2008.

[23] J. W. Kim, S. M. Choi, and K. T. Kim, "Variable on-time control of the critical conduction mode boost power factor correction converter to improve zero-crossing distortion," in *International Conference on Power Electronics and Drives Systems*, vol. 2, pp. 1542–1546, Nov. 2005.

[24] K. Yao, Y. Wang, J. Guo, and K. Chen, "Critical conduction mode boost PFC converter with fixed switching frequency control," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 6845–6857, Aug. 2018.

[25] C.-Y. Lim, J. Kim, Y. Jeong, D.-K. Kim *et al.*, "A high efficiency critical mode boost PFC using a variable inductor," in *IEEE International Power Electronics and Motion Control Conference*, pp. 2792–2797, May. 2016.

[26] C. Lim, Y. Jeong, and G. Moon, "Phase leading input capacitor compensation using variable inductor with high efficiency in a CRM boost PFC," in *IEEE International Future Energy Electronics Conference and ECCE Asia*, pp. 852–856, Jun. 2017.

[27] B. Choi, S.-S. Hong, and H. Park, "Modeling and small-signal analysis of controlled on-time boost power-factor-correction circuit," *IEEE Transactions on Industrial Electronics*, vol. 48, no. 1, pp. 136–142, Feb. 2001.

[28] Y. Li, Y. Yang, Z. Zhu, and W. Qiang, "Zero-crossing distortion analysis in one cycle controlled boost PFC for low THD," in *IEEE International Conference on ASIC*, pp. 661–664, Oct. 2011.

[29] J. Tsai, C. Chen, Y. Chen, C. Ni *et al.*, "Perturbation on-time (POT) control and inhibit time control (ITC) in suppression of THD of power factor correction (PFC) design," in *IEEE Custom Integrated Circuits Conference*, pp. 1–4, Sep. 2011.

[30] J. Tsai, C. Chen, Y. Chen, C. Ni *et al.*, "Perturbation on-time (POT) technique in power factor correction (PFC) controller for low total harmonic distortion and high power factor," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 199–212, Jan. 2013.

[31] Z. Guo, X. Ren, H. Gui, Y. Wu *et al.*, "A universal variable on-time compensation to improve thd of high-frequency crm boost pfc converter," in *IEEE Energy Conversion Congress and Exposition*, pp. 1–6, Sep. 2016.

[32] Z. Guo, X. Ren, Y. Wu, Z. Zhang *et al.*, "A novel simplified variable on-time method for CRM boost PFC converter," in *IEEE Applied Power Electronics Conference and Exposition*, pp. 1778–1784, Mar. 2017.

[33] J. Kim, H. Youn, and G. Moon, "A digitally controlled critical mode boost power factor corrector with optimized additional on time and reduced circulating losses," *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3447–3456, Jun. 2015.

[34] C. Zhao, J. Zhang, and X. Wu, "Phase leading input current compensation for CRM boost PFC converter," in *IEEE Energy Conversion Congress and Exposition*, pp. 1–5, Sep. 2016.

[35] J. Kim, J. Moon, H. Youn, Y. Jeong *et al.*, "Phase leading input current compensation in digitally controlled critical mode boost PFC," in *IEEE International Conference on Power Electronics and ECCE Asia*, pp. 2688–2695, Jun. 2015.

[36] Y. Chen and Y. Chen, "Line current distortion compensation for DCM/CRM boost PFC converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 2026–2038, Mar. 2016.

[37] Q. Ji, X. Ruan, and Z. Ye, "The worst conducted EMI spectrum of critical conduction mode boost PFC converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1230–1241, Mar. 2015.

[38] F. Yang, X. Ruan, Q. Ji, and Z. Ye, "Input differential-mode EMI of CRM boost PFC converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 3, pp. 1177–1188, Mar. 2013.

[39] B. Addreycak, "Controlled on-time , zero current switched power factor correction technique," *Unitrode Power Supply Seminar*, vol. 3, pp. 1–11, 1991.

[40] S. Mao, R. Ramabhadran, J. Popovic, and J. A. Ferreira, "Investigation of CCM boost PFC converter efficiency improvement with 600V wide band-gap power semiconductor devices," in *IEEE Energy Conversion Congress and Exposition*, pp. 388–395, Sep. 2015.

[41] K. D. Gusseme, D. M. V. de Sype, A. P. M. V. den Bossche, and J. A. Melkebeek, "Digitally controlled boost power-factor-correction converters operating in both continuous and discontinuous conduction mode," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 88–97, Feb. 2005.

[42] K. D. Gusseme, D. M. V. de Sype, A. P. M. V. den Bossche, and J. A. Melkebeek, "Input-current distortion of CCM boost PFC converters operated in DCM," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 2, pp. 858–865, Apr. 2007.

[43] L. Roggia, F. Beltrame, J. E. Baggio, and J. R. Pinheiro, "Digital control system applied to a PFC boost converter operating in mixed conduction mode," in *Brazilian Power Electronics Conference*, pp. 698–704, Sep. 2009.

[44] S. M. O'Driscoll and D. A. Grant, "Combining peak current mode control with average current mode control using digitally assisted analog," in *IEEE Applied Power Electronics Conference and Exposition*, pp. 76–88, 2014.

[45] I. Zverev, "Switching frequency related trade off's in a hard switching CCM PFC boost converter," in *IEEE Applied Power Electronics Conference and Exposition*, vol. 2, pp. 671–676, Feb. 2003.

[46] S. F. Lim and A. M. Khambadkone, "A simple digital DCM control scheme for boost PFC operating in both CCM and DCM," in *IEEE Energy Conversion Congress and Exposition*, pp. 1218–1225, Sep. 2010.

[47] M. A. Ebrahimzadeh and A. R. Rahmati, "Adaptive and fast-response controller for boost PFC converter with wide range of operating conditions," in *IEEE Power Electronic Drive Systems Technologies Conference*, pp. 157–162, Feb. 2010.

[48] H. S. Athab and P. K. S. Khan, "A simple effective duty cycle controller for high power factor boost rectifier," in *IEEE International Conference on Power Electronics and Drive Systems*, pp. 664–668, Nov. 2007.

[49] C. Spiazzi, P. Mattavelli, and L. Rossetto, "Power factor preregulators with improved dynamic response," *IEEE Transactions on Power Electronics*, vol. 12, no. 2, pp. 343–349, Mar. 1997.

[50] J. Kim, H. Choi, and C. Won, "New modulated carrier controlled PFC boost converter," *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 4772–4782, Jun. 2018.

[51] S. Buso, P. Mattavelli, L. Rossetto, and G. Spiazzi, "Simple digital control improving dynamic performance of power factor preregulators," *IEEE Transactions on Power Electronics*, vol. 13, no. 5, pp. 814–823, Sep. 1998.

[52] A. Prodic, J. Chen, D. Maksimovic, and R. W. Erickson, "Self-tuning digitally controlled low-harmonic rectifier having fast dynamic response," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 420–428, Jan. 2003.

[53] L. T. Jakobsen, N. Nielsen, C. Wolf, and M. A. E. Andersen, "Hybrid control method for a single phase PFC using a low cost microcontroller," in *IEEE Applied Power Electronics Conference and Exposition*, vol. 3, pp. 1710–1715 Vol. 3, Mar. 2005.

[54] B. Mather, B. Ramachandran, and D. Maksimovic, "A digital PFC controller without input voltage sensing," in *IEEE Applied Power Electronics Conference and Exposition*, pp. 198–204, Feb. 2007.

[55] A. A. de Melo Bento and E. R. C. da Silva, "Hybrid one-cycle controller for boost PFC rectifier," *IEEE Transactions on Industry Applications*, vol. 45, no. 1, pp. 268–277, Jan. 2009.

[56] L.Dixon, "Average current mode control of switching power supplies," in *Unitrode Power Supply Design Seminar*, vol. 5, pp. 1–14, 1998.

[57] W. Tang, F. C. Lee, and R. B. Ridley, "Small-signal modeling of average current-mode control," in *IEEE Applied Power Electronics Conference and Exposition*, pp. 747–755, Feb. 1992.

[58] J. P. Gegner and C. Q. Lee, "Linear peak current mode control: a simple active power factor correction control technique for continuous conduction mode," in *IEEE Power Electronics Specialists Conference*, vol. 1, pp. 196–202, Jun. 1996.

[59] J. Chen, A. Prodic, R. W. Erickson, and D. Maksimovic, "Predictive digital current programmed control," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 411–419, Jan. 2003.

[60] S. Bibian and H. Jin, "Digital control with improved performance for boost power factor correction circuits," in *IEEE Applied Power Electronics Conference and Exposition*, vol. 1, pp. 137–143 vol.1, Mar. 2001.

[61] Y. Chen, D. He, and R. M. Nelms, "Control of a single-phase PFC preregultaor using an 8-bit microcontroller," in *IEEE Applied Power Electronics Conference and Exposition*, pp. 1454–1460, Feb. 2007.

[62] A. Marcos-Pastor, E. Vidal-Idiarte, A. Cid-Pastor, and L. Martinez-Salamero, "Interleaved digital power factor correction based on the sliding-mode approach," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4641–4653, Jun. 2016.

[63] D. Maksimovic, Y. Jang, and R. W. Erickson, "Nonlinear-carrier control for high-power-factor boost rectifiers," *IEEE Transactions on Power Electronics*, vol. 11, no. 4, pp. 578–584, Jul. 1996.

[64] D. M. V. de Sype, K. D. Gusseme, A. P. M. V. den Bossche, and J. A. Melkebeek, "Duty-ratio feedforward for digitally controlled boost pfc converters," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 1, pp. 108–115, Feb. 2005.

[65] S. Choudhury and J. P. Noon, "A DSP based digitally controlled interleaved PFC converter," in *IEEE Applied Power Electronics Conference and Exposition*, vol. 1, pp. 648–654, Mar. 2005.

[66] Y. Roh, Y. Moon, J. Park, and C. Yoo, "A two-phase interleaved power factor correction boost converter with a variation-tolerant phase shifting technique," *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 1032–1040, Feb. 2014.

[67] J. Shin, G. Seo, B. Cho, and K. Lee, "Digitally controlled open-loop master-slave interleaved boost PFC rectifier," in *IEEE Applied Power Electronics Conference and Exposition*, pp. 304–309, Feb. 2012.

[68] J. Jang, S. K. Pidaparthy, S. Lee, and B. Choi, "Performance of an interleaved boundary conduction mode boost PFC converter with wide band-gap switching devices," in *IEEE International Future Energy Electronics Conference*, pp. 1–6, Nov. 2015.

[69] C. Adragna, L. Huber, B. T. Irving, and M. M. Jovanovic, "Analysis and performance evaluation of interleaved DCM/CCM boundary boost PFC converters around zero-crossing of line voltage," in *IEEE Applied Power Electronics Conference and Exposition*, pp. 1151–1157, Feb. 2009.

[70] H. Choi and L. Balogh, "A cross-coupled master–slave interleaving method for boundary conduction mode (BCM) PFC converters," *IEEE Transactions on Power Electronics*, vol. 27, no. 10, pp. 4202–4211, Oct. 2012.

[71] L. Huber, B. T. Irving, C. Adragna, and M. M. Jovanovic, "Implementation of open-loop control for interleaved DCM/CCM boundary boost PFC converters," in *IEEE Applied Power Electronics Conference and Exposition*, pp. 1010–1016, Feb. 2008.

[72] L. Huber, B. T. Irving, and M. M. Jovanovic, "Review and stability analysis of PLL-based interleaving control of DCM/CCM boundary boost PFC converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 8, pp. 1992–1999, Aug. 2009.

[73] L. Huber, B. T. Irving, and M. M. Jovanovic, "Closed-loop control methods for interleaved DCM/CCM boundary boost PFC converters," in *IEEE Applied Power Electronics Conference and Exposition*, pp. 991–997, Feb. 2009.

[74] X. Xu and A. Q. Huang, "A novel closed loop interleaving strategy of multiphase critical mode boost PFC converters," in *IEEE Applied Power Electronics Conference and Exposition*, pp. 1033–1038, Feb. 2008.

[75] X. Xu, W. Liu, and A. Q. Huang, "Two-phase interleaved critical mode PFC boost converter with closed loop interleaving strategy," *IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 3003–3013, Dec. 2009.

[76] T. Grote, H. Figge, N. Fröhleke, J. Böcker *et al.*, "Digital control strategy for multiphase interleaved boundary mode and DCM boost PFC converters," in *IEEE Energy Conversion Congress and Exposition*, pp. 3186–3192, Sep. 2011.

[77] H. Chen, S. Lee, Y. Chen, Y. Chen *et al.*, "A stepping on-time adjustment method for interleaving three-channel critical mode boost PFC converter," in *IEEE Energy Conversion Congress and Exposition*, pp. 749–754, Sep. 2013.

[78] Y. Chen, H. Chen, Y. Chen, and K. H. Liu, "A stepping on-time adjustment method for interleaved multichannel PFC converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1170–1176, Mar. 2015.

[79] http://www.onsemi.com/PowerSolutions/product.do?id=FAN9611. Accessed on 06/10/2018.

[80] http://www.ti.com/product/UCC28063. Accessed on 06/10/2018.

[81] http://www.onsemi.com/PowerSolutions/product.do?id=NCP1631. Accessed on 06/10/2018.

[82] Y. Liu, E. Meyer, and X. Liu, "Recent developments in digital control strategies for DC/DC switching power converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2567–2577, Nov. 2009.

[83] Maksimovic, Zane, and Erickson, "Impact of digital control in power electronics," in *IEEE International Symposium on Power Semiconductor Devices and ICs*, pp. 13–22, May. 2004.

[84] R. T. Ryan, J. G. Hayes, R. Morrison, and D. Hogan, "Digital control of an interleaved BCM boost PFC converter with fast transient response at low input voltage," in *IEEE Energy Conversion Congress and Exposition*, pp. 257–264, Oct. 2017.

[85] S. Khare, "Features, value and benefits of digital control for power supplies," Microchip Technology, 2010. http://ww1.microchip.com/downloads/en/DeviceDoc/70631A.pdf. Accessed on 08/10/2018.

[86] H. Nene, C. Jiang, and S. Choudhury, "Digital controller with integrated valley switching control for light load efficiency and THD improvements in PFC converter," in *IEEE Applied Power Electronics Conference and Exposition*, pp. 1785–1788, Mar. 2017.

[87] S. Wall and R. Jackson, "Fast controller design for practical power-factor correction systems," in *IEEE Industrial Electronics*, pp. 1027–1032 vol.2, Nov. 1993.

[88] S. Wall and R. Jackson, "Fast controller design for single-phase power-factor correction systems," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 5, pp. 654–660, Oct. 1997.

[89] M. O. Eissa, S. B. Leeb, G. C. Verghese, and A. M. Stankovic, "Fast controller for a unity-power-factor PWM rectifier," *IEEE Transactions on Power Electronics*, vol. 11, no. 1, pp. 1–6, Jan. 1996.

[90] A. Pandey, B. Singh, and D. P. Kothari, "A simple fast voltage controller for single-phase PFC converters," in *IEEE Industrial Electronics Society Conference*, vol. 2, pp. 1235–1237, Nov. 2002.

[91] Z. Yang and C. S. Paresh, "A novel technique to achieve unity power factor and fact transient response in ac-to-dc converters," *IEEE Transactions on Power Electronics*, vol. 16, no. 6, pp. 764–775, Nov. 2001.

[92] A. H. Mitwalli, S. B. Leeb, G. C. Verghese, and V. J. Thottuvelil, "An adaptive digital controller for a unity power factor converter," *IEEE Transactions on Power Electronics*, vol. 11, no. 2, pp. 374–382, Mar. 1996.

[93] D. G. Lamar, A. Fernandez, M. Arias, M. Rodriguez *et al.*, "A unity power factor correction preregulator with fast dynamic response based on a low-cost microcontroller," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 635–642, Mar. 2008.

[94] A. Prodic, J. Chen, R. W. Erickson, and D. Maksimovic, "Digitally controlled low-harmonic rectifier having fast dynamic responses," in *IEEE Applied Power Electronics Conference and Exposition*, vol. 1, pp. 476–482, Mar. 2002.

[95] J. B. Williams, "Design of feedback loop in unity power factor ac to dc converter," in *IEEE Power Electronics Specialists Conference*, pp. 959–967 vol.2, Jun. 1989.

[96] G. Spiazzi, P. Mattavelli, and L. Rossetto, "Methods to improve dynamic response of power factor preregulators: An overview," in *IEEE European Power Electronics Conference*, vol. 3, pp. 754–759, Sep. 1995.

[97] C. P. Henze and N. Mohan, "A digitally controlled ac to dc power conditioner that draws sinusoidal input current," in *IEEE Power Electronics Specialists Conference*, pp. 531–540, Jun. 1986.

[98] J. Rajagopalan, J. G. Cho, B. H. Cho, and F. C. Lee, "High performance control of single-phase power factor correction circuits using a discrete time domain control method," in *IEEE Applied Power Electronics Conference and Exposition*, vol. 2, pp. 647–653 vol.2, Mar. 1995.

[99] T. T. Vu and G. Young, "Digital adaptive control approach to dynamic response improvement for compact PFC rectifiers," in *International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pp. 1–8, May. 2016.

[100] A. Prodic, D. Maksimovic, and R. W. Erickson, "Dead-zone digital controllers for improved dynamic response of low harmonic rectifiers," *IEEE Transactions on Power Electronics*, vol. 21, no. 1, pp. 173–181, Jan. 2006.

[101] M. Rathi, N. Bhiwapurkar, and N. Mohan, "Dual voltage controller based power factor correction circuit for faster dynamics and zero steady state error," in *IEEE Industrial Electronics Society Conference*, vol. 1, pp. 238–242, Nov. 2003.

[102] P. Das, M. Pahlevaninezhad, J. Drobnik, G. Moschopoulos *et al.*, "A nonlinear controller based on a discrete energy function for an ac/dc boost PFC converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 12, pp. 5458–5476, Dec. 2013.

[103] S. Yu and L. Liu, "Observer-based compensation for improving dynamic response of a boost PFC rectifier," in *IEEE International Symposium on Industrial Electronics*, pp. 801–804, Jun. 2017.

[104] "C2000 delfino 32-bit microcontrollers," Texas Instruments, 2018. http://www.ti.com/microcontrollers/c2000-real-time-control-mcus/delfino-premium-performance/overview.html. Accessed on 01/12/2018.

[105] "C2000 piccolo 32-bit microcontrollers," Texas Instruments, 2018. http://www.ti.com/microcontrollers/c2000-real-time-control-mcus/piccolo-entry-performance/overview.html. Accessed on 01/12/2018.

[106] "Xmc series 32-bit microcontrollers," Infineon, 2018. https://www.infineon.com/cms/en/product/microcontroller/32-bit-industrial-microcontroller-based-on-arm-cortex-m/. Accessed on 01/12/2018.

[107] "Elliptic filter design," Matlab, 2018. https://uk.mathworks.com/help/signal/ref/ellip.html. Accessed on 28/11/2018.

[108] A. Antoniou, *Digital Signal Processing: Signals, Systems and Filters*. McGraw-Hill, 2006.

[109] "Fan3224 gate drive ic," ON Semiconductor, 2018. https://www.onsemi.com/PowerSolutions/product.do?id=FAN3224TU_F085. Accessed on 18/12/2018.

[110] S. Tang, D. Chen, C. Huang, C. Liu *et al.*, "A new on-time adjustment scheme for the reduction of input current distortion of critical-mode power factor correction boost converters," in *The 2010 International Power Electronics Conference - ECCE ASIA -*, pp. 1717–1724, Jun. 2010.

[111] A. Kar and M. Sengupta, "Design, analysis, fabrication and testing of a 3 kW power factor correction boost rectifier," in *IEEE International Conference Power Electronics, Drives and Energy Systems (PEDES)*, pp. 1–6, 2016.

[112] J. Moldaschl, J. Broulím, and L. Paločko, "Boost power factor correction topology with average current control," in *IEEE Applied Power Electronics Conference and Exposition*, pp. 213–216, 2014.

APPENDIX A

SIMULINK SIMULATION MODEL

The following Appendix presents a full description of the Simulink model used to verify the design of the voltage compensator. All circuit components were taken from the Simscape specialized-technology power-electronics simulation blocks. The simulation was ran at a fixed time step of 10.41 ns, corresponding to a simulation sampling frequency of 96 MHz. The full simulation model is subsequently shown in Figure A.2, Figure A.3, Figure A.4, Figure A.5 and Figure A.7. The color of the block in each figure corresponds to the rate of execution of that block. Figure A.1 gives a description of the execution rate each color corresponds to.

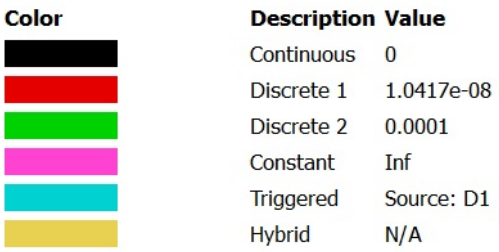


Figure A.1. The color code that defines the execution rate of each Simulink block

A.1 Power Stage

Figure A.2 shows the Simulink model of the power stage of the single-channel BCM boost converter. The model includes a differential-mode EMI filter, a bridge rectifier, a single-channel BCM boost converter and a current-source load. The drain-source capacitance of

the MOSFET is accounted for by approximating it as a linear capacitor. The zero-current-detection (ZCD) winding is accounted for by measuring the voltage across the boost inductor

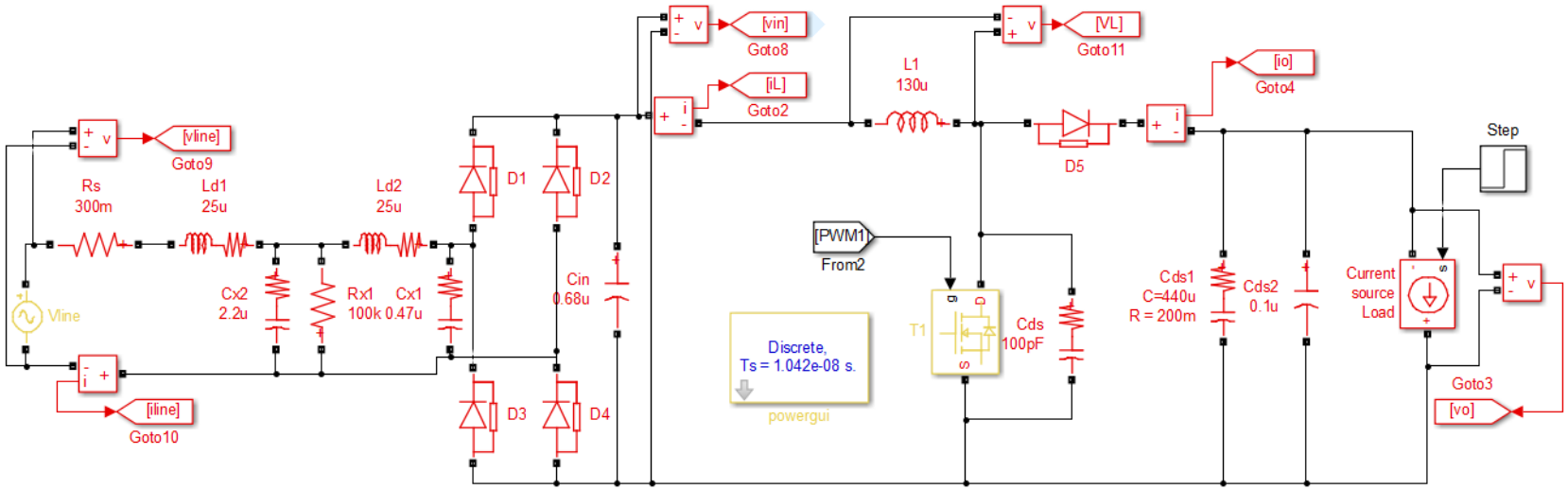


Figure A.2. Simulink power-stage simulation model.

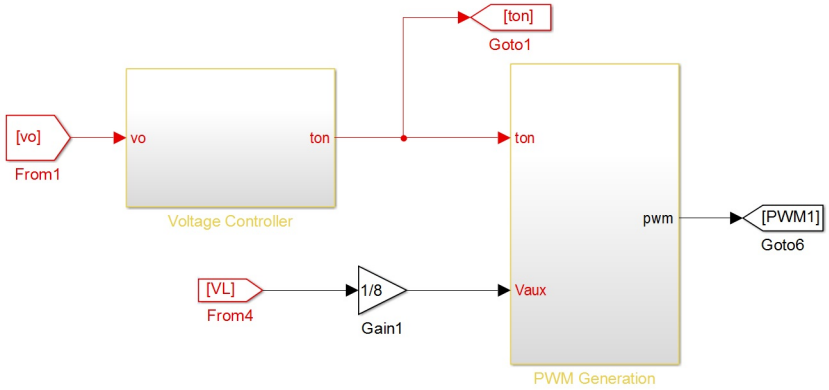


Figure A.3. Simulink controller simulation model.

using a voltage-measurment block, the output of this output-measurment block is used as the input to the ZCD-circuit model.

Figure A.3 shows the Simulink model of the voltage controller. This model is divided into two different subsystems, one for simulating the voltage compensator and the other for simulating the PWM generation including the ZCD circuit.

A.2 Voltage Compensator

The voltage compensator subsystem model is shown in Figure A.4. The input to the subsystem is the measured output voltage, and the output is the converter's on-time in units of seconds. The model takes into account the output voltage adc-sensor gain H_v and scales the output of the voltage compensator by $\frac{1}{f_{pwm}}$, to convert from units of ticks to seconds. The controller coefficients b_{v0}, b_{v1}, b_{v2}, a_{v1} and a_{v2} were calculated per (2.30), (2.31), (2.32), (2.33) and (2.34) respectively in a separate Matlab *.m* file. The estimated steady-state on-time in units of ticks was added to the output of the voltage compensator in the model, this ensures that the simulation begins from steady-state operation.

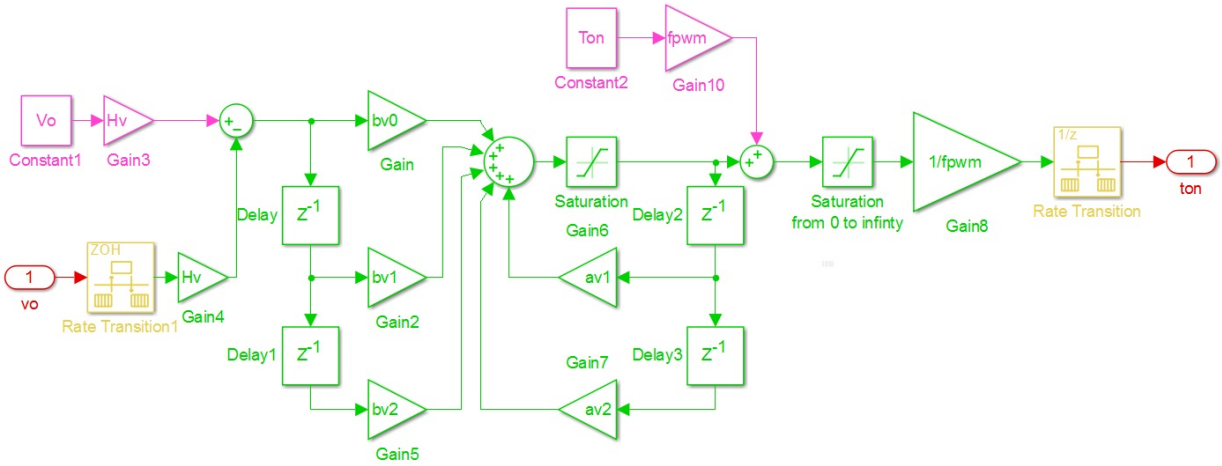


Figure A.4. Voltage compensator Simulink model.

A.3 PWM Generation

The PWM generation subsystem model is given in Figure A.5. The system has two inputs, the first is the on-time calculated by the voltage compensator. The second is the voltage denoted V_{aux}, this voltage represents the voltage at the output of the boost inductor auxiliary winding used as part of the ZCD-circuit. This voltage is calculated by scaling the measured boost-inductor voltage by a factor of $\frac{1}{8}$, where the ratio of $\frac{1}{8}$ corresponds to the turns ratio of the number of turns on the boost inductor winding, to the number of turns on the auxiliary ZCD sense winding. The voltage V_{aux} is input to another subsystem that model's the ZCD circuit, and creates a pulse that sets the S-R flip-flop and triggers the boost switch's turn-on instant.

The turn-off instant is generated by comparing the on-time to a timer output. The timer is created by using an integrator with a unity input that is reset by the rising edge of the PWM output. The model also incorporates a maximum switching period, after which period the boost switch is also triggered on.This acts as a reset timer for when no ZCD signal is present.

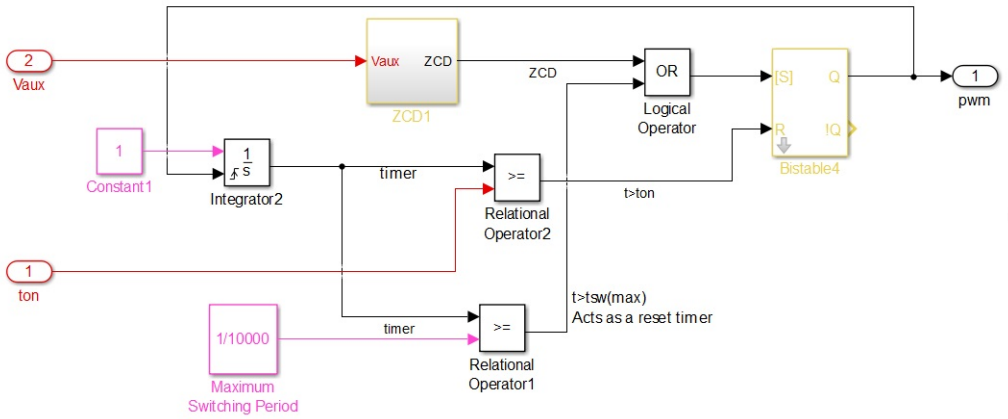


Figure A.5. PWM generation Simulnik model.

A.4 ZCD Circuit

Figure A.6 shows the circuit diagram for the ZCD circuit.The operation of this circuit is covered in more detail in Section 3.2.1. The circuit is used to generate a square wave voltage denoted v_{zcd}, that toggles from 0 to 5 V, with a rising edge and falling edge that are synchronised to the falling edge and rising edge of the inductor voltage, respectively. Since the rising edge of the inductor voltage corresponds to the inductor current's zero-current instance, the falling edge of the voltage v_{zcd} corresponds to the inductor current's zero-current instance. Therefore, in a real-life hardware implementation, the voltage v_{zcd} is fed in to a digital microcontroller pin, and it's falling edge is used to trigger the boost switch's turn-on instant.

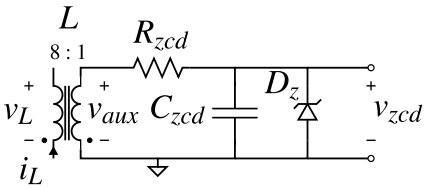


Figure A.6. Zero-current-detection circuit.

The circuit is simulated in Simulink using integrator and gain blocks that behave with the same circuit elements to those of Figure A.6. The Simulink model for the ZCD circuit is shown in Figure A.7. The voltage v_{aux} is calculated assuming perfect magnetic coupling between the boost inductor winding and auxiliary winding, so that

$$v_{aux} = -\frac{1}{8}v_L$$

If the zener diode D_z is not conducting the circuit can be mathematically modelled by

$$\frac{d}{dt}v_{zcd} = \frac{1}{R_{zcd}C_{zcd}}(v_{aux} - v_{zcd})$$

This is the same mathematical model implemented by the subtract, gain and integrator block shown in Figure A.7. The effects of the zener diode are taken into account by limiting the output of the integrator, which is v_{zcd}, to between the zener-diode zener voltage, and the negative value of the zener-diode forward voltage drop. Hence the output of the integrator, which corresponds to the voltage v_{zcd}, is limited to from -0.4 V to 5 V.

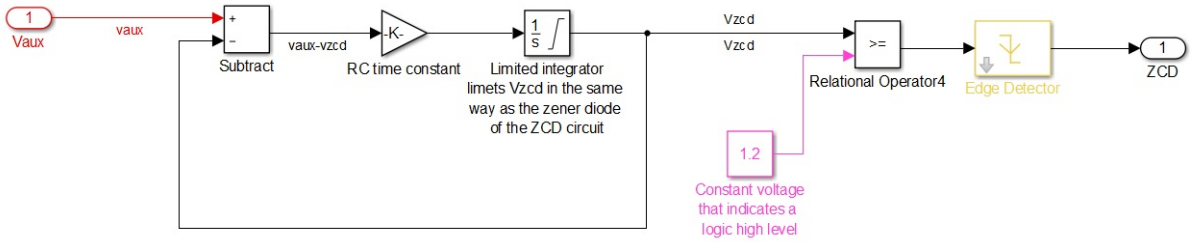


Figure A.7. ZCD circuit simulation model.

The voltage v_{zcd} is compared to a constant voltage of 1.4 V, to converter it to a bit-logic signal that toggles between 1 and 0. The voltage 1.4 V corresponds to the voltage on the microcontroller's digital pin, above which the signal is given a value of 1 bit. The signal is then passed through a falling-edge-detector block that generates the *ZCD* trigger signal that turns on the boost switch.

APPENDIX B

CONTROLLER IMPLEMENTATION WITH FIXED-POINT MATH

B.1 Voltage Compensator Design using Fixed-Point Math

The voltage-compensator fixed-point controller coefficients are calculated in this Appendix.

A block diagram of the voltage compensator implemented using fixed-point math is given in Figure B.1.

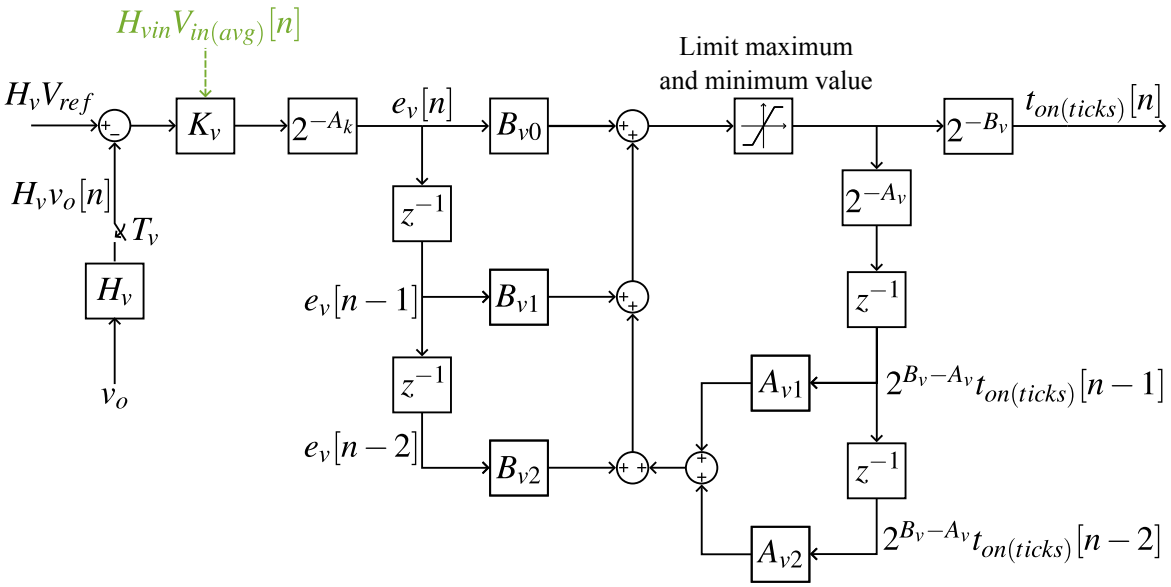


Figure B.1. Voltage compensator block diagram for a fixed-point implementation.

The terms A_k, A_v and B_v must be defined, in order to calaculate the fixed-point controller coefficients and to complete the voltage compensator design. The term A_k is set as high as possible to reduce the rounding error associated with the right-shift bit operation 2^{-A_k}, as shown in Figure B.1, and also high enough to minimise the quantization error associated with converting the different values of gain k_v to the gain K_v. The term A_k must not be set excessively high to cause positive integer overflow at the output of the K_v gain block, as shown in Figure B.1. The following inequality must be satisfied to prevent positive integer overflow at the output of the K_v gain block.

$$\max\left\langle (H_vV_{ref} - H_vv_o[n])K_v \right\rangle < 2^{31} - 1 \tag{B.1}$$

The output voltage is sensed using an ADC with a 12-bit resolution, and so the maximum value of the term $H_v v_o[n]$ is equal to $2^{12}-1=4095$, with a minimum value of zero. The reference voltage is set to a constant 400 V, hence the term $H_v V_{ref}$ has a constant value of 3244. Substituting this information into (B.1), the inequality can be simplified as follows:

$$(3244)2^{A_k} max\langle k_v \rangle < 2^{31}-1$$

From Table 2.3 the maximum value of the coefficient k_v is 5.71. Therefore

$$(3244)2^{A_k}(5.71) < 2^{31}-1$$

$$(3244)2^{A_k}(5.71) < \frac{2^{31}-1}{(3244)(5.71)}$$

$$A_k < \log_2\left(\frac{2^{31}-1}{(3244)(5.71)}\right)$$

$$A_k < 16.8$$

The following similar inequality can be written to describe the condition needed to prevent negative integer overflow at the output of the K_v gain block.

$$\min\langle (H_v V_{ref} - H_v v_o[n])K_v \rangle > -2^{31} \tag{B.2}$$

This inequality can be simplified and solved as follows

$$(3244-4095)2^{A_k}(5.71) > -2^{31}$$

$$2^{A_k} < \frac{2^{31}}{(4095-3244)((5.71))}$$

$$A_k < \log_2\left(\frac{2^{31}}{(4095-3244)(5.71)}\right)$$

$$A_k < 18.75 \qquad \therefore \qquad A_k = 16$$

Hence, to prevent both positive and negative integer overflow, the term A_k is set to $A_k = 16$.

The maximum value of B_v for which positive-integer overflow can not occur, is calculated by summing the maximum output of each filter-coefficient-gain block shown in Figure 2.17, and ensuring the result is less than $2^{31}-1$. This results in the inequality obtained in (B.3).

$$\begin{aligned}\max\langle B_{v0}k_v(H_v v_{ref} - H_v v_o[n])\rangle + \max\langle B_{v1}k_v(H_v v_{ref} - H_v v_o[n-1])\rangle + ... \\ \max\langle B_{v2}k_v(H_v v_{ref} - H_v v_o[n-2])\rangle + \max\langle 2^{B_v} a_{v1} t_{on(ticks)[n]}\rangle + ... \\ \max\langle 2^{B_v} a_{v2} t_{on(ticks)[n-1]}\rangle < 2^{31}-1\end{aligned} \tag{B.3}$$

The converter's maximum on-time must be known to solve this inequality. The steady-state on-time of the converter can be calculated using (2.10). The maximum steady-state on-time, denoted $\max\langle T_{on}\rangle$, occurs when the line voltage is at its minimum and the output power is at its maximum. Hence, the maximum steady-state on-time can be calculated by

$$\max\langle T_{on}\rangle = \max\left\langle \frac{2L}{N}\frac{1}{V_{in(rms)}^2}\frac{P_o}{\eta}\right\rangle = \frac{2(0.130\,\text{mH})}{3}\frac{1}{(85\,\text{V})^2}\frac{1000\,\text{W}}{0.96} = 0.0125\,\text{ms} \quad \text{(B.4)}$$

Assuming the instantaneous on-time t_{on} can overshoot to twice the steady-state on-time T_{on} during load disturbances, the maximum value of the instantaneous on-time in ticks $t_{on(ticks)}$ can be calculated as follows

$$\max\langle t_{on(ticks)}[n]\rangle = f_{pwm}\max\langle t_{on}[n]\rangle = 2f_{pwm}\max\langle T_{on}\rangle = (25\,)(96\,\text{MHz}) = 2500\,\text{Ticks} \quad \text{(B.5)}$$

Applying this maximum on-time to the inequality described by (B.3), the inequality can be simplified and solved as follows,

$$2^{B_v}b_{v0}(5.71)(3244) + 2^{B_v}b_{v1}(5.71)(3244) + 2^{B_v}b_{v2}(5.71)(4095-3244) + \ldots$$
$$2^{B_v}a_{v1}(2400) + 0 < 2^{31}-1$$

$$2^{B_v} < \frac{2^{31}-1}{(5.71)(3244)(b_{v0}+b_{v1}) + (4095-3244)b_{v2} + a_{v1}(2400)}$$

$$B_v < \log_2\left(\frac{2^{31}-1}{(5.71)(3244)(b_{v0}+b_{v1}) + (4095-3244)b_{v2} + a_{v1}(2400)}\right)$$

$$B_v < \log_2\left(\frac{2^{31}-1}{(5.71)(3244)(0.01847+0.0001436) + (-851)(-0.01832) + 1.956(2400)}\right)$$

$$B_v < 18.7 \quad \text{(B.6)}$$

A similar inequality to that described in (B.3), which determines the condition to prevent positive integer overflow, can be derived to obtain the values of B_v which prevent negative integer overflow as follows

$$\min\langle B_{v0}k_v(H_v v_{ref} - H_v v_o[n])\rangle + \min\langle B_{v1}k_v(H_v v_{ref} - H_v v_o[n-1])\rangle + \ldots$$
$$\min\langle B_{v2}k_v(H_v v_{ref} - H_v v_o[n-2])\rangle + \min\langle 2^{B_v}a_{v1}t_{on(ticks)}[n]\rangle + \ldots$$
$$\min\langle 2^{B_v}a_{v2}t_{on(ticks)}[n-1]\rangle > -2^{31} \quad \text{(B.7)}$$

This inequality can be simplified and solved thusly

$$2^{B_v}(b_{v0}+b_{v1})(5.71)(3244-4095) + 2^{B_v}b_{v2}(5.71)(3244) + 0 + 2^{B_v}a_{v2}(2500) > -2^{31}$$

$$2^{B_v} < \frac{-2^{31}}{(5.71)(3244-4095)(b_{v0}+b_{v1})+(5.71)(3244)b_{v2}+(2500)a_{v2}}$$

$$B_v < \log_2\left(\frac{-2^{31}}{(5.71)(3244-4095)(b_{v0}+b_{v1})+(5.71)(3244)b_{v2}+(2500)a_{v2}}\right)$$

$$B_v < \log_2\left(\frac{-2^{31}}{(5.71)(3244-4095)(0.01861)+(5.71)(3244)(-0.01832)+(2500)(-0.9555)}\right)$$

$$B_v < 19.53 \qquad \therefore \qquad B_v = 18 \tag{B.8}$$

The term B_v was set to $B_v = 18$, to satisfy both inequalities defined by (B.6) and (B.8).

The term A_v is set as high as possible in order to reduce the quantization error of the filter coefficients a_{v1} and a_{v2}, but not excessively high as to cause unwanted computational error due to integer rounding. It is possible to calculate the effect of the coefficient quantization error on the voltage compensator's magnitude and phase response by substituting the filter coefficients b_{v0}, b_{v1}, b_{v2}, a_{v1} and a_{v2}, for the scaled and rounded coefficients B_{v0}, B_{v1}, B_{v2}, A_{v1} and A_{v2}. Therefore, the voltage-controller transfer function can be re-written as follows

$$C_v(z) = 2^{A_v - B_v}\frac{B_{v0}+B_{v1}z^{-1}+B_{v2}z^{-2}}{2^{A_v}-A_{v1}z^{-1}-A_{v2}z^{-2}} \tag{B.9}$$

Figure B.2 shows the controller transfer function calculated at three different values of A_v, as well as the ideal transfer function with no coefficient-quantization error calculated using (2.28). It can be seen from the figure that as the value of A_v is increased, the controller's magnitude response becomes closer to the ideal response, and that setting the term A_v to equal 10 provides a good match between the controller's actual response and the ideal response. Hence, this value is used for A_v.

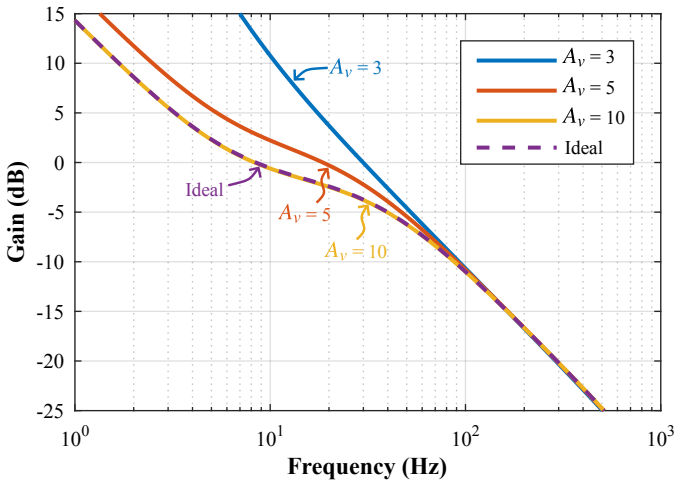


Figure B.2. Voltage compensator magnitude variation with A_v.

Table B.1 gives a full-list of the voltage compensator fixed-point coefficients, that are used in microcontroller software to define the fixed-point recursive algorithm that implements

the controller.

TABLE B.1
VOLTAGE CONTROLLER FIXED-POINT COEFFICIENTS

Parameter	Value
Input voltage adc-sensor gain, H_v	8.11
Coefficient, A_k	16
Coefficient, B_v	18
Coefficient, A_v	10
Coefficient, B_{v0}	4841
Coefficient, B_{v1}	38
Coefficient, B_{v2}	-4803
Coefficient, A_{v1}	2002
Coefficient, A_{v2}	-978

B.2 Notch Filter Design with Fixed-Point Math

The terms A_n, B_n and A_x must be defined in order to complete the design of the filter at a single line frequency. Therefore, the coefficients described by (2.53) can be defined. If B_n is set too low, the filter coefficients B_{n1}, B_{n2} and B_{n2} suffer from quantization error from the rounding function of (2.53). However, using too-high a value for B_n causes integer overflow to occur, which results in undesired filter behaviour. Thus, B_n must be set to the highest possible value, where integer overflow does not occur. An inequality can be derived for the necessary conditions to prevent positive integer overflow of any notch filter variable by summing the output of all notch filter gain blocks in Figure B.3, and ensuring this summed value is less than $2^{31}-1$. Hence, the following inequality must be satisfied to prevent positive integer overflow.

$$\begin{aligned}&\max\left\langle B_{n0}x_n[n]\right\rangle + \max\left\langle B_{n1}x_n[n-1]\right\rangle + \max\left\langle B_{n2}x_n[n-2]\right\rangle + ... \\ &\quad \max\left\langle 2^{B_n+A_x}a_{n1}t_{on(ticks)}[n-1]\right\rangle + \max\left\langle 2^{B_n+A_x}a_{n2}t_{on(ticks)}[n-2]\right\rangle < 2^{31}-1 \end{aligned} \quad \text{(B.10)}$$

Given that $x_n[n] \approx 2^{A_x}t_{on(ticks)}[n]$, we can write $\max\left\langle B_{n0}x_n[n]\right\rangle \approx 2^{A_x}2^{B_n}b_{n0}\max\left\langle t_{on(ticks)}[n]\right\rangle \approx 2^{A_x}2^{B_n}b_{n0}(2400\text{ Ticks})$. By applying the same logic to the other terms, the inequality can be simplified and solved as follows

$$2^{A_x}2^{B_n}b_{n0}(2400)+0+2^{A_x}2^{B_n}b_{n0}(2400)+2^{A_x}2^{B_n}a_{n1}(2400)+0<2^{31}-1$$

$$2^{A_x}2^{B_n}(2400)(b_{n0}+b_{n2}+a_{n1})<2^{31}-1$$

$$2^{A_x}2^{B_n}<\frac{2^{31-1}}{(2400)(b_{n0}+b_{n2}+a_{n1})}$$

$$B_n<\log_2\left(\frac{2^{31}-1}{(2^{12}-1)(b_{n0}+b_{n2}+a_{n1})}\right)-A_x$$

$$B_n<\log_2\left(\frac{2^{31}-1}{(2^{12}-1)(1.027+1.027+1.925)}\right)-A_x$$

$$B_n<17.7-A_x \quad \text{(B.11)}$$

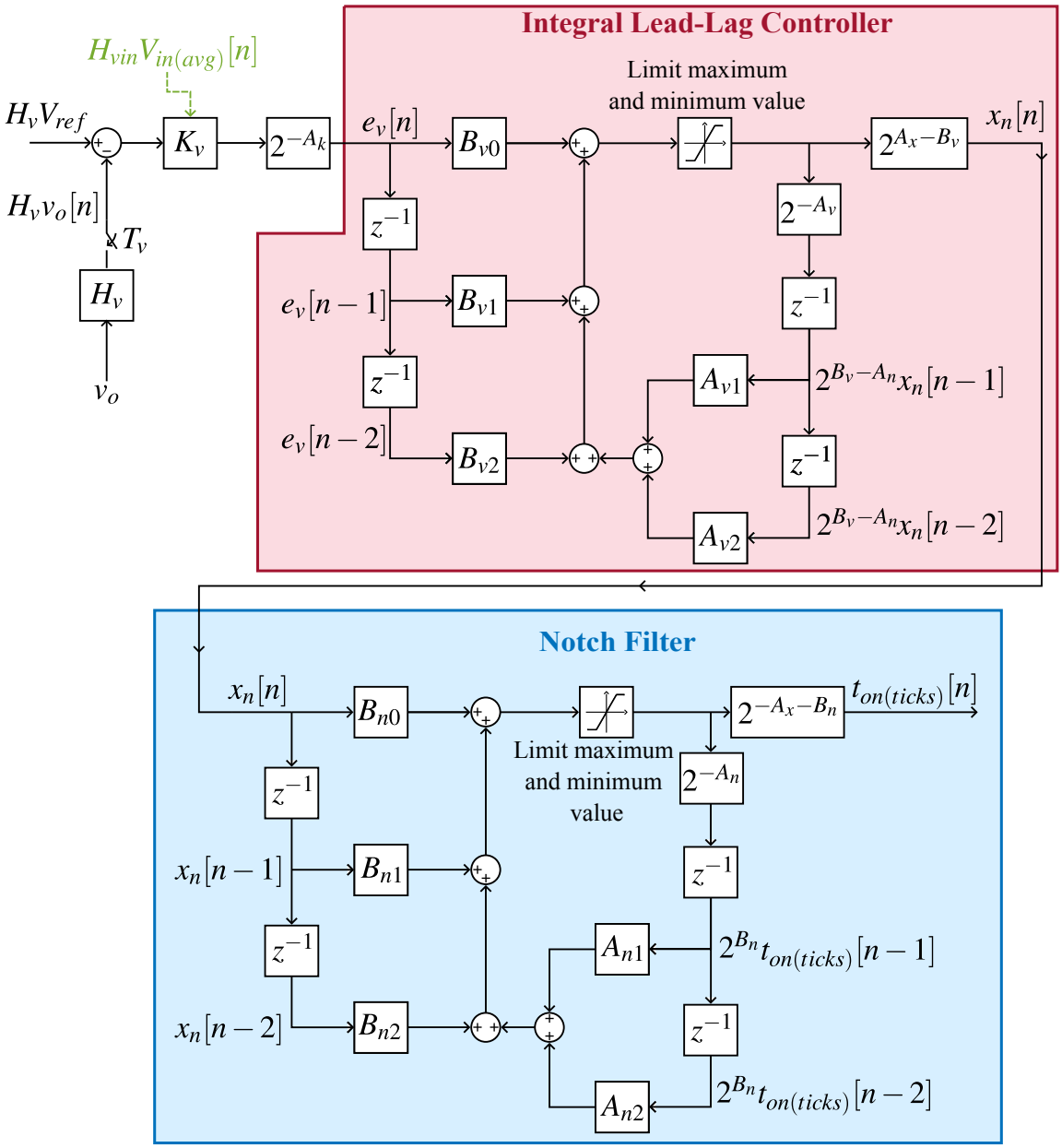


Figure B.3. Notch filter block diagram for a fixed-point implementation.

A similar analysis is performed to check that no variable of the filter can overflow negatively. This results in the following inequality.

$$\min\langle B_{n0}x_n[n]\rangle + \min\langle B_{n1}x_n[n-1]\rangle + \min\langle B_{n2}x_n[n-2]\rangle + \ldots$$
$$\min\langle 2^{B_n+A_x}a_{n1}t_{on(ticks)}[n-1]\rangle + \min\langle 2^{B_n+A_x}a_{n2}t_{on(ticks)}[n-2]\rangle > -2^{31} \quad \text{(B.12)}$$

Given that $x_n[n] \approx 2^{A_x}t_{on(ticks)}[n]$, the minimum possible input to the notch filter is equal to the minimum possible value for the on-time, which is zero. Hence, as the the coefficient $B_{n0} > 0$, the term $\min\langle B_{n0}x_n[n]\rangle$ simplifies to $2^{A_x}2^{B_n}b_{n0}min\langle t_{on(ticks)}[n]\rangle$, which equals zero. The coefficient B_{n1} on the other hand is negative. Therefore, the term $\min\langle B_{n1}x_n[n-1]\rangle$ simplifies to $2^{A_x}2^{B_n}b_{n1}\max\langle t_{on(ticks)[n]} >= 2^{A_x}2^{B_n}b_{n1}(2400\,\text{Ticks})$. Applying the same logic

to the other terms in the inequality, the inequality can be simplified and solved as follows

$$0+2^{A_x}2^{B_n}b_{n1}(2400)+0+0+2^{A_x}2^{B_n}a_{n2}(2400)>-2^{31}$$

$$2^{A_x}2^{B_n}(2400)(b_{n1}+a_{n2})>-2^{31}$$

$$2^{A_x}2^{B_n}<\frac{-2^{31}}{(2400)(b_{n1}+a_{n2})}$$

$$B_n<\log_2\left(\frac{-2^{31}}{(2400)(b_{n1}+a_{n2})}\right)-A_x$$

$$B_n<18.2-A_n \qquad \therefore \qquad B_n=17-A_x \tag{B.13}$$

Therefore, to satisfy both inequalities, the term B_n can be calculated as a function of A_x by $B_n=17-A_x$.

The term A_x must be set as high as possible to reduce computational error, but not excessively high as to cause excessive quantization error when coefficients B_{n0}, B_{n1} and B_{n2} are calculated, by scaling and rounding the coefficients b_{n0}, b_{n1} and b_{n2}. The effect of this error can be seen by re-calculating the notch-filter transfer function given in (2.50), but using the fixed-point coefficients B_{n0}, B_{n1}, B_{n2} instead of the filter coefficients b_{n0}, b_{n1}, b_{n2}. Therefore, the notch filter's transfer function can be re-written as

$$H_n(z)=2^{-B_n}\frac{B_{n0}+B_{n1}z^{-1}+B_{n2}z^{-2}}{1-a_{n1}z^{-1}-a_{n2}z^{-2}} \tag{B.14}$$

The magnitude response defined by (B.14) is calculated using different values of A_x, and compared to the ideal magnitude response with no coefficient-quantization error, defined by (2.50). This comparison is shown in Figure B.4 for three different values of A_x. It can be seen from the figure that if A_x is set too high, such as when $A_x=8$, or $A_x=6$, there is excessive quantization error. Whereas, when $A_x=4$ there is a strong match to the filter's ideal response. Hence, A_x was set to 4, and B_n was set to 13. Similarly, the term A_n must be set has high as possible to reduce the quantization error of the filter coefficients A_{n1} and A_{n2}, but not excessively high to cause unwanted computational error due to integer rounding from right-shift bit operations. It is possible to calculate the effect of the coefficient quantization error on the controller's magnitude and phase response by substituting the filter coefficients a_{n1} and a_{n2}, for the scaled and rounded coefficients A_{n1} and A_{n2}. Therefore, the voltage controller transfer function can be re-written as follows

$$H_n(z)=2^{A_n-B_n}\frac{B_{n0}+B_{n1}z^{-1}+B_{n2}z^{-2}}{2^{A_n}-A_{n1}z^{-1}-A_{n2}z^{-2}} \tag{B.15}$$

The most-suitable value for A_n is determined by plotting the magnitude response of the filter

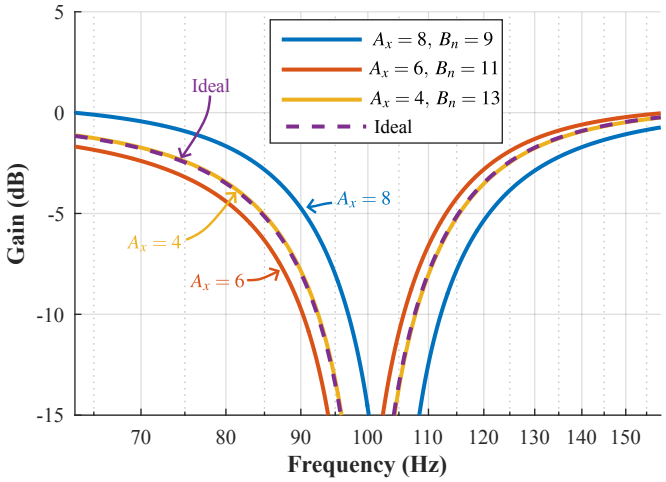


Figure B.4. Notch-filter magnitude response variation with A_x.

transfer function defined in (B.15) for different values of A_n, and comparing to the ideal transfer function with no quantization-coefficient error. Figure B.5 demonstrates when A_n is set to $A_n = 5$ or $A_n = 9$ there is a large mismatch between the actual filter's response and the ideal response. Setting the term A_n to 11, results in very strong match between the ideal and actual magnitude response. Thus, this value is used for A_n.

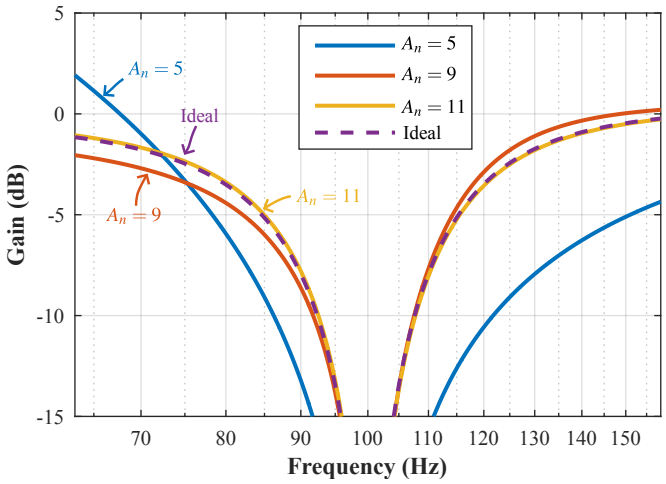


Figure B.5. Notch-filter magnitude response variation with A_n.

With the terms A_n and B_n now defined, it is possible to calculate the fixed-point notch filter coefficients using (2.53). A full list of all notch filter fixed-point coefficients is presented in Table B.2.

TABLE B.2
NOTCH-FILTER FIXED-POINT COEFFICIENTS

Parameter	Value
Coefficient, A_x	4
Coefficient, B_n	13
Coefficient, A_n	11
Coefficient, B_{n0}	8414
Coefficient, B_{n1}	-16695
Coefficient, B_{n2}	8414
Coefficient, A_{n1}	3942
Coefficient, A_{n2}	-1927

APPENDIX C

MATH DERIVATIONS

(4.7) and (4.13) are derived by solving characteristic equation of Fig 4.3when operating in Mode 2. The characteristic equation for the circuit in this mode of operation is given by

$$LC_{ds}\frac{d^2v_{ds}}{dt^2}+v_{ds}=v_{in} \tag{C.1}$$

The characteristic equation can be solved by first solving the homogeneous solution $v_{ds}^h(t)$, by setting the right-hand side of (C.1) equal to zero, and then solving for a particular solution $v_{ds}^p(t)$, that satisfies (C.1). The voltage $v_{ds}(t)$ can then be found by

$$v_{ds}(t)=v_{ds}^p(t)+v_{ds}^h(t) \tag{C.2}$$

To solve the homogenoeous solution, we must find a suitable equation for $v_{ds}^h(t)$, that satisfies

$$LC_{ds}\frac{d^2v_{ds}^h}{dt^2}+v_{ds}^h=0 \tag{C.3}$$

If we let $v_{ds}^h=A\sin(\omega_r(t-t_{on})+\theta)$, where A and θ are constants, the second derivative of v_{ds}^h can be calculated as

$$\frac{d^2v_{ds}^h}{dt^2}=-\omega_r^2A\sin(\omega_r(t-t_{on})+\theta) \tag{C.4}$$

Substituting these expressions for v_{ds}^h and its second derivative into (C.3) we get

$$-LC_{ds}\omega_r^2A\sin(\omega_r(t-t_{on})+\theta)+A\sin(\omega_r(t-t_{on})+\theta)=0$$

$$\therefore \qquad LC_{ds}\omega_r^2=1$$

$$\therefore \qquad \omega_r=\frac{1}{\sqrt{LC_{ds}}}$$

Since this expression for v_{ds}^h satisfies (C.3), it can be used as the homogeneous solution. Next, to calculate v_{ds}, the calculation of a particular solution that satisfies (C.1) is required. We will try $v_{ds}^p=B$, where B is a constant, therefore $\frac{d^2v_{ds}^p}{dt^2}=0$. Substituting this value of v_{ds}^p

into (C.1), we get

$$LC_{ds}\frac{d^2B}{dt^2}+B=v_{in}$$

$$\therefore \qquad B=v_{in} \tag{C.5}$$

Hence, by substituting the expressions obtained for the homogeneous solution and particular solution into (C.2), the following expression is obtained to describe v_{ds}.

$$v_{ds}(t)=v_{in}+A\sin(\omega_r(t-t_{on})+\theta) \tag{C.6}$$

This equation can be used to derive both (4.7) and (4.13), by applying the appropriate initial conditions, and solving for the values of A and θ.

C.1 Solving (4.7)

To solve (4.7) the following initial conditions can be used,

$$v_{ds}(t_{on})=0 \tag{C.7}$$

$$i_L(t_{on})=\frac{v_{in}t_{on}}{L} \tag{C.8}$$

First, by applying the drain-source-voltage initial condition to (C.13) the following expression can be obtained to describe the constants θ and A

$$v_{ds}(t_{on})=v_{in}+A\sin(\omega_r(t_{on}-t_{on})+\theta)=0$$

$$\therefore \qquad A\sin(\theta)=-v_{in} \tag{C.9}$$

Next, since $i_L=C_{ds}\frac{dv_{ds}}{dt}$, the inductor-current initial condition can be used to find a second expression describing θ and A, as follows

$$i_L(t_{on})=C_{ds}\frac{dv_{ds}}{dt}\bigg|_{t_{on}}=\omega_rC_{ds}A\cos(\omega_r(t_{on}-t_{on})+\theta)=\frac{v_{in}t_{on}}{L}$$

$$\therefore \qquad A\cos(\theta)=\omega_rt_{on}v_{in} \tag{C.10}$$

There are now two equations, (C.9) and (C.10), and two unknowns A and θ. The two equations can be solved for A by squaring both and using the trigonometric identity $\cos^2(\theta)+\sin^2(\theta)=1$.

$$A^2\cos^2(\theta)+A^2\sin^2(\theta)=(v_{in}\omega_rt_{on})^2+v_{in}^2$$

$$A^2 = v_{in}^2(1+(\omega_r t_{on})^2)$$

$$\therefore \qquad A = v_{in}\sqrt{1+(\omega_r t_{on})^2} \tag{C.11}$$

Similarly both equations can be used to solve for θ by dividing one by the other, and using the trigonometric identity $\tan(\theta) = \frac{\sin(\theta)}{\cos\theta}$.

$$\frac{A\sin(\theta)}{A\cos(\theta)} = \frac{-v_{in}}{\omega_r t_{on} v_{in}}$$

$$\tan(\theta) = \frac{-1}{\omega_r t_{on}}$$

$$\therefore \qquad \theta = \tan^{-1}\left(\frac{-1}{\omega_r t_{on}}\right) \tag{C.12}$$

Substituting the values for A obtained in (C.11) into (4.7), and using the value for θ obtained in (C.12) , results in full solution to describe vds.

$$v_{ds}(t) = v_{in} + v_{in}\sqrt{1+(\omega_r t_{on})^2}\sin(\omega_r(t-t_{on})+\theta) \tag{C.13}$$

The current i_L can be derived using $i_L = C_{ds}\frac{dv_{ds}}{dt}$.

$$i_L(t) = \omega_r v_{in} C_{ds}\sqrt{1+(\omega_r t_{on})^2}\cos(\omega_r(t-t_{on})+\theta) \tag{C.14}$$

The expressions defined by (C.13) and (C.14) are identical to the equation given in (4.7).

C.2 Solving (4.13)

(4.7) can also be solved using (C.13), but it is easier if the expression is re-written by replacing the term $(t-t_{on})$ with $(t-t_3)$, so that

$$v_{ds}(t) = v_{in} + A\sin(\omega_r(t-t_3)+\theta) \tag{C.15}$$

Since (4.7) is used to define the waveshape of v_{ds} and i_L in the region between t_3 and t_4, the following initial conditions are used to solve for the terms A and θ.

$$v_{ds}(t_3) = v_o \tag{C.16}$$

$$i_L(t_3) = 0 \tag{C.17}$$

If the inductor-current initial condition is first applied to (C.15) we get

$$i_L(t_3) = C_{ds}\frac{dv_{ds}}{dt}\bigg|_{t_3} = \omega_r C_{ds} A\cos(\omega_r(t_3 - t_3) + \theta) = 0$$

$$\therefore \qquad \cos(\theta) = 0$$

$$\therefore \qquad \theta = \frac{\pi}{2} \tag{C.18}$$

Substituting this value for θ into (C.15) we get

$$v_{ds}(t) = v_{in} + A\sin(\omega_r(t - t_3) + \pi/2)$$

$$\therefore \qquad v_{ds}(t) = v_{in} + A\cos(\omega_r(t - t_3))$$

The term A can be solved by applying the drain-source initial condition to (C.2).

$$v_{ds}(t_3) = v_{in} + A\cos(\omega_r(t_3 - t_3)) = v_o$$

$$\therefore \qquad A = v_o - v_{in} \tag{C.19}$$

Substituting this value of A into (C.2) gives the fully-defined solution for the drain-source voltage.

$$v_{ds}(t) = v_{in} + (v_o - v_{in})\cos(\omega_r(t - t_3)) \tag{C.20}$$

The inductor current can be sloved for by taking the derivative of the drain-source voltage. Hence

$$i_L(t) = C_{ds}\frac{dv_{ds}}{dt} = -\omega_r C_{ds}(v_o - v_{in})\sin(\omega_r(t - t_3)) \tag{C.21}$$

The two equations defined by (C.20) and (C.21) are identical to the expression given in (4.13)